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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNIFIED 1008

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *June 7, 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/27/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on July 27, 2007 was filed after the mailing date of the application on June 12, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Arguments

2. Applicant's arguments, see pages 8-11, filed June 7, 2007, with respect to the claim objection and the 35 U.S.C. 101 rejections have been fully considered and are persuasive. The objection to Claim 25 and the 35 U.S.C. 101 rejections of Claims 20-22 have been withdrawn.

3. Applicant's arguments with respect to claims 1-7, 10-22, 24, and 25 have been considered but are moot in view of the new ground(s) of rejection.

4. Applicant's arguments, see pages 12-13, filed June 7, 2007, with respect to the rejection(s) of claim(s) 1-5, 7, 10, 12-16, 18, 20-22, 24, and 25 under 35 U.S.C. 102(b) and claims 6, 11, 17, and 19 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Perego (US006864896B2).

5. Applicant argues that Kelleher (US005794016A) does not teach "a memory controller coupled to the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory" (pages 12-13).

In reply, new grounds of rejection are made in view of Perego.

6. As per Claim 25, Applicant argues that Kelleher teaches that each block is square. Since Kelleher does not teach any blocks that are not square, and therefore does not teach a region that includes NxM number of pixels (page 14).

In reply, the Examiner points out that Claim 25 does not recite that N is not equal to M. Therefore, N can be equal to M. New grounds of rejection are made in view of Perego, which more clearly teaches Applicant's disclosed invention. Even if N does not equal to M, Perego teaches that each region is rectangular (c. 5, ll. 23-25).

7. Applicant's arguments filed June 7, 2007 with respect to Claim 24 have been fully considered but they are not persuasive.

8. As per Claim 24, Applicant argues that Kelleher discloses multiple processors 20, each of which may have its own front end circuitry and a scan converter. Kelleher does not disclose a first and a second scan converter both coupled to the front end circuitry (pages 13-14).

In reply, Examiner disagrees. Kelleher teaches first and second scan converter (update stage, Fig. 7 in 20A and 20B, Fig. 3) both coupled to front end circuitry 14 (c.8, ll. 32-c. 9, ll. 4).

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-4, 7, 10, 12, 14, 20-22, and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Perego (US006864896B2).

11. As per Claims 1 and 25, Perego teaches graphics processing circuit (300, Fig. 3; Col. 3, ll. 61-63) having at least two graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two graphics pipelines operative to process data in a dedicated tile (c. 5, ll. 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least two graphics pipelines (312), operative to transfer pixel data between each of first pipeline and second pipeline and shared memories (314) (c. 3, ll. 65-67; c. 4, ll. 1-10, 48-65). The shared memories (314) are each part of the main memory (c. 1, ll. 44-54; c. 3, ll. 3-6), and therefore are considered to be one memory. The repeating tile pattern includes a horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (c. 5, ll. 19-27, 38-44).

12. As per Claim 2, Perego discloses that the square regions comprise a two dimensional partitioning of memory (c. 5, ll. 19-33).

13. As per Claim 3, Perego discloses that the memory is a frame buffer (c. 5, ll. 32-33).

14. As per Claim 4, Perego discloses that each of at least two graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process a portion of pixel data (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44). In order for the front end circuitry (308) to generate pixel data, it must inherently receive vertex data.

15. As per Claim 7, Perego teaches the at least two graphics pipelines (312, Fig. 3) separately receive the pixel data from the front end circuitry (308) (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44).

16. As per Claim 10, Perego discloses that a first of the at least two graphics pipelines (first rendering engine of 312, Fig. 3) processes the pixel data only in a first set of tiles (tiles labeled "RE0" in Fig. 5) in the repeating tile pattern (c. 5, ll. 23-44).

17. As per Claim 12, Perego discloses that a second of the at least two graphics pipelines (second rendering engine of 312, Fig. 3) processes the pixel data only in a second set of tiles (tiles labeled "RE1" in Fig. 5) in the repeating tile pattern (c. 5, ll. 23-44).

18. As per Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Perego teaches four graphics pipelines (c. 5,.ll. 41-44). So Claim 14 is rejected under the same rationale as Claims 4 and 10.

19. As per Claim 20, Perego teaches a graphics processing method, comprising generating pixel data (c. 5, ll. 19-25), which is inherently generated in response to received vertex data; determining pixels within set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of at least two graphics pipelines (312, Fig. 3) in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines (c. 5, ll. 19-44); and transmitting the processed pixels to a memory controller (310), wherein the at least two graphics pipelines share the memory controller (c. 3, ll. 65-c. 4, ll. 25; c. 5, ll. 31-44).

20. As per Claim 21, Perego discloses that determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for (c. 5, ll. 19-50).

21. As per Claim 22, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed comprises providing position coordinates of pixels within determined set of tiles to be processed to corresponding one of at least two graphics pipelines (c. 5, ll. 19-44).

Thus, it reasonably appears that Perego describes or discloses every element of Claims 1-4, 7, 10, 12, 14, 20-22, and 25 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

22. The text of those sections of Title 35, U.S. Code 103(a) not included in this action can be found in a prior Office action.

23. Claims 5, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Kelleher (US005794016A).

24. As per Claim 5, Perego is relied upon for the teachings as discussed relative to Claim 4.

However, Perego does not explicitly teach that at each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry. However, Kelleher discloses that each of the at least two graphics pipelines (20A, 20B, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) further includes a scan converter (update stage, Fig. 7), coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry (c. 8, ll. 52-61; c. 9, ll. 1-23; c. 6, ll. 26-28).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Perego so that at each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry as suggested by Kelleher

because Kelleher suggests that the scan converters are needed in order to define the image data as an array of pixels by calculating the pixel addresses (c. 9, ll. 1-23), as is well-known in the art.

25. As per Claim 18, Perego does not teach a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines. However, Kelleher discloses a bridge (38, Fig. 3) operative to transmit vertex data to each of the first (20A), second (20B), third (20C) and fourth (20N) graphics pipelines (c. 3, ll. 22-23; c. 4, ll. 9-14; c. 8, ll. 56-65; c. 3, ll. 46-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego to include a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines as suggested by Kelleher because Kelleher suggests the advantage of being able to convert the vertex data to pixel data in parallel, which increases the efficiency of the graphics system (c. 2, ll. 31-35; c. 8, ll. 56-65; c. 9, ll. 1-23).

26. As per Claim 24, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63), having front end circuitry (308) operative to generate pixel data in response to primitive data for primitive to be rendered (c. 5, ll. 19-23); first back end circuitry (first rendering engine 312), coupled to front end circuitry 308, operative to process first portion of pixel data (labeled "RE0" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by first back end circuitry, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; second back end circuitry (second rendering engine 312), coupled to front end circuitry 308, operative to process second portion of pixel data (labeled "RE1" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by second back end circuitry (c. 3, ll. 63-c. 4, ll. 2; c. 5, ll. 19-44);

and memory controller (310), coupled to first and second back end circuitry (312) operative to transmit and receive processed pixel data (c. 3, ll. 65-67; c. 4, ll. 1-53; c. 5, ll. 32-44).

However, Perego does not explicitly teach a first scan converter and a second scan converter. However, Kelleher discloses a first scan converter, coupled between the front end circuitry (14, Fig. 3) and the first back end circuitry (update stage, Fig. 7 in 20A, Fig. 3), operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23), and operative to provide the position coordinates to the first back end circuitry in response to the pixel data (c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38); a second scan converter, coupled between the front end circuitry and the second back end circuitry (update stage, Fig. 7 in 20B, Fig. 3), operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23; c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38). This would be obvious for the same reasons given in the rejection for Claim 5.

27. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1).

28. As per Claim 6, Perego is relied upon for the teachings as discussed relative to Claim 1.

However, Perego does not explicitly teach that each tile of the set of tiles further comprises a 16x16 pixel array. However, Furtner describes that each tile of the set of tiles further comprises a 16x16 pixel array (c. 11, ll. 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Perego so that each tile of the set of tiles further comprises a

16x16 pixel array as suggested by Furtner because Furtner suggests that depending on the number of parallel image-rendering pipelines and depending on the memory organization, the optimum tile size and shape can be selected (c. 11, ll. 45-48, 64-65), and therefore it would be obvious to modify the tile size to be 16x16 pixels if that would be the optimum tile size for a particular number of parallel image-rendering pipelines and particular memory organization.

29. As per Claim 17, Perego does not teach 3rd and 4th graphics pipelines are on separate chips. However, Furtner teaches 3rd and 4th pipelines are on separate chips (c. 6, ll. 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Perego so that pipelines are on separate chips as suggested by Furtner because Furtner suggests that this makes the system more configurable by being able to easily add more graphics pipelines to increase the performance (c. 6, ll. 29-30, 42-51).

30. Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Kelleher (US005794016A), further in view of Hamburg (US005905506A).

Perego is relied upon for the teachings as discussed relative to Claim 10.

However, Perego does not explicitly teach a scan converter. However, Kelleher discloses that the first of the at least two graphics pipelines (20A, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) further includes a scan converter (84, Fig. 7), coupled to the front end circuitry (80, 82) and the back end circuitry (c. 8, ll. 52-c. 9, ll. 23). The scan converter determines which groups of blocks 52 within the graphics memory 22 are allocated to and controlled by the graphics pipelines (c. 8, ll. 52-65; c. 6, ll. 26-28). The graphics memory is partitioned into a plurality of pixel blocks that are tiled in the x-and y-direction of the graphics memory (c. 4, ll. 60-62).

Therefore, the scan converter is inherently operative to provide memory addresses or position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry. This would be obvious for the same reasons given in the rejection for Claim 5.

However, Perego and Kelleher do not explicitly teach using tile identification data to indicate which tiles are to be processed. However, Hamburg discloses a pixel identification line for receiving tile identification data indicating which tiles are to be processed (c. 5, ll. 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Perego and Kelleher to include using tile identification data to indicate which tiles are to be processed as suggested by Hamburg because Hamburg suggests the advantage of using tile identification data to easily track the storage locations of the tile pixel data and being able to easily retrieve data for a particular image tile (c. 1, ll. 46-54).

31. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) and Furtner (US006778177B1) in view of Kent (US 20030164830A1).

Perego and Furtner are relied upon for the teachings discussed relative to Claim 17. Perego teaches data includes a polygon (c. 5, ll. 19-23). Furtner teaches third and fourth graphics pipelines are on separate chips (c. 6, ll. 47-51), as discussed in the rejection for Claim 17.

However, Perego and Further do not teach creating a bounding box around the polygon and each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one. However, Kent discloses that the graphics pipeline [0006] calculates the bounding box of the primitive and testing this against the VisRect. If the bounding box of the primitive is contained

in the other P10's super tile the primitive is discarded at this stage [0129]. A primitive can be a polygon [0088]. The method used is to calculate the distance from each subpixel sample point in the point's bounding box to the point's center and compare this to the point's radius. Subpixel sample points with a distance greater than the radius do not contribute to a pixel's coverage. The cost of this is kept low by only allowing small radius points hence the distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within the bounding box [0144]. Since the method calculates the distance from each subpixel sample point in the point's bounding box, this must include all the corners of the bounding box. Therefore, Kent discloses that the data includes a polygon and that the graphics pipeline creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to the graphics pipeline and wherein if the bounding box does not overlap any of the super tiles, then the processing circuit rejects the whole polygon and processes a next one. .

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Perego and Furtner to include a bounding box as suggested by Kent because Kent suggests the advantage of processing the super tiles one at a time in order to hide the page break costs [0129, 0051].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

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