**Stephen W. Melvin, Ph.D.**

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## EDUCATION

**Ph.D., Computer Science**, University of California, Berkeley**,** May 1991.
Research Areas: High-performance computer architecture and microarchitecture (exploiting fine-grained parallelism in general purpose programs through a combination of hardware and software techniques); Microcode-based system performance analysis tools.
Minor Areas: Statistics, Computer Theory

**B.S. (with high honors), Electrical Engineering and Computer Science,** University of California, Berkeley**,** May 1982.

## WORK EXPERIENCE

August 1983 – Present, **President, Zytek Communications Corporation**
Founded Zytek as an engineering, consulting and small-scale manufacturing company. Zytek currently provides consulting services related to intellectual property litigation and licensing, patent prosecution as well as services related to the design, implementation and testing of embedded systems. Zytek's general areas of activity have also included source code analysis and comparison, forensic hard disk analysis and file recovery, industrial control and measurement, Internet related services and computer engineering research services.

January 2014 - December 2015, **President, Stage Innovations, Inc.**
Formed Stage Innovations to hold and develop patents in the area of Internet based voice messaging and fax and email notification. Prosecuted multiple patent applications to issuance and successfully negotiated a sale of the entire portfolio.

August, 2002 – October 2005, **Patent Agent and Technical Advisor, O'Melveny & Myers LLP**
Assistance with a broad range of intellectual property cases, including patent, copyright and trade secret litigation, patent licensing and due diligence. Prior art research, patent validity and infringement analysis, source code comparison, forensic hard disk analysis. Preparation and prosecution of patents in different areas of technology.

May 2001 – August 2002, **Founder and Chief Architect, FlowStorm, Inc.**
Defined and guided the overall chip architecture for a new packet processor. Managed a group of RTL designers to develop working RTL code for the processing core, packet management and interconnect blocks. Developed verification strategy and worked with performance analysis and software groups.

March 2000 - May 2001, **Senior Architect, Clearwater Networks (formerly XStream Logic, Inc.)**
Helped define the architecture and microarchitecture of the XStream network processor. Worked with a team of design engineers to evaluate tradeoffs in microarchitecture, directed design choices to balance tradeoffs in performance and cost. Documented the architecture and worked with software engineers to analyze performance and develop software.

July 1999 – July 2002, **Consulting Engineer, Adroit Engineering, Inc.**
Development of hardware and firmware for optical headlight alignment system for Ford Motor Company. Analog and digital circuit design, firmware engineering, calibration and testing.

September 1998 - December 1998, **Consulting Engineer, HaL Computer Systems, Inc.**
Analysis and testing of cycle by cycle simulator of new SPARC based microprocessor. Validation of results and comparison with microarchitecture definition.

June 1988 - October 1997, **Consulting Engineer, Talking Technology, Inc.**
Designed a microprocessor-based voice mail telecommunications board for the IBM PC bus, including circuit design, firmware development for two on-board microcontrollers and host level software. Continued long-term maintenance of the firmware, which includes proprietary, voice compression and call progress algorithms.

June, 1986 - January, 1995, **Consulting Engineer, American Diversified Silver, Inc**
January, 1995 - December, 1995, **Consulting Engineer, Academy Corporation**
January, 1996 - July, 1996, **Consulting Engineer, SafetyKleen Corporation**
Designed a stand-alone microprocessor-based control unit for efficiently electroplating silver from photochemical solutions, including digital and analog circuit design, printed circuit board layout and the development of microcontroller firmware. Experimentation to measure electrochemical cell characteristics and development of new algorithms for adjusting plating voltage. Adaptation of this unit to high volume batch processing applications. Diagnosis and repairs of failed units.

September 1991 - July 1995, **Consulting Engineer, HaL Computer Systems, Inc.**
Assisted in advanced microarchitecture research on a new implementation of the SPARC architecture, including performance modeling and simulation. Maintenance and enhancement of microarchitecture level and architecture level simulation tools.

June 1985 - September 1987, **Consulting Engineer, Adroit Engineering, Inc.**
Development of software algorithms for a machine vision application involving the analysis of captured video images in a manufacturing process.

June, 1986 - December, 1987, **Consulting Engineer, Digital Equipment Corporation**
Consulting for the High Performance Advanced Development Group in Marlboro on VAX 8600 microcode and the application of out-of-order execution concepts to the VAX architecture. Development of special purpose VAX 8600 microcode and porting and improvement of an HPS/VAX microarchitectural simulator.

June, 1984 - September, 1984, **Engineer, Denelcor Corporation**
Investigation of the design of architecture to follow the HEP-1 and HEP-2 under the supervision of Dr. Burton Smith. Development of a new architecture, Vulture, allowing higher function unit utilization and incorporating a new method of scheduling register reads and writes in a multiprogrammed pipelined system.

## SELECTED LITIGATION CONSULTING EXPERIENCE

October, 2014 – Present, **Consulting Expert, Samsung Electronics v. NVIDIA Corporation (VAED)**
Analysis of patents, prior art and firmware relating to graphics processor and system-on-chip microarchitectures.

February, 2012 – Present, **Testifying Expert / Consulting Expert, Mentor Graphics Corporation v. EVE-USA, Inc., Emulation and Verification Engineering, S.A., Synopsys, Inc. (OR, CAND, Japan)**
Analysis of patents, prior art and software and firmware technology related to electronic design automation. Declarations for Japan litigation.

August, 2010 – March, 2014, **Testifying Expert, The Quantum World Corporation v. Dell Inc. et al. (TXWD)**
Analysis of patents and prior art relating to true random number generators. Statistical analysis of random data sets.

June, 2010 – May, 2013, **Consulting Expert, Microunity Systems v. Samsung Electronics et al. (TXED)**
Analysis of patents, prior art and firmware relating to processor microarchitecture.

September, 2012 – February, 2013, **Consulting Expert, Walker Digital LLC v. Google Inc. (DE)**
Analysis of patents and software relating to image processing and mapping.

August, 2011 – November, 2012, **Consulting Expert, MobileMedia Ideas LLC v. Apple Inc. (DE)**
Analysis of patents, prior art and software relating to audio data compression.

February, 2011 – April, 2012, **Consulting Expert, Pact XPP Technologies, AG v. Xilinx, Inc. (TXED)**
Analysis of patents, prior art and technology related to programmable logic devices.

April, 2011 – May, 2011, **Testifying Expert, Microsoft Corporation v. Phoenix Solutions, Inc. (CACD)**
Analysis of technology related to speech processing and voice recognition.

January, 2010 – June, 2010, **Testifying Expert, Optimum Processing Solutions, v. AMD et al. (GAND)**
Analysis of patent relating to optically interconnected processing elements. Testimony regarding claim construction.

May, 2009 – October, 2009, **Testifying Expert, Saxon Innovations v. Samsung Electronics (ITC)**
Analysis of patents and prior art relating to interprocessor communication and interrupt masking. Review of source code for cell phones. Testimony at ITC hearing.

January, 2008 – March, 2009, **Testifying Expert, Quantum World Corporation v. Atmel Corp., et al. (TXED)**
Analysis of patents and prior art relating to true random number generators. Statistical analysis of random data sets.

January, 2007 – August, 2009, **Consulting Expert, Fujitsu et al. v. Netgear (CAND)**
Analysis of patents, prior art and technology relating to wireless transmission of multimedia data. Analysis of firmware and RTL for wireless devices, analysis of test results.

March, 2007 – August, 2008, **Testifying Expert, Silicon Image Inc. v. Analogix Semiconductor, Inc. (CAND)**
Analysis of data sheets, product specifications and firmware related to HDMI digital television interface and devices for receiving and processing digital video data.

December, 2006 – November, 2007, **Consulting Expert, Microunity v. Advanced Micro Devices**
Analysis of patents relating to arithmetic computation in a microprocessor architecture. Prior art searching, review and analysis. Claim construction support. Non-infringement and invalidity analysis and support.

May, 2006 – October, 2007, **Transmeta Corporation v. Intel Corporation**
Analysis of patents relating to microprocessor architecture features for low power, data handling and memory address translation. Prior art review and analysis.

December, 2005 – July, 2007, **Consulting Expert, Fujitsu v. Centillium Communications (Japan)**
Analysis of patent related to communications technology. Analysis of ADSL technology and non-infringement support. Prior art searching, review and analysis. Preparation of technical documentation to support Japanese counsel.

June, 2006 – August, 2006, **Biax Corporation v. Philips Semiconductors (ITC)**
Analysis of patents related to microprocessor architecture. Prior art review and analysis.

July, 2001 – October, 2001, **Testifying Expert, Intel v. Via Technologies**
Analysis of patents, AGP specifications, and other documents related to CPU/memory systems and architectures.

October, 1999 - May, 2000, **Testifying Expert, Accton v. Micro Linear Corporation**
July, 1999 - September, 1999, **Testifying Expert, Allied Telesyn v. Micro Linear Corporation**
Analysis of on-chip circuitry, testing procedures and data sheets for Ethernet controller ICs. Analysis of the application of Ethernet controller ICs in hubs and switches, design and testing. Compliance with data sheet and other published specifications.

November, 1998 - March, 1999, **Consulting Expert, Ericsson v. Qualcomm**
Analysis and comparison of firmware source code of cellular telephones relating to copyright and trade secret issues; analysis of documents and meeting notes relating to CDMA technology and the application to cellular handsets and base stations.

August 1998 - December 1998, **Court Appointed Expert, Cadence v. Avant!**
Assisting Northern California Federal District Court Judge Ronald Whyte in understanding issues and technology relating to CAD design software and its alleged copyright infringement and trade secret misappropriation; source code analysis and comparison.

May, 1997 - February, 2000, **Consulting Expert, AMD v. Alliance**
Analysis of transistor-level schematics of Flash EEPROM memory devices, patents and other references in patent infringement case.

June 1998 - December 1998, **Testifying Expert, Canter, et. al. v. West Publishing**
Analysis of source code, proposals, internal documentation and other materials relating to natural language processing of database queries in connection with patent and trade secret misappropriation case.

June 1998 – December 1998, **Testifying Expert, Xircom v. General Patent**
Analysis of patents and other references relating to modem and packaging technology.

May, 1998 - Present, **Testifying Expert, Hilgraeve v. Symantec**
December, 1997 - February, 1998, **Consulting Expert**, **Trend v. Symantec**
Analysis of source code, patents and other references relating to virus checking software. Analysis and operation of virus checking software and development operational tests.

December, 1997 - May, 1998, **Iomega v. Nomai**
Analysis and comparison of microcode for disk drive microprocessors and ASICs relating to copyright and trade secret issues. Review of ASIC specification sheets and analysis of empirically derived firmware sequences.

September 1997 - October 1997, **Consulting Engineer, Creative Labs, Inc.**
Analysis, testing and reverse engineering of audio processing circuit boards for PC-based applications. Circuit analysis and logic analyzer tracing to determine firmware and hardware operation. Clean room development of encryption software.

June, 1997 - December, 1997, **Sharp Image Gaming**
Analysis and comparison of firmware for video slot machines relating to copyright issues. Review of EPROM contents including images for video display and microprocessor firmware.

March, 1997 - September, 1997, **Diamond Multimedia v. Lans**
Analysis and research relating to video graphics technology. Analysis of patent disclosures, analysis of function and operation of S3 video driver chips.

May 1995 - May 1997, **Testifying Expert, DSC v. DGI**
Analysis and comparison of firmware for a microprocessor-based telecommunications board relating to copyright issues. Testimony regarding source code analysis and concepts and practices in reverse engineering.

March 1996 - November 1996, **Testifying Expert, AMD v. Hyundai**
Analysis of flash EEPROM integrated circuits including analysis of internal circuitry, analysis of product development data and comparison of testing procedures in a trade secret case.

October 1996 - November 1996, **Testifying Expert, Texas Instruments v. Samsung**
Analysis of firmware (ladder logic) for programmable controllers used in assembly lines in a patent infringement case.

May 1995 - April 1996, **Consulting Expert, AMD v. Cypress**
September 1994 - March 1996, **Consulting Expert, AMD v. Altera**
Analysis of transistor-level schematics of integrated circuits, patents and other references in patent infringement analysis.

December 1992 - July 1993, **Testifying Expert, Conner v. Western Digital**
August 1994 to December 1995, **Testifying Expert, IBM v. Conner**
Analysis of the architecture of hard disk drives, including microcontroller firmware analysis, digital and analog circuit analysis, and dynamic testing. Analysis of patents and other references.

June 1991 - October 1992, **Consulting Expert, AMD v. Cypress**
Analysis of transistor-level schematics for a wide variety of CMOS and Bipolar PLD integrated circuits in a patent infringement case.

## TEACHING AND ACADEMIC EXPERIENCE

December 2011 - December 2012, **General Chair, 45th Annual Symposium in Microarchitecture (MICRO-45)**
Set up and managed academic conference held in Vancouver, British Columbia in December 2012.

September 2001 – April 2002, **Visiting Scholar, University of Texas, Austin**
Monthly visit to lead discussions and direct graduate students in research into high performance computer architecture.

December 1995 - December 1996, **Co-Chair, 29th Annual Symposium in Microarchitecture (MICRO-29)**
Set up and managed academic conference held in Paris, France in December 1996.

January 1985, May 1986, January 1987, **Co-Instructor, Digital Equipment Corporation**
Assistance in the planning and teaching of industrial short courses in logic design and computer architecture conducted by Dr. Yale Patt.

## PUBLICATIONS

Melvin, S., "Endpoint Identification Using System Logs", Workshop on the Analysis of System Logs (WASL) 2009, held in conjunction with the 22nd ACM Symposium on Operating System Principles (SOSP), Big Sky, Montana, October 2009.

Melvin, S., Nemirovsky, M., Musoll, E., Huynh, J., Milito, R., Urdaneta, H., and Saraf, K., "A Massively Multithreaded Packet Processor," *NP2: Workshop on Network Processors, held in conjunction with The 9th International Symposium on High-Performance Computer Architecture (HPCA-9)*, Anaheim, California, February 8-9, 2003.

Melvin, S. and Patt, Y., "Handling of Packet Dependencies: A Critical Issue for Highly Parallel Network Processors," Proceedings*, International Conference on Compilers, Architectures, and Synthesis for Embedded Systems*, October 8 – 11, 2002.

Melvin, S., and Patt, Y., "Enhancing Instruction Scheduling with a Block-Structured ISA,*" International Journal of Parallel Processing*, 23(3):221-243, 1995.

Melvin, S., and Patt, Y., "Exploiting Fine-grained Parallelism Through a Combination of Hardware and Software Techniques,*" Proceedings, 18th International Symposium on Computer Architecture*, Toronto, Canada, May 1991.

Melvin, S., and Patt, Y., "Performance Benefits of Large Execution Atomic Units in Dynamically Scheduled Machines," *Proceedings, 1989 Supercomputer Conference*, Crete, Greece, June 1989.

Melvin, S., Shebanow, M., and Patt, Y., "Hardware Support for Large Atomic Units in Dynamically Scheduled Machines," *Proceedings, 21st Annual Workshop on Microprogramming and Microarchitecture*, San Diego, California, November 1988.

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