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Routing lookups in hardware at memory access speeds

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P. Gupta ; S. Lin ; N. McKeown

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Abstract:

The increased bandwidth in the Internet puts great demands on network routers; for example, to route minimum sized Gigabit Ethernet packets, an IP router must process about 1.5/spl times/10/sup 6/ packets per second per port. Using the "rule-of-thumb" that it takes roughly 1000 packets per second for every 10/sup 6/ bits per second of line rate, an OC-192 line requires 10/spl times/10/sup 6/ routing lookups per second; well above current router capabilities. One limitation of router performance is the route lookup mechanism. IP routing requires that a router perform a longest-prefix-match address lookup for each incoming datagram in order to determine the datagram's next hop. We present a route lookup mechanism that when implemented in a pipelined fashion in hardware, can achieve one route lookup every memory access. With current 50 ns DRAM, this corresponds to approximately 20/spl times/10/sup 6/ packets per second; much faster than current commercially available routing lookup schemes. We also present novel schemes for performing quick updates to the forwarding table in hardware. We demonstrate using real routing update patterns that the routing tables can be updated with negligible overhead to the central processor.

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Keywords

IEEE Keywords

Routing, Hardware, Random access memory, Costs, Spine, Laboratories, Bit rate, Internet, Ethernet networks, Uninterruptible power systems

INSPEC: Controlled Indexing

pipeline processing, telecommunication network routing, Internet, packet switching, transport protocols, table lookup, DRAM chips

INSPEC: Non-Controlled Indexing

50 ns, memory access speeds, IP routing lookups, bandwidth, Internet, network routers, Gigabit Ethernet packets, longest-prefix-match address lookup, OC-192 line, router performance, datagram, pipelined hardware implementation, DRAM, routing update patterns, forwarding table updates, routing tables, central processor

Authors

P. Gupta

Comput. Syst. Lab., Stanford Univ., CA, USA

S. Lin

N. McKeown

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