United States Patent [19]

Riseman

[11] **4,106,050**

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[54] **INTEGRATED CIRCUIT STRUCTURE WITH FULLY ENCLOSED AIR ISOLATION**

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[51] **Int. Cl.**[2] **H01L 27/04**

[52] **U.S. Cl.** **357/49**

[58] **Field of Search** 357/49, 47, 50, 55

[56] **References Cited**

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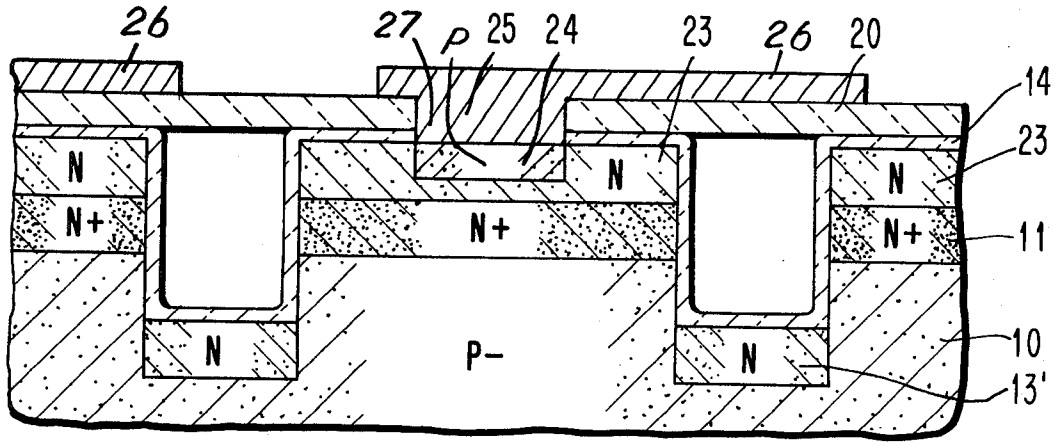
Primary Examiner—Stanley D. Miller, Jr.
Assistant Examiner—James W. Davie
Attorney, Agent, or Firm—Julius B. Kraft; Theodore E. Galanthay

[57] **ABSTRACT**

An integrated circuit member structure comprising a semiconductor substrate having formed therein a pattern of cavities extending from one surface of the substrate into the substrate and fully enclosed within said member, a plurality of pockets of semiconductor material extending from said substrate laterally surrounded and electrically insulated by said cavities and a planar layer of electrically insulative material on said surface.

5 Claims, 8 Drawing Figures



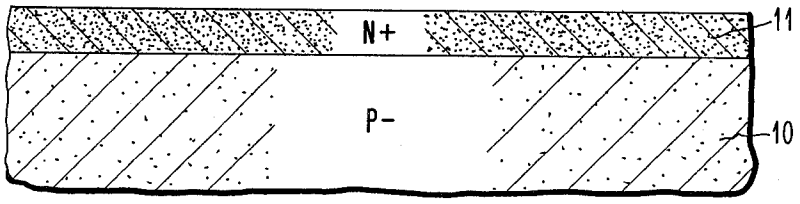


FIG. 1

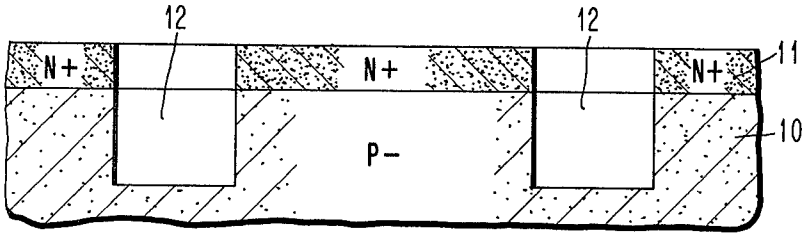


FIG. 2

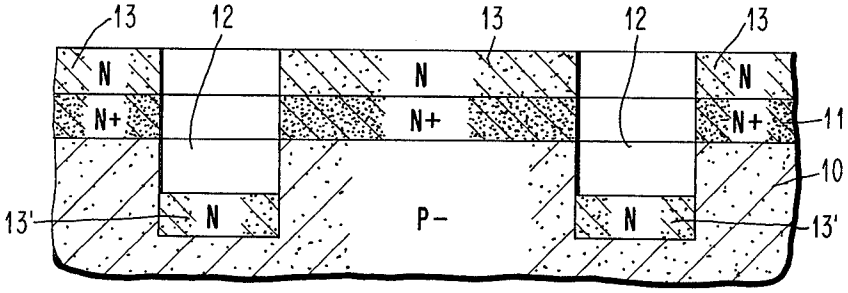


FIG. 3

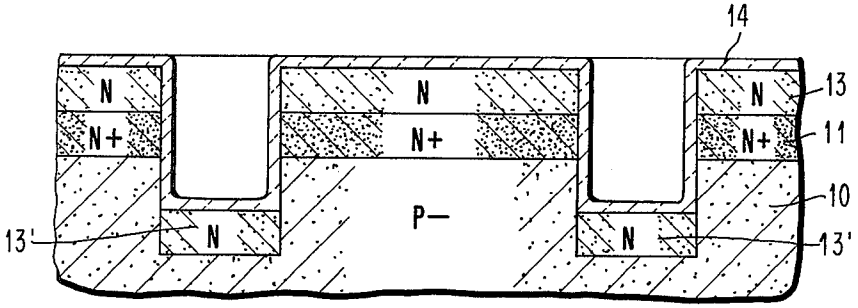


FIG. 4

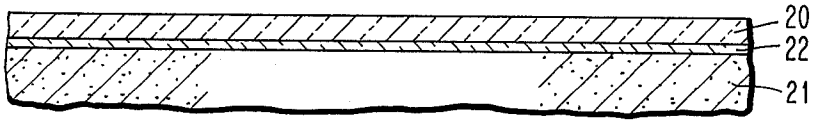


FIG. 4A

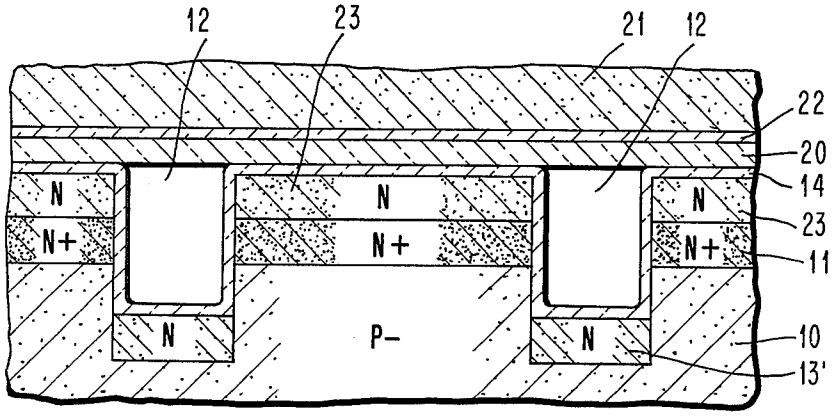


FIG. 5

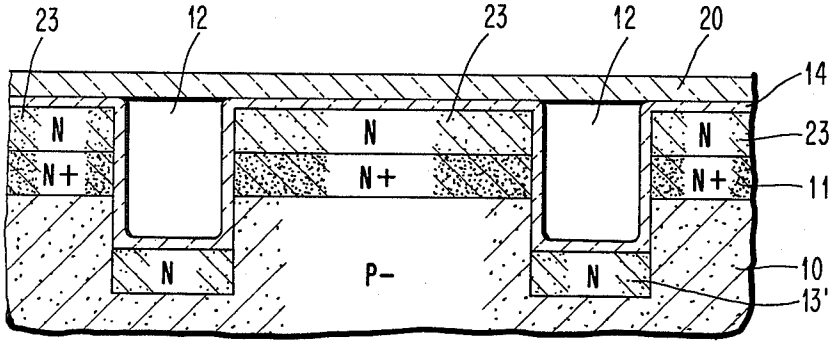


FIG. 6

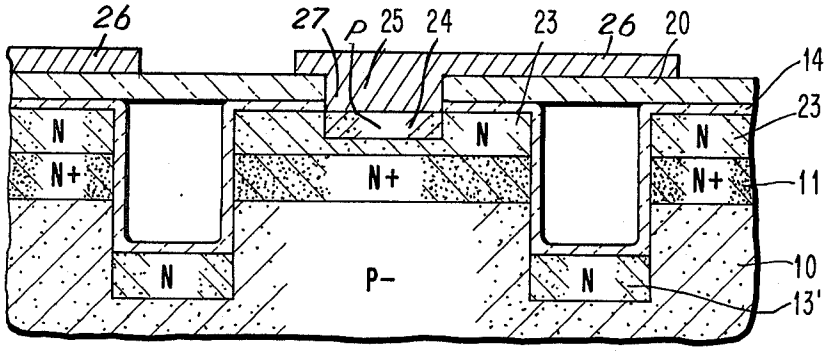


FIG. 7

INTEGRATED CIRCUIT STRUCTURE WITH FULLY ENCLOSED AIR ISOLATION

BACKGROUND OF THE INVENTION

The present invention relates to integrated circuit structures and more particularly to dielectric isolation in such integrated circuit structures, particularly by air-isolation.

The form of most existing integrated circuits is the so-called monolithic form. Such a structure contains great numbers of active and passive devices in a block or monolith of semiconductor material. Electrical connections between these active and passive devices are generally made on a surface of the semiconductor block of material. Until recently, junction isolation has been by far the most widely practiced manner of isolating devices or circuits in the integrated circuit from each other. For example, active P-type diffusions are customarily used to isolate conventional FET and bipolar devices from one another and from other devices such as the resistors and capacitors. Such junction isolation is also used in integrated circuits utilizing field effect transistor devices. More detailed descriptions of junction isolation may be found in U.S. Pat. Nos. 3,319,311; 3,451,866; 3,508,209 and 3,539,876.

Although junction isolation has provided excellent electrical isolation in integrated circuits which have functioned very effectively over the years, at the present stage of the development of the integrated circuit art, there is an increasing demand in the field of digital integrated circuits for faster switching circuits. It has long been recognized that the capacitive effect of the isolating P-N junctions has a slowing effect on the switching speed of the integrated circuits. Until recently, the switching demands of the integrated circuits have been of a sufficiently low frequency that the capacitive effect in junction isolation has presented no major problems. However, with the higher frequency switching demand which can be expected in the field in the future, the capacitive effect produced by junction isolation may be an increasing problem. In addition, junction isolation requires relatively large spacing between devices, and, thus, relatively low device densities which is contrary to higher device densities required in large scale integration. Junction isolation also tends to give rise to parasitic transistor effects between the isolation region and its two abutting regions. Consequently, in recent years there has been a revival of interest in integrated circuits having dielectric isolation instead of junction isolation. In such dielectrically isolated circuits, the semiconductor devices are isolated from each other by insulative dielectric materials or by air.

Conventionally, such dielectric isolation in integrated circuits has been formed by etching channels in a semiconductor member corresponding to the isolation regions from the back side of the member, i.e., the side opposite to the planar surface at which the devices and wiring of the integrated circuit are to be formed. This leaves an irregular or channeled surface over which a substrate back side, usually a composite of a thin dielectric layer forming the interface with the semiconductor member covered by a thicker layer of polycrystalline silicon is deposited. Alternatively, the polycrystalline silicon need not be deposited in which case, the channels would provide air-isolation. Next, the other or planar surface of the semiconductor member may be either mechanically ground down or chemically etched until the bottom portions of the previously etched channels are reached. This leaves the structure wherein a plurality of pockets of semiconductor material surrounded by a thin dielectric layer are either supported on a polycrystalline silicon substrate and separated from each other by the extensions of the polycrystalline substrate or in the absence of the polysilicon, a structure in which the pockets of semiconductor material are, in effect, "air-isolated" from each other. While such structures provide an essentially flat and thus wirable planar surface of coplanar pockets of semiconductor material, such integrated circuit structures have limited utility with integrated circuits of high device densities. This is due to the fact that the etched channels which correspond to the isolation regions must be formed from the back side of the integrated circuit substrate and etched until the level of the active planar surface of the substrate is reached.

It is recognized in the art that when etching from the back side of an integrated circuit member the etching must be made to greater depth than when etching directly from the planar front surface in order to insure uniform lateral isolation. It is also recognized that when etching through a member, the extent of lateral etching will be substantially the same as the depth of etching. Accordingly, when etching channels from the back side of the substrate, so much lateral "real estate" is consumed on the wafer that such an approach has very limited practicality in high density integrated circuits.

On the other hand, if the etching to form the channels in the above dielectric isolation or air-isolation structure is carried out from the active or front surface of the integrated circuit, only limited lateral etching is necessary to reach practical isolation depths. However, the result is an essentially corrugated active surface rather than a planar one. Such a corrugated active surface is, of course, difficult to wire, i.e., form integrated circuit metallurgy interconnections by conventional photolithographic integrated circuit fabrication techniques.

Another approach which has been utilized for forming lateral dielectric isolation in the art involves the formation of recessed silicon dioxide lateral isolation regions, usually in the eptitaxial layer where the semiconductor devices are to be formed, through the expedient of first selectively etching a pattern of recesses in the layer of silicon, and then thermally oxidizing the silicon in the recesses with appropriate oxidation blocking masks, e.g., silicon nitride masks, to form recessed or inset regions of silicon dioxide which provide the lateral electrical isolation. Representative of the prior art teaching in this area are U.S. Pat. No. 3,648,125 and an article entitled, "Locos Devices," E. Kooi et al., Philips Research Report 26, pp. 166 – 180 (1971).

While this approach has provided both planarity at the active device integrated circuit surface as well as good lateral dielectric isolation, it has encountered some problems. Originally, the art applied the silicon nitride masks directly onto the silicon substrates. This gave rise to problems associated with high stresses created on the underlying silicon substrate by the silicon nitride-silicon interface. Such stresses were found in many cases to produce dislocations in the silicon substrate which appear to result in undesirable leakage current pipes and otherwise adversely affect the electrical characteristics of the interface. In order to minimize such interface stresses with silicon nitride layers, it has become the practice in the art to form a thin layer of silicon dioxide between the silicon substrate and the

silicon nitride layer. During such thermal oxidation, there is a substantial additional lateral penetration of silicon oxide from the thermal oxidation beneath the silicon nitride. This lateral penetration is greatest at the mask-substrate interface to provide a laterally sloping structure known and recognized in the prior art as the undesirable, "bird's beak."

The publications, "Local Oxidation of Silicon; New Technological Aspects," by J. A. Appels et al., Philips Research Report 26, pp. 157 – 165, June 1971, and "Selective Oxidation of Silicon and Its Device Application," E. Kooi et al., *Semiconductor Silicon* 1973, published by the Electrochemical Society, Edited by H. R. Huff and R. R. Burgess, pp. 860 – 879, are representative of the recognition in the prior art of the "bird's beak" problems associated with silicon dioxide-silicon nitride composite masks, particularly when used in the formation of recessed silicon dioxide by thermal oxidation. Because of such "bird's beak" problems, the art has experienced some difficulty in achieving well-defined lateral isolation boundaries.

In addition, while, as previously mentioned, air isolation has been used in the prior art in integrated circuits, no practical approach has been developed for the application of air isolation to high density, large scale integrated circuits.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an air-isolated integrated circuit structure with a planar wirable surface.

It is another object of the present invention to provide an air-isolated integrated circuit structure in which the air isolation regions are of minimal dimensions so that the integrated circuit structure is adaptable to high-device density integrated circuits.

It is a further object of the present invention to provide an air-isolated integrated circuit structure in which both the upper and lower surfaces of the structure are planar.

It is yet a further object of the present invention to provide a dielectrically isolated integrated circuit structure in which both upper and lower surfaces are planar and which is substantially free from stresses created by changes in volume in the semiconductor material during integrated circuit fabrication heating steps.

It is an even further object of the present invention to provide a method for fabricating an integrated circuit structure having the above described advantages.

In accordance with the present invention, there is provided an integrated circuit member comprising a semiconductor substrate having formed therein a pattern of cavities extending from one surface of the substrate into the substrate and fully enclosed within the member, a plurality of pockets of semiconductor material extending from said surface laterally surrounded and electrically insulated by said cavities and a planar layer of electrically insulative material on the surface.

The integrated circuit member is formed by a fabrication method comprising first etching a pattern of cavities extending from one surface of a first silicon substrate into the substrate; the cavities laterally surround and electrically isolate the plurality of silicon substrate pockets. Next, a first layer of silicon dioxide is formed on this first substrate surface. There is also formed over a second silicon substrate a planar second layer comprising a glass, and preferably a siliceous glass. The glass composition may be any conventional glass composition including those described in Volume 10, pp. 533 – 546, of the Encyclopedia of Chemical Technology, Kirk and Othmer, Second Edition, published in 1966 by Interscience Publishers. However, the silicate glasses, such as those described on pp. 540 – 545 in the above encyclopedia, have been found to be particularly desirable. The term "siliceous glass" as used in this application, is meant to include all silica-containing glasses including glasses which are substantially unmodified silica (SiO_2). In addition, among the silicate glasses which may be used are alkali silicate glasses which are modified by Na_2O, soda-lime glasses, borosilicate glasses, alumino-silicate glasses, and lead glasses. Then, the two substrates are bonded together by fusing the planar layer over the second substrate to the silicon dioxide layer over the first substrate to thereby fully enclose the cavities. Finally, the second silicon substrate is removed from the fused structure.

The resulting structure is one having a planar surface, at which the active devices of the integrated circuit may be subsequently formed, i.e., the surface of the first silicon substrate covered by the planar layer of silicon dioxide. Further, since the cavities have been formed by etching down from this surface rather than the back side surface of the structure, only minimal lateral integrated circuit "real estate" has been consumed in forming such cavities. In addition, the back side surface of the structure remains unetched and thus planar. Finally, because of the fully enclosed air-isolation, the structure has cavities capable of absorbing changes in volume of the silicon material resulting from the application of heat during the processing steps. Thus, heat-induced stresses are minimized.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of the preferred embodiments of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1** – **7** are diagrammatic sectional views of a portion of an integrated circuit in order to illustrate the method of forming the preferred embodiment of the present invention.

PREFERRED EMBODIMENTS OF THE PRESENT INVENTION

FIGS. **1** – **7** illustrate the preferred embodiment of the present invention. On a suitable P— wafer **10** having a resistivity of 10 ohm/cm, an N+ region **11** which will subsequently serve as a subcollector is formed by conventional thermal diffusion of impurities as set forth for example in U.S. Pat. No. 3,539,876. When introduced into substrate **10**, N+ region **11** has a surface concentration of 10^{21} atoms/cm^3. Region **11** may also be formed by conventional ion implantation techniques.

Then, FIG. **2**, a pattern of recesses or cavities **12** are etched in the substrate. This pattern of recesses corresponds to the desired air-isolation pattern for the integrated circuit structure. Recesses **12** are formed by etching utilizing a conventional mask such as a silicon dioxide mask formed by standard photolithographic integrated circuit fabrication techniques which mask has apertures corresponding to the recessed pattern to be formed. Then, the substrate may be etched in the conventional manner through the apertures defined in the silicon dioxide mask.

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