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Ying

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[54] **METHOD FOR FABRICATING SEMICONDUCTOR DEVICES**

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[73] Assignee: **Hughes Aircraft Co.,** Culver City, Calif.

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[21] Appl. No.: **184,767**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 95,652, Dec. 7, 1970, abandoned.

[52] **U.S. Cl.** **29/583,** 29/580

[51] **Int. Cl.** **B01j 17/00**

[58] **Field of Search** 29/580, 590, 583

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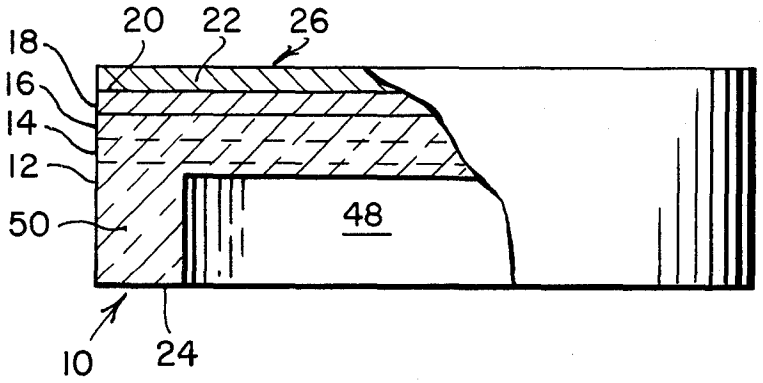
Primary Examiner—Roy Lake
Assistant Examiner—W. Tupman

[57] **ABSTRACT**

A plurality of individual semiconductor devices are simultaneously produced by thinning a doped semiconductor wafer to a desired uniform thickness, thermocompression bonding the thinned semiconductor wafer to a metal support plate, etching the wafer into many tiny discrete members, and punching out small individual sections of the support plate, each section forming a heat sink and having one of the bonded semiconductor members thereon. Alternately, the semiconductor wafer may be thinned after the bonding step has been effected, although prior thinning is preferred.

15 Claims, 12 Drawing Figures



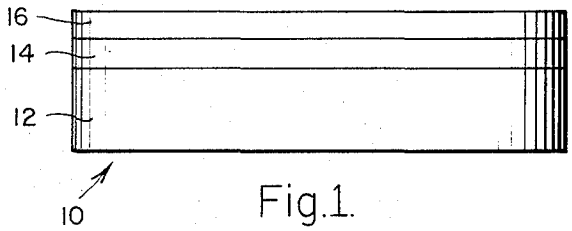


Fig.1.

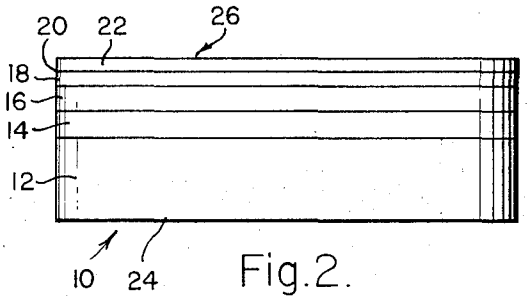


Fig.2.

Fig.3a.

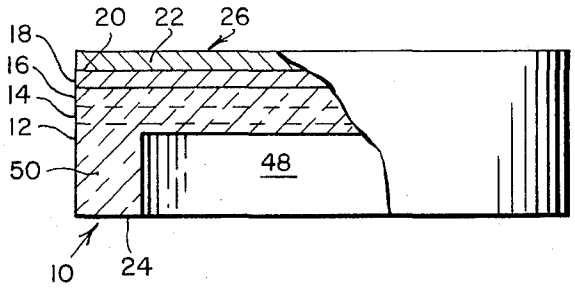


Fig. 3b.

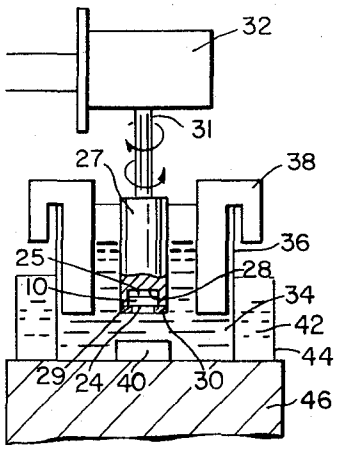
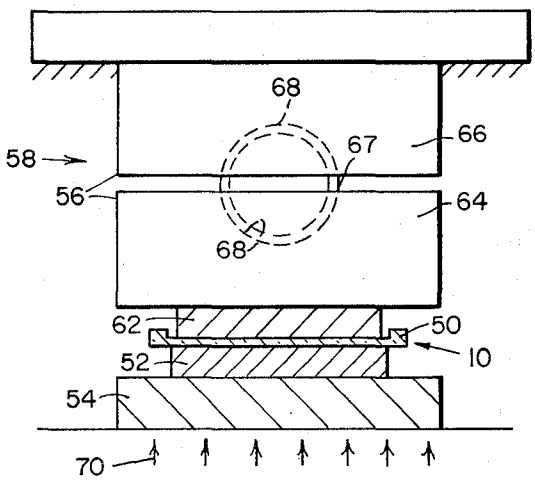


Fig. 4a.



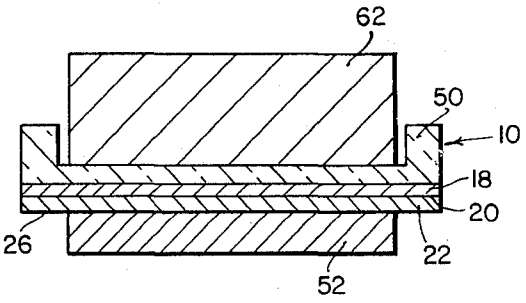


Fig.4b.

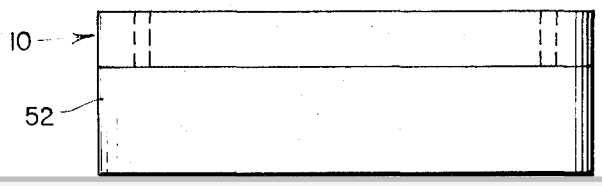


Fig.5.

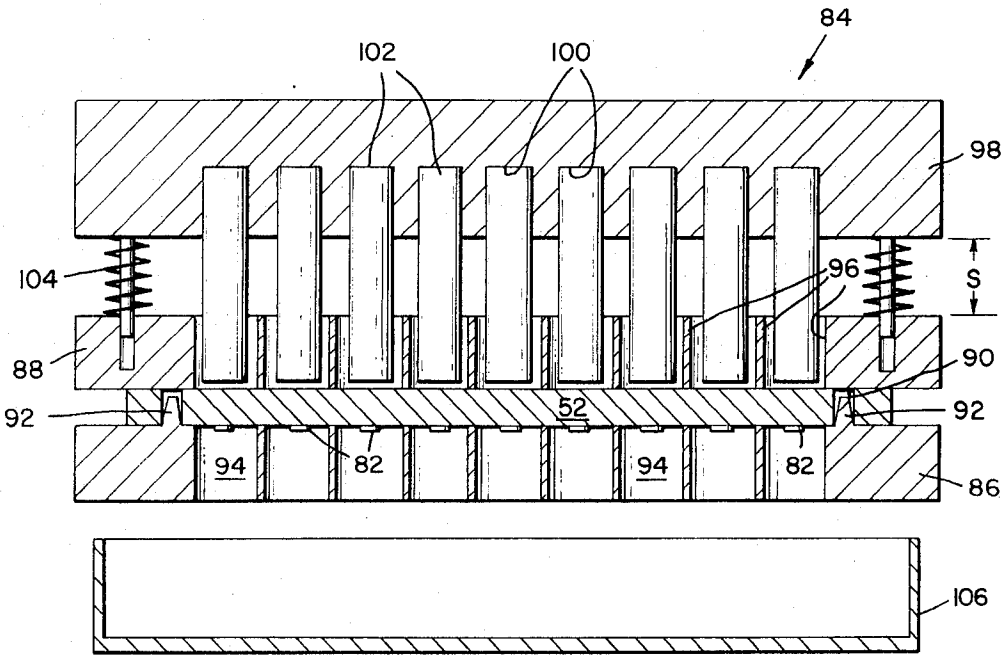


Fig. 8.

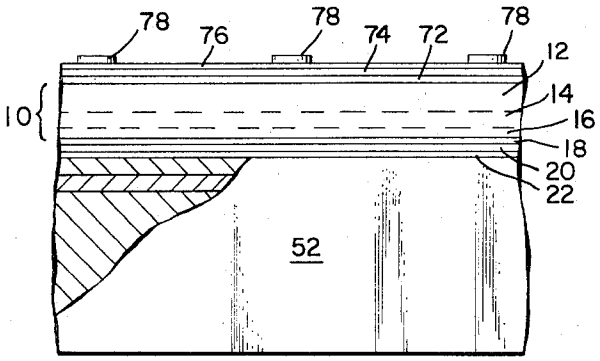


Fig. 6

Fig. 7.

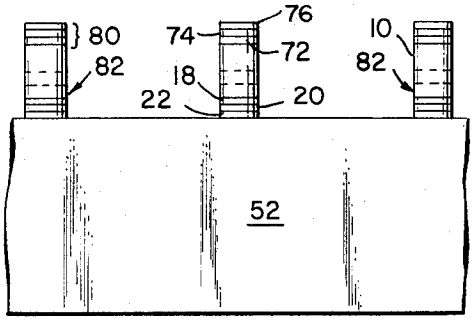
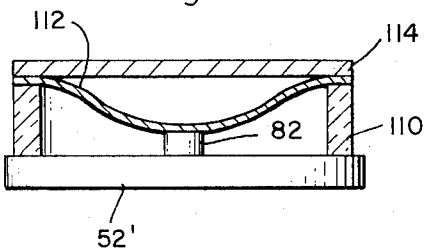


Fig. 10.



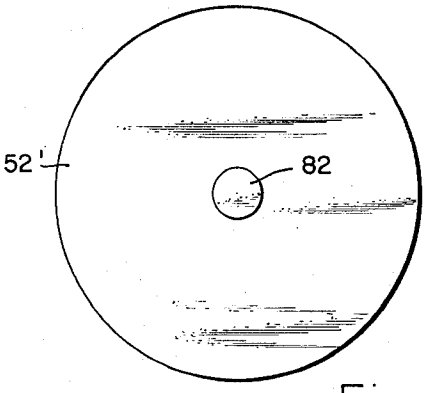


Fig. 9

METHOD FOR FABRICATING SEMICONDUCTOR DEVICES

This is a continuation-in-part of copending U.S. Pat. application, Ser. No. 95,652, filed Dec. 7, 1970, for "Semiconductor Devices And Method Of Making Same", and now abandoned.

The present invention relates to the fabrication of small semiconductor devices and, more particularly, to an inexpensive method for simultaneously fabricating a plurality of such devices.

Small semiconductor devices are useful for a variety of functions, such as for use as PN diodes, PIN diodes, varactor diodes, IMPATT (impact avalanche ionization transit time) and TRAPATT (trapped plasma avalanche trigger transit) diodes, triodes, etc., and transistors. The primary function of IMPATT and TRAPATT diodes, when employed as avalanche diodes, is to generate and/or amplify microwave and millimeter wave signals. Several factors must be considered for the fabrication of these devices, namely, low cost, efficiency and power output, reliability, ease of packaging, high frequency operation, adaptability to various applications and to various circuits, e.g., coaxial, waveguide and microstrip.

The purpose of this invention is to provide a process for fabrication of such devices wherein all the above features are combined so that a high power and high efficiency packaged device can be produced in an economical fashion. As is known, such devices comprise a tiny, thin, semiconductor element affixed to a small metal plate. Because of their small size, they have been relatively difficult to fabricate and several techniques have been devised therefor. The two most common methods are infrared alignment to form a pill structure diode and double mask alignment to form a mesa structure diode which, in both cases, is thermocompression bonded with other individual diodes into a package. In both techniques, a small section is punched out of a copper plate and the tiny, thin, pre-shaped silicon semiconductor element is then thermocompression bonded to the small section. These techniques require separate assembling and bonding operations and, consequently, are tedious, time consuming, cumbersome, and therefore, expensive. In addition, because of handling difficulties, the diodes must be more than 50 microns thick. Since the active region of the device is only about 1 to 5 microns thick, the excess silicon thickness adds series loss and reduces the diodes rf performance. The packages used are also frequency limited because of high loss at higher frequencies and, therefore, they are not suitable to integrated microstrip circuit application.

The present invention avoids these and other problems by mass producing many such devices in a single operation. Briefly, a semiconductor wafer is thinned to a desired thickness and secured to a metal support plate. Alternatively, the wafer may be thinned after being secured to the plate. Thereafter, the wafer is etched into a plurality of discrete devices. The plate with each device is then subjected to a multiple, single step punching or dicing operation to form a plurality of individual devices.

It is, therefore, an object of the present invention to provide a method for mass producing small semiconductor devices.

Another object of the present invention is to provide

vices each including a tiny, thin semiconductor element bonded to a small metal support member.

These and other objects and advantages of the present invention will become apparent from the following description and drawings of illustrative embodiment, wherein:

FIG. **1** depicts an exemplary doped silicon wafer preparatory to the processing steps of the present invention;

FIG. **2** depicts the wafer of FIG. **1** metallized on its upper doped surface;

FIGS. **3***a* and **3***b* respectively depict the wafer of FIG. **2** in partial cross-section having a thinned substrate and the apparatus for thinning the wafer;

FIGS. **4***a* and **4***b* illustrate the step of bonding the thinned semiconductor wafer to a metal support plate in accordance with the present invention, FIG. **4***b* showing an enlarged view of the wafer, plate and block portion of FIG. **4**a;

FIG. **5** shows the bonded wafer-metal support plate assembly with a portion of the wafer removed after the bonding operation of FIG. **4**;

FIGS. **6** and **7** illustrate successive steps in fabricating an array of a plurality of tiny semiconductor elements disposed on a common face of the metal support plate;

FIG. **8** depicts the assembly of FIG. **7**, positioned in a punch press prior to the punching out of separate sections from the metal support plate, each having a semiconductor element thereon;

FIG. **9** is a plan view of a single tiny semiconductor device assembly; and

FIG. **10** is a side elevational view of a hermetically packaged semiconductor device.

In order to produce various kinds of devices such as PN diodes, PIN diodes, varactor diodes, IMPATT and TRAPATT diodes, triodes, etc., a wafer, for example, of silicon, gallium arsenide, and germanium, may at the outset contain regions of predetermined conductivity type. Although the wafer described herein comprises a specific $p+-n-n+$ layer configuration, it is to be understood that other, differently doped wafers may be utilized in the inventive process. However, for purposes of clarity and simplication in explaining the process of the present invention, a specifically P+—n—n+ doped wafer will be utilized in the description of the preferred embodiment of the process.

Accordingly, with reference to FIG. **1**, a wafer **10** includes a thick $n+$ substrate **12** almost as thick as the wafer, a thin n layer **14**, and a thin $p+$ layer **16**. For purposes of illustration, layers **14** and **16** are shown greatly thickened. However, as examples of thicknesses utilized, substrate **12** is approximately 6 mils in thickness, layer **14** is 1 micron in thickness, and layer **16** is 12 microns in thickness. Alternatively, in a 7 mil thick wafer, the n and $p+$ layers may be extremely thin, the n layer being typically about 1.4 microns in thickness and the $p+$ layer being typically about 0.4 microns in thickness. The wafer is, for example, of general circular cross-section having a diameter of approximately 1.25 inches and one edge may be flattened for alignment purposes, although other cross-sectional configurations can be used. Such as-doped wafers are commercially obtainable, or may be otherwise doped by well-known processes, such as by diffusion and ion implantation.

As shown in FIG. **2**, layer **16** is coated with a metal film comprising, for example, coatings **18**, **20** and **22** of

coating **20** may be replaced with a chromium-gold interface. Examples of thicknesses for the former are 10,000 A gold, 1,000 A platinum, and 800 A chromium. For the latter, gold layer **18** may be approximately 15 microns thick, platinum layer **20** may be approximately 200 A thick, and a chromium layer **22** about 600 A thick. Coatings **18, 20** and **22** are applied by standard evaporation techniques except that, after some of the gold of layer **22** has been evaporated in situ, further gold is added by electroplating to build up its thickness.

Wafer **10,** as built and metallized, is then thinned at its unmetallized end surface **24** to form the configuration shown in FIG. **3***a* by a process utilizing the apparatus depicted in FIG. **3***b*. Wafer **10** is first affixed, by a wax, such as bees wax, to a disc **25,** such as sapphire, which is not capable of being attacked by an etching solution utilized in the thinning process. The disc is affixed to surface **26** at the metallized side of the wafer containing coating **22.** Such affixation may be effected by placing the wax between the wafer and the disc and by heating the two for a time and at a temperature sufficient to enable the wax to melt and the two to stick together upon cooling after the wax has melted. The secured together disc and wafer are then hand pressed into a holder **27,** such as of "Teflon" (trademark of E. I. Du Pont de Nemours & Co.), the disc side being within the holder within an end recess **28** thereof. For this purpose, recess **28** is provided with width and depth dimensions which are substantially the same as those of the disc and wafer to permit substrate side **24** of the wafer to be flush with an end **29** of the holder.

A black wax, such as "Apiezon" (trademark of James G. Biddle Co.), (see also "The Condensed Chemical Dictionary," A. and E. Rose, Reinhold Publishing Corporation, 1969, 7th Ed.) is placed around the intersecting edges of the holder and the wafer substrate so as to produce a rim **30** which extends slightly onto the surface of the wafer substrate to form an exposed interior portion of surface **24.**

The holder is then secured to the apparatus depicted in FIG. 3b by attaching it to a motor shaft **31** which is capable of being alternately rotated by a reversible motor **32.** The end of the holder containing the waxed wafer is then placed within an etchant solution **34** contained within a receptacle **36.** A plurality of "Teflon" baffles **38** are symmetrically placed around the holder. Below the receptacle is placed a magnetic stirrer **40.** In order to maintain constant temperature of solution **34,** a coolant **42,** such as water, is placed around the receptacle and held within a container **44.** The whole apparatus is supported on a base **46.**

Solution **34** is an etching solution for removal of a portion of substrate **12** not masked by the black wax. The type of etchant utilized will, of course, depend upon the material of the substrate, all of which are well-known in the prior art. However, for purposes of illustration, the etching solution for silicon comprises 3 parts by volume of hydrogen fluoride, 5 parts by volume of nitric acid, and 3 parts by volume of acetic acid. For gallium arsenide, the etching solution may comprise 3 parts by volume sulphuric acid, 1 part by volume water, and one part by volume hydrogen peroxide. Germanium is etchable by a solution comprising 3 parts by volume hydrogen fluoride, 5 parts by volume nitric acid, 6 parts by volume of acetic acid, and 0.3 percent of the foregoing combination of bromine.

Motor **32** is caused to alternately rotate holder **27** and wafer **10** within solution **34** while the solution is magnetically stirred to obtain washing-machine-like agitation, in order to obtain a smooth, ungrooved, fine etch on the exposed portion of surface **24** of substrate **12.** The speed of rotation and the period of reversing the direction of rotation of the motor is determined experimentally in accordance with the depth of etching and the quality thereof. In the etching of silicon, for example, motor **32** is caused to turn at 1,000 rpm with a reversal in direction of rotation every 1 minute for the first 5 mil etch. Thereafter, reversal is every 5 seconds for final control of etch. The water jacket cools the solution to maintain a constant temperature in order to overcome the heating of the solution by the etching process.

After etching, the holder and wafer are removed from the solution and rinsed in deionized water to remove remnants of the etchant. The disc and wafer are then removed from the holder and separated from one another. Any remaining wax on the wafer is removed with tetrachloroethylene and methyl alcohol. After drying, the etched wafer had the appearance as that illustrated in FIG. **3***a*, showing a thinned wafer **10** having an etched portion **48** and a rim **50.** The purpose of the rim was to facilitate ease in further handling of the wafer since, at this time, the wafer had an approximate thickness of 10 microns ± 2 microns.

As shown in FIGS. **4***a* and **4***b*, wafer **10,** as thinned, is then disposed in face-to-face relation on a copper plate **52,** with metallized side **26** in contact therewith. The copper plate has a thickness of several mils and a diameter smaller than the wafer diameter between the periphery of rim **50.** Typically, copper plate **52** is about 10 mils thick. It is to be understood that support plate **52** need not be made of copper but may be made of various suitable metals; but it is preferred to utilize commercially available; oxygen-free copper material for the plate in view of its excellent thermal and electrical conductivity.

The assembled wafer and plate are placed between opposed plates **54** and **56** of a manually operated hydraulic laboratory bench press **58** having heater filaments and water coolant lines within the plates. A stainless steel block **62,** having a diameter less than wafer **10** to fit within rim **50,** is placed on the substrate. Blocks **56** includes portions **64** and **66** having a ball bearing **67** arranged within spherical recesses **68** in the block portions to provide an adjustment for non-parallelism of block portion **64** and plate **54** and non-alignment of plate **52** and wafer **10.** Lower press plate **54** is moved upward (as indicated by arrows **70**) toward upper block **56** to press wafer **10** and plate **52** together. The wafer and copper plate are heated to a temperature less than the silicon-gold eutectic temperature while the wafer-plate assembly is under compression. In this way thermocompression bonding of wafer **10** to plate **52** is accomplished. Illustratively, the wafer-plate assembly can be thermocompression bonded by heating it to 200°C for about 20 to 30 minutes while exerting a pressure on the assembly of about 40,000 psi. It is preferred that the pressure not exceed 100,000 psi to prevent wafer damage. In practice, the temperature, pressure and time of the thermocompression step are variable to a considerable extent with continued satisfactory results. It is to be understood, however, that, although a particular thermocompression bonding step

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