<u>Consolidated Petitioners</u> Apple Inc. HTC Corp.* HTC America, Inc.*

IPR2016-00923 (U.S. Pat. No. 5,812,789)

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*Petitioner in IPR2016-00

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Argument

- Lambrecht anticipates each and every element of the challenged claims including:
 - a "decoder" that requires access to memory sufficient to maintain real time operation; and
 - b a "shared bus" with sufficient bandwidth to allow a decoder to access memory and operat in real time.
- Patent Owner mischaracterizes Lambrecht and makes incorrect assumptions about the prior art.

'789 Patent, Claim 1

- 1. An electronic system coupled to a memory, comprising:
- a first device that requires access to the memory;
- a decoder that requires access to the memory sufficient to maintain real time operation; and
- a memory interface for coupling to the memory, and coupled to the first device and to the decoder, the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory and a <u>shared bus</u> coupled to the memory the first device, and the decoder, <u>the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.</u>

Ex. 1001 ('789 Patent), claim 1.

Lambrecht anticipates claim 1*

*Patent Owner does not separately dispute the unpatentability of the dependent claim limitations over the recited prior art. (*See* Response, Paper No. 22 at 24-26).

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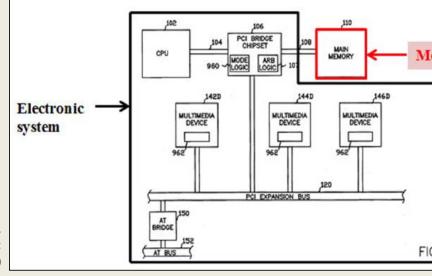
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Lambrecht teaches an "electronic system"

<u>Claim 1:</u> "<u>An electronic system</u> <u>coupled to a memory...</u>"

Ex. 1032 (Lambrecht), Fig. 21 (cited in Petition, Paper No. 2 at 11; see also Ex. 1030 (Stone Decl.) ¶ 78 at 35)



Referring now to FIG. 21, a computer system is a which includes an expansion bus, preferably a PCI bus and which includes mode logic which selects be different modes of the PCI bus 120. The computer system FIG. 21 is similar to the computer system of FI However, the mode logic in the computer system of FI is operable to place the PCI bus 120 in either a normal mode or in a real-time/multimedia mode optimized multimedia transfers of periodic data. As described b

Ex. 1032 (Lambrecht) at 26:49-56 (cited in Petition, Paper No. 2 at 10-11)

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