UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co., Ltd., and
Samsung Electronics America, Inc.
Petitioners

v.

Parthenon Unified Memory Architecture LLC
Patent Owner

INTER PARTES REVIEW OF U.S. PATENT NO. 5,812,789
Case IPR No.: *To Be Assigned*

DECLARATION OF HAROLD S. STONE, PH.D., REGARDING U.S. PATENT NO. 5,812,789

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I, Harold S. Stone, Ph.D., declare as follows:

I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for the Petitioners to submit this declaration in connection with Petitioners' Petition for *Inter Partes* Review of claims 1, 3-6, 11 and 13 of U.S. Patent No. 5,812,789 ("'789 patent") (Ex. 1001).

B. Background and Qualifications

2. I was awarded a Ph.D. and Master's Degree in Electrical Engineering from the University of California-Berkeley in 1963 and 1961, respectively. I received a Bachelor of Science degree in Electrical Engineering from Princeton University in 1960.

3. After my graduation from Berkeley in 1963, I served as a Research Engineer at Boeing and SRI International. I then held faculty positions at Stanford University and at the University of Massachusetts, where I served as a professor of computer science and electrical engineering.

4. In 1984, I started working for IBM as a Manager of Advanced Architecture Studies. In 1990, I became a Research Staff Member at IBM. During my time at IBM, I managed and conducted research in the area of memory systems and optical interconnections. I worked at IBM until 1994, when I became a Fellow at the NEC Research Institute, the highest technical position in the company. At NEC, I conducted research in image processing. I am an inventor of a patent to

NEC regarding a technique for decompressing JPEG images in a novel way that permits images to be searched without fully decompressing them. The decompression technique is based on inverse discrete cosine transforms, which are one of the basic elements of MPEG decompression.

5. I have authored, coauthored, or edited 9 books in various technical areas, the most recent of which appeared in 2011. My textbooks have sold over 100,000 copies. My work on the use of the perfect shuffle interconnections for supercomputers is widely recognized, and many supercomputers based on these interconnections were developed and marketed. For this work and my textbook contributions to the field, I was elected an IEEE Fellow and ACM Fellow, and received the IEEE Piore Field Award, the IEEE Computer Society Taylor Booth Award, and the Charles Babbage Award. I am the principal inventor or co-inventor of 27 patents, including seven in the area of computer architecture - U.S. Patent Nos. 4,989,131, 5,065,310, 5,163,149, 5,611,070, 5,742,785, 5,790,823, and 6,311,260.

6. I have served as a consultant to industry while holding my academic positions and have extensive experience in computer design for embedded computers as a consequence, including low-power computers for use in satellites and ultra-reliable computers for use in nuclear submarine navigation systems. In recent years I have been a member of two Division Review Committees at Los

Alamos National Laboratory in the area of Nuclear Nonproliferation and a consultant to NASA in the area of satellite image processing.

7. My work influenced the industry to develop several different "hypercube" computers in the 1980s, all of which had interconnections based on the perfect shuffle. In the 1990s, near when the '789 patent was filed, Intel, Sun, HP, and MIPS Technologies, Inc., introduced extension instruction sets for multimedia applications, all of which incorporated perfect shuffle data movement operations. The shuffle and its inverse are common operations used by MPEG software algorithms in processors that have multimedia instructions sets.

8. In 1977, together with W. Kahan and J. Coonen, I authored the original proposal ("the KCS proposal") to the working group charged for developing a floating-point standard, which is now known as the IEEE 754 Floating Point Standard. The standard that emerged is that proposal with small changes and additions. It has been implemented in several billion processors.

9. My Curriculum Vitae is submitted herewith as Ex. 1029.

C. Compensation and Prior Testimony

10. I am being compensated at a rate of $500 per hour for my study and other work in this matter, plus actual expenses. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

11. I am also acting as an expert in the pending litigation between Patent Owner and Petitioners.

12. I previously prepared declarations in support of *inter partes* review petitions filed by Petitioners and other defendants in the pending litigation, which I understand are now identified as IPR2015-01494, IPR2015-01500, IPR2015-01501, IPR2015-01502, and IPR2015-01503.

13. Previously, I have testified either by deposition or at trial in the following litigation matters. The list below includes all deposition and trial testimony within the last five years:

- *Parthenon Unified Memory Architecture LLC v. Samsung Electronics Co., Ltd. et al.* (U.S. District Court, Eastern District of Texas), Case No. 2:14-cv-00902-JRG-RSP;
- *Advanced Internet Technologies, Inc. v. Dell, Inc.* (U.S. District Court, Eastern District of North Carolina), Case No. 5:07-cv-00426-H;
- *Microunity Systems Engineering Inc v. Acer Inc et al.* (U.S. District Court, Eastern District of Texas), Case No. 2:10-cv-00091-LED-RSP;

- *Technology Service Corporation v. Mountcastle et al.* (U.S. District Court, Eastern District of Virginia – Alexandria), Case No. 1:10-cv-00901-TSE-TCB;
- *BIAX Corporation v. Motorola Solutions, Inc. et al.* (U.S. District Court, District of Colorado – Denver), Case No. 1:10-cv-03013-PAB-KLM;
- Certain Computing Devices with Associated Instructions Sets and Software (International Trade Commission), Inv. 337-TA-812;
- *Stragent, LLC et al. v. Intel Corporation* (U.S. District Court, Eastern District of Texas – Tyler), Case No. 6:11-cv-00421-TBD-JDL; and
- *Convolve Inc. et al. v. Compaq Computer Corporation et al.*, (U.S. District Court, Southern District of New York – Foley Square), Case No. 1:00-cv-05141-GBD-JCF.

D. Information Considered

14. My opinions are based on my years of education, research, and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this declaration and those listed in Appendix A.

15. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

16. My analysis of the materials produced in this investigation is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. LEGAL STANDARDS FOR PATENTABILITY

17. In expressing my opinions and considering the subject matter of the claims of the ’789 patent, I am relying upon certain basic legal principles that have been explained to me.

18. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

19. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as “prior art” and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

20. I understand that the prior art includes patents and printed publications that existed before the earliest filing date (the "effective filing date") of the claim in the patent. I also understand that a patent will be prior art if it was filed before the effective filing date of the claimed invention, while a printed publication will be prior art if it was publicly available before that date.

21. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person having ordinary skill in the art. My understanding of the two legal standards is set forth below.

A. Anticipation

22. I understand that the following standards govern the determination of whether a patent claim is "anticipated" by the prior art.

23. I have applied these standards in my evaluation of whether the claims of the ’789 patent would have been anticipated by the prior art.

24. I understand that, for a patent claim to be "anticipated" by the prior art, each and every requirement of the claim must be found, expressly or inherently, in a single prior art reference as recited in the claim. I understand that claim limitations that are not expressly described in a prior art reference may still be there if they are "inherent" to the thing or process being described in the prior

art. For example, an indication in a prior art reference that a particular process complies with a published standard would indicate that the process must inherently perform certain steps or use certain data structures that are necessary to comply with the published standard.

25. I understand that if a reference incorporates other documents by reference, the incorporating reference and the incorporated reference(s) should be treated as a single prior art reference for purposes of analyzing anticipation.

26. I understand that it is acceptable to consider evidence other than the information in a particular prior art document to determine if a feature is necessarily present in or inherently described by that reference.

B. Obviousness

27. I understand that a claimed invention is not patentable if it would have been obvious to a person having ordinary skill in the field of the invention at the time the invention was made.

28. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such

> that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the asserted claims of the ’789 patent would have been considered obvious as of the effective filing date of the claims in the ’789 patent.

30. When considering the issue of obviousness, I understand that I am to do the following: (i) determine the scope and content of the prior art; (ii) ascertain the differences between the prior art and the claims at issue; (iii) resolve the level of ordinary skill in the art; and (iv) consider objective evidence of non-obviousness (also known as “secondary considerations” of non-obviousness). Examples of evidence of secondary considerations of non-obviousness include evidence of commercial success, long-felt but unsolved needs, failure of others, and unexpected results. I am not presently aware of any evidence of “objective factors” suggesting any of the challenged claims of the ’789 patent are not obvious, and reserve my right to address any such evidence if it is identified in the future.

31. I understand that a person having ordinary skill is also a person of ordinary creativity.

32. My understanding is that not all innovations are patentable. Even if a claimed product or method is not disclosed in its entirety in a single prior art reference, the patent claim is invalid if the invention would have been obvious to a person having ordinary skill in the art at the time of the invention. In particular, I understand that a patent claim is normally invalid as obvious if it would have been a matter of "ordinary innovation" within the relevant field to create the claimed product or method at the time of the invention.

33. I also understand that the following exemplary scenarios would support a conclusion that a claimed product or method would have been obvious:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

- "Obvious to try" – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;
- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

34. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

35. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry disclosed in the reference(s). A reference does not "teach away" from an invention

simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (e.g., because it would not work or explicit statements saying the combination should not be made).

III. TECHNOLOGY BACKGROUND

A. Basics of Computer Architecture & Video Encoding/Decoding

1. Tom Shanley and Don Anderson, "PCI System Architecture," Third Edition, Addison-Wesley Publishing Company, Feb. 1995 ("*Shanley*") (Ex. 1019)

36. Tom Shanley and Don Anderson, "PCI System Architecture," Third Edition, Addison-Wesley Publishing Company, Feb. 1995 ("*Shanley*") describes PC architectures having a PCI bus. At the time of the alleged invention, the PCI bus, as defined in the PCI Special Interest Group's PCI Local Bus Specification Revision 2.1, was a high performance industry standard bus. *See, e.g.*, Ex. 1019, 58-60.

37. *Shanley* Figures 1-2 and 1-3 depict the application of a three-way real-time video teleconference with four video streams (one local video preview stream, two remote video streams, and a larger graphical stream).

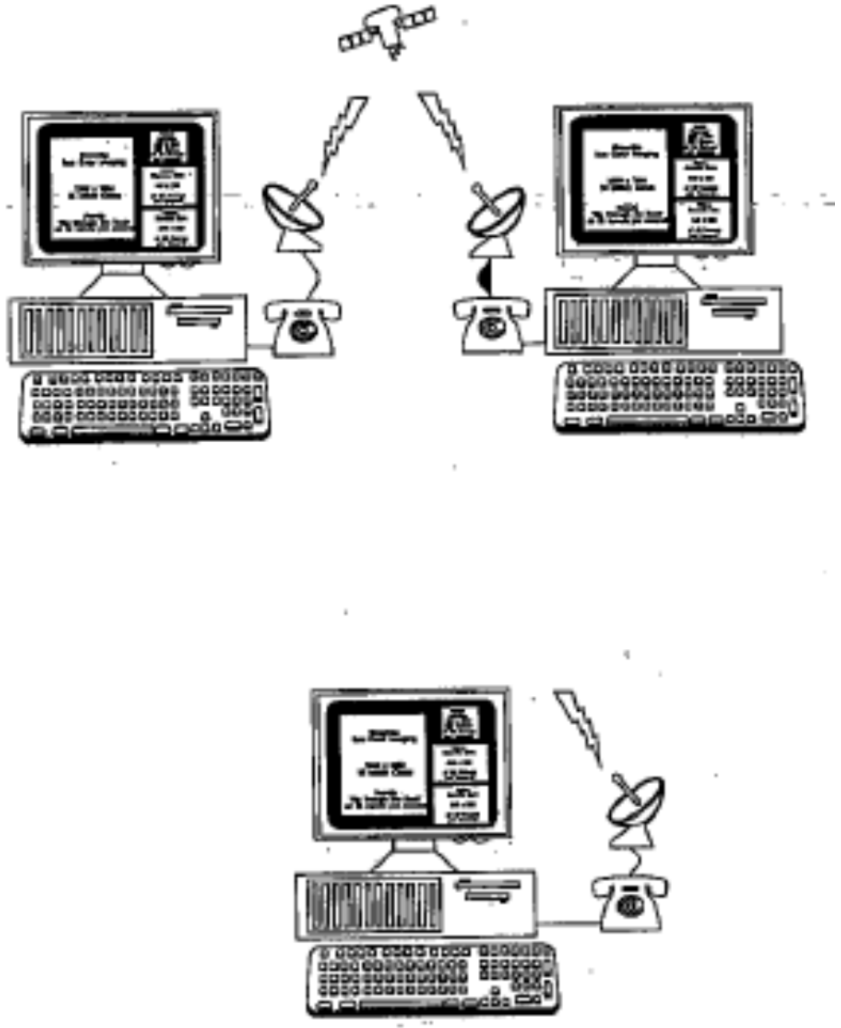


Figure 1-2. The Teleconference

Ex. 1019, 42.

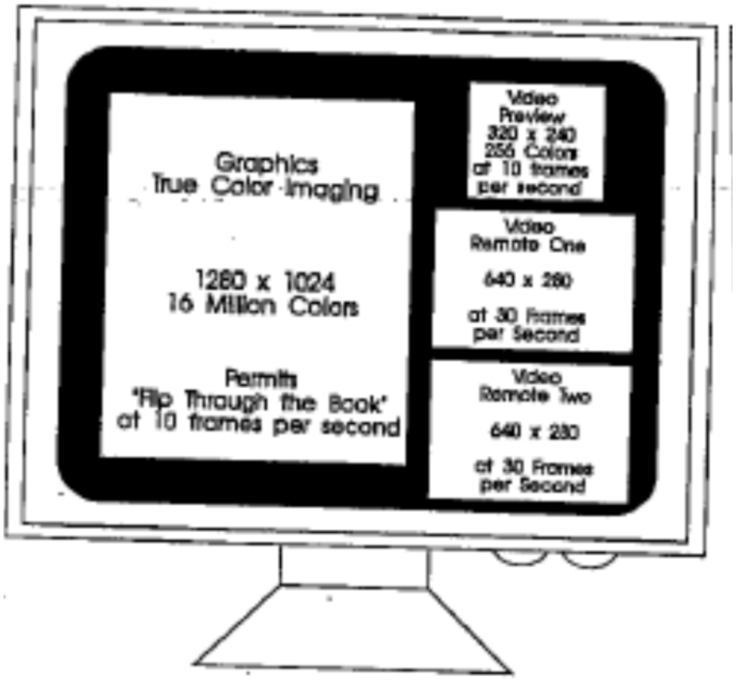


Figure 1-3. The Teleconference Screen Layout

Ex. 1019, 43.

38. The PCI bus enabled such applications. An example of a PC employing the PCI bus is shown below in Figure 2-4.

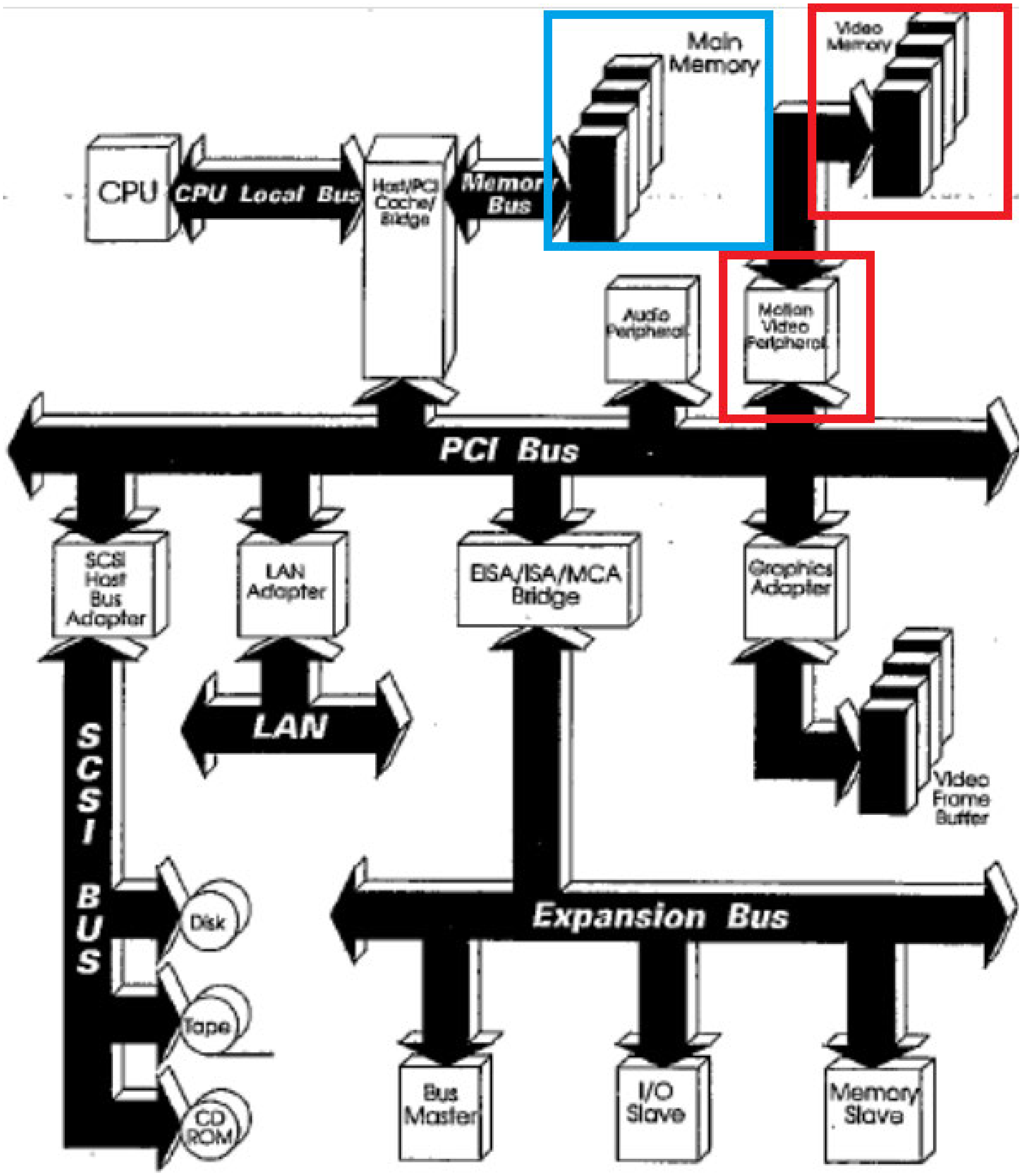


Figure 2-4. The PCI Bus

Ex. 1019, 57 (Figure 2-4, annotated).

39. As shown in Figure 2-4, the system includes a PCI bus that links a motion video peripheral, audio peripheral, graphics adapter, and other devices. The

motion video peripheral (red) has its own video memory (also red) that is separate from the main memory (blue).

40. Arbitration for access to main memory is largely left up to the designer. Ex. 1019, 92-127. In the PCI specification, each potential bus master's interface has a set of lines to handle arbitration, REQ# and GNT#. Ex. 1019, 69. The REQ# and GNT# are separately routed from each potential bus master to the arbitration mechanism:

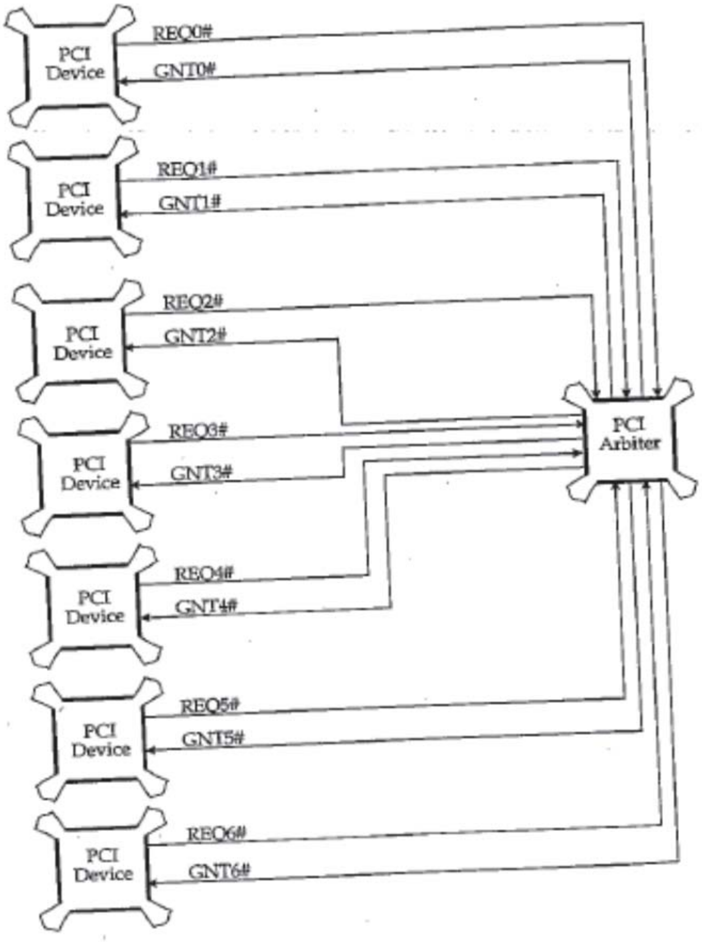


Figure 6-1. The PCI Bus Arbiter

Ex. 1019, 93 (Figure 6-1).

41. The arbiter may be a separate component or may be integrated into another device, such as the PCI chip set. *See* Ex. 1019, 92 ("Although the arbiter is shown as a separate component, it usually is integrated into the PCI chip set; specifically, it is typically integrated into the host/PCI or the PCI/expansion bus bridge chip.")

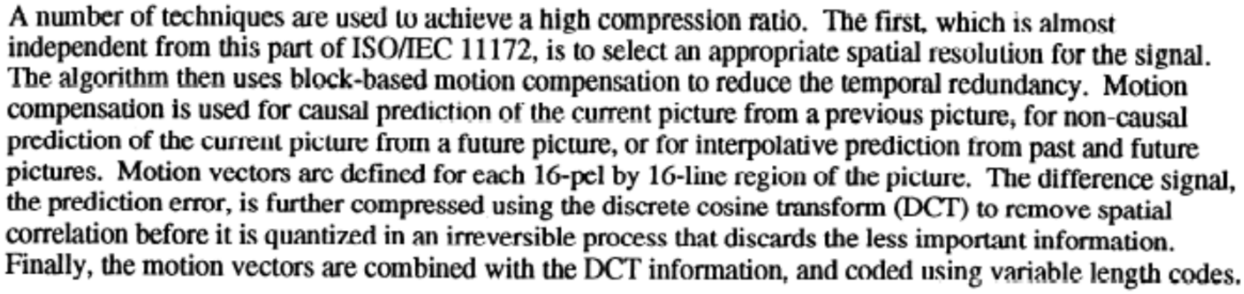
42. *Shanley* describes one particular implementation of a system using the VLSI VL82C59x SuperCore PCI chipset. Ex. 1019, 187-220.

43. In the VL82C59x chipset, the VL82C591 Pentium System Controller in combination with the two VL82C592 Pentium Processor Data Buffers incorporate the "PCI and host bus arbiters" for memory accesses by the peripherals or CPU/processor. Ex. 1019, 189-190.

44. Arbitration must be present in any system that shares access to a resource (e.g., a memory) via a bus to prevent conflicts (i.e., two devices attempting to access a memory over a bus at the same time). Ex. 1020, 4-6. I described this in my book, "Microcomputer Interfacing," first published in 1982 by Addison-Wesley Publishing Company (Ex. 1020): "the role of the arbitration lines is then very clearly defined. They guarantee that, at most, one module at a time transmits on the bus." Ex. 1020, 6.

2. International Organization for Standardization, "ISO/IEC 11172-2:1993: Information technology—Coding of moving pictures and associated audio for digital storage media at up to about 1,5 Mbit/s—Part 2: Video," 1st ed., August 1, 1993 ("*MPEG Standard*") (Ex. 1004)

45. I understand that the International Organization for Standardization, "ISO/IEC 11172-2:1993: Information technology—Coding of moving pictures and associated audio for digital storage media at up to about 1,5 Mbit/s—Part 2: Video," 1st ed., August 1, 1993 ("*MPEG Standard*") describes a video compression standard using two forms of compression: spatial and temporal. Like JPEG, spatial compression in MPEG involves compressing a single image based on blocks of pixels within the image in which the pixels have similar characteristics. Because MPEG deals with video, MPEG further includes temporal compression to compress an image based on similarities to other frames in the video sequence. As described by *MPEG Standard*:

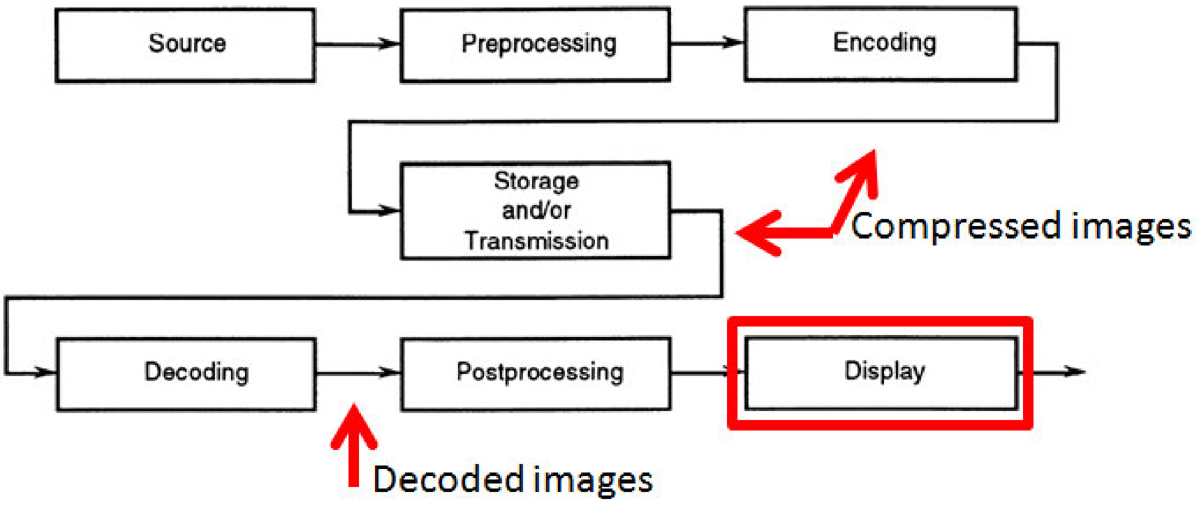


> A number of techniques are used to achieve a high compression ratio. The first, which is almost independent from this part of ISO/IEC 11172, is to select an appropriate spatial resolution for the signal. The algorithm then uses block-based motion compensation to reduce the temporal redundancy. Motion compensation is used for causal prediction of the current picture from a previous picture, for non-causal prediction of the current picture from a future picture, or for interpolative prediction from past and future pictures. Motion vectors are defined for each 16-pel by 16-line region of the picture. The difference signal, the prediction error, is further compressed using the discrete cosine transform (DCT) to remove spatial correlation before it is quantized in an irreversible process that discards the less important information. Finally, the motion vectors are combined with the DCT information, and coded using variable length codes.

Ex. 1004, 5 (§ 0.2 Overview of the algorithm).

46. The 16-pel by 16-line (16x16 pixel region) referenced above referred to as a macroblock and may vary in data size depending on the color format. Ex. 1004, 17 (2.1.86 macroblock [video]).

47. The compression disclosed in *MPEG Standard* is useful for storage and/or transmission. Videos can be encoded to reduce bandwidth or memory requirements during storage or transmission and subsequently decoded for display.

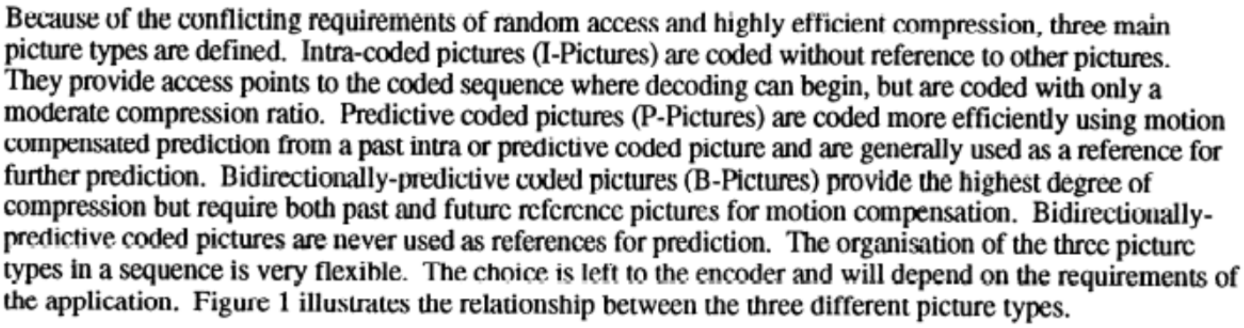


Compressed images

Decoded images

Ex. 1004, 62 (Figure D.1, annotated).

48. To permit predictive and non-causal interpolative temporal processing, *MPEG Standard* defines three picture types:



Because of the conflicting requirements of random access and highly efficient compression, three main picture types are defined. Intra-coded pictures (I-Pictures) are coded without reference to other pictures. They provide access points to the coded sequence where decoding can begin, but are coded with only a moderate compression ratio. Predictive coded pictures (P-Pictures) are coded more efficiently using motion compensated prediction from a past intra or predictive coded picture and are generally used as a reference for further prediction. Bidirectionally-predictive coded pictures (B-Pictures) provide the highest degree of compression but require both past and future reference pictures for motion compensation. Bidirectionally-predictive coded pictures are never used as references for prediction. The organisation of the three picture types in a sequence is very flexible. The choice is left to the encoder and will depend on the requirements of the application. Figure 1 illustrates the relationship between the three different picture types.

Ex. 1004, 5 (§ 0.2.1 Temporal processing).

49. As stated above, I-pictures are coded without reference to other pictures, P-pictures are coded with reference to past pictures, and B-pictures are coded with reference to past and future pictures and are never used as references for prediction.

50. The following figure illustrates the relationship between the three picture types:

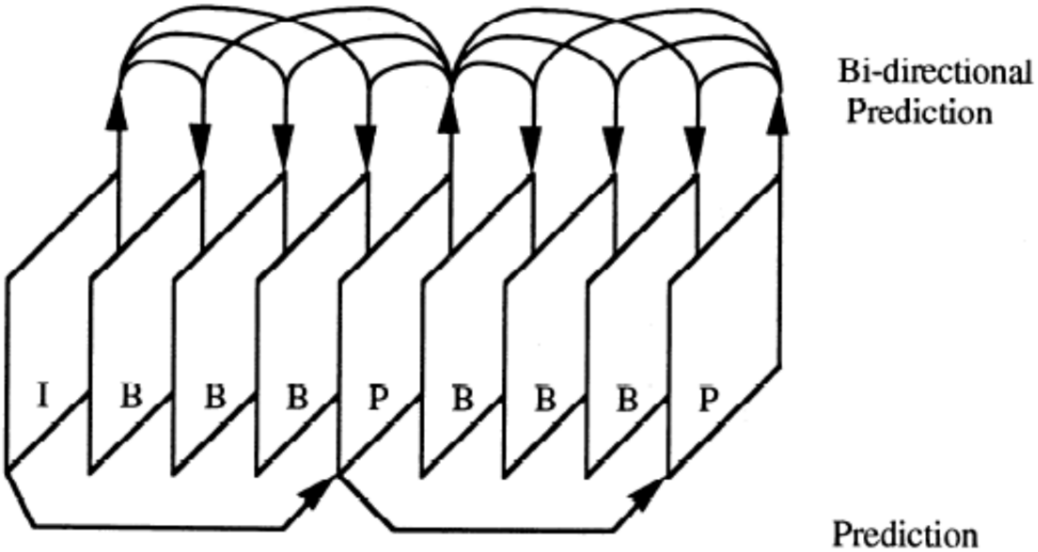
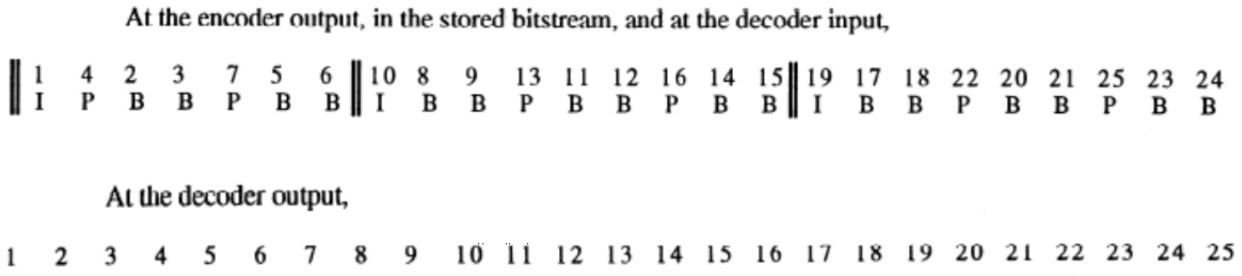


Figure 1 -- Example of temporal picture structure

Ex. 1004, 5 (Figure 1).

51. Note that in decoding, if a B-picture was encoded with reference to a previous P-picture and a subsequent P-picture (in sequence), the two P-pictures are decoded in time (but not displayed in time) prior to the decoding of the B-picture:



At the encoder output, in the stored bitstream, and at the decoder input,

1	4	2	3	7	5	6	10	8	9	13	11	12	16	14	15	19	17	18	22	20	21	25	23	24
I	P	B	B	P	B	B	I	B	B	P	B	B	P	B	B	I	B	B	P	B	B	P	B	B

At the decoder output,

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

Ex. 1004, 24-25.

52. *MPEG Standard* depicts a simplified decoder implementation:

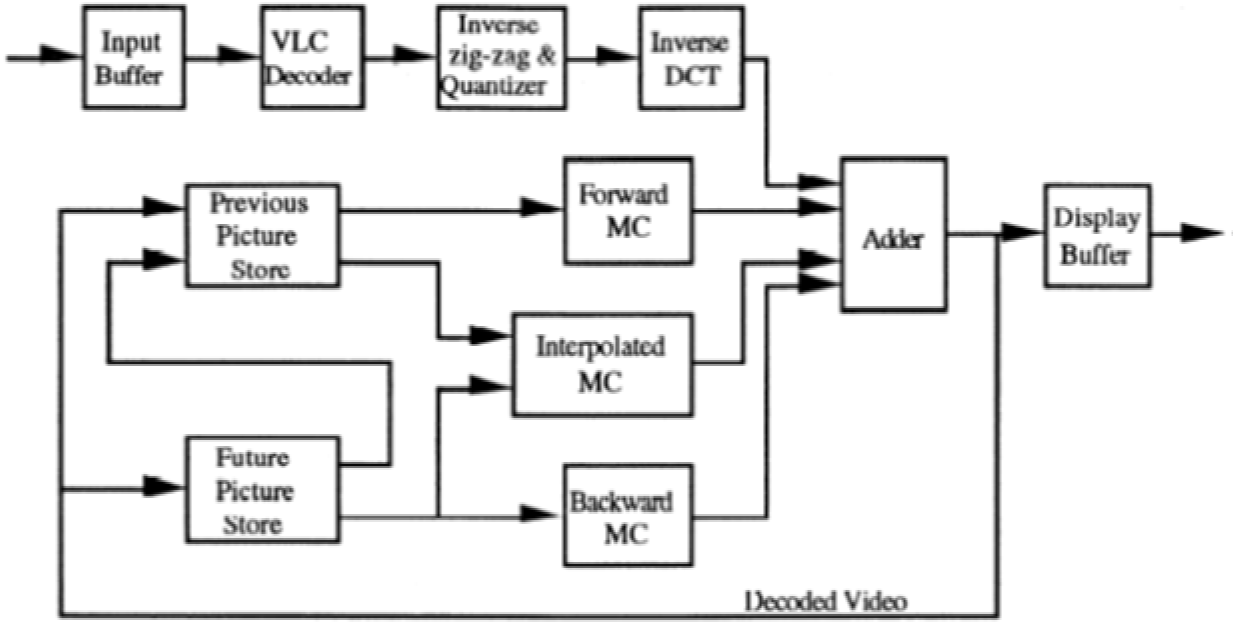


Figure D.7 -- Simplified decoder block diagram

Ex. 1004, 66 (Figure D.7).

53. As shown above, the decoder receives an encoded or compressed bitstream from a source (e.g., a memory). The VLC decoder, inverse zig-zag and quantizer, and inverse DCT blocks decode the bitstream, and then the various motion compensation blocks act (for the various picture types). Two frame stores

are present, one for past and one for future frames to facilitate decoding of B-pictures. Once a frame is no longer needed, it may be output to a display buffer for display. Note that the MPEG Standard does not restrict the location of the picture stores. In the absence of such a constraint conforming implementations could use shared memory or a combination of shared and dedicated memory.

B. The Consolidation of MPEG and Other Multimedia Device's Memory

54. One widely recognized goal in computing was reducing cost. As detailed below, one well known technique to reduce cost was to eliminate dedicated memory associated with an MPEG or other media device.

1. Intel Corporation "Acceleration Graphics Port Interface Specification," Revision 1.0 ("*AGP*") (Ex. 1024)

55. The stated purpose of Intel Corporation "Acceleration Graphics Port Interface Specification," Revision 1.0 ("*AGP*") was to control costs by sharing memory:

> In general, 3D rendering has a voracious appetite for memory bandwidth, and continues to put upward pressure on memory footprint as well. As 3D hardware and software become more pervasive, these two trends are likely to accelerate, requiring high speed access to ever larger amounts of memory, thus raising the bill of

> material costs for 3D enabled platforms. Containing these costs while enabling performance improvements is the primary motivation for the A.G.P.. *By providing up to an order of magnitude bandwidth improvement between the graphics accelerator and system memory, some of the 3D rendering data structures may be effectively shifted into main memory, relieving the pressure to increase the cost of the local graphics memory*.

Ex. 1024, 11 (Motivation) (emphasis added).

2. Video Electronics Standards Association published the "VESA Unified Memory Architecture Hardware Specifications Proposal," Version 1.0p ("*VUMA*") (Ex. 1025)

56. Video Electronics Standards Association published the "VESA Unified Memory Architecture Hardware Specifications Proposal," Version 1.0p ("*VUMA*") stated purpose was to eliminate the need for a component to incorporate a dedicated memory by instead using a shared system memory to serve as the component's memory:

> The concept of VESA Unified Memory Architecture (VUMA) is to share physical system memory (DRAM) between system and an external device, a VUMA device; as shown in Figure 1-1. A VUMA device could be any

> type of controller which needs to share physical system memory (DRAM) with system and directly access it. One example of a VUMA device is graphics controller. In a VUMA system, graphics controller will incorporate graphics frame buffer in physical system memory (DRAM) or in other words VUMA device will use a part of physical system memory as its frame buffer, thus, sharing it with system and directly accessing it. *This will eliminate the need for separate graphics memory, resulting in cost savings*.

Ex. 1025, 6 (Introduction) (emphasis added).

3. U.S. Patent No. 5,774,676 to Stearns ("*Stearns*") (Ex. 1007)

57. *Stearns* issued June 30, 1998 based on an application filed on October 3, 1995. *See* Ex. 1007.

58. *Stearns* described the MPEG accelerator circuit in Figure 2 below as "a dedicated digital signal processor for video decompression." *See* Ex. 1007, 6:56-57.

59. In contrasting Figures 2 and 3, below, *Stearns* discloses eliminating MPEG accelerator 46's private memory 44 (red) and satisfying the memory

requirements by sharing either frame buffer 38 or system memory 36 (blue). *See* Ex. 1007, 5:63-6:7.

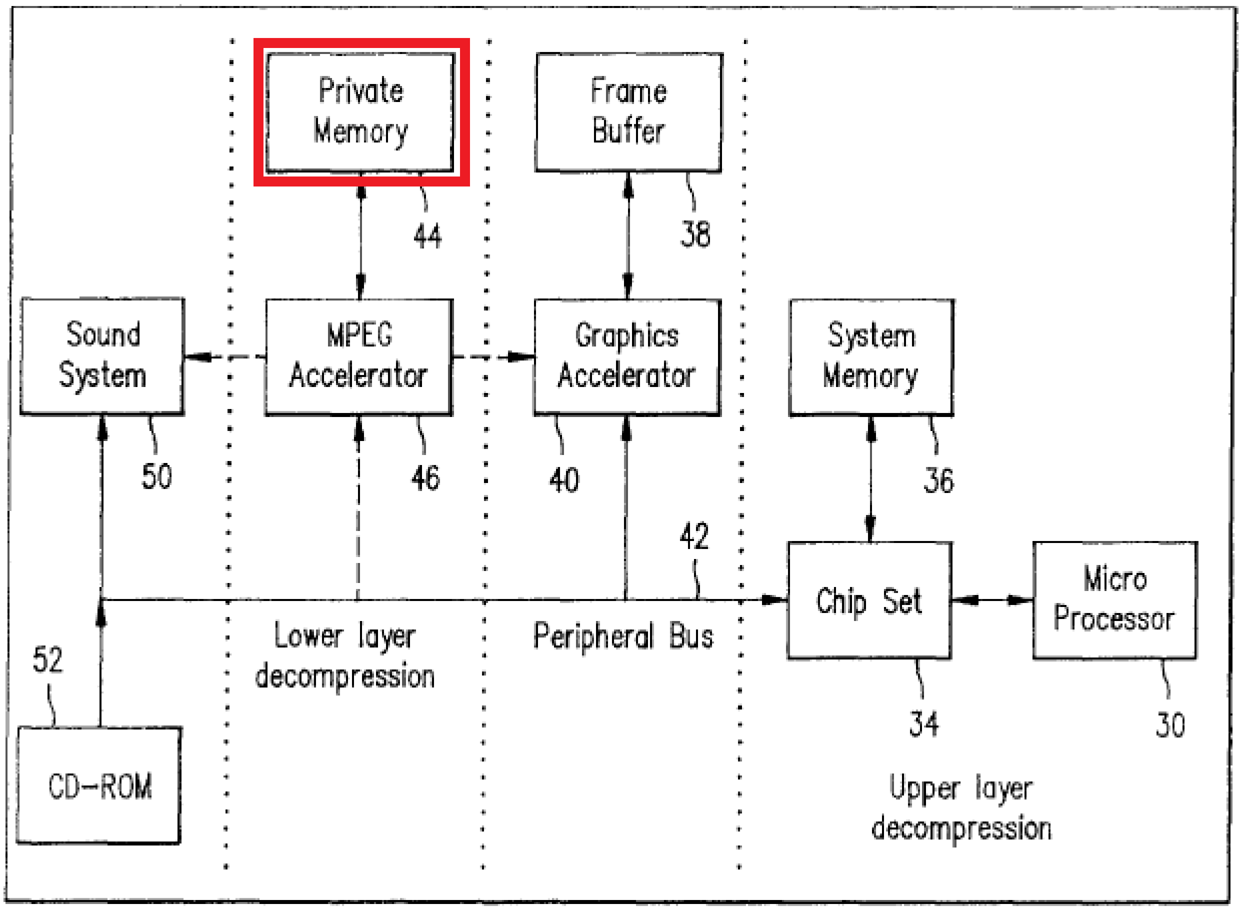


FIG. 2

Ex. 1007, Figure 2 (annotated).

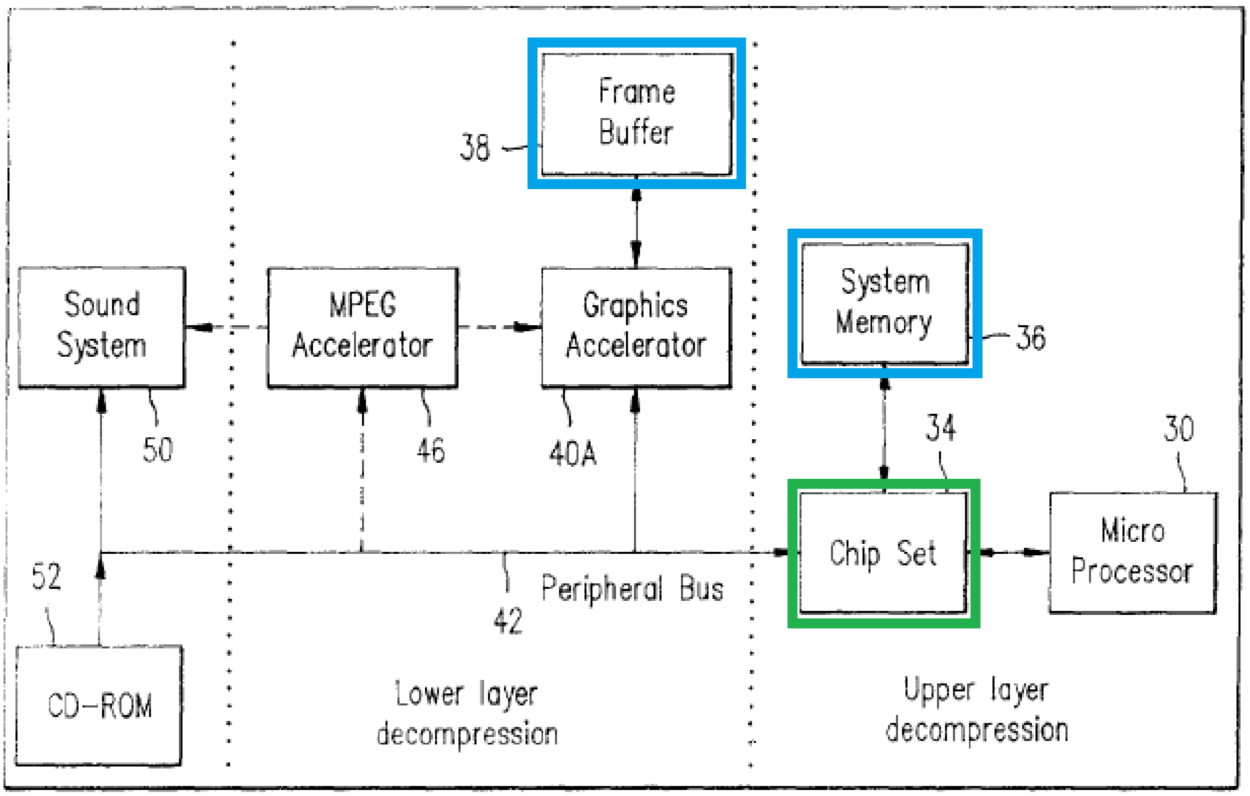


FIG. 3

Ex. 1007, Figure 3 (annotated).

60. *Stearns* describes the core logic chip set (above, green) as follows: "The core logic chip set of a computer interfaces the microprocessor to the peripherals, manages the memory subsystem, arbitrates usage and maintains coherency." Ex. 1007, 3:53-55.

4. U.S. Patent No. 5,797,028 to Gulick ("*Gulick 028*") (Ex. 1023)

61. *Gulick 028* issued based on an application filed on September 11, 1995. *See* Ex. 1023.

62. *Gulick 028* Figure 2, below, depicts a digital system chip 112 (red) having a general purpose DSP 206 (blue).

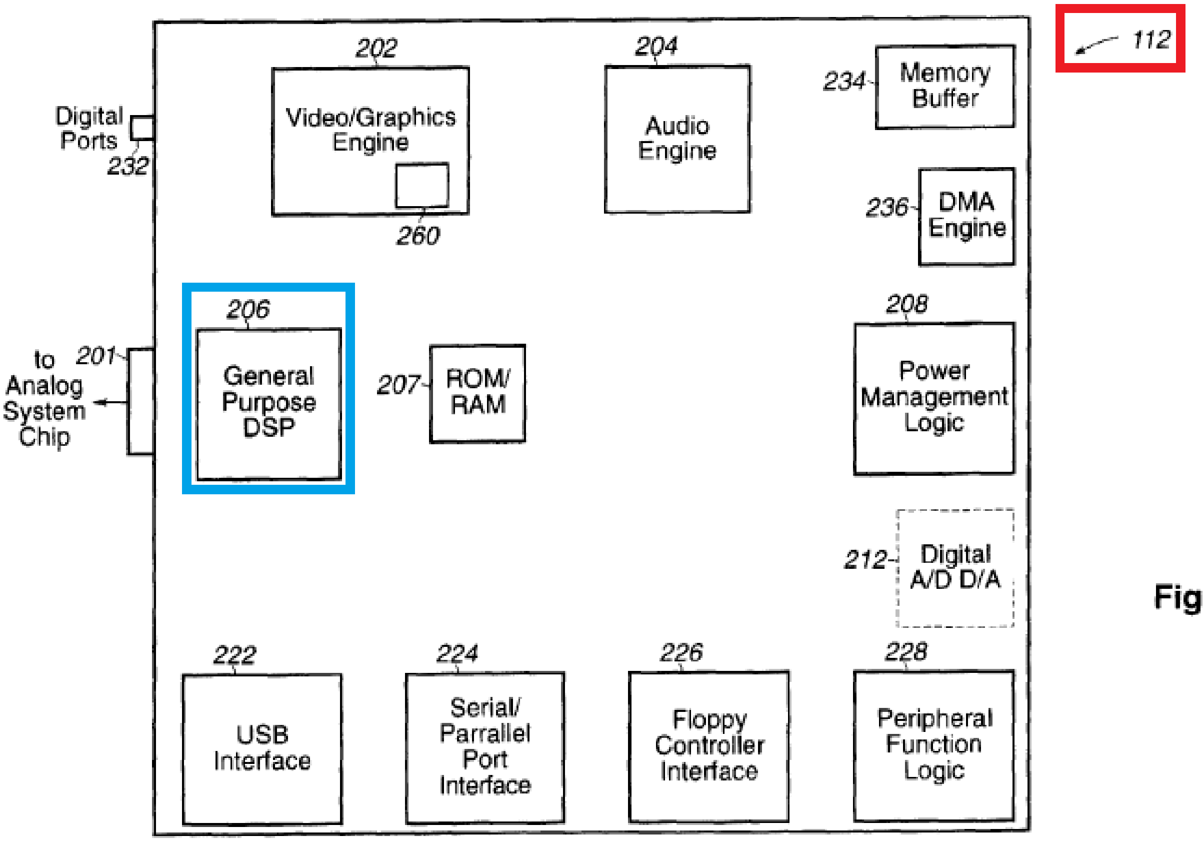
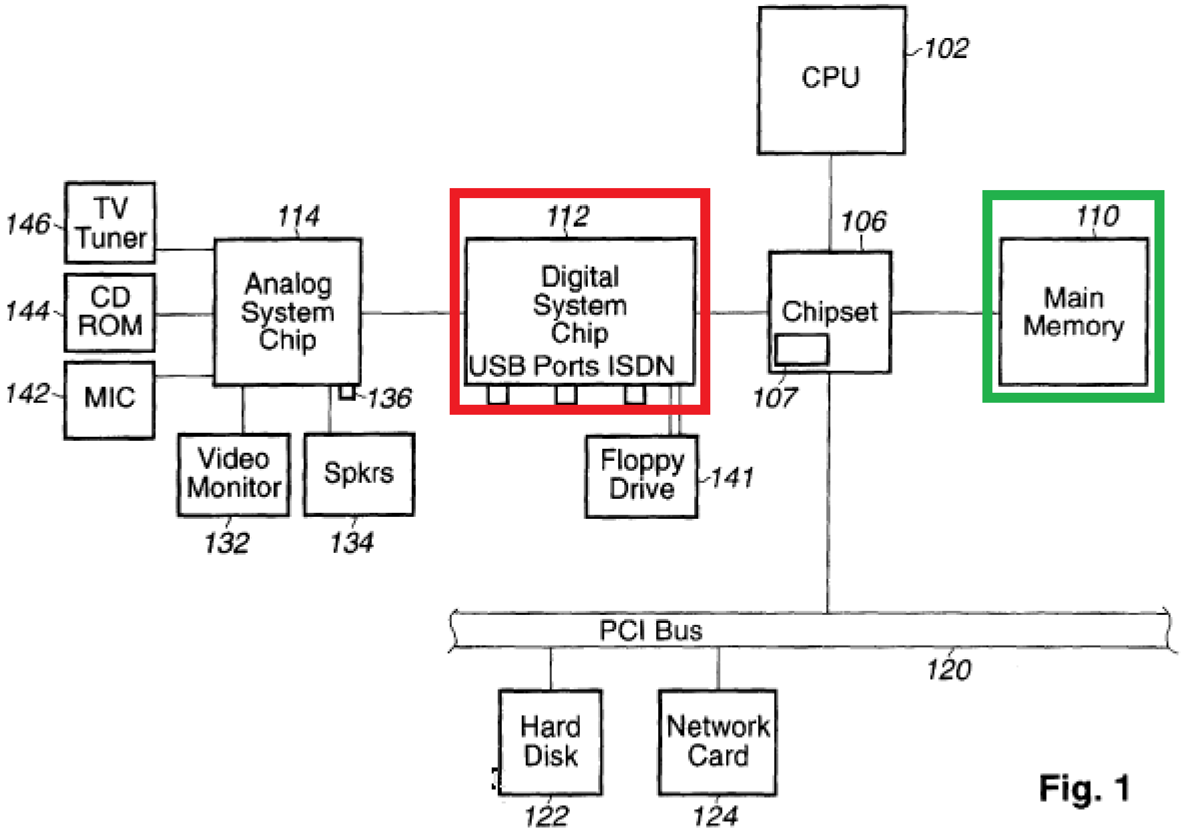


Fig. 2

Ex. 1023, Figure 2 (annotated).

63. *Gulick 028* explains that “[t]he digital system chip 112 also preferably includes a general purpose DSP engine 206 which is programmable to perform various functions, such as MPEG decoding . . . .” Ex. 1023, 6:20-24.

64. *Gulick 028* Figure 1, below, places the digital system chip 112 (red) in context in the larger system.



Ex. 1023, Figure 1 (annotated).

65. *Gulick 028* discloses:

> *In one embodiment, the digital system chip 112 does not include multimedia memory, but rather video data and audio data are stored in the system memory 110 according to a unified memory architecture*. In this embodiment, the digital system chip 112 preferably includes a memory buffer 234 and a direct memory access (DMA) engine 236 for transferring data from the

> main memory 110 to the memory buffer 234 in the digital system chip 112.

Ex. 1023, 6:48-55.

66. That is, *Gulick 028's* MPEG decoder operates out of main or system memory 110 depicted above in Figure 1 (green).

IV. SUMMARY OF THE '789 PATENT

A. Effective Filing Date of the '789 patent

67. The '789 patent issued from U.S. Application No. 702,911 filed August 26, 1996. Ex. 1001 at Face. I therefore understand that the effective filing date of the claims of the '789 patent is no earlier than August 26, 1996.

B. Overview of the '789 patent

68. I have reviewed the '789 patent to identify its novel aspects as one skilled in the art would view them. My high-level summary is that the alleged novelty is how to use shared memory within a video system to reduce cost without compromising the ability to meet video processing performance requirements. For example, under the "Summary of the Invention," the '789 patent specification states:

> Both the first device and the video and/or audio decompression and/or compression device require access to a memory. The video and/or audio decompression

> and/or compression device *shares the memory with the first device*.

Ex. 1001, 3:65-4:2 (emphasis added).

69. The ’789 patent concerns the arbitration for access to a memory shared between a video decoder and another device, such as a central processing unit (CPU). The inventors conceded that video coding and decoding techniques such as MPEG, H.261, and H.263 were “well accepted standards” at the time. But, the inventors alleged, a video decoder conventionally would be given its own dedicated memory, to allow it to operate in “real time.”[1] The dedicated memory would remain unused most of the time and significantly increase costs. To address these alleged problems, the inventors proposed having the video decoder share memory with other devices. The ’789 patent accomplishes this using an arbiter, which arbitrates between the video decoder and the device when either one requests access to the memory.

C. The Prosecution History of the ’789 patent

70. The original application for the ’789 patent contained 49 claims. These claims were rejected as being anticipated by Lin et al., On the Bus Arbitration for MPEG 2 Video Decoder, and obvious in view of U.S. Patent No.

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[1] The ’789 patent never defines “real time.”

5,557,538 (Retter et al.) and U.S. Patent No. 5,522,080 (Harney). Ex. 1002, 93, 94. In response, most notably with respect to the claims challenged here, the Applicant amended what later issued as claims 1 and 13. *Id.*, 105-108. For example, independent claim 1 was amended to additionally recite “and a shared bus coupled to the memory, the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.” *Id.* This claim and its dependent claims were subsequently allowed.

D. Claim Construction

71. I understand that a claim subject to *inter partes* review receives the broadest reasonable interpretation in light of the specification and file history of the patent in which it appears. I also understand that any term that is not construed should be given its plain and ordinary meaning under the broadest reasonable interpretation. I have followed these principles in my analysis. I discuss certain claim terms below and what I understand to be Petitioners’ construction of these terms, which I apply in my analysis. The remaining claim terms in the ’789 patent are given their plain and ordinary meaning under the broadest reasonable interpretation, which I also apply in my analysis.

72. I understand that Petitioners have proposed that the broadest reasonable interpretation of the claimed term “video decoder” is “hardware and/or

software that translates data streams into video information." I agree with this construction based on the claims and specification of the '789 patent. For example, the '789 patent generally refers to a decoder as a "video and/or audio decompression device." Ex. 1001, 1:46-51. According to the specification, "[a]ny *conventional decoder* including a decoder complying to the MPEG-1, MPEG-2, H.261, or H.261 standards, or any combination of them, or any other conventional standard *can be used as the decoder*/encoder." *Id.*, 12:23-27 (emphasis added). A conventional decoder around the time of the alleged invention of the '789 patent was understood to include "any hardware or software system that translates data streams into video or audio information." Ex. 1014 at 3. Consistent with this understanding of a decoder, the '789 patent acknowledges that a decoder can be implemented as hardware or software. *See, e.g.*, Ex. 1001, 5:43-45. In one example, the specification explains that video decoding can be performed by hardware and audio decoding can be performed by software. *Id.*, 5:50-56.

73. I have been asked to assume that the broadest reasonable interpretation of the claimed term "real time" is "fast enough to keep up with an input data stream." I have applied this understanding in my analysis.

V. LEVEL OF ORDINARY SKILL IN THE ART

74. I understand that the claims of a patent are reviewed from the point of view of a hypothetical person having ordinary skill in the art as of the effective filing date of the ’789 patent.

75. Based on my review of the ’789 patent specification, claims, and file history, in my opinion, a person having ordinary skill in the art as of the effective filing date of the ’789 patent would have held an accredited Bachelor’s degree in Electrical Engineering and/or Computer Science and/or Computer Engineering and had three years’ experience in the fields of data compression and overall computer system architecture.

76. The reason that I have chosen that definition of a person having ordinary skill in the art for the ’789 patent is because that person would have been exposed to compression techniques described in the ’789 patent. That person would also be familiar with the basic computer components recited in the claims and would understand how to use those components to build a multimedia processing system using shared resources like a memory.

77. As described in more detail above, I was a person with at least ordinary skill in the art as of the effective filing date of the ’789 patent.

VI. COMPARISON OF THE PRIOR ART TO THE ’789 PATENT

A. Ground A: *Lambrecht* anticipates, under 35 U.S.C. § 102, claims 1, 3, 5, 11, and 13

1. Claim 1

78. In my opinion, *Lambrecht* discloses every feature of claim 1.

Claim Language	*LAMBRECHT*
[1.0] An electronic system coupled to a memory, comprising:	*Lambrecht* discloses an electronic system coupled to a memory. *See, e.g.*, Ex. 1032, *Lambrecht* at Fig. 21 (annotated below); *see also id.* at 27:4-9, 26:51-56 (“The computer system of FIG. 21 is similar to the computer system of FIG. 1. However, the mode logic in the computer system of FIG. 21 is operable to place the PCI bus 120 in either a normal PCI mode or in a real-time/multimedia mode optimized for multimedia transfers of periodic data.”).

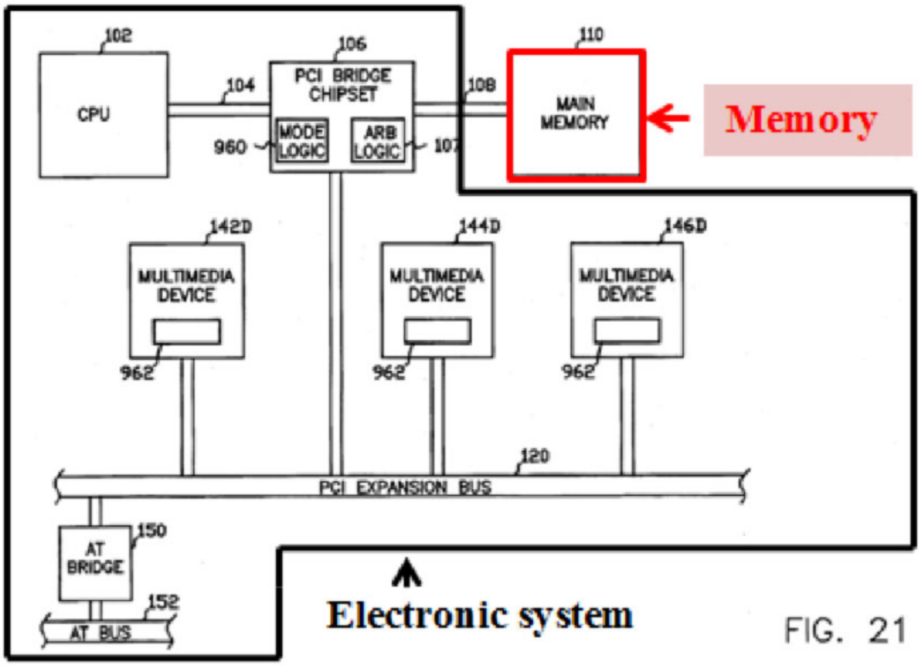
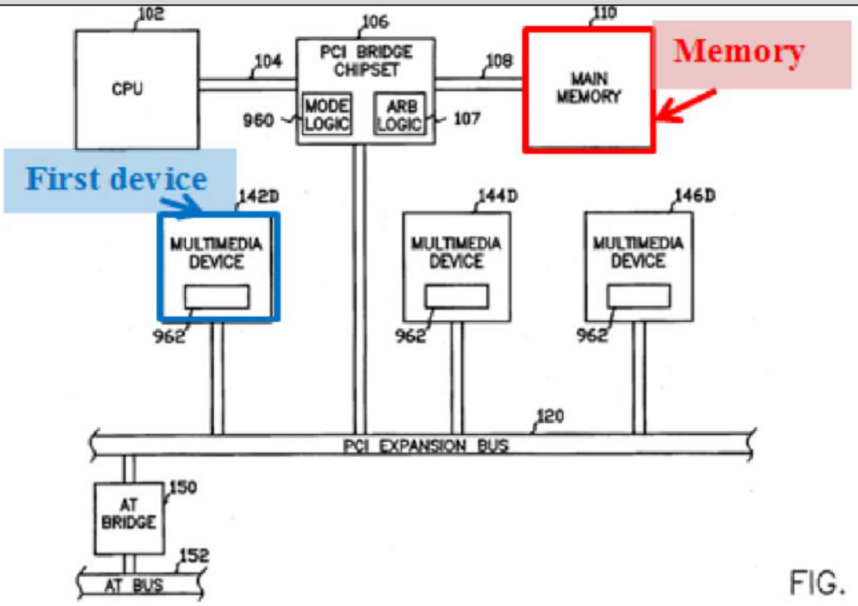
<table>
<tr><th>Claim Language</th><th>LAMBRECHT</th></tr>
<tr><td></td><td>


FIG. 21

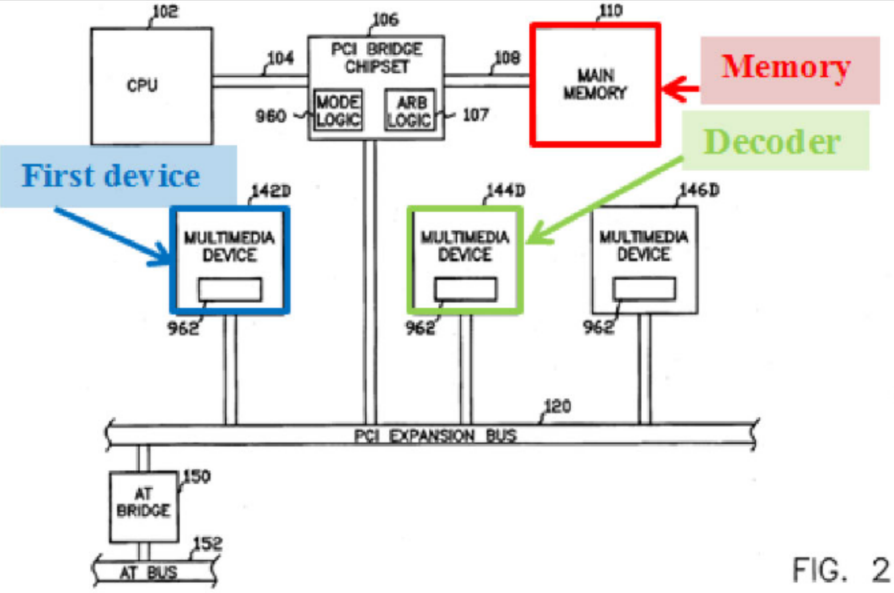
At Fig. 21 (annotations added).

In particular, *Lambrecht* teaches an electronic system that includes a CPU, chipset, and various multimedia devices. *See id.* A dynamic random access memory (DRAM) acts as main memory and is coupled to the electronic system. *See, e.g., id.* at 27:4-9 ("The bridge or chipset 106 couples through a memory bus 108 to main memory 110. The main memory 110 is preferably DRAM (dynamic random access memory) or EDO (extended data out) memory, or other types of
</td></tr>
</table>

Claim Language	*LAMBRECHT*
	memory, as desired. The chipset logic 106 preferably includes a memory controller for interfacing to the main memory 110."), Fig. 21; *see also* analysis and citations below for other claim elements.
[1.1] a first device that requires access to the memory;	*Lambrecht* discloses a first device (light blue) that requires access to the memory (red). *See, e.g.*, Ex. 1032 at Fig. 21; 27:4-9. In particular, *Lambrecht* discloses a first device that requires access to the memory. *See, e.g.*, Ex. 1032, Fig. 21 (annotated below), 27:32-34 ("One or more multimedia devices or *multimedia devices 142D, 144D, and 146D* are coupled to each of the PCI bus 120 and the multimedia bus 130.") (emphasis added).

Claim Language	*Lambrecht*
	 FIG. 21 At Fig. 21 (annotations added). *Lambrecht* adds: The *multimedia devices 142D-146D* may be any of various types of input/output devices, including multimedia devices and communication devices, as described above. The multimedia devices 142D-146D are preferably similar to the multimedia devices 142-146 described above, except that the interface logic 962 in the multimedia devices 142D-146D each include the interface logic for interfacing to the PCI bus 120 in multiple modes. As described above, the multimedia devices 142D-146D may

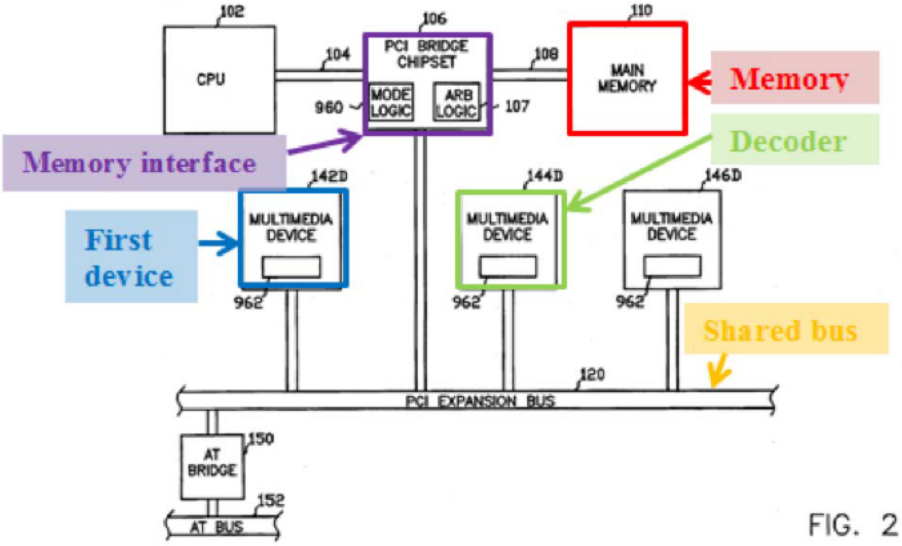
Claim Language	***Lambrecht***
	comprise video accelerator or graphics accelerator cards, video playback cards, MPEG decoder cards, sound cards, network interface cards, SCSI adapters for interfacing to various input/output devices, such as CD-ROMS and tape drives, or other devices as desired. *See id.* at 27:43-56 (emphasis added). The first device disclosed in *Lambrecht* requires access to memory. *See id.*at 27:57-59 ("Thus, the multimedia devices 142D-146D communicate with each other and with the CPU 102 and main memory 110 via the PCI bus 12 as is well known in the art.").
[1.2] a decoder that requires access to the memory sufficient to maintain real time operation; and	*Lambrecht* discloses a decoder that requires access to the memory sufficient to maintain real time operation. *See, e.g.*, Ex. 1032 at Fig. 21 (annotated below), 27:32-34 ("One or more multimedia devices or *multimedia devices 142D, 144D, and 146D* are coupled to each of the PCI bus 120 and the multimedia bus 130.") (emphasis added).

Claim Language	***LAMBRECHT***
	 FIG. 21 At Fig. 21 (annotations added). *Lambrecht* describes that one of the several multimedia devices is a decoder: The *multimedia devices 142D-146D* may be any of various types of input/output devices, including multimedia devices and communication devices, as described above. The multimedia devices 142D-146D are preferably similar to the multimedia devices 142-146 described above, except that the interface logic 962 in the multimedia devices 142D-146D each include the interface logic for interfacing to the PCI bus 120 in multiple modes. As described above,

Claim Language	*LAMBRECHT*
	the multimedia devices 142D-146D may comprise video accelerator or graphics accelerator cards, video playback cards, *MPEG decoder cards*, sound cards, network interface cards, SCSI adapters for interfacing to various input/output devices, such as CD-ROMS and tape drives, or other devices as desired. *See id.* at 27:43-56 (emphasis added). In other words, *Lambrecht* discloses an arrangement in which multimedia device 144D is a decoder (i.e., an MPEG decoder card). The decoder disclosed in *Lambrecht* requires access to memory. *See id.* at 27:57-59 ("Thus, the multimedia devices 142D-146D communicate with each other and with the CPU 102 and main memory 110 via the PCI bus 120, as is well known in the art."). The memory access is sufficient to operate in real time. *See id.* at 27:66-28:2 ("In the preferred embodiment of the invention of FIG. 21, the multimedia mode comprises

Claim Language	***Lambrecht***
	placing the system bus or *PCI bus 120* in a special mode optimized for *real-time data transfers*.”); *see also*: - “Referring now to FIG. 21, a computer system is shown which includes an expansion bus, preferably a PCI bus 120, and which includes mode logic which selects between different modes of the PCI bus 120. The computer system of FIG. 21 is similar to the computer system of FIG. 1. However, the mode logic in the computer system of FIG. 21 is operable *to place the PCI bus 120* in either a normal PCI mode or *in a real-time/multimedia mode* optimized for multimedia transfers of periodic data. As described below, multimedia devices use the PCI bus 120 for normal PCI transfers and also use the PCI bus fines in the multimedia mode for high speed data multimedia transfers, preferably transfers of periodic multimedia data. In the following description, elements which are preferably identical to elements previously described include the same reference numerals for convenience.” *Id.* at 26:48-63 (emphasis added).

Claim Language	*LAMBRECHT*
	• "In one embodiment, the system bus (preferably PCI) implements a new mode of operation specifically *for real-time transfers***.** A signal (or signals) is used to indicate that the system bus should be placed in a special real time mode. When not in special real time mode, the system bus operates as usual. The *real time mode* is optimized for the transfer of high bandwidth real-time information. Therefore, the present invention comprises a novel computer system architecture and method which provides one or more real-time or multimedia buses, optionally with a local expansion bus, to increase the performance of *real-time peripherals and applications*. The multimedia bus of the present invention provides *improved data transfers performance and throughput for real-time devices*. The various embodiments discussed above may be combined in various ways for *optimum real-time and/or multimedia performance*." *Id.* at 5:33-48 (emphasis added).

Claim Language	***LAMBRECHT***
[1.3] a memory interface for coupling to the memory, and coupled to the first device and to the decoder, the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient	*Lambrecht* discloses this limitation. *See, e.g.*, Ex. 1032 at Fig. 21 (annotated below).  FIG. 21 *Lambrecht*'s chipset is a memory interface having an arbiter. *See, e.g.*, Ex. 1032 at 7:45-47 ("The chipset logic 106 preferably includes a memory controller for interfacing to the main memory 110 and also includes the arbitration logic 107."); *see also id.*, 26:66-27:2. *Lambrecht* discloses the memory interface is coupled to memory, the first device, and the decoder: As shown, the computer system includes a central processing unit (CPU) 102 which is coupled through a CPU local bus 104 to a host/PCI/cache bridge or chipset 106. The

Claim Language	***LAMBRECHT***
bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.	chipset 106 includes various bridge logic and includes *arbitration logic 107*. The chipset 106 is preferably similar to the Triton chipset available from Intel Corporation, including certain arbiter modifications to accommodate the real-time bus of the present invention. A second level or L2 cache memory (not shown) may be coupled to a cache controller in the chipset 106, as desired. The bridge or chipset 106 *couples through a memory bus 108 to main memory 110***.** The *main memory 110* is preferably DRAM (dynamic random access memory) or EDO (extended data out) memory, or other types of memory, as desired. The chipset logic 106 preferably includes *a memory controller for interfacing to the main memory 110* and also includes the *arbitration logic 107*. *See id.* at 7:30-47 (emphasis added); *see also id.* at 26:66-27:9, Fig. 21 (annotated above). The memory interface (i.e. the chipset) includes an arbiter

Claim Language	***Lambrecht***
	that "selectively provid[es] access for the first device and the decoder to the memory and a shared bus coupled to the memory the first device, and the decoder," as claimed. *See, e.g.,* Ex. 1032 at 26:66-27:2 ("The chipset logic 106 preferably includes a memory controller for interfacing to the main memory 110 and also includes the arbitration logic 107."); *see also* Fig. 21 (annotated above). Furthermore, *Lambrecht*'s bus is of "sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus," as claimed. *Lambrecht* teaches a design that allows real-time operation of a bus while simultaneously allowing access to two different devices. *See, e.g.*, Ex. 1032 at 5:33-48; 27:66-28:11. *Lambrecht* discloses a "byte sliced mode" that divides the bus into different byte lanes, which allows for two different simultaneous data transfers. *See* Ex. 1032 at 27:66-28:11. *Lambrecht* adds: In one embodiment, the centralized

Claim Language	***Lambrecht***
	> multimedia I/O processor byte slices the multimedia bus to allow different data streams to use *different byte channels simultaneously*. Thus the *byte sliced* multimedia bus allows different peripherals *to share the bus simultaneously*. The centralized multimedia I/O processor thus may assign one data stream to a subset of the total byte lanes on the multimedia bus, and fill the unused byte lanes with another data stream. For example, with a 32-bit multimedia bus, if an audio data stream is only 16 bits wide and thus only uses half of the multimedia data bus, the multimedia bus intelligently allows data stream transfers on the unused bits of the bus. In this embodiment, the centralized multimedia I/O processor includes knowledge of the destinations and allows transfers to occur without addressing information. *Lambrecht* at 5:17-33 (emphasis added). Byte slice mode allows for simultaneous, real-time video and audio transfers over the same PCI bus:

Claim Language	***LAMBRECHT***
	In the preferred embodiment of the invention of FIG. 21, the multimedia mode comprises placing the system bus or PCI bus 120 in a special mode optimized for *real-time data transfers*. In one embodiment of FIG. 21, the special mode comprises *a byte sliced mode* which uses different byte lanes or channels of the PCI data lines for different types of *multimedia transfers* as described above. Thus, 16 bits of the *PCI bus* may be used for *video transfers* while the remaining 16 bits may be used for *audio transfers simultaneously*. Alternatively, the special mode comprises placing the PCI bus 120 in a time sliced or time slotted mode as described above with reference to FIGS. 11 and 12. In another embodiment, the special or real time mode comprises placing the PCI bus 120 in mode for performing periodic multimedia data transfers as described above. Other types of multimedia modes may be used as desired. *See id.* at 27:66-28:11 (emphasis added).

Claim Language	***Lambrecht***
	By using byte slice mode over the PCI bus disclosed in *Lambrecht* (*see* Fig. 21 (annotated above)), the bus has sufficient bandwidth to allow real-time access to memory to both the first device (for example, an audio circuit) and the decoder. *See also*: • "In one embodiment, the centralized multimedia I/O processor byte slices the multimedia bus to allow different data streams to use *different byte channels simultaneously*. Thus the byte sliced multimedia bus allows different peripherals *to share the bus simultaneously*. The centralized multimedia I/O processor thus may assign one data stream to a subset of the total byte lanes on the multimedia bus, and fill the unused byte lanes with another data stream. For example, with a 32-bit multimedia bus, if an audio data stream is only 16 bits wide and thus only uses half of the multimedia data bus, the multimedia bus intelligently allows data stream transfers on the unused bits of the bus. In this embodiment, the centralized multimedia I/O processor

Claim Language	*LAMBRECHT*
	includes knowledge of the destinations and allows transfers to occur without addressing information." *Id.* at 19:39-54 (emphasis added). *See also*: • "Referring now to FIG. 21, a computer system is shown which includes an expansion bus, preferably a PCI bus 120, and which includes mode logic which selects between different modes of the PCI bus 120. The computer system of FIG. 21 is similar to the computer system of FIG. 1. However, the mode logic in the computer system of FIG. 21 is operable *to place the PCI bus 120* in either a normal PCI mode or *in a real-time/multimedia mode* optimized for multimedia transfers of periodic data. As described below, multimedia devices use the PCI bus 120 for normal PCI transfers and also use the PCI bus fines in the multimedia mode for high speed data multimedia transfers, preferably transfers of periodic multimedia data. In the following description, elements

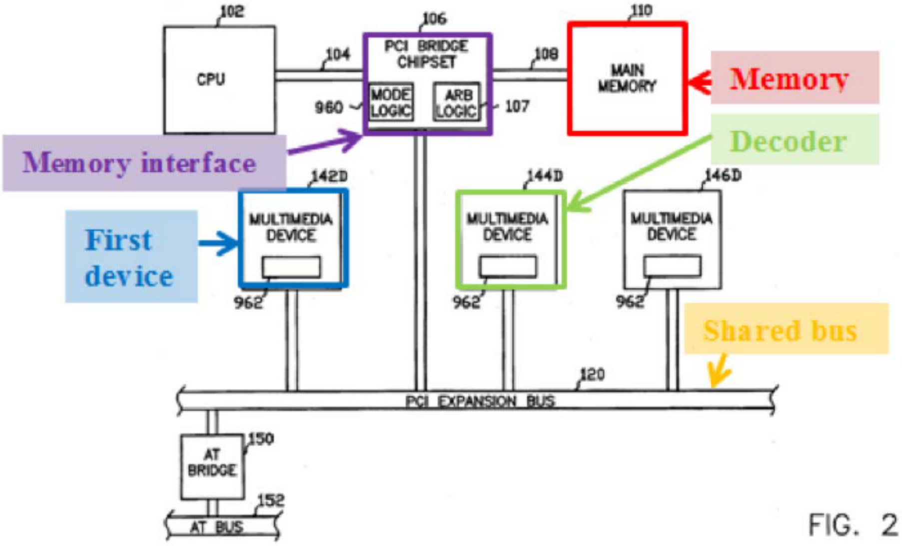
Claim Language	***Lambrecht***
	which are preferably identical to elements previously described include the same reference numerals for convenience." *Id.* at 26:48-63 (emphasis added). • "In one embodiment, the system bus (preferably PCI) implements a new mode of operation specifically *for real-time transfers***.** A signal (or signals) is used to indicate that the system bus should be placed in a special real time mode. When not in special real time mode, the system bus operates as usual. The *real time mode* is optimized for the transfer of high bandwidth real-time information. Therefore, the present invention comprises a novel computer system architecture and method which provides one or more real-time or multimedia buses, optionally with a local expansion bus, to increase the performance of *real-time peripherals and applications*. The multimedia bus of the present invention provides *improved data transfers performance and throughput for real-time devices*. The various embodiments discussed above may be combined in various ways for *optimum*

Claim Language	***Lambrecht***
	real-time and/or multimedia performance." *Id.* at 5:33-48 (emphasis added).

2. Claim 3

79. In my opinion, *Lambrecht* discloses every feature of claim 3.

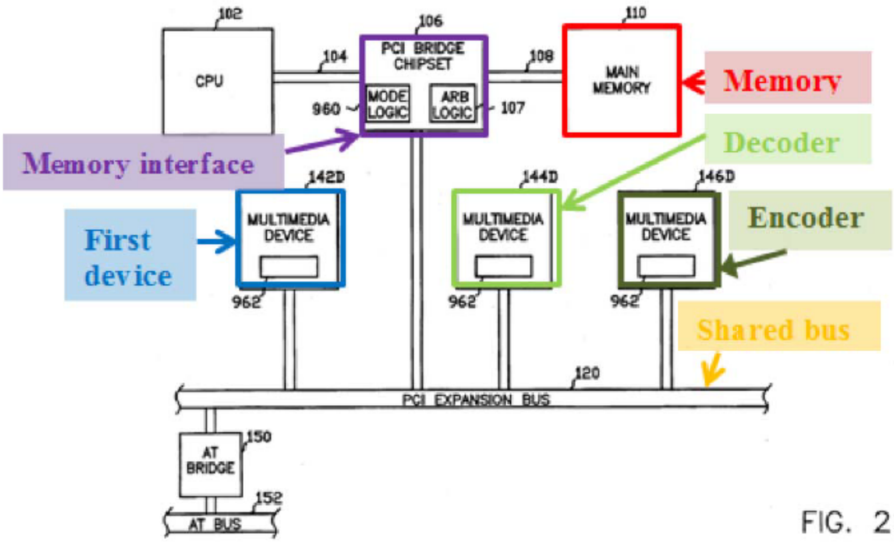
Claim Language	***Lambrecht***
[3.1] The electronic system of claim 1, wherein the decoder comprises a video decoder.	As discussed above, *Lambrecht* discloses all elements of claim 1. Further, *Lambrecht* teaches that the decoder is a video decoder. *See, e.g.,* Ex. 1032 at 27:51-53; *see also id.* at 27:43-56 ("The *multimedia devices 142D-146D* may be any of various types of input/output devices, including multimedia devices and communication devices, as described above. The *multimedia devices 142D-146D* are preferably similar to the multimedia devices 142-146 described above, except that the interface logic 962 in the multimedia devices 142D-146D each include the interface logic for interfacing to the PCI bus 120 in multiple modes. As described above, the *multimedia devices 142D-146D* may comprise video accelerator or graphics accelerator cards, video playback

Claim Language	***LAMBRECHT***
	cards, *MPEG decoder* cards, sound cards, network interface cards, SCSI adapters for interfacing to various input/output devices, such as CD-ROMS and tape drives, or other devices as desired.”), Fig. 21 (annotated below).  FIG. 21

3. Claim 5

80. In my opinion, *Lambrecht* discloses every feature of claim 5.

Claim Language	***LAMBRECHT***
[5.1] The electronic system of claim 1, further comprising an encoder coupled to the memory interface.	As discussed above, *Lambrecht* discloses all elements of claim 1. Further, *Lambrecht* teaches the inclusion of an encoder coupled to the memory interface. *See, e.g.,* Ex. 1032 at 2:66-3:7 ("In the preferred embodiment, the computer system comprises a CPU coupled through chip set or bridge logic to main memory. The bridge logic couples to a local bus such as the PCI bus. The computer system also includes a real-time expansion bus or multimedia bus for transferring real-time or multimedia data. A plurality of multimedia devices, such video devices, audio devices, *MPEG encoders* and/or decoders, and/or communications devices, are coupled to each of the PCI bus and the multimedia bus.") (emphasis added); *id*. at 8:13-17 ("For example, the multimedia devices 142-146 may comprise video accelerator or graphics accelerator devices, video playback devices, *MPEG encoder* or decoder devices . . .") (emphasis added); *id.* at Fig. 21 (annotated below).

Claim Language	***LAMBRECHT***
	 FIG. 21 At Fig. 21 (annotations added). *See also* Ex. 1032, 27:43-50 ("The *multimedia devices 142D-146D* may be any of various types of input/output devices, including multimedia devices and communication devices, as described above. The *multimedia devices 142D-146D* are preferably *similar to the multimedia devices 142-146 described above, except that the interface logic 962 in the multimedia devices 142D-146D each include the interface logic for interfacing to the PCI bus 120 in multiple modes*.") (emphasis added).

4. Claim 11

81. In my opinion, *Lambrecht* discloses every feature of claim 11.

Claim Language	***LAMBRECHT***
[11.1] The electronic system of claim 1, wherein the first device is a graphics accelerator.	As discussed above, *Lambrecht* discloses all elements of claim 1. *Lambrecht* also teaches that the first device can be a graphics accelerator. *See, e.g.,* Ex. 1032, 27:43-56 ("The *multimedia devices 142D-146D* may be any of various types of input/output devices, including multimedia devices and communication devices, as described above. The *multimedia devices 142D-146D* are preferably similar to the multimedia devices 142-146 described above, except that the interface logic 962 in the multimedia devices 142D-146D each include the interface logic for interfacing to the PCI bus 120 in multiple modes. As described above, the multimedia devices 142D-146D may comprise *video accelerator or graphics accelerator* cards, video playback cards, MPEG decoder cards, sound cards, network interface cards, SCSI adapters for interfacing to various input/output devices, such as CD-ROMS and tape drives, or other devices as desired.") (emphasis added).; *see also id.* at Fig.

Claim Language	*Lambrecht*
	21.

5. Claim 13

82. In my opinion, *Lambrecht* discloses every feature of claim 13.

Claim Language	*Lambrecht*
[13.1] The electronic system of claim 1, wherein the bus has a bandwidth of at least twice the bandwidth required for the decoder to operate in real time.	As discussed above, *Lambrecht* discloses all elements of claim 1. Furthermore, *Lambrecht* teaches that the bus has a bandwidth of at least twice the bandwidth required for the decoder to operate in real time. *Lambrecht* discloses that its bus, which is preferably a PCI bus, can service real time operation. *See, e.g.,* • Ex. 1032 at 27:66-28:2 ("In the preferred embodiment of the invention of FIG. 21, the multimedia mode comprises placing the system bus or *PCI bus 120* in a special mode optimized for *real-time data transfers*.") (emphasis added). • Ex. 1032 at 26:48-63 ("Referring now to FIG. 21, a

Claim Language	***LAMBRECHT***
	computer system is shown which includes an expansion bus, preferably a PCI bus 120, and which includes mode logic which selects between different modes of the PCI bus 120. The computer system of FIG. 21 is similar to the computer system of FIG. 1. However, the mode logic in the computer system of FIG. 21 is operable *to place the PCI bus 120* in either a normal PCI mode or *in a real-time/multimedia mode* optimized for multimedia transfers of periodic data. As described below, multimedia devices use the PCI bus 120 for normal PCI transfers and also use the PCI bus fines in the multimedia mode for high speed data multimedia transfers, preferably transfers of periodic multimedia data. In the following description, elements which are preferably identical to elements previously described include the same reference numerals for convenience.") (emphasis added).

Claim Language	***Lambrecht***
	Lambrecht adds: "In one embodiment, the system bus (preferably PCI) implements a new mode of operation specifically *for real-time transfers*. A signal (or signals) is used to indicate that the system bus should be placed in a special real time mode. When not in special real time mode, the system bus operates as usual. The *real time mode* is optimized for the transfer of high bandwidth real-time information. Therefore, the present invention comprises a novel computer system architecture and method which provides one or more real-time or multimedia buses, optionally with a local expansion bus, to increase the performance of *real-time peripherals and applications*. The multimedia bus of the present invention provides *improved data transfers performance and throughput for real-time devices*. The various embodiments discussed above may be combined in various ways for *optimum real-time and/or multimedia performance*." *Id.* at 5:42-59 (emphasis added).

Claim Language	***Lambrecht***
	Lambrecht discloses using a PCI bus as a real time bus in a "special mode optimized for real-time data transfers." *See, e.g.*, Ex. 1032 at 28:1-2. *Lambrecht* discloses that the PCI bus used is a 32 bit PCI bus and further discloses that only 16 bits of this PCI bus are needed to transfer video in real time. *See, e.g.*, Ex. 1032 at 27:66-28:8 ("In the preferred embodiment of the invention of FIG. 21, the multimedia mode comprises placing the system bus or PCI bus 120 in a *special mode optimized for real-time data transfers*. In one embodiment of FIG. 21, the special mode comprises a byte sliced mode which uses different byte lanes or channels of the PCI data lines for different types of multimedia transfers as described above. Thus, *16 bits of the PCI bus may be used for video transfers while the remaining 16 bits may be used for audio transfers simultaneously*."). Thus, by indicating that only 16 bits of the 32 bit PCI bus are needed to transfer data in real time, *Lambrecht* discloses a bus having a bandwidth of at least twice the bandwidth required for the

Claim Language	***Lambrecht***
	decoder to operate in real time.

B. Ground B: *Lambrecht* in view of *Artieri*, renders obvious, under 35 U.S.C. § 103, claim 4

1. Claim 4

83. In my opinion, *Lambrecht* and *Artieri* discloses every feature of claim 4.

Claim Language	***LAMBRECHT***
[4.1] The electronic system of claim 1, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.	As discussed above, *Lambrecht* discloses all elements of claim 1. *Lambrecht* also teaches that the decoder is an MPEG decoder. *See, e.g.,* Ex. 1032 at 27:51-53 ("the multimedia devices 142D-146D may comprise . . . MPEG decoder cards . . . ."). *Lambrecht* does not explicitly disclose that its MPEG decoder is capable of decoding a bitstream formatted to comply with the "MPEG-2" standard. However, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention to modify the decoder of *Lambrecht* to include the capability of decoding a bitstream formatted to comply with the MPEG-2 standard, in view of *Artieri*. *Artieri* discloses that its "invention relates to picture processing

Claim Language	***LAMBRECHT***
	systems and more particularly to a system for decoding pictures encoded in accordance with an MPEG standard." Ex. 1036, 1:6-9. *Artieri* explains that "[a]ll MPEG decoders, *especially for the MPEG-2 standard*, generally include a variable length decoder (VLD) 10, a run-level decoder (RLD) 11, an inverse quantizer circuit (Q-1) 12, an inverse discrete cosine transform circuit (DCT-1) 13, a half-pixel filter 14, and a memory 15. The encoded data are provided to the decoder via a bus CDin and the decoded data are output via a bus VIDout." *Id.* at 1:12-18. It would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the '789 patent to modify the MPEG decoder of *Lambrecht* to specifically decode a bitstream formatted to comply with the "MPEG-2" standard, like the decoder described in *Artieri*. Indeed, the '789 patent itself admits that at the time of the alleged invention of the '789 patent, the MPEG-2 standard was in use and well accepted. Ex. 1001 at 1:33-67. With the MPEG-2 standard already in use at the time of the alleged invention, its characteristics would have

Claim Language	***LAMBRECHT***
	been understood and predictable to those of ordinary skill. As alleged by the ’789 patent, the MPEG-2 standard is a “decompression protocol[] that describe[s] how an encoded bitstream is to be decoded.” Ex. 1001 at 41-45. Thus, modifying *Lambrecht*’s decoder to perform MPEG-2 video decoding, as disclosed in *Artieri*, would constitute a combination of familiar elements according to known methods to yield predictable results.

C. Ground C: *Lambrecht* in view of *Moore*, renders obvious, under 35 U.S.C. § 103, claim 6

1. Claim 6

84. In my opinion, *Lambrecht* and *Moore* discloses every feature of claim 6.

Claim Language	***LAMBRECHT***
[6.1] The electronic system of claim 5, wherein the decoder, the encoder and the memory interface are monolithically integrated into the first device.	As discussed above, *Lambrecht* discloses all of the elements of claim 5. *Lambrecht* does not explicitly disclose that the decoder, the encoder and the memory interface are *monolithically integrated into* the first device. However, it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention to monolithically integrate these components into a first device, in view of *Moore* (Ex. 1035). *Moore* discloses that even as far back as the 1960s, "[i]ntegrated electronics [was] established." Ex. 1035 at 2. *Moore* teaches the advantages of integration, namely "reduced cost" and that "the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate." Ex. 1035 at 2. Indeed, by the

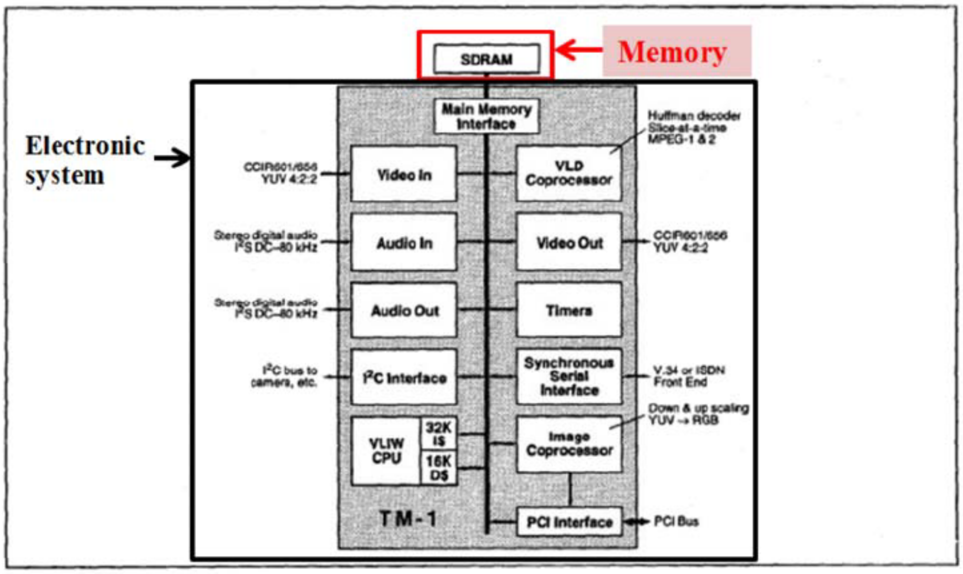
Claim Language	***Lambrecht***
	mid-1990s, the concept of integrating components on a single chip had been widely adopted and applied in the arena of multimedia processing chips, leading to faster multimedia processing chips. *See, e.g.*, Ex. 1006 (discussing the MVP, a video chip from Texas Instruments). Accordingly, a person of ordinary skill in the art at the time of the alleged invention would have been motivated to apply *Moore*'s teachings regarding integration to the system described in *Lambrecht*. Because chip integration was a well-known technique, its use with *Lambrecht* would have led to predictable results. Therefore, monolithically integrating the decoder, the encoder and the memory interface into the first device in *Lambrecht*, similar to the manner described in *Moore*, would have been nothing more than a combination of familiar elements that would have yielded predictable results.

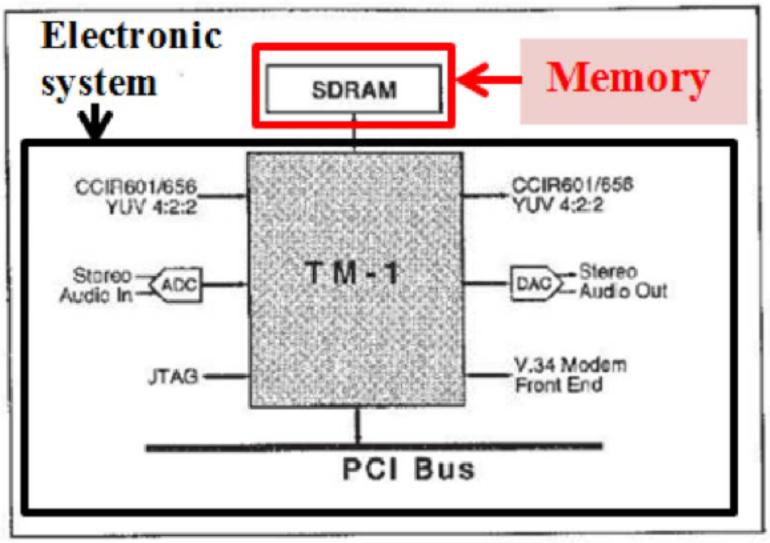
D. Ground D: Rathnam in view of *Lambrecht*, renders obvious, under 35 U.S.C. § 103, claims 1, 3, 4, 5, and 11

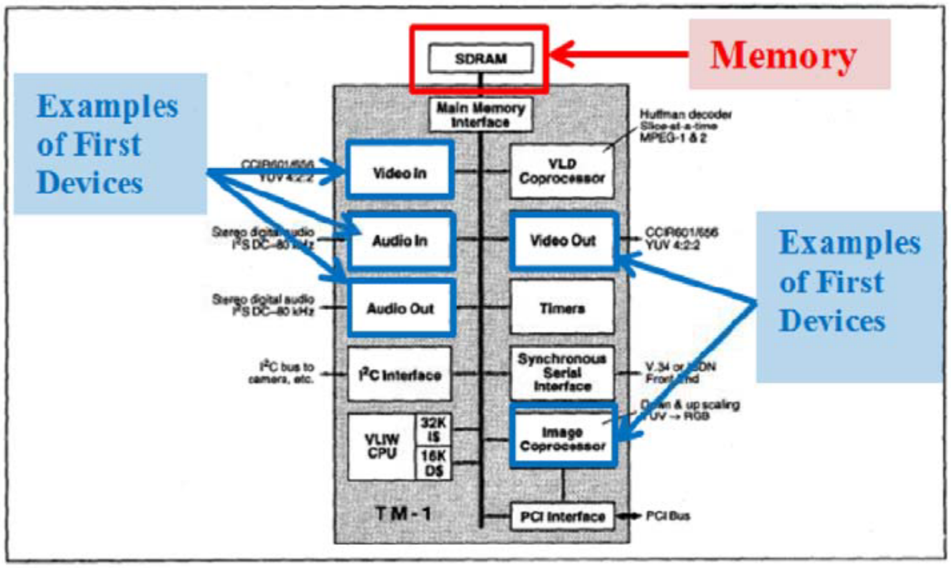
1. Claim 1

85. In my opinion, *Rathnam* and *Lambrecht* discloses every feature of claim 1.

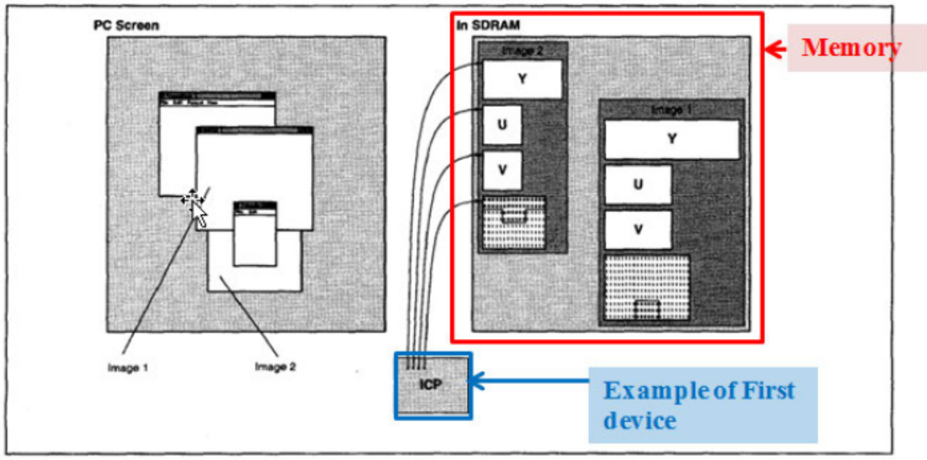
Claim Language	***RATHNAM***
[1.0] An electronic system coupled to a memory, comprising:	*Rathnam* discloses an electronic system coupled to a memory. *See, e.g.*, Ex. 1005, 12-14. For example, *Rathnam* describes the TM-1 which "is the first in a family of programmable multimedia processor from the Trimedia product group of Philips Semiconductors." *Id.*, 12. *Rathnam* explains that "the TM-1 microprocessor is a fluid computer system controlled by a small real-time OS kernel that runs on the VLIW processor core. TM-1 contains a CPU, a high bandwidth internal bus, and internal bus-mastering DMA peripherals." *Id.*, 12-13 (emphasis added). Moreover, *Rathnam* teaches a memory coupled to the electronic system. *See, e.g.,* Ex. 1005 at 13 ("Figure 1 shows a block diagram of the TM-1 chip. The bulk of a TM-1 system includes

Claim Language	***RATHNAM***
	the TM-1 microprocessor itself, a block of synchronous DRAM (SDRAM), and minimal external circuitry to interface to the incoming and/or outgoing multimedia data streams."); *see also id.* at Figs. 1-2 (annotated below).  **Figure 1. TM-1 block diagram.** *Rathnam* at Fig. 1 (annotations added).

Claim Language	***Rathnam***
	 **Figure 2. TM-1 system connections. A minimal TM-1 system requires few supporting components.** *Rathnam* at Fig. 2 (annotations added). The coupling to the shared main memory is then further disclosed. *See, e.g.*, *id*., 15 ("The internal data bus connects all internal blocks together and provides access to internal control registers (in each on-chip peripheral units), external SDRAM, and the external PCI bus.").
[1.1] a first device that requires access	*Rathnam* discloses several first devices that require access to the memory. *See, e.g.*, Ex. 1005, 15-17; Fig. 1-2. Examples of such a first device are the Image Coprocessor, Video-In, Video-Out,

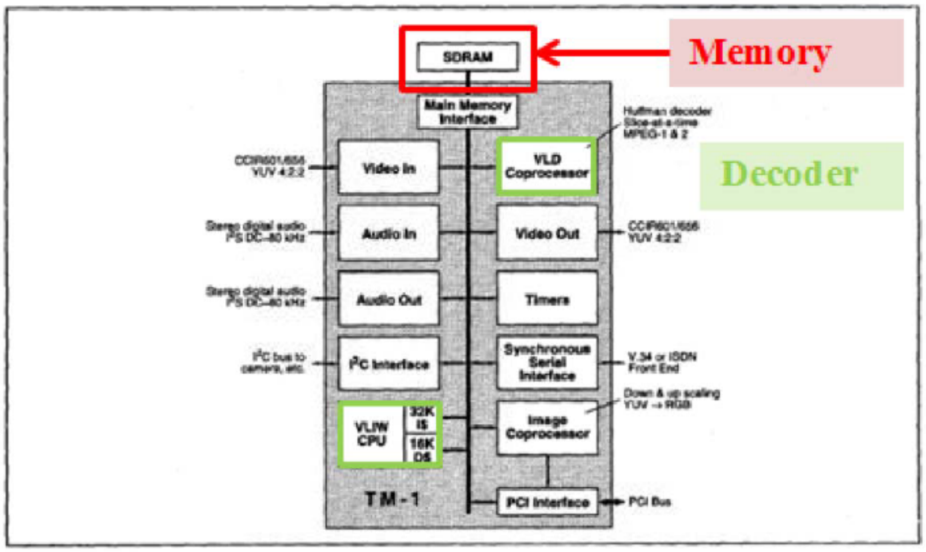
Claim Language	***Rathnam***
to the memory;	Audio-In, Audio-Out, etc., as shown in the annotated Fig. 1 of *Rathnam* below.  Figure 1. TM-1 block diagram. *Rathnam* at Fig. 1 (annotations added). These devices require access to the memory. For example, *Rathnam* discloses a Video-In unit that requires access to memory. *See, e.g.*, Ex. 1005, 15 ("The video-in unit demultiplexes the captured YUV data before writing it into *local TM-1 SDRAM*.") (emphasis added); *id*. ("The video-in unit can be programmed to perform on-the-fly horizontal resolution subsampling by a factor of two if needed.").

Claim Language	***Rathnam***
	Rathnam also discusses a Video-out unit that "essentially performs the inverse function of the video-in unit. Video-out generates an eight-bit, multiplexed YUV data stream by gathering bits from the separate Y, U, and V *data structures in SDRAM*." *See, e.g.*, Ex. 1005, 15 (emphasis added). Similarly, *Rathnam* also discloses Audio-In and Audio-Out units that require memory access. *See, e.g.*, Ex. 1005, 17 ("As with the video units, the audio-in and audio-out units buffer incoming and outgoing audio data *in SDRAM*.") (emphasis added); *id*. at 15 ("The audio-in and audio-out units are similar to the video units. They connect to most serial ADC and DAC chips, and are programmable enough to handle most reasonable protocols. These units can transfer MSB or LSB first and left or right channel first."). *Rathnam* discloses another example of a device that requires access to the memory, in particular, the TM-1's Image Coprocessor. *See, e.g.*, Ex. 1005, 15-16. One of the Image

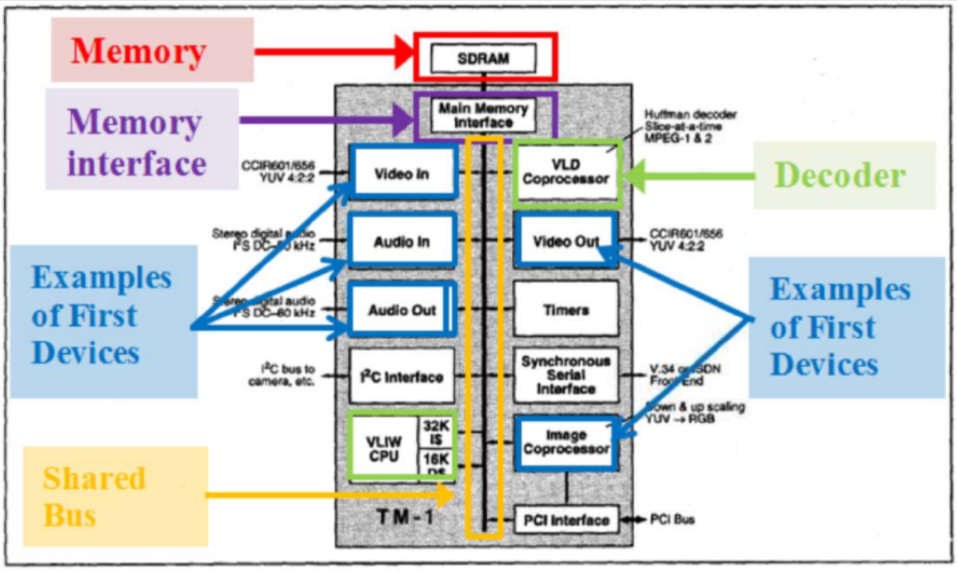
Claim Language	***RATHNAM***
	Coprocessor's purposes is "copying an image from SDRAM to the host's video frame buffer." *Id.* at 15. *Rathnam* adds that the Image Coprocessor "can operate as either a memory-to-memory or a memory-to-PCI coprocessor device." *Id.* at 16. Moreover, *Rathnam* teaches that the Image Coprocessor can maintain pointers in the memory. *See id.* ("When the ICP is displaying an image (i.e., copying it from SDRAM to a frame buffer), it maintains four pointers to the data structures in SDRAM."); *see also* Figure 4 of *Rathnam* (annotated below) is a visual representation of the Image Coprocessor's ability to access memory.  **Figure 4. ICP operation. Windows on the PC screen and data structures in SDRAM for two live video windows.** *Rathnam* at Fig. 4 (annotations added).

Claim Language	***Rathnam***
[1.2] a decoder that requires access to the memory sufficient to maintain real time operation; and	*Rathnam* teaches this element. *See, e.g.*, Ex. 1005, 14-15, Fig. 1 (annotated below). For example, *Rathnam* discloses a decoder comprised of the VLD coprocessor and the VLIW CPU, which can decode video data. *Rathnam*'s video decoding functionality whereby it receives encoded (*i.e.*, compressed) images and decodes (*i.e.*, decompresses) them is described: > The variable-length decoder (VLD) is included to relieve the TM-1 CPU of the task of *decoding Huffman-encoded video data streams*. It can be used to help *decode MPEG-1 and MPEG-2 video streams. The VLD is a memory-to-memory coprocessor*. The TM-1 CPU hands the VLD a pointer to a Huffman-encoded bit stream, and the VLD produces a tokenized bit stream that is very convenient for the TM-1 image decompression software to use. *See* Ex. 1005, 17 (emphasis added). > The TM-1 CPU fetches data from the compressed video stream via the PCI

Claim Language	***RATHNAM***
	bus, decompresses frames from the video stream, and places them into *local* SDRAM. Decompression may be aided by the VLD (variable-length decoder) unit, which implements Huffman decoding and is controlled by the TM-1 CPU. *Id.*, 14 (emphasis added). *See also* The CPU switches from one task to the next; first it *decompresses* a video frame, then it *decompresses* a slice of the audio stream, then back to video, etc. *Id.* at 14 (emphasis added). The TM-1 operation set includes all traditional microprocessor operations. In addition, multimedia-specific operations are included that dramatically accelerate standard

Claim Language	***RATHNAM***
	video compression and *decompression* algorithms. *Id.* at 15 (emphasis added). *Rathnam*'s decoder, which comprises the VLD coprocessor and VLIW CPU working in tandem, is coupled to memory, as shown below in Figure 1. *See also id.*, 15 ("The internal data bus connects all internal blocks together and provides access to internal control registers (in each on-chip peripheral units), external SDRAM, and the external PCI bus.").  **Figure 1. TM-1 block diagram.** *Rathnam* at Fig. 1 (annotations added).

Claim Language	***Rathnam***
	Rathnam discloses that its system is a real time system. *See, e.g.*, Ex. 1005, 15 ("The bus allocation mechanism is one of the features of TM-1 that makes it a true *real-time system* instead of just a highly integrated microprocessor with unusual peripherals.") (emphasis added); *id.*, 13 ("TM-1 enhances a PC system to provide *real-time multimedia*, and it does so with the advantages of a special purpose, embedded solution-low cost and chip count - and the advantages of a general-purpose processor-reprogrammability.").
[1.3] a memory interface for coupling to the memory, and coupled to the first device and to the decoder, the memory interface having	*Rathnam* in view of *Lambrecht* discloses this limitation. For example, *Rathnam* discloses "a memory interface for coupling to the memory." *See, e.g.*, Ex. 1005, 15 ("TM-1 has a glueless *interface with synchronous DRAM (SDRAM)*.") (emphasis added); Fig. 1 (annotated below).

Claim Language	***Rathnam***
an arbiter for selectively providing access for the first device and the decoder to the memory and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and	 **Figure 1. TM-1 block diagram.** *Rathnam* at 319 (annotations added). Furthermore, the memory interface is coupled to both the first device and the decoder via an internal bus. *See, e.g.,* Fig. 1 (annotated above). *Rathnam* explains that the "internal data bus connects all *internal blocks* together and provides access to internal control registers (in each on-chip peripheral units), *external SDRAM*, and the external PCI bus." Ex. 1005 at 15 (emphasis added). Therefore, the memory interface in *Rathnam* includes a "shared bus coupled to the memory the first device, and the decoder," as claimed.

Claim Language	***Rathnam***
operate in real time when the first device simultaneously accesses the bus.	*Rathnam* discloses an arbiter, explaining that: Access to the internal bus is controlled by a *central arbiter*, which has a request line from each potential bus master. The *arbiter* is configurable in a number of different modes so that the arbitration algorithm can be tailored for different applications. *Peripheral units make requests to the arbiter for access*, and depending on the arbitration mode, bus bandwidth is allocated to the units in different amounts. Each mode allocates bandwidth differently, but each mode guarantees each unit a minimum bandwidth and maximum service latency. All unused bandwidth is allocated to the TM-1 CPU. Ex. 1005 at 15 (emphasis added). *Rathnam* also suggests that the bus has "sufficient bandwidth to enable the decoder to access the memory and operate in real time." *See, e.g.,* Ex. 1005, *Rathnam* at 15 ("*The bus* allocation mechanism is one of the features of TM-1 that makes it a true *real-time system* instead of just a highly integrated

Claim Language	***Rathnam***
	microprocessor with unusual peripherals.") (emphasis added). *Rathnam* is capable of decoding multimedia in real-time. *See, e.g., id.* at 13 ("TM-1 enhances a PC system to provide real-time multimedia."). Thus, the TM-1 must have sufficient bandwidth to operate in real time. *Rathnam* discloses concurrent execution of multiple functions or operations as follows: • "TM-1 is designed to *concurrently process video, audio, graphics, and communication data*." Ex. 1005 at 12 (emphasis added). • "The VLIW-CPU core is capable of executing a maximum of twenty seven operations per cycle, and the sustained execution rate is about *five operations per cycle for the tuned applications*." Ex. 1005 at 12 (emphasis added). • "Further, users demand that their systems provide *live video and audio* without sacrificing the responsiveness of the system." Ex. 1005 at 13 (emphasis added). • "TM-1 is a low-cost, programmable processor for the

Claim Language	***Rathnam***
	consumer multimedia market. This product provides the additional processing power required for a true-to-life computer based experience. The Trimedia processor *concurrently processes multiple data types including audio, video, graphics and communications*." Ex. 1005 at 19 (emphasis added). Moreover, *Rathnam* is capable of delivering high bandwidth access to the memory. *See, e.g.*, Ex. 1005 at 15 ("TM-1's memory hierarchy satisfies the low cost and high bandwidth requirement of multimedia markets. Since multimedia video streams can require relatively large temporary storage, a significant amount of DRAM is required."). To the extent that *Rathnam* does not explicitly disclose "the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory" or "the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device

Claim Language	*RATHNAM*
	simultaneously accesses the bus," these elements would have been obvious to a person of ordinary skill in the art at the time of the alleged invention in view of *Lambrecht*. As discussed above, *Lambrecht* discloses a "computer system for real-time applications." *See* Ex. 1032, Abstract. In particular, as discussed in more detail above, *Lambrecht* discloses a memory interface that has an arbiter. *See, e.g.,* Ex. 1032 at 7:45-47 ("The chipset logic 106 preferably includes a memory controller for interfacing to the main memory 110 and also includes the arbitration logic 107."); *see also id.*, 7:30-44, 26:66-27:2 ("The chipset 106 [in Fig. 21] includes various bridge logic, peripheral logic and arbitration logic 107, as described above with reference to FIG. 1."). Furthermore, *Lambrecht* teaches a design that allows real-time operation of a bus while also simultaneously allowing access to two different devices. *See, e.g.*, Ex. 1032 at 5:18-48; 27:66-28:11. *Lambrecht* discloses a "byte sliced mode" that divides the

Claim Language	***Rathnam***
	bus into different byte lanes, which allows for two different simultaneous data transfers. *See* Ex. 1032 at 27:66-28:11; *see also id.* at 5:18-48. Byte slice mode allows for simultaneous, real-time video and audio transfers over the same PCI bus. *See id.* at 27:66-28:11. By using byte slice mode over the PCI bus disclosed in *Lambrecht*, the bus has sufficient bandwidth to allow real-time access to memory to both a first device (for example, an audio circuit) and the decoder. It would have been obvious to one of ordinary skill in the art at the time of the alleged invention to modify the TM-1 chip disclosed in *Rathnam* such that "the memory interface [has] an arbiter for selectively providing access for the first device and the decoder to the memory" and a "bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus ," similar to the manner disclosed in *Lambrecht*. *Rathnam* itself suggests both features, as discussed above, disclosing that its chip includes an arbiter and real-time operation. *See, e.g.*, Ex. 1005, 15.

Claim Language	***RATHNAM***
	One of ordinary skill would have been motivated to modify the TM-1 chip in this way (to the extent it does not already perform these features) because doing so would enable improved operation, allowing, e.g., two different simultaneous data transfers. *See* Ex. 1032 at 27:66-28:11; *see also id.* at 5:18-48. Moreover, one of ordinary skill would have recognized that the combination would have involved nothing more than a combination of familiar elements that would have yielded predictable results.

2. Claim 3

86. In my opinion, *Rathnam* and *Lambrecht* discloses every feature of claim 3.

Claim Language	*Rathnam*
[3.1] The electronic system of claim 1, wherein the decoder comprises a video decoder.	As discussed above, *Rathnam* in combination with *Lambrecht* discloses all elements of claim 1. Further, *Rathnam* discloses "the decoder comprises a video decoder." Ex. 1005, 14-15; 17. *Rathnam*'s video decoding functionality whereby it receives encoded (*i.e.*, compressed) images and decodes (*i.e.*, decompresses) them is described: The variable-length decoder (VLD) is included to relieve the TM-1 CPU of the task of *decoding Huffman-encoded video data streams*. It can be used to help *decode MPEG-1 and MPEG-2 video streams. The VLD is a memory-to-memory coprocessor*. The TM-1 CPU hands the VLD a pointer to a Huffman-encoded bit stream, and the VLD produces a tokenized bit stream that is very convenient for the TM-1 image decompression software to use.

	See Ex. 1005, 17 (emphasis added). The TM-1 CPU fetches data from the compressed video stream via the PCI bus, decompresses frames from the video stream, and places them into *local* SDRAM. Decompression may be aided by the VLD (variable-length decoder) unit, which implements Huffman decoding and is controlled by the TM-1 CPU. *Id.* at 14 (emphasis added). *See also* The CPU switches from one task to the next; first it *decompresses* a video frame, then it *decompresses* a slice of the audio stream, then back to video, etc. *Id.* at 14 (emphasis added). The TM-1 operation set includes all traditional microprocessor operations. In addition,

	multimedia-specific operations are included that dramatically accelerate standard *video* compression and *decompression* algorithms. *Id.* at 15 (emphasis added).

3. Claim 4

87. In my opinion, *Rathnam* and *Lambrecht* discloses every feature of claim 4.

Claim Language	***RATHNAM***
[4.1] The electronic system of claim 1, wherein the decoder is capable of decoding a bitstream	As discussed above, *Rathnam* in combination with *Lambrecht* discloses all elements of claim 1. Further, *Rathnam*'s decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard: The variable-length decoder (VLD) is included to relieve the TM-1 CPU of the task of decoding Huffman-encoded video data streams. It can be used to help *decode* MPEG-1 and *MPEG-2 video streams*. The VLD is a memory-to-memory coprocessor.

Claim Language	***RATHNAM***
formatted to comply with the MPEG-2 standard.	The TM-1 CPU hands the VLD a pointer to a Huffman-encoded bit stream, and the VLD produces a tokenized bit stream that is very convenient for the TM-1 image decompression software to use. *See, e.g.*, Ex. 1005, 17 (emphasis added). "TM-1 easily implements popular multimedia standards such as MPEG-1 and *MPEG-2*." *See, e.g.*, Ex. 1005, 12 (emphasis added).

4. Claim 5

88. In my opinion, *Rathnam* and *Lambrecht* discloses every feature of claim 5.

Claim Language	***RATHNAM***
[5.1] The electronic system of claim 1, further comprising an	As discussed above, *Rathnam* in combination with *Lambrecht* discloses all elements of claim 1. *Rathnam* discloses that the TM-1 also includes an encoder coupled to the memory interface. *See, e.g.*, Ex. 1005, *Rathnam*, 14-15; *id*. at 15 ("The TM-1 operation set includes all traditional microprocessor operations. In addition,

encoder coupled to the memory interface.	multimedia-specific operations are included that dramatically accelerate standard *video compression* and decompression algorithms.") (emphasis added); Fig. 1 (annotated below). A device that decompresses data is a decoder while a device that compresses data is an encoder. *See, e.g.*, Ex. 1001 at 1:46-51 ("Video and/or audio *compression devices (hereinafter encoders*) are used to encode the video and/or audio sequence before it is transmitted or stored. The resulting bitstream is decoded by a video and/or audio *decompression device (hereinafter decoder*) before the video and/or audio sequence is displayed.") (emphasis added). *Rathnam* teaches that the VLW CPU in the TM-1 is an encoder. *See, e.g.*, Ex. 1005, *Rathnam*, 14 ("When a complete video frame has been read from the camera chip by the video-in unit, it interrupts the TM-1 CPU. The CPU *compresses the video data* in software (using a set of powerful data-parallel operations) and *writes the compressed data to a separate area of SDRAM*") (emphasis added). The CPU writes the encoded data into the

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memory that is coupled to the CPU through the memory interface. *See, e.g.*, *id.* at 14, Fig. 1 (annotated below).

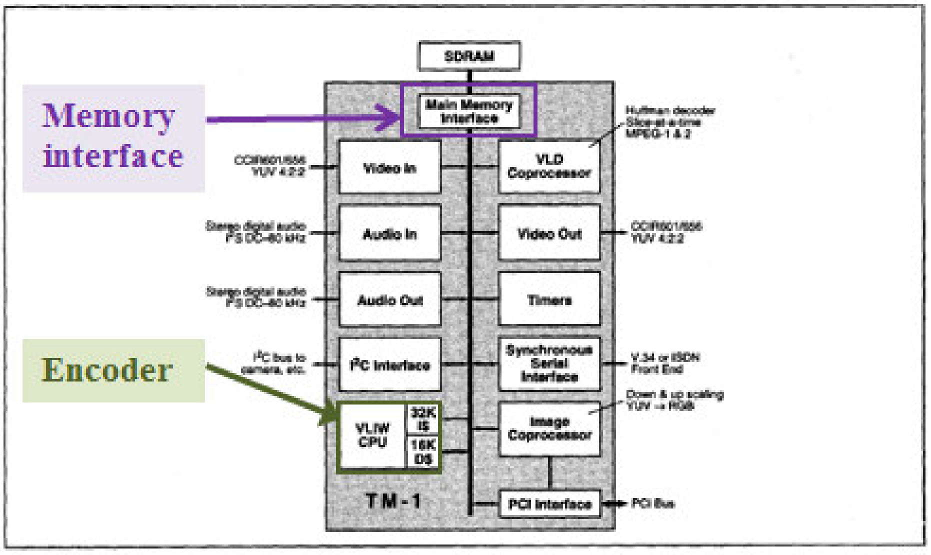

Figure 1. TM-1 block diagram.

Ex. 1005 at Fig. 1 (annotations added).
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5. Claim 11

89. In my opinion, *Rathnam* and *Lambrecht* discloses every feature of claim 11.

Claim Language	***RATHNAM***
[11.1] The electronic system of claim 1, wherein the first device is a graphics accelerator.	As discussed above, *Rathnam* in combination with *Lambrecht* discloses all elements of claim 1. Furthermore, *Rathnam* teaches that the first device can be a graphics accelerator. *See, e.g.*, Ex. 1005, 15 ("The TM-1 operation set includes all traditional microprocessor operations. In addition, multimedia-specific operations are included that dramatically *accelerate standard video compression and decompression algorithms*.") (emphasis added). As another example, *Rathnam* discloses an image coprocessor for enhancing the TM-1's graphical performance. *See id.* ("The image coprocessor (ICP) is used for several purposes to off-load tasks from the TM-1 CPU, such as copying an image from SDRAM to the host's video frame buffer. Although these tasks can be easily performed by the CPU, they *are a poor use of the*

Claim Language	***RATHNAM***
	relatively expensive CPU resource. When performed in parallel by the ICP, these tasks are *performed efficiently* by simple hardware, which allows the CPU to continue with more complex tasks.") (emphasis added). Moreover, *Rathnam* discloses that the image coprocessor can perform "horizontal resizing," "color-space conversion," accommodation of overlapping windows on a PC screen, generation of pixels, "modification of occulusion bitmaps," and "scaling." *See e.g.,* Ex. 1005 at 15-17, Fig. 4.

E. Ground E: *Rathnam* in view of *Lambrecht* and *Moore*, renders obvious, under 35 U.S.C. § 103, claim 6

1. Claim 6

90. In my opinion, *Rathnam* and *Lambrecht* and *Moore* discloses every feature of claim 6.

Claim Language	*RATHNAM*
[6.1] The electronic system of claim 5, wherein the decoder, the encoder and the memory interface are monolithically integrated into the first device.	As discussed above, *Rathnam* in combination with *Lambrecht* discloses all elements of claim 5. *Rathnam* further discloses that the decoder, the encoder and the memory interface are monolithically integrated into the TM-1 chip. *See, e.g.,* Ex. 1005 at 19 ("TM-1 is a *single chip* video teleconferencing solution that runs all current video codecs across all common transport mechanisms.") (emphasis added). To the extent *Rathnam* may not explicitly disclose integration of the encoder, decoder, and memory interface "into" the first device, it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention to monolithically integrate these components into a first device, in view of *Moore* (Ex. 1035).

Claim Language	*RATHNAM*
	Moore discloses that even as far back as the 1960s, "[i]ntegrated electronics [was] established." Ex. 1035 at 2. *Moore* teaches the advantages of integration, namely "reduced cost" and that "the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate." Ex. 1035 at 2. Indeed, by the mid-1990s, the concept of integrating components on a single chip had been widely adopted and applied in the arena of multimedia processing chips, leading to faster multimedia processing chips. *See, e.g.*, Ex. 1006 (discussing the MVP, a video chip from Texas Instruments). Accordingly, a person of ordinary skill in the art at the time of the alleged invention would have been motivated to apply *Moore*'s teachings regarding single-chip integration to the system described in *Lambrecht*. Because chip integration was a well-known technique, its use with *Lambrecht* would have led

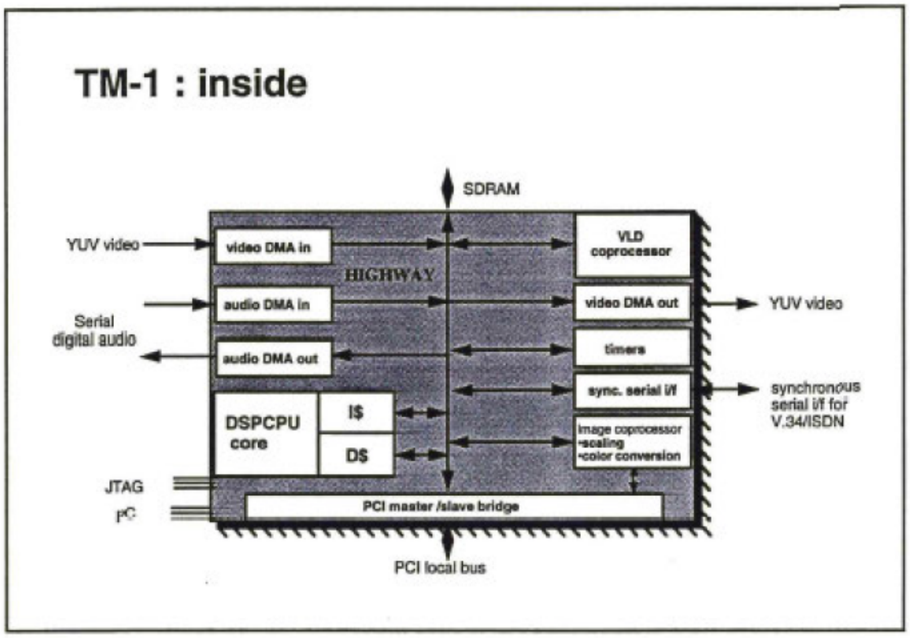
Claim Language	***RATHNAM***
	to predictable results. Therefore, monolithically integrating the decoder, the encoder and the memory interface into the first device in *Lambrecht*, similar to the manner described in *Moore*, would have been nothing more than a combination of familiar elements that would have yielded predictable results.

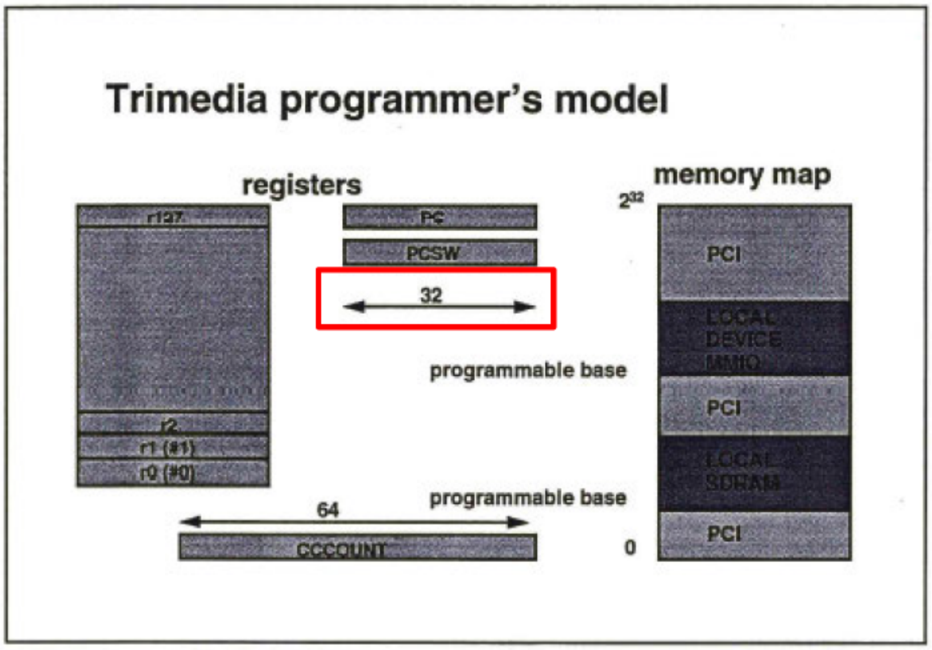
F. Ground F: *Rathnam* in view of *Lambrecht* and *Slavenburg*, renders obvious, under 35 U.S.C. § 103, claim 13

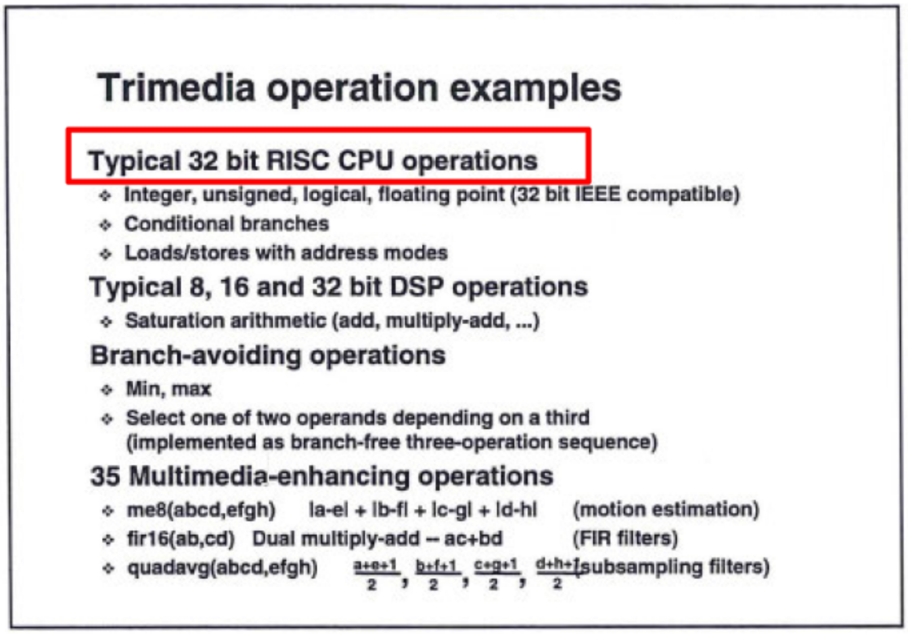
1. Claim 13

91. In my opinion, *Rathnam* in view of *Lambrecht* and *Slavenburg* discloses every feature of claim 13.

Claim Language	*RATHNAM*
[13.1] The electronic system of claim 1, wherein the bus has a bandwidth of at least twice the bandwidth required for the decoder to operate in real time.	As discussed above, *Rathnam* in combination with *Lambrecht* discloses all elements of claim 1. Further, *Rathnam* discloses that the TM-1 is capable of delivering high bandwidth access to the memory. *See, e.g.*, Ex. 1005, *Rathnam* at 15 ("TM-1's memory hierarchy satisfies the low cost and high bandwidth requirement of multimedia markets. Since multimedia video streams can require relatively large temporary storage, a significant amount of DRAM is required."). Furthermore, the bus in *Rathnam* operates in real-time. *See, e.g., id.* ("The bus allocation mechanism is one of the features of TM-1 that makes it a true real-time system instead of just a highly integrated microprocessor with unusual peripherals."). The *Slavenburg* publication, authored by one of the co-authors

Claim Language	***Rathnam***
	of *Rathnam* discloses that the TM-1 memory bus is capable of having a bandwidth at least two times greater than the amount of data carried to the decoder when the decoder decodes in real time. For example, *Slavenburg* discloses that the TM-1 has 400Mbyte/Sec bandwidth. *See id.* More particularly, *Slavenburg* discloses that the TM-1 was capable of accessing the SDRAM at 100 MHz. *See, e.g.*, Ex. 1034 at 12-9 ("100 MHz SDRAM interface, under worst-case conditions"). Moreover, *Slavenburg* discloses that the TM-1 accesses the SDRAM via the internal bus. *See, e.g.*, *id.* at 12-2. 

Claim Language	*RATHNAM*
	Slavenburg at 12-2 *Slavenburg* and *Rathnam* each demonstrate that the TM-1 uses a 32 bit architecture, including memory and bus. "The internal bus consists of separate 32-bit data and address buses." *See, e.g.*, Ex. 1005, *Rathnam* at 15.  Ex. 1034, *Slavenburg* at 12-6 (emphasis added).

Claim Language	***Rathnam***
	 **Trimedia operation examples** **Typical 32 bit RISC CPU operations** - Integer, unsigned, logical, floating point (32 bit IEEE compatible) - Conditional branches - Loads/stores with address modes **Typical 8, 16 and 32 bit DSP operations** - Saturation arithmetic (add, multiply-add, ...) **Branch-avoiding operations** - Min, max - Select one of two operands depending on a third (implemented as branch-free three-operation sequence) **35 Multimedia-enhancing operations** - me8(abcd,efgh) |a-e| + |b-f| + |c-g| + |d-h| (motion estimation) - fir16(ab,cd) Dual multiply-add -- ac+bd (FIR filters) - quadavg(abcd,efgh) $\frac{a+e+1}{2}, \frac{b+f+1}{2}, \frac{c+g+1}{2}, \frac{d+h+1}{2}$ (subsampling filters) Ex. 1034, *Slavenburg* at 12-7 (emphasis added). The combination of a 32 bit bus operating at over 100MHz creates a bus with a bandwidth of over 400 Mbytes/Sec. This follows from the fact that 32 bits correspond to 4 Bytes because 1 Byte consists of 8 bits. And 4 Bytes multiplied times 100 MHz corresponds to 400 Mbytes/sec. The TM-1 decodes MPEG 2 at 15Mbit/sec, which is well below half of 400 Mbytes/sec. *See Slavenburg* at 12-8 ("application performance: MPEG-2 main level, main profile, 15Mbit/sec")

Claim Language	***Rathnam***
	400 Mbytes/sec is well over twice the bandwidth required to operate the TM-1 in real time. The ’789 patent itself admits that 400 Mbytes/Sec is “at least twice the bandwidth required for an optimized decoder/encoder 45, allowing the decoder/encoder 45 to operate in real time.” *See* Ex. 1001 at 8:56-62 (“In current technology the memory bus 167, which corresponds to the fast bus 70, for coupling a core logic chipset to a memory, is capable of having a bandwidth of approximately *400 Mbytes/s*. This bandwidth is *at least twice the bandwidth* required for an optimized decoder/encoder 45, allowing the decoder/encoder 45 to *operate in real time*.”). Thus, the TM-1’s bus can operate with at least twice the bandwidth required to operate in real time. It would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the ’789 patent to modify the TM-1 chip disclosed in *Rathnam* to include the features disclosed regarding the TM-1 chip in *Slavenburg*. One of

Claim Language	***RATHNAM***
	ordinary skill would have recognized that, since both publications discuss the same chip, any modification of the TM-1 chip described in *Rathnam* would have yielded predictable results. Moreover, one of ordinary skill would have been motivated to apply the teachings of *Slavenburg* to the TM-1 chip described in *Rathnam* because both publications describe the same chip. Therefore, modifying the bus described in *Rathnam* to include a bandwidth of at least twice the bandwidth required for the decoder to operate in real time would have been nothing more than a predictable and common sense implementation based on the disclosures of *Rathnam* and *Slavenburg*.

* * *

I, Harold S. Stone, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: September 21, 2015

Harold S Stone

Harold S. Stone

VII. APPENDIX A

Exhibit	Title
1001	U.S. Patent No. 5,812,789
1002	File History for U.S. Patent No. 5,812,789
1004	ISO/IEC 11172-2:1993: Information technology—Coding of moving pictures and associated audio for digital storage media at up to about 1,5 Mbit/s—Part 2: Video," (1st ed. August 1, 1993) ("*MPEG Standard*")
1005	S. Rathnam et al., "An Architectural Overview of the Programmable Multimedia Processor, TM-1," IEEE Proceedings of COMPCON '96, pp. 319-326 (1996) ("*Rathnam*")
1006	R.J. Gove, "The MVP: A Highly-Integrated Video Compression Chip," Proceedings of the IEEE Data Compression Conference (DCC '94), pp. 215-224 (March 29-31, 1994) ("*Gove*")
1007	U.S. Patent No. 5,774,676 ("*Stearns*")
1014	Brad Hansen, The Dictionary of Multimedia, 1997
1019	Shanley, et al., "PCI System Architecture," Addison-Wesley Publishing Company, 1995 (3rd ed.) ("*Shanley*")
1020	Stone, H., "Microcomputer Interfacing," Addison-Wesley Publishing Company, 1982
1023	U.S. Patent No. 5,797,028 ("*Gulick 028*")
1024	"Accelerated Graphics Port Interface Specification," Intel Corporation, July 31, 1996 (Revision 1.0) ("*AGP*")
1025	VESA Unified Memory Architecture Hardware Specifications Proposal," Version 1.0p ("*VUMA*")
1032	U.S. Patent No. 5,682,484 ("*Lambrecht*")
1034	Slavenburg, G., "The TriMedia VLIW-Based PCI Multimedia Processor," Microprocessor Forum 1995, Oct. 10-11, 1995 ("*Slavenburg*")
1035	G. Moore, "Cramming more components onto integrated circuits," Electronics, Vol. 38, No. 8, Apr. 19, 1965 ("*Moore*")
1036	U.S. Patent No. 5,579,052 ("*Artieri*")