

Accelerated Graphics Port Interface Specification

Revision 1.0

Intel Corporation

July 31, 1996

Intel may have patents and/or patent applications related to the various Accelerated Graphics Port (AGP or A.G.P.) interfaces described in the *Accelerated Graphics Port Interface Specification*. A reciprocal, royalty-free license to the electrical interfaces and bus protocols described in, and required by, the *Accelerated Graphics Port Interface Specification Revision 1.0* is available from Intel.

Accelerated Graphics Port Interface Specification

Copyright © Intel Corporation 1996

All rights reserved.

THIS SPECIFICATION IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION , OR SAMPLE. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED OR INTENDED HEREBY.

INTEL DISCLAIMS ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OF INFORMATION IN THIS SPECIFICATION. INTEL DOES NOT WARRANT OR REPRESENT THAT SUCH USE WILL NOT INFRINGE SUCH RIGHTS.

*THIRD-PARTY BRANDS AND NAMES ARE THE PROPERTY OF THEIR RESPECTIVE OWNERS.

Table of Contents

1. INTRODUCTION.....	1
1.1 MOTIVATION	1
1.2 RELATIONSHIP TO PCI	1
2. ARCHITECTURAL CONTEXT AND SCOPE.....	3
2.1 TWO USAGE MODELS: “EXECUTE” & “DMA”	3
2.2 A.G.P. QUEUING MODELS	4
2.3 PERFORMANCE CONSIDERATIONS.....	6
2.4 PLATFORM DEPENDENCIES	6
3. SIGNALS AND PROTOCOL SPECIFICATION.....	9
3.1 A.G.P. OPERATION OVERVIEW	9
3.1.1 Pipeline Operation.....	9
3.1.2 Addressing Modes and Bus Operations	11
3.1.3 Address Demultiplexing Option.....	13
3.2 ACCESS ORDERING RULES & FLOW CONTROL.....	16
3.2.1 Ordering Rules and Implications	16
3.2.2 Deadlock Avoidance	19
3.2.3 Flush and Fence Commands.....	19
3.2.4 Access Request Priority.....	20
3.2.5 Flow Control	21
3.2.5.1 Introduction.....	21
3.2.5.2 Read Flow Control	22
3.2.5.3 Write Data Flow Control	25
3.2.5.4 1 and 2 Clock Rule for IRDY# and TRDY#	27
3.2.5.5 Other Flow Control Rules.....	27
3.2.6 Source Throttling Address Flow Control.....	27
3.3 PIN DESCRIPTION	28
3.4 A.G.P. SEMANTICS OF PCI SIGNALS.....	31
3.5 BUS TRANSACTIONS.....	33
3.5.1 Address Transactions	33
3.5.1.1 AD Bus	33
3.5.1.2 SBA Port.....	35
3.5.2 Basic Data Transactions	36

3.5.2.1 1x Data Transfers.....	37
3.5.2.2 2x Data Transfers.....	39
3.5.3 Flow Control	42
3.5.3.1 Initial Data Block.....	42
3.5.3.2 Subsequent Data Block	44
3.6 ARBITRATION SIGNALING RULES	51
3.6.1 Introduction.....	51
3.6.2 A.G.P. Compliant Master's REQ#	52
3.6.3 GNT# and ST[2::0]	53
3.6.4 GNT# for Single Transactions	53
3.6.5 GNT# Pipelining	54
3.6.6 GNT# Interaction with RBF#	61
3.7 A.G.P. SEQUENCER STATE MACHINE EQUATIONS	61
3.7.1 Error Reporting.....	62
4. ELECTRICAL SPECIFICATION.....	63
4.1 OVERVIEW.....	63
4.1.1 Introduction.....	63
4.1.2 1X Transfer Mode Operation.....	63
4.1.3 2X Transfer Mode Operation.....	63
4.1.3.1 Transmit/Receive Outer Loop.....	65
4.1.3.2 Transmit to Receive Inner loop.....	65
4.1.3.3 Transmit Outer to Inner Loop.....	66
4.1.3.4 Receive Inner to Outer Loop.....	66
4.1.3.5 SB_STB Synchronization.....	68
4.2 COMPONENT SPECIFICATION.....	69
4.2.1 DC SPECIFICATIONS.....	69
4.2.1.1 A.G.P. 1X Mode DC Specification.....	70
4.2.1.2 A.G.P. 2X Mode DC Specification.....	70
4.2.2 AC Timings.....	71
4.2.2.1 A.G.P. 1X Timing Parameters	72
4.2.2.2 A.G.P. 2X AC Timing Parameters	73

4.2.2.3 Measurement and Test Conditions	76
4.2.3 Signal Integrity Requirement.....	78
4.2.4 Driver Characteristics	78
4.2.5 Receiver Characteristics.....	79
4.2.6 Maximum AC Ratings and Device Protection.....	80
4.2.7 Component Pinout Recommendations	81
4.3 MOTHERBOARD SPECIFICATION.....	82
4.3.1 System Timing Budget	82
4.3.2 Clock Skew.....	83
4.3.3 Reset.....	84
4.3.4 Interconnect Delay	85
4.3.5 Physical Requirements.....	85
4.3.5.1 Interface Signaling	85
4.3.5.2 Pullups	85
4.3.5.3 Signal Routing and Layout	86
4.3.5.4 Impedances	86
4.3.5.5 Vref Generation	86
4.3.5.6 Crosstalk Consideration.....	86
4.3.5.7 Line Termination.....	87
4.4 ADD-IN CARD SPECIFICATION	87
4.4.1 Clock Skew.....	87
4.4.2 Interconnect Delay	87
4.4.3 Physical Requirements.....	88
4.4.3.1 Pin Assignment	88
4.4.3.2 Signal Routing and Layout	88
4.4.3.3 Impedances	88
4.4.3.4 Vref Generation	88
4.4.3.5 Power supply delivery.....	88
5. MECHANICAL SPECIFICATION.....	89
5.1 INTRODUCTION	89
5.2 EXPANSION CARD PHYSICAL DIMENSIONS AND TOLERANCES	89

Explore Litigation Insights



Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.