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APPLICATION NUMBER: *10/459,797*
FILING DATE: *June 12, 2003*
PATENT NUMBER: *8,933,945*
ISSUE DATE: *January 13, 2015*

By Authority of the
Under Secretary of Commerce for Intellectual Property
and Director of the United States Patent and Trademark Office

P. SWAIN
Certifying Officer


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17611 U.S. PTO 06/12/03

PTO/SB/05 (05-03)
Approved for use through 04/30/2003. OMB 0651-0032
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	00100.02.0053
First Inventor	Mark M. Leather
Title	Dividing Work Among Multiple Graphics Pipelines Using a Super-Tiling Technique
Express Mail Label No.	EV 063310627 US

15447 U.S. PTO 10/459797 06/12/03

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria VA 22313-1450**

1. ☑ Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. ☐ Applicant claims small entity status. See 37 CFR 1.27.
3. ☑ Specification [*Total Pages* 21] *(preferred arrangement set forth below)*
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☑ Drawing(s) (*35 U.S.C. 113*) [*Total Sheets* 5]
5. Oath or Declaration [*Total Sheets* 2]
   a. ☑ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 18 completed)*
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Reader Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☑ Assignment Papers (cover sheet & document(s))
10. ☐ 37 CFR 3.73(b) Statement ☑ Power of Attorney *(when there is an assignee)*
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement (IDS)/PTO-1499 ☐ Copies of IDS Citations
13. ☑ Preliminary Amendment
14. ☑ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☐ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. ☐ Other: .....

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: .....

Prior application information: *Examiner* _____ *Art Unit:* _____

For CONTINUATION OF DIVISIONAL APPS only; The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

☐ *Customer Number or Bar Code Label* (*Insert Customer No. or Attach bar code label here*) OR ☑ *Correspondence address below*

Name	Christopher J. Reckamp				
Address	Vedder, Price, Kaufman & Kammholz 222 North LaSalle Street				
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Name (Print/Type)	Christopher J. Reckamp	*Registration No. (Attorney/Agent)*	34,414
Signature	C. J. Reckamp	*Date*	06/12/03

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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06/12/03 17611 U.S. PTO

PTO/SB/17 (01-03)
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FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 862.00

Complete if Known	
Application Number	
Filing Date	6/12/03
First Named Inventor	Mark M. Leather
Examiner Name	
Art Unit	
Attorney Docket No.	00100.02.0053

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 50-0441

Deposit Account Name: ATI Technologies Inc.

The Commissioner is authorized to: *(check all that apply)*

☑ Charge fee(s) indicated below ☑ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	750.00
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 750.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below	Fee Paid
Total Claims	24	-20** = 4	x	18	= 72.00
Independent Claims	3	- 3** = 0	x	0	= 0.00
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 72.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	40.00
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40.00

SUBMITTED BY				(Complete *if applicable*)	
Name (Print/Type)	Christopher J. Reckamp	*Registration No. (Attorney/Agent)*	34,414	*Telephone*	312-609-7598
Signature	Christopher J. Reckamp			*Date*	6/12/03

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[redacted]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Leather et al. Examiner:

Serial No.: Art Group:

Filing Date: June 12, 2003 Docket No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Patent Application
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Express Mail No. EV 063310627 US.

06/12/03 Winona K. Jackson
Date *Winona K. Jackson*

PRELIMINARY AMENDMENT

Dear Sir:

Prior to examination, Applicants respectfully request that the above-identified application be amended as follows:

In The Specification:

Please add the following new paragraph directly below the invention title on page 1 of the specification as follows:

This application claims the benefit of U. S. Provisional Application Ser. No. 60/429,641 filed November 27, 2002, entitled "Dividing Work Among Multiple Graphics Pipelines Using a Super-Tiling Technique", having as inventors Mark M. Leather and Eric Demers, and owned by instant assignee.

REMARKS

Applicants submit that the specification is fully supported by the original provisional application, and the claims are fully supported by the criginally filed provisional application.

Respectfully submitted,

By: _____
Christopher J. Reckamp
Reg. No. 34,414

Dated: June 12, 2003

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Chicago, Illinois 60601
Telephone: (312) 609-7500
Facsimile: (312) 609-5005

[redacted]

020053

PATENT APPLICATION
ATTY. DOCKET NO. 00100.02.0053

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FILING OF A UNITED STATES PATENT APPLICATION

DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

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Date of Deposit: June 12, 2003

I hereby certify that this paper is being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. Section 1.10 on the 'Date of Deposit', indicated above, and is addressed to: Mail Stop Patent Application, Commissioner of Patents, P. O. Box 1450, Alexandria, VA, 22313-1450.

Name of Depositor: Winona K. Jackson

Signature: Winona K. Jackson

[redacted]

DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

RELATED CO-PENDING APPLICATION

[0001] This is a related application to a co-pending application entitled "Parallel Pipeline Graphics System" having docket number 010025, having serial number _____, having Leather et al. as the inventors, filed on even date, owned by the same assignee and hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0001] The present invention generally relates to graphics processing circuitry and, more particularly, to dividing graphics processing operations among multiple pipelines.

BACKGROUND OF THE INVENTION

[0002] Computer graphics systems, set top box systems or other graphics processing systems typically include a host processor, graphics (including video) processing circuitry, memory (e.g. frame buffer), and one or more display devices. The host processor may have a graphics application running thereon, which provides vertex data for a primitive (e.g. triangle) to be rendered on the one or more display devices to the graphics processing circuitry. The display device, for example, a CRT display includes a plurality of scan lines comprised of a series of pixels. When appearance attributes (e.g. color, brightness, texture) are applied to the pixels, an object or scene is presented on the display device. The graphics processing circuitry receives the vertex data and generates pixel data including the appearance attributes which may be presented on the display device according to a particular protocol. The pixel data is typically stored in the frame buffer in a manner that corresponds to the pixels location on the display device.

[0003] FIG. 1 illustrates a conventional display device 10, having a screen 12 partitioned into a series of vertical strips 13-18. The strips 13-18 are typically 1-4 pixels in width. In like manner, the frame buffer of conventional graphics processing systems is partitioned into a series of vertical strips having the same screen space width.

[redacted]

Alternatively, the frame buffer and the display device may be partitioned into a series of horizontal strips. Graphics calculations, for example, lighting, color, texture and user viewing information are performed by the graphics processing circuitry on each of the primitives provided by the host. Once all calculations have been performed on the primitives, the pixel data representing the object to be displayed is written into the frame buffer. Once the graphics calculations have been repeated for all primitives associated with a specific frame, the data stored in the frame buffer is rendered to create a video signal that is provided to the display device.

[0004] The amount of time taken for an entire frame of information to be calculated and provided to the frame buffer becomes a bottleneck in graphics systems as the calculations associated with the graphics become more complicated. Contributing to the increased complexity of the graphics calculation is the increased need for higher resolution video, as well as the need for more complicated video, such as 3-D video. The video image observed by the human eye becomes distorted or choppy when the amount of time taken to render an entire frame of video exceeds the amount of time in which the display device must be refreshed with a new graphic or frame in order to avoid perception by the human eye. To decrease processing time, graphics processing systems typically divide primitive processing among several graphics processing circuits where, for example, one graphics processing circuit is responsible for one vertical strip (e.g. 13) of the frame while another graphics processing circuit is responsible for another vertical strip (e.g. 14) of the frame. In this manner, the pixel data is provided to the frame buffer within the required refresh time.

[0005] Load balancing is a significant drawback associated with the partitioning systems as described above. Load balancing problems occur, for example, when all of the primitives 20-23 of a particular object or scene are located in one strip (e.g. strip 13) as illustrated in FIG. 1. When this occurs, only the graphics processing circuit responsible strip 13 is actively processing primitives; the remaining graphics processing circuits are idle. This results in a significant waste of computing resources as at most only half of the graphics processing circuits are operating. Consequently, graphics processing system performance is decreased as the system is only operating at a maximum of fifty percent capacity.

[redacted]

[0006] Changing the width of the strips has been employed to counter the system performance problems. However, when the width of a strip is increased, the load balancing problem is enhanced as more primitives are located within a single strip; thereby, increasing the processing required of the graphics processing circuit responsible for that strip, while the remaining graphics processing circuits remain idle. When the width of the strip is decreased (e.g. four bits to two bits), cache (e.g. texture cache) efficiency is decreased as the number of cache lines employed in transferring data is reduced in proportion to the decreased width of the strip. In either case, graphics processing system performance is still decreased due to the idle graphics processing circuits.

[0007] Frame based subdivision has been used to overcome the performance problems associated with conventional partitioning systems. In frame based subdivision, each graphics processor is responsible for processing an entire frame, not strips within the same frame. The graphics processors then alternate frames. However, frame subdivision introduces one or more frames of latency between the user and the screen, which is unacceptable in real-time interactive environments, for example, providing graphics for a flight simulator application.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The present invention and the related advantages and benefits provided thereby, will be best appreciated and understood upon review of the following detailed description of a preferred embodiment, taken in conjunction with the following drawings, where like numerals represent like elements, in which:

[0009] FIG. 1 is a schematic block diagram of a conventional display partitioned into several vertical strips:

[0010] FIG. 2 is a schematic block diagram of a graphics processing system employing an exemplary multi-pipeline graphics processing circuit according to one embodiment of the present invention;

[0011] FIG. 3 is a schematic block diagram of a memory partitioned into an exemplary super-tile pattern according to the present invention;

[redacted]

[0012] FIG. 4 is a schematic block diagram of a memory partitioned into a super-tile pattern according to an alternate embodiment of the present invention;

[0013] FIG. 5 is a schematic block diagram of an exemplary multi-pipeline graphics processing circuit used in a multi processor configuration according to an alternate embodiment of the present invention;

[0014] FIG. 6 is a flow chart of the operations performed by the graphics processing circuit according to the present invention;

[0015] FIG. 7 is a diagram illustrating a polygon bounding box to determine which, if a polygon fits in a tile or super tile; and

[0016] FIG. 8 is a schematic block diagram of an exemplary multi-pipeline graphics processing circuit used in a multi processor configuration according to an alternate embodiment of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

[0017] A multi-pipeline graphics processing circuit includes at least two pipelines operative to process data in a corresponding tile of a repeating tile pattern, a respective one of the at least two pipelines is operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. The multi-pipeline graphics processing circuit may be coupled to a frame buffer that is subdivided into a replicating pattern of square regions (e.g. tiles), where each region is processed by a corresponding one of the at least two pipelines such that load balancing and texture cache utilization is enhanced.

[0018] A multi-pipeline graphics processing method includes receiving vertex data for a primitive to be rendered, generating pixel data in response to the vertex data, determining the pixels within a set of tiles of a repeating tile pattern to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines. An exemplary embodiment of the present invention will now be described with reference to Figures 2-6.

[0019] FIG. 2 is a schematic block diagram of an exemplary graphics processing system 30 employing an example of a multi-pipeline graphics processing circuit 34 according to one embodiment of the present invention. The graphics processing system 30 can be implemented with a single graphics processing circuit 34 or with two or more graphics processing circuits 34, 54. The components and corresponding functionality of the graphics processing circuits 34, 54 are substantially the same. Therefore, only the structure and operation of graphics processing circuit 34 will be described in detail. An alternate embodiment, employing both graphics processing circuits 34 and 54 will be discussed in greater detail below with reference to FIGS. 4-5.

[0020] Graphics data 31, for example, vertex data of a primitive (e.g. triangle) 80 (FIG. 3) is transmitted as a series of strips to the graphics processing circuit 34. As used herein, graphics data 31 can also include video data or a combination of video data and graphics data. The graphics processing circuit 34 is preferably a portion of a stand-alone graphics processor chip or may also be integrated with a host processor or other circuit, if

desired, or part of a larger system. The graphics data 31 is provided by a host (not shown). The host may be a system processor (not shown) or a graphics application running on the system processor. In an alternate embodiment, an Accelerated Graphics Port (AGP) 32 or other suitable port receives the graphics data 31 from the host and provides the graphics data 31 to the graphics processing circuit 34 for further processing.

[0021] The graphics processing circuit 34 includes a first graphics pipeline 101 operative to process graphics data in a first set of tiles as discussed in greater detail below. The first pipeline 101 includes front end circuitry 35, a scan converter 37, and back end circuitry 39. The graphics processing circuit 34 also includes a second graphics pipeline 102, operative to process graphics data in a second set of tiles as discussed in greater detail below. The first graphics pipeline 101 and the second graphics pipeline 102 operate independently of one another. The second graphics pipeline 102 includes the front end circuitry 35, a scan converter 40, and back end circuitry 42. Thus, the graphics processing circuit 34 of the present invention is configured as a multi-pipeline circuit, where the back end circuitry 39 of the first graphics pipeline 101 and the back end circuitry 42 of the second graphics pipeline 102 share the front end circuitry 35, in that the first and second graphics pipelines 101 and 102 receive the same pixel data 36 provided by the front end circuitry 35. Alternatively, the back end circuitry 39 of the first graphics pipeline 101 and the back end circuitry 42 of the second pipeline 102 may be coupled to separate front end circuits. Additionally, it will be appreciated that a single graphics processing circuit can be configured in similar fashion to include more than two graphics pipelines. The illustrated graphics processing circuit 34 has the first and second pipelines 101-102 present on the same chip. However, in alternate embodiments, the first and second graphics pipelines 101-102 may be present on multiple chips interconnected by suitable communication circuitry or a communication path, for example, a synchronization signal or data bus interconnecting the respective memory controllers.

[0022] The front end circuitry 35 may include, for example, a vertex shader, set up circuitry, rasterizer or other suitable circuitry operative to receive the primitive data 31 and generate pixel data 36 to be further processed by the back end circuitry 39 and 42, respectively. The front end circuitry 35 generates the pixel data 36 by performing, for example, clipping, lighting, spatial transformations, matrix operations and rasterizing

[redacted]

operations on the primitive data 31. The pixel data 36 is then transmitted to the respective scan converters 37 and 40 of the two graphics pipelines 101-102.

[0023] The scan converter 37 of the first graphics pipeline 101 receives the pixel data 36 and sequentially provides the position (e.g. x, y) coordinates 60 in screen space of the pixels to be processed by the back end circuitry 39 by determining or identifying those pixels of the primitive, for example, the pixels within portions 81-82 of the triangle 80 (FIG. 3) that intersect the tile or set of tiles that the back end circuitry 39 is responsible for processing. The particular tile(s) that the back end circuitry 39 is responsible for is determined based on the tile identification data present on the pixel identification line 38 of the scan converter 37. The pixel identification line 38 is illustrated as being hard wired to ground. Thus, the tile identification data corresponds to a logical zero. This corresponds to the back end circuitry 39 being responsible for processing the tiles labeled "A" (e.g. 72 and 75) in FIG. 3. Although the pixel identification line 38 is illustrated as being hard wired to a fixed value, it is to be understood and appreciated that the tile identification data can be programmable data, for example, from a suitable driver and such a configuration is contemplated by the present invention and is within the spirit and scope of the instant disclosure.

[0024] Back end circuitry 39 may include, for example, pixel shaders, blending circuits, z-buffers or any other circuitry for performing pixel appearance attribute operations (e.g. color, texture blending, z-buffering) on those pixels located, for example, in tiles 72, 75 (FIG. 3) corresponding to the position coordinates 60 provided by the scan converter 37. The processed pixel data 43 is then transmitted to graphics memory 48 via memory controller 46 for storage therein at locations corresponding to the position coordinates 60.

[0025] The scan converter 40 of the second graphics pipeline 102, receives the pixel data 36 and sequentially provides position (e.g. x, y) coordinates 61 in screen space of the pixels to be processed by the back end circuitry 42 by determining those pixels of the primitive, for example, the pixels within portions 83-84 of the triangle 80 (FIG. 3) that intersect the tiles that the back end circuitry 42 is responsible for processing. Back end circuitry 42 tile responsibility is determined based on the tile identification data present on the pixel identification line 41 of the scan converter 41. The pixel

[redacted]

identification line 41 is illustrated as being hard wired to V_{CC}; thus, the tile identification data corresponds to a logical one. This corresponds to the back end circuitry 42 being responsible for processing the tiles labeled "B" (e.g. 73-74) in FIG. 3. Although the pixel identification line 41 is illustrated as being hard wired to a fixed value, it is to be understood and appreciated that the tile identification data can be programmable data, for example, from a suitable driver and such configuration is contemplated by the present invention and is within the spirit and scope of the instant disclosure.

[0026] Back end circuitry 42 may include, for example, pixel shaders, blending circuits, z-buffers or any suitable circuitry for performing pixel appearance attribute operations on those pixels located, for example, in tiles 73 and 74 (FIG. 3) corresponding to the position coordinates 61 provided by the scan converter 40. The processed pixel data 44 is then transmitted to the graphics memory 48, via memory controller 46, for storage therein at locations corresponding to the position coordinates 61.

[0027] The memory controller 46 is operative to transmit and receive the processed pixel data 43-44 from the back end circuitry 39 and 42; transmit and retrieve pixel data 49 from the graphics memory 48; and in a single circuit implementation, transmit pixel data 50 for presentation on a suitable display 51. The display 51 may be a monitor, a CRT, a high definition television (HDTV) or any other device or combination thereof.

[0028] Graphics memory 48 may include, for example, a frame buffer that also stores one or more texture maps. Referring to FIG. 3, the frame buffer portion of the graphics memory 48 is partitioned in a repeating tile pattern of horizontal and vertical square regions or tiles 72-75, where the regions 72-75 provide a two dimensional partitioning of the frame buffer portion of the memory 48. Each tile is implemented as a 16 x 16 pixel array. The repeating tile pattern of the frame buffer 48 corresponds to the partitioning of the corresponding display 51 (FIG. 2). When rendering a primitive (e.g. triangle) 80, the first graphics pipeline 101 processes only those pixels in portions 81, 82 of the primitive 80 that intersects tiles labeled "A", for example, 72 and 75, as the back end circuitry 39 is responsible for the processing of tiles corresponding to tile identification 0 present on pixel identification line 38 (FIG. 2). In corresponding fashion, the second graphics pipeline 102 processes only those pixels in portions 83, 84 of the

primitive 80 that intersects tiles labeled "B", for example 73-74, as the back end circuitry 42 (FIG. 2) is responsible for the processing of tiles corresponding to tile identification 1 present on pixel identification line 41 (FIG. 2).

[0029] By configuring the frame buffer 48 according to the present invention, as the primitive data 31 is typically written in strips, the tiles (e.g. 72 and 75) being processed by the first graphics pipeline 101 and the tiles (e.g. 73 and 74) being processed by the second graphics pipeline 102 will be substantially equal in size, notwithstanding the primitive 80 orientation. Thus, the amount of processing performed by the first graphics pipeline 101 and the second graphics pipeline 102, respectively, are substantially equal; thereby, effectively eliminating the load balance problems exhibited by conventional techniques.

[0030] FIG. 4 is a schematic block diagram of a frame buffer 68 partitioned into a super-tile pattern according to an alternate embodiment of the present invention. Such a partitioning would be used, for example, in conjunction with a multi-processor implementation to be discussed below with reference to FIG. 5. As illustrated, the frame buffer 68 is partitioned into a repeating tile pattern where the tiles, for example, 92-99 that form the repeating tile pattern are the responsibility of and processed by a corresponding one of the graphics pipelines provided by the multi-processor implementation.

[0031] FIG. 5 is a schematic block diagram of a graphics processing circuit 54 which may be coupled with the graphics processing circuit 34 (FIG. 2), for example, by the AGP 32 or other suitable port, to form one embodiment of a multi-processor implementation. The graphics processing circuit 54 is preferably a portion of a stand-alone graphics processor chip or may also be integrated with a host processor or other circuit, if desired, or port of a larger system. The multi-processor implementation exhibits an increased fill rate of, for example, 9.6 billion pixels/sec with a triangle rate of 300 million triangles/sec. This represents a tremendous performance increase as compared to conventional graphics processing systems. The triangle rate is defined as the number of triangles the graphics processing circuit can generate per second. The fill rate is defined as the number of pixels the graphics processing circuit can render per second.

[redacted]

[0032] Referring briefly to FIG. 2, in the multi-processor implementation, processed pixel data 52 from the graphics processing circuit 34 is provided as a first of two inputs to a high speed switch 70. The second input to the high speed switch 70 is the processed pixel data 55 from the graphics processing circuit 54. The high speed switch 70 has a switching frequency (f) sufficient to provide the pixel information 71 to a suitable display device without any detectable latency.

[0033] Returning to FIG. 5, the graphics processing circuit 54 includes a third graphics pipeline 201 operative to process graphics data in a third set of tiles. The third graphics pipeline 201 includes front end circuitry 135, which may be the front end circuitry 35 discussed with reference to FIG. 2, a scan converter 137 and back end circuitry 139. The graphics processing circuit 54 also includes a fourth graphics pipeline 202, operative to process graphics data in a fourth set of tiles. The fourth graphics pipeline 202 includes the front end circuitry 135, a scan converter 140 and back end circuitry 142. The third graphics pipeline 201 and the fourth graphics pipeline 202 also operate independently of one another. Thus, the graphics processing circuit 54 is configured as a multi-pipeline circuit, where the back end circuitry 139 of the third graphics pipeline 201 and the back end circuitry 142 of the fourth graphics pipeline 202 share the front end circuitry 135, in that the respective back end circuitry 139 and 142 receives the same pixel data from the front end circuitry 135. As illustrated, the components of the third and fourth graphics pipelines are present on a single chip. Additionally, the back end circuitry 139 and the back end circuitry 142 may be configured to share the front end circuitry 35 of the graphics processing circuit 34. Alternatively, the third and fourth graphics pipelines may be configured to be on multiple chips interconnected by a communication path, for example, a synchronization signal or data bus.

[0034] The front end circuitry 135 may include, for example, a vertex shader, set up circuitry, rasterizer or other suitable circuitry operative to receive the primitive data 31 from the AGP 32 and generate pixel data 136 to be processed by the third graphics pipeline 201 and fourth graphics pipeline 202, respectively. The front end circuitry 135 generates the pixel data 136 by performing, for example, clipping, lighting, spatial transformations, matrix operations, rasterization or any suitable primitive operations or

[redacted]

combination thereof on the primitive data 31. The pixel data 136 is then transmitted to the respective scan converters 137 and 140 of the two graphics pipelines 201-202.

[0035] The scan converter 137 of the third graphics pipeline 201 receives the pixel data 136 and sequentially provides the position (e.g. x, y) coordinates 160 in screen space of the pixels to be processed by the back end circuitry 139, based on the tile identification data present on pixel identification line 138. In corresponding fashion, scan converter 140 of the fourth graphics pipeline 202 receives the pixel data 136 and sequentially provides the position (e.g. x, y) coordinates 161 in screen space of the pixels to be processed by the back end circuitry 143, based on the tile identification data present on pixel identification line 141.

[0036] Referring to FIG. 4, in the multi-processor implementation, when a logical zero or other suitable value is present on pixel identification line 138 (e.g. corresponding to the pixel identification line 138 being tied to ground), the back end circuitry 139 is responsible for processing, for example, tiles labeled "A0" (e.g. 92 and 95). In corresponding manner, when a logical one or other suitable value is present on pixel identification line 141 (e.g. corresponding to pixel identification line 142 being tied to V_{CC}), the back end circuitry 142 will be responsible for processing the tiles labeled "B0" (e.g. 93 and 94). When a logical zero or other suitable value is present on pixel identification line 38 (FIG. 2), the back end circuitry 39 is responsible for processing, for example, the tiles labeled "A1" (e.g. 96 and 99). When a logical one or other suitable value is present on pixel identification line 41 (FIG. 2), the back end circuitry 42 is responsible for processing, for example, the tiles labeled "B1" (e.g. 97 and 98). The tile pattern illustrated in FIG. 4 is referred to as a super-tile pattern 68.

[0037] As illustrated, the super-tile pattern 68 is formed of a horizontally and vertically repeating pattern of regions or tiles 92-99, where each tile is a 16 x 16 pixel array. With this frame buffer configuration, as the primitive data 31 is typically written in strips, at least one tile (e.g. 92) being processed by the third graphics pipeline 201 and at least one tile (e.g. 93) being processed by the fourth graphics pipeline 202 will be intersected or contain at least a portion of the primitive data 31, notwithstanding the primitive orientation; thereby achieving substantially equal load balancing between the pipelines.

[redacted]

[0038] Thus, in the multi-processor implementation, each of the graphics pipelines is responsible for processing 1/(MxN) of the tiles present in the partitioned graphics memory 68, where M represents the number of pipelines per circuit and N represents the number of graphics processing circuits being used. Thus, in an embodiment where graphics processing circuit 34 and graphics processing circuit 54 are combined, for example, through AGP 32 (FIG. 2), each graphics pipeline 101, 102, 201 and 202 will be responsible for processing one-fourth of the tiles 92-99 of the repeating tile pattern. This results in increased graphics processing performance as each graphics pipeline is responsible for processing one-quarter of total pixels maintained in the frame buffer 68.

[0039] FIG. 6 is a flow chart of the operations performed by the graphics processing circuit 34 according to the present invention. In the multi-processor implementation, graphics processing circuits 34 and 54 perform substantially the same operations. In step 100, the front end circuitry 35 receives the graphics data 31 (FIG. 2), for example, vertex data of an object to be rendered and generates corresponding pixel data 36 (FIG. 2) in response to the primitive data 31 in step 102. The pixel data may be generated by performing, for example, clipping, lighting, spatial transformations. matrix transformations and rasterizing operations on the graphics data 31.

[0040] In step 104, the pixels within a set of tiles of the repeating tile pattern to be processed by a corresponding one of the at least two graphics pipelines in response to the pixel data is determined. This is accomplished, for example, in step 105 by the scan converter 37 determining which of tiles (e.g. 72 and 75) of the repeating tile pattern are to be processed by the back end circuitry 39 based on the tile identification data present on the pixel identification line 38. Next, in step 106, the scan converter 37 provides the position coordinates 60 of the pixels within portions 81-82 of the triangle 80 that intersect the tiles (e.g. 72 and 75) to the back end circuitry 39.

[0041] In step 108, pixel operations are performed on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines is performed. This is accomplished, for example, by the back end circuitry 39 performing color, shading, blending, texturing and/or z-buffering operations on the pixels within the portions (e.g. 81-82) of the tiles (e.g. 72 and 75) they are responsible for.

[redacted]

[0042] In step 109, a determination is made as to whether the processing is complete. If the processing is complete, the process proceeds to step 100 where vertex data for a new primitive is received. Otherwise, the process ends. In the multi-processor implementation, graphics processing circuit 54 performs substantially the same operations as discussed above, in conjunction with graphics processing circuit 34.

[0043] As noted above, a rasterizer setup unit manages the distribution of polygons to the different rasterizer pipelines within a chip. The design divides the screen into multiple square tiles. Each pipeline is responsible for a subset of the tiles. In our design, the tile sizes are 8 x 8 pixels, 16x16 pixels (default) or 32x32 pixels. However, any number of square pixels or even non-square tiles could be done. It will be recognized that the number of pixels in the tiles be a common divisor of the number of pixels on the screen, in both X and Y directions.

[0044] Vertices are given by the application currently executing on the host. The vertices are converted from object space three-dimensional homogeneous coordinate system to a screen based coordinate system. This conversion can be done on the host processor or in the front end section of the graphics chip (i.e. vertex transformation). The screen based coordinate system has at least X and Y coordinates for each vertex.

[0045] As shown in FIG. 7, the setup unit creates a bounding box based on the screen space X, Y coordinates of each vertex. This bounding box is then compared against the current tile pattern. This tiling pattern is based on the number of graphics pipelines currently active. In the one pipe configuration, the tiles just repeat and are all mapped to the same pipeline. In the two pipe configuration, a "checkerboard" pattern is created for the pipes and the patterns repeat over the full screen.

[0046] The bounding boxes' four corners are mapped to the tile pattern, simply by discarding the lower bits of X & Y. The four corners map to the same or different tiles. If they all map to the same tile, then only the pipeline that is associated with that tile receives the polygon. If it maps to only tiles that are associated with only one pipeline, then again only that pipeline receives the polygon. If it maps to tiles that are associated with multiple pipelines, then the entire polygon is sent to all pipelines. In our implementation, we broadcast the polygon to all pipelines, masking the pipelines that

should not receive it. Consequently, polygons can be sent to only one pipe or up to all the pipes, depending on the coverage of the tiles by the polygon.

[0047] For super tiling when using multiple graphics chips, the rasterizer setup unit manages the distribution of polygons to different graphics chips. The super tiles, which are a square assembly of pixels, are used to perform load balancing between each processor. Basically, each processor is responsible for generating all of the pixels in its subset of super tiles. The tiles are distributed evenly across all processors, in a checkerboard pattern. The tile size is variable, but one implementation may be 32x32 pixels, or 2x2 tiles. This amount can be changed through programming registers. Super tiles do not have to be of a size which is a common divisor of the screen resolution, but it's more efficient if it is. The number of chips in use should be a power of two.

[0048] FIG. 8 shows some examples of super tile configurations for various numbers of chips (super tile size or STS). As shown, C# represents the tile that chip # controls. The patterns repeat across the whole screen, in both X & Y directions, until the full screen is fully covered. For odd powers of 2 (STS=2, STS=8), a simple square pattern of different chips cannot be made, so a secondary pattern of checkerboard is applied to generate a square arrangement.

[0049] In operation, an application generates vertex data, which assembles into polygons (i.e. 2 vertices for a line, 3 for a triangle). Each vertex's homogeneous object space coordinate (generated by the application) is transformed into screen space coordinates by either the host or the front end of the graphics chip (transform unit or vertex processor). The screen space coordinates hold X, Y coordinates (in screen pixels) for each of the vertices. The polygons coming from an application are all broadcast to all chips. Each chip processes the vertices as needed to generate the same X, Y coordinates for all vertices. Then, each chip creates a bounding box around the polygon as shown in FIG. 7. The X, Y coordinates of each corner of the bounding box is checked against the super tiles that belongs to each processor. If the bounding box overlaps a super tile assigned to a given processor, then that processor must render some or the entire polygon. The setup unit then sends the whole polygon to the various raster pipe(s). If the bounding box does not overlap any of the tiles associated with a processor, then the setup unit rejects the whole polygon and processes the next one.

[redacted]

[0050] In this way, triangle setup performance does not scale with each processor (since all polygons go through all setup units), but fill rate (defined as the number of pixels output total) does scale with each processor added.

[0051] The above detailed description of the invention and the examples described therein have been provided for the purposes of illustration and description. Although an exemplary embodiment of the present invention has been described in detail herein with reference to the accompanying drawings, it is to be understood that the present invention is not limited to the precise embodiment disclosed, and that various changes and modifications to the invention are possible in light of the above teaching. Accordingly, the scope of the present invention is to be defined by the claims appended hereto.

CLAIMS

What is claimed is:

1. A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile,

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

[redacted]

8. The graphics processing circuit of claim 4, wherein the at least two graphics pipelines are on multiple chips.

9. The graphics processing circuit of claim 1, further including a memory controller coupled to the at least two graphics pipeline, operative to transfer pixel data between each of the first pipeline and the second pipeline and a memory.

10. The graphics processing circuit of claim 4, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the pixel data only in a second set of tiles in the repeating tile pattern.

13. The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

[redacted]

19. The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; and

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines.

21. The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. The graphics processing method of claim 20, further comprising transmitting the processed pixels to memory.

[redacted]

24. A graphics processing circuit, comprising:

front end circuitry operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles or the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller, coupled to the first and second back end circuitry. operative to receive transmit and receive the processed pixel data.

DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

ABSTRACT

A graphics processing circuit includes at least two pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern, a respective one of the at least two pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. A graphics processing method includes receiving vertex data for a primitive to be rendered; generating pixel data in response to the vertex data; determining the pixels within a set of tiles of a repeating tile pattern to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; and performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines.

[redacted]

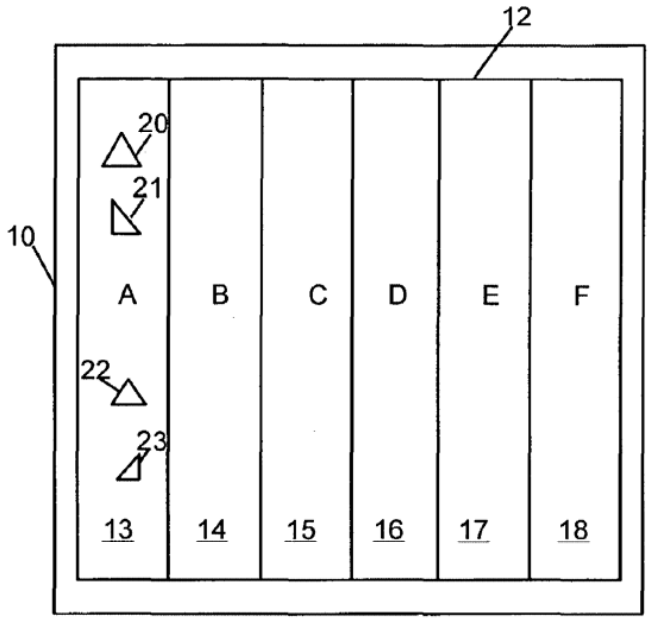


FIG. 1
PRIOR ART

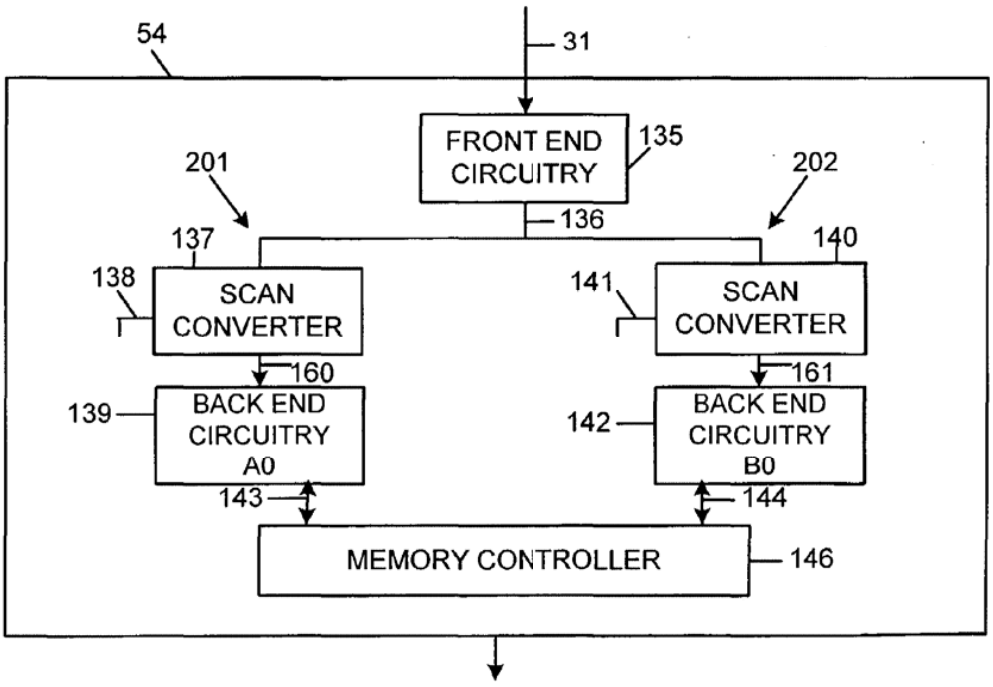
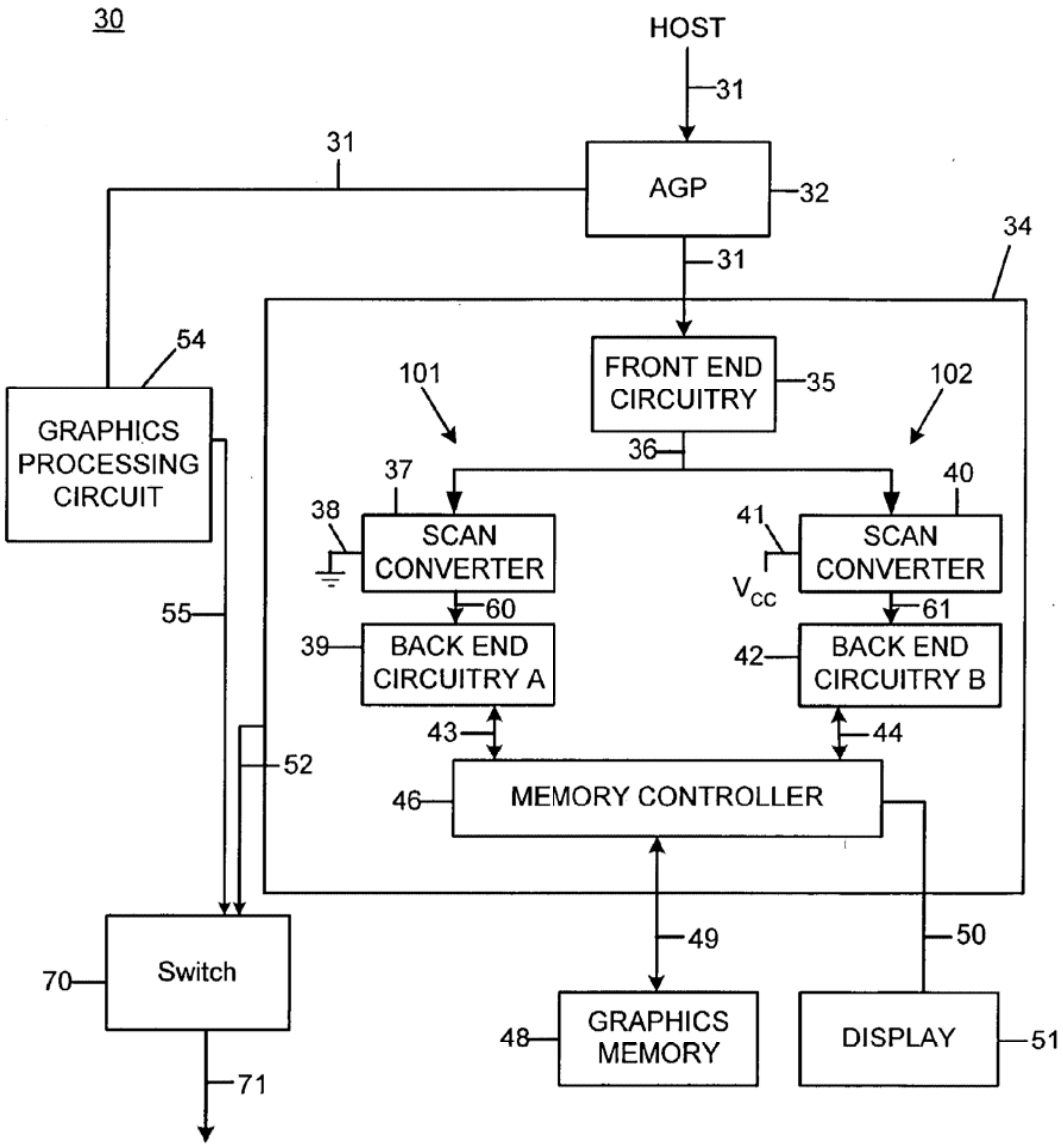


FIG. 5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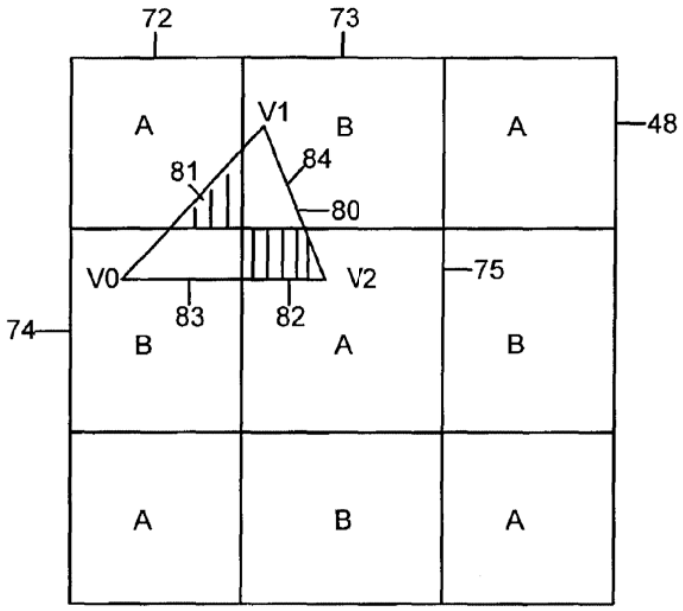
HOST
31
31
AGP
32
34
31
54
101
FRONT END CIRCUITRY
35
102
GRAPHICS PROCESSING CIRCUIT
36
37
40
38
SCAN CONVERTER
41
SCAN CONVERTER
V_{CC}
55
60
61
39
BACK END CIRCUITRY A
42
BACK END CIRCUITRY B
43
44
52
46
MEMORY CONTROLLER
49
50
70
Switch
48
GRAPHICS MEMORY
DISPLAY
51
71

FIG. 2


72
73
A
V1
B
A
48
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84
80
V0
V2
75
83
82
74
B
A
B
A
B
A

FIG. 3

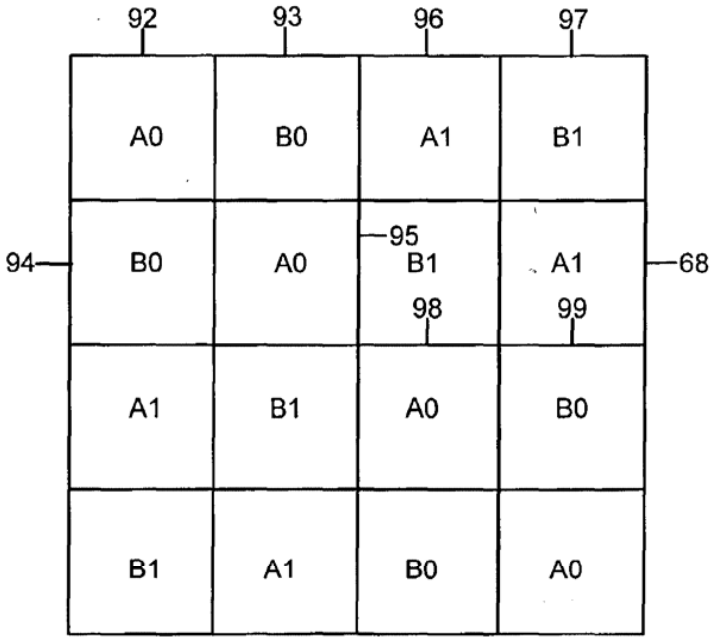
92
93
96
97
A0
B0
A1
B1
95
94
B0
A0
B1
A1
68
98
99
A1
B1
A0
B0
B1
A1
B0
A0

FIG. 4

START
RECEIVE VERTEX DATA FOR A PRIMITIVE TO BE RENDERED
100
GENERATE PIXEL DATA IN RESPONSE TO THE VERTEX DATA
102
DETERMINE THE PIXELS WITHIN A SET OF TILES OF THE REPEATING TILE PATTERN TO BE PROCESSED BY A CORRESPONDING ONE OF THE AT LEAST TWO GRAPHICS PIPELINES IN RESPONSE TO THE PIXEL DATA, THE REPEATING TILE PATTERN INCLUDING A HORIZONTALLY AND VERTICALLY REPEATING PATTERN OF SQUARE REGIONS
104
DETERMINE THE SET OF TILES THAT THE CORRESPONDING GRAPHICS PIPELINE IS RESPONSIBLE FOR
105
PROVIDE POSITION COORDINATES OF THE PIXELS WITHIN THE DETERMINED SET OF TILES TO BE PROCESSED
106
PERFORM PIXEL OPERATIONS ON THE PIXELS WITHIN THE DETERMINED SET OF TILES BY THE CORRESPONDING ONE OF THE AT LEAST TWO GRAPHICS PIPELINES
108
PROCESSING COMPLETE ?
109
Y
N
END

FIG. 6

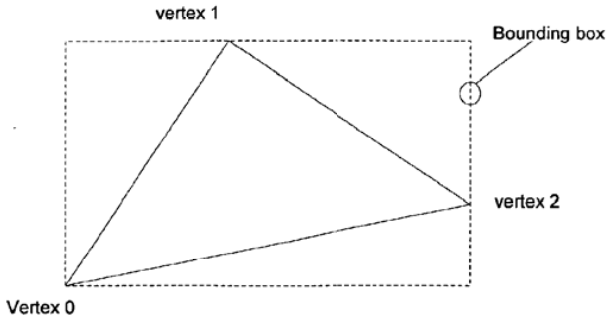
vertex 1
Bounding box
vertex 2
Vertex 0

FIG. 7

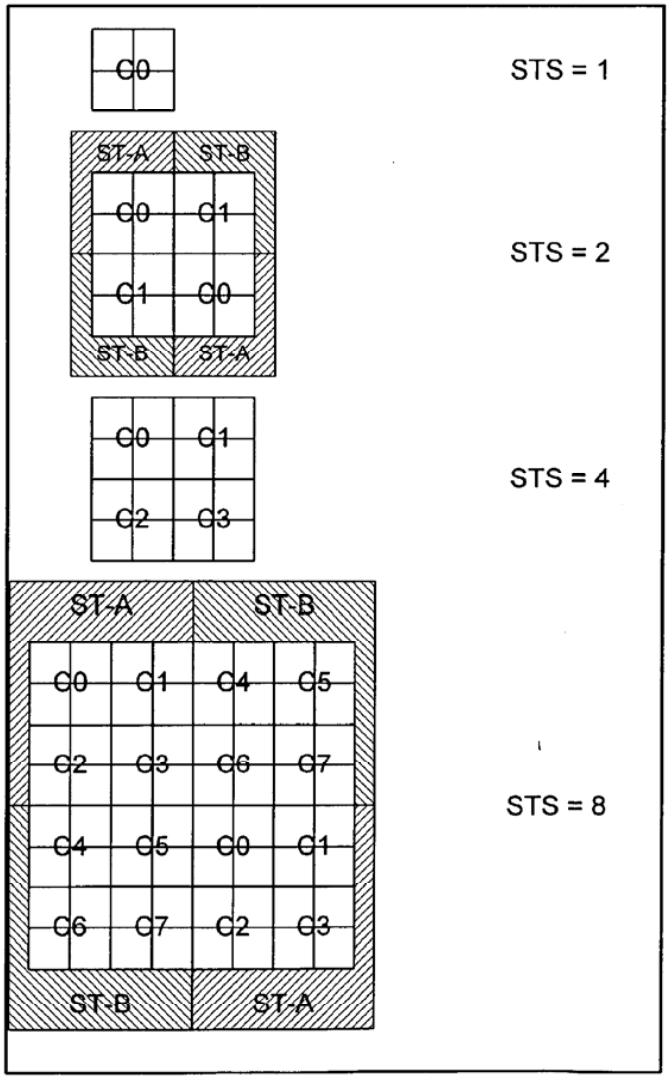
C0
STS = 1
ST-A
ST-B
C0
C1
C1
C0
ST-B
ST-A
STS = 2
C0
C1
C2
C3
STS = 4
ST-A
ST-B
C0
C1
C4
C5
C2
C3
C6
C7
C4
C5
C0
C1
C6
C7
C2
C3
ST-B
ST-A
STS = 8

FIG. 8

020053

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☒ Declaration Submitted with Initial Filing, OR
☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(e)) required)

Attorney Docket Number 00100.02.0053
First Named Inventor: Mark M. Leather
COMPLETE IF KNOWN
Application Number:
Filing Date:
Group Art Unit:
Examiner Name:

As a below named inventor, I hereby declare that:
My residence, post office address, and citizenship are as stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

the specification of which:
☒ is attached hereto.
☐ was filed on _____ as _____ Application Number _____ or as PCT International Application Number _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Data (MM/DD/YYYY)
60/429,641	11/27/2002

☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

[redacted]

020053

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transaction all business in the Patent and Trademark Office connected therewith:

Name	Registration Number	Name	Registration Number
Christopher J. Reckamp	34,414	Angelo J. Bufalino	29,622
Joseph P. Krause	32,578	Robert Beiser	28,687
Michael J. Turgeon	39,404	Brent A. Boyd	51,020
Timothy J. Bechen	48,126	Themi Anagnos	47,388

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.\

Direct all correspondence to:

Vedder, Price, Kaufman & Kammholz
222 N. LaSalle Street, Suite 2600
Chicago, Illinois 60601
Telephone: 312-609-7500
Facsimile: 312-609-5005

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

☐ A petition has been filed for this unsigned inventor

Name of Sole or First Inventor:

Given Name (first and middle [if any]			Family Name or Surname	
Mark M.			Leather	
Inventor's Signature	Mark M Leather		**Date** 5/23/03	
Residence	City: Saratoga	State: California	Country: USA	Citizenship: United Kingdom
Post Office Address	12187 Woodside Drive			
City: Saratoga	State: California		ZIP: 95070	Country: USA

☐ A petition has been filed for this unsigned inventor

Name of Additional Joint Inventor:

Given Name (first and middle [if any]			Family Name or Surname	
Eric			Demers	
Inventor's Signature	Eric Demers		**Date** 6/2/03	
Residence	City: Palo Alto	State: California	Country: USA	Citizenship: Canadian
Post Office Address	901 Sycamore Drive			
City: Palo Alto	State: California		ZIP: 94303	Country: USA

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

06/16/2003 DTESSEM1 00000014 500441 10459797

01 FC:1001 750.00 CH
02 FC:1202 72.00 CH

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10459797

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	72
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

CLAIMS ONLY	SERIAL NO.	FILING DATE
	APPLICANT(S)	

CLAIMS

	AS FILED		AFTER 1ST AMENDMENT		AFTER 2ND AMENDMENT							
	IND	DEP	IND	DEP	IND	DEP		IND	DEP	IND	DEP	IND	DEP
1	1						51						
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50							100						
TOTAL IND.	3						TOTAL IND.						
TOTAL DEP.	21						TOTAL DEP.						
TOTAL CLAIMS	24						TOTAL CLAIMS						

PTO-2202 (Replication only) (1/03)

BEST AVAILABLE COPY

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10459797

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	72
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	

6/12/03

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 24	Minus	** 24	=
Independent	* 3	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	257	345/506.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/08 13:46
S2	50	345/506.ccls. and tile	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:58
S3	41	345/506.ccls. and tile and frame adj buffer	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:59
S4	41	345/506.ccls. and tile and frame adj buffer and pixel	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:59
S5	36	345/506.ccls. and tile and frame adj buffer and pixel and vertex	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:59
S6	33	345/506.ccls. and tile and frame adj buffer and pixel and vertex and primitive	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:59
S7	33	345/506.ccls. and tile and frame adj buffer and pixel and vertex and primitive and render$3	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:59
S8	7	345/506.ccls. and tile and frame adj buffer and pixel and vertex and primitive and render$3 and scan adj converter	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:03
S9	24	345/506.ccls. and multiple adj pipelines	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:21
S10	9	345/506.ccls. and multiple adj pipelines and tile	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:01
S12	7	345/506.ccls. and tile and frame adj buffer and pixel and vertex and primitive and render$3 and scan adj converter and "16"	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:34
S13	13	345/506.ccls. and multiple adj pipelines and chip$1	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:08
S14	5	345/506.ccls. and multiple adj pipelines and memory adj controller	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:08
S15	15	345/506.ccls. and scan adj converter	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:11
S16	14	345/506.ccls. and scan adj converter and coordinates	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:11
S17	3	345/506.ccls. and multiple adj pipelines and scan adj converter	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:21
S18	127	345/506.ccls. and polygon	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:24
S20	40	345/506.ccls. and polygon and bounding adj box	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:24
S21	25	345/506.ccls. and polygon and bounding adj box and tile	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:26

S22	21	345/506.ccls. and polygon and bounding adj box and tile and overlap	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:26
S23	19	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:26
S24	4	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and scan adj converter	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:26
S25	19	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and pixel	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:27
S26	19	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and pixel and vertex	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:27
S27	19	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and pixel and vertex and primitive	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:27
S28	16	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and pixel and vertex and primitive and frame adj buffer	US-PGPUB; USPAT	OR	OFF	2004/12/08 15:21
S29	3	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and pixel and vertex and primitive and frame adj buffer and multiple adj pipelines	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:28
S30	1	345/506.ccls. and repeating adj tile$1	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:31
S31	35	repeating adj tile$1	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:31
S32	10	repeating adj tile$1 and graphics	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:31
S33	1	("6753878").PN.	USPAT	OR	OFF	2004/12/07 15:34
S34	11	345/506.ccls. and front adj end and back adj end	US-PGPUB; USPAT	OR	OFF	2004/12/08 13:46
S36	222	345/530.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/08 15:24
S37	245	345/505.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/08 15:28

Search Notes	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2676	

SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505	12/7/2004	

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached search history.	12/7/2004	

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIBDATASHEET

Bib Data Sheet

CONFIRMATION NO. 4148

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/459,797	06/12/2003 RULE	345	2676	00100.02.0053

APPLICANTS

Mark M. Leather, Saratoga, CA;

Eric Demers, Palo Alto, CA;

** CONTINUING DATA **********

This appln claims benefit of 60/429,641 11/27/2002

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 08/07/2003

Foreign Priority claimed ☐ yes ☑ no 35 USC 119 (a-d) conditions met ☐ yes ☑ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature Initials	STATE OR COUNTRY CA	SHEETS DRAWING 5	TOTAL CLAIMS 24	INDEPENDENT CLAIMS 3

ADDRESS
Christopher J. Reckamp
Vedder, Price, Kaufman & Kammholz
222 North LaSalle Street
Chicago , IL
60601

TITLE
Dividing work among multiple graphics pipelines using a super-tiling technique

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue)

822		☐ Other ☐ Credit

Index of Claims

Application No.	Applicant(s)
10/459,797	LEATHER ET AL.
Examiner	**Art Unit**
Joni Hsu	2676

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	12/19/04
	1	✓
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Claim		Date
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Claim		Date
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

7590 12/14/2004

Christopher J. Reckamp
Vedder, Price, Kaufman & Kammholz
222 North LaSalle Street
Chicago, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☒ Claim(s) *9 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 9 objected to because of the following informalities: In line 6 on page 17, the claim states "two graphics pipeline" where it should state "two graphics pipelines". Appropriate correction is required.

2. Claim 24 objected to because of the following informalities: In lines 14-15 on page 20, the claim states "set of tiles *or* the repeating tile pattern" where it should state "set of tiles *of* the repeating tile pattern". In line 18 on page 20, the claim states "*receive* transmit and receive" where it should state "transmit and receive". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 9, 12, and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "the first pipeline" and "the second pipeline". There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "the pixel data". There is insufficient antecedent basis for this limitation in the claim.

Claim 13 recites the limitation "the front end circuitry" and "the back end circuitry". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-8, 10-18, and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal (US006762763B1) in view of Heirich (US006753878B1), further in view of Duffy (US005179640A).

8. With regard to Claim 1, Migdal describes a graphics processing circuit, comprising a graphics pipeline (Col. 1, line 66-Col. 2, line 17) operative to process data in a corresponding set of tiles, the graphics pipeline operative to process data in a dedicated tile (Col. 8, lines 20-23).

However, Migdal does not teach that there are at least two graphics pipelines and each graphics pipeline processes data in a dedicated tile. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33) and each graphics pipeline processes data in a dedicated part of the image (PI, Col. 6, lines 1-6).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Migdal so that there are at least two graphics pipelines and each graphics pipeline processes data in a dedicated tile as suggested by Heirich. Heirich suggests that it is advantageous to use multiple graphics pipelines because each pipeline can work on a different process or part of the image without waiting for the other processes to finish first (Col. 2, lines 24-39), so using multiple graphics pipelines speeds up the processing operation.

However, Migdal and Heirich do not teach a repeating tile pattern, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. However, Duffy describes a repeating tile pattern, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Col. 3, line 67-Col. 4, line 4; Col. 4, lines 31-32; Col. 5, lines 17-20).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Migdal and Heirich to include a repeating tile pattern, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions

as suggested by Duffy because Duffy suggests that rather than generating an entire simulated halftone screen for each process color of an image, which takes up substantial additional computing power, a set of rectangular repeating patterns can be stored and retrieved for use in filling incremental regions of the image (Col. 3, line 63-Col. 4, line 4).

9. With regard to Claim 2, Migdal describes that the square regions comprise a two dimensional partitioning of memory (Col. 7, lines 63-65).

10. With regard to Claim 3, Migdal describes that the memory is a frame buffer (Col. 5, lines 63-67).

11. With regard to Claim 4, Migdal describes that the graphics pipeline further includes front end circuitry (105, Figure 1) operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered (Col. 4, lines 46-51; Col. 5, lines 39-41; Col. 8, lines 17-19), and back end circuitry (108), coupled to the front end circuitry, operative to receive and process a portion of the pixel data (Col. 4, lines 46-51).

However Migdal does not teach that there are two graphics pipelines operative to receive and process a portion of the pixel data. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33) operative to receive and process a portion of the pixel data (PI, Col. 6, lines 1-6), as discussed in the rejection for Claim 1.

12. With regard to Claim 5, Migdal describes that the graphics pipeline further includes a scan converter (602, Figure 6), coupled to the back end circuitry (603-615), operative to determine the portion of the pixel data to be processed by the back end circuitry (Col. 8, lines 7-19).

However Migdal does not teach that there are two graphics pipelines. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33), as discussed in the rejection for Claim 1.

13. With regard to Claim 6, Migdal describes that each tile of the set of tiles further comprises a 16x16 pixel array (Col. 7, lines 63-65).

14. With regard to Claim 7, Migdal does not teach that the at least two graphics pipelines separately receive the pixel data from the front end circuitry. However, Heirich describes that the at least two graphics pipelines (22, 24, Figure 1) separately receive the pixel data (PI) from the front end circuitry (22) (Col. 6, lines 1-6).

It would have been obvious at the time of invention by applicant to modify the device of Migdal so that the at least two graphics pipelines separately receive the pixel data from the front end circuitry as suggested by Heirich. Since Heirich describes using multiple graphics pipelines, each graphics pipeline must inherently separately receive the pixel data from the front end circuitry. The advantages of using multiple graphics pipelines were discussed in the rejection for Claim 1.

15. With regard to Claim 8, Migdal does not teach that the at least two graphics pipelines are on multiple chips. However, Heirich describes multiple graphics pipelines and that each graphics pipeline can be on a separate workstation (Figure 4; Col. 16, lines 53-59). Since the graphics pipelines are on separate workstations, the graphics pipelines must inherently be on multiple chips.

It would have been obvious at the time of invention by applicant to modify the device of Migdal so that the at least two graphics pipelines are on multiple chips as suggested by Heirich because Heirich suggests the advantage of being able to put the different chips on different workstations. In this configuration, off-the-shelf workstations and graphics accelerator cards can be used for image generation, which greatly reduces the cost of the system. The marginal costs of the image generation process might be reduced even further if the workstations and graphics accelerators are used for other purposes (Col. 16, lines 41-46).

16. With regard to Claim 10, Migdal does not teach that a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1), and each graphics pipeline processes only a part of an image (PI; Col. 6, lines 1-6). Therefore, Heirich describes that a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles.

However, Migdal and Heirich do not teach a repeating tile pattern. However, Duffy describes a repeating tile pattern (Col. 4, lines 26-53; Col. 5, lines 17-20), as discussed in the rejection for Claim 1.

17. With regard to Claim 11, Migdal describes that the graphics pipeline further includes a scan converter (602, Figure 6), coupled to the front end circuitry (105, Figure 1) and the back end circuitry (603-615, Figure 6), operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry (Col. 8, lines 17-19). The scan converter provides position coordinates to the texture request generator (603). From these position coordinates, the texture request generator knows which of the set of tiles is to be processed by the back end circuitry and generates the required tile addresses for theses tiles (Col. 8, lines 17-23). Therefore, the scan converter must inherently include a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

However Migdal does not teach that there are two graphics pipelines. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33), as discussed in the rejection for Claim 1.

18. With regard to Claim 12, Claim 12 is similar in scope to Claim 10, and therefore is rejected under the same rationale.

19. With regard to Claim 13, Claim 13 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

20. With regard to Claim 14, Migdal describes a graphics pipeline (Col. 1, line 66-Col. 2, line 17) including front end circuitry (105, Figure 1) operative to receive vertex data and generate

pixel data corresponding to a primitive to be rendered (Col. 4, lines 46-51; Col. 5, lines 39-41; Col. 8, lines 17-19), and back end circuitry (108), coupled to the front end circuitry, operative to receive and process the pixel data in a set of tiles in the repeating tile pattern (Col. 4, lines 46-51).

However, Migdal does not teach a third graphics pipeline and a fourth graphics pipeline. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33), as discussed in the rejection for Claim 1. Heirich also describes that each pipeline processes the pixel data only in one set of tiles in the repeating tile pattern, as discussed in the rejection for Claim 10.

However, Migdal and Heirich do not teach a repeating tile pattern. However, Duffy describes a repeating tile pattern (Col. 4, lines 26-53; Col. 5, lines 17-20), as discussed in the rejection for Claim 1.

21. With regard to Claim 15, Claim 15 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

22. With regard to Claim 16, Claim 16 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

23. With regard to Claim 17, Claim 17 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

24. With regard to Claim 18, Migdal does not teach a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines. However, Heirich describes a bridge (20, Figure 1) operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines (22) (Col. 5, lines 45-50).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Migdal to include a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines as suggested by Heirich because Heirich suggests the advantage of being able to distribute all of the vertex data at once (Col. 5, lines 53-58). The advantages of having multiple graphics pipelines were discussed in the rejection for Claim 1.

25. With regard to Claim 20, Migdal describes a graphics processing method, comprising receiving vertex data for a primitive to be rendered; generating pixel data in response to the vertex data (Col. 4, lines 46-51); determining the pixels within a set of tiles to be processed by a the graphics pipeline in response to the pixel data; and performing pixel operations on the pixels within the determined set of tiles by the graphics pipeline (Col. 8, lines 6-23).

However, Migdal does not teach a repeating tile pattern including a horizontally and vertically repeating pattern of square regions. However, Duffy describes a repeating tile pattern including a horizontally and vertically repeating pattern of square regions (Col. 4, lines 26-53; Col. 5, lines 17-20) as discussed in the rejection for Claim 1.

However, Migdal and Duffy do not teach two graphics pipelines. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33), as discussed in the rejection for Claim 1.

26. With regard to Claim 21, Migdal does not teach that determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1), and each graphics pipeline processes only a part of an image (PI, Col. 6, lines 1-6), as discussed in the rejection for Claim 10. Therefore, Heirich inherently teaches determining the pixels within a set of tiles to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

However, Migdal and Heirich do not teach a repeating tile pattern. However, Duffy describes a repeating tile pattern (Col. 4, lines 26-53; Col. 5, lines 17-20), as discussed in the rejection for Claim 1.

27. With regard to Claim 22, Migdal describes determining the pixels within a set of tiles to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the graphics pipeline (Col. 8, lines 17-23).

However, Migdal does not teach a repeating tile pattern. However, Duffy describes a repeating tile pattern (Col. 4, lines 26-53; Col. 5, lines 17-20), as discussed in the rejection for Claim 1.

However, Migdal and Duffy do not teach two graphics pipelines. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33), as discussed in the rejection for Claim 1.

28. With regard to Claim 23, Migdal describes transmitting the processed pixels to memory (109, Figure 1; Col. 8, line 48-Col. 9, line 3).

29. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal (US006762763B1) in view of Heirich (US006753878B1), further in view of Duffy (US005179640A), further in view of Wang (US006184906B1).

Migdal, Heirich, and Duffy are relied upon for the teachings as discussed above relative to Claim 1.

However, Migdal, Heirich, and Duffy do not teach a memory controller coupled to the at least two graphics pipelines, operative to transfer pixel data between each of the first pipeline and the second pipeline and a memory. However, Wang describes a memory controller (28, Figure 2) coupled to the at least two graphics pipelines, operative to transfer pixel data between each of the first pipeline and the second pipeline and a memory (60) (Col. 3, lines 55-58).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Migdal, Heirich, and Duffy to include a memory controller coupled to the at least two graphics pipelines, operative to transfer pixel data between each of the first pipeline and the second pipeline and a memory as suggested by Wang because Wang

suggests the advantage of improving the speed of operation and allowing for a single memory clock cycle read/write operation (Col. 1, lines 51-55).

30. Claim 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal (US006762763B1) in view of Heirich (US006753878B1), further in view of Duffy (US005179640A), further in view of Kent (US 20030164830A1).

Migdal, Heirich, and Duffy are relied upon for the teachings as discussed above relative to Claim 17.

However, Migdal, Heirich, and Duffy do not teach that the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip [0010, 0012] and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one. However, Kent describes the data includes a polygon [0006] and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one [0129, 0144].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Migdal, Heirich, and Duffy so that the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and

wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one as suggested by Kent because Kent suggests the advantage of being able to determine if a polygon is within the super tiles associated with a separate chip [0129, 0144]. This is needed in order for each separate chip to only process the pixel data in one set of tiles, as discussed in the rejections for Claims 8 and 10.

31. Claim 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal (US006762763B1) in view of Duffy (US005179640A), further in view of Morgan (US006714203B1), further in view of Wang (US006184906B1).

Migdal describes a graphics processing circuit, comprising front end circuitry (105, Figure 1) operative to generate pixel data in response to primitive data for a primitive to be rendered (Col. 4, lines 46-51; Col. 5, lines 39-41; Col. 8, lines 17-19); first back end circuitry (108), coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates (Col. 8, lines 20-23); a first scan converter (602, Figure 6), coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles are to be processed by the first back end circuitry, and operative to provide the position coordinates of the first back end circuitry in response to the pixel data (Col. 8, lines 7-23).

However, Migdal does not teach a repeating tile pattern including a horizontally and vertically repeating pattern of square regions. However, Duffy describes a repeating tile pattern (Col. 4, lines 26-53; Col. 5, lines 17-20), as discussed in the rejection for Claim 1.

However, Migdal and Duffy do not teach a second back end circuitry. However, Morgan describes a front end circuitry (202, Figure 2) coupled to multiple back end circuitries (208, 210) (Col. 3, lines 41-42).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Migdal and Duffy to include a second back end circuitry as suggested by Morgan because Morgan suggests that it is simpler to have one front-end circuitry as a data communications interface for the image generation system (Col. 3, lines 32-34) and couple the one front-end circuitry to multiple back end circuitries. The multiple back-end circuitries are for multiple graphics pipelines. The advantages of having multiple graphics pipelines were discussed in the rejection for Claim 1.

However, Migdal, Duffy, and Morgan do not teach a memory controller, coupled to the first and second back end circuitry, operative to transmit and receive the processed pixel data. However, Wang describes a memory controller (28, Figure 2), coupled to multiple pipelines or the first and second back end circuitry, operative to transmit and receive the processed pixel data (Col. 3, lines 55-58), as discussed in the rejection for Claim 9.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 703-305-4418. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Notice of References Cited	Application/Control No. 10/459,797	Applicant(s)/Patent Under Reexamination LEATHER ET AL.	
	Examiner Joni Hsu	Art Unit 2676	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,762,763 B1	07-2004	Migdal et al.	345/506
	B	US-6,753,878 B1	06-2004	Heirich et al.	345/629
	C	US-5,179,640 A	01-1993	Duffy, Christopher J.	345/596
	D	US-6,184,906 B1	02-2001	Wang et al.	345/532
	E	US-2003/0164830 A1	09-2003	Kent, Osman	345/505
	F	US-6,714,203 B1	03-2004	Morgan et al.	345/506
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Amendments to the Specification:

Please replace paragraph [0046] with the following amended paragraph:

[0046] The bounding boxes' four corners are mapped to the tile pattern, simply by discarding the lower bits of X & Y. The four corners map to the same or different tiles. If they all map to the same tile, then only the pipeline that is associated with that tile receives the polygon. If it maps to only tiles that are associated with only one pipeline, then again only that pipeline receives the polygon. If it maps to tiles that are associated with multiple pipelines, then the entire polygon is sent to all pipelines. In [[our]]one implementation, ~~we broadcast~~ the polygon is broadcast to all pipelines, masking the pipelines that should not receive it. Consequently, polygons can be sent to only one pipe or up to all the pipes, depending on the coverage of the tiles by the polygon.

Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (original) A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile,

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines are on multiple chips.

9. (currently amended) The graphics processing circuit of claim 1, further including a memory controller coupled to the at least two graphics ~~pipeline~~pipelines, operative to transfer pixel data between each of [[the]]a first pipeline and [[the]]a second pipeline and a memory.

10. (original) The graphics processing circuit of claim 4, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first

set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (currently amended) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the [[pixel]] data only in a second set of tiles in the repeating tile pattern.

13. (currently amended) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to [[the]] front end circuitry and [[the]] back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip

and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (original) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; and

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (original) The graphics processing method of claim 20, further comprising transmitting the processed pixels to memory.

24. (currently amended) A graphics processing circuit, comprising:

front end circuitry operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles [[or]]of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller, coupled to the first and second back end circuitry. operative to receive transmit and receive the processed pixel data.

25. (new) A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles a repeating tile pattern, a respective one of the at least two graphics pipelines operative to process

data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions.

26. (new) The graphics processing circuit of claim 25 wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels.

REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 9 and 24 are objected to due to typographical errors. These errors have been corrected.

Claims 9, 12 and 13 stand rejected under 35 U.S.C. §112, 2nd paragraph, as being indefinite due to antecedent discrepancies caused by typographical errors. Applicants have corrected typographical errors and as such, this rejection is respectfully requested to be withdrawn.

Claims 1-8, 10-18, 20-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Migdal in view of Heirich further in view of Duffy. Applicants respectfully submit that the Migdal reference actually teaches away from a multi-graphics pipeline structure and as such, cannot render the claimed invention obvious. For example, the Migdal reference is directed to a computer system having a distributed texture memory architecture to overcome problems associated with parallel pipelined architectures. As specifically stated for example in column 2, lines 26-27, Migdal states that there are several disadvantages with using a parallel pipelined approach especially in the case when several pipelines perform parallel processing together in order to generate a single frames worth of data. (See specifically, column 2, lines 31-33). Since Applicants claim a multigraphics pipeline structure that processes data in sets of tiles in a frame, Migdal teaches away from the claimed circuit. Moreover, the office action also admits that Migdal does not teach that there are multiple graphics pipelines and wherein each graphics pipeline processes data in a dedicated tile. As noted, Migdal actually teaches away from Applicants' claimed invention. (See for example, columns 2 and 3 of Migdal). Since the Migdal reference teaches away from Applicants' claimed invention, the claims are in condition for

allowance and that the combination of the cited references with Migdal does not render the claims obvious.

In addition, the Duffy reference has been alleged to be properly combinable with Migdal and Heirich and is allegedly cited as describing a repeating tile pattern where the repeating tile patterns include a horizontally and vertically repeating pattern of square regions (office action citing column 3, lines 67 through column 4, line 4; column 4, lines 31-32; column 5, lines 17-20). However, Applicants respectfully submit that the cited portions of Duffy actually teach a completely different pattern than the repeating tile patterns that are processed by two graphics pipelines wherein the repeating tile pattern includes horizontally and vertically repeating patterns of regions as claimed. For example, the "repeating patterns" cited in the portions referenced in the office action of Duffy, are actually pixel "fill" patterns used for dithering. (See for example, column 3, lines 52-66). As such, the "repeating patterns" of tiles described in Duffy are actually patterned wallpaper or filled patterns that are when displayed allow a person's eye to blend neighboring pixels of differing visual patterns.

In contrast, the "tiles" and "repeating tile pattern" of the claimed invention deal with processing tiles that are used by graphics pipelines to process primitive data such as polygons to generate pixels that are ultimately displayed. Accordingly, although some of the wording is similar, the Duffy reference actually refers to a dithering halftone visual pattern of pixels whereas Applicants' claim is directed to tile processing using graphics pipelines. As such, upon further investigation of Duffy, it appears that the Duffy reference may have been misapprehended and actually teaches a different system from that described by Applicants and accordingly, the claims are in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter and are also allowable for at least depending upon allowable base claims.

As to claim 20, Applicants respectfully reassert the relevant remarks made above with respect to claim 1 and as such, this claim is also allowable.

Claim 9 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Migdal in view of Heirich further in view of Duffy and in view of Wang. Applicants respectfully reassert the relevant remarks made above with respect to the Migdal and Duffy reference and as such, this claim is also believed to be in condition for allowance.

Claim 19 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Migdal in view of Heirich further in view of Duffy and in view of Kent. Applicants respectfully reassert the relevant remarks made above with respect to the Migdal and Duffy reference and as such, this claim is also in condition for allowance. In addition, this claim adds additional novel and non-obvious subject matter and is also therefore allowable.

Claim 24 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Migdal in view of Duffy further in view of Morgan and in view of Wang. Applicants respectfully reassert the relevant remarks made above with respect to the Migdal and Duffy reference and as such, this claim is also believed to be in condition for allowance.

New claims 25 and 26 are also allowable for similar reasons stated above as the references in combination do not teach or suggest the graphic pipelines and non-square tile processing in horizontally and vertically repeating patterns as claimed.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 3-14-05

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 N. LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7599
FAX: (312) 609-5005

PTO/SB/17 (12-04v2)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 300.00

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Examiner Name	Joni Hsu
Art Unit	2676
Attorney Docket No.	00100.02.0053

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-0441 Deposit Account Name: ATI International SRL

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
26 - 24 or HP =	2	x 50	= 100

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
4 - 3 or HP =	1	x 200	= 200

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims — Fee ($): _____ Fee Paid ($): _____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____	/ 50 = _____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

Fees Paid ($)

Non-English Specification, $130 fee (no small entity discount) _____

Other (e.g., late filing surcharge): _____ _____

SUBMITTED BY

Signature	/Christopher J. Reckamp/	Registration No. (Attorney/Agent) 34,414	Telephone 312-609-7599
Name (Print/Type)	Christopher J. Reckamp		Date March 14, 2005

2676 TW

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2676
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [x] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):
  -return postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Vedder, Price, Kaufman & Kammholz, P.C.		
Signature			
Printed name	Christopher J. Reckamp		
Date	March 14, 2005	Reg. No.	34,414

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Christine A. Wright	Date	March 14, 2005

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Group: 2676
Docket No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate of First Class Mailing
I hereby certify that this paper is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

3-14-05 Christine A. Wright
Date *Christine A. Wright*

AMENDMENT AND RESPONSE

Dear Sir:

In response to the Office Action mailed December 14, 2004, Applicants submit the following Amendment and Response.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks begin on page 10 of this paper.

BEST AVAILABLE COPY

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10459797

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	72
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	822

* If the difference in column 1 is less than zero, enter "0" in column 2

3/7/05 **CLAIMS AS AMENDED - PART II**

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 26	Minus	** 24	= 2
Independent	* 4	Minus	*** 3	= 1
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18= 50	100
X42=		OR	X84= 200	200
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	300

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/459,797		2676	26M1

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 29153 on 07/20/2005

- Correspondence Address

The address of record for Customer Number 29153 is:
ATI TECHNOLOGIES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO,IL 60601

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/459,797		2676	26M1

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 29153 on 07/22/2005

- Correspondence Address

The address of record for Customer Number 29153 is:
ATI TECHNOLOGIES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO,IL 60601

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	307	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L2	256	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L3	272	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L4	37	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L5	81	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L6	448	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L7	68	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L8	712	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05

L9	335	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L10	557	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L16	1179	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:08
L17	933	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:08
L18	100	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:09
L19	73	til$3 and repeat$3 with (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:10
L24	212	scan adj conver$5 and pixel$1 and til$3 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:12
L27	277	(multiple plurality) same pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:14

L28	72	(multiple plurality) near2 pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:14
L29	68	(multiple plurality) near2 pipelin$3 and scan adj conver$5 and pixel$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:15
L30	79	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:15
L32	34	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:16

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/459,797	LEATHER ET AL.	
Examiner	**Art Unit**	
Joni Hsu	2671	

SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505	12/7/2004	JH
Above	UPDATED	7/26/2005	JH
345	588, 544	7/26/2005	JH
345	545, 532	7/26/2005	JH
345	501, 502	7/26/2005	JH
345	531	7/26/2005	JH

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached search history.	7/26/2005	JH

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/459,797	LEATHER ET AL.
Examiner	**Art Unit**
Joni Hsu	2671

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	7/22/05
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Claim		Date
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Claim		Date
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Bib Data Sheet

CONFIRMATION NO. 4148

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/459,797	06/12/2003 RULE	345	2676	00100.02.0053

APPLICANTS

Mark M. Leather, Saratoga, CA;

Eric Demers, Palo Alto, CA;

** CONTINUING DATA **********

This appln claims benefit of 60/429,641 11/27/2002

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 08/07/2003

Foreign Priority claimed	35 USC 119 (a-d) conditions met	Verified and Acknowledged	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☑ no	☐ yes ☑ no ☐ Met after Allowance	Examiner's Signature / Initials	CA	5	24	3

ADDRESS
29153
ATI TECHNOLOGIES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO , IL
60601

TITLE
Dividing work among multiple graphics pipelines using a super-tiling technique

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time)

1122		☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 08/01/2005

ATI TECHNOLOGIES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18, 20-26* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. In light of Applicant's amendments to Claim 9, the objection to this claim has been withdrawn.

2. In light of Applicant's amendments to Claims 9, 12, and 13, the rejections of these claims under 35 U.S.C. 112, 2nd paragraph have been withdrawn.

3. Applicant's arguments, see page 12, filed March 14, 2005, with respect to Claim 19 have been fully considered and are persuasive. The rejection under 35 U.S.C. 103(a) of Claim 19 has been withdrawn.

4. With regard to Claim 19, Applicant argues that this claim adds additional novel and non-obvious subject matter and is also therefore allowable (page 12).

In reply, the Examiner agrees. The rejection under 35 U.S.C. 103(a) of Claim 19 has been withdrawn.

5. Applicant's arguments with respect to claims 1-18 and 20-24 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's arguments, see pages 10-12, filed March 14, 2005, with respect to the rejection(s) of claim(s) 1-18 and 20-24 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Alcorn (US005745118A).

7. With regard to Claim 1, Applicant argues that the Migdal reference (US006762763B1) actually teaches away from a multi-graphics pipeline structure and as such, cannot render the claimed invention obvious (pages 10-11). Applicant also argues that the "repeating patterns" of tiles described in Duffy (US005179640A) are actually patterned wallpaper or filled patterns that are when displayed allow a person's eye to blend neighboring pixels of differing visual patterns. In contrast, the "tiles" and "repeating tile pattern" of the claimed invention deal with processing tiles that are used by graphics pipelines to process primitive data such as polygons to generate pixels that are ultimately displayed (page 11).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Alcorn. Alcorn describes a graphics processing circuit (Col. 3, lines 58-60), comprising at least two graphics pipelines (*front end board 10, texture mapping board 12 and frame buffer board 14 each is pipelined and operates on multiple primitives simultaneously*, Col. 6, lines 33-35; *front end board 10 includes three 3-D geometry accelerator chips 32A, 32B and 32C, a 2-D geometry accelerator chip 34*, Col. 6, lines 40-43) operative to process data in a corresponding set of tiles (tiler, Col. 11, lines 8-31). Alcorn describes mapping a texture to an object in a repeating fashion, such that the texture is mapped to multiple portions of the object (Col. 11, lines 35-37). Alcorn describes having a wrapping feature for coordinates falling outside the boundary of the

texture map, and pixels having S,T coordinates [10, 10] through (20, 20) would respectively map to the texels at S,T coordinates [0, 0] through (10, 10) (Col. 11, lines 46-50). According to the disclosure of this application, a repeating tile pattern means that the pixel data is repeated [0022], and the pixel data includes appearance attributes such as texture [0003]. Therefore, Alcorn describes that the tiles have a repeating tile pattern, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile (*tiler processes data within the texture map*, Col. 11, lines 8-31; *for example, texture is defined have S,T coordinates ranging from [0, 0] through (10, 10)*, Col. 11, lines 37-39). Alcorn discloses that the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Col. 15, lines 44-57), as shown in Figure 6.

8. With regard to Claims 2-18 and 20-24, Applicant argues that these claims should be allowed for the same reasons given above (pages 11-12).

In reply, the Examiner disagrees for the same reasons given above.

9. With regard to Claims 25 and 26, Applicant argues that the references in combination do not teach or suggest the graphic pipelines and non-square tile processing in horizontally and vertically repeating patterns as claimed (page 12).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Alcorn, as discussed above. According to the disclosure of this application, the NxM format for the tile sizes are 8x8, 16x16, or 32x32 [0043], so the invention deals with square tile processing. Alcorn discloses that the repeating tile pattern includes a horizontally and vertically repeating

pattern of square regions (Col. 15, lines 44-57), as shown in Figure 6, and the horizontally and vertically repeating pattern of regions include NxM (4x4) number of texels (Col. 15, lines 44-57). In one example, Alcorn describes that one pixel maps to four texels (Col. 15, lines 55-57). Since the pixels map to the texels, the repeating pattern of regions of the pixels would still be in NxM format.

Claim Objections

10. Claim 24 is objected to because of the following informalities: Claim 24 recites "a memory controller, coupled to the first and second back end circuitry, operative to *receive* transmit and receive the processed pixel data" where it should recite "a memory controller, coupled to the first and second back end circuitry, operative to transmit and receive the processed pixel data." Appropriate correction is required.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-4, 6-8, 9, 10, 12, 14, 17, 18, 20-23, 25, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Alcorn (US005745118A).

13. With regard to Claim 1, Alcorn describes a graphics processing circuit (Col. 3, lines 58-60), comprising at least two graphics pipelines (*front end board 10, texture mapping board 12 and frame buffer board 14 each is pipelined and operates on multiple primitives simultaneously*, Col. 6, lines 33-35; *front end board 10 includes three 3-D geometry accelerator chips 32A, 32B and 32C, a 2-D geometry accelerator chip 34*, Col. 6, lines 40-43) operative to process data in a corresponding set of tiles (tiler, Col. 11, lines 8-31). Alcorn describes mapping a texture to an object in a repeating fashion, such that the texture is mapped to multiple portions of the object (Col. 11, lines 35-37). Alcorn describes having a wrapping feature for coordinates falling outside the boundary of the texture map, and pixels having S,T coordinates [10, 10] through (20, 20) would respectively map to the texels at S,T coordinates [0, 0] through (10, 10) (Col. 11, lines 46-50). According to the disclosure of this application, a repeating tile pattern means that the pixel data is repeated [0022], and the pixel data includes appearance attributes such as texture [0003]. Therefore, Alcorn describes that the tiles have a repeating tile pattern, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile (*tiler processes data within the texture map*, Col. 11, lines 8-31; *for example, texture is defined have S,T coordinates ranging from [0, 0] through (10, 10)*, Col. 11, lines 37-39). Alcorn discloses that the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Col. 15, lines 44-57), as shown in Figure 6.

14. With regard to Claim 2, Alcorn describes that the square regions comprise a two dimensional partitioning of memory (*blocks of texture data are organized to take advantage of*

the four interleave implementation of the cache memory, Col. 15, lines 43-57, *S,T texture map coordinates*, Col. 10, lines 1-9).

15. With regard to Claim 3, Alcorn describes that the texture map partitions are provided to the frame buffer (Col. 14, lines 51-63), and therefore the memory is a frame buffer.

16. With regard to Claim 4, Alcorn describes that each of the at least two graphics pipelines (Col. 6, lines 33-35, 40-43) further includes front end circuitry (32A, 32B, 32C, Figure 2) are operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered (*distributes 3-D primitive data evenly among the 3-D geometry accelerator chips*, Col. 6, lines 43-47; *each 3-D geometry accelerator chip processes primitive data*, Col. 6, lines 56-62; *rendering hardware interpolates the primitive data to compute the display screen pixels that are turned on to represent each primitive*, Col. 1, lines 31-33; *vertex data*, Col. 7, lines 22-33), and back end circuitry (12), coupled to the front end circuitry (Col. 7, lines 5-10), operative to receive and process a portion of the pixel data (Col. 12, lines 13-20).

17. With regard to Claim 6, Alcorn describes that each texture map can comprise of texel arrays of either 4x4 (Col. 2, lines 38-41), 16x16 or 64x64 texels (Col. 2, lines 65-66). The pixel maps are in one-to-one correspondence with a single texel in the texture map (Col. 2, lines 62-64). The tiler partitions the memory into texture maps (Col. 11, lines 8-31), so each tile contains a texture map. Therefore, Alcorn discloses that each tile of the set of tiles further comprises a 16x16 pixel array.

18. With regard to Claim 7, Alcorn describes that the at least two graphics pipelines (Col. 6, lines 33-35, 40-43) separately receive the pixel data from the front end circuitry (32A, 32B, 32C, Figure 2) (*distributes 3-D primitive data evenly among the 3-D geometry accelerator chips*, Col. 6, lines 43-47; *each 3-D geometry accelerator chip processes primitive data*, Col. 6, lines 56-62; *rendering hardware interpolates the primitive data to compute the display screen pixels that are turned on to represent each primitive*, Col. 1, lines 31-33; *texture mapping board receives data from the separate 3-D geometry accelerator chips*, Col. 7, lines 5-10).

19. With regard to Claim 8, Alcorn describes that the at least two graphics pipelines are on multiple chips (Col. 6, lines 33-35, *3-D geometry accelerator chips*, Col. 6, lines 40-43).

20. With regard to Claim 9, Alcorn describes a memory controller (50, Figure 2) coupled to the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory (51) (Col. 6, lines 33-35, 40-43; Col. 8, lines 27-40).

21. With regard to Claim 10, Alcorn describes processing pixel data in a corresponding set of tiles (tiler, Col. 11, lines 8-31). Alcorn describes mapping a texture to an object in a repeating fashion, such that the texture is mapped to multiple portions of the object (Col. 11, lines 35-37). Alcorn describes having a wrapping feature for coordinates falling outside the boundary of the texture map, and pixels having S,T coordinates [10, 10] through (20, 20) would respectively map

to the texels at S,T coordinates [0, 0] through (10, 10) (Col. 11, lines 46-50). Therefore, since the tiles are repeated, only a first set of tiles are processed, and then those tiles are repeated. Therefore, Alcorn discloses that a first of the at least two graphics pipelines (Col. 6, lines 33-35, 40-43) processes the pixel data only in a first set of tiles in the repeating tile pattern.

22. With regard to Claim 12, Claim 12 is similar in scope to Claim 10, and therefore is rejected under the same rationale.

23. With regard to Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Alcorn gives an example of three graphics pipelines (Col. 6, lines 33-35, 40-43), however, Alcorn describes that the number of graphics pipeline can be modified (Col. 5, line 65-Col. 6, line 3). Therefore, Claim 14 is rejected under the same rationale as Claims 4 and 10.

24. With regard to Claim 17, Claim 17 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

25. With regard to Claim 18, Alcorn describes a bridge (30, Figure 2) operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines (Col. 6, lines 32-35, 40-47; Col. 7, lines 28-33; Col. 5, line 65-Col. 6, line 3).

26. With regard to Claim 20, Alcorn describes a graphics processing method (Col. 3, lines 58-60), comprising receiving vertex data for a primitive to be rendered; generating pixel data in response to the vertex data (Col. 7, lines 21-33); determining the pixels within a set of tiles (tiler, Col. 11, lines 8-31) of a repeating tile pattern to be processed by a corresponding one of at least two graphics pipelines (Col. 6, lines 33-35, 40-43) in response to the pixel data (Col. 11, lines 35-50). Alcorn discloses that the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Col. 15, lines 44-57), as shown in Figure 6. Alcorn describes performing pixel operations on the pixels within the determined set of tiles (Col. 12, lines 13-20) by the corresponding one of the at least two graphics pipelines (Col. 6, lines 33-35, 40-43).

27. With regard to Claim 21, Alcorn describes that determining the pixels within a set of tiles of the repeating tile pattern to be processed, as discussed in the rejection for Claim 20, and the set of tiles to be processed is inherently the set of tiles that the corresponding graphics pipeline is responsible for.

28. With regard to Claim 22, Alcorn describes that determining the pixels within a set of tiles of the repeating tile pattern (Col. 11, lines 35-50) to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines (Col. 10, lines 1-8; *texel data output from the parameter interpolator circuit 64 is provided to the tiler 72, which determines the address of the four texels...checks to determine whether each is within the boundary of the*

texture... texel data includes the interpolated S, T coordinates as well as the map number, Col. 11, lines 8-31; Col. 6, lines 33-35, 40-43).

29. With regard to Claim 23, Alcorn describes transmitting the processed pixels to memory (Col. 6, lines 14-20).

30. With regard to Claim 25, Claim 25 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

31. With regard to Claim 26, Alcorn discloses that the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Col. 15, lines 44-57), as shown in Figure 6, and the horizontally and vertically repeating pattern of regions include NxM (4x4) number of texels (Col. 15, lines 44-57). According to the disclosure of this application, the NxM format for the tile sizes are 8x8, 16x16, or 32x32 [0043], and therefore 4x4 fits this format. In one example, Alcorn describes that one pixel maps to four texels (Col. 15, lines 55-57). Since the pixels map to the texels, the repeating pattern of regions of the pixels would still be in NxM format.

32. Thus, it reasonably appears that Alcorn describes or discloses every element of Claims 1-4, 6-8, 9, 10, 12, 14, 17, 18, 20-23, 25, and 26 and therefore anticipates the claims subject.