DETAILED ACTION

Information Disclosure Statement

1. Information disclosure statement (IDS) submitted on November 28, 2007 was filed after mailing date of application on June 12, 2003. Submission is in compliance with provisions of 37 CFR 1.97. Accordingly, information disclosure statement is being considered by the examiner.

Response to Arguments

2. Applicant's arguments, see pages 9-11, filed November 28, 2007, with respect to the rejection(s) of claim(s) 1-4, 7, 10, 12, 14, 20-22, and 25 under 35 U.S.C. 102(e) and claims 5, 6, 11, 13, 15-19, and 24 under 35 U.S.C. 103(a) have been fully considered and are persuasive. So, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Furtner (US006778177B1) and MacInnis (US006570579B1).

3. Applicant argues Perego (US006864896B2) does not teach multi-graphics pipeline circuitry on same chip nor memory controller on the same chip but instead teaches discrete memory modules having separate and single graphics engines thereon. The memory controller taught in Perego is not on a same chip nor is it part of the memory module (page 10).

In reply, new grounds of rejection are made in view of Furtner and MacInnis.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-4, 6, 7, 10, 12, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1), further in view of MacInnis (US006570579B1).

6. As per Claim 1, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63) having at least 2 graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two graphics pipelines operative to process data in dedicated tile (c. 5, ll. 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines (312), operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories (314) (c. 3, ll. 65-67; c. 4, ll. 1-10, 48-65). Shared memories (314) are each part of main memory (c. 1, ll. 44-54; c. 3, ll. 3-6), and so are considered to be one memory. Repeating tile pattern includes horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (c. 5, ll. 19-27, 38-44).

However, Perego does not teach that the graphics pipelines are on a same chip. However, Furtner teaches that the graphics pipelines are on a same chip (c. 6, ll. 30-32).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Perego so graphics pipelines are on same chip as suggested by Furtner. Placing plurality of modules on single chip takes up less space as compared to using multiple chips, and this is well-known in the art.

However, Perego and Furtner do not teach memory controller is also on the same chip. However, MacInnis teaches memory controller (54) is on same chip (10) as graphics pipeline (58), as shown in Fig. 2 (c. 4, ll. 65-67; c. 5, ll. 36-41; c. 6, ll. 10-13). This would be obvious for same reasons given above.

7. As per Claim 2, Perego teaches square regions have two dimensional partitioning of memory (c. 5, ll. 19-33).

8. As per Claim 3, Perego discloses that the memory is a frame buffer (c. 5, ll. 32-33).

9. As per Claim 4, Perego teaches each of at least two graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process portion of pixel data (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44). In order for front end circuitry (308) to generate pixel data, it must inherently receive vertex data.

10. As per Claim 6, Perego does not explicitly teach each tile of set of tiles has 16x16 pixel array. But, Furtner teaches each tile of set of tiles has 16x16 pixel array (c. 11, ll. 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so each tile of set of tiles further has 16x16 pixel array because Furtner suggests depending on number of parallel image-rendering pipelines and depending on memory organization, optimum tile size and shape can be selected (c. 11, ll. 45-48, 64-65), and

so it would be obvious to modify tile size to be 16x16 pixels if that would be optimum tile size for particular number of parallel image-rendering pipelines and particular memory organization.

11. As per Claim 7, Perego teaches the at least two graphics pipelines (312, Fig. 3) separately receive the pixel data from the front end circuitry (308) (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44).

12. As per Claim 10, Perego teaches first of at least two graphics pipelines (first rendering engine of 312, Fig. 3) processes pixel data only in first set of tiles (tiles labeled "RE0" in Fig. 5) in repeating tile pattern (c. 5, ll. 23-44).

13. As per Claim 12, Perego teaches second of at least two graphics pipelines (second rendering engine of 312, Fig. 3) processes pixel data only in second set of tiles (tiles labeled "RE1" in Fig. 5) in repeating tile pattern (c. 5, ll. 23-44).

14. As per Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Perego teaches four graphics pipelines (c. 5, ll. 41-44). So Claim 14 is rejected under the same rationale as Claims 4 and 10.

15. As per Claim 17, Perego does not teach 3rd and 4th graphics pipelines are on separate chips. However, Furtner teaches 3rd and 4th pipelines are on separate chips (c. 6, ll. 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so pipelines are on separate chips because Furtner teaches this makes system more configurable by being able to easily add more graphics pipelines to increase performance (c. 6, ll. 29-30, 42-51).

16. Claims 5, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kelleher (US005794016A).

17. As per Claim 5, Perego, Furtner, and MacInnis are relied upon for teachings for Claim 4.

But, Perego, Furtner, and MacInnis do not explicitly teach at each of at least two graphics pipelines further includes scan converter, coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry. But, Kelleher teaches each of at least two graphics pipelines (20A, 20B, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) further includes scan converter (update stage, Fig. 7), coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry (c. 8, ll. 52-61; c. 9, ll. 1-23; c. 6, ll. 26-28).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Perego, Furtner, and MacInnis so at each of at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry because Kelleher suggests scan converters are needed in order to define image data as array of pixels by calculating pixel addresses (c. 9, ll. 1-23), as is well-known in the art.

18. As per Claim 18, Perego does not teach a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines. However, Kelleher discloses a bridge (38, Fig. 3) operative to transmit vertex data to each of the first (20A), second (20B), third (20C) and fourth (20N) graphics pipelines (c. 3, ll. 22-23; c. 4, ll. 9-14; c. 8, ll. 56-65; c. 3, ll. 46-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego to include a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines as suggested by Kelleher because Kelleher suggests the advantage of being able to convert the vertex data to pixel data in parallel, which increases the efficiency of the graphics system (c. 2, ll. 31-35; c. 8, ll. 56-65; c. 9, ll. 1-23).

19. As per Claim 24, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63), having front end circuitry (308) operative to generate pixel data in response to primitive data for primitive to be rendered (c. 5, ll. 19-23); first back end circuitry (first rendering engine 312), coupled to front end circuitry 308, operative to process first portion of pixel data (labeled "RE0" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by first back end circuitry, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; second back end circuitry (second rendering engine 312), coupled to front end circuitry 308, operative to process second portion of pixel data (labeled "RE1" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by second back end circuitry (c. 3, ll. 63-c. 4, ll. 2; c. 5, ll. 19-44); and memory controller (310), coupled to first and second back end circuitry (312) operative to transmit and receive processed pixel data (c. 3, ll. 65-67; c. 4, ll. 1-53; c. 5, ll. 32-44).

However, Perego does not explicitly teach first scan converter and second scan converter. However, Kelleher teaches first scan converter, coupled between front end circuitry (14, Fig. 3) and first back end circuitry (update stage, Fig. 7 in 20A, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by first back end circuitry (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23), and operative to provide position coordinates to first back end circuitry in response to pixel data (c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38); second scan converter, coupled between front end circuitry and second back end circuitry (update stage, Fig. 7 in 20B, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by second back end circuitry, and operative to provide position coordinates to second back end

circuitry in response to pixel data (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23; c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38). This would be obvious for same reasons given in the rejection for Claim 5.

However, Perego and Kelleher do not teach front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. However, Furtner teaches graphics pipelines are on same chip (c. 6, ll. 30-32). Front end circuitry, first back end circuitry, and first scan converter of Perego-Kelleher combination make up one graphics pipeline, and front end circuitry, second back end circuitry, and second scan converter of Perego-Kelleher combination make up another graphics pipeline, as discussed above. Since Furtner teaches graphics pipelines are on same chip, this teaching from Furtner can be applied to Perego-Kelleher combination so front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. This would be obvious for reasons for Claim 1.

However, Perego, Kelleher, and Furtner do not teach memory controller is also on the same chip. However, MacInnis teaches this limitation, as discussed in the rejection for Claim 1.

20. Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kelleher (US005794016A), further in view of Hamburg (US005905506A).

Perego, Furtner, and MacInnis are relied upon for teachings relative to Claim 10.

However, Perego, Furtner, and MacInnis do not explicitly teach scan converter. However, Kelleher teaches first of the at least two graphics pipelines (20A, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) further includes scan converter (84, Fig. 7), coupled to front end circuitry (80, 82) and back end circuitry (c. 8, ll. 52-c. 9, ll. 23). Scan converter determines which groups of blocks

52 within graphics memory 22 are allocated to and controlled by graphics pipelines (c. 8, ll. 52-65; c. 6, ll. 26-28). Graphics memory is partitioned into plurality of pixel blocks that are tiled in x-and y-direction of graphics memory (c. 4, ll. 60-62). So, scan converter is inherently operative to provide memory addresses or position coordinates of pixels within first set of tiles to be processed by back end circuitry. This would be obvious for reasons for Claim 5.

But, Perego, Furtner, MacInnis, Kelleher do not explicitly teach using tile identification data to indicate which tiles are to be processed. But, Hamburg teaches pixel identification line for receiving tile identification data indicating which tiles are to be processed (c. 5, ll. 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Perego, Furtner, MacInnis, and Kelleher to include using tile identification data to indicate which tiles are to be processed because Hamburg suggests advantage of using tile identification data to easily track storage locations of tile pixel data and being able to easily retrieve data for particular image tile (c. 1, ll. 46-54).

21. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kent (US 20030164830A1).

Perego, Furtner, and MacInnis are relied on for teachings for Claim 17. Perego teaches data includes polygon (c. 5, ll. 19-23). Furtner teaches third and fourth graphics pipelines are on separate chips (c. 6, ll. 47-51), as discussed for Claim 17.

But, Perego, Furtner, and MacInnis do not teach creating bounding box around polygon and each corner of bounding box is checked against super tile that belongs to each separate chip and if bounding box does not overlap any of super tiles associated with separate chip, then

processing circuit rejects whole polygon and processes next one. But, Kent teaches graphics pipeline [0006] calculates bounding box of primitive and testing this against VisRect. If bounding box of primitive is contained in other P10's super tile the primitive is discarded at this stage [0129]. Primitive can be polygon [0088]. Method used is to calculate distance from each subpixel sample point in point's bounding box to point's center and compare this to point's radius. Subpixel sample points with distance greater than radius do not contribute to pixel's coverage. Cost of this is kept low by only allowing small radius points hence distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within bounding box [0144]. Since method calculates distance from each subpixel sample point in point's bounding box, this must include all corners of bounding box. So, Kent teaches data includes polygon and graphics pipeline creates bounding box around polygon and wherein each corner of bounding box is checked against super tile that belongs to graphics pipeline and if bounding box does not overlap any of super tiles, then processing circuit rejects whole polygon and processes next one.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego, Furtner, and MacInnis to include bounding box as because Kent suggests processing super tiles one at a time in order to hide page break costs [0129, 0051].

22. Claims 20-22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1).

23. As per Claim 20, Perego teaches graphics processing method, comprising generating pixel data (c. 5, ll. 19-25), which is inherently generated in response to received vertex data; determining pixels within set of tiles of repeating tile pattern corresponding to screen locations to be processed by corresponding one of at least two graphics pipelines (312, Fig. 3) in response to

pixel data, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; performing pixel operations on pixels within determined set of tiles by corresponding one of at least two graphics pipelines (c. 5, ll. 19-44); and transmitting processed pixels to memory controller (310), wherein at least two graphics pipelines share memory controller (c. 3, ll. 65-c. 4, ll. 25; c. 5, ll. 31-44).

However, Perego does not teach that the graphics pipelines are on a same chip. However, Furtner teaches graphics pipelines are on a same chip (c. 6, ll. 30-32), as discussed for Claim 1.

24. As per Claim 21, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed further comprises determining set of tiles that corresponding graphics pipeline is responsible for (c. 5, ll. 19-50).

25. As per Claim 22, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed comprises providing position coordinates of pixels within determined set of tiles to be processed to corresponding one of at least two graphics pipelines (c. 5, ll. 19-44).

26. As per Claim 25, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63) having at least two graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two graphics pipelines operative to process data in a dedicated tile (c. 5, ll. 19-27, 38-44), wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (c. 5, ll. 19-27, 38-44).

However, Perego does not teach that the graphics pipelines are on a same chip. However, Furtner teaches graphics pipelines are on a same chip (c. 6, ll. 30-32), as discussed for Claim 1.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP §.706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

KEE M. TUNG
SUPERVISORY PATENT EXAMINER

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/07/2007								
	1	✓								
	2	✓								
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	26	-								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
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SEARCHED

Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545, 532, 501, 502, 531	8/9/07	JH
Above	UPDATED	12/7/07	JH
345	519	12/7/07	JH

SEARCH NOTES

Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) -- See attached search history.	12/7/07	JH

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

PTO/SB/08A (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/J.H./		US- 6,980,209 B1	12-27-2005	Donham et al.	
/J.H./		US- 5,550,962	08-27-1996	Nakamura et al.	
/J.H./		US- 5,818,469	10-06-1998	Lawless et al.	
/J.H./		US- 6,118,452	09-12-200	Gannett	
/J.H./		US- 6,353,439 B1	03-05-2002	Lindholm et al.	
/J.H./		US- 6,384,824 B1	05-07-2002	Morgan et al.	
/J.H./		US- 6,417,858 B1	07-09-2002	Bosch et al.	
/J.H./		US- 6,573,893 B1	06-03-2003	Naqvi et al.	
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/J.H./		US- 6,650,330 B2	11-18-2003	Lindholm et al.	
/J.H./		US- 6,724,394 B1	04-20-2004	Zatz et al.	
/J.H./		US- 6,731,289 B1	05-04-2004	Peercy et al.	
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/J.H./		US- 2003/0076320 A1	04-24-2003	Collodi	
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/J.H./		US- 2004/0041814 A1	03-04-2004	Wyatt et al.	

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Examiner Signature	/Joni Hsu/	Date Considered	12/13/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

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Sheet 2 of 3

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/J.H./		US- 6,222,550 B1	04-2001	Rosman et al.	
/J.H./		US- 6,557,083 B1	04-2003	Sperber et al.	
/J.H./		US- 6,219,062 B1	04-2001	Matsuo et al.	
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/J.H./		US- 6,344,852	02-05-2002	Zhu et al.	
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/J.H./		US- 6,636,232	10-21-2003	Larson	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Joni Hsu/	Date Considered	12/13/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08B (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 3 of 3

	Complete if Known
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/J.H./		BRETERNITZ, JR., MAURICIO et al.; Compilation, Architectural Support, and Evaluation of SIMD Graphics Pipeline Programs on a General-Purpose CPU; IEEE; 2003; pages 1-11.	
/J.H./		International Search Report for PCT Patent Application PCT/IB2004/003821 dated March 22, 2005.	

Examiner Signature	/Joni Hsu/	Date Considered	12/13/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Notice of References Cited	Application/Control No. 10/459,797	Applicant(s)/Patent Under Reexamination LEATHER ET AL.	
	Examiner Joni Hsu	Art Unit 2628	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,570,579	05-2003	MacInnis et al.	345/629
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PTO/SB/30 (04-05)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

      ii. ☐ Other _____

   b. ☑ Enclosed

      i. ☑ Amendment/Reply

      ii. ☐ Affidavit(s)/ Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☑ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 22-0259. I have enclosed a duplicate copy of this sheet.

      i. ☑ RCE fee required under 37 CFR 1.17(e)

      ii. ☑ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☐ Other _____

   b. ☐ Check in the amount of $ _____ enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	/Christopher J. Reckamp/	Date	July 3, 2008
Name (Print/Type)	Christopher J. Reckamp	Registration No.	34,414

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being forwarded via electronic submission to: Electronic Business Center, Commissioner for Patents, Mail Stop RCE, on the date shown below.

Signature	/Christine A. Wright/		
Name (Print/Type)	Christine A. Wright	Date	July 3, 2008

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 1-4, 6, 7, 10, 12, 14 and 17 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner, further in view of U.S. Patent No. 6,570,579 (MacInnis). Applicants wish to thank the Examiner for reconsideration in view of the prior remarks. As a result, this is a new ground of rejection. Applicants respectfully traverse however based on the actual teachings of the references since the alleged combination would actually result in the inoperability of the primary Perego reference. Combining teachings that render the operation of a reference inoperable is not a prima facia case of obviousness. As such, Applicants respectfully submit that the claims are in condition for allowance.

For example, Perego requires multiple discrete memory modules each with its own rendering engine and each with its own memory and shared main memory. Perego teaches an opposite approach from that claimed by Applicants. Perego requires interconnecting modules that can allow variable scalability in addition to requiring shared memory controllers. In addition, a separate memory controller is described as being a part of a different and separate memory controller subsystem/CPU 302 that is coupled "to four distinct memory modules 304". (See column 4, lines 26-36). Perego further describes that the memory controller/graphics controller is responsible for distributing particular processing tasks to the different rendering engines on different discrete memory modules.

It is alleged however that placing a plurality of modules on a single chip is taught in Furtner, and modifying Perego accordingly would be proper. However, Perego requires multiple discrete memory modules each with its own rendering engine and each with its own memory. Placing rendering engines 312 onto a single chip would require redesign of the memory graphics controller and CPU memory subsystem as well as each individual module of Perego. Applicants

respectfully submit that the alleged motivation, namely that placing a plurality of modules on a single chip takes up less space is not applicable in this instance as to Perego since it would render the Perego system inoperable for its intended purpose since Perego teaches a scalable module system and unified memory architecture with a memory controller coupled to multiple modules (see Abstract). Perego teaches an opposite approach from that claimed by Applicants where interconnecting modules can allow variable scalability in addition to requiring shared memory controllers. As such, the motivation does not appear to be applicable to the teachings of Perego. In fact, modifying Perego as suggested would render Perego inoperable for its intended purpose. For these reasons alone, the claims are in condition for allowance.

Moreover, not only does Furtner fail to teach the claimed subject matter, but the office action also attempts to combine the teachings of MacInnis as a further level of consolidation. However, Applicants respectfully submit that again the teachings of the references cannot be ignored. As noted above, the combination of Perego, MacInnis and Furtner would change the operation of Perego to the point where it would be inoperable for its intended purpose. As such, further combination would further render the Perego operation unusable for its intended purposes. Accordingly, Applicants respectfully request reconsideration and respectfully submit that the claims are in condition for allowance.

Applicants respectfully reassert the relevant remarks made above with respect to the independent claims and as such, the independent claims are in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter. For example, as to claim 4, the claim requires that each of the two graphics pipelines on a same chip include front end circuitry that receives vertex data and generates pixel data corresponding to a primitive to be rendered. The office action cites the CPU 308 as being the front end circuitry in

Perego. However as claimed, the multiple graphics pipelines on the same chip include the front end circuitry, and not a separate CPU that passes information through a graphics controller as taught in Perego. Accordingly, Applicants respectfully submit that this claim is also in condition for allowance. The other dependent claims add additional novel and non-obvious subject matter.

Claims 5, 18, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perego in view of Kelleher. Claim 24 requires front end circuitry on a chip and first and second backend circuitry on the chip. The first and second backend circuitry processes different portions of the pixel data in response to position coordinates. A memory controller on the same chip is also coupled to the first and second backend circuitry. In this example, common front end circuitry is used on a chip for multiple backend operations. Again, the Perego reference illustrates a completely different structure and does not describe multiple backend circuitry on a common chip nor common front end circuitry and memory controller on a common chip as claimed. As such, the claim is also in condition for allowance. Also, these claims add additional novel and non-obvious subject matter.

Claims 11, 13, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego, Furtner, and MacInnis in view of Kelleher, further in view of Hamburg. A fourth reference has been added in an attempt to render these claims obvious. Applicants respectfully reassert the remarks made above with respect to the Perego, Further and MacInnis references and as such, these claims are also believed to be in condition for allowance.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego, Furtner, and MacInnis in view of Kent. Applicants respectfully reassert the relevant remarks made above and as such, this claim is also in condition for allowance.

Claims 20-22 and 25 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner. Applicants respectfully reassert the remarks made above with respect to Perego and Furtner and as such, these claims are also in condition for allowance.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: July 3, 2008

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Registration No. 34,414

Vedder Price P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005

Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A graphics processing circuit, comprising:

at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; and

a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory;

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (canceled)

9. (canceled)

10. (currently amended) The graphics processing circuit of claim [[4]]7, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (previously presented) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. (previously presented) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for

receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (previously presented) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of at least two graphics pipelines on a same chip in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions;

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines; and

transmitting the processed pixels to a memory controller, wherein the at least two graphics pipelines share the memory controller.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (canceled)

24. (previously presented) A graphics processing circuit, comprising:

front end circuitry on a chip operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry on the chip, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter on the chip, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry on the chip, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter on the chip, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller on the chip, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data.

25. (previously presented) A graphics processing circuit, comprising:

at least two graphics pipelines on a chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions;

wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels.

26. (canceled)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2628
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Sir:

In response to the Final Office Action mailed February 4, 2008, Applicants submit a Request for Continued Examination, petition for a two month extension of time and submit the following preliminary amendment.

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 8 of this paper.

Electronic Patent Application Fee Transmittal

Application Number:	10459797
Filing Date:	12-Jun-2003
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Filer:	Christopher J. Reckamp/Christine Wright
Attorney Docket Number:	00100.02.0053
Filed as Large Entity	

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 2 months with $0 paid	1252	1	460	460

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**1270**

Electronic Acknowledgement Receipt	
EFS ID:	3563474
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	03-JUL-2008
Filing Date:	12-JUN-2003
Time Stamp:	11:52:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1270
RAM confirmation Number	8524
Deposit Account	220259
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	10459797_RCE.pdf	80172 5fa39899ec6684b5c885ed7d753b7cc18a6fa8f3	no	1
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2		10459797_PrelAmdt.pdf	112437 c9c1d74a30b9a2bb32af8c2b140a319a720e7bd6	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	11

Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8352 ae06602d6b443b30f386312664b07ec9366b716b	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	200961		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/459,797	06/12/2003	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	07/03/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/THERESA LINDSAY/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545, 532, 501, 502, 531, 519	12/7/07	JH
Above	UPDATED	7/29/08	JH

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) -- See attached search history.	7/29/08	JH

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	568	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L2	400	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L3	127	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L4	92	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L5	931	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L6	483	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19

L7	56	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L8	739	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L9	481	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L10	2085	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L11	1693	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L12	384	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L13	316	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19

L14	192	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal $2 and vertical $2 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L15	145	til$3 and repeat$3 with (til$3 pattern $3) same pixel $1 and pattern $3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L16	316	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L17	456	(multiple plurality) same pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L18	166	(multiple plurality) near2 pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L19	115	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19

L20	50	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L21	316	345/519.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L22	91	(multiple plural$3) adj2 graphic$1 adj (pipelin$3 process$3 engine$1) same (circuit chip)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L23	141	graphic$1 adj pipelin$3 same memory adj controller$1 and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19

7/29/08 4:22:02 PM
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 08/25/2008

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EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2628	
MAIL DATE	**DELIVERY MODE**
08/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 3, 2008 has been entered.

Response to Arguments

2. Applicant's arguments filed July 3, 2008 have been fully considered but they are not persuasive.

3. Applicant argues that the alleged motivation for modifying Perego (US006864896B2) with Furtner's (US006778177B1) teaching of placing a plurality of modules on a single chip, namely that placing a plurality of modules on a single chip takes up less space is not applicable in this instance as to Perego since it would render the Perego system inoperable for its intended purpose since Perego teaches a scalable module system and unified memory architecture with a memory controller coupled to multiple modules (p. 8-9).

In reply, the Examiner disagrees. Perego actually describes that it is advantageous to integrate a plurality of subsystems into a single integrated circuit. Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (col. 1, lines 34-39). Since Perego describes that it is advantageous to integrate a plurality of

subsystems into a single integrated circuit, implementing the teaching of placing the plurality of graphics pipelines on a single chip as taught by Furtner (col. 6, lines 30-32) into the Perego system would not render the Perego system inoperable for its intended purpose.

4. Applicant argues combination of Perego, MacInnis (US006570579B1) and Furtner would change operation of Perego to point where it would be inoperable for its intended purpose (p. 9).

In reply, Examiner disagrees. MacInnis is used for its teaching of having memory controller on same chip as graphics pipeline (col. 4, lines 65-67; col. 5, lines 36-41; col. 6, lines 10-13). Perego teaches it is advantageous to integrate a plurality of subsystems into a single integrated circuit (col. 1, lines 34-39), as discussed above. Perego also goes on to describe "As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 39-43). So, implementing the teaching of having memory controller on same chip as a graphics pipeline as taught by MacInnis into the Perego system would not render the Perego system inoperable for its intended purpose.

5. As per Claim 4, Applicant argues that as claimed, the multiple graphics pipelines on the same chip include the front end circuitry, and not a separate CPU that passes information through a graphics controller as taught in Perego (p. 9-10).

In reply, Examiner points out that Claim 4 does not recite that multiple graphics pipelines are on same chip, and that is why this limitation is not addressed in rejection for Claim 4. This limitation is addressed in the rejection for Claim 1, and Furtner is used to teach this limitation.

6. As per Claim 24, Applicant argues Perego does not teach multiple backend circuitry on common chip nor common front end circuitry and memory controller on common chip (p. 10).

In reply, Examiner points out Furtner and MacInnis are used to teach these limitations.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-4, 6, 7, 10, 12, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1), further in view of MacInnis (US006570579B1).

10. As per Claim 1, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63) having at least 2 graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two graphics pipelines operative to process data in dedicated tile (col. 5, lines 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines (312), operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories (314) (col. 3, lines 65-67; col. 4, lines 1-10, 48-65). Shared memories (314) are each part of main

memory (col. 1, lines 44-54; col. 3, lines 3-6), and so are considered to be one memory. Repeating tile pattern includes horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (col. 5, lines 19-27, 38-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 34-43).

However, Perego does not expressly teach graphics pipelines (312) are on a same chip. However, Furtner teaches that the graphics pipelines are on a same chip (col. 6, lines 30-32).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Perego so graphics pipelines are on same chip as suggested by Furtner. Placing plurality of modules on single chip takes up less space as compared to using multiple chips, and this is well-known in the art.

However, Perego and Furtner do not expressly teach memory controller is also on the same chip. However, MacInnis teaches memory controller (54) is on same chip (10) as graphics pipeline (58), as shown in Fig. 2 (col. 4, lines 65-67; col. 5, lines 36-41; col. 6, lines 10-13). This would be obvious for same reasons given above.

11. As per Claim 2, Perego teaches square regions have two dimensional partitioning of memory (col. 5, lines 19-33).

12. As per Claim 3, Perego discloses that the memory is a frame buffer (col. 5, lines 32-33).

13. As per Claim 4, Perego teaches each of at least two graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process portion of pixel data (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). In order for front end circuitry (308) to generate pixel data, it must receive vertex data.

14. As per Claim 6, Perego does not expressly teach each tile of set of tiles has 16x16 pixel array. But, Furtner teaches this limitation (col. 11, lines 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so each tile of set of tiles further has 16x16 pixel array because Furtner suggests depending on number of parallel image-rendering pipelines and depending on memory organization, optimum tile size and shape can be selected (col. 11, lines 45-48, 64-65), and so it would be obvious to modify tile size to be 16x16 pixels if that would be optimum tile size for particular number of parallel image-rendering pipelines and particular memory organization.

15. As per Claim 7, Perego teaches the at least two graphics pipelines (312, Fig. 3) separately receive pixel data from front end circuitry (308) (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44).

16. As per Claim 10, Perego teaches first of at least two graphics pipelines (first rendering engine of 312, Fig. 3) processes pixel data only in first set of tiles (tiles labeled "RE0" in Fig. 5) in repeating tile pattern (col. 5, lines 23-44).

17. As per Claim 12, Perego teaches second of at least two graphics pipelines (second rendering engine of 312, Fig. 3) processes pixel data only in second set of tiles (tiles labeled "RE1" in Fig. 5) in repeating tile pattern (col. 5, lines 23-44).

18. As per Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Perego teaches four graphics pipelines (col. 5, lines 41-44). So Claim 14 is rejected under the same rationale as Claims 4 and 10.

19. As per Claim 17, Perego does not teach 3rd and 4th graphics pipelines are on separate chips. However, Furtner teaches 3rd and 4th pipelines are on separate chips (col. 6, lines 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so pipelines are on separate chips because Furtner teaches this makes system more configurable by being able to easily add more graphics pipelines to increase performance (col. 6, lines 29-30, 42-51).

20. Claims 5, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1), further in view of MacInnis (US006570579B1), further in view of Kelleher (US005794016A).

21. As per Claim 5, Perego, Furtner, and MacInnis are relied upon for teachings for Claim 4.

But, Perego, Furtner, and MacInnis do not explicitly teach at each of 2 graphics pipelines includes scan converter, coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry. But, Kelleher teaches each of at least 2 graphics pipelines (20A, 20B, Fig. 3; col. 3, lines 22-23; col. 4, lines 9-14) includes scan converter (update stage, Fig. 7), coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry (col. 8, lines 52-61; col. 9, lines 1-23; col. 6, lines 26-28).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Perego, Furtner, and MacInnis so at each of at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to

determine the portion of the pixel data to be processed by the back end circuitry because Kelleher suggests scan converters are needed in order to define image data as array of pixels by calculating pixel addresses (col. 9, lines 1-23), as is well-known in the art.

22. As per Claim 18, Perego does not teach a bridge operable to transmit vertex data to each of the 1st, 2nd, 3rd and 4th graphics pipelines. But, Kelleher teaches a bridge (38, Fig. 3) operative to transmit vertex data to each of the first (20A), second (20B), third (20C) and fourth (20N) graphics pipelines (col. 3, lines 22-23; col. 4, lines 9-14; col. 8, lines 56-65; col. 3, lines 46-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego to include a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines because Kelleher suggests the advantage of being able to convert the vertex data to pixel data in parallel, which increases the efficiency of the graphics system (col. 2, lines 31-35; col. 8, lines 56-65; col. 9, lines 1-23).

23. As per Claim 24, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63), having front end circuitry (308) operative to generate pixel data in response to primitive data for primitive to be rendered (col. 5, lines 19-23); 1st back end circuitry (1st rendering engine 312), coupled to front end circuitry 308, operative to process 1st portion of pixel data (labeled "RE0" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 1st back end circuitry, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; 2nd back end circuitry (second rendering engine 312), coupled to front end circuitry 308, operative to process 2nd portion of pixel data (labeled "RE1" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 2nd back end circuitry (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44); and

memory controller (310), coupled to 1st and 2nd back end circuitry (312) operative to transmit and receive processed pixel data (col. 3, lines 65-67; col. 4, lines 1-53; col. 5, lines 32-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 34-43).

However, Perego does not explicitly teach first scan converter and second scan converter. However, Kelleher teaches first scan converter, coupled between front end circuitry (14, Fig. 3) and first back end circuitry (update stage, Fig. 7 in 20A, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by first back end circuitry (col. 3, lines 22-23; col. 8, lines 33-col. 9, lines 23), and operative to provide position coordinates to first back end circuitry in response to pixel data (col. 4, lines 60-62; col. 8, lines 52-65; col. 6, lines 36-38); second scan converter, coupled between front end circuitry and second back end circuitry (update stage, Fig. 7 in 20B, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by second back end circuitry, and operative to provide position coordinates to second back end circuitry in response to pixel data (col. 3, lines 22-23; col. 8, line 33-col. 9, line 23; col. 4, lines 60-62; col. 8, lines 52-65; col. 6, lines 36-38). This would be obvious for same reasons given in the rejection for Claim 5.

However, Perego and Kelleher do not expressly teach front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. However, Furtner teaches graphics pipelines are on same chip (col. 6, lines 30-32). Front end circuitry, first back end circuitry, and first scan converter of Perego-Kelleher combination make up one graphics pipeline, and front end circuitry, second back end circuitry, and second scan converter of Perego-Kelleher combination make up another graphics pipeline, as discussed above. Since Furtner teaches graphics pipelines are on same chip, this teaching from Furtner can be applied to Perego-Kelleher combination so front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. This would be obvious for reasons for Claim 1.

However, Perego, Kelleher, and Furtner do not expressly teach memory controller is also on the same chip. However, MacInnis teaches this limitation, as discussed for Claim 1.

24. Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), in view of Furtner (US006778177B1), further in view of MacInnis (US006570579B1), further in view of Kelleher (US005794016A), further in view of Hamburg (US005905506A).

Perego, Furtner, and MacInnis are relied upon for teachings relative to Claim 10.

However, Perego, Furtner, and MacInnis do not explicitly teach scan converter. However, Kelleher teaches first of the at least two graphics pipelines (20A, Fig. 3; col. 3, lines 22-23; col. 4, lines 9-14) further includes scan converter (84, Fig. 7), coupled to front end circuitry (80, 82) and back end circuitry (col. 8, lines 52-col. 9, lines 23). Scan converter determines which groups of blocks 52 within graphics memory 22 are allocated to and controlled

by graphics pipelines (col. 8, lines 52-65; col. 6, lines 26-28). Graphics memory is partitioned into plurality of pixel blocks that are tiled in x-and y-direction of graphics memory (col. 4, lines 60-62). So, scan converter is inherently operative to provide memory addresses or position coordinates of pixels within first set of tiles to be processed by back end circuitry. This would be obvious for the same reasons given in the rejection for Claim 5.

But, Perego, Furtner, MacInnis, and Kelleher do not expressly teach using tile identification data to indicate which tiles are to be processed. But, Hamburg teaches pixel identification line for receiving tile identification data indicating which tiles are to be processed (col. 5, lines 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Perego, Furtner, MacInnis, and Kelleher to include using tile identification data to indicate which tiles are to be processed because Hamburg suggests advantage of using tile identification data to easily track storage locations of tile pixel data and being able to easily retrieve data for particular image tile (col. 1, lines 46-54).

25. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1), further in view of MacInnis (US006570579B1), further in view of Kent (US 20030164830A1).

Perego, Furtner, and MacInnis are relied on for teachings for Claim 17. Perego teaches data includes polygon (col. 5, lines 19-23). Furtner teaches third and fourth graphics pipelines are on separate chips (col. 6, lines 47-51), as discussed for Claim 17.

But, Perego, Furtner, and MacInnis do not teach creating bounding box around polygon and each corner of bounding box is checked against super tile that belongs to each separate chip

and if bounding box does not overlap any of super tiles associated with separate chip, then processing circuit rejects whole polygon and processes next one. But, Kent teaches graphics pipeline [0006] calculates bounding box of primitive and testing this against VisRect. If bounding box of primitive is contained in other P10's super tile the primitive is discarded at this stage [0129]. Primitive can be polygon [0088]. Method used is to calculate distance from each subpixel sample point in point's bounding box to point's center and compare this to point's radius. Subpixel sample points with distance greater than radius do not contribute to pixel's coverage. Cost of this is kept low by only allowing small radius points hence distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within bounding box [0144]. Since method calculates distance from each subpixel sample point in point's bounding box, this must include all corners of bounding box. So, Kent teaches data includes polygon and graphics pipeline creates bounding box around polygon and wherein each corner of bounding box is checked against super tile that belongs to graphics pipeline and if bounding box does not overlap any of super tiles, then processing circuit rejects whole polygon and processes next one.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego, Furtner, and MacInnis to include bounding box as because Kent suggests processing super tiles one at a time in order to hide page break costs [0129, 0051].

26. Claims 20-22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1).

27. As per Claim 20, Perego teaches graphics processing method, comprising generating pixel data (col. 5, lines 19-25), which is inherently generated in response to received vertex data; determining pixels within set of tiles of repeating tile pattern corresponding to screen locations to

be processed by corresponding one of at least two graphics pipelines (312, Fig. 3) in response to pixel data, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; performing pixel operations on pixels within determined set of tiles by corresponding one of at least two graphics pipelines (col. 5, lines 19-44); and transmitting processed pixels to memory controller (310), wherein at least two graphics pipelines share memory controller (col. 3, line 65-col. 4, line 25; col. 5, lines 31-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (col. 1, lines 34-39).

But, Perego does not expressly teach graphics pipelines (312) are on a same chip. But, Furtner teaches graphics pipelines are on a same chip (col. 6, lines 30-32), as discussed for Claim 1.

28. As per Claim 21, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed further comprises determining set of tiles that corresponding graphics pipeline is responsible for (col. 5, lines 19-50).

29. As per Claim 22, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed comprises providing position coordinates of pixels within determined set of tiles to be processed to corresponding one of at least 2 graphics pipelines (col. 5, lines 19-44).

30. As per Claim 25, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63) having at least two graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two

graphics pipelines operative to process data in a dedicated tile (col. 5, lines 19-27, 38-44), wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (col. 5, lines 19-27, 38-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (col. 1, lines 34-39).

But, Perego does not expressly teach graphics pipelines are on a same chip. But, Furtner teaches graphics pipelines are on a same chip (col. 6, lines 30-32), as discussed for Claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Joni Hsu/
Patent Examiner, Art Unit 2628

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	**Art Unit**
	Hsu, Joni	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/29/2008								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	-								
	9	-								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
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	19	✓								
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	21	✓								
	22	✓								
	23	-								
	24	✓								
	25	✓								
	26	-								

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2628
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

Dear Sir:

In response to the Office Action mailed August 25, 2008, Applicants respond as follows.

Listing of the Claims begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

Electronic Acknowledgement Receipt	
EFS ID:	4354403
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	25-NOV-2008
Filing Date:	12-JUN-2003
Time Stamp:	16:21:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		10459797_Response.pdf	108637 87a32e9a8b434141fe8e8d0021fe3cb5db22806f	yes	12

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	12
Warnings:			
Information:			
	Total Files Size (in bytes):	108637	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Listing of Claims:

1. (previously presented) A graphics processing circuit, comprising:

at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; and

a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory;

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (canceled)

9. (canceled)

10. (previously presented) The graphics processing circuit of claim 7, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (previously presented) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. (previously presented) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front

end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to

be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (previously presented) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of at least two graphics pipelines on a same chip in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions;

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines; and

transmitting the processed pixels to a memory controller, wherein the at least two graphics pipelines share the memory controller.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (canceled)

24. (previously presented) A graphics processing circuit, comprising:

front end circuitry on a chip operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry on the chip, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter on the chip, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry on the chip, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter on the chip, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller on the chip, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data.

25. (previously presented) A graphics processing circuit, comprising:

at least two graphics pipelines on a chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions;

wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels.

26. (canceled)

REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 1-4, 6, 7, 10, 12, 14 and 17 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner, further in view of MacInnis. Applicants respectfully request reconsideration in view of the "Response to Arguments" section of the office action and the rejection. Applicants respectfully submit that the cited portion of Perego is being taken out of context and that the actual teachings of Perego are being ignored. Ignoring the teachings of the reference as a whole for purposes of rejecting a claim under 35 U.S.C. §103(a) is improper. Although the Perego reference in the Background section makes a general statement as noted by the Examiner, the Perego reference actually describes an invention that only allows certain elements that are integrated and specifically comes up with an invention whose architecture prevents the integration alleged to be taught by the office action. As specifically stated by Perego in column 4, lines 48-65 reproduced below:

> The architecture of FIG. 3 allows the memory controller/graphics controller 310 to issue high level primitive commands to the various rendering engines 312, thereby reducing the volume or bandwidth of data that must be communicated between the controller 310 and the memory modules 304. Thus, the partitioning of memory among multiple memory modules 304 improves graphical data throughput relative to systems in which a single graphics controller performs all processing tasks and reduces bandwidth contention with the CPU. This bandwidth reduction occurs because the primitive commands typically contain significantly less data than the amount of data referenced when rendering the primitive. Additionally, the system partitioning described allows aggregate bandwidth between the rendering engines and the memory devices to be much higher than the bandwidth between the controller and memory modules. Thus, effective system bandwidth is increased for processing graphics tasks. (Emphasis added).

The reference also refers to the specific structure of Perego stating "This ability to add and remove memory modules 304 provides an upgradeable and scalable memory and computing architecture." (Column4 , lines 45-48). Perego requires multiple discrete memory modules each

with its own rendering engine and each with its own memory and shared main memory. Perego requires interconnecting such modules to allow variable scalability in addition to requiring shared memory controllers. Moreover, a separate memory controller 310 is required by Perego which is part of a different and separate memory controller subsystem 302 that is coupled "to four distinct memory modules 304". (Column 4, lines 26-36). As stated in the reproduced portion of Perego above, Perego specifically requires a non-integration technique to facilitate the bandwidth reduction described by Perego (above) as well as allowing the scalability described in Perego. The teachings of the reference must not be ignored in a determination as to whether a combination would be obvious and where the combination would result in the inoperability or complete redesign of the cited reference, the combination and alleged suggestion is improper. Perego does not teach or suggest that any and all integration is proper. If so, the Perego patent would be invalid.

The Furtner reference has been cited as being properly combinable with Perego for allegedly teaching a motivation to place multiple graphic pipelines on the same chip as taught by Furtner. However, doing so as specifically stated by Perego would prevent the scalable architecture of Perego from existing. Perego teaches an opposite approach from that claimed and that described by Furtner and instead requires that the interconnecting modules allow variable scalability in addition to requiring shared memory controllers. One of ordinary skill in the art could not obtain a combination given the actual teachings of the references alleged in the office action.

In addition, the MacInnis reference is allegedly cited as teaching that "memory controller 54 is on same chip 10 as graphics pipeline, as shown in FIG. 2" (office action, page 5). Again, it is improper to combine teachings of multiple references wherein those teachings teach away

from one another and would render one of the references to be inoperable. Combining MacInnis with Furtner and Perego could not teach one of ordinary skill in the art that which is claimed since the MacInnis reference specifically teaches an opposite approach from that required by the Perego reference as to the memory controller. As stated in Perego, Perego cannot have a memory controller on the same chip as alleged. Perego would be improperly combinable with MacInnis and Furtner since Perego specifically teaches that the memory controller 310 cannot be integrated with the graphics controller. As set forth in the cited portion above, Perego specifically states that the architecture of FIG. 3 allows the memory controller/graphics controller 310 to issue high level primitive commands to various rendering engines 312 that are on separate modules, thereby reducing the volume or bandwidth of data that must be communicated between the controller 310 and the memory module 304. The partitioning of the memory among multiple memory modules improves graphical data throughput etc. Since the office action alleges that it would be obvious for the same reasons given above with respect to Perego, Applicants respectfully submit that this reasoning is not supported by the teachings of the references when the references are considered for what they actually teach. Accordingly, Applicants respectfully submit that the claims are in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter. For example, as to claim 4, in the "Response to Arguments" section, the Examiner states that "Claim 4 does not recite that multiple graphics pipelines are on the same chip". Applicants respectfully submit that claim 4 does recite this because it includes all of the limitations of claim 1. The office action appears to disregard the actual teachings of Perego since the office action cites the CPU 308 as being the front end circuitry. However, the claim requires that the graphics pipelines include the front end circuitry as claimed. There is no front end circuitry described

related to the CPU 308 in Perego. Applicants respectfully request a showing by column and line number if the rejection is maintained as it does not appear to be present in the cited portions.

Claims 5, 18, and 24 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner, further in view of MacInnis, further in view of Kelleher. Applicants respectfully reassert the relevant remarks made above and as such, these claims are also in condition for allowance. Claim 24 requires front end circuitry on a chip and first and second backend circuitry on the chip. The first and second backend circuitry processes different portions of the pixel data in response to position coordinates. A memory controller on the same chip is also coupled to the first and second backend circuitry. In this example, common front end circuitry is used on a chip for multiple backend operations. Again, the Perego reference illustrates a completely different structure and does not describe multiple backend circuitry on a common chip nor common front end circuitry and memory controller on a common chip as claimed. As such, the claim is also in condition for allowance. Also, these claims add additional novel and non-obvious subject matter.

Claims 11, 13, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego, in view of Furtner, further in view of MacInnis, further in view of Kelleher, further in view of Hamburg. Applicants respectfully reassert the remarks made above with respect to the Perego, Further and MacInnis references and as such, these claims are also believed to be in condition for allowance.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego, in view of Furtner, further in view of MacInnis, further in view of Kent. Applicants respectfully reassert the relevant remarks made above and as such, this claim is also in condition for allowance.

Claims 20-22 and 25 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner. Applicants respectfully reassert the remarks made above with respect to Perego and Furtner and as such, these claims are also in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: November 25, 2008

By: /Christopher J. Reckamp/
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PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/459,797	06/12/2003	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/25/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DORIS m. BURNS/

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S129	597	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S130	423	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S131	134	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S132	99	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S133	975	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S134	506	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S135	57	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S136	765	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42

S137	507	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S138	2244	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S139	1835	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S140	405	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S141	332	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S142	203	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal $2 and vertical $2 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S143	153	til$3 and repeat$3 with (til$3 pattern $3) same pixel $1 and pattern $3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42

S144	332	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S145	491	(multiple plurality) same pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S146	182	(multiple plurality) near2 pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S147	120	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S148	55	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S149	333	345/519.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S150	105	(multiple plural $3) adj2 graphic$1 adj (pipelin$3 process$3 engine$1) same (circuit chip)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S151	147	graphic$1 adj pipelin$3 same memory adj controller $1 and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42

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HSU, JONI	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed November 25, 2008 have been fully considered but they are not persuasive.

2. As per Claim 1, Applicant argues that Perego (US006864896B2) describes an invention that only allows certain elements that are integrated and specifically comes up with an invention whose architecture prevents the integration alleged to be taught by the office action. The reference also refers to the specific structure of Perego stating "This ability to add and remove memory modules 304 provides an upgradeable and scalable memory and computing architecture. Perego requires multiple discrete memory modules each with its own rendering engine and each with its own memory and shared main memory. Moreover, a separate memory controller 310 is required by Perego which is part of a different and separate memory controller subsystem 302 that is coupled to four distinct memory modules 304". Perego specifically requires a non-integration technique to facilitate the bandwidth reduction described by Perego as well as allowing the scalability described in Perego. The teachings of the reference must not be ignored in a determination as to whether a combination would be obvious and where the combination would result in the inoperability or complete redesign of the cited reference, the combination and alleged suggestion is improper. Perego does not suggest that any and all integration is proper. If so, the Perego patent would be invalid. Perego teaches an opposite approach from that claimed and that described by Furtner and instead requires that the interconnection modules allow variable scalability in addition to requiring shared

memory controllers. One of ordinary skill in the art could not obtain a combination given the actual teachings of the references alleged in the office action (p. 8-9).

In reply, the Examiner points out Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; c. 6, ll. 61-62). From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip. The Examiner makes note that Claim 1 recites "**at least two** graphics pipelines on a same chip", and this is what Perego teaches.

3. Applicant argues MacInnis (US006570579B1) specifically teaches an opposite approach from that required by Perego as to memory controller. As stated in Perego, Perego cannot have memory controller on the same chip as alleged. Perego specifically teaches that memory controller 310 cannot be integrated with the graphics controller. Perego specifically states that the architecture of Fig. 3 allows the memory controller/graphics controller 310 to issue high level primitive commands to various rendering engines 312 that are on separate modules, thereby reducing the volume or bandwidth of data that must be communicated between the controller 310 and the memory module 304. The partitioning of the memory among multiple memory modules improves graphical data throughput (p. 9-10).

In reply, the Examiner points out that the section in Perego cited by Applicant describes that the reduction in bandwidth is due to the fact that there are a plurality of graphics pipelines, and each graphics pipeline has a corresponding portion of shared memory (c. 4, ll. 48-65). However, Perego does not actually describe that the reduction

in bandwidth is due to the fact that the memory controller is on a separate chip from the graphics pipelines. Therefore, if the device of Perego is modified so that the memory controller and at least two graphics pipelines are on the same chip, the device of Perego would still be able to reduce the bandwidth by having the memory controller issue high level primitive commands to various rendering engines that are on the same chip. Therefore, the various rendering engines that are on the same chip would still be able to perform the processing tasks rather than having a single graphic controller perform all the processing tasks, therefore reducing the bandwidth, and reducing bandwidth contention with the CPU. Therefore, if the device of Perego is modified so that the memory controller and at least two graphics pipelines are on the same chip, the device of Perego would still be able to operate in the same manner that reduces the bandwidth. Therefore, Perego does not teach away from the teaching from MacInnis, and therefore the teaching from MacInnis is able to be combined with the teachings from Perego.

4. Applicant argues that as to Claim 4 in the "Response to Arguments" section, the Examiner states that "Claim 4 does not recite that multiple graphics pipelines are on the same chip". Claim 4 does recite this because it includes all of the limitations of Claim 1 (p. 10).

In reply, the Examiner respectfully again clarifies that the limitation that multiple graphics pipelines are on the same chip was not expressly addressed in the rejection for Claim 4 because it was **already addressed in the rejection for Claim 1**, and this limitation is not recited in Claim 4. The Examiner understands that Claim 4 includes all of the limitations of Claim 1, but since all of the limitations of Claim 1 were already

addressed in the rejection for Claim 1, the Examiner did not feel the need to continually repeat the rejection for Claim 1 for each of the claims that depend from Claim 1.

5. Applicant argues that the office action cites the CPU 308 as being the front end circuitry. However, the claim requires that the graphics pipelines include the front end circuitry. There is no front end circuitry described related to the CPU 308 in Perego (p. 10-11).

In reply, the Examiner points out that Perego teaches that the CPU sorts the primitive data according to the spatial region of the rendering surface (e.g., the x and y coordinates) covered by that primitive, and the rendering surface is divided into multiple rectangular regions of pixels (c. 5, ll. 19-27). One of ordinary skill in the art would understand that data pertaining to the x and y coordinates covered by the primitive would include vertex data. The main memory is used to store data which are referenced during the execution of the programs (c. 1, ll. 18-21). Therefore, the CPU is operative to receive vertex data (data pertaining to the x and y coordinates covered by the primitive) from the main memory and generate pixel data corresponding to a primitive to be rendered (c. 5, ll. 19-27; c. 1, ll. 18-21). Perego teaches that rendering engine 312 is coupled to the CPU, and is operative to receive and process a rectangular region of pixel data (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44). Since the CPU is coupled to the rendering engine 312, and the CPU and the rendering engine 312 both perform graphics processing, and, the CPU performs the operations of the front end circuitry, and the rendering engine 312 performs the operations of the back end circuitry, the CPU and the rendering engine 312 are considered to be part of a graphics pipeline, and the CPU is considered to be the front end circuitry included in the graphics pipeline.

6. As per Claim 24, Applicant argues that Perego does not describe multiple backend circuitry on a common chip nor common front end circuitry and memory controller on a common chip (p. 11).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Furtner (US006778177B1) and Kelleher (US005794016A) are used to expressly teach these limitations.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-4, 6, 7, 10, 12, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1).

10. As per Claim 1, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63) having at least 2 graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least 2 graphics pipelines operative to process data in dedicated tile (c. 5, ll. 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines 312, operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories 314 (c. 3, ll. 65-67; c. 4, ll. 1-10, 48-65). Shared memories 314 are each part of main memory (c. 1, ll. 44-54; c. 3, ll. 3-6), and so are considered to be one memory. Repeating tile pattern includes horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (c. 5, ll. 19-27, 38-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (c. 1, ll. 34-43). Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; c. 6, ll. 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800.

However, Perego does not expressly teach graphics pipelines (312) are on a same chip. However, Furtner teaches this limitation (c. 6, ll. 30-32).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Perego so graphics pipelines are on same chip as suggested by Furtner. Placing plurality of modules on single chip takes up less space as compared to using multiple chips, and this is well-known in the art.

However, Perego and Furtner do not expressly teach memory controller is also on the same chip. However, MacInnis teaches memory controller (54) is on same chip (10) as graphics pipeline (58), as shown in Fig. 2 (c. 4, ll. 65-67; c. 5, ll. 36-41; c. 6, ll. 10-13). This would be obvious for reasons given above. Perego describes that the reduction in bandwidth is due to the fact that there are a plurality of graphics pipelines, and each graphics pipeline has a corresponding portion of shared memory (c. 4, ll. 48-65). However, Perego does not actually describe that the reduction in bandwidth is due to the fact that the memory controller is on a separate chip from the graphics pipelines. Therefore, if the device of Perego is modified so that the memory controller and at least two graphics pipelines are on the same chip, the device of Perego would still be able to reduce the bandwidth by having the memory controller issue high level primitive commands to various rendering engines that are on the same chip. Therefore, the various rendering engines that are on the same chip would still be able to perform the processing tasks rather than having a single graphic controller perform all the processing tasks, therefore reducing the bandwidth, and reducing bandwidth contention with the CPU. Therefore, if the device of Perego is modified so that the memory controller and at least two graphics pipelines are on the same chip, the device of Perego would still be able to operate in the same manner that reduces the bandwidth. Therefore, Perego does not teach

away from the teaching from MacInnis, and therefore the teaching from MacInnis is able to be combined with the teachings from Perego.

11. As per Claim 2, Perego teaches square regions have two dimensional partitioning of memory (c. 5, ll. 19-33).

12. As per Claim 3, Perego teaches that the memory is a frame buffer (c. 5, ll. 32-33).

13. As per Claim 4, Perego teaches each of at least 2 graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process portion of pixel data (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44). In order for front end circuitry (308) to generate pixel data, it must receive vertex data. Perego teaches that the CPU sorts the primitive data according to the spatial region of the rendering surface (e.g., the x and y coordinates) covered by that primitive, and the rendering surface is divided into multiple rectangular regions of pixels (c. 5, ll. 19-27). One of ordinary skill in the art would understand that data pertaining to the x and y coordinates covered by the primitive would include vertex data. The main memory is used to store data which are referenced during the execution of the programs (c. 1, ll. 18-21). Therefore, the CPU is operative to receive vertex data (data pertaining to the x and y coordinates covered by the primitive) from the main memory and generate pixel data corresponding to a primitive to be rendered (c. 5, ll. 19-27; c. 1, ll. 18-21). Perego teaches that rendering engine 312 is coupled to the CPU, and is operative to receive and process a rectangular region of pixel data (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44). Since the CPU is coupled to the rendering engine 312, and the CPU and the rendering engine 312 both perform graphics processing, and, the CPU performs the operations of the front end

circuitry, and the rendering engine 312 performs the operations of the back end circuitry, the CPU and the rendering engine 312 are considered to be part of a graphics pipeline, and the CPU is considered to be the front end circuitry included in the graphics pipeline.

14. As per Claim 6, Perego does not expressly teach each tile of set of tiles has 16x16 pixel array. But, Furtner teaches this limitation (c. 11, ll. 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so each tile of set of tiles further has 16x16 pixel array because Furtner suggests depending on number of parallel image-rendering pipelines and depending on memory organization, optimum tile size and shape can be selected (c. 11, ll. 45-48, 64-65), and so it would be obvious to modify tile size to be 16x16 pixels if that would be optimum tile size for particular number of parallel image-rendering pipelines and particular memory organization.

15. As per Claim 7, Perego teaches at least two graphics pipelines (312) separately receive pixel data from front end circuitry (308) (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44).

16. As per Claim 10, Perego teaches first of at least two graphics pipelines (first rendering engine of 312, Fig. 3) processes pixel data only in first set of tiles (tiles labeled "RE0" in Fig. 5) in repeating tile pattern (c. 5, ll. 23-44).

17. As per Claim 12, Perego teaches second of at least two graphics pipelines (second rendering engine of 312, Fig. 3) processes pixel data only in second set of tiles (tiles labeled "RE1" in Fig. 5) in repeating tile pattern (c. 5, ll. 23-44).

18. As per Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Perego teaches four graphics pipelines (c. 5, ll. 41-44). So Claim 14 is rejected under the same rationale as Claims 4 and 10.

19. As per Claim 17, Perego does not teach 3rd and 4th graphics pipelines are on separate chips. However, Furtner teaches this limitation (c. 6, ll. 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so pipelines are on separate chips because Furtner teaches this makes system more configurable by being able to easily add more graphics pipelines to increase performance (c. 6, ll. 29-30, 42-51).

20. Claims 5, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kelleher (US005794016A).

21. As per Claim 5, Perego, Furtner, and MacInnis are relied on for teachings for Claim 4.

But, Perego, Furtner, and MacInnis do not explicitly teach at each of 2 graphics pipelines includes scan converter, coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry. But, Kelleher teaches each of at least 2 graphics pipelines (20A, 20B, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) includes scan converter (update stage, Fig. 7), coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry (c. 8, ll. 52-61; c. 9, ll. 1-23; c. 6, ll. 26-28).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego, Furtner, and MacInnis so at each of at least two graphics pipelines includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry

because Kelleher suggests scan converters are needed in order to define image data as array of pixels by calculating pixel addresses (c. 9, ll. 1-23), as is well-known in the art.

22. As per Claim 18, Perego does not teach a bridge operable to transmit vertex data to each of the 1st, 2nd, 3rd and 4th graphics pipelines. But, Kelleher teaches a bridge (38, Fig. 3) operative to transmit vertex data to each of the 1st (20A), 2nd (20B), 3rd (20C) and 4th (20N) graphics pipelines (c. 3, ll. 22-23; c. 4, ll. 9-14; c. 8, ll. 56-65; c. 3, ll. 46-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego to include a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines because Kelleher suggests being able to convert the vertex data to pixel data in parallel, which increases the efficiency of the graphics system (c. 2, ll. 31-35; c. 8, ll. 56-65; c. 9, ll. 1-23).

23. As per Claim 24, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63), having front end circuitry (308) operative to generate pixel data in response to primitive data for primitive to be rendered (c. 5, ll. 19-23); 1st back end circuitry (1st rendering engine 312), coupled to front end circuitry 308, operative to process 1st portion of pixel data (labeled "RE0" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 1st back end circuitry, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; 2nd back end circuitry (second rendering engine 312), coupled to front end circuitry 308, operative to process 2nd portion of pixel data (labeled "RE1" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 2nd back end circuitry (c. 3, ll. 63-c. 4, ll. 2; c. 5, ll. 19-44); and memory controller (310), coupled to 1st and 2nd back end circuitry (312) operative to transmit and receive processed pixel

data (c. 3, ll. 65-67; c. 4, ll. 1-53; c. 5, ll. 32-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (c. 1, ll. 34-43).

However, Perego does not explicitly teach first scan converter and second scan converter. However, Kelleher teaches first scan converter, coupled between front end circuitry (14, Fig. 3) and first back end circuitry (update stage, Fig. 7 in 20A, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by first back end circuitry (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23), and operative to provide position coordinates to first back end circuitry in response to pixel data (c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38); second scan converter, coupled between front end circuitry and second back end circuitry (update stage, Fig. 7 in 20B, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by second back end circuitry, and operative to provide position coordinates to second back end circuitry in response to pixel data (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23; c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38). This would be obvious for reasons given in the rejection for Claim 5.

However, Perego and Kelleher do not expressly teach front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. However, Furtner teaches graphics pipelines are on same

chip (c. 6, ll. 30-32). Front end circuitry, first back end circuitry, and first scan converter of Perego-Kelleher combination make up one graphics pipeline, and front end circuitry, second back end circuitry, and second scan converter of Perego-Kelleher combination make up another graphics pipeline, as discussed above. Since Furtner teaches graphics pipelines are on same chip, this teaching from Furtner can be applied to Perego-Kelleher combination so front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. This would be obvious for reasons for Claim 1.

However, Perego, Kelleher, and Furtner do not expressly teach memory controller is also on the same chip. However, MacInnis teaches this limitation, as discussed for Claim 1.

24. Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kelleher (US005794016A), further in view of Hamburg (US005905506A).

Perego, Furtner, and MacInnis are relied upon for teachings relative to Claim 10.

However, Perego, Furtner, and MacInnis do not explicitly teach scan converter. However, Kelleher teaches first of the at least two graphics pipelines (20A, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) further includes scan converter (84, Fig. 7), coupled to front end circuitry (80, 82) and back end circuitry (c. 8, ll. 52-c. 9, ll. 23). Scan converter determines which groups of blocks 52 within graphics memory 22 are allocated to and controlled by graphics pipelines (c. 8, ll. 52-65; c. 6, ll. 26-28). Graphics memory is partitioned into plurality of pixel blocks that are tiled in x-and y-direction of graphics

memory (c. 4, ll. 60-62). So, scan converter is inherently operative to provide memory addresses or position coordinates of pixels within first set of tiles to be processed by back end circuitry. This would be obvious for the reasons given in the rejection for Claim 5.

But, Perego, Furtner, MacInnis, and Kelleher do not expressly teach using tile identification data to indicate which tiles are to be processed. But, Hamburg teaches pixel identification line for receiving tile identification data indicating which tiles are to be processed (c. 5, ll. 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego, Furtner, MacInnis, and Kelleher to include using tile identification data to indicate which tiles are to be processed because Hamburg suggests advantage of using tile identification data to easily track storage locations of tile pixel data and being able to easily retrieve data for particular image tile (c. 1, ll. 46-54).

25. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kent (US 20030164830A1).

Perego, Furtner, and MacInnis are relied on for teachings for Claim 17. Perego teaches data includes polygon (c. 5, ll. 19-23). Furtner teaches third and fourth graphics pipelines are on separate chips (c. 6, ll. 47-51), as discussed for Claim 17.

But, Perego, Furtner, and MacInnis do not teach creating bounding box around polygon and each corner of bounding box is checked against super tile that belongs to each separate chip and if bounding box does not overlap any of super tiles associated with separate chip, then processing circuit rejects whole polygon and processes next one. But, Kent teaches graphics pipeline [0006] calculates bounding box of primitive and

testing this against VisRect. If bounding box of primitive is contained in other P10's super tile the primitive is discarded at this stage [0129]. Primitive can be polygon [0088]. Method used is to calculate distance from each subpixel sample point in point's bounding box to point's center and compare this to point's radius. Subpixel sample points with distance greater than radius do not contribute to pixel's coverage. Cost of this is kept low by only allowing small radius points hence distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within bounding box [0144]. Since method calculates distance from each subpixel sample point in point's bounding box, this must include all corners of bounding box. So, Kent teaches data includes polygon and graphics pipeline creates bounding box around polygon and wherein each corner of bounding box is checked against super tile that belongs to graphics pipeline and if bounding box does not overlap any of super tiles, then processing circuit rejects whole polygon and processes next one.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego, Furtner, and MacInnis to include bounding box as because Kent suggests processing super tiles one at a time in order to hide page break costs [0129, 0051].

26. Claims 20-22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) and Furtner (US006778177B1).

27. As per Claim 20, Perego teaches graphics processing method, comprising generating pixel data (c. 5, ll. 19-25), which is inherently generated in response to received vertex data; determining pixels within set of tiles of repeating tile pattern corresponding to screen locations to be processed by corresponding one of at least two

graphics pipelines (312, Fig. 3) in response to pixel data, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; performing pixel operations on pixels within determined set of tiles by corresponding one of at least two graphics pipelines (c. 5, ll. 19-44); and transmitting processed pixels to memory controller 310, at least 2 graphics pipelines share memory controller (c. 3, ll. 65-c. 4, ll. 25; c. 5, ll. 31-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (c. 1, ll. 34-39).

But, Perego does not expressly teach graphics pipelines (312) are on a same chip. But, Furtner teaches this limitation (c. 6, ll. 30-32), as discussed for Claim 1.

28. As per Claim 21, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed further comprises determining set of tiles that corresponding graphics pipeline is responsible for (c. 5, ll. 19-50).

29. As per Claim 22, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed comprises providing position coordinates of pixels within determined set of tiles to be processed to corresponding one of at least 2 graphics pipelines (c. 5, ll. 19-44).

30. As per Claim 25, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63) having at least two graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two graphics pipelines operative to process data in a dedicated tile (c. 5, ll. 19-27, 38-44), wherein the repeating tile pattern includes a horizontally and

vertically repeating pattern of regions of square regions, as shown in Fig. 5 (c. 5, ll. 19-27, 38-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (c. 1, ll. 34-39).

But, Perego does not expressly teach graphics pipelines are on a same chip. But, Furtner teaches this limitation (c. 6, ll. 30-32), as discussed for Claim 1.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Kee M Tung/
Supervisory Patent Examiner, Art Unit 2628

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/29/2008	02/06/2009							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	-	-							
	9	-	-							
	10	✓	✓							
	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
	14	✓	✓							
	15	✓	✓							
	16	✓	✓							
	17	✓	✓							
	18	✓	✓							
	19	✓	✓							
	20	✓	✓							
	21	✓	✓							
	22	✓	✓							
	23	-	-							
	24	✓	✓							
	25	✓	✓							
	26	-	-							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545, 532, 501, 502, 531, 519	7/29/08	JH
Above	UPDATED	2/6/09	JH

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) -- See attached search history.	2/6/09	JH

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Electronic Acknowledgement Receipt	
EFS ID:	5331837
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	13-MAY-2009
Filing Date:	12-JUN-2003
Time Stamp:	21:02:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$810
RAM confirmation Number	7005
Deposit Account	500441
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	10459797_IDS.pdf	608458 797f35070139ae47c305ff9d2381ed8a1f324acb	no	4
Warnings:					
Information:					
2	Transmittal Letter	10459797_IDSCover.pdf	70507 b11c424c53a05bfd41ee061ed95dba8bcc813c30	no	1
Warnings:					
Information:					
3	NPL Documents	10459797_Ref.pdf	2004500 37680eec53592334f809905f10cc03e77ff8dcde	no	10
Warnings:					
Information:					
4	Request for Continued Examination (RCE)	10459797_RCETransmittal.pdf	697435 1cfebae046d39e46b54c8623bb17436f39438d70	no	3
Warnings:					
Information:					
5		10459797_response.pdf	116628 f82cb3dfb40763bb7c9d67d39adcd0d3b1dd21ae	yes	12

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Claims	2	7
Applicant Arguments/Remarks Made in an Amendment	8	12

Warnings:					
Information:					
6	Fee Worksheet (PTO-875)	fee-info.pdf	30075 110784f12639bd35872b3823d227fe6fb8cb776e	no	2
Warnings:					