



US005579052A

United States Patent [19]

[11] Patent Number: **5,579,052**

Artieri

[45] Date of Patent: **Nov. 26, 1996**

[54] PICTURE PROCESSING SYSTEM

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[21] Appl. No.: **247,996**

[22] Filed: **May 24, 1994**

[30] Foreign Application Priority Data

May 27, 1993	[FR]	France	93 06612
Oct. 29, 1993	[FR]	France	93 13293

[51] Int. Cl.⁶ **H04N 7/30; H04N 7/32**

[52] U.S. Cl. **348/416**

[58] Field of Search 348/416, 699;
382/56, 43; 375/245, 246, 253; H04N 7/30,
7/32

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Primary Examiner—Tommy P. Chin

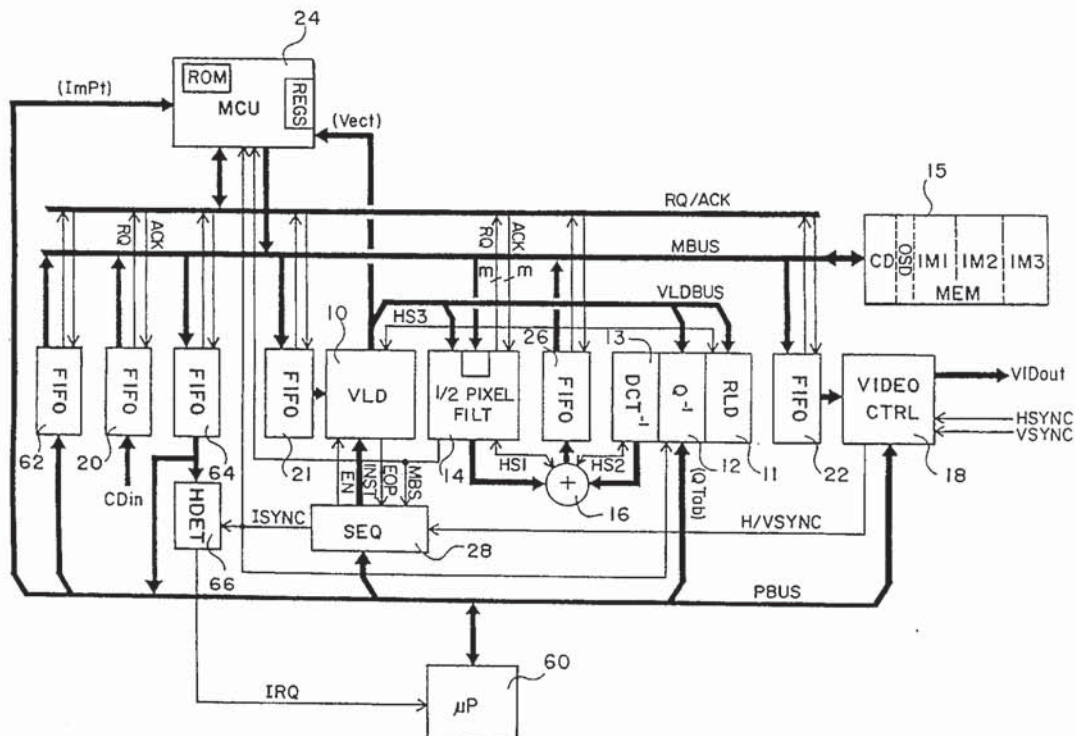
Assistant Examiner—Vu Le

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[57] ABSTRACT

A system that processes compressed data arriving in packets corresponding to picture blocks, the packets being separated by headers containing decoding parameters of the packets. A memory bus is controlled by a memory controller to exchange data between the processing elements and a picture memory. A pipeline circuit contains a plurality of processing elements. A parameter bus provides packets to be processed to the pipeline circuit, as well as the decoding parameters to elements of the system. The parameter bus is controlled by a variable length decoder that receives the compressed data from the memory bus and that extracts the packets and the decoding parameters therefrom.

13 Claims, 7 Drawing Sheets



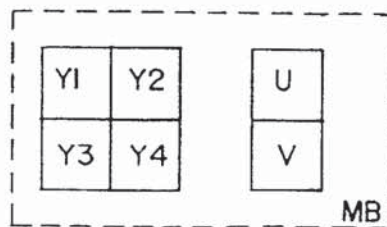
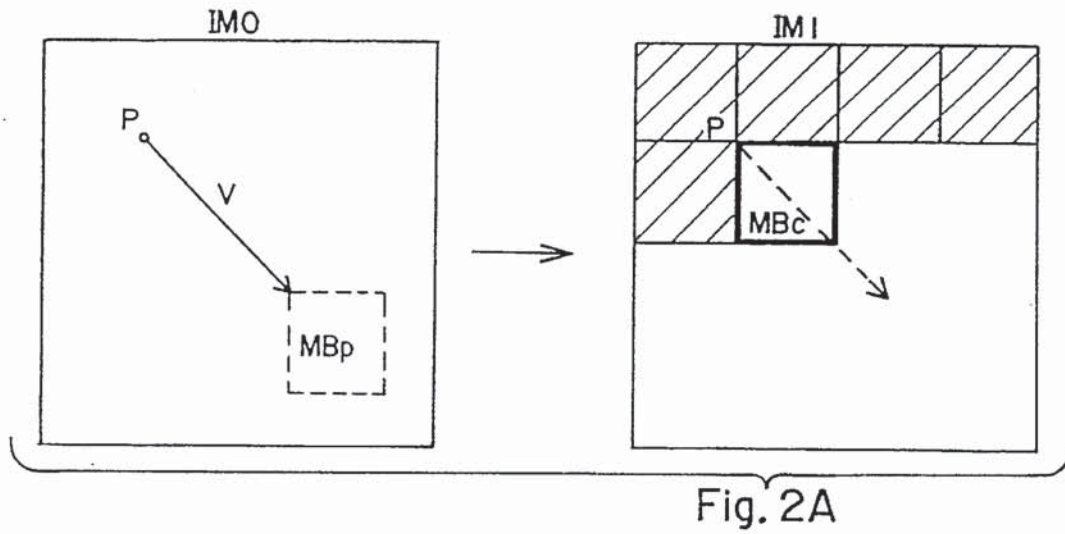
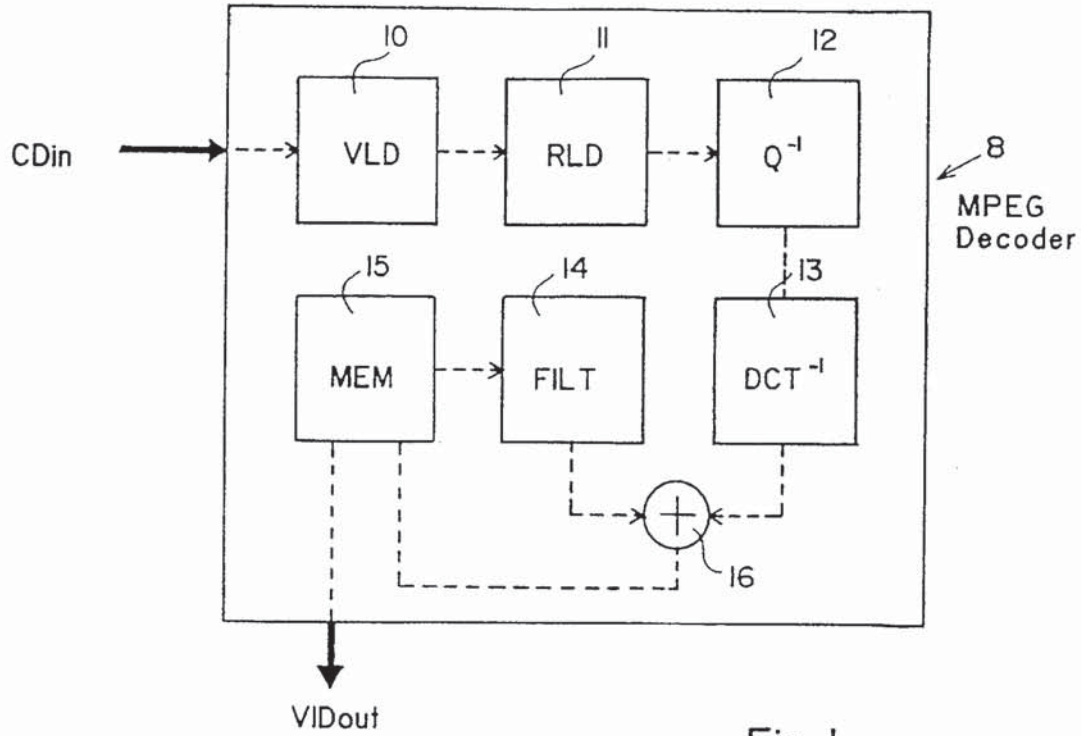
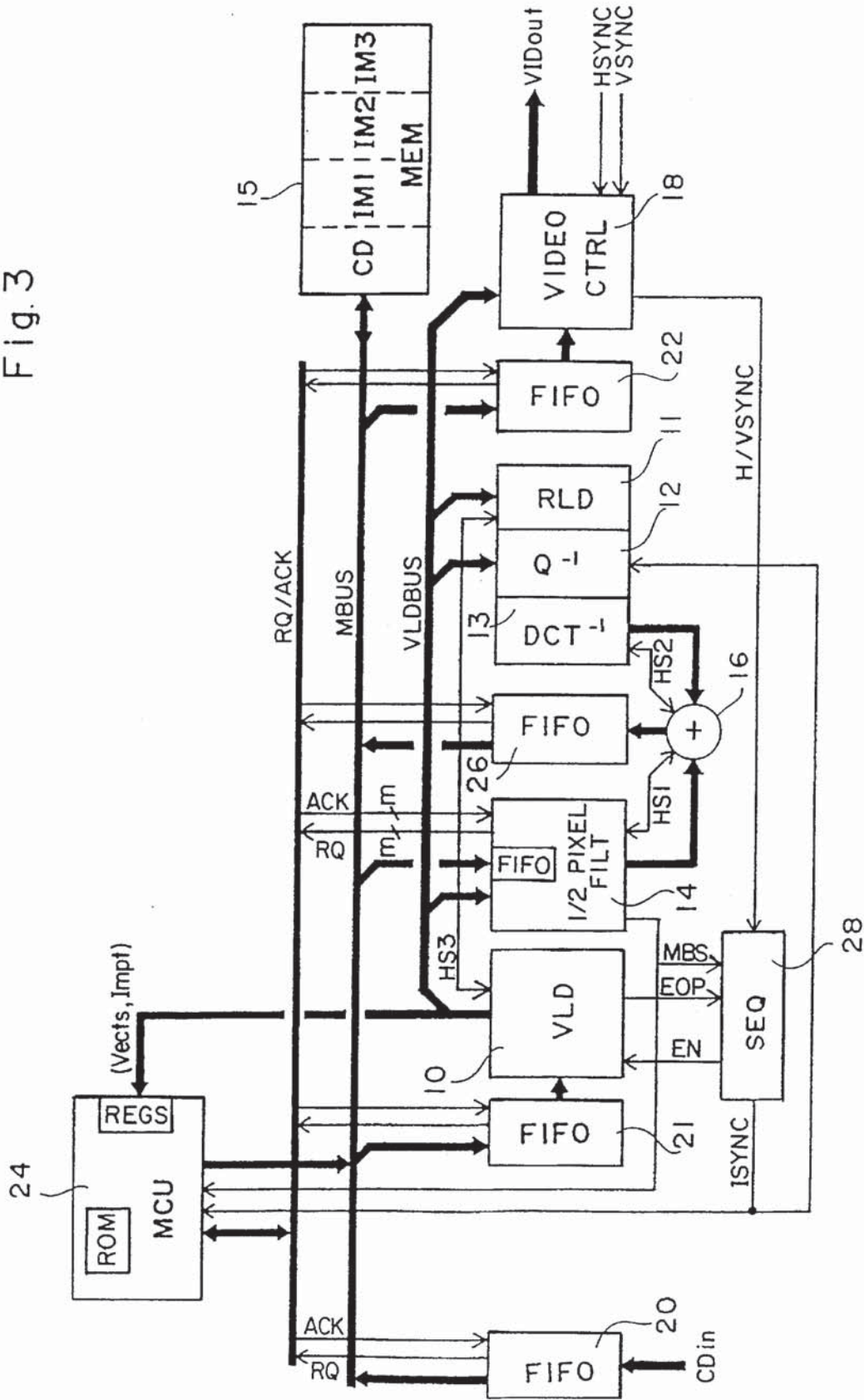


Fig. 3



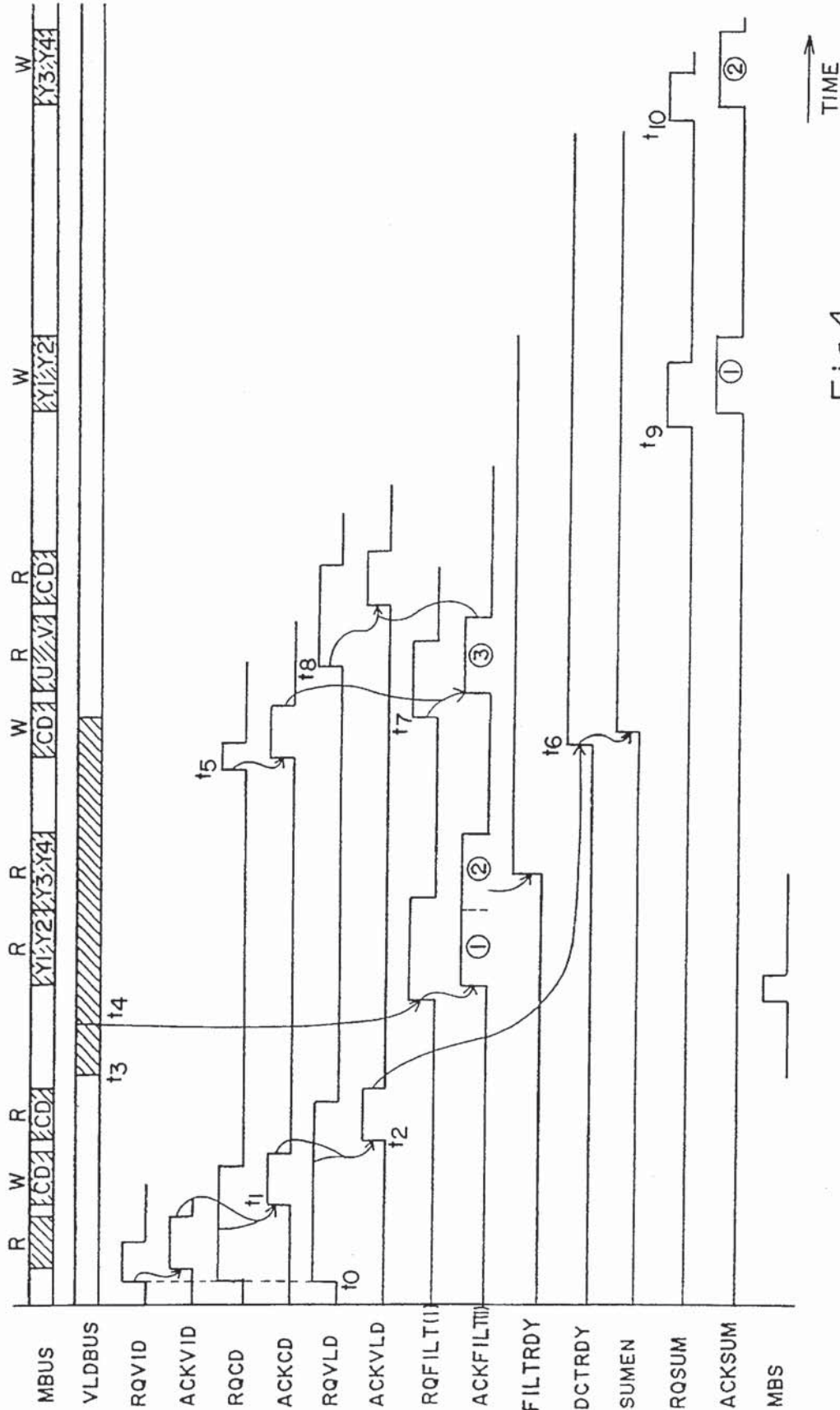


Fig.4

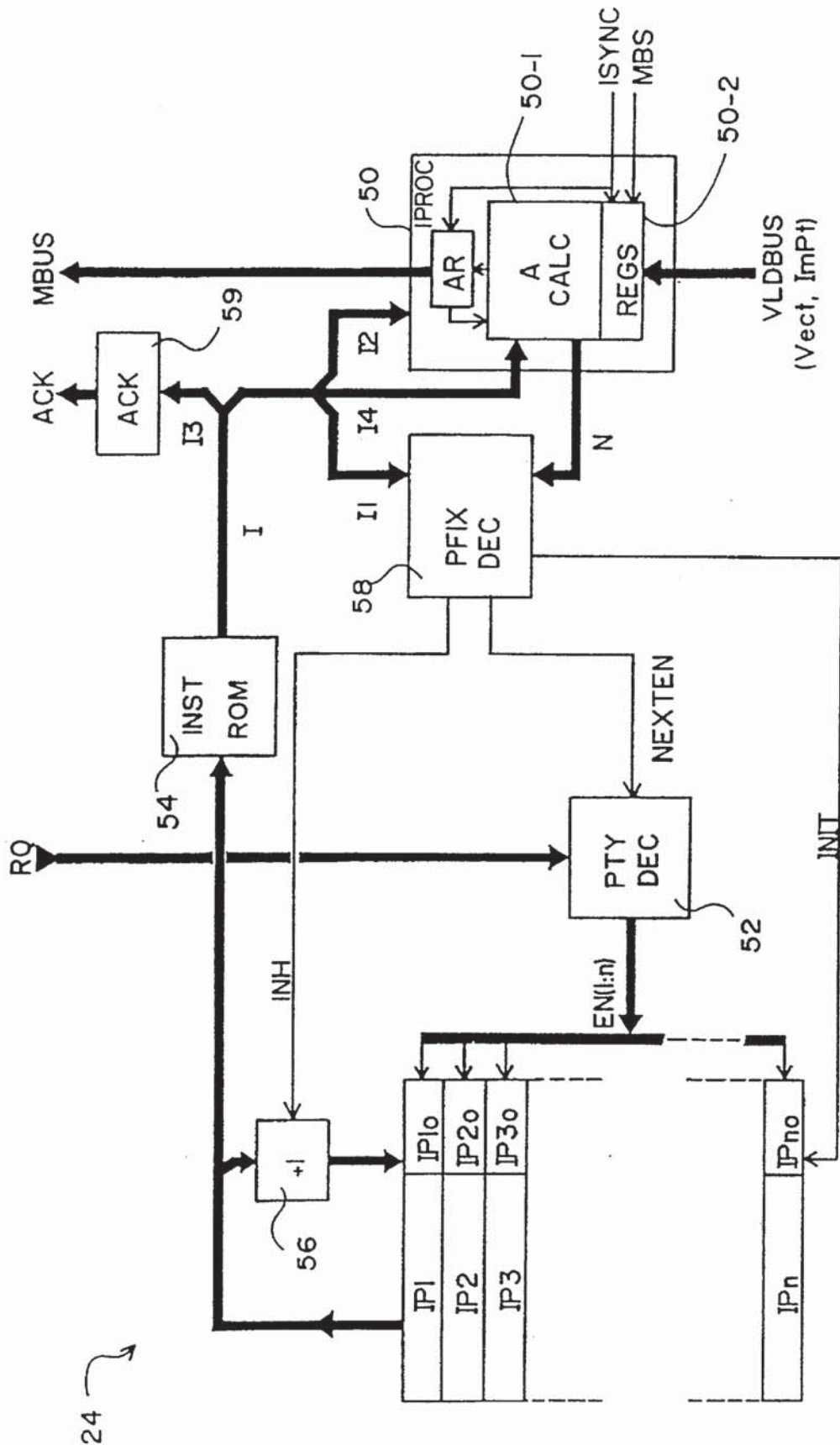


Fig. 5

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