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### VUMA Proposal

(Draft)

Video Electronics Standards Association

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#### VESA Unified Memory Architecture Hardware Specifications Proposal

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Document Revision: 0.4p

#### October 31, 1995

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#### Purpose

To enable core logic chipset and VUMA device designers to design VUMA devices supporting the Unified Memory Architecture.

#### Summary

This document contains a specification for VUMA devices' hardware interface. It includes logical and electrical interface specifications. The BIOS protocol is described in VESA document VUMA VESA BIOS Extensions (VUMA-SBE) rev. 1.0.

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#### Scope

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#### Support For This Specification

If you have a product that incorporates VUMA<sup>TM</sup>, you should ask the company that manufactured your product for assistance. If you are a manufacturer of the product, VESA can assist you with any clarification that you may require. All questions must be sent in writing to VESA via:

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#### Acknowledgments

This document would not have been possible without the efforts of the members of the 1995 VESA Unified Memory Architecture Committee and the professional support of the VESA staff.

#### Work Group Members

Any industry standard requires information from many sources. The following list recognizes members of the VUMA Committee, which was responsible for combining all of the industry input into this proposal.

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#### **Revision History**

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| Revision 0.2p                                    | Oct 5 '95  |
|--|------------|
| Added sync DRAM support                          | 5 a        |
| Electrical Section                               |            |
| Boot Protocol                                    | · .        |
| Reformatted document                             | -          |
| Revision 0.3p                                    | Oct 19 '95 |
| Graphics controller replaced with VUMA device    |            |
| MD[n:0] changed to t/s                           |            |
| Modified Aux Memory description                  |            |
| Added third solution to Memory Expansion Problem |            |
| Synch DRAM burst length changed to 2/4           |            |
| Modified all the bus hand off diagrams           |            |
| Added DRAM Driver Characteristics section        |            |
| Added DRAWI Driver Characteristics Section       |            |
| Revision 0.4p                                    | Oct 19 '95 |
| Sync DRAM Burst Length changed to 1/2/4          |            |
| DRAM controller pin multiplexing added           |            |
| Changed AC timing parameters                     |            |

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