

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,	§	Case No. 2:14-cv-902-JRG-RSP
	§	(Lead)
	§	
Plaintiff,	§	
	§	
v.	§	
	§	
SAMSUNG ELECTRONICS CO. LTD. and	§	
SAMSUNG ELECTRONICS AMERICA,	§	
INC.,	§	
	§	
<hr/>		
HUAWEI TECHNOLOGIES CO. LTD,	§	Case No. 2:14-cv-687-JRG-RSP
HUAWEI TECHNOLOGIES USA, INC.	§	(Consolidated)
and HUAWEI DEVICE USA, INC.,	§	
	§	
MOTOROLA MOBILITY LLC	§	Case No. 2:14-cv-689-JRG-RSP
	§	(Consolidated)
Defendants.	§	
	§	
	§	
<hr/>		

**PLAINTIFF PARTHENON UNIFIED MEMORY ARCHITECTURE LLC'S
OPENING CLAIM CONSTRUCTION BRIEF**

TABLE OF CONTENTS

I. Introduction..... 1

II. Overview of Patented Technology..... 2

III. Relevant Legal Standards 3

IV. Agreed Constructions..... 5

V. Terms for Construction..... 5

 A. “bus” 5

 B. “memory bus” 8

 C. “in real time” and related terms 9

 D. “fast bus”..... 13

 E. “coupled,” “coupleable” and “coupling” 14

 F. “directly supplied” and “directly supplies” 16

 G. “display device” and “display adapter 18

 H. “arbiter” terms..... 19

 I. “control circuit” 20

 J. “monolithically integrated into” and “integrated into” 21

 K. “contiguous” and “non-contiguous” 23

 L. “direct memory access (DMA) engine” and “direct memory access engine” 24

 M. “refresh logic” 24

 N. “[first, second, third] onboard memory” 25

VI. Conclusion 25

TABLE OF AUTHORITIES

Cases

<i>Abtox, Inc. v. Exitron Corp.</i> , 122 F.3d 1019 (Fed. Cir. 1997)	4
<i>Brown v. 3M</i> , 265 F.3d 1349 (Fed. Cir. 2001)	4
<i>Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.</i> , 381 F.3d 1111 (Fed. Cir. 2004)	3
<i>Markman v. Westview Instruments, Inc.</i> , 517 U.S. 370 (1996).....	3
<i>O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.</i> , 521 F.3d 1351 (Fed. Cir. 2008)	4
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005)	3, 4
<i>Power Integrations, Inc. v. Fairchild Semiconductor Int’l, Inc.</i> , 711 F.3d 1348 (Fed. Cir. 2013)	4
<i>U.S. Surgical Corp. v. Ethicon, Inc.</i> , 103 F.3d 1554 (Fed. Cir. 1997)	3, 4
<i>UltimatePointer, L.L.C. v. Nintendo Co., Ltd.</i> , 2013 WL 2325118 (E.D. Tex. May 28, 2013).....	23

I. INTRODUCTION

Plaintiff Parthenon Unified Memory Architecture LLC (“PUMA”) proposes constructions for the terms-in-dispute that are based on the intrinsic and extrinsic evidence.¹ In contrast, Defendants Samsung, Huawei and Motorola propose constructions that improperly import limitations from the specification, add extraneous language not contemplated by the claims, and ignore the inventive features of the patents.

PUMA has asserted nine patents against the Defendants relating to the implementation of shared memory in a computer system. All nine patents were originally assigned to STMicroelectronics, Inc. (“STMicro”), a semiconductor company based in Texas. STMicro filed the patent applications for U.S. Patent No. 5,812,789 and U.S. Patent No. 6,058,459 on the same day, and the two patents substantially overlap in their specifications, figures, and named inventors. Additionally, each of the ’789 Patent and the ’459 Patent explicitly incorporate by reference the specification of the other. Six additional asserted patents—U.S. Patent Nos. 6,427,194; 7,321,368; 7,542,045; 7,777,753; 8,054,315; and 8,681,164—are continuation applications of the ’459 Patent. Together, those eight patents describe inventive systems and methods for selectively allowing multiple devices, such as a CPU and an audio/video decoder, to access a shared memory. The ninth asserted patent, U.S. Patent No. 5,960,464, describes an inventive memory management system that allows a device that typically requires a large contiguous block of memory, such as a video decoder, to share noncontiguous memory with other devices.

STMicro previously asserted the ’789 Patent in a patent infringement suit against Motorola Inc. in the Eastern District of Texas, Sherman Division. As part of that case, on July 16, 2004,

¹ Most of the terms at issue here were recently briefed and argued in separate consolidated cases brought by PUMA (bus, real time, fast bus, coupled, directly supplied, display device/display adapter, and control circuit). See Parthenon Unified Memory Architecture LLC v. HTC Corp., Case Nos. 2:14-cv-690-JRG (Lead), 2:14-cv-691-JRG-RSP.

Judge Davis entered a claim construction order construing the terms “shared bus,” “real time operation” and “arbiter,” which are all implicated in the current claim construction dispute. *See STMicroelectronics, N.V. v. Motorola Inc.*, 327 F. Supp. 2d 687 (E.D. Tex. 2004). PUMA’s constructions for those terms adopt the constructions previously applied by Judge Davis, which are consistent with how the terms are used in the patent specifications and with how a person of ordinary skill in the art would interpret these common terms. In contrast, Defendants’ constructions deviate from Judge Davis’s claim construction order by incorporating extraneous concepts that are inconsistent with the intrinsic and extrinsic evidence.

For other terms, Defendants’ constructions either read out embodiments of the inventions disclosed in the patent specification and figures or improperly import limitations from the specification, whichever serves their needs at the moment. Instead of proposing constructions that adhere to the intrinsic evidence, Defendants’ claim construction efforts are an attempt to manufacture non-infringement arguments by restricting the scope of the asserted claims. Additionally, because many of Defendants’ proposed constructions insert extraneous language not found in the patents, Defendants’ constructions increase the risk of confusion.

PUMA’s constructions, on the other hand, seek to provide the Jury and the Court with guidance for understanding the elements of the claimed inventions without either restricting or broadening their true scope. Because PUMA’s proposed constructions are firmly rooted in the intrinsic and extrinsic evidence and are consistent with Judge Davis’s previous claim construction order, PUMA respectfully requests that the Court adopt its proposed constructions.

II. OVERVIEW OF PATENTED TECHNOLOGY

All of the asserted patents in this case relate to sharing memory in a computer system. The ’789 Patent, ’459 Patent, ’194 Patent, ’368 Patent, ’045 Patent, ’753 Patent, ’315 Patent, and ’164 Patent are generally directed toward novel systems and architectures that allow for multiple

devices, such as a microprocessor and an audio/video decoder, to share a computer memory. By sharing a memory, the cost of a computer system can be decreased and its efficiency increased because the individual devices no longer need their own dedicated memory and support circuitry. This, in turn, can lead to smaller consumer devices that use less battery power during operation.

The last of the nine asserted patents, the '464 Patent, describes an inventive memory management system that allows a device that would typically require a large contiguous block of memory, such as a video decoder, to share noncontiguous memory with other devices. When a video decoder shares memory with other devices, the computer system needs to make sure that the video decoder has access to a large enough chunk of contiguous memory to handle video decompression. The '464 Patent addresses this issue by effectively stitching together noncontiguous memory blocks for use by the decoder. This is accomplished by translating the noncontiguous memory addresses into a set of contiguous addresses. To the video decoder, this makes it appear as if it has access to a contiguous block of memory large enough for the video decompression process. The above inventions are discussed in detail in PUMA's technical tutorial.

III. RELEVANT LEGAL STANDARDS

The purpose of claim construction is to resolve the meanings and technical scope of claim terms. *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). Accordingly, claim construction begins with and “remain[s] centered on the claim language itself.” *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004). The construction of terms used in a patent claim is a question of law. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 391 (1996).

Claims are to be construed from the perspective of a person of ordinary skill in the art of the field of the patented invention at the time of the effective filing date of the patent application. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (*en banc*). If commonly understood

words are used in the claims, then the “ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words.” *Id.* at 1314. “Elaborate interpretation” is not required. *Id.* (citing *Brown v. 3M*, 265 F.3d 1349, 1352 (Fed. Cir. 2001)). To do otherwise would convert claim construction from “a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims,” into “an obligatory exercise in redundancy.” *U.S. Surgical*, 103 F.3d at 1568. Thus, “district courts are not (and should not be) required to construe every limitation present in a patent’s asserted claims.” *O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008).

When an ordinary meaning is not apparent, the courts look to the language of the claims, the specification, prosecution history, and extrinsic evidence such as dictionaries and treatises. *Phillips*, 415 F.3d at 1314-18. Construction begins with the language of the claim, and the court “presume[s] that the terms in the claim mean what they say.” *Power Integrations, Inc. v. Fairchild Semiconductor Int’l, Inc.*, 711 F.3d 1348, 1360 (Fed. Cir. 2013) (citing *Phillips*, 415 F.3d at 1312). Also, “the context in which a term is used in the asserted claim can be highly instructive.” *Phillips*, 415 F.3d at 1314; *see also Abtox, Inc. v. Exitron Corp.*, 122 F.3d 1019, 1023 (Fed. Cir. 1997) (“[T]he language of the claim frames and ultimately resolves all issues of claim interpretation.”).

The prosecution history may also be helpful. *Phillips*, 415 F.3d at 1317. However, “it often lacks the clarity of the specification and thus is less useful for claim construction purposes.” *Id.* Extrinsic evidence may provide guidance in some circumstances, but should not be used to “change the meaning of the claims in derogation of the indisputable public records consisting of the claims, the specification and the prosecution history.” *Id.* at 1319 (quotation marks omitted).

IV. AGREED CONSTRUCTIONS

The parties have reach agreement regarding the construction of the term “simultaneously accesses the bus” as “accesses the bus at the same time;” the term “translate” as “convert;” and the term “algorithmically translate” as “convert using at least one mathematical operation.” See Joint Claim Construction Statement, Dkt. 66 at 1.

V. TERMS FOR CONSTRUCTION

A. “bus”

Term	PUMA’s Proposal	Defendants’ Proposal
“bus”	No construction necessary. Alternatively: “a signal line or a set of signal lines to which a number of devices are coupled and over which information may be transferred”	“a signal line or set of parallel signal lines to which three or more devices are attached and over which information may be transferred to each of the three or more devices as controlled by an arbiter”

The term “bus” is widely used and understood by those of ordinary skill in the art, and the Court need not construe it. To the extent that the term needs construction, however, the Court should adopt PUMA’s proposed construction, which accurately reflects how a person of ordinary skill in the art would understand the term.

PUMA’s construction is supported by a previous case involving the ’789 patent. In that case, both the plaintiff, STMicro, and the defendant, Motorola, agreed that the term “shared bus” is “[a] signal or set of signal lines to which a number of devices are coupled and over which information may be transferred between them.” *STMicroelectronics, N.V. v. Motorola Inc.*, 327 F. Supp. 2d 687, 710 (E.D. Tex. 2004). Judge Davis adopted this agreed construction. *Id.* As explained above, the eight asserted patents that use the term “bus”—including the ’789 Patent—contain substantial overlap in their specifications, figures, and named inventors. The term “bus” is used across all eight of those patents in a manner consistent with this construction.

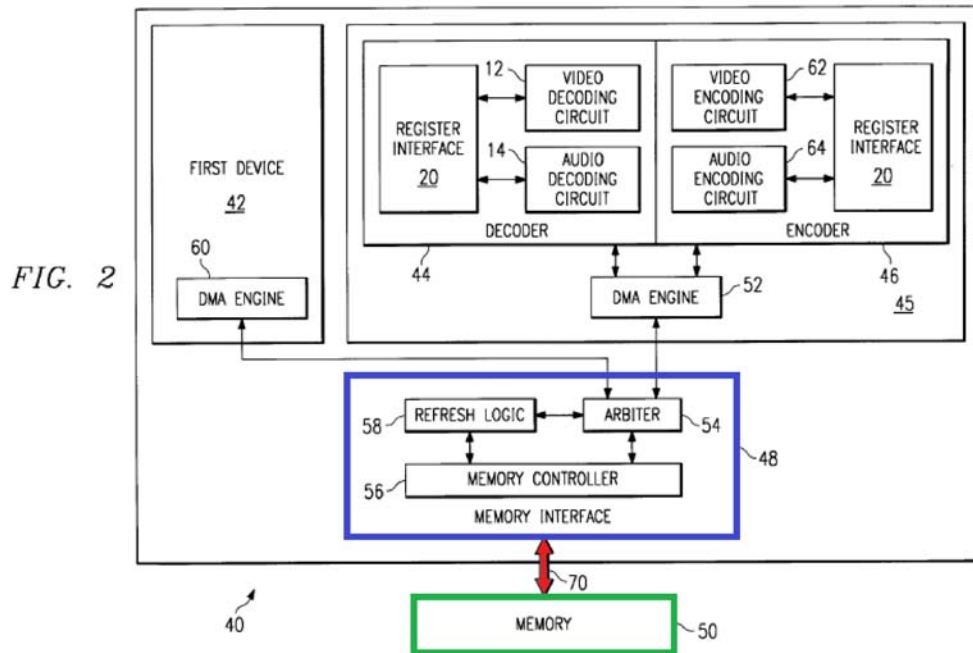
Additionally, this construction is consistent with extrinsic sources. For example, the Sixth Edition of the IEEE Standard Dictionary of Electrical and Electronics Terms, which was published contemporaneously with the filing date of the '789 Patent and the '459 Patent, defines the term "bus" as a "signal line or set of lines used by an interface system to connect a number of devices and to transfer data." *See* Ex. K, IEEE STANDARD DICTIONARY OF ELEC. & ELECS. TERMS 117 (6th ed. 1996) (definition of "bus"). To the extent a construction is necessary, PUMA requests that the Court adopt its construction for this term.

Despite the fact that STMicro and Motorola, two sophisticated semiconductor electronics companies, agreed to a construction for "bus" in the earlier case, Defendants now propose a materially different construction that uses words that do not appear in the patent specifications or prosecution histories. Defendants would require a "bus" to have a set of "parallel" signal lines that connect "three or more devices." Neither of those concepts are supported by the intrinsic evidence, and adding those limitations would only serve to confuse the Jury.

Defendants' addition of the term "parallel" is ambiguous in that it could refer either to a geometrical arrangement of the signal lines (*i.e.*, parallel lines versus perpendicular lines) or to the method of data transmission (*i.e.*, parallel data versus serial data). However, the asserted patents do not make either of those distinctions and do not use the term "parallel." As a result, a Jury would have no guidance as to what that term means in the context of Defendants' proposed construction. Any attempt by Defendants to further interpret this added term in their Response Brief cannot cure this defect: on its face, the Defendants' construction uses language that has no connection to the asserted patents, and the Jury would have no ability to apply that construction to the merits of this case. To the extent Defendants believe that the term "parallel" means something specific, then they should have proposed a construction that provides explicit and meaningful

guidance to PUMA, the Court and the Jury as to the scope of that term.

Defendants’ added requirement that a bus must be attached to “three or more devices” is also not supported by the patent specifications. For example, Figure 2 of the ‘789 patent shows “bus 70” (shown in red below) that is attached to *only* two devices: memory interface 48 (shown in blue below) and memory 50 (shown in green below). See Ex. A, Fig. 2 and 6:29–30.



Additionally, Defendants’ added requirement that information is transferred “to each of the three or more devices as controlled by an arbiter” is also not supported by the patent specifications or how a person of ordinary skill in the art would understand the term “bus.” First, Defendants’ added language would read out any bus that is not implemented with an arbiter. For example, although claim 15 of the ‘789 Patent recites a “bus,” the element of an “arbiter” is added in dependent claim 19. Ex. A at 13:36–38. Second, Defendants’ requirement that information is transferred to “each” of the devices is ambiguous. To the extent Defendants would require all attached devices to receive the transferred information, this interpretation mirrors HTC and LG’s attempt to add the term “broadcast” to the construction of “bus” in related Case No. 2:14-cv-690.

In their briefing, HTC and LG suggested that a signal line with an “intervening component” or “switch” does not “broadcast” data because it would only send data to parts of the signal line and not to all of the attached devices. *See* Case No. 2:14-cv-690, Dkt. 121 at 4. However, this would read out types of buses that were known and commonly used at the time of the asserted patents, such as the SPARC memory bus—or “MBus”—developed by Sun Microsystems circa 1991 and similar buses featuring switches, tri-state buffers, and multiplexers. *See* Ex. P at 22 (stating that the “SuperCache supports the MBus multiprocessor bus, a circuit-switch bus”). Indeed, the Defendants’ own expert, Dr. Harold Stone, characterized the MBus’s tri-state buffer as a “switch” that physically disconnects drivers from the bus so “there’s no electrical connection.” Ex. Q, Stone Depo. Trans. at 41:25-42:4. Without an electrical connection, the information is not being sent to “each” of the devices on the MBus, as required by Defendants’ construction. As a result, Defendants’ added language would read out buses using tri-state buffers or similar components that route information through the bus to various devices.

Lastly, the Defendants’ own expert, Dr. Stone, has defined “bus” in a manner that contradicts Defendants’ construction. In U.S. Patent No. 5,093,890, on which Dr. Stone is a named inventor, the term “bus” is defined as “a series of electrical lines interconnecting the modules in the computer.” Ex. L, U.S. Patent No. 5,093,890, at 1:19–21. Notably, Dr. Stone’s definition does not require “parallel” signal lines or more than three devices. As a result, the Court should reject Defendants’ overly narrow construction and adopt PUMA’s construction instead.

B. “memory bus”

Term	PUMA’s Proposal	Defendants’ Proposal
------	-----------------	----------------------

“memory bus”	No construction necessary. Alternatively: “a signal line or a set of signal lines to which a number of devices, including a memory, are coupled and over which information may be transferred”	“bus [as construed] that connects directly with a memory”
--------------	---	---

As discussed above, the term “bus” is widely used and understood by those of ordinary skill in the art, and the Court need not construe it. To the extent that the term needs construction, however, the Court should adopt PUMA’s proposed construction, which accurately reflects how a person of ordinary skill in the art would understand the term. A person of ordinary skill in the art would know that a memory bus is a bus in which one of the coupled devices is a memory.

Defendants’ proposal would require the memory to be connected “directly” to the bus. As explained above in the context of “bus,” common bus technologies like the MBus may include intervening components or interfaces that would prevent the bus from being connected “directly” to the memory. As a result, Defendants’ construction would unjustifiably read out these types of buses from the scope of the claims. Additionally, nothing in the specification suggests that the patentees intended to restrict the generic term “memory bus” in such a narrow fashion.

C. “in real time” and related terms

Term	PUMA’s Proposal	Defendants’ Proposal
“in real time”	“fast enough to keep up with an input data stream”	Indefinite. Alternatively: “fast enough to keep up with the input data stream, wherein obtaining bus mastership does not consume bus cycles”

Like the term “bus,” the term “real time” was previously construed in the earlier litigation between STMicro and Motorola involving the ’789 Patent. In that case, Judge Davis construed the term “real time operation” to mean “processing fast enough to keep up with an input data

stream.” *STMicroelectronics*, 327 F. Supp. 2d at 710. This construction, which PUMA proposes above, comports with both the intrinsic and extrinsic evidence.

The term “real time” is commonly used in the context of multimedia applications and audio/video decoding. In this regard, the patent specifications describe a number of indicia of real time operation. For example, the patent specifications state that “[i]f the decoder does not operate in **real time** the decoded movie would stop periodically between images until the decoder can get access to the memory.” Ex. A at 3:21–24 (emphasis added).

PUMA’s construction also comports with how the term “real time” is understood by persons of ordinary skill in the art. For example, the Sixth Edition of the IEEE Standard Dictionary of Electrical and Electronics Terms defines the term “real time” as “a system or mode of operation in which computation is performed during the actual time that an external process occurs.” See Ex. K, IEEE STANDARD DICTIONARY OF ELEC. & ELECS. TERMS 879 (6th ed. 1996) (definition of “real time”); see also *STMicroelectronics*, 327 F. Supp. 2d at 693. As observed by Judge Davis in the earlier litigation, “[t]he relevant dictionary definition indicates that real time concerns the processor’s ability to ‘keep up with’ the data input.” *STMicroelectronics*, 327 F. Supp. 2d at 693. For those reasons, the Court should adopt PUMA’s construction.

Despite the fact that “real time” is a common term with a well-known meaning, and despite the fact that another court in this Judicial District has already construed it without issue for the ’789 Patent, Defendants argue that this term cannot be construed. However, a claim is indefinite only if the specification and prosecution history fail to inform, with “reasonable certainty,” those skilled in the art about the scope of the invention. *Nautilus Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014). As observed by this Court, the “definiteness inquiry does not require ‘absolute precision’ because, for example, the statute ‘must take into account the inherent

limitations of language’ and ‘some modicum of uncertainty is the price of ensuring the appropriate incentives for innovation.’” *Thomas Swan & Co. v. Finisar Corp.*, Case No. 2:13-cv-178, 2014 WL 2885296, at *10 (E.D. Tex. Jun. 25, 2014) (quoting *Nautilus*).

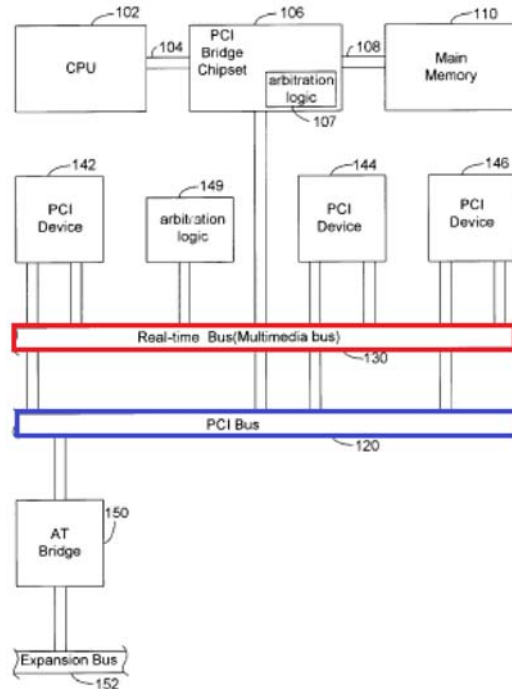
Here, the patent specifications, together with the prosecution history, inform a person of ordinary skill in the art with “reasonable certainty” of the scope of the invention. The fact that Defendants propose a different construction that is more limiting does not make the term “real time” or its earlier construction indefinite. Referring to *Nautilus*, this Court has noted that the Supreme Court “declined to adopt a test that would render a claim invalid when ‘readers could reasonably interpret the claim’s scope differently.’” *Id.* at *10. Indeed, Defendants’ own expert uses the term “real time” in a variety of his own publications without even bothering to define it, which further highlights the fact that a person of ordinary skill in the art would understand the metes and bounds of the term and the scope of the claimed inventions with “reasonable certainty.” *See* Decl. of Dr. Mangione-Smith, Ex. J at ¶¶ 13–16; Exs. M, N and O.

In the alternative, Defendants argue that the term “real time” should be construed to mean “fast enough to keep up with the input data stream, wherein obtaining bus mastership does not consume bus cycles.” This is the same construction offered by the HTC and LG defendants in their Responsive Brief in related Case No. 2:14-cv-690, and it should be rejected for the same reasons previously briefed and argued before this Court.

The language added by Defendants concerning “bus mastership” and “bus cycles” comes from a fundamental misreading of the prosecution history and the cited art. The patentees did not distinguish *Gulick*² by narrowing the ordinary scope of “real time.” Instead, the patentees distinguished *Gulick* on the basis that the PCI bus—as used in the specific context of *Gulick*—was

² U.S. Patent No. 5,812,800 (“*Gulick*”) is included as Ex. R.

insufficient for real time performance. *See* Decl. of William H. Mangione-Smith, Ex. J at ¶¶ 25–27. Defendants’ misunderstanding is readily apparent from Figure 1 of *Gulick*, shown below:



As clearly shown in Figure 1 above, *Gulick* includes a PCI bus (shown in blue) *in addition to a real-time bus* (shown in red). Ex. R, Fig. 1 (coloring added). Thus, *Gulick* itself represents that the PCI bus it was using was insufficient to guarantee real time performance for its purposes, which explains why an actual real time bus was required. Although Defendants focus on the concept of latency, this was a concern raised by *Gulick* in relation to the non-real time performance of the PCI bus as used in the context of the specific system described in *Gulick*—not a characterization of PCI buses made by the patentees in an attempt to restrict the scope of the claims. *See* Ex. J at ¶¶ 28–29. In other words, the fact that *Gulick* represents that its PCI bus was not a real time bus has nothing to do with the parameters of PCI buses in general—such as bus mastership or bus cycles—but rather with the specific context in which the PCI bus was used in *Gulick*. As it was used and described in *Gulick*, the PCI bus could not process data fast enough to keep up with *Gulick*’s input data stream.

For the related terms reciting a “sufficient bandwidth to enable the decoder to access the memory and operate in real time,” the parties’ arguments and positions appear to depend entirely on the dispute over the term “real time.” PUMA respectfully requests that the Court adopt its constructions for the related terms.

D. “fast bus”

Term	PUMA’s Proposal	Defendants’ Proposal
“fast bus”	“bus with a bandwidth equal to or greater than the required bandwidth to operate in real time”	Indefinite. Alternatively: “bus [as construed] having a bandwidth sufficient to allow real time operation”

The Court should adopt PUMA’s proposed construction of “fast bus” because it is the very definition that the patentee provided in the asserted patents: “A **fast bus** 70 is any bus whose bandwidth is equal to or greater than the required bandwidth.” Ex. B at 8:1–2 (emphasis added). Similarly, the patent specifications state that “two devices are coupled to the memory through a fast bus having a bandwidth of *at least the minimum bandwidth* needed for the video and/or audio decompression and/or compression device to operate in real time.” *Id.* at 4:59–62 (emphasis added). The specification is “the single best guide to the meaning of a disputed term,” and the explicit definition of “fast bus” in the specification should be adopted as the term’s construction. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

Defendants’ initial argument is that the term “fast bus” is indefinite, presumably because of the specification’s reference to the term “real time.” But as explained above with respect to “real time,” this term is not indefinite and a person of ordinary skill in the art would understand the meaning of “real time” with reasonable certainty. For those same reasons, Defendants’ indefiniteness argument should be rejected.

Defendants' alternative construction, although similar to PUMA's proposed construction, does not track the explicit language used in the specification to define the term and is less clear as to its meaning. For example, replacing the phrase "equal to or greater than" with "sufficient" would not assist the Jury. As a result, the Court should reject Defendants' construction.

E. "coupled," "coupleable" and "coupling"

Term	PUMA's Proposal	Defendants' Proposal
a. "coupled"	a. "directly or indirectly connected"	a. Plain and ordinary meaning. No construction necessary.
b. "coupleable"	b. "directly or indirectly connectable"	b. Plain and ordinary meaning. No construction necessary.
c. "coupling"	c. "directly or indirectly connecting"	c. Plain and ordinary meaning. No construction necessary.

The term "coupled" is commonly understood and has routinely been construed by district courts to mean directly or indirectly connected. *See, e.g., Negotiated Data Solutions, LLC v. Dell, Inc.*, 596 F. Supp. 2d 949 (E.D. Tex. 2009) ("the court defines 'coupled' to mean the following: 'connected directly or indirectly'"); *GSK Tech. Inc. v. Eaton Elec. Inc.*, Case No. 6:06-cv-358, 2008 WL 906713, at *5 (E.D. Tex. Apr. 1, 2008) (construing "electrically coupled" to mean "arranged so that electrical signals may be passed either directly, or indirectly via intervening circuit, from one component to another"); *O2 Micro, Int'l, Ltd. v. Rohm Co., Ltd.*, Case No. 2:05-cv-211, 2007 WL 4116803, at *4 (E.D. Tex. Nov. 6, 2007) (noting that the court "previously construed the term 'coupled' to mean 'electrically connected, directly or indirectly.'").

This common construction comports exactly with how the patentees used the term in the asserted patents. For example, referring to Figure 1b, the '789 Patent states that the "memory interface 18 is **coupled** to a memory 22." Ex. A at 2:25 (emphasis added). As illustrated in Figure 1b below, the memory interface 18 (shown in red) is connected *indirectly* to the memory 22 (shown in blue) through at least the audio decoding circuit 14 (shown in green).

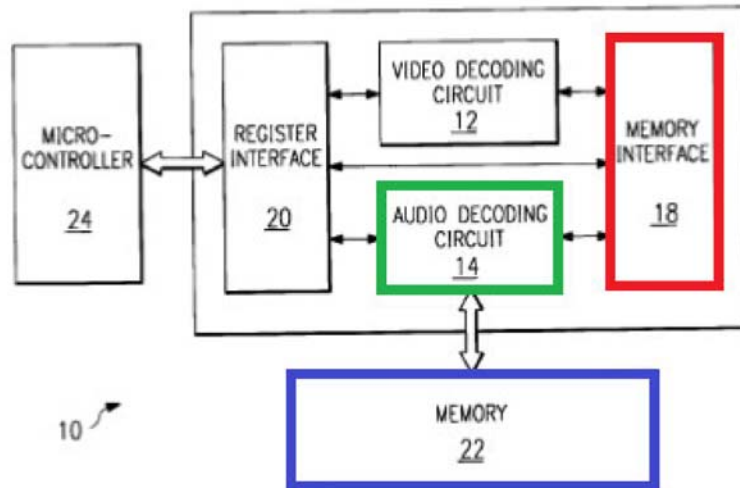


FIG. 1b
(PRIOR ART)

Similarly, referring to Figure 2, the '789 Patent states that the “decoder/encoder 45 is **coupled** to the memory 50 *through devices*, typically a bus 70.” *Id.* at 6:29–32 (emphasis added). As illustrated in Figure 2, the decoder/encoder 45 (shown in red) is connected *indirectly* to the memory 50 (shown in blue) through at least the memory interface 48 (shown in green) and bus 70.

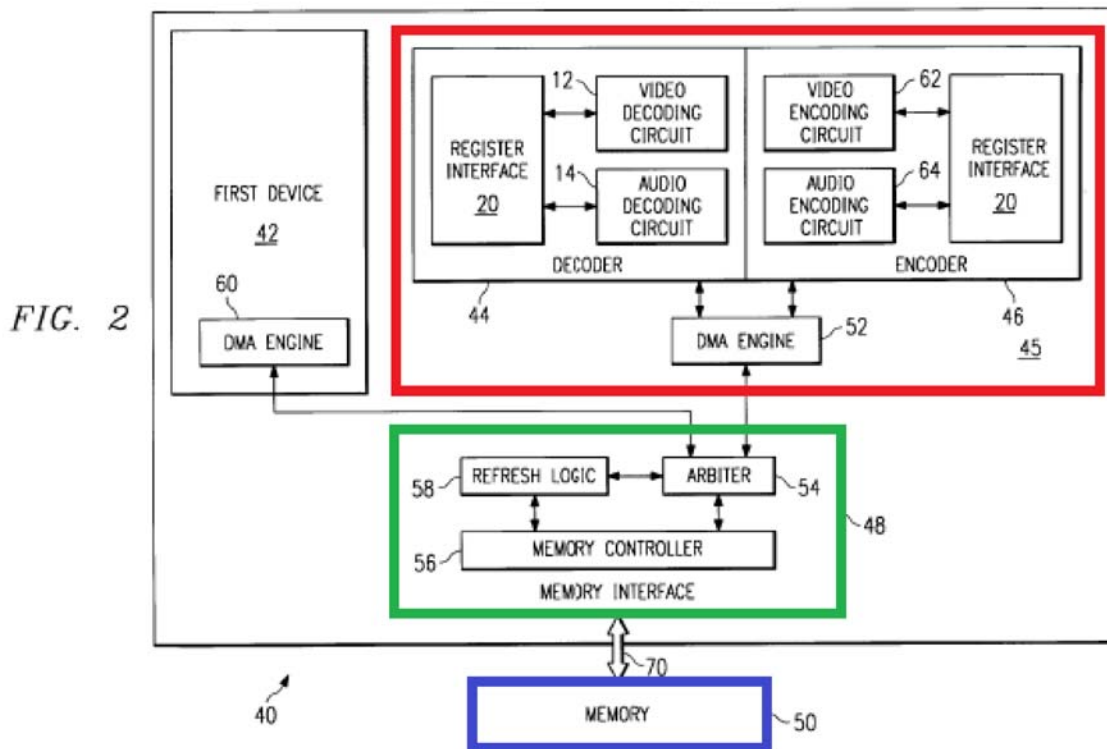


FIG. 2

The '459 Patent and the other related patents contain similar passages. *See* Ex. B at 2:28 and 7:39–42. The patents also use the term “coupled” to refer to direct connections. For example, referring to Figure 2 above, the '789 Patent states that the “DMA engine 60 of the first device 42 is **coupled** to the arbiter 54 of the memory interface 48.” Ex. A at 6:15–17 (emphasis added).

Defendants do not appear to dispute that the term “coupled” includes both direct and indirect connections. Instead, Defendants suggest that “no construction is necessary” for the coupled terms because their plain and ordinary meaning is readily apparent. However, given that the HTC and LG defendants in related Case No. 2:14-cv-690 disagreed with the plain and ordinary meaning of “coupled” and proposed an alternative construction, PUMA respectfully requests that the Court construe the “coupled” terms in both sets of cases.

F. “directly supplied” and “directly supplies”

Term	PUMA’s Proposal	Defendants’ Proposal
“directly supplied/supplies”	“supplied/supplies without being stored in main memory for purposes of decoding subsequent images”	“supplied/supplies without intervening components”

The term “directly supplied” concerns the system’s use of decompressed frames in the context of video decoding and does not require the absence of “intervening components.” In fact, the asserted patents disclose embodiments involving multiple buses and additional “intervening components.”

For example, Figure 3 of the '194 Patent illustrates one of the embodiments of the claimed invention. As can be seen in Figure 3 below, the Decoder/Encoder 80 (shown in added blue) is connected to the Graphics Accelerator 200 and the Display 182 (shown in added red) through the Core Logic Chipset 190 (shown in added green). Under Defendants’ construction, this embodiment would be read out of the claims because of the intervening Core Logic Chipset 190

component. In this embodiment, any frames supplied from the video decoder to the display would necessarily need to pass through *multiple* components and buses.

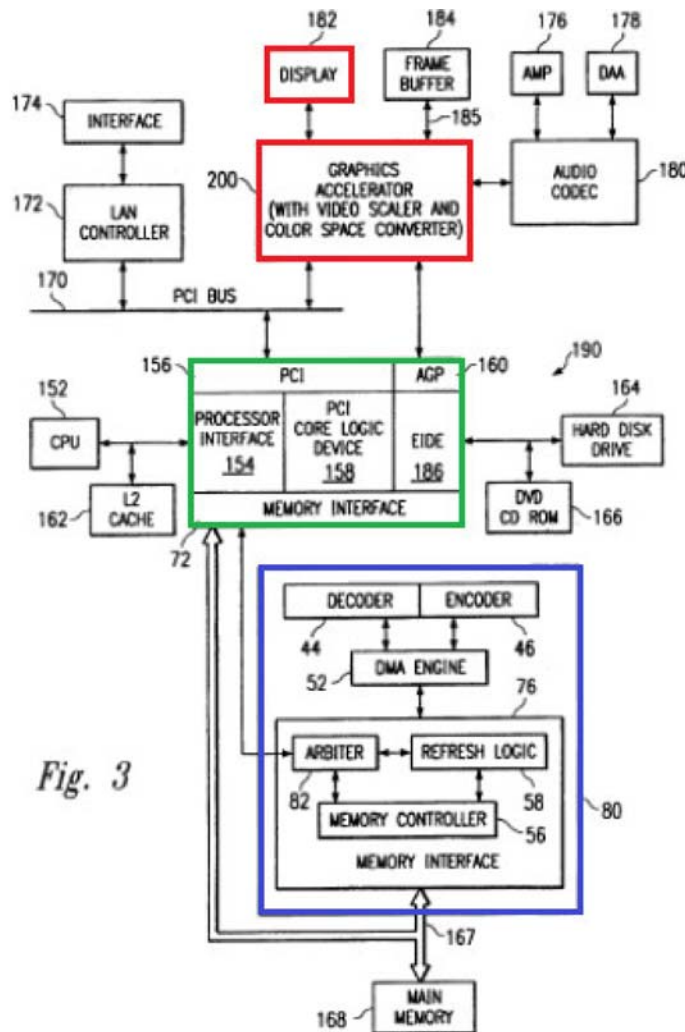


Fig. 3

Instead, the phrase “directly supplied” concerns the fact that certain types of frames do not need to be transferred to main memory for use in the subsequent decoding of other frames. Dependent claim 14 of the ’194 Patent states that the “decoder **directly supplies** a display adapter of the display device with an image **for use other than decoding a subsequent image.**” Dkt. 120, Ex. C at 16:65–67 (emphasis added). Similarly, dependent claim 15 states that “the images **directly supplied** to the display adapter [are] **bidirectional images** obtained from two preceding intra and predicted images.” *Id.* at 17:4–6 (emphasis added). The ’194 Patent states that the “intra

and predicted images are likely to be used to reconstruct subsequent predicted and bidirectional images, while **the bidirectional images are not used again.**” *Id.* at 3:22–25 (emphasis added).

For this reason, “**a buffer associated with bidirectional images is not required**, these bidirectional images B being **directly supplied** to display adapter 120 as they are being decoded.” *Id.* at 10:39–42 (emphasis added). Thus, the term “directly supplied” must be viewed in the context of bidirectional frames, which do not need to be stored in main memory for purposes of decoding other images. PUMA’s construction properly captures this concept.

G. “display device” and “display adapter

Term	PUMA’s Proposal	Defendants’ Proposal
“display device”	“screen and associated display circuitry”	“a device for displaying images or video, such as a screen”
“display adapter”	No construction necessary. Alternatively: “a circuit for processing images”	“an adapter that processes images for a display device such as a screen”

PUMA does not oppose construing “display device” as “a device for displaying images or video, such as a screen.” However, the parties’ dispute appears to be over what the word “screen” connotes in the context of that construction. Defendants appear to seek to restrict the term to the narrowest of possibilities—the physical screen—despite the fact that no person of ordinary skill in the art would interpret “display device” in such a restrictive manner.

The claim language states that the display device has “access” to the main memory “subject to a display device access control.” Dkt. 120, Ex. C at 15:51–53. Logically, the physical screen must be accompanied by circuitry that accesses the main memory. Claim 12 of the ’194 Patent recites “wherein the display device is either a chipset or a graphics accelerator,” which unambiguously confirms that the term “display device” connotes more than the physical screen.

Id. at 16:62. The patentees were not attempting to restrict “display device” in an overly-narrow manner, but rather provide general examples of *devices* for displaying images—such as screens, projectors, televisions, or computer monitors and the associated circuitry that enables the displaying of images.

H. “arbiter” terms

Term	PUMA’s Proposal	Defendants’ Proposal
a. “arbiter”	“circuitry that uses a priority scheme to determine which requesting device will gain access”	“a component that controls direct access without multiplexing inputs”
b. “arbitration circuit”		
c. “memory arbiter”		
d. “arbiter circuit”		

Like the terms “bus” and “real time,” the term “arbiter” was previously construed by Judge Davis in the earlier litigation involving STMicro and Motorola, namely as “a device that use[s] a priority scheme to determine which requesting device will gain access to the memory.” *STMicroelectronics*, 327 F. Supp. 2d at 710. In fact, STMicro and Motorola, both sophisticated semiconductor corporations, jointly submitted the above construction despite the prosecution history that Defendants now purport to rely upon. This construction comports with how the term is used in the patents and how a person of ordinary skill in the art would understand arbitration. PUMA simply has applied that same construction to the above “arbitration” terms.

In contrast, Defendants seek to narrow the meaning of the term to a “component that controls direct access without multiplexing inputs” even though that definition appears nowhere in the patent specifications or prosecution history. Defendants appear to rely heavily on an excerpt from the file history for the ’459 Patent. As an initial matter, Defendants’ proposal is facially problematic because it would seek to construe the arbiter terms for *all of the asserted patents*, not

just the '459 Patent. However, looking solely at the prosecution history for the '459 Patent, Defendants' construction is not justified for *any* of the asserted patents.

For example, Defendants cite to the Examiner's rejection of the then-pending claims of the '459 Patent application in support of their construction. In response to that rejection, the patentees amended the then-pending claims to add language concerning "direct access" and a requirement that "the arbiter [is] configured to determine which of at least the first device and the decoder receives direct access" to the memory. Ex. S at 2–8. The patentees did not redefine the term "arbiter" but rather added other surrounding language to traverse the cited art. More importantly, neither the then-pending claims nor the amended claims made it to allowance. In response to a subsequent office action raising other rejections, the patentees *canceled all of the pending claims* and wrote a new set of claims that would become the claims of the '459 Patent. Ex. T at 1. That new set of claims contains its own elements, including the requirement of "without also requiring a second bus," and does not use the "direct access" phrase that Defendants rely upon to change the meaning of the term "arbiter." As a result, Defendants' attempt to import that limitation into the actual resulting claims of the '459 Patent is improper and should be rejected.

I. "control circuit"

Term	PUMA's Proposal	Defendants' Proposal
"control circuit"	No construction necessary.	"an electronic control device that is separate from the CPU or processor and that interacts with the operating system"

The Court does not need to construe "control circuit" because the term is effectively defined by the surrounding claim language. For example, claim 1 of the '464 patent specifies that the "control circuit" is coupled to the decoding circuit, the processor, and the main memory. Ex. I at 9:66–10:6. Claim 1 further describes that the "control circuit" is configured to "request

continuous use of several portions of the main memory from the operating system” and “translate the noncontiguous addresses to contiguous addresses of a block of memory.” *Id.* Because “the claim language already provides substantial guidance as to the meaning of the claim terms, the plain and ordinary meaning of the claim language controls” and no construction of the term “control circuit” is necessary. *Uniloc USA, Inc. v. Imagine Corp.*, Case No. 6:12-cv-93, 2013 WL 3871360, at *4 (E.D. Tex. Jul. 24, 2013).

Defendants’ proposed construction suffers from several flaws. First, the substitution of “device” for “circuit” is unhelpful and provides “no meaningful guidance as to the meaning of the term.” *UltimatePointer, L.L.C. v. Nintendo Co.*, Case No. 6:11-cv-496, 2013 WL 2325118, at *14 (E.D. Tex. May 28, 2013). Second, requiring that the “control circuit” be “separate” from the CPU or processor would only lead to jury confusion over the alleged boundaries between the claim elements. The specification does not define what “separate” means in the context of the patent, and inclusion of this term would lead to less clarity. Moreover, because “the CPU” is not used in the claims that include the term “control circuit,” Defendants’ addition of this term would add further confusion for the Jury. In essence, Defendants seek to impose a nineteen-word definition on a two-word term, despite the fact that the surrounding claim language gives proper guidance as to the meaning and scope of the term “control circuit.” For the above reasons, the Court should decline to construe the term.

J. “monolithically integrated into” and “integrated into”

Term	PUMA’s Proposal	Defendants’ Proposal
“monolithically integrated into” and “integrated into”	“formed on a single semiconductor chip with”	“formed within”

Although not explicitly defined in the asserted patents, the concept of monolithic integration is well-understood by a person of ordinary skill in the art. The term “monolithic”

originates from the Greek words *monos* ‘single’ and *lithos* ‘stone.’ In the context of semiconductor circuits, this means that the components are formed on a single semiconductor crystal. For example, the Modern Dictionary of Electronics states that “a monolithic semiconductor integrated circuit has all circuit components manufactured on top of a single crystal semiconductor material.” Ex. U at 637 (entry for “monolithic circuit”). Similarly, the IBM Dictionary of Computing defines “Monolithic Technology” as “a technology in which all electronic components of a circuit, such as transistors, diodes, resistors, and capacitors, are integrated into one chip.” Ex. V at 440 (entry for “monolithic technology”). The Dictionary of Scientific and Technical Terms echoes this concept by defining a “Monolithic Integrated Circuit” as “an integrated circuit having elements formed in place on or within a semiconductor substrate.” Ex. W at 1294 (entry for “monolithic integrated circuit”). PUMA’s proposed construction is based on the common meaning of the term monolithic by stating that the integrated components are “formed on a single semiconductor chip.”

In contrast, Defendants’ term substitutes the relatively clear concept of “formed on a single semiconductor chip” with the much more ambiguous concept of “formed within.” However, two components can be monolithically integrated on the same semiconductor chip without one component being “formed within” the physical footprint of the other component. The purpose of “monolithic integration” is to reduce costs and promote the efficient use of space by building multiple components on the same piece of silicon. Defendants’ construction ignores that fundamental purpose and would unnecessarily require some overlapping of physical layouts. However, this would compel the Jury to make arbitrary determinations of where the physical boundaries of various components begin and end and whether one component is “formed within” another component. As a result, Defendants’ construction narrows the concept of monolithic integration well beyond how a person of ordinary skill in the art would understand the term.

K. “contiguous” and “non-contiguous”

Term	PUMA’s Proposal	Defendants’ Proposal
a. “contiguous”	No construction required.	a. “adjacent”
b. “non-contiguous”		b. “non-adjacent”

The terms “contiguous” and “non-contiguous” are used in the ‘464 Patent in the context of memory addresses. As such, a person of ordinary skill in the art would understand the meaning of these terms, and the Court need not construe the terms. *See, e.g., UltimatePointer, L.L.C. v. Nintendo Co., Ltd.*, 2013 WL 2325118, *14 (E.D. Tex. May 28, 2013) (“Substituting ‘separation’ for ‘distance’ provides no meaningful guidance as to the meaning of the term. . . . Therefore, no construction is necessary for these terms.”).

Defendants’ proposed constructions does not add any clarity or guidance to the meaning of “contiguous” or “non-contiguous.” In fact, by substituting the terms “adjacent” and “non-adjacent” into the claim language, Defendants’ constructions run the risk of improperly changing the claim scope and confusing the Jury. For example, the term “adjacent” may connote a geographic proximity: the federal courthouse in Marshall is “adjacent” to the Baxter Building. As a result, from the Defendants’ substitution of “adjacent,” the Jury may mistakenly conclude that “contiguous” memory addresses require the corresponding memory cells on the actual memory chip to be in geographic or physical proximity in order to satisfy the claim language. This would improperly exclude systems where contiguous memory *addresses* are not physically adjacent on the memory chip. For example, the Baxter Building in Marshall is at 104 E. Houston St. and the OS² Restaurant & Pub in Marshall is at 105 E. Houston St. However, a Jury may conclude that the Baxter Building is not “adjacent” to the OS² Restaurant & Pub because of the Harrison County Courthouse located between them and their physical separation.

L. “direct memory access (DMA) engine” and “direct memory access engine”

Term	PUMA’s Proposal	Defendants’ Proposal
a. “direct memory access (DMA) engine” b. “direct memory access engine”	No construction required.	“a block transfer processor that transfers data between an external device and a memory without interrupting program flow or requiring CPU intervention”

The term “DMA engine” is a term-of-art that is commonly used in the field of computer design and readily understood by a person of ordinary skill in the art. Ex. J at ¶ 30. As such, no construction is necessary. In contrast, Defendants propose a hyper-detailed construction of this term-of-art that spans twenty-two words and does nothing to assist either a person of ordinary skill in the art or the Jury in applying the claim language to the merits of the case. Because the asserted patents do not reference or explain concepts like a “block transfer processor” or “interrupting program flow” or “requiring CPU intervention,” the Jury would be in a worse position in terms of clarity and understanding. For that reason, the Court should decline to provide a construction for this common term-of-art.

M. “refresh logic”

Term	PUMA’s Proposal	Defendants’ Proposal
“refresh logic”	No construction required.	“logic to repeat the storage of data to keep it from becoming lost”

Like the term “DMA engine” above, the term “refresh logic” is commonly used in the field of computer design and readily understood by a person of ordinary skill in the art. The general purpose of refresh logic is to refresh the contents of a dynamic random access memory (DRAM) to compensate for charge leakage in the memory cells. Because the concept is readily understood by a person of ordinary skill in the art, no construction is necessary.

In contrast, Defendants propose a construction that adds ambiguity to the claim language. For example, the asserted patents do not discuss what it means to “repeat the storage of data” or what it means to “keep [data] from being lost.” Although Defendants may not intend for this added language to change the plain and ordinary meaning of the term “refresh logic,” transforming an easily-understood two-word term into a thirteen-word definition runs the risk of unnecessarily complicating the task of the Jury and should be rejected.

N. “[first, second, third] onboard memory”

Term	PUMA’s Proposal	Defendants’ Proposal
“[first, second, third] onboard memory”	No construction required.	“[first, second, third] memory within the decoder”

The term “onboard memory” does not need to be construed because the meaning is straightforward: the memory is on-board. Although the term “onboard” is not explicitly used in the specification, the ’315 Patent discusses the terms “motherboard” and “removable boards.” Ex. G at 2:66-67. Thus, in the context of the claim language, which discusses an “image decoder circuit” that includes “onboard memory,” a person of ordinary skill in the art would understand the above term to refer to memory that is on the board with the decoder, as opposed to a memory that is on a separate circuit board.

In contrast, Defendants propose a construction that incorrectly requires the memory to be “within the decoder.” A memory can be located on the same circuit board as the decoder without being “within” the decoder. As a result, Defendants’ construction should be rejected.

VI. CONCLUSION

PUMA requests that the Court adopt its proposed claim constructions because its proposed constructions adhere to the language set out in the patents themselves and represent how these terms would be understood by a person of ordinary skill in the art.

Dated: June 18, 2015

Respectfully submitted,

/s/ Demetrios Anaipakos

Demetrios Anaipakos
Texas Bar No. 00793258
danaipakos@azalaw.com

Amir Alavi
Texas Bar No. 00793239
aalavi@azalaw.com

Michael McBride
Texas Bar No. 24065700
mmcbride@azalaw.com

Alisa A. Lipski
Texas Bar No. 24041345
alipski@azalaw.com

Justin Chen
Texas Bar No. 24074204
jchen@azalaw.com

AHMAD, ZAVITSANOS, ANAIPAKOS,
ALAVI & MENSING P.C.

1221 McKinney Street, Suite 3460
Houston, TX 77010
Telephone: 713-655-1101
Facsimile: 713-655-0062

T. John Ward, Jr.
Texas Bar No. 00794818
jw@wsfirm.com
WARD & SMITH LAW FIRM
P.O. Box 1231
Longview, TX 75606-1231
Telephone: 909-757-6400
Facsimile: 909-757-2323

**ATTORNEYS FOR PLAINTIFF
PARTHENON UNIFIED MEMORY
ARCHITECTURE LLC**

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on June 18, 2015.

/s/ Michael McBride _____