ISSUE CLASSIFICATION

Class	Subclass
395	200.77

[redacted]

5812789

UTILITY SERIAL NUMBER 08/702911	PATENT DATE SEP 22 1998	PATENT NUMBER 5812789

SERIAL NUMBER	FILING DATE	CLASS	SUBCLASS	GROUP ART UNIT	EXAMINER
08/702,911	08/26/96	395	~~200.18~~ 200.77	2756	E. RAMIREZ

APPLICANTS

RAUL Z. DIAZ, PALO ALTO, CA; JEFFERSON E. OWEN, FREEMONT, CA.

395/200.77

CONTINUING DATA*******************
VERIFIED

No

FOREIGN/PCT APPLICATIONS**********
VERIFIED

No

FOREIGN FILING LICENSE GRANTED 10/29/96

Foreign priority claimed / 35 USC 119 conditions met / Verified and Acknowledged	☐ yes ☑ no / ☐ yes ☑ no / Examiner's initials	AS FILED	STATE OR COUNTRY	SHEETS DRWGS.	TOTAL CLAIMS	INDEP. CLAIMS	FILING FEE RECEIVED	ATTORNEY'S DOCKET NO.
			CA	5	49	5		96-S-11

ADDRESS

LISA K. JORGENSON
SGS THOMSON MICROELECTRONICS INC
1310 ELECTRONICS DRIVE
CARROLLTON TX 75006

TITLE

VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE

U.S. DEPT. of COMMERCE • Patent and Trademark Office–PCT-436L (rev. 7-94)

PARTS OF APPLICATION FILED SEPARATELY		4/10/98 Applications Examiner
NOTICE OF ALLOWANCE MAILED: 3/30/98	Assistant Examiner	CLAIMS ALLOWED — Total Claims: 33; Print Claim: 1
ISSUE FEE — Amount Due: $1320.00; Date Paid: 7/2/98	ELLIS B. RAMIREZ PRIMARY EXAMINER — Primary Examiner	DRAWING — Sheets Drwg.: 5; Figs. Drwg.: 6; Print Fig.: 2
Label Area	PREPARED FOR ISSUE	ISSUE BATCH NUMBER: C25

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

Form PTO-436A
(Rev. 8/92)

ISSUE FEE IN FILE

(FACE)

08/702911

PATENT APPLICATION

08702911

APPROVED FOR LICENSE

INITIALS

SEP 25 96 5

CONTENTS

Date Entered or Counted			Date Received or Mailed
	1.	Application 5 papers.	
	2.	IDS	11-4-96
	3.	IDS	11-19-96
	4.	Petition to Secure Filing (411)	7/8/97
	5.	Date Petition dismissed (411)	8/11/97
9.2.97	6.	BES(3)	9/3/97
	7.	~~Extension of time (3)~~	3/9/98 cm 3/3/98
	8.	~~Amendment A~~	3/9/98 cm 3/3/98
	9.	Notice of Allowability	3/30/98
	10.	Supple. Notice of Allow	4/10/98
7/13/98	11.	Formal Drawings (5 shts) cat 1	6/29/98
	12.	PTO Grant SEP 22 1998	
9/22/98	13.	SUP DEC	6/29/98
	14.		
	15.		
	16.		
	17.		
	18.		
	19.		
	20.		
	21.		
	22.		
	23.		
	24.		
	25.		
	26.		
	27.		
	28.		
	29.		
	30.		
	31.		
	32.		

(FRONT)

Staple Issue Slip Here

POSITION		ID NO.	DATE
CLASSIFIER		12	9/25/96
EXAMINER		390	10-4-
TYPIST	Struck	318	10/29/96 445
VERIFIER		446	10/
CORPS CORR.			
SPEC. HAND			
FILE MAINT.			
DRAFTING			

INDEX OF CLAIMS

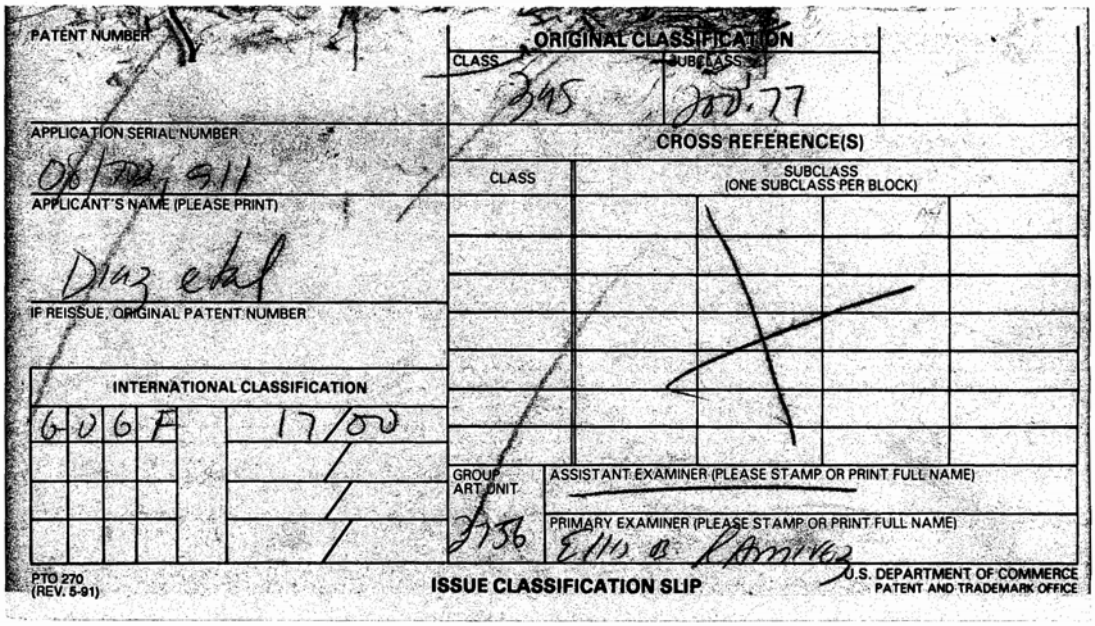
Claim Final	Claim Original	Date
1	14	=
2	15	
3	16	
4	17	
5	18	
6	19	
7	20	
8	21	
9	22	
10	23	
11	24	
12	25	
13	26	
14	27	
15	28	
16	29	
17	30	
18	31	
19	32	
20	33	
21	34	
22	35	
23	36	
24	37	
25	38	
26	39	
27	40	
28	41	=
	42	
	43	
29	44	
30	45	=
31	46	
32	47	
33	48	=
	49	
	50	

SYMBOLS

- ✓ ..... Rejected
- = ... Allowed
- - (Through numberal) Canceled
- + ... Restricted
- N ..... Non-elected
- I ..... Interference
- A ..... Appeal
- O ..... Objected

Claim Final	Claim Original	Date
	51	
	52	
	53	
	54	
	55	
	56	
	57	
	58	
	59	
	60	
	61	
	62	
	63	
	64	
	65	
	66	
	67	
	68	
	69	
	70	
	71	
	72	
	73	
	74	
	75	
	76	
	77	
	78	
	79	
	80	
	81	
	82	
	83	
	84	
	85	
	86	
	87	
	88	
	89	
	90	
	91	
	92	
	93	
	94	
	95	
	96	
	97	
	98	
	99	
	100	

(LEFT INSIDE)



PATENT NUMBER

ORIGINAL CLASSIFICATION

CLASS 345 SUBCLASS 207.77

APPLICATION SERIAL NUMBER 08/[illegible],911

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)

APPLICANT'S NAME (PLEASE PRINT)

Diaz et al

IF REISSUE, ORIGINAL PATENT NUMBER

INTERNATIONAL CLASSIFICATION

G 06 F 17/00

GROUP ART UNIT 2736

ASSISTANT EXAMINER (PLEASE STAMP OR PRINT FULL NAME)

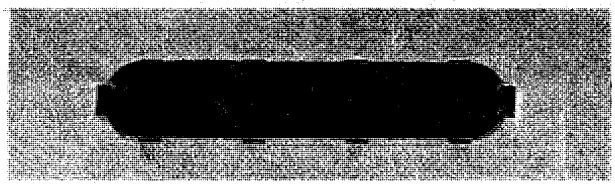
PRIMARY EXAMINER (PLEASE STAMP OR PRINT FULL NAME)

Ellis B. Ramirez

PTO 270 (REV. 5-91)

ISSUE CLASSIFICATION SLIP

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE



SEARCHED

Class	Sub.	Date	Exmr.
395	200.77	8/20/17	Q
	200.82		
	507		
	890		
	729		
348	402		
	407		
	10	8/20/17	Q
	Updated	3/26/18	Q

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
395	200.77	3/26/18	Q

SEARCH NOTES

	Date	Exmr.

(RIGHT OUTSIDE)

08/702911

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

340 BA 19-1353 10/28/96 08702911
34011 101 188.00CH

340 TL 10/02/96 08702911
1 101 1,356.00 CK

PTO-1556
(5/87)

IR/702911

SGS-THOMSON MICROELECTRONICS

August 23, 1996

THE ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Re: Inventor(s): Raul Z. Diaz and Jefferson E. Owen

For: Video and/or Audio Decompression and/or Compression Device that Shares a Memory Interface

Our File No: 96-S-11

Sir:

Enclosed with this transmittal letter are:

(1) Subject patent application with Declaration and Power of Attorney;
(2) Five (5) sheets of informal drawings;
(3) Certificate of Express Mail;
(4) Assignment and Recordation Cover Sheet;
(5) Check in the amount of $1,396.00;
(6) Return postcard which we would appreciate your date stamping and returning to us upon receipt;

The total filing fee has been calculated as follows:

Basic fee	=	$ 750.00
Recordation of Assignment	=	40.00
29 claims in excess of 20	=	638.00
2 independent claim in excess of 3	=	156.00
Total filing fee	=	$1.584.00

I authorize the Commissioner to charge any additional fees which may be required, or credit any overpayment to Account No. 19-1353. A duplicate copy of this sheet is enclosed.

Irena Lager
Reg. No. 39,260

SGS-THOMSON Microelectronics, Inc. • 1310 Electronics Drive • Carrollton, TX 75006-5039
Telephone (214) 466-6000, Telex 730643

ST002-CAR

08/709911

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. 96-S-011

In Re Application of:

Raul Z. Diaz and Jefferson E. Owen

For: **Video and/or Audio Decompression and/or Compression Device that Shares a Memory Interface**

CERTIFICATE OF EXPRESS MAIL

"EXPRESS MAIL" NO. EG947362259US

Date of Deposit: August 23, 1996

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Signature of person mailing paper or fee

5

1,356.00

08/702911

VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE

Cross-reference to Related Applications

This application contains some text and drawings in common with pending U.S. Patent Applications entitled: "Video and/or Audio Decompression and/or Compression Device that Shares a Memory" by Jefferson E. Owen, Raul Z. Diaz, and Osvaldo Colavin S/N 08/702,913 Filed on 08/26/96 (~~Attorney's Docket No. 96-S-012~~), and has the same effective filing date and ownership as the present application, and to that extent is related to the present application, which is incorporated herein by reference.

Background

The present invention relates to the field of electronic systems having a video and/or audio decompression and/or compression device, and is more specifically directed to sharing a memory interface between a video and/or audio decompression and/or compression device and another device contained in the electronic system.

The size of a digital representation of uncompressed video images is dependent on the resolution, and color depth of the image. A movie composed of a sequence of such images, and the audio signals that go along with them, quickly becomes large enough so that uncompressed such a movie typically cannot fit entirely onto conventional recording medium, such as a CD. It is also typically

now prohibitively expensive to transmit such a movie uncompressed.

It is therefore advantageous to compress video and audio sequences before they are transmitted or stored. A great deal of effort is being expanded to develop systems to compress these sequences. There are several coding standards currently used that are based on the discrete cosine transfer algorithm including MPEG-1, MPEG-2, H.261, and H.263. (MPEG stands for "Motion Picture Expert Group", a committee of the International Organization for Standardization, ISO.) The MPEG-1, MPEG-2, H.261, and H.263 standards are decompression protocols that describe how an encoded bitstream is to be decoded. The encoding can be done in any manner, as long as the resulting bitstream complies with the standard.

Video and/or audio compression devices (hereinafter encoders) are used to encode the video and/or audio sequence before it is transmitted or stored. The resulting bitstream is decoded by a video and/or audio decompression device (hereinafter decoder) before the video and/or audio sequence is displayed. However, a bitstream can only be decoded by a decoder if it complies to the standard used by the decoder. To be able to decode the bitstream on a large number of systems it is advantageous to encode the video and/or audio sequences to comply to a well accepted decompression standard. The MPEG standards are currently well accepted standards for one way communication. H.261, and H.263 are currently well accepted standards for video telephony.

Once decoded the images can be displayed on an electronic system dedicated to displaying video and audio, such as television or digital video disk (DVD) player, or on electronic systems where image display is just one feature of the system, such as a computer. A decoder needs to be added to these systems to

allow them to display compressed sequences, such as received images and associated audio, or ones taken from a storage device. An encoder needs to be added to allow the system to compress video and/or audio sequences, to be transmitted or stored. Both need to be added for two way communication such as video telephony.

A typical decoder, such as an MPEG decoder 10 shown in Figure 1a, contains video decoding circuitry 12, audio decoding circuitry 14, a microcontroller 16, and a memory interface 18. The decoder can also contain other circuitry depending on the electronic system the decoder is designed to operate in. For example, when the decoder is designed to operate in a typical television the decoder will also contain an on screen display (OSD) circuit.

Figure 1b shows a better decoder architecture, used in the STi3520 and STi3520A MPEG Audio/MPEG-2 Video Integrated Decoder manufactured by SGS-THOMSON Microelectronics. The decoder has a register interface 20 instead of a microcontroller. The register interface 20 is coupled to an external microcontroller 24. The use of a register interface 20 makes it possible to tailor the decoder 10 to the specific hardware the decoder 10 interfaces with or change its operation without having to replace the decoder by just reprogramming the register interface. It also allows the user to replace the microcontroller 24, to upgrade or tailor the microcontroller 24 to a specific use, by just replacing the microcontroller and reprogramming the register interface 20, without having to replace the decoder 10.

The memory interface 18 is coupled to a memory 22. A typical MPEG decoder 10 requires 16 Mbits of memory to operate in the main profile at main

level mode (MP at ML). This typically means that the decoder requires a 2Mbyte memory. Memory 22 is dedicated to the MPEG decoder 10 and increases the price of adding a decoder 10 to the electronic system. In current technology the cost of this additional dedicated memory 22 can be a significant percentage of the cost of the decoder.

An encoder also requires a memory interface 18 and dedicated memory. Adding the encoder to an electronic system again increases the price of the system by both the price of the encoder and its dedicated memory.

A goal in the semiconductor industry is to reduce the die area of an integrated circuit device for a given functionality. Some advantages of reducing the die area is the increase in the number of the die that can be manufactured on same size silicon wafer, and the reduction in price per die resulting therefrom. This results in both an increase in volume and reduction in price of the device.

Many of the functional circuits described above for Figure 1a and Figure 1b take up a lot of die space. However, each of them is needed to make the respective decoder operate.

Figure 1c shows a computer 25 containing a decoder 10, a main memory 168 and other typical components such as a modem 199, and graphics accelerator 188. The decoder 10 and the rest of the components are coupled to the core logic chipset 190 through a bus 170. The bus is typically a PCI (peripheral component interface) or ISA (industry standard architecture) bus, and each component contains an appropriate interface for interfacing with the bus.

When any component needs access to the memory 168 either to read from or write to the main memory 168, it generates a request which is placed on the bus 26. When the request is a write the data to be written is also placed on the bus 26. The request is processed in the core logic chipset 190 and the data is then either written to or read from the main memory 168. When data is read from the main memory 168 the data is now placed on the bus and goes to the component that requested the read.

There are typically many components in the computer systems that may require access to the main memory 168, and they are typically all coupled to the same bus 174, or possibly several buses 170, ~~188~~ 198 connected together by a PCI bridge 192, if there are not enough connectors on one bus to accommodate all of the peripherals. However, the addition of each bus is very expensive. Each request is typically processed according to a priority scheme. The priority scheme is typically based on the priority given to the device and the order in which the requests are received. Typically, the priority scheme is set up so no device monopolizes the bus, starving all of the other devices. Good practice suggests that no device on the bus require more than approximately 50% of the bus's bandwidth.

The minimum bandwidth required for the decoder 10 can be calculated based on the characteristics and desired operation of the decoder. These characteristics include the standard to which the bitstream is encoded to comply with, whether the decoder is to operate in real time, to what extent frames are dropped, and how the images are stored. Additionally, the latency of the bus that couples the decoder to the memory should be considered.

If the decoder does not operate in real time the decoded movie would stop

periodically between images until the decoder can get access to the memory to process the next image. The movie may stop quite often between images and wait.

To reduce the minimum required bandwidth and still operate in real time, the decoder 10 may need to drop ~~frame~~ frames. If the decoder 10 regularly does not decode every frame then it may not need to stop between images. However, this produces very poor continuity in the images. This is problematic with an image encoded to the MPEG-1 or MPEG-2 standards, or any standards that uses temporal compression. In temporal (interpicture) compression some of the images are decoded based on previous images and some based on previous and future images. Dropping an image on which the decoding of other images is based is unacceptable, and will result in many poor or even completely unrecognizable images.

The computer can also contain both a decoder and encoder to allow for video telephony, as described above. In this case not operating in real time would mean that the length of time between the occurrence of an event, such as speaking, at one end of the conversation until the event is displayed at the other end of the conversation is increased by the time both the encoder and then the decoder must wait to get access to the bus and the main memory. Not being able to operate in real time means that there would be gaps in the conversation until the equipment can catch up. This increases the time needed to have a video conference, and makes the conference uncomfortable for the participants.

One widely used solution to allow a component in a computer system to operate in real time is to give the component its own dedicated memory. Thus, as shown in Figure 1c, the decoder 10 can be given its own dedicated memory 22, with a dedicated bus 26 to connect the decoder 10 to its memory 22. The

dedicated memory 22, its controller and the pins to control this memory significantly increase the cost of adding a decoder 10 to the computer.

Summary of the Invention

The present application discloses an electronic system that contains a first device and video and/or audio decompression and/or compression device capable of operating in real time. Both the first device and the video and/or audio decompression and/or compression device require a memory interface. The video and/or audio decompression and/or compression device shares a memory interface and the memory with the first device. In the preferred embodiment of the invention the shared memory interface contains an arbiter. The arbiter and DMA engines of the video and/or audio decompression and/or compression device and of the first device are configured to arbitrate between the two devices when one of them is requesting access to the memory. This allows the use of one memory interface to control the access of both the video and/or audio decompression and/or compression device and the first device to the memory.

When the video and/or audio decompression and/or compression device used in an electronic system, such as a computer, already containing a device that has a memory interface the video and/or audio decompression and/or compression device can share that memory interface and the memory of the device and the memory interface and memory of the video and/or audio decompression and/or compression device can be eliminated. Eliminating this memory interface reduces the die area without changing the critical dimensions of the device. Therefore increasing the volume and reducing the cost of the decoder or encoder. Eliminating the memory greatly reduces the cost of adding the video and/or audio decompression and/or compression device to the electronic system while not requiring the video and/or audio decompression and/or compression device to be connected to the system bus, allowing the video and/or audio decompression and/or

compression device to operate in real time.

An advantage of the present invention is significant cost reduction due to the fact that the video and/or audio decompression and/or compression device does not need its own dedicated memory but can share a memory with another device and still operate in real time.

Another significant advantage of the present invention is that the die space needed for the video and/or audio decompression and/or compression device is smaller because the memory interface on the video and/or audio decompression and/or compression device is eliminated.

A further advantage of the present invention is that the video and/or audio decompression and/or compression device can share the memory of the device with which it is sharing the memory interface more efficiently.

Another advantage of the present invention is that the cost of producing a video and/or audio decompression and/or compression device is reduced because the memory interface on the video and/or audio decompression and/or compression device is eliminated.

Another advantage of the present invention is that the video and/or audio decompression and/or compression device can be monolithically integrated into the first device and no extra packaging or pins are needed for the video and/or audio decompression and/or compression device, and no pins are needed for the first device to connect to the video and/or audio decompression and/or compression device, saving pins on both devices and producing a better connection between the

two devices.

Other advantages and objects of the invention will be apparent to those of ordinary skill in the art having reference to the following specification together with the drawings.

Brief Description of the Drawings

Figure 1a and 1b are electrical diagrams, in block form, of prior art decoders.

Figure 1c is an electrical diagram, in block form, of a computer system containing a decoder according to the prior art.

Figure 2 is an electrical diagram, in block form, of an electronic system containing a device having a memory interface and an encoder and decoder.

Figure 3 is an electrical diagram, in block form, of a computer system containing a core logic chipset designed for the CPU to share a memory interface with an encoder and decoder.

Figure 4 is an electrical diagram, in block form, of a computer system containing a graphics accelerator designed to share a memory interface with an encoder and/or decoder.

Detailed Description of the Preferred Embodiment

Figure 2 shows an electronic system 40 containing a first device 42 having access to a memory 50 through a memory interface 48, and a decoder 44 and encoder 46, having access to the same memory 50 through the same memory interface 48. First device 42 can be a processor, a core logic chipset, a graphics accelerator, or any other device that requires access to the memory 50, and either contains or is coupled to a memory interface. Any parts common to Figures 1 through 4 are indicated using the same numbering system. In the preferred embodiment of the invention, electronic system 40 contains a first device 42, a decoder 44, an encoder 46, a memory interface 48, and a memory 50. Although, either the decoder 44 or encoder 46 can be used in the decoder/encoder 45 without the other. For ease of reference, a video and/or audio decompression and/or compression device 45 will hereinafter be referred to as decoder/encoder 45. The decoder/encoder 45 may be a single device, or cell on an integrated circuit, or may be two separate devices, or cells in an integrated circuit. In the preferred embodiment of the invention, the first device 42, decoder/encoder 45, and memory interface 48 are on one integrated circuit, however, they can be on separate integrated circuits in any combination.

a The decoder 44 includes a video decoding ~~12 circuit~~ circuit 12 and an audio decoding circuit 14, both coupled to a register interface 20. The decoder 44 can be either a video and audio decoder, just a video, or just an audio decoder. If the decoder 44 is just a video decoder it does not contain the audio decoding circuitry 14. The audio decoding can be performed by a separate audio codec coupled to the first device 42, or through software. In the preferred embodiment of the invention, when the decoder/encoder 45 is in a system containing a processor and is coupled

to the processor, the audio decoding is performed in software. This frees up space on the die without causing significant delay in the decoding. If the audio decoding is performed in software, the processor should preferably operate at a speed to allow the audio decoding to be performed in real time without starving other components of the system that may need to utilize the processor. For example, currently software to perform AC-3 audio decoding takes up approximately 40% of the bandwidth of a 133 MHz Pentium. The encoder 46 includes a video encoding circuit 62 and an audio encoding circuit 64, both coupled to a register interface 20. The encoder 46 can be either a video and audio encoder, just a video, or just an audio encoder. If the encoder 46 is just a video encoder, it does not contain the audio encoding circuitry 64. The audio encoding can be performed by a separate audio codec coupled to the first device 42, or through software. In the preferred embodiment of the invention, when the decoder/encoder 45 is in a system containing a processor and is coupled to the processor, the audio encoding is performed in ~~software. Presenting~~ Software presenting the same advantages of freeing up space on the die without causing significant delay in the encoding. The register interfaces 20 of the decoder 44 and encoder 46 are coupled to a processor.

The decoder 44 and encoder 46 are coupled to the direct memory access (DMA) engine 52. The decoder and encoder can be coupled to the same DMA engine as shown in Figure 2, or each can have its own DMA engine, or share a DMA engine with another device. When the decoder/encoder 45 are two separate devices or cells, decoder 44 and encoder 46 can still be coupled to one DMA engine 52. When the decoder/encoder is one device or is one cell on an integrated circuit, the DMA engine 52 can be part of the decoder/encoder 45, as shown in Figure 2. The DMA engine 52 is coupled to the arbiter 54 of the memory interface 48.

The first device 42 also contains a DMA engine 60. The DMA engine 60 of the first device 42 is coupled to the arbiter 54 of the memory interface 48. The arbiter is also coupled to the refresh logic 58 and the memory controller 56. The memory interface 48 is coupled to a memory 50. The memory controller 56 is the control logic that generates the address the memory interface 48 accesses in the memory 50 and the timing of the burst cycles.

In current technology, memory 50 is typically a DRAM. However, other types of memory can be used. The refresh logic 58 is needed to refresh the DRAM. However, as is known in the art, if a different memory is used, the refresh logic 58 may not be needed and can be eliminated.

The decoder/encoder 45 is coupled to the memory 50 through devices, typically a bus 70, that have a bandwidth greater than the bandwidth required for the decoder/encoder 45 to operate in real time. The minimum bandwidth required for the decoder/encoder 45 can be calculated based on the characteristics and desired operation of the decoder, including the standard to which the bitstream is encoded to comply with, whether the decoder/encoder 45 is to operate in real time, to what extent frames are dropped, and which images are stored. Additionally, the latency of the bus 70 that couples the decoder/encoder 45 to the memory 50 should be considered.

A goal is to have the decoder/encoder 45 operate in real time without dropping so many frames that it becomes noticeable to the human viewer of the movie. To operate in real time the decoder/encoder 45 should decoder and/or encode images fast enough so that any delay in decoding and/or encoding cannot be detected by a human viewer. This means that the decoder/encoder 45 has a

required bandwidth that allows the decoder/encoder 45 to operate fast enough to decode the entire image in the time between screen refreshes, which is typically 1/30 of a second, with the human viewer not being able to detect any delay in the decoding and/ or encoding. To operate in real time the required bandwidth should be lower than the bandwidth of the bus. In order not to starve the other components on the bus, i.e. deny these components access to the memory for an amount of time that would interfere with their operation, this required bandwidth should be less the entire bandwidth of the bus. Therefore a fast bus 70 should be used. A fast bus 70 is any bus whose bandwidth is equal to or greater that the required bandwidth. There are busses, in current technology, including the ISA bus, whose bandwidth is significantly below the bandwidth required for this.

In the preferred embodiment of the invention the decoder/encoder 45 is coupled to the memory 50 through a fast bus 70 that has a bandwidth of at least the bandwidth required for the decoder/encoder 45 to operate in real time, a threshold bandwidth. Preferably the fast bus 70 has a bandwidth of at least approximately twice the bandwidth required for the decoder/encoder 45 to operate in real time. In the preferred embodiment the fast bus 70 is a memory bus, however any bus having the required bandwidth can be used.

The decoder/encoder 45 only requires access to the memory during operation. Therefore, when there is no need to decode or encode, the first device 42, and any other devices sharing the memory 50 have exclusive access to the memory, and can use the entire bandwidth of the fast bus 70.

In the preferred embodiment, even during decoding and encoding the decoder/encoder 45 does not always use the entire required bandwidth. Since the

fast bus 70 has a bandwidth a little less than twice the required bandwidth the decoder/encoder 45 uses at most 60% of the bandwidth of the fast bus 70.

The required bandwidth is determined based on the size and resolution of the image, and the type of frame (I, P, or B). In the preferred embodiment the decoder/encoder typically will be using less than 40% of the bandwidth of the fast bus 70. This frees up the remaining bandwidth to be used by the other devices the decoder/encoder 45 is sharing the memory 50 with.

The decoder/encoder 45 can decode a bitstream formatted according to any one or a combination of standards. In the preferred embodiment of the invention the decoder/encoder 45 is a multi-standard decoder/encoder capable of decoding and encoding sequences formatted to comply to several well accepted standards. This allows the decoder/encoder 45 to be able to decode a large number of video and/or audio sequences. The choice of which standards the decoder/encoder 45 is capable of decoding bitstreams formatted to and of encoding sequences to comply to is based on the desired cost, efficiency, and application of the decoder/encoder 45.

In the preferred embodiment, these standards are capable of both intrapicture compression and interpicture compression. In intrapicture compression the redundancy within the image is eliminated. In interpicture compression the redundancy between two images are eliminated and only the difference information is transferred. This requires the decoder/encoder 45 to have access to the previous or future image that contains information needed to decode or encode the current image. These precious and/or future images need to be stored then used to decode the current image. This is one of the reasons the decoder/encoder 45 requires access to the memory, and requires a large bandwidth. The MPEG-1 and MPEG-2

standards allow for decoding based on both previous images and/or future images. Therefore for a decoder/encoder 45 capable of operating in real time to be able to comply with the MPEG-1 and MPEG-2 standards it should be able to access two images, a previous and a future image, fast enough to decode the current image in the 1/30 of a second between screen refreshes.

An MPEG environment is asymmetrical; there are much fewer encoders than decoders. The encoders are very difficult and expensive to manufacture and the decoders are comparatively easy and cheap. This encourages many more decoders than encoders, with the encoders in centralized locations, and decoders available such that every end user can have a decoder. Therefore, there are many receivers but few transmitters.

For video telephony and teleconferencing each end user has to be able to both receive and transmit. H.261, and H.263 are currently well accepted standards for video telephony. An encoder that can encode sequences to comply to the H.261 and H.263 standards is less complicated, having a lower resolution and lower frame rate than an encoder that complies to the MPEG-1 or MPEG-2 ~~standards~~ standards, possibly. ~~Possibly~~ making the quality of the decoded images somewhat lower than those from an encoder that complies with the MPEG-1 or MPEG-2 standards. Such an encoder, since it should be inexpensive and operate in real time, is also less efficient than an encoder to encode sequences to comply to the MPEG-1 or MPEG-2 standards. ~~Meaning that compression~~ This means that the compression factor, which is the ratio between the source data rate and the encoded bitstream data rate, of such an encoder is lower for a given image quality than the compression factor of an MPEG encoder. However, because such an encoder is less ~~complicated is it~~ complicated, it is much cheaper and faster than an encoder capable of complying with the MPEG-1 and/or MPEG-2 standards.

This makes video telephony possible, since both a long delay in encoding the signal and a cost that is prohibitively expensive for many users is unacceptable in video telephony.

In the preferred embodiment, the decoder/encoder 45 is capable of decoding a bitstream formatted to comply to the MPEG-1, MPEG-2, H.261, and H.263 standards, and encoding a sequence to produce a bitstream to comply to the H.261, and H.263 standards. This allows the decoder/encoder 45 ~~to be able~~ to be used for video telephony. ~~The encoding to comply~~ Having the encoding comply to the H.261 and H.263 standards but not the MPEG-1 and MPEG-2 standards balances the desire to reduce the cost of transmission and storage by encoding to produce the highest compression factor and the desire to keep cost low enough to be able to mass market the device.

The decoder/encoder 45 is preferably monolithically integrated into the first device as shown in Figure 3 and Figure 4. In Figure 3 the decoder/encoder 45 is integrated into a core logic chipset 150. In Figure 4 the decoder/encoder 45 is integrated into a graphics accelerator 200. Although, the decoder/encoder 45 can be separate from the first device 42, as shown in Figure 2.

Figure 3 shows a computer where the decoder/encoder 45 and the memory interface 48 are integrated into a core logic chipset 150. The core logic chipset 150 can be any core logic chipset known in the art. In the embodiment shown in Figure 3 the core logic chipset 150 is a PCI core logic chipset 150, which contains a PCI core logic device 158, the processor interface 154, and bus interfaces 156 for any system busses 170 to which it is coupled. The core logic chipset 150 can also contain a accelerated graphics port (AGP) 160 if a graphics accelerator 200 is present in the computer, and an enhanced integrated device electronics (EIDE)

interface 186. The core logic chipset 150 is coupled to a processor 152, peripherals, such as a hard disk drive 164 and a DVD CD-ROM 166, a bus, such as a PCI bus 170, and a main memory 168.

In this embodiment, the main memory 168 is the memory 50 to which the memory interface 48 is coupled to. The main memory 168 is coupled to the memory interface 48 through a memory bus 167. In current technology the memory bus 167, which corresponds to the fast bus 70, for coupling a core logic chipset to a memory, is capable of having a bandwidth of approximately 400 Mbytes/s. This bandwidth is at least twice the bandwidth required for an optimized decoder/encoder 45, allowing the decoder/encoder 45 to operate in real time.

The core logic chipset 150 can also be coupled to cache memory 162 and a graphics accelerator 200 if one is present in the computer. The PCI bus 170 is also coupled to the graphics accelerator 200 and to other components, such as a local-area network (LAN) controller 172. The graphics accelerator 200 is coupled to a display 182, and a frame buffer 184. The graphics accelerator can also be coupled to an audio codec 180 for decoding and/or encoding audio signals.

Figure 4 shows a computer where the decoder/encoder 45 and the memory interface 48 are integrated into a graphics accelerator 200. The graphics accelerator 200 can be any graphics accelerator known in the art. In the embodiment shown in Figure 4, the graphics accelerator 200 contains a 2D accelerator 204, a 3D accelerator 206, a digital to analog converter 202, and bus interfaces 210 for any system busses 170 to which it is coupled. The graphics accelerator 200 can also contain an audio compressor/decompressor 208. The graphics accelerator 200 is coupled to a display 182, and a frame buffer 184.

In this embodiment, the frame buffer 184 is the memory 50 to which the memory interface 48 is coupled. The frame buffer 184 is coupled to the memory interface 48 through a memory bus 185. In this embodiment, memory bus 185 corresponds to the fast bus 70. In current technology the memory bus 185, for coupling a graphics accelerator to a memory, is capable of having a bandwidth of up to 400 Mbytes/s. This bandwidth is more that twice the bandwidth required for an optimized decoder/encoder 45. This allows the decoder/encoder 45 to operate in real time.

The graphics accelerator 200 can also be coupled to an audio codec 180 for decoding and/or encoding audio signals. The PCI bus 170 is also coupled to a chipset 190, and to other components, such as a LAN controller 172. In the present embodiment the chipset is a PCI chipset, although it can be any conventional chipset. The chipset 190 is coupled to a processor 152, main memory 168, and a PCI bridge 192. The PCI bridge bridges between the PCI bus 170 and the ISA bus 198. The ISA bus 198 is coupled to peripherals, such as a modem 199 and to an EIDE interface 186, which is coupled to other peripherals, such as a hard disk drive 164 and a DVD CD-ROM 166. Although, if the peripherals are compatible to the PCI bus the EIDE interface 186 can be integrated in to the PCI chipset 190 and the peripherals 164, 166 can be coupled directly to the PCI chipset, eliminating the PCI bridge 192 and the ISA bus 198.

Referring to Figure 2, the operation of the memory interface 48 during a memory request will now be described. During operation the decoder/encoder 45, the first device 42, and the refresh logic 58, if it is present, request access to the memory through the arbiter 54. There may also be other devices that request access to the memory 50 through this arbiter. The arbiter 54 determines which of

the devices gets access to the memory 50. The decoder gets access to the memory in the first time interval and the first device gets access to the memory in the second time interval. The DMA engine 52 of the decoder/encoder 45 determines the priority of the decoder/encoder 45 for access to the memory 50 and of the burst length when the decoder/encoder 45 has access to the memory. The DMA engine 60 of the first device determines its priority for access to the memory 50 and the burst length when the first device 42 has access to the memory.

The decoder/encoder 45 or one of the other devices generates a request to access the memory 50. The request will be transferred to the arbiter 54. The state of the arbiter 54 is determined. The arbiter typically has three states. The first state is idle, when there is no device accessing the memory and there are no requests to access the memory. The second state is busy when there is a device accessing the memory and there are no a request to access the memory. The third state is queue when there is a device accessing the memory and there is another request to access the memory.

It is also determined if two requests are issued simultaneously. This can be performed either before of after determining the state of the arbiter. Access to the memory is determined according to the following chart.

Arbiter state	Simultaneous requests	Action
Idle	Yes	One of the requests gets access to the memory based on the priority scheme, and the other request is queued.
Busy	Yes	Both requests are queued in an order based on the priority scheme.
Queue	Yes	Both requests are queued in an order based on the priority scheme.
Idle	No	The device gets access to the memory.
Busy	No	The request is queued.
Queue	No	The requests are queued in an order based on the priority scheme.

The priority scheme can be any priority scheme that ensures that the decoder/encoder 45 gets access to the memory 50 often enough and for enough of a burst length to operate properly, yet not starve the other devices sharing the memory. The priority of the first device, device priority, and the priority of the decoder/encoder 45, decoder priority, is determined by the priority scheme. This can be accomplished in several ways.

To operate in real time, the decoder/encoder 45 has to decode an entire image in time to be able to display it the next time the screen is refreshed, which is typically every 1/30 of a second. The decoder/encoder 45 should get access to the

memory to store and retrieve parts of this and/or of past and/or future images, depending on the decoding standard being used, often enough and for long enough burst lengths to be able to decode the entire image in the 1/30 of a second between screen refreshes.

There are many ways to this. One way to do this is to make the burst length of the first device, and any other device like the screen refresh that shares the memory and memory interface, [hereinafter sharing device] have short burst lengths, and to make sure that the same device is not the next device to get access to the memory when other devices have been waiting for a long time. Another way is to preempt the sharing device if its burst length exceeds a burst length threshold and again to make sure that the same device is not the next device to get access to the memory when other devices have been waiting for a long time. Preferably, when the preemption is used the sharing device would be preempted when its burst length exceeds 16 words. A third way is to limit the bandwidth available to the sharing devices, this way the decoder/encoder 45 always has enough bandwidth to operate in real time. Preferably the bandwidth of the sharing devices is limited only when the decoder/encoder 45 is operating. In the preferred embodiment a memory queue, such as a FIFO, in the decoder/encoder 45 generates an error signal when it falls below a data threshold. The error is sent to the CPU 152 and the CPU 152 can either shut down the system, drop ~~a image~~ an image frame or resume the decoding/encoding process.

There are also many ways to make sure that the same device is not the next device to get access to the memory when other devices have been waiting for a long time. This both ensures decoder/encoder 45 gets access to the memory 50 often enough, yet not starve the other devices sharing the memory. One way to do

this is to disallow back to back requests. Another is to have shifting priority, where a particular request starts with a lower priority when first made and the priority increases with the length of time the request is in the queue, eventually reaching a priority above all of the other requests. In the preferred embodiment, the decoder/encoder 45 has a one clock cycle delay between requests to allow a sharing device to generate a request between the decoder/encoder requests.

In the preferred embodiment the burst length of the decoder is relatively short, approximately four to seventeen words. This allows the graphics accelerator more frequent access to the memory to ensure that the display is not disturbed by the sharing of the memory interface 48 and memory 50 when the decoder/encoder is in the graphics accelerator 200.

An electronic system 40, shown in Figure 2, containing the first device 42, the memory interface 48 coupled to a memory 50 and to the first device 42, a decoder/encoder 45 coupled to the memory interface 48, where the decoder/encoder 45 shares the memory interface 48 with the first device 42 provides several advantages. Referring to Figure 2 and Figure 1b simultaneously, the decoder 44, and encoder 46, according to the preferred embodiment of the invention do not need their own memory interfaces 18, as was needed in the prior art. Eliminating the memory interface 18 results in reducing the die size. This allows both a reduction in the price per die of the decoder, or encoder, and an increase in the volume of the product that can be produced.

Additionally, because the decoder/encoder 45 shares the memory interface 48 of the first device it also shares its memory 50. This eliminates the dedicated memory 22 that was necessary in the prior art for the decoder/encoder to operate

in real time, resulting in significant reduction in the cost of the device. Allowing the decoder/encoder 45 to share the memory 50 with a first device 42 and to allow the decoder/encoder 45 to access the memory 50 through a fast bus 70 having a bandwidth of a least the bandwidth threshold permits the decoder/encoder to operate in real time. This allows the decoder/encoder to operate in real time and reduces stops between images and dropping frames to a point where both are practically eliminated. This produces better images, and eliminates any discontinuities and delays present in the prior art.

Furthermore, as the geometry used for devices decreases and the functionality of device increases the number of pads required in them increases. This at times requires the die size to be dictated by the number of pads and their configuration, leaving empty space on the die. This is typically the situation for core logic chipsets. In current technology, the pad requirements of a core logic chipset require the chipset to be one-third larger than required for the functional components of the core logic chipset. That means that one-third of the die space is empty. Incorporating the decoder/encoder 45 into the core logic chipset 150, as shown in Figure 3 provides the added advantage of effectively utilizing that space, without adding any extra pins to the core logic chipset 150. It also provides better connections between the decoder/encoder 45 and the core logic chipset 150.

Further background on compression can be found in: International Organization for Standards, INFORMATION TECHNOLOGY - CODING OF MOVING PICTURES AND ASSOCIATED AUDIO FOR DIGITAL STORAGE MEDIA AT UP TO ABOUT 1.5 MBITS/S, Parts 1-6, International Organization for Standards; International Standards Organization, INFORMATION TECHNOLOGY - GENERIC CODING OF MOVING PICTURES AND ASSOCIATED AUDIO INFORMATION, Parts 1-4, International

Organization for Standards; Datasheet "STi3500A" Datasheet of SGS-THOMSON Microelectronics; STi3500A - Advanced Information for an MPEG Audio/ MPEG-2 Video Integrated Decoder" (June 1995); Watkinson, John, COMPRESSION IN VIDEO AND AUDIO, Focal Press, 1995; Minoli, Daniel, VIDEO DIALTONE TECHNOLOGY, McGraw-Hill, Inc., 1995. Further background on computer architecture can be found in Anderson, Don and Tom Shanley, ISA SYSTEM ARCHITECTURE, 3rd ed., John Swindle ed., MindShare Inc., Addison-Wesley Publishing Co., 1995. All of the above references incorporated herein by reference.

While the invention has been specifically described with reference to several preferred embodiments, it will be understood by those of ordinary skill in the prior art having reference to the current specification and drawings that various modifications may be made and various alternatives are possible therein without departing from the spirit and scope of the invention.

For example:

Although the memory is described as DRAM the other types of memories including read-only memories, SRAMs, or FIFOs may be used without departing from the scope of the invention.

Any conventional decoder including a decoder complying to the MPEG-1, MPEG-2, H.261, or H.261 standards, or any combination of them, or any other conventional standard can be used as the decoder/encoder.

WE CLAIM:

1. An electronic system coupled to a memory and to a first device that requires access to the memory, the electronic system comprising:

a decoder that requires access to the memory sufficient to maintain real-time operation; and

a memory interface coupled to the decoder, for selectively providing access for the first device and the decoder to the memory.

2. The electronic system of claim 1, wherein the memory interface is coupled to the first device.

3. The electronic system of claim 1, wherein the memory interface is coupled to the memory.

4. The electronic system of claim 1, wherein the decoder comprises a video decoder.

5. The electronic system of claim 1, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.

6. The electronic system of claim 1, wherein the memory interface further comprises an arbiter for selectively providing access for the first device and the decoder to the memory.

7. The electronic system of claim 1, further comprising an encoder coupled to the memory interface.

8. The electronic system of claim 7, wherein the decoder, the encoder and the memory interface are monolithically integrated into the first device.

9. The electronic system of claim 7, wherein the encoder is capable of producing a bitstream that complies with the H.263 standard.

10. The electronic system of claim 1, wherein the decoder and the memory interface are monolithically integrated into the first device.

11. The electronic system of claim 1, further comprising a fast bus coupled to the memory, to the decoder and to the first device.

12. The electronic system of claim 11, wherein the fast bus has a bandwidth of greater than a threshold bandwidth.

13. The electronic system of claim 11, wherein the fast bus comprises a memory bus.

14. An electronic system coupled to a memory, comprising:

a first device that requires access to the memory;

a decoder that requires access to the memory sufficient to maintain real time operation;

a fast bus coupled to the first device and the decoder; and

a memory interface for coupling to the memory, and coupled to the first device, and to the decoder, the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory.

15. The electronic system of claim 14, wherein:
the first device is capable of having a variable bandwidth; and
the decoder is capable of having a variable bandwidth.

16. The electronic system of claim 14, wherein the decoder comprises a video decoder.

17. The electronic system of claim 14, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.

18. The electronic system of claim 14, further comprising an encoder coupled to the memory interface.

19. The electronic system of claim 18, wherein the decoder, the encoder and the memory interface are monolithically integrated into the first device.

20. The electronic system of claim 18, wherein the encoder is capable of producing a bitstream that complies with the H.263 standard.

21. The electronic system of claim 14, wherein the decoder and the memory interface are monolithically integrated into the first device.

22. The electronic system of claim 14, wherein the first device is a processor chipset.

23. The electronic system of claim 22, wherein the processor chipset is coupled to a processor.

24. The electronic system of claim 14, wherein the first device is a graphics accelerator.

25. The electronic system of claim 14, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.

26. The electronic system of claim 14, ~~wherein the fast bus has a bandwidth of~~ greater than a threshold bandwidth.

27. The electronic system of claim 14, wherein the fast bus comprises a memory bus.

28. A computer comprising:

an input device;

an output device;

a memory;

a first device that requires access to the memory;

a decoder that requires access to the memory sufficient to maintain real time operation; and

a memory interface coupled to the memory, to the first device, and to the decoder, the memory interface having a means for selectively providing access for the first device and the decoder to the memory.

29. The computer of claim 28, wherein:

the first device is capable of having a variable bandwidth; and

the decoder is capable of having a variable bandwidth.

17 15
30. The computer of claim 28, wherein the decoder comprises a video decoder.

18 15
31. The computer of claim 28, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.

19 15
32. The computer of claim 28, wherein the memory interface further comprises an arbiter for selectively providing access for the first device and the decoder to the memory.

20 15
33. The computer of claim 28, further comprising an encoder coupled to the memory interface.

21 20
34. The computer of claim 33, wherein the decoder, the encoder and the memory interface are monolithically integrated into the first device.

22 20
35. The computer of claim 33, wherein the encoder is capable of producing a bitstream that complies with the H.263 standard.

23 15
36. The computer of claim 28, wherein the decoder and the memory interface are monolithically integrated into the first device.

24 15
37. The computer of claim 28, wherein the first device is a processor chipset.

25 24
38. The computer of claim 37, wherein the processor chipset is coupled to a processor.

39. The computer of claim 28, wherein the first device is a graphics accelerator.

40. The computer of claim 28, wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard.

41. The computer of claim 28, further comprising a fast bus coupled to the memory, to the decoder and to the first device.

42. The computer of claim 41, wherein the fast bus has a bandwidth of greater than a threshold bandwidth.

43. The electronic system of claim 41, wherein the fast bus comprises a memory bus.

44. In an electronic system having a first device coupled to a memory interface and a memory coupled to the memory interface, the first device having a device priority and capable of generating a request to access the memory, a method for selectively providing access to the memory comprising the steps of:

providing a decoder coupled to the memory interface, the decoder capable of operating in real time, having a decoder priority and capable of generating a request to access the memory;

providing an arbiter having an idle, a busy and a queue state;

generating a request by the decoder to access the memory;

determining the state of the arbiter;

providing the decoder access to the memory responsive to the arbiter being in the idle state;

queuing the request responsive to the arbiter being in the busy state; and

queuing the request responsive to the arbiter being in the queue state in an order responsive to the priority of the decoder request and the priority of any other queued requests.

30 ~~45~~. The method of claim 29 ~~44~~, further comprising the steps of:

determining the number of requests issued simultaneously;

responsive to number of requests issued simultaneously being greater than one:

selectively providing access to the memory responsive to the arbiter being in the idle state, and the priority of the simultaneously issued requests;

queuing the simultaneously issued requests responsive to the arbiter being in the busy state in an order responsive to the priority of the simultaneously issued requests;

queuing the simultaneously issued requests responsive to the arbiter being in the queue state in an order responsive to the priority of the simultaneously issued requests and the priority of any other queued requests.

31 ~~46~~. The method of claim 30 ~~45~~, wherein the step of determining the number of requests issued simultaneously is performed prior to the step of determining the state of the arbiter.

32 ~~47~~. The method of claim 29 ~~44~~, further comprising the step of preempting the first device access to the memory and providing the decoder access to the memory responsive to the first device having a burst length above a burst length threshold.

33 ~~48~~. The method of claim 29 ~~44~~, wherein the decoder priority increases

responsive to the length of time the request issued by the decoder is queued.

49. In an electronic system having a first device coupled to a memory interface and a memory coupled to the memory interface, a method for selectively providing access to the memory comprising the steps of:

providing a memory management system;

providing a decoder coupled to the memory interface, the decoder capable of operating in real time;

providing access to the memory at a first time interval to the decoder; and

providing access to the memory at a second time interval to the first device.

08/702911

ABSTRACT

An electronic system that contains a first device that requires a memory interface and video and/or audio decompression and/or compression device that shares a memory interface and memory with the first device while still permitting the video and/or audio decompression and/or compression device to operate in real time is disclosed.

Docket No. 96-S-11

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name,

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Video and/or Audio Decompression and/or Compression Device that Shares a Memory Interface

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

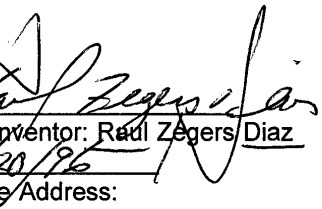
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint Lisa K. Jorgenson, Reg. No. 34,845 and Irena Lager, Reg. No. 39,260 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

2

Please send all correspondence to:

Lisa K. Jorgenson
Reg. No. 34,845
SGS-Thomson Microelectronics, Inc.
1310 Electronics Drive
Carrollton, TX 75006
(214) 466-7414

1-00 Inventor's Signature: 
Full Name of First Joint Inventor: Raul Zegers Diaz
Date of Signature: 8/20/96
Residence and Post Office Address:
750 Montrose Ave.
Palo Alto, CA 94303

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Second Joint Inventor: Jefferson Eugene Owen
Date of Signature: _____
Residence and Post Office Address:
44177 Bowers Court
Freemont, CA 94539

Citizenship: United States of America

Inventor's Signature: _____
Full Name of First Joint Inventor: Raul Zegers Diaz
Date of Signature: _____
Residence and Post Office Address:
750 Montrose Ave.
Palo Alto, CA 94303

Citizenship: United States of America

2-00 Inventor's Signature: _____
Full Name of Second Joint Inventor: Jefferson Eugene Owen
Date of Signature: Aug 22, 1996
Residence and Post Office Address:
44177 Bowers Court
Freemont, CA 94539

Citizenship: United States of America

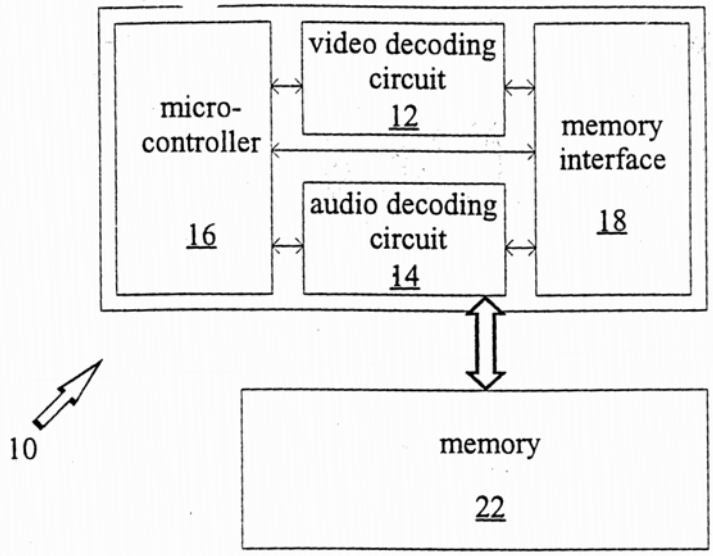


Figure 1a
(Prior Art)

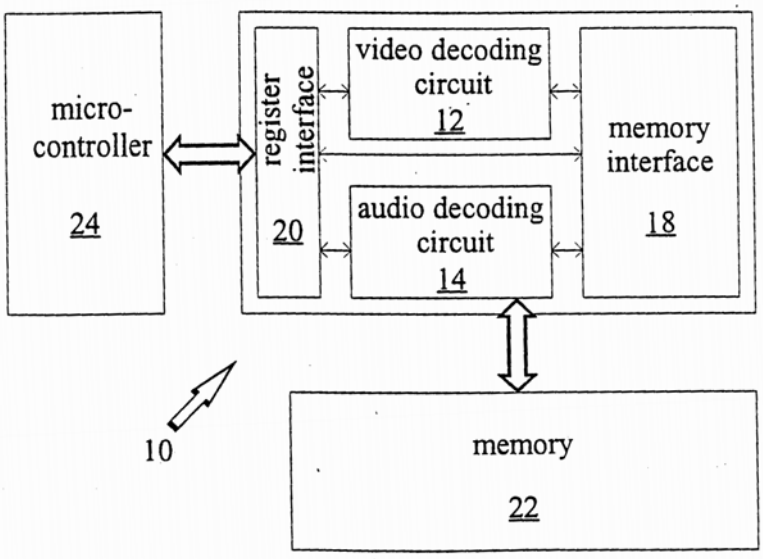


Figure 1b
(Prior Art)

Figure 1C
(Prior Art)

register interface 20
video encoding circuit 62
audio encoding circuit 64
Encoder 46
45
video decoding circuit 12
audio decoding circuit 14
register interface 20
Decoder 44
DMA Engine 52
Memory Interface
48
Arbiter 54
Refresh Logic 58
Memory Controller 56
70
Memory 50
First Device 42
DMA Engine 60
40

Figure 2

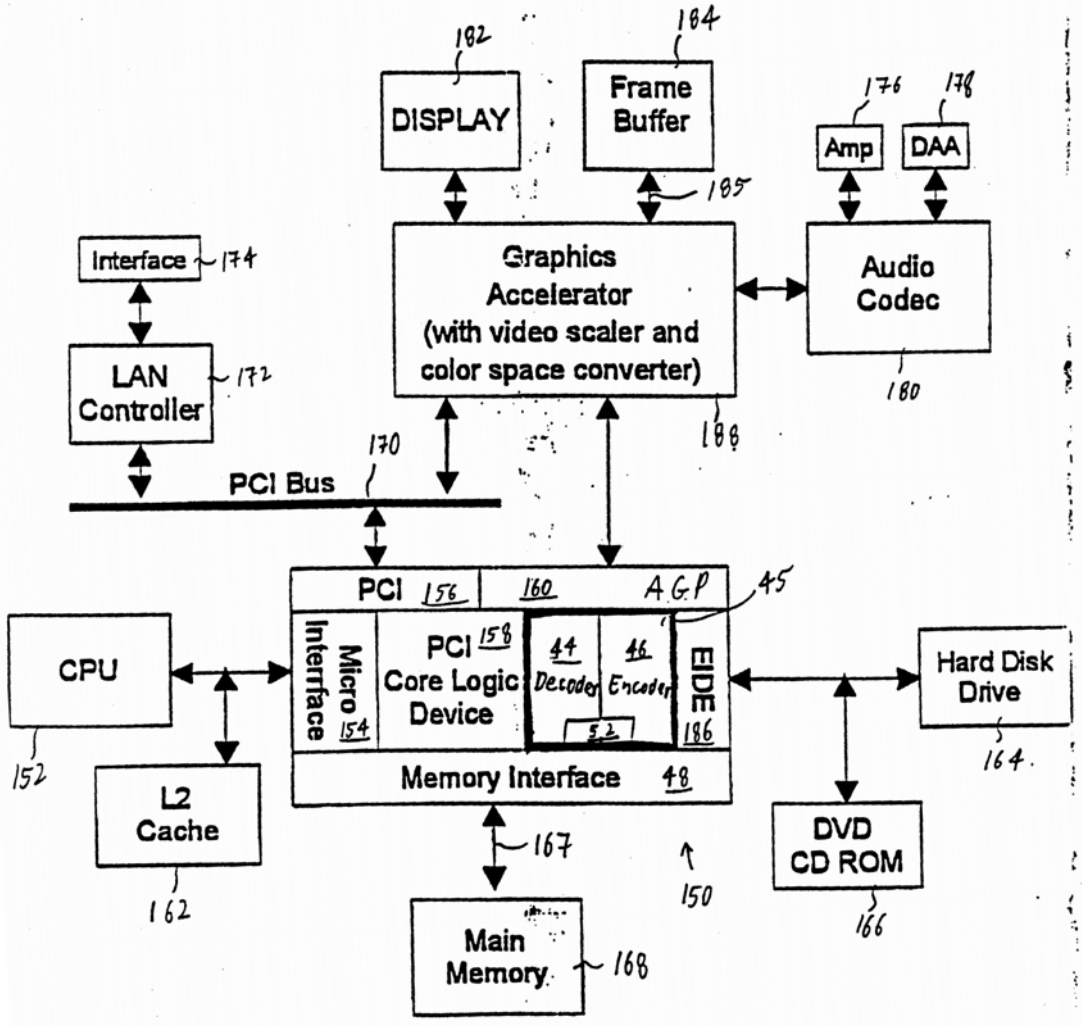


Figure 3

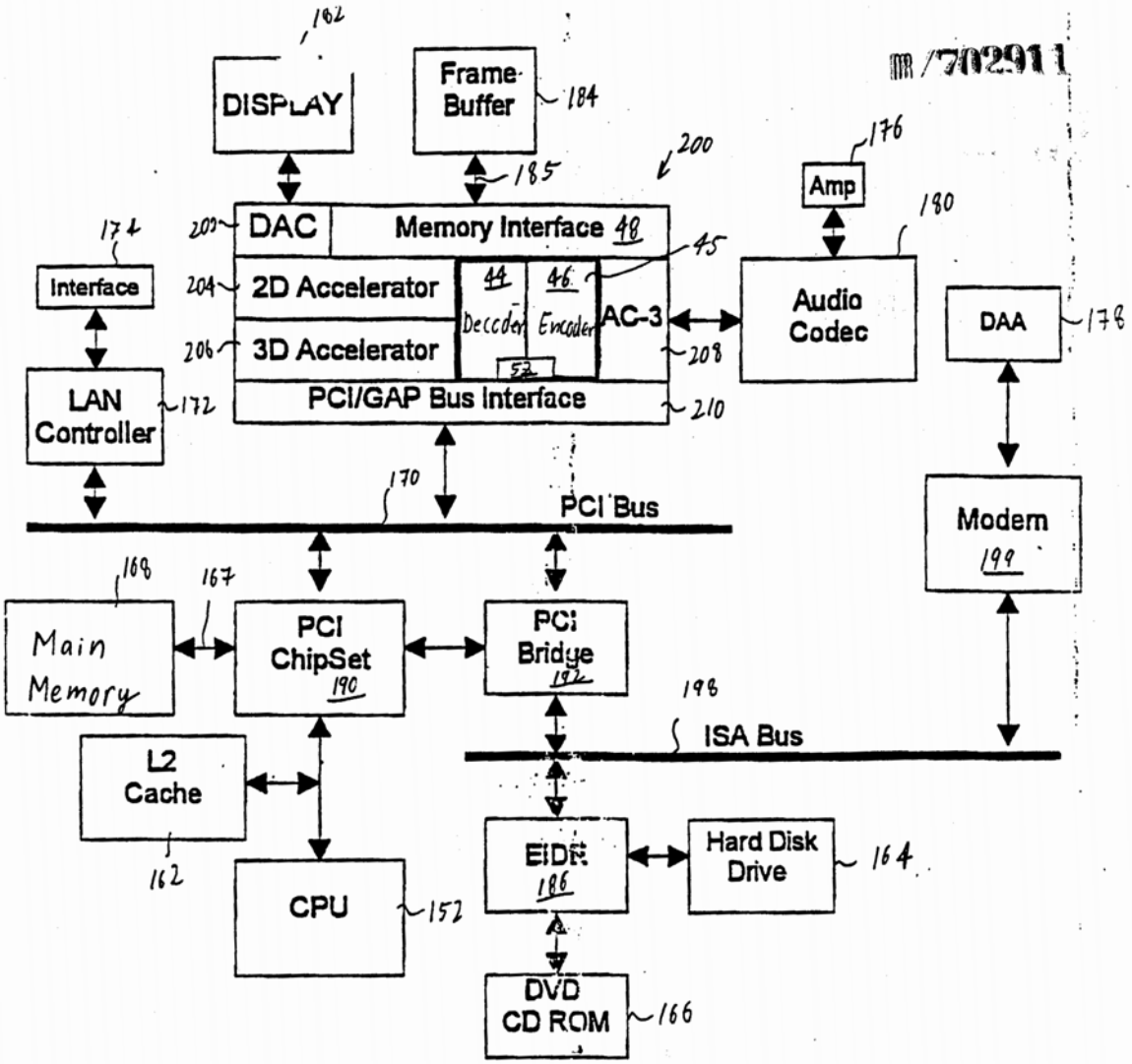


Figure 4

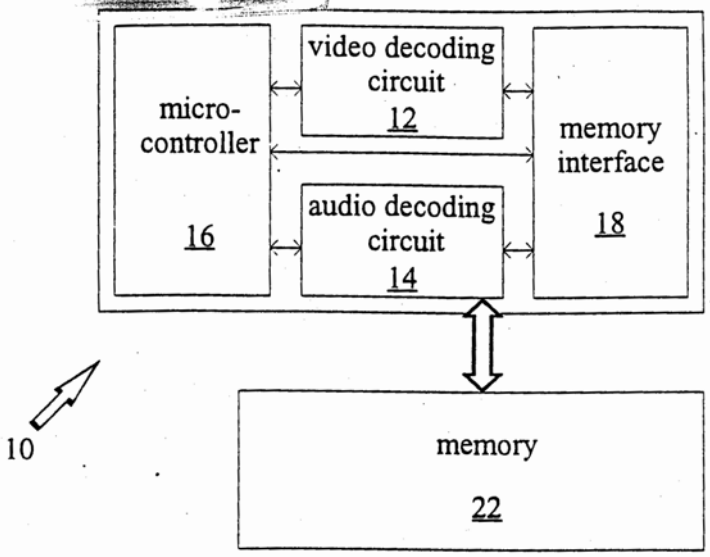


Figure 1a
(Prior Art)

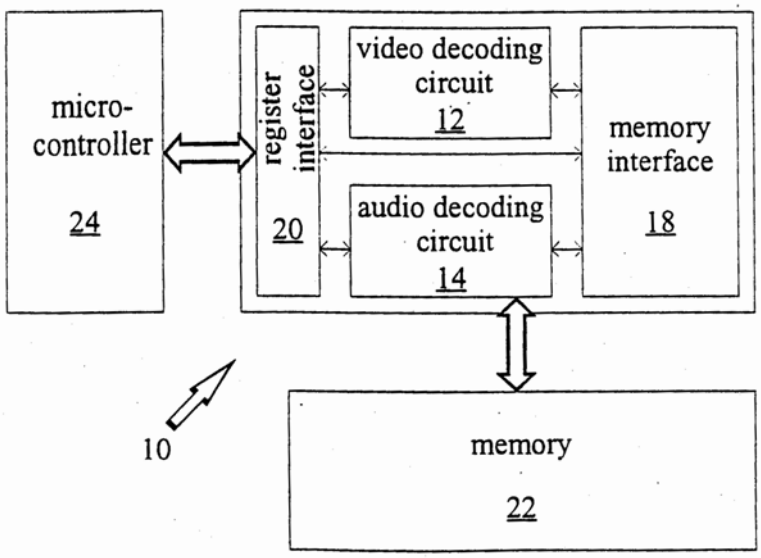


Figure 1b
(Prior Art)

PRINT OF DP INGS AS ORIGIN FILED

BR/702911

Figure 1C
(Prior Art)

25

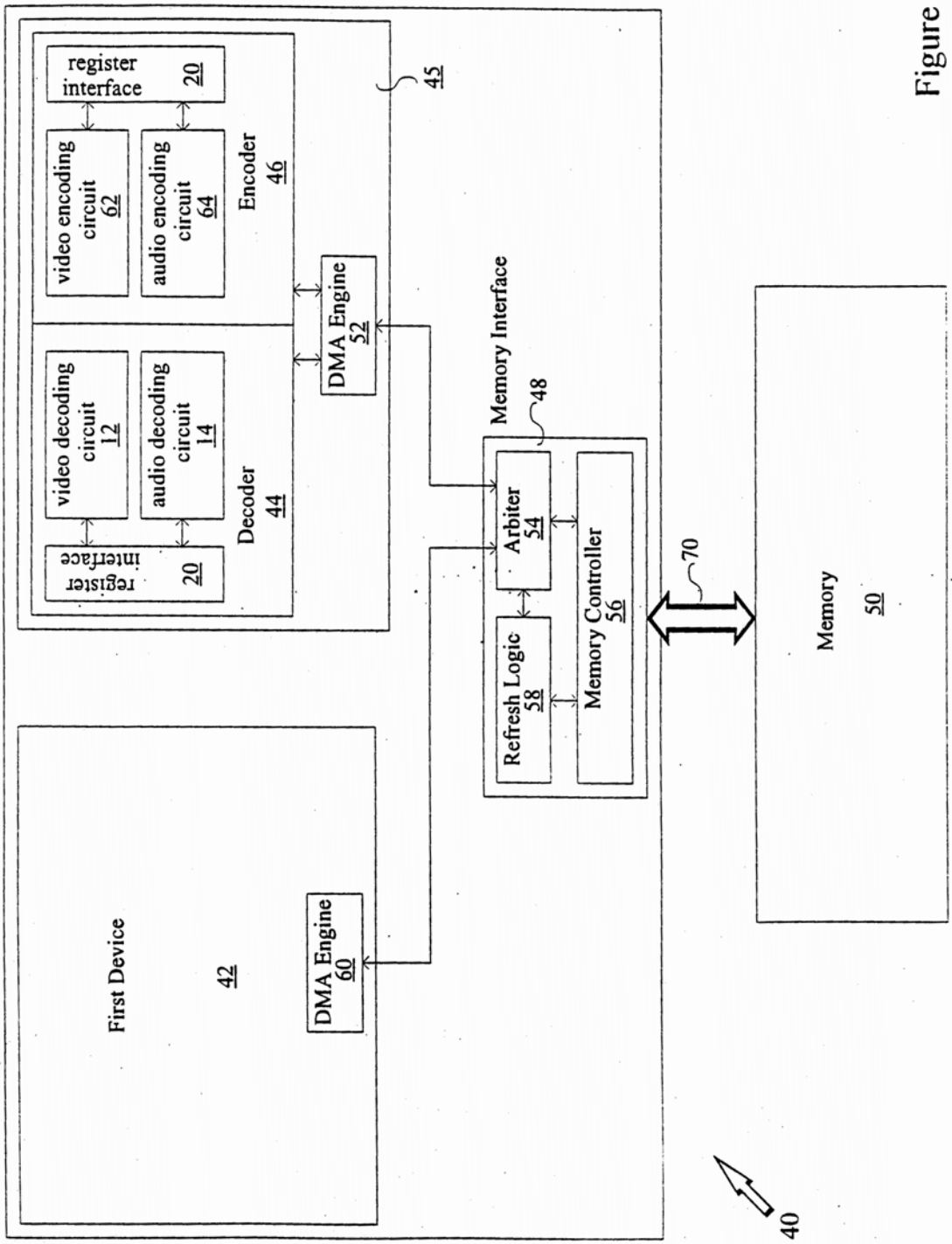


Figure 2

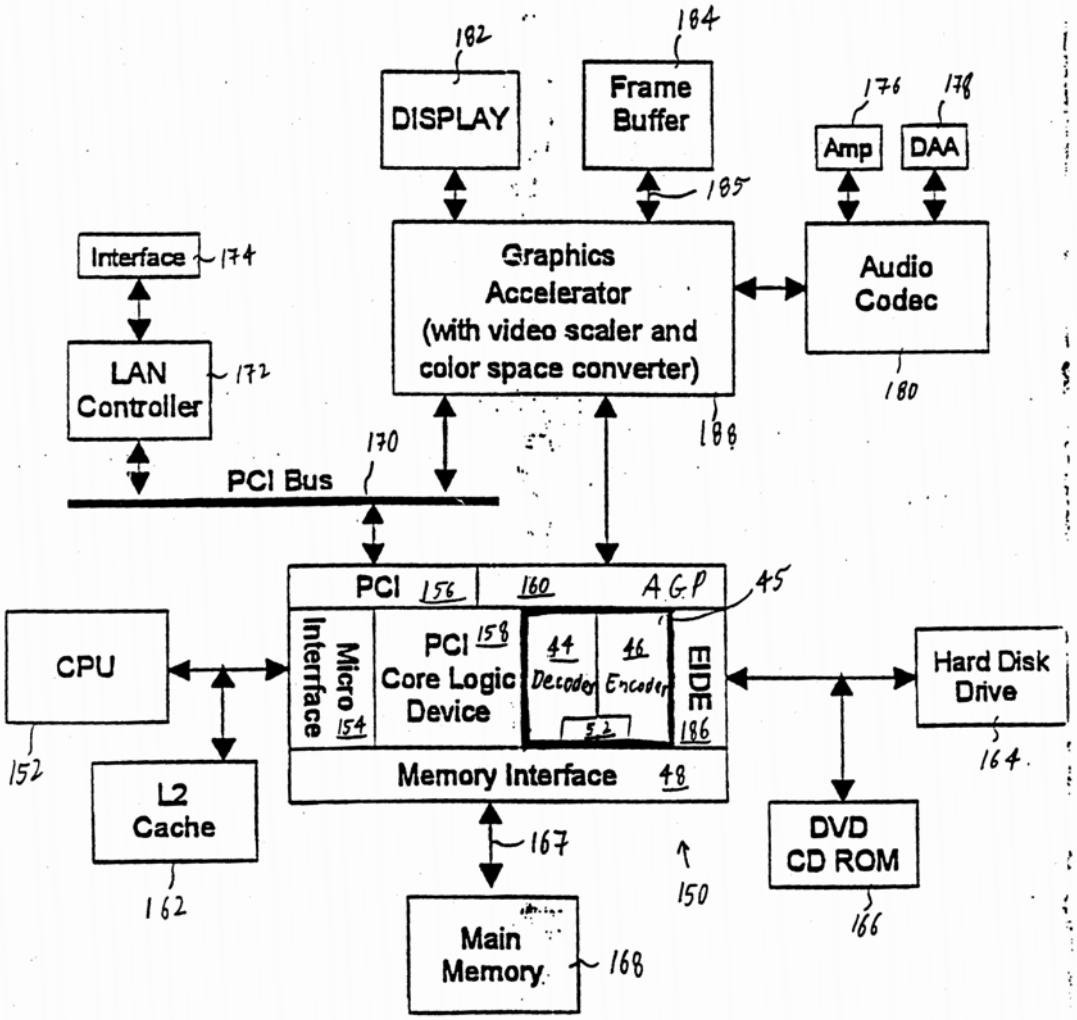


Figure 3

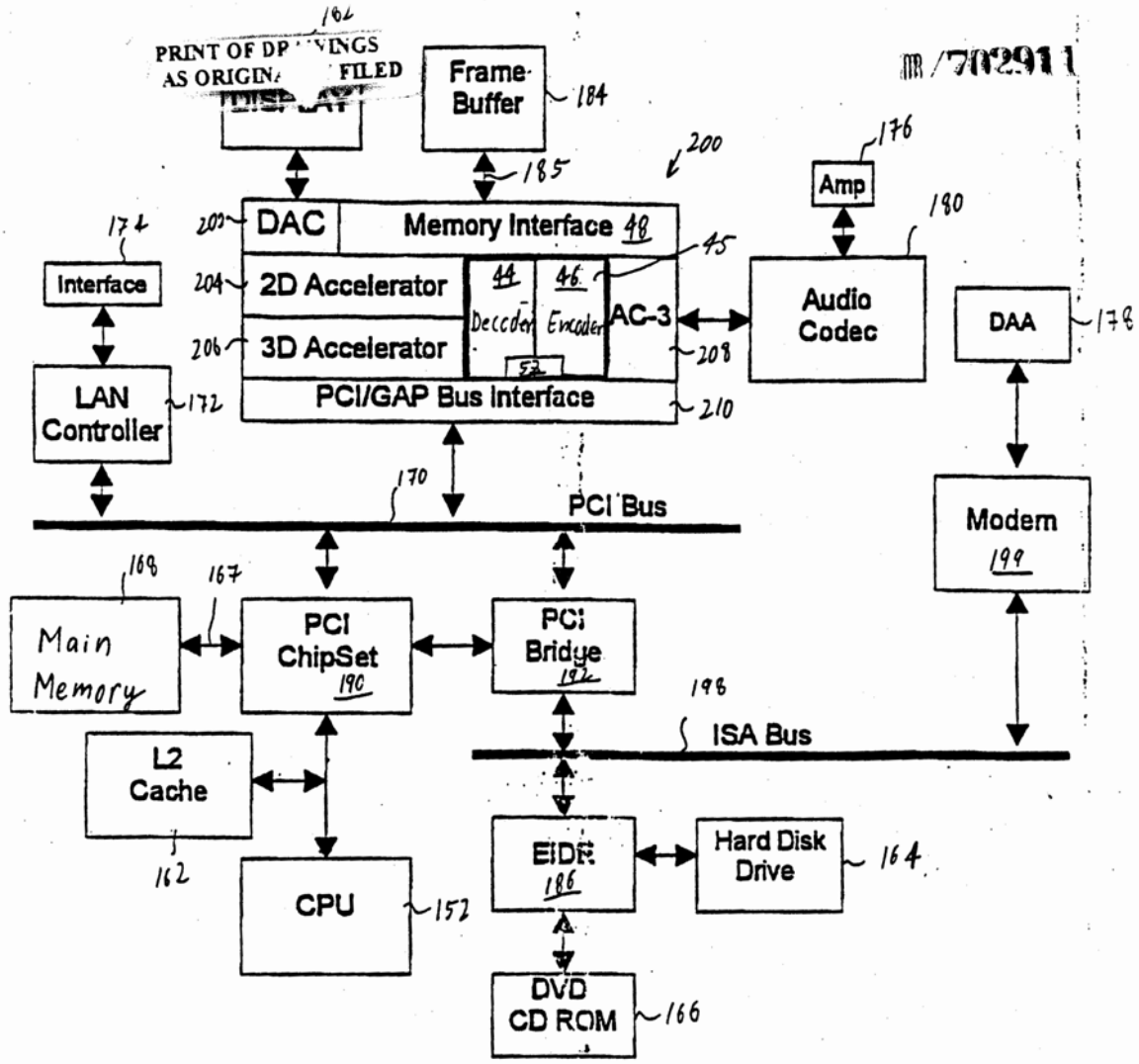


Figure 4

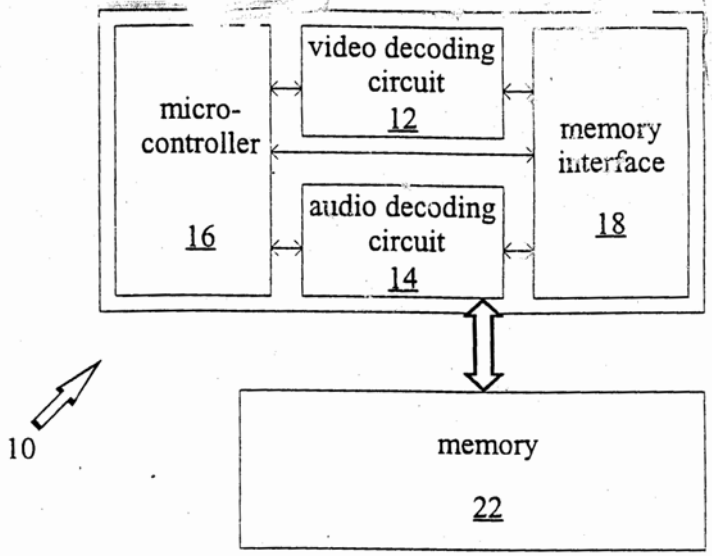


Figure 1a
(Prior Art)

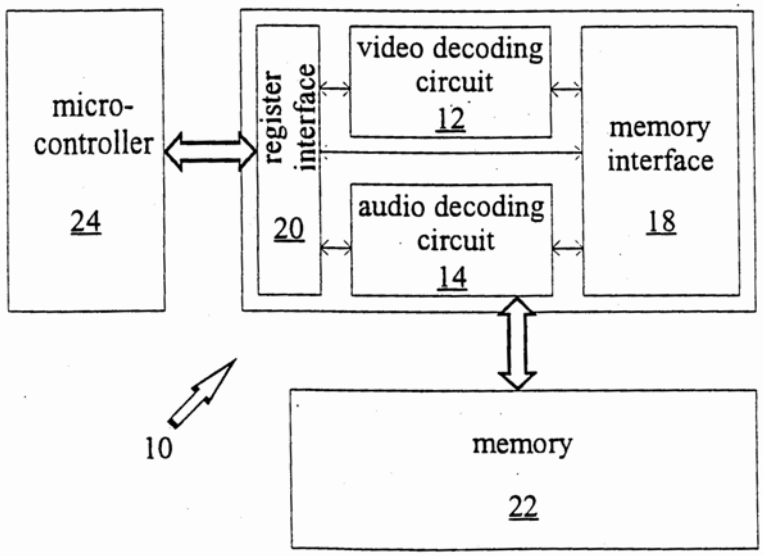


Figure 1b
(Prior Art)

PRINT OF DRAWINGS AS ORIGINALLY FILED

B/702911

Figure 1C
(Prior Art)

PRINT OF DR[illegible]INGS AS ORIGIN[illegible] FILED

[illegible]/702911

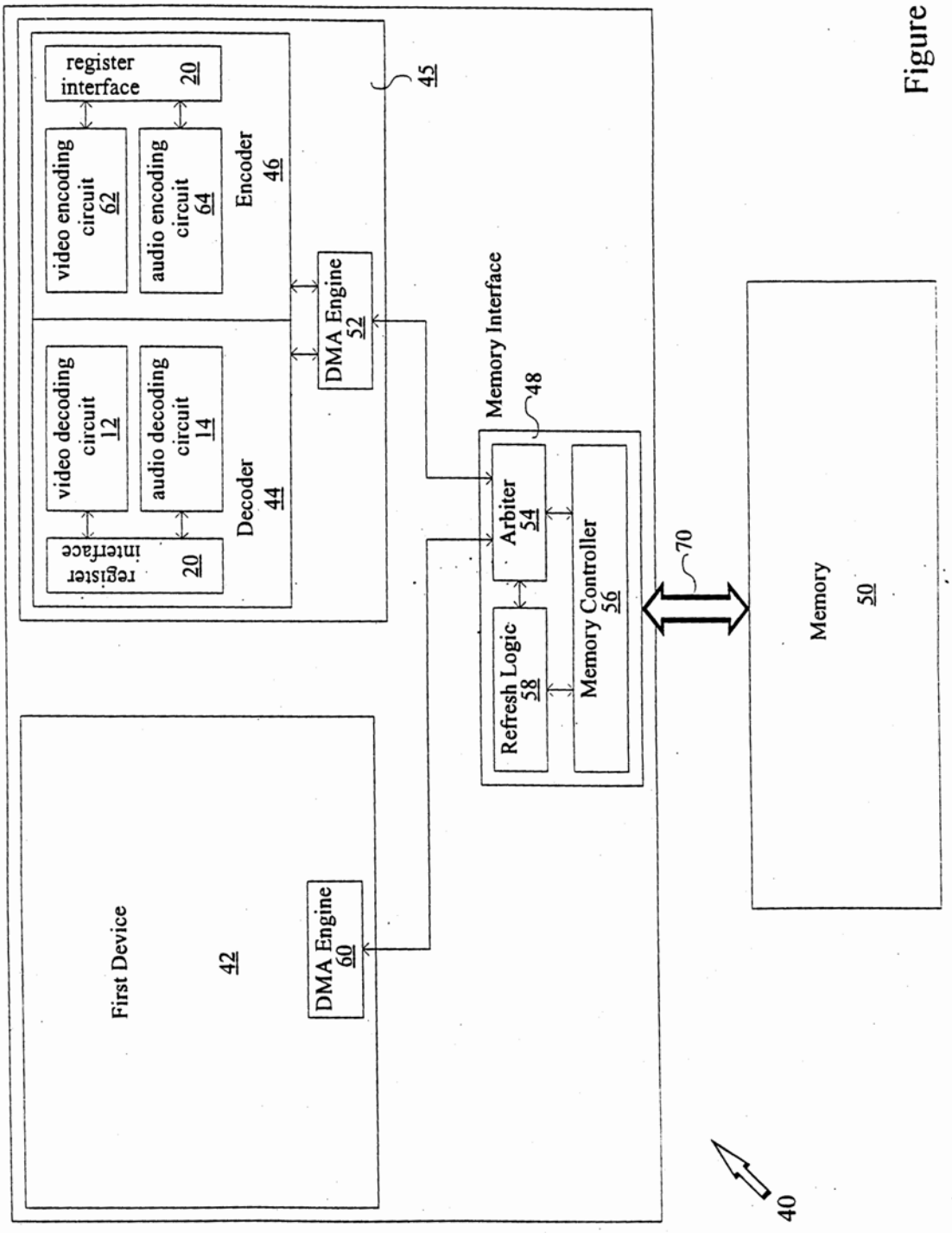


Figure 2

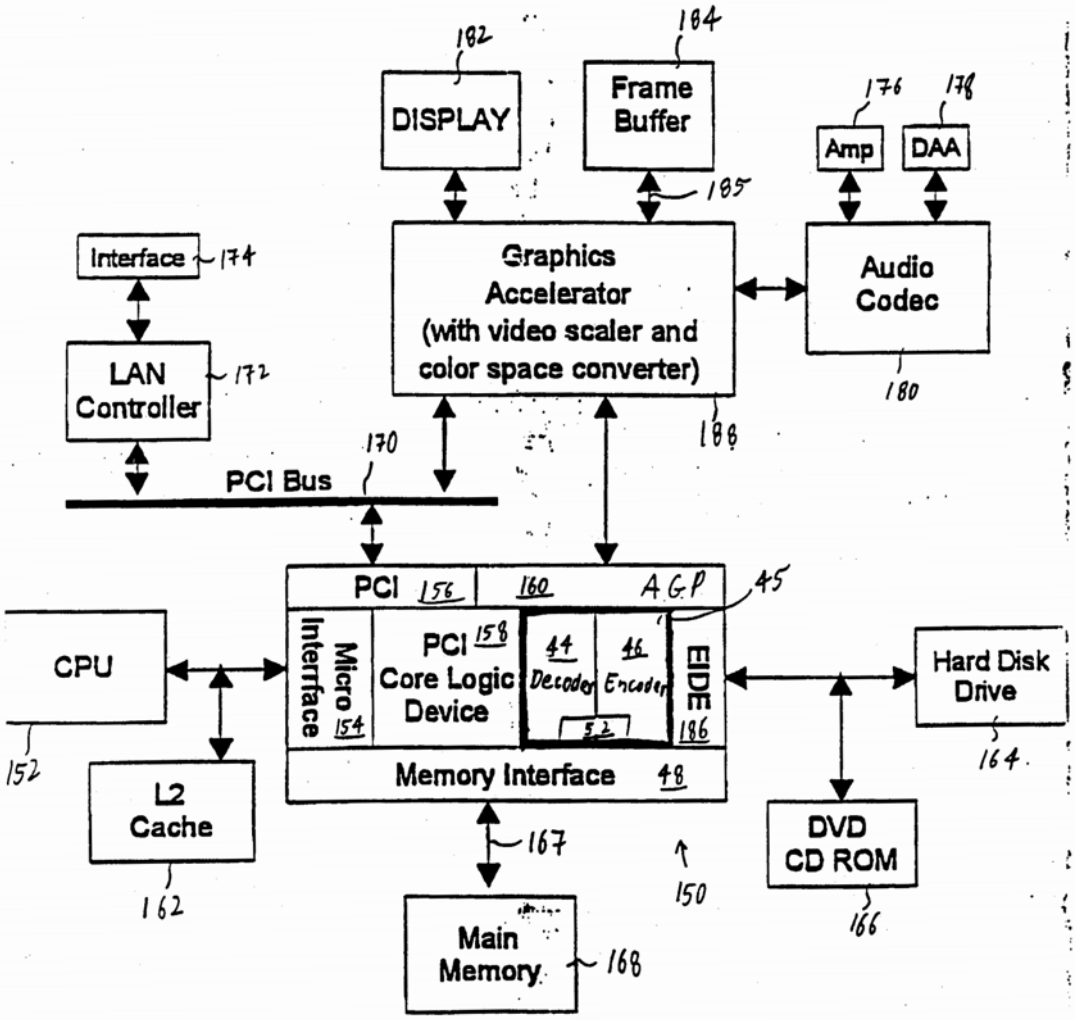


Figure 3

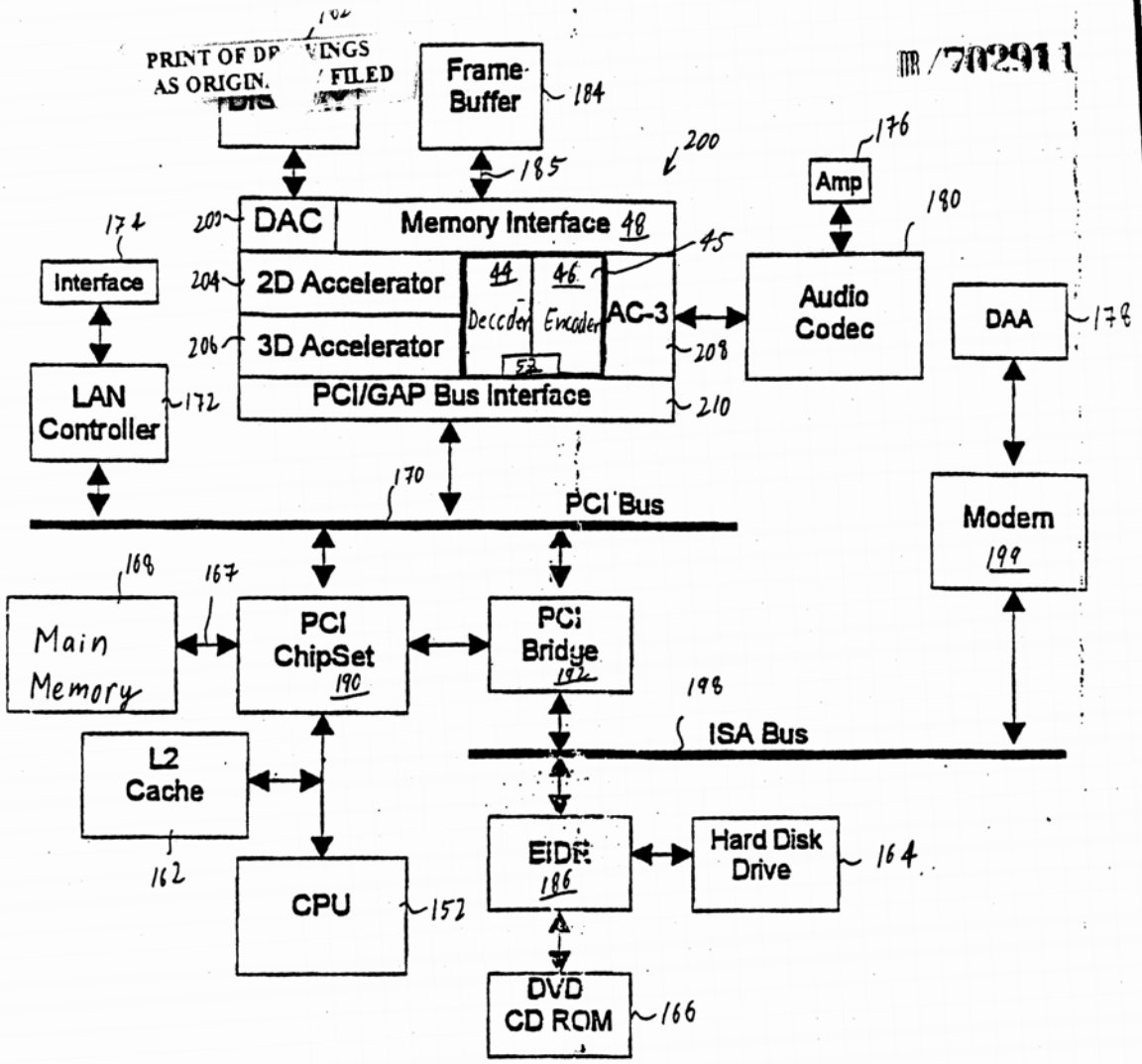


Figure 4

GP 2612

#28

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:
Raul Diaz et al.

2318
2/28/97

Examiner: NOT ASSIGNED

Serial No.: 08/702,911

Art Unit: 2318

Filed: August 23, 1996

Docket No: 96-S-11

For: Video and/or Audio Decompression and/or Compression Device that Shares a Memory Interface

INFORMATION DISCLOSURE STATEMENT UNDER C.F.R. 1.97

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

Applicants request that the information listed on the attached Form PTO-1449 be considered by the Office during the pendency of the above entitled application, pursuant to 37 C.F.R. 1.97.

Please charge any fees necessary for prosecution of the present application to deposit account no. 19-1353. If any extension of time is required, such extension is hereby requested. Please charge any additional required fee for extension of time to Applicant's Deposit Account No. 19-1353.

CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231, on Oct. 31, 1996.

Mary L. Kiesel
Signature

In accordance with 37 C.F.R. 1.97(h), the filing of this Information Disclosure Statement shall not constitute an admission that any information cited therein is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56(b). In the interest of full and complete disclosure to the Office, some or all of the art cited herein may not be considered by Applicant(s) or the Undersigned to be material under the new standards of materiality defined in 37 C.F.R 1.56(b), enacted March 16, 1992, but may be material under the old standard of materiality defined in 37 C.F.R. 1.56(a), last amended on November 28, 1988, or may merely be technical background which may be of interest to the Examiner. In accordance with 37 C.F.R. 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made.

This Information Disclosure Statement is being filed under 37 C.F.R. § 1.97(b) within three months of the filing date of the application, or before the mailing date of a first office action on the merits. No fee or certification is required.

Respectfully submitted,

Irena Lager
Registry No. 39,260
SGS-THOMSON Microelectronics, Inc.
1310 Electronics Drive
Carrollton, Texas 75006
(972) 466-7511

Attorney for Applicants

Form PTO 1449 Rev 7-80	U.S. Dept of Commerce Patent & Trademark Off.	Atty. Docket No. 96-S-11	Serial No. 08/702,911
		Applicant Raul Diaz et al.	
LIST OF PRIOR ART CITED BY APPLICANT (Use several sheets if necessary)		Filing Date August 23, 1996	Group

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
AA	5,459,519	10/17/95	Scalise et al.	348/431	
AB					

FOREIGN COUNTRIES

	DOC. NO.	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION
AC	0 673 171 A2	09/20/95	Europe	— —	English

OTHER PRIOR ART (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGE, ETC.)

AD	Bheda, H. and P. Srinivasan, "A High-Performance Cross-Platform MPEG Decoder," Digital Video Compression on Personal Computers: Algorithms and Technologies. SPIE Proceedings, February 7-8, 1994, Vo. 2187, pp. 241-248.
AE	Bursky, D., "Highly Integrated Controller Eases MPEG-2 Adoption," Electronic Design, August 21, 1995, Vol. 43, No. 17, pp. 141-142.
AF	Galbi, D. et al., "An MPEG-1 Audio/Video Decoder With Run-Length Compressed Antialiased Video Overlays," 1995 IEEE International Solid-State Circuits Conference, pp. 286-287, 381.
AG	Maturi, G., "Single Chip MPEG Audio Decoder," IEEE Transactions on Consumer Electronics, Vol. 38, No. 3, August 1992, pp. 348-356.
AH	Butler, B. and T. Mace, "The Great Leap Forward," PC Magazine, October 11, 1994, pp. 241-244, 246, 248, 250, 253-254, 256, 260-261, 264, 266-268, 273-275, 278.
AI	Doquilo, J., "Symmetric Multiprocessing Servers: Scaling the Performance Wall," Infoworld, March 27, 1995, pp. 82-85, 88-92.
AJ	Video Electronics Standards Association, "VESA Unified Memory Architecture Hardware Specifications Proposal," Version: 1.0p, October 31, 1995, pp. 1-38.
AK	Video Electronics Standards Association, "VESA Unified Memory Architecture VESA BIOS Extensions (VUMA-SBE Proposal," Version: 1.0p, November 1, 1995, pp. 1-26.
AL	Giorgis, T., "SMP Network Operating Systems," Computer Dealer News, Vol. 12, No. 16, August 8, 1996.

EXAMINER [signature] DATE CONSIDERED 8/20/97

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with PEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

TH

2612

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:
Raul Diaz et al.

Examiner:

Serial No.: 08/702,911

Art Unit:

Filed: August 23, 1996

Docket No: 96-S-11

For: Video and/or Audio Decompression and/or Compression Device that Shares a Memory Interface

INFORMATION DISCLOSURE STATEMENT UNDER C.F.R. 1.97

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

Applicants request that the information listed on the attached Form PTO-1449 be considered by the Office during the pendency of the above entitled application, pursuant to 37 C.F.R. 1.97.

Please charge any fees necessary for prosecution of the present application to deposit account no. 19-1353. If any extension of time is required, such extension is hereby requested. Please charge any additional required fee for extension of time to Applicant's Deposit Account No. 19-1353.

CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231, on NOV 11, 1996.

Kim Lawson
Signature

In accordance with 37 C.F.R. 1.97(h), the filing of this Information Disclosure Statement shall not constitute an admission that any information cited therein is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56(b). In the interest of full and complete disclosure to the Office, some or all of the art cited herein may not be considered by Applicant(s) or the Undersigned to be material under the new standards of materiality defined in 37 C.F.R 1.56(b), enacted March 16, 1992, but may be material under the old standard of materiality defined in 37 C.F.R. 1.56(a), last amended on November 28, 1988, or may merely be technical background which may be of interest to the Examiner. In accordance with 37 C.F.R. 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made.

This Information Disclosure Statement is being filed under 37 C.F.R. § 1.97(b) within three months of the filing date of the application, or before the mailing date of a first office action on the merits. No fee or certification is required.

Respectfully submitted,

Irena Lager
Registry No. 39,260
SGS-THOMSON Microelectronics, Inc.
1310 Electronics Drive
Carrollton, Texas 75006
(972) 466-7511

Attorney for Applicants

Form PTO 1449 Rev 7-80	U.S. Dept of Commerce Patent & Trademark Off.	Atty. Docket No. 96-S-011	Serial No. 08/702,911
LIST OF PRIOR ART CITED BY APPLICANT (Use several sheets if necessary)		Applicant Raul Diaz et al.	
		Filing Date August 23, 1996	Group

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
AA					
AB					
AC					
AD					
AE					
AF					
AG					
AH					
AI					
AJ					
AK					
AL					

FOREIGN COUNTRIES

	DOC. NO.	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION
AM					
AN					

OTHER PRIOR ART (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGE, ETC.)

AO	King, A., *Inside Windows 95*, Microsoft Press, Redmond, Washington, 1994, pp. 85-90.
AP	"MPEG Video Overview," *SGS-THOMSON Microelectronics Technical Note*, April 1992, pp. 1-4.
AQ	

EXAMINER [signature] DATE CONSIDERED 8/20/97

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with PEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

#4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:
Raul Z. Diaz et al.

Docket No.: 96-S-011

2318
2/28/97

Serial No.: 08/702,911

Examiner:

Filed: August 23, 1996

Art Unit: ~~2612~~ 2318

For: Video and/or audio decompression and/or compression device that shares a memory interface

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

PETITION TO SECURE FILING DATE AS OF

MAILING DATE VIA EXPRESS MAIL

Applicant petitions that this application be accorded the filing date on which the papers were sent "Express Mail Post Office to Addressee" mailing label no. EG947362259US on August 23, 1996.

CERTIFICATE OF MAILING (37 CFR 1.8a)
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231, on Feb 24, 1997.

Kim Larsen
Signature

SUBMISSIONS

Submitted herewith is:

1. A copy of the executed Express Mail certificate with mailing label number EG947362259US.
2. A copy of the Express Mail Receipt No. EG947362259US with a "date in" of August 24, 1996 as entered by the U.S. Postal Service.
3. Declaration of Kimberley K. Larson.
4. A copy of Collection Management System, Collection Point Inventory by Address (CPIA) for the U.S. Post Office, Dallas District.

Applicant respectfully requests that the above-referenced application be accorded a filing date of August 23, 1996 as shown by the attached declaration of Kimberley K. Larson and the attached CPIA from the U.S. Post Office. Applicant had a reasonable basis to believe that the correspondence placed in the Express Mail envelope and deposited in a U.S. Postal Service Mail box on August 23, 1996 would be picked up that same day and, therefore, the Express Mail label would have a "date in" of August 23, 1996. Therefore, Applicants request that the application be accorded a filing date of August 23, 1996 as specified in 37 C.F.R. §1.10(c) in effect on August 23, 1996.

PETITION FEE

The petition fee (37 CFR 1.17(h)) is hereby authorized to be charged to Deposit Account No. 19-1353 of SGS-THOMSON Microelectronics, Inc.

REQUEST FOR REFUND OF PETITION FEE

Because no defect exists in applicants' previous submission, a refund of the petition fee is respectfully requested.

Respectfully submitted,

Irena Lager
Reg. No. 39,260
SGS-THOMSON Microelectronics, Inc.
Mail Station 2346
1310 Electronics Dr.
Carrollton, Texas 75006
(972) 466-7511

Attorney for Applicant

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:
Raul Z. Diaz et al.

Docket No.: 96-S-011

Serial No.: 08/702,911

Examiner:

Filed: August 23, 1996

Art Unit: 2612

For: Video and/or audio decompression and/or compression device that shares a memory interface

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

DECLARATION OF KIMBERLEY K. LARSON

I, KIMBERLEY K. LARSON, do hereby take oath and swear as follows:

(1) I am employed as a patent secretary in the Patent Department of SGS-THOMSON Microelectronics, Inc.

(2) As part of my duties, I am responsible for the preparation of certain documents for transmittal to the Patent and Trademark Office, including ensuring that proper documents are present to be transmitted, organizing the documents to be transmitted and placing these documents in envelopes for transmittal.

(3) On August 23, 1996, I prepared an Express Mail mailing label bearing mailing label number EG947362259US addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231. I also prepared and signed a Certificate of Mailing by Express Mail dated August 23, 1996 with express mail mailing label number EG947362259US, a copy of which is attached hereto.

(4) Pursuant to the requirements of 37 CFR 1.10, I placed the correspondence in an Express Mail envelope and deposited the Express Mail envelope in a U.S. Express Mail mailbox on Friday, August 23, 1996 around 4:45 p.m. This was prior to the last designated pick-up time of 5:00 p.m for this U.S. Express Mail mailbox. Therefore, the certificate of Express Mailing and the application was deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on August 23, 1996 addressed to the Assistant Commissioner for Patents, Box Patent Applications, Washington, D.C. 20231. Attached is a copy of the collection times sent via facsimile from Vincent Lewis of the Consumer Affairs/Claims Division of the U.S. Postal Service. This facsimile shows the last collection time of 5:00 p.m. for the post office on 13904 Josey Lane where the Express Mail package was deposited.

(5) I am unaware as to the circumstances that caused our express mail package not be picked up and processed by the U.S. Postal Service until the next day, August 24, 1996. The above-referenced application was accorded a filing date of August 26, 1996, instead of August 23, 1996. A copy of the return postcard bearing a cancelled date of August 24, 1996, and an actual receipt date of August 26, 1996 is enclosed, along with a copy of the Express Mail Receipt No. EG947362259US with a postmark date of August 24, 1996.

I declare further that all statements made herein of my own knowledge are true; that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of this application and any registration resulting therefrom.

Signed at Carrollton, Texas this 24 day of February, 1997.

By: Kimberley K. Larson
Kimberley K. Larson

STATE OF TEXAS
COUNTY OF DALLAS

Subscribed and sworn to before me this 24th day of February, 1997

Mary L. Hiner
Notary Public

MARY L. HINER
Notary Public, State of Texas
My Commission Expires 02/22/99

/30/96
:01:15

COLLECTION MANAGEMENT SYSTEM

COLLECTION POINT INVENTORY BY ADDRESS
DALLAS DISTRICT OPS
961 W BETHEL RD
COPPELL TX 75099-9331

Page: 6

FARMERS BRANCH STATION (214)247-4591

ID	Box Address Description of Address Last Box in the Area Nearest Express Mail Box	Service Class Type of Box Button Number	Area of Box	Weekdays Coll by AM	Weekdays Coll by PM	Saturdays Coll by AM	Saturdays Coll by PM	Holidays Coll by AM	Holidays Coll by PM
10	11400 LUNA RD WESTWOOD BUSINESS PARK ENTRANCE 13904 JOSEY LN 13904 JOSEY LN	MIXED STANDARD 0000004AC84A	BUS	3478 3488	2:00 4:30		34908 12:00		
11	14280 MARSH LN SE MARSH & SPRING VALLEY 13904 JOSEY LN 13904 JOSEY LN	MIXED STANDARD 0000004AC51D	RES	3474 3484	2:00 4:30		34915 12:00		
13	7 MEDICAL PARKWAY NE WEBB CHAPEL & MEDICAL PKY 13904 JOSEY LN 13904 JOSEY LN	STAMPED STANDARD 0000004AC74A	BUS	3473 3483	2:00 4:30		34918 12:00		
17	7 MEDICAL PARKWAY NE WEBB CHAPEL & MEDICAL PKY 13904 JOSEY LN 13904 JOSEY LN	METERED STANDARD 0000004ACF8C	BUS	3473 3483	2:00 4:30		34915 12:00		
16	2270 VALLEY VIEW LN SOUTHEAST VALLEY VIEW/VALLEY BRANCH 13904 JOSEY LN 13904 JOSEY LN	MIXED STANDARD 0000004AC5EE	RES	3476 3486	2:00 6:00		34908 12:00		
16	2270 VALLEY VIEW LN SOUTHEAST VALLEY VIEW/VALLEY BRANCH 13904 JOSEY LN 13904 JOSEY LN	EXPRESS EXPRESS 0000004AD43A	RES	3476 3486	2:00 6:00		34908 12:00		
15	2570 VALLEY VIEW LN 2570 VALLEY VIEW & WILLIAM DODSON 13904 JOSEY LN 13904 JOSEY LN	MIXED STANDARD 0000004AC50F	RES	3476 3486	2:30 6:00		34906 12:30		
18	2655 VILLA CREEK DR ONE METRO SQUARE WEST LOBBY 13904 JOSEY LN 13904 JOSEY LN	MIXED WALL 0000004ACA53	BUS	3479 3489	2:00 4:30				
18	2665 VILLA CREEK DR TWO METRO SQUARE 13904 JOSEY LN 13904 JOSEY LN	MIXED WALL 0000004ACB00	BUS	3479 3489	2:00 4:30				
1	2695 VILLA CREEK DR TWO METRO SQUARE 13904 JOSEY LN 13904 JOSEY LN	MIXED WALL 0000004AC30A	BUS	3479 3489	2:00 4:30				
4			S	3479 3489	2:00 4:30				

OPTIONAL FORM 99 (7-90)

FAX TRANSMITTAL

# of pages ▶

To: Kim LAeson
Dept./Agency:
Fax #:

From: Vincent R. Lewis
Phone #: 972-393-6700
Fax #: 972-393 6770

NSN 7540-01-317-7368 5099-101 GENERAL SERVICES ADMINISTRATION

RECEIVED
MAR 19 1997
GROUP 2300

SGS-THOMSON MICROELECTRONICS

FAX Transmission **PATENT DEPARTMENT**

From:	IRENA LAGER	Date:	07/03/97
To:	OFFICE OF PETITIONS	Time:	10:40 AM
Company:	USPTO	FAX #:	703-308-6916

pages sent including this page: 13

Message:

RE: SERIAL NO.: 08/702,911
DOCKET NO.: 96-S-11

Following is a Status Report, and all documents referenced in the Status Report, for the above-referenced case.

FAX RECEIVED
JUL 3 1997
PETITIONS OFFICE

VOICE: 972-466-7511 FAX: 972-466-7044

MS 2346 - 1310 ELECTRONICS DRIVE- CARROLLTON, TX 75006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Raul Diaz et al. Art Unit: 2612

Serial No.: 08/702,911 Docket No.: 96-S-11

Filed: August 23, 1996

FOR: Video and/or Audio Decompression and/or Compression Device That Shares a Memory Interface

STATUS REPORT

Hon. Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

Please provide us with a Status Report on the above-referenced matter. A copy of the "Petition to Secure Filing Date as of Mail Date Via Express Mail" mailed February 24, 1997 along with a copy of the stamped return postcard indicating a receipt date of February 26, 1997 is enclosed. Please charge any fees necessary for prosecution of the present application to deposit account no. 19-1353.

Respectfully submitted:

Irena Lager
Reg. No. 39,260
Attorney for Applicant

FAX RECEIVED
JUL 3 1997
PETITIONS OFFICE

SGS-THOMSON Microelectronics, Inc.
1310 Electronics Drive/MS 2346
Carrollton, TX 75006
972-466-7511

CERTIFICATE OF MAILING
37 CFR 1.8(a)

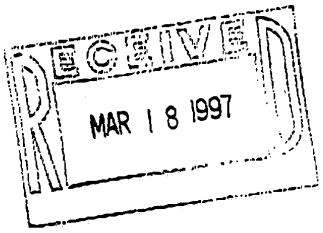
I hereby certify that the following papers are being facsimile transmitted to the Patent and Trademark Office (fax No. 703-308-6916) on the date shown below.

July 3, 1997 Kim Larson
Date Signature

Received in the U.S.P.T.O.:
Re: Raul Diaz et al.
Serial No.: 08/702,911
Docket No.: 96-S-11

1. Petition to Secure Filing Date as of Mailing Date Via Express Mail
2. Declaration of Kimberley K. Larson
3. Express Mail Certificate
4. Express Mail Receipt

Mailed: February 24, 1997



#4

2400
6/23/97

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:
Raul Z. Diaz et al.

Docket No.: 96-S-011

Serial No.: 08/702,911

Examiner:

Filed: August 23, 1996

Art Unit: 2612

For: Video and/or audio decompression and/or compression device that shares a memory interface

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

PETITION TO SECURE FILING DATE AS OF

MAILING DATE VIA EXPRESS MAIL

Applicant petitions that this application be accorded the filing date on which the papers were sent "Express Mail Post Office to Addressee" mailing label no. EG947362259US on August 23, 1996.

CERTIFICATE OF MAILING (37 CFR 1.8a)
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231, on Feb 24, 1997.

Signature

SUBMISSIONS

Submitted herewith is:

1. A copy of the executed Express Mail certificate with mailing label number EG947362259US.
2. A copy of the Express Mail Receipt No. EG947362259US with a "date in" of August 24, 1996 as entered by the U.S. Postal Service.
3. Declaration of Kimberley K. Larson.
4. A copy of Collection Management System, Collection Point Inventory by Address (CPIA) for the U.S. Post Office, Dallas District.

Applicant respectfully requests that the above-referenced application be accorded a filing date of August 23, 1996 as shown by the attached declaration of Kimberley K. Larson and the attached CPIA from the U.S. Post Office. Applicant had a reasonable basis to believe that the correspondence placed in the Express Mail envelope and deposited in a U.S. Postal Service Mail box on August 23, 1996 would be picked up that same day and, therefore, the Express Mail label would have a "date in" of August 23, 1996. Therefore, Applicants request that the application be accorded a filing date of August 23, 1996 as specified in 37 C.F.R. §1.10(c) in effect on August 23, 1996.

PETITION FEE

The petition fee (37 CFR 1.17(h)) is hereby authorized to be charged to Deposit Account No. 19-1353 of SGS-THOMSON Microelectronics, Inc.

REQUEST FOR REFUND OF PETITION FEE

Because no defect exists in applicants' previous submission, a refund of the petition fee is respectfully requested.

Respectfully submitted,

Irena Lager
Reg. No. 39,260
SGS-THOMSON Microelectronics, Inc.
Mail Station 2346
1310 Electronics Dr.
Carrollton, Texas 75006
(972) 466-7511

Attorney for Applicant

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:
Raul Z. Diaz et al.

Docket No.: 96-S-011

Serial No.: 08/702,911

Examiner:

Filed: August 23, 1996

Art Unit: 2612

For: Video and/or audio decompression and/or compression device that shares a memory interface

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

DECLARATION OF KIMBERLEY K. LARSON

I, KIMBERLEY K. LARSON, do hereby take oath and swear as follows:

(1) I am employed as a patent secretary in the Patent Department of SGS-THOMSON Microelectronics, Inc.

(2) As part of my duties, I am responsible for the preparation of certain documents for transmittal to the Patent and Trademark Office, including ensuring that proper documents are present to be transmitted, organizing the documents to be transmitted and placing these documents in envelopes for transmittal.

(3) On August 23, 1996, I prepared an Express Mail mailing label bearing mailing label number EG947362259US addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231. I also prepared and signed a Certificate of Mailing by Express Mail dated August 23, 1996 with express mail mailing label number EG947362259US, a copy of which is attached hereto.

(4) Pursuant to the requirements of 37 CFR 1.10, I placed the correspondence in an Express Mail envelope and deposited the Express Mail envelope in a U.S. Express Mail mailbox on Friday, August 23, 1996 around 4:45 p.m. This was prior to the last designated pick-up time of 5:00 p.m for this U.S. Express Mail mailbox. Therefore, the certificate of Express Mailing and the application was deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on August 23, 1996 addressed to the Assistant Commissioner for Patents, Box Patent Applications, Washington, D.C. 20231. Attached is a copy of the collection times sent via facsimile from Vincent Lewis of the Consumer Affairs/Claims Division of the U.S. Postal Service. This facsimile shows the last collection time of 5:00 p.m. for the post office on 13904 Josey Lane where the Express Mail package was deposited.

(5) I am unaware as to the circumstances that caused our express mail package not be picked up and processed by the U.S. Postal Service until the next day, August 24, 1996. The above-referenced application was accorded a filing date of August 26, 1996, instead of August 23, 1996. A copy of the return postcard bearing a cancelled date of August 24, 1996, and an actual receipt date of August 26, 1996 is enclosed, along with a copy of the Express Mail Receipt No. EG947362259US with a postmark date of August 24, 1996.

I declare further that all statements made herein of my own knowledge are true; that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of this application and any registration resulting therefrom.

Signed at Carrollton, Texas this 24 day of February, 1997.

By: Kimberley K. Larson
Kimberley K. Larson

STATE OF TEXAS
COUNTY OF DALLAS

Subscribed and sworn to before me this 24th day of February, 1997

Mary L. Hiner
Notary Public

MARY L. HINER
Notary Public, State of Texas
My Commission Expires 02/22/99

Received in the U.S.P.T.O.:

Re: Raul Diaz and Jeff Owen
Docket No.: 96-S-11
For: Video and/or audio decompression and/or compression device that shares a memory interface
Enclosed:
1. Patent specification, claims & Abstract
2. Five (5) pages of drawings
3. Declaration and Power of Attorney
4. Transmittal Letter + 1 copy
5. Certificate of Mailing
6. Assignment and Assignment Recordal Form
7. Check in the amount of $1,396.00
Mailed: August 23, 1996

08/702,911

DALLAS DISTRICT OPS
951 W BETHEL RD
COPPELL TX 75099-9331

FARMERS BRANCH STATION (214)247-4691

ID	Box Address Description of Address Last Box in the Area Nearest Express Mail Box	Service Class Type of Box Button Number	Area of Box	Weekdays Coll by	AM	Coll by	PM	Saturdays Coll by	AM	Coll by	PM	Holidays Coll by	AM	Coll by	PM
10	11400 LUNA RD WESTWOOD BUSINESS PARK ENTRANCE 13904 JOSEY LN 13904 JOSEY LN	MIXED STANDARD 0000004AC04A	BUS			3478 3490	2:00 4:30			34908	12:00				
11	14280 MARSH LN SE MARSH & SPRING VALLEY 13904 JOSEY LN 13904 JOSEY LN	MIXED STANDARD 0000004AC51D	RES			3478 3494	2:00 4:30			34915	12:00				
13	7 MEDICAL PARKWAY NE WEBB CHAPEL & MEDICAL PKY 13904 JOSEY LN 13904 JOSEY LN	STAMPED STANDARD 0000004AC74A	BUS			3473 3483	2:00 4:30			34918	12:00				
17	7 MEDICAL PARKWAY NE WEBB CHAPEL & MEDICAL PKY 13904 JOSEY LN 13904 JOSEY LN	METERED STANDARD 0000004ACF6C	BUS			3473 3483	2:00 4:30			34918	12:00				
18	2270 VALLEY VIEW LN SOUTHEAST VALLEY VIEW/VALLEY BRANCH 13904 JOSEY LN 13904 JOSEY LN	MIXED STANDARD 0000004AC5EE	RES			3478 3488	2:00 6:00			34905	12:00				
18	2270 VALLEY VIEW LN SOUTHEAST VALLEY VIEW/VALLEY BRANCH 13904 JOSEY LN 13904 JOSEY LN	EXPRESS EXPRESS 0000004AD43A	RES			3478 3488	2:00 6:00			34908	12:00				
18	2670 VALLEY VIEW LN 2670 VALLEY VIEW & WILLIAM DODSON 13904 JOSEY LN 13904 JOSEY LN	MIXED STANDARD 0000004AC50F	RES			3478 3488	2:00 6:00			34906	12:00				
9	2055 VILLA CREEK DR ONE METRO SQUARE WEST LOBBY 13904 JOSEY LN 13904 JOSEY LN	MIXED WALL 0000004ACA52	BUS			3478 3489	2:00 4:30								
9	2055 VILLA CREEK DR TWO METRO SQUARE 13904 JOSEY LN 13904 JOSEY LN	MIXED WALL 0000004AC800	BUS			3478 3489	2:00 4:30								
	2055 VILLA CREEK DR TWO METRO SQUARE 13904 JOSEY LN 13904 JOSEY LN	MIXED WALL 0000004AC3DA	BUS			3478 3489	2:00 4:30								
			S			3478 3489	2:00 4:30								

OPTIONAL FORM 99 (7-90)

FAX TRANSMITTAL # of pages ▶

To Kim LAeson	From Vincent L. Lewis
Dept./Agency	Phone # 972-393-6700
Fax #	Fax # 972-392-6770

NSN 7540-01-317-7368 5099-101 GENERAL SERVICES ADMINISTRATION

JUL 03 '97 10:35AM SGS-THOMSON LEGAL P.11

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. 96-S-011

In Re Application of:

Raul Z. Diaz and Jefferson E. Owen

For: **Video and/or Audio Decompression and/or Compression Device that Shares a Memory Interface**

CERTIFICATE OF EXPRESS MAIL

"EXPRESS MAIL" NO. EG947362259US

EG947362259US

Date of Deposit: August 23, 1996

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Signature of person mailing paper or fee

JUL 03 SGS-THOMSON LEGAL

POST OFFICE TO ADDRESSEE

EXPRESS MAIL

EG947362259US

CUSTOMER COPY

SEE REVERSE SIDE FOR THE SERVICE GUARANTEE AND LIMITS ON THE INSURANCE COVERAGE

ORIGIN (POSTAL USE ONLY)

CUSTOMER USE ONLY

METHOD OF PAYMENT:

Express Mail Corporate Acct. No.

Federal Agency Acct. No. or Postal Service Acct. No.

FROM: (PLEASE PRINT) PHONE

Lisa K. Jorgenson
408-782-6850 Microelectronics
1310 Electronics Dr.
MS 2346
Carrollton, TX 75006

96-8-13

TO: (PLEASE PRINT) PHONE

Assistant Commissioner for Patents
Box Patent Applications
Washington, D.C. 20231

For Pickup or Tracking Call 1-800-222-1811

LABEL 11-B 5/94

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER OF
PATENTS AND TRADEMARKS
Washington, D.C. 20231

#5

Lisa K. Jorgenson
SGS Thomson Microelectronics Inc.
1310 Electronics Drive
Carrollton, TX 75006

In re Application of	:	
Raul Z. Diaz et al.	:	DECISION DISMISSING
Application No. 08/702,911	:	PETITION
Filed: August 26, 1996	:	
Attorney Docket No. 96-S11	:	

This is a decision on the petition filed February 26, 1997, requesting that the above-identified application be accorded a filing date of August 23, 1996, rather than the presently accorded filing date of August 26, 1996.

Petitioners request the earlier filing date on the basis that the application was purportedly deposited in Express Mail service on August 23, 1996, pursuant to the requirements of 37 CFR 1.10. Petitioners acknowledge that the date of deposit in Express Mail shown on petitioners' Express Mail receipt is August 24, 1996, a Saturday, but argue that the application was actually deposited in an Express Mail drop box on August 23, 1996, before the last scheduled pick up for the day.

Paragraph (c) of 37 CFR 1.10 stated on August 23, 1996, that:

> "the...Office will accept the certificate of mailing by 'Express Mail' and accord the paper or fee the certificate date under 35 U.S.C. 21(a)... without further proof of the date on which the mailing by 'Express Mail' occurred unless a question is present regarding the date of mailing."

However, on May 16, 1995, the Commissioner waived the requirement for a certificate of mailing under 37 CFR 1.10. See 1174 Off. Gaz. Pat. Office 92. The Commissioner noted that the certificate of mailing under 37 CFR 1.10 is redundant in view of the fact that the date of deposit in Express Mail is entered as the "Date-In" on the Express Mail label by the U.S. Postal Service (USPS). Thus, the PTO considers the date "the paper or fee is shown to have been deposited as Express Mail" to be the "Date-In" on the Express Mail label.

Placing the "Date-In" on the Express Mail label or receipt by the postal clerk establishes that the package was actually received by the USPS. That is the date that verifies that the package was actually mailed. Accordingly, the application was accorded a filing date of August 26, 1996, the next business following the date of deposit in Express Mail service.

Petitioners allege that the date of deposit in Express Mail shown by petitioners' Express Mail receipt is a USPS error. In support, the petition is accompanied by a declaration of Kimberley K. Larson stating her recollection that the Express Mail package she deposited six (6) months earlier was deposited in an Express Mail drop box at about 4:45 p.m. and that the last pickup for the day at that particular drop box was 5:00 p.m.

The arguments and evidence presented have been considered, but are not persuasive. Petitioners' Express Mail receipt is considered to be more probative of the correct date of deposit than the declaration presented with the petition, because the Express Mail receipt was completed by the USPS contemporaneously with the processing of the Express Mail package by the USPS while the Larson declaration was made six (6) months after the date of mailing. Postal employees are presumed to discharge their duties in a proper manner. Charlson Realty Co. v. United States, 690 F.2d 434, 442 (Ct. Cl. 1967). Therefore, in view of the August 24, 1996 "date-in" shown on the Express Mail receipt it is concluded that the Express Mail package in question must have been deposited either after the last scheduled pickup for the day on August 23, 1996, or on Saturday, August 24, 1996. It is petitioners' burden to establish to the satisfaction of the Commissioner that the August 24, 1996 "Date-In" on Express Mail label No. EG947362259US is the result of

an error on the part of an employee of the USPS. However, no statement from the USPS has been presented verifying that any error was made by the USPS in the processing of petitioners' Express Mail package. Petitioners were made aware of the date of deposit in Express Mail acknowledged by the USPS upon return of petitioners' Express Mail receipt to counsel's office. It is not understood why petitioners did not obtain a statement in writing from the USPS acknowledging an error in the processing of petitioners' Express Mail package immediately after receiving the Express Mail receipt. It is also unfortunate that petitioners chose to deposit a paper as important as a patent application in Express Mail without immediately obtaining an Express Mail receipt showing the desired date of deposit. Since the date of mailing is established by the rule as the date shown by the Express Mail receipt and petitioners' receipt shows a date of mailing of August 24, 1996, the application was correctly accorded a filing date of August 26, 1996.

The petition is dismissed.

Any request for reconsideration should be filed within TWO MONTHS of the date of this decision in order to be considered timely. See 37 CFR 1.181(f). This time period may not be extended pursuant to 37 CFR 1.136(a) or (b).

Further correspondence with respect to this matter should be addressed as follows:

By mail: Assistant Commissioner for Patents
Box DAC
Washington, D.C. 20231

By FAX: (703) 308-6916
Attn: Special Program Law Office

By hand: One Crystal Park, Suite 520
2011 Crystal Drive
Arlington, VA

The application is being returned to Examining Group 2400 for examination in due course with the presently accorded filing date of August 26, 1996.

Telephone inquiries specific to this matter should be directed to the undersigned at (703) 305-9282.

John F. Gonzales
Senior Legal Advisor
Special Program Law Office
Office of the Deputy Assistant Commissioner
for Patent Policy and Projects

JFG

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231 NM

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/702,911	08/26/96	DIAZ	R 96-S-11

B3M1/0903

LISA K JORGENSON
SGS THOMSON MICROELECTRONICS INC
1310 ELECTRONICS DRIVE
CARROLLTON TX 75006

EXAMINER	
RAMIREZ,E	
ART UNIT	PAPER NUMBER
2414	6

DATE MAILED: 09/03/97

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 03 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-49 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-49. is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of Reference Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2 & 3

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

-- SEE OFFICE ACTION ON THE FOLLOWING PAGES --

PTOL-326 (Rev. 10/95) ★ U.S. GPO: 1996-409-290/40...

1. This Application has been examined.

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-49 are rejected under 35 U.S.C. 102(B) as being clearly anticipated by Lin et al..

The publication of Lin discloses in Figure one a MPEG II decoder which employs memory interface which uses bus arbitration to allocate resources between the decoder and another device. The arbitration scheme, see figure 3, allocates access to the memory on a priority level. The basic requirement of having the interface and the decoder be monolithic is presumed from figures one since both component are found in the rectangle box, and the introduction which discloses uses in " TV set-top boxes, PC add-on and entertainment machines."

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Retter et al. (US Patent 5,557,538) in view of Harney (US Patent 5,522,080).

Retter discloses the prior art devices employed in the compression and decompression of video and audio data. Retter diploses most of the requirements of the claimed invention with the exception of having a memory interface employing an arbitration routine. Though not expressly reciting an arbitration routine the patent does concern itself with managing " an internal bidirectional bus on which all data transfers between the external DRAM buffer and all the internal units." It would stand to reason that Retter must determine who has priority of the DRAM or must settle contentions if one arises when clients are accessing the same resource simultaneously. The Patent to Harney discloses a an arbitration scheme in the same environment as the patent to Retter:

> Additionally, it is permitted to impose no relative local priority within Group III if all three types of request are equally likely and equally important. In this alternate embodiment of method x the transfers

> of Group III are processed on a first come, first served basis. There is by definition arbitration between transfers involving the system bus because system 300 contains two hi-directional burst buffers which allow up to sixteen word transfers to be captured. It also contains a set of dual scaler buffers, which are used to capture scaler accesses. These buffers allow scaler and burst request to be performed even if the bus resource is unavailable.
> With respect to Group III local arbitration , the band width requirements are highly dependent upon system configuration.
> The functions performed by block transfer controller 368 during block data transfers of data between global memory 366 and local memories 362a-n include arbitration of transfer requests of competing global memory 366 and execution units 360a-n, address generation and control for two-dimensional block transfers between global memory 366 and local memories 362a-n, control for scalar, first-in first-out, and statistical decoder transfers between local memories 362a-n and global memory 366 and address generation and control for block instruction load following cache miss.
> A number of different types of transfers requiring input/output access arbitration by block transfer controller 368 may take place between global memory 366 and local memories 362a-n. These include fetching instructions from global memory 366. Image processor system 300 initializes the process by downloading instructions from system memory 364 to global memory 366. On power up of image processor 300 the instructions are loaded from system memory 364 or global memory 366 into the controller.
> Different types of transfers may be prioritized by block transfer controller 368 as follows, proceeding from highest priority to lowest priority: (1) instruction, (2) scalar, first-in, first-out and statistical decoder, and (3) block transfer. Thus block transfer controller 368 not only prioritizes and arbitrates within image processor 300 based upon whether a request is an instruction type of request or a data type of request. Block transfer controller 368 also prioritizes and arbitrates based upon the subtypes of data. Column 21, lines 1-30.

Harney recognizes the problem associated with systems, like Retter, which have multiple processors requiring access to the same resource. In column 3, lines 9-12, Harney discloses that

to allow each datapath (i.e., process) to have a independent access to external memory is impractical for semiconductor implementation. A sharing of resources is proposed and elucidated upon by the patent.

Therefore, it would have been obvious to those of ordinary skill in the art, at the time of the invention, to combine the Retter patent with the patent of Harney because when the same resource is required by multiple users and since it would be impractical to have independent or exclusive access, an arbitration scheme would insures the most optimal means of assuring prompt resolution of contentions and a judicial process for allocating the memory pie.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Primary Examiner Ellis B. Ramirez, Esq.,** whose telephone number is (703) 305-9786. The examiner can normally be reached on Monday-Friday from 7:30 AM to 6:00 PM . If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, E. Voeltz, can be reached on (703) 305-9714. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703)308-5356 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

ELLIS B. RAMIREZ
PRIMARY EXAMINER
GROUP 2400

Notice of References Cited

Application No.	Applicant(s)		
08/702,911	Diaz et al.		
Examiner		Group Art Unit	Page 1 of 1
Ellis B. Ramirez		2414	

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
	A	5,557,538	9/17/96	Retter et al.	348	402
	B	5,598,525	1/28/97	Nally et al.	395	507
	C	5,027,400	6/25/91	Baji et al.	348	10
	D	5,371,893	12/6/94	Price et al.	395	729
	E	5,623,672	4/22/97	Poppat	395	729
	F	5,522,080	5/28/96	Harney et al.	395	729
	G	5,621,893	4/15/97	Joh	395	200.82
	H	4,774,660	9/27/88	Conforti	395	729
	I	4,894,565	1/16/90	Marquardt	395	729
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	U	"ON THE BUS ARBITRATION FOR MPEG 2 VIDEO DECODER" ; VLSI Tech, System And Application, !995 Symposium	1995
	V	"A LOW COST GRAPHICS AND MULTIMEDIA WORKSTATIONM CHIP SET"; IEEE Micro	1994
	W		
	X		

#7
8. 3rd
3/20/98

PATENT

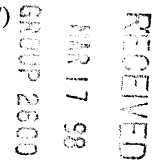
I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Assistant Commissioner for Patents, 2011 Jefferson Davis Highway, Washington, DC 20231.

March 3, 1998 — Date

E. Russell Tarleton — E. Russell Tarleton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Raul Z. Diaz et al.
Application No.	:	08/702,911
Filed	:	August 26, 1996
For	:	VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE
Examiner	:	E. Ramirez
Art Unit	:	2414
Docket No.	:	96-S-11 (850063.517)
Date	:	March 3, 1998



Assistant Commissioner for Patents
2011 Jefferson Davis Highway
Washington, DC 20231

PETITION FOR AN EXTENSION OF TIME
UNDER 37 C.F.R. § 1.136(a)

Sir:

Applicants herewith petition the Assistant Commissioner of Patents under 37 C.F.R. § 1.136(a) for a three-month extension of time for filing the response to the Examiner's Action dated September 3, 1997, from December 3, 1997 to March 3, 1998. Submitted herewith is a check in the amount of $950 to cover the cost of the extension.

Any deficiency or overpayment should be charged or credited to Deposit Account No. 19-1090. This petition is being submitted in triplicate.

Respectfully submitted,
Raul Z. Diaz et al.
SEED and BERRY LLP

E. Russell Tarleton
E. Russell Tarleton
Registration No. 31,800

ERT:jb
Enclosures:
Two copies of this Petition

6300 Columbia Center
701 Fifth Avenue
Seattle, Washington 98104-7092
(206) 622-4900
Fax: (206) 682-6031
users:\joanneb\ert98\0092

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Raul Z. Diaz et al.
Application No.	:	08/702,911
Filed	:	August 26, 1996
For	:	VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE

Examiner	:	E. Ramirez
Art Unit	:	2414
Docket No.	:	96-S-11 (850063.517)
Date	:	March 3, 1998

Assistant Commissioner for Patents
2011 Jefferson Davis Highway
Washington, DC 20231

GENERAL AUTHORIZATION UNDER 37 C.F.R. § 1.136(a)(3)

Sir:

With respect to the above-identified application, the Assistant Commissioner is authorized to treat any concurrent or future reply requiring a petition for an extension of time under 37 C.F.R. § 1.136(a)(3) for its timely submission as incorporating a petition therefor for the appropriate length of time. The Assistant Commissioner is also authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account No. 19-1090.

Respectfully submitted,
Raul Z. Diaz et al.
SEED and BERRY LLP

E. Russell Tarleton
Registration No. 31,800

ERT:jb
SEED and BERRY LLP
6300 Columbia Center
701 Fifth Avenue
Seattle, Washington 98104-7092
(206) 622-4900
FAX: (206) 682-6031

users:\joanneb\ert98\0091

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Assistant Commissioner for Patents, 2011 Jefferson Davis Highway, Washington, DC 20231.

March 3, 1998 — E. Russell Tarleton
Date — E. Russell Tarleton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Raul Z. Diaz et al.
Application No.	:	08/702,911
Filed	:	August 26, 1996
For	:	VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE
Examiner	:	E. Ramirez
Art Unit	:	2414
Docket No.	:	96-S-11 (850063.517)
Date	:	March 3, 1998

RECEIVED
MAR 17 98
GROUP 2600

Assistant Commissioner for Patents
2011 Jefferson Davis Highway
Washington, DC 20231

PETITION FOR AN EXTENSION OF TIME
UNDER 37 C.F.R. § 1.136(a)

Sir:

Applicants herewith petition the Assistant Commissioner of Patents under 37 C.F.R. § 1.136(a) for a three-month extension of time for filing the response to the Examiner's Action dated September 3, 1997, from December 3, 1997 to March 3, 1998. Submitted herewith is a check in the amount of $950 to cover the cost of the extension.

Any deficiency or overpayment should be charged or credited to Deposit Account No. 19-1090. This petition is being submitted in triplicate.

Respectfully submitted,
Raul Z. Diaz et al.
SEED and BERRY LLP

E. Russell Tarleton
Registration No. 31,800

ERT:jb
Enclosures:
Two copies of this Petition

6300 Columbia Center
701 Fifth Avenue
Seattle, Washington 98104-7092
(206) 622-4900
Fax: (206) 682-6031
users:\joanneb\ert98\0092

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Assistant Commissioner for Patents, 2011 Jefferson Davis Highway, Washington, DC 20231.

March 3, 1998 — E. Russell Tarleton

Date — E. Russell Tarleton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Raul Z. Diaz et al.
Application No.	:	08/702,911
Filed	:	August 26, 1996
For	:	VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE
Examiner	:	E. Ramirez
Art Unit	:	2414
Docket No.	:	96-S-11 (850063.517)
Date	:	March 3, 1998

Assistant Commissioner for Patents
2011 Jefferson Davis Highway
Washington, DC 20231

PETITION FOR AN EXTENSION OF TIME
UNDER 37 C.F.R. § 1.136(a)

Sir:

Applicants herewith petition the Assistant Commissioner of Patents under 37 C.F.R. § 1.136(a) for a three-month extension of time for filing the response to the Examiner's Action dated September 3, 1997, from December 3, 1997 to March 3, 1998. Submitted herewith is a check in the amount of $950 to cover the cost of the extension.

Any deficiency or overpayment should be charged or credited to Deposit Account No. 19-1090. This petition is being submitted in triplicate.

Respectfully submitted,
Raul Z. Diaz et al.
SEED and BERRY LLP

E. Russell Tarleton
Registration No. 31,800

ERT:jb
Enclosures:
Two copies of this Petition

6300 Columbia Center
701 Fifth Avenue
Seattle, Washington 98104-7092
(206) 622-4900
Fax: (206) 682-6031
users:\joanneb\ert98\0092

FORM PTO-1083

S -THOMSON MICROELECTRONI INC.
1310 Electronics Drive
Carrollton, Texas 75006-5039
Phone (972) 466-6000
Fax (972) 466-7044

Gm-2444 $
2756

MAR 0 9 1998

Docket No.: **96-S-11**
Date: **March 3, 1998**

#8

In re application of **Raul Z. Diaz et al.**
Application No.: **08/702,911**
Filed: **August 26, 1996**
For: **VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE**

ASSISTANT COMMISSIONER FOR PATENTS
2011 JEFFERSON DAVIS HIGHWAY
WASHINGTON DC 20231

RECEIVED
MAR 17 98
GROUP 2600

Sir:

Transmitted herewith is **an amendment** in the above-identified application.

[X] A Petition for an Extension of Time for three months is enclosed.
[X] No additional claim fee is required.
[] The fee has been calculated as shown.

	(Col. 1)		(Col. 2)	(Col. 3)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST PREV. PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
TOTAL	* 33	MINUS	** 49	0	x 11	$		x 22	$
INDEP.	* 3	MINUS	*** 5	0	x 41	$		x 82	$
[ ] FIRST PRESENTATION OF MULTIPLE CLAIMS					+ 135	$	OR	+ 270	$
EXTENSION OF TIME FEE						$			$ 950
TOTAL ADDITIONAL FEE						$	TOTAL		$ 950

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior amendment or the number of claims originally filed.

[] Please charge my Deposit Account No. 19-1090 in the amount of $_. A duplicate copy of this sheet is enclosed.
[X] A check in the amount of $ 950 is attached.
[X] The Assistant Commissioner is hereby authorized to charge payment of the following additional fees associated with this communication or credit any overpayment to Deposit Account No. 19-1090 . A duplicate copy of this sheet is enclosed.
[X] Any filing fees under 37 CFR 1.16 for the presentation of extra claims.
[X] Any patent application processing fees under 37 CFR 1.17.

03/11/1998 BHINES 00000030 08702911
01 FC:117 950.00 OP

Respectfully submitted,

SGS-Thomson Microelectronics, Inc.

E. Russell Tarleton

E. Russell Tarleton
Registration No. 31,800

users:\joanneb\ert98\0093

FORM PTO-1083

SGS-THOMSON MICROELECTRONICS, INC.
1310 Electronics Drive
Carrollton, Texas 75006-5039
Phone (972) 466-6000
Fax (972) 466-7044

#8

Docket No.: **96-S-11**
Date: **March 3, 1998**

In re application of **Raul Z. Diaz et al.**
Application No.: **08/702,911**
Filed: **August 26, 1996**
For: **VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE**

ASSISTANT COMMISSIONER FOR PATENTS
2011 JEFFERSON DAVIS HIGHWAY
WASHINGTON DC 20231

RECEIVED
MAR 17 98
GROUP 2800

Sir:

Transmitted herewith is **an amendment** in the above-identified application.

[X] A Petition for an Extension of Time for three months is enclosed.
[X] No additional claim fee is required.
[] The fee has been calculated as shown.

	(Col. 1)		(Col. 2)	(Col. 3)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST PREV. PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
TOTAL	* 33	MINUS	** 49	0	x 11	$		x 22	$
INDEP.	* 3	MINUS	*** 5	0	x 41	$		x 82	$
[ ] FIRST PRESENTATION OF MULTIPLE CLAIMS					+ 135	$	OR	+ 270	$
EXTENSION OF TIME FEE						$			$ 950
TOTAL ADDITIONAL FEE						$	TOTAL		$ 950

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior amendment or the number of claims originally filed.

[] Please charge my Deposit Account No. 19-1090 in the amount of $_. A duplicate copy of this sheet is enclosed.
[X] A check in the amount of $ 950 is attached.
[X] The Assistant Commissioner is hereby authorized to charge payment of the following additional fees associated with this communication or credit any overpayment to Deposit Account No. 19-1090 . A duplicate copy of this sheet is enclosed.
[X] Any filing fees under 37 CFR 1.16 for the presentation of extra claims.
[X] Any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

SGS-Thomson Microelectronics, Inc.

E. Russell Tarleton

E. Russell Tarleton
Registration No. 31,800

users:\joanneb\ert98\0093

#8a
D. Sand
3/20/98

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Assistant Commissioner for Patents, 2011 Jefferson Davis Highway, Washington, DC 20231.

March 3, 1998 — Date

E. Russell Tarleton — E. Russell Tarleton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Raul Z. Diaz et al.
Application No.	:	08/702,911
Filed	:	August 26, 1996
For	:	VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE
Examiner	:	E. Ramirez
Art Unit	:	2414
Docket No.	:	96-S-11 (850063.517)
Date	:	March 3, 1998

Assistant Commissioner for Patents
2011 Jefferson Davis Highway
Washington, DC 20231

AMENDMENT

Sir:

In response to the Office Action dated September 3, 1997, please extend the period of time for response three months, to expire on March 3, 1998. Enclosed are a Petition for an Extension of Time and the requisite fee. Please amend the application as follows:

In the Specification:

On page 5, line 11, please replace "188" with -- 198 --.

On page 5, line 17, please replace "suggest" with -- suggests --.

On page 6, line 5, please replace "frame" with -- frames --.

On page 6, line 8, please replace "standards" with -- standard --.

On page 6, line 11, please delete the "," after "acceptable".

On page 12, line 21, please replace "12 circuit" with -- circuit 12 --.

On page 13, line 15, please replace "software. Presenting" with – software, presenting --.

On page 14, line 5, please replace "access" with -- accesses --.

On page 15, please delete the "," after "busses".

On page 15, line 23, please delete the "," after "memory".

On page 17, lines 18 and 19, please replace "standards. Possibly" with -- standards, possibly --.

On page 17, line 23, please replace "Meaning that compression" with -- This means that the compression --.

On page 17, line 26, please replace "complicated is it" with -- complicated, it is --.

On page 18, line 8, please delete "to be able".

On page 18, line 9, please replace "The encoding to comply" with -- Having the encoding comply --.

On page 18, line 10, please insert -- standards -- between "MPEG-2" and "balances".

On page 21, line 14, please replace "the are no a request" with -- there are no requests --.

On page 21, line 19, please replace "before of after" with -- before or after --.

On page 23, line 21, please replace "a image" with -- an image --.

In the Claims:

Please cancel claims 1-13, 42-43, and 49, and amend claims 14, 26, 28, 41, and 44 as follows:

---

14. (Amended) An electronic system coupled to a memory, comprising:

a first device that requires access to the memory;

a decoder that requires access to the memory sufficient to maintain real time operation;

[a fast bus coupled to the first device and the decoder;] and

a memory interface for coupling to the memory, and coupled to the first device[,] and to the decoder, the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory and a shared bus coupled to the memory, the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.

---

a2 13 ~~26~~. (Amended) The electronic system of claim 1 ~~14~~, wherein the [fast] bus has a bandwidth of [greater than a threshold] at least twice the bandwidth required for the decoder to operate in real time.

15 ~~28~~. (Amended) A computer comprising:

a3 processing means;

an input device connected to the processing means;

an output device connected to the processing means;

a memory connected to the processing means;

a first device that requires access to the memory;

a decoder that requires access to the memory sufficient to maintain real time operation; and

a memory interface coupled to the memory, to the first device, and to the decoder, the memory interface having a means for selectively providing access for the first device and the decoder to the memory and a shared bus coupled to the decoder, the first device, and the memory, the shared bus having a sufficient bandwidth to enable the decoder to operate in real time while sharing access to the bus.

a4 28 ~~41~~. (Amended) The computer of claim 15 ~~28~~, [further comprising a fast] wherein the shared bus [coupled to the memory, to the decoder to the first device] has at least twice the required bandwidth for the decoder to operate in real time.

a5 29 ~~44~~. (Amended) In an electronic system having a first device coupled to a memory interface and a memory coupled to the memory interface, the first device having a device priority and capable of generating a request to access the memory, a method for selectively providing access to the memory comprising the steps of:

providing a decoder coupled to the memory interface[,] through a bus having sufficient bandwidth to enable the decoder [capable of operating] to operate in real time while sharing access to the bus, having a decoder priority and capable of generating a request to access the memory;

providing an arbiter having an idle, a busy and a queue state;

generating a request by the decoder to access the memory;

determining the state of the arbiter;

36

providing the decoder access to the memory responsive to the arbiter being in the idle state for the decoder to operate in real time;

queuing the request responsive to the arbiter being in the busy state; and

queuing the request responsive to the arbiter being in the queue state in an order responsive to the priority of the decoder request and the priority of any other queued requests.

REMARKS

In the first Office Action, claims 1-49 were rejected under 35 U.S.C. § 102(b) in view of Lin et al., which is an article entitled "On the Bus Arbitration for MPEG II Video Decoder." Claims 1-49 were also rejected under 35 U.S.C. § 103(a) over Retter et al. (U.S. Patent No. 5,557,538) in view of Harney (U.S. Patent No. 5,522,080).

Applicants respectfully disagree with the bases for the rejections and request reconsideration and withdrawal of the rejections.

Some of the technical differences between the applied references and embodiments of the invention will now be discussed. Of course, these discussed differences regarding the embodiments, which are disclosed in detail in the patent specification, do not define the scope of interpretation of any of the claims; where presented below, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter. Embodiments of the present invention are directed to systems and method for coupling memory to a plurality of devices through a single shared bus that enables one of the devices, such as a decoder, to operate in real time. The shared bus has a bandwidth that is at least the required bandwidth for the decoder to operate in real time, and preferably at least twice the size of the required decoder bandwidth.

Lin et al. discusses a scheme for assigning duration rates to input/output tasks to ensure the decoding duration rate is greater than the display input requirements. Lin et al. does not suggest using a single shared bus having a bandwidth of sufficient size to permit real time decoding when sharing the bus with one or more other devices.

Retter et al., U.S. Patent No. 5,557,538, is directed to the management of internal bidirectional busses for data transfers with DRAM and other internal units. The arbitration scheme proposed by Retter et al. does not suggest or disclose a bus having a bandwidth sufficient to permit a decoder to operate in real time while sharing bus access with

one or more other devices, and Retter et al. does not disclose the claimed arbitration method for accomplishing real time operation of the decoder.

Harney, U.S. Patent No. 5,522,080, is not concerned with real time operation and does not teach or suggest a bandwidth of at least the required bandwidth for the decoder to operate in real time while simultaneously sharing bus access with one or more other devices. Rather, each of the devices in Harney has a local memory and interface.

Turning to the claims, independent claim 14, as amended, is directed to an electronic system coupled to a memory that comprises a "first device requiring access to the memory", a "decoder that requires access to the memory sufficient to maintain real time operation", and a "memory" interface for coupling to the memory, the memory interface being coupled to the first device and the decoder. Claim 14 further recites the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory through a shared bus, the "shared bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus"

Lin et al. does not teach or suggest such a system. More particularly, Lin et al. does not disclose a bus having a sufficient bandwidth to enable the decoder to operate and maintain real time operation when simultaneously accessing the shared bus with the first device. Rather, Lin et al. proposes a scheme for assigning duration rates for input/output tasks that ensures the decoding duration rate is greater than the display input requirements.

Retter et al. and/or Harney fail to make up for Lin et al.'s deficiencies. Retter et al. in combination with Harney fails to teach, disclose, or suggest to one of ordinary skill a shared bus having sufficient bandwidth to enable the decoder to operate in real time and maintain real time operation when simultaneously accessing the bus with the first device. While Retter et al. and Harney propose various methods for accomplishing their particular purposes, they do not suggest maintaining real time operation of a device through shared use of a bus interface to memory. Consequently, applicants respectfully submit that claim 14 is allowable over the references cited and applied by the Examiner.

Claim 15, which depends from claim 14, recites the first device and the decoder as being capable of having a variable bandwidth. Nowhere does Lin et al. or the combination of Retter et al. or Harney disclose or suggest to one of ordinary skill a decoder and first device having variable bandwidths in combination with a shared bus having sufficient bandwidth to enable the decoder to operate in real time when simultaneously

accessing the bus with the first device. Claim 26, which depends from claim 14, recites the bus as having a bandwidth at least twice the bandwidth required for the decoder to operate in real time. Lin et al., Harney, and Retter et al. are all silent with respect to providing a bus having at least twice the bandwidth required for a decoder to operate in real time. Applicants respectfully submit that claims 15-26 are allowable for these reasons as well as for the reasons why claim 14 is allowable.

The remaining claims recite limitations similar to those explained above. Claim 28 is directed to a computer comprising a processing means, an input and output device coupled to the processing means along with a memory, and a first device and decoder coupled to a memory interface through a shared bus that has a sufficient bandwidth to enable the decoder to operate in real time. Claim 29, which depends from claim 28, recites the first device and decoder as having a variable bandwidth. Claim 41, which depends from claim 28, recites the bus as having at least twice the required bandwidth for the decoder to operate in real time. Applicants respectfully submit that claims 28-41 are allowable for the reasons why claims 14-26 are allowable.

Claim 44 recites a method for selectively providing access to the memory of an electronic system having a first device coupled thereto, the method comprising the steps of providing a decoder coupled to the memory interface for operating in real time and having a decoder priority and request generation capability, providing an arbiter having an ideal, busy, and queue state, generating a request by the decoder to access memory, determining the state of the arbiter, and providing the decoder access to the memory for the decoder to operate in real time. As discussed above, neither Lin et al. nor the combination of Harney with Retter et al. teach or suggest to one of ordinary skill a method for providing decoder access to a memory through a shared bus that utilizes a bus of "sufficient bandwidth to enable the decoder to operate in real time while sharing access to the bus". In the prior devices described in Lin et al., Retter et al., and Harney, bandwidth is not discussed in the context of providing real time operation for a decoder and maintaining real time operation while sharing access to the bus. None of the applied references taken individually or in any motivated combination thereof teaches the combination of claimed steps in the recited method. Consequently, applicants respectfully submit that claim 44 and dependent claims 45-48 are allowable over the references cited and applied by the Examiner.

Overall, none of the applied references, taken alone or in any combination thereof apparently teach or suggest the claimed features recited in independent claims 14, 28,

and 44, and thus such claims are allowable. Since these independent claims are allowable based on the above reasons, the claims which depend from them are likewise allowable. If the undersigned attorney has overlooked a relevant teaching in any of the references, the Examiner is requested to point out specifically where such teaching may be found.

In light of the foregoing remarks, the Applicant respectfully submits that all pending claims are allowable. The Applicant, therefore, respectfully requests the Examiner to reconsider this application and timely allows all pending claims. Examiner Ramirez is encouraged to contact Mr. Tarleton by telephone to discuss the above and other distinctions between the claims and the applied reference, if desired. If the Examiner notes any informalities in the claims, the Examiner is encouraged to contact Mr. Tarleton to expediently correct any such informalities by telephone.

In view of the forgoing, applicants respectfully submit that all of the claims remaining in this application are now clearly in condition for allowance. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

Respectfully submitted,

Raul Z. Diaz et al.

SEED and BERRY LLP

E. Russell Tarleton

E. Russell Tarleton
Registration No. 31,800

ERT:alb/jp
Enclosures:
Postcard
Check
Form PTO-1083 (+ copy)
Petition for an Extension of Time (+ 2 copies)
General Authorization

6300 Columbia Center
701 Fifth Avenue
Seattle, Washington 98104-7092
(206) 622-4900
Fax: (206) 682-6031

WPN/850063/517-AM/V4

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/702,911	08/26/96	DIAZ	R 96-S-11

LM21/0330

LISA K JORGENSON
SGS THOMSON MICROELECTRONICS INC
1310 ELECTRONICS DRIVE
CARROLLTON TX 75006

EXAMINER	
RAMIREZ, E	
ART UNIT	PAPER NUMBER
2756	9

DATE MAILED: 03/30/98

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to Papers filed on 3/9/98.

☒ The allowed claim(s) is/are 14-41, and 45-48.

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☒ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☐ Examiner's Statement of Reasons for Allowance

ELLIS B. RAMIREZ
PRIMARY EXAMINER

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

LM21/0330

LISA K JORGENSON
SGS THOMSON MICROELECTRONICS INC
1310 ELECTRONICS DRIVE
CARROLLTON TX 75006

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/702,911	08/26/96	032	RAMIREZ, E 2756	03/30/98

First Named Applicant: DIAZ, RAUL Z.

TITLE OF INVENTION: VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 96-8-11	395-200.770	C25	UTILITY	NO	$1320.00	06/30/98

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 06/30/99. (0651-0033)

*U.S. GPO: 1998-437-639/80023

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

LM21/0410

LISA K JORGENSON
SGS THOMSON MICROELECTRONICS INC
1310 ELECTRONICS DRIVE
CARROLLTON TX 75006

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/702,911	08/26/96	033	RAMIREZ, E 2756	09/30/98
First Named Applicant	DIAZ, RAUL Z.			

TITLE OF INVENTION: VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 96-S-11	395-200.770	C25	UTILITY	NO	$1320.00	06/30/98

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 06/30/99. (0651-0033)

*U.S. GPO: 1998-437-639/80023

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/702,911	08/26/96	DIAZ	R 96-S-11

EXAMINER

LM21/0410

LISA K JORGENSON
SGS THOMSON MICROELECTRONICS INC
1310 ELECTRONICS DRIVE
CARROLLTON TX 75006

RAMIREZ,E

ART UNIT	PAPER NUMBER
2756	10

DATE MAILED: 04/10/98

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

Supplemental. NOTICE OF ALLOWABILITY (NOA)

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to Supplemental NOA.

☒ The allowed claim(s) is/are 14-41, and 44-48. (renumbered 1-33)

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☐ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☐ Examiner's Statement of Reasons for Allowance

ELLIS B. RAMIREZ
PRIMARY EXAMINER

PTOL-37 (Rev. 10/95)

*U.S. GPO: 1997-417-381/62714

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Applicant	: Raul Z. Diaz, et al	Docket No	: 96-S-011
Serial No	: 08/702,911	Group	: 2756
Filed	: August 26, 1996	Examiner	: E. Ramirez
For	: Video and/or Audio Decompression and/or Compression Device That Shares a Memory Interface	Batch No.	: C25

TRANSMITTAL OF FORMAL DRAWINGS

OFFICIAL DRAFTSMAN
Hon. Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the "Notice of Allowability" (POL 37) mailed March 30, 1998, in the above-referenced patent application, please find enclosed for filing five (5) sheet(s) of formal drawings.

I hereby authorize the Commissioner to charge any fees which may be required to Deposit Account No. 19-1353. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Lisa K. Jorgenson

Lisa K. Jorgenson
Reg. No. 34,845
Attorney for Applicant

SGS-Thomson Microelectronics, Inc.
1310 Electronics Drive/MS 2346
Carrollton, TX 75006
972-466-7414

CERTIFICATE OF MAILING
37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Official Draftsman, Assistant Commissioner for Patents, Washington, D.C. 20231 on the date below:

June 24, 1998
Date

Angie Rodriguez
Signature

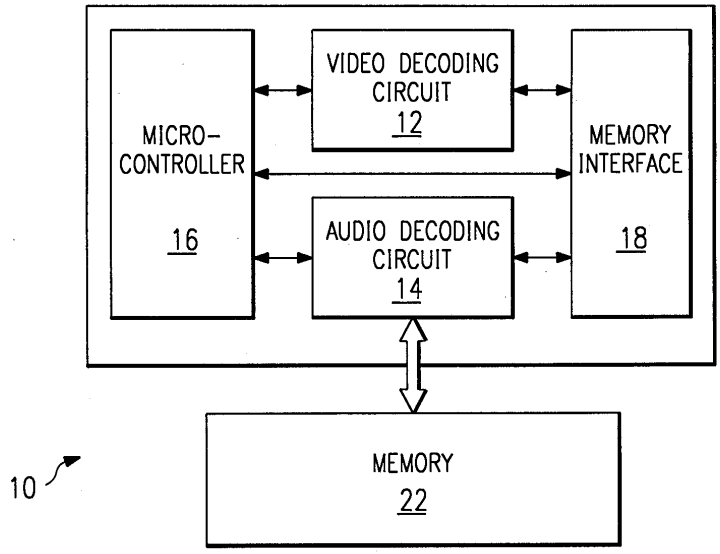


FIG. 1a
(PRIOR ART)

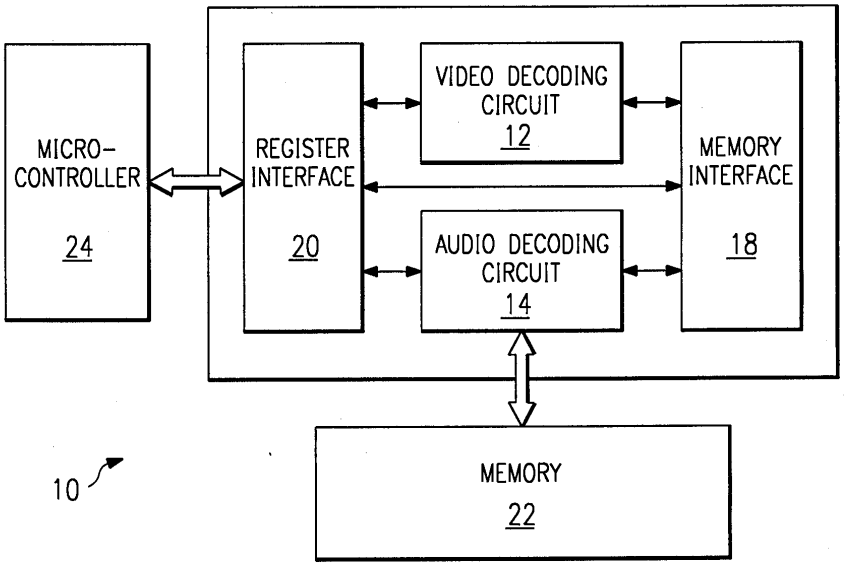


FIG. 1b
(PRIOR ART)

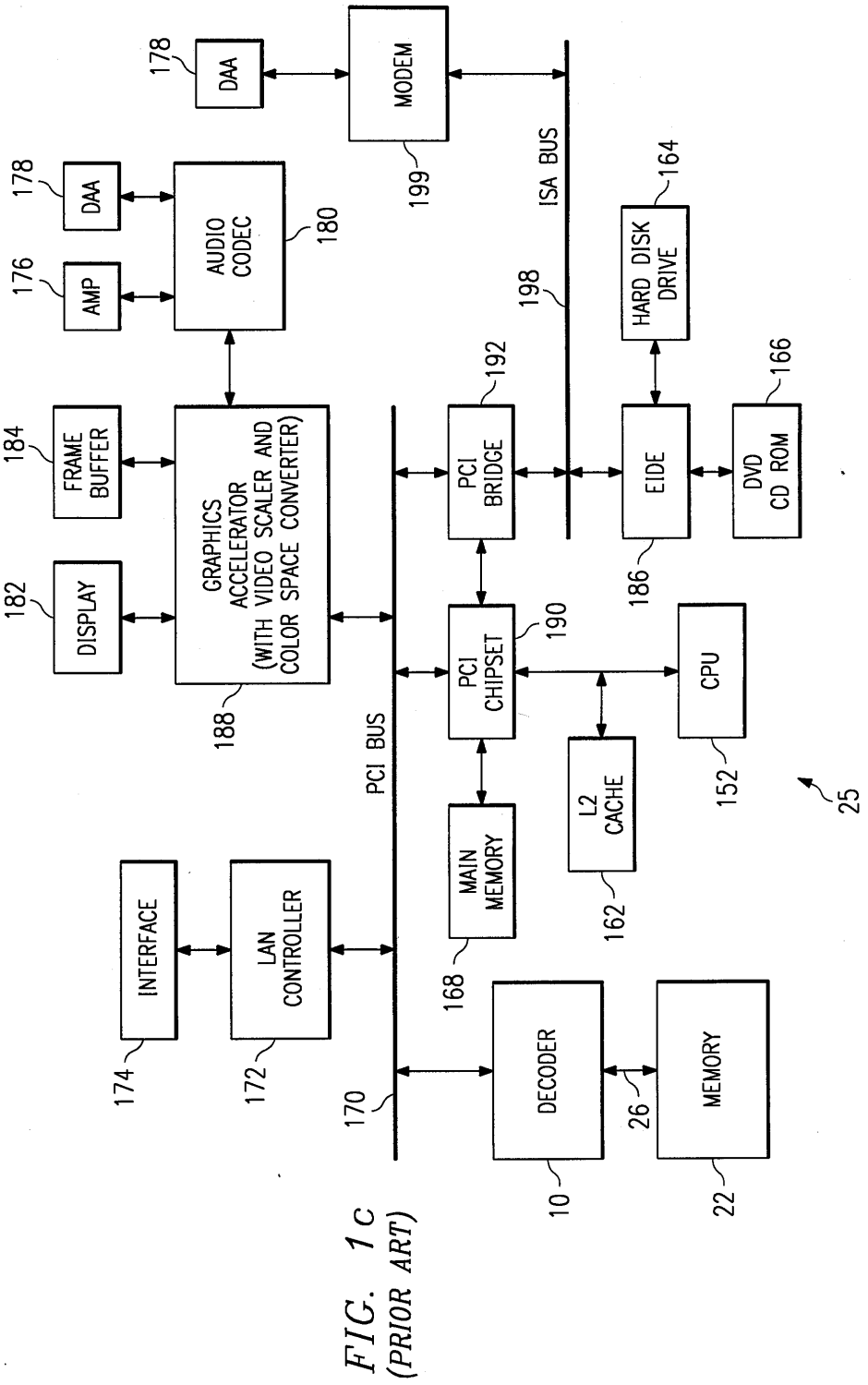


FIG. 1c
(PRIOR ART)

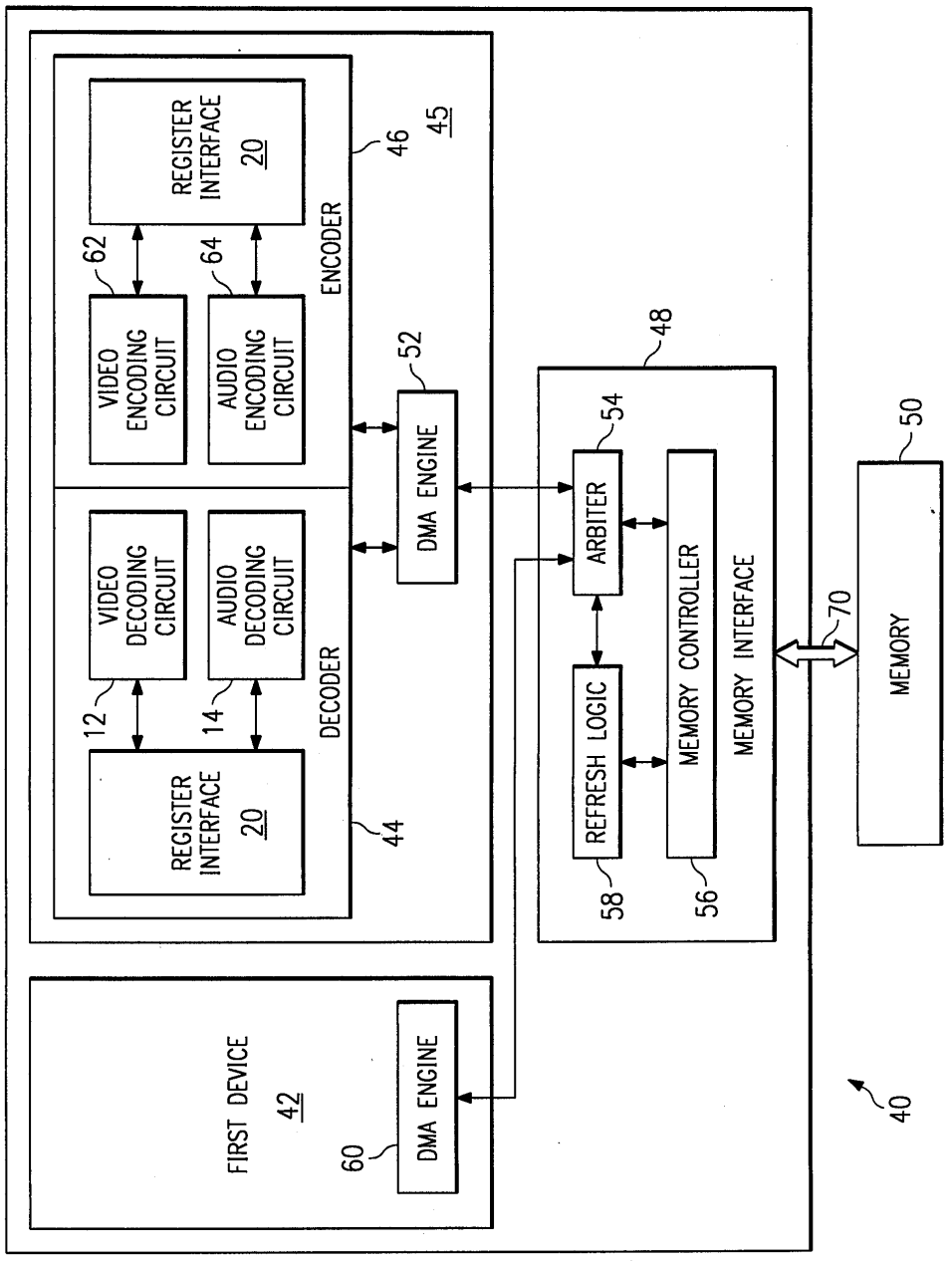


FIG. 2

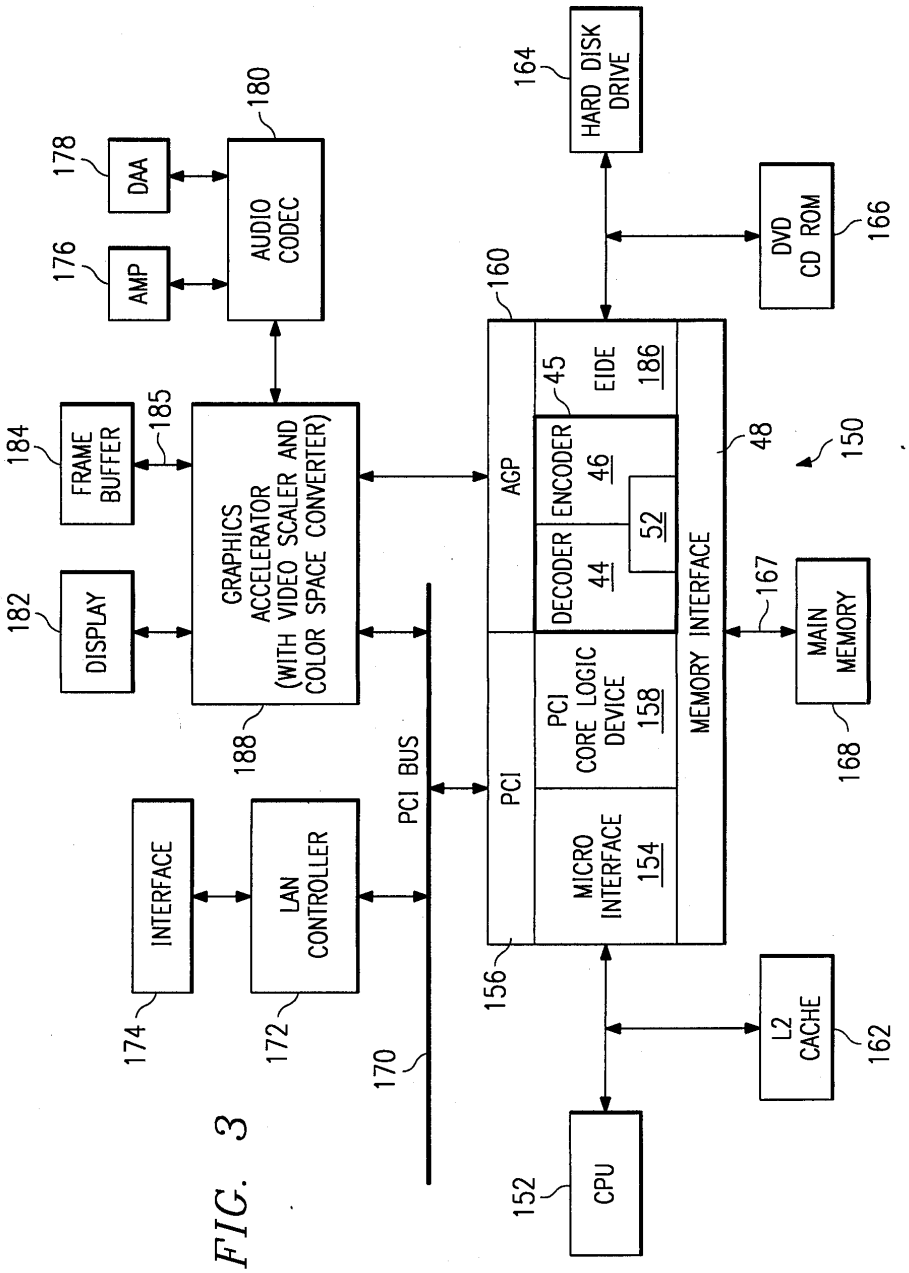


FIG. 3

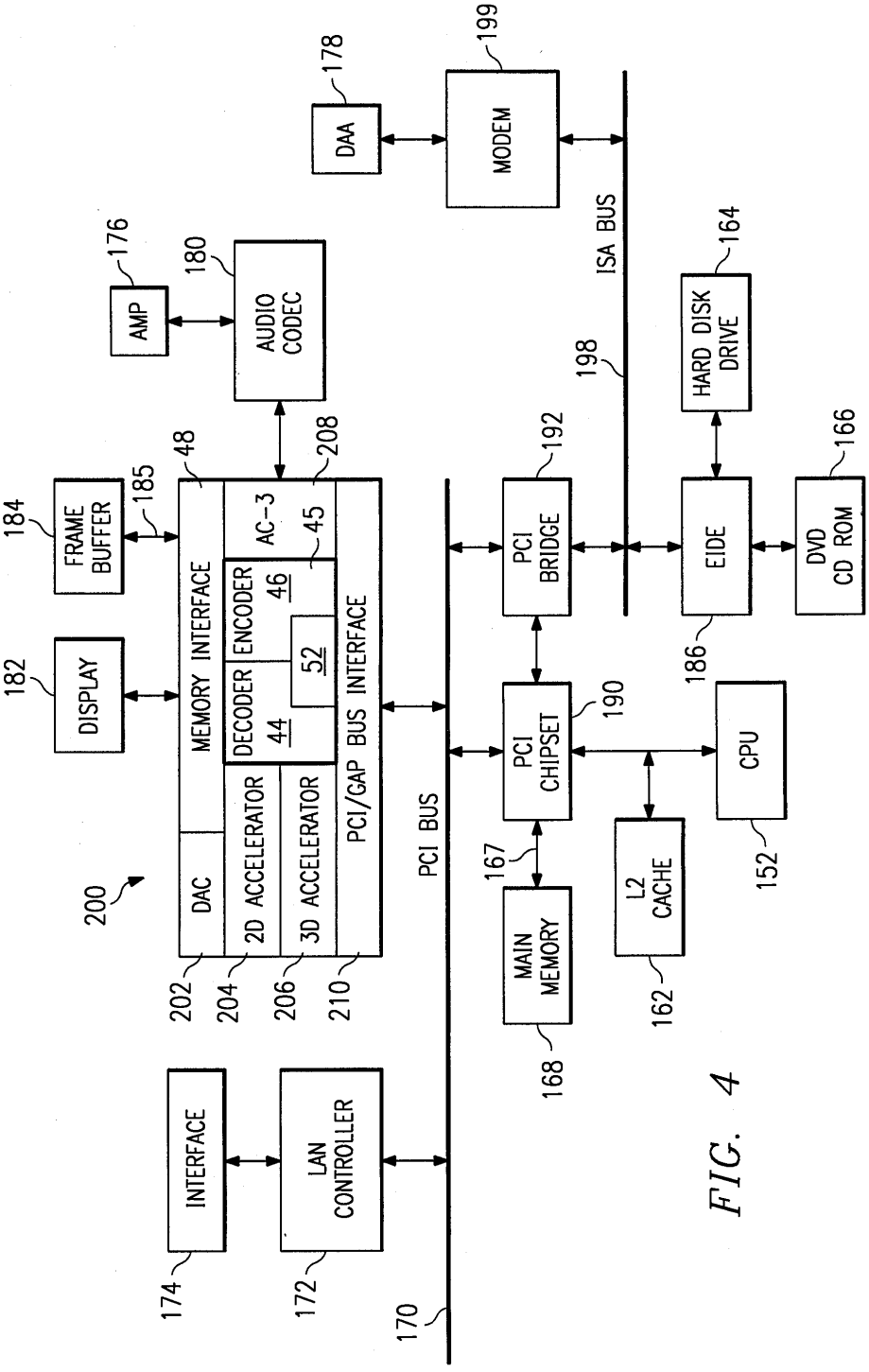
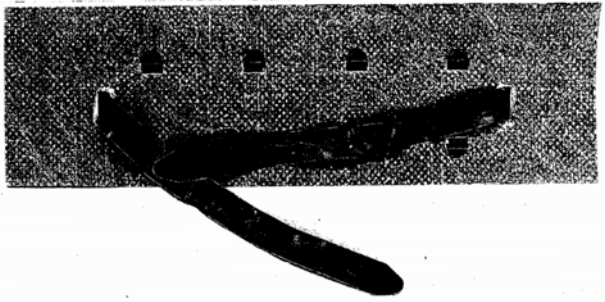


FIG. 4



PTO UTILITY GRANT
Paper Number 12

The Commissioner of Patents and Trademarks

Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America for the term set forth below, subject to the payment of maintenance fees as provided by law.

If this application was filed prior to June 8, 1995, the term of this patent is the longer of seventeen years from the date of grant of this patent or twenty years from the earliest effective U.S. filing date of the application, subject to any statutory extension.

If this application was filed on or after June 8, 1995, the term of this patent is twenty years from the U.S. filing date, subject to an statutory extension. If the application contains a specific reference to an earlier filed application or applications under 35 U.S.C. 120, 121 or 365(c), the term of the patent is twenty years from the date on which the earliest application was filed, subject to any statutory extension.

The United States of America

PATENT AND TRADEMARK OFFICE
UNITED STATES OF AMERICA

Bruce Lehman
Commissioner of Patents and Trademarks

Attest Mary L. Lee

Form PTO-1584 (Rev. 2/97)

FPI-LOM

(RIGHT INSIDE)

#13

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Applicant	: Raul Z. Diaz, et al	Docket No	: 96-S-011
Serial No	: 08/702,911	Group	: 2756
Filed	: August 26, 1996	Examiner	: E. Ramirez
For	: Video and/or Audio Decompression and/or Compression Device That Shares a Memory Interface	Batch No.	: C25

TRANSMITTAL LETTER

Hon. Assistant Commissioner for Patents
Washington, D.C.

Dear Sir:

Enclosed herewith is a Supplemental Declaration for filing in the above-identified application.

Please charge any fees necessary to deposit account No. 19-1353. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Lisa K. Jorgenson

Lisa K. Jorgenson
Reg. No. 34,845
Attorney for Applicant

SGS-Thomson Microelectronics, Inc.
1310 Electronics Drive/MS 2346
Carrollton, TX 75006
972-466-7414

CERTIFICATE OF MAILING
37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on the date below:

June 24, 1998
Date

Angie Rodriguez
Signature

094 4/10 7.7.98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

395/200.770 5/11/98 (13)

In re the application of:

Applicant	: Raul Z. Diaz, et al	Docket No	: 96-S-011
Serial No	: 08/702,911	Group	: 2756
Filed	: August 26, 1996	Examiner	: E. Ramirez
For	: Video and/or Audio Decompression and/or Compression Device That Shares a Memory Interface	Batch No.	: C25

SUPPLEMENTAL DECLARATION

Hon. Assistant Commissioner for Patents
Washington, D.C.

Dear Sir:

I, Raul Z. Diaz, and Jefferson E. Owen, as below-named inventors in the application for letters patent for an improvement in Video and/or Audio Decompression and/or Compression Device That Shares a Memory Interface, Serial No. 08/702,911, filed in the United States Patent and Trademark Office on or about the 26th day of August, 1996, declare that my residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought;

I hereby state that I have reviewed and understand the contents of the above-identified patent application, including the claims;

that said subject matter, including the claims as amended, was part of my invention before the filing of the original application, above identified, for such invention; and that I acknowledge my duty to disclose information of which I am aware which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

PAT No. 5812789
Issue: 9/22/98

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor's Signature: _____
Full Name of First Joint Inventor: Raul Z. Diaz
Date of Signature: June 10, 1998
Residence and Post Office Address:
750 Montrose Ave.
Palo Alto, CA 94303

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Second Joint Inventor: Jefferson E. Owen
Date of Signature: 6/19/98
Residence and Post Office Address:
44177 Bowers Court
Fremont, CA 94539

Citizenship: United States of America

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Applicant	: Raul Z. Diaz, et al	Docket No	: 96-S-011
Serial No	: 08/702,911	Group	: 2756
Filed	: August 26, 1996	Examiner	: E. Ramirez
For	: Video and/or Audio Decompression and/or Compression Device That Shares a Memory Interface	Batch No.	: C25

TRANSMITTAL LETTER

BOX: ISSUE FEE
Hon. Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed:
(1) Issue Fee Transmittal PTOL-85B with Certificate of Mailing:
(2) Check in the amount of $1,350.00 for payment of Issue Fee and advanced order of ten (10) copies;
(3) Our return postcard.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-1353. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Lisa K. Jorgenson

Lisa K. Jorgenson
Reg. No. 34,845
Attorney for Applicant

SGS-Thomson Microelectronics, Inc.
1310 Electronics Drive/MS 2346
Carrollton, TX 75006
972-466-7414

CERTIFICATE OF MAILING
37 CFR 1.8(a)
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Box Issue Fee, Assistant Commissioner for Patents, Washington, D.C. 20231 on the date below:

June 24, 1998
Date

Angie Rodriguez
Signature

PART B—ISSUE FEE TRANSMITTAL

142-1320.00
501-30.00
8.

Complete and mail this form, together with 4160 **cable fees, to:** **Box ISSUE FEE**
Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

LM21/0410

LISA K JORGENSON
SGS THOMSON MICROELECTRONICS INC
1310 ELECTRONICS DRIVE
CARROLLTON TX 75006

RECEIVED
JUL 02 1998
Group 2100

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

Angie Rodriguez (Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
08/702,911	08/26/96	033	RAMIREZ, E	2756	03/30/98

First Named Applicant: DIAZ, RAUL Z.

TITLE OF INVENTION: VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 96-S-11	395-200.770	C25	UTILITY	NO	$1320.00	06/30/98

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 David V. Carlson
2 Theodore E. Galanthay
3 Lisa K. Jorgenson

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropiate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a subsititue for filing an assignment.

(A) NAME OF ASSIGNEE STMicroelectronics, Inc.

(B) RESIDENCE: (CITY & STATE OR COUNTRY)
Carrollton, Texas

Please check the appropriate assignee category indicated below (will not be printed on the patent)
☐ Individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):
☑ Issue Fee
☒ Advance Order - # of Copies 10

4b. The following fees or deficiency in these fees should be charged to:
DEPOSIT ACCOUNT NUMBER 19-1353
(ENCLOSE AN EXTRA COPY OF THIS FORM)
☐ Issue Fee
☐ Advance Order - # of Copies

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) Lisa K. Jorgenson (Date) 6/9/98

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1995

Application or Docket Number

CLAIMS AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE				375.00	OR		750.00
TOTAL CLAIMS	49 minus 20 =	* 29	x$11=		OR	x$22=	638
INDEPENDENT CLAIMS	5 minus 3 =	* 2	x39=		OR	x78=	156
MULTIPLE DEPENDENT CLAIM PRESENT			+125=		OR	+250=	
			TOTAL		OR	TOTAL	1544

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total	* 33	Minus	** 49	= —	x$11=		OR	x$22=	
Independent	* 3	Minus	*** 5	= —	x39=		OR	x78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+125=		OR	+250=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total	*	Minus	**	=	x$11=		OR	x$22=	
Independent	*	Minus	***	=	x39=		OR	x78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+125=		OR	+250=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total	*	Minus	**	=	x$11=		OR	x$22=	
Independent	*	Minus	***	=	x39=		OR	x78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+125=		OR	+250=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875
(Rev. 10/95)

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Form PTO 1130 (REV 2/94)

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

PACE DATA ENTRY CODING SHEET

1ST EXAMINER	230	DATE	10-15
2ND EXAMINER		DATE	

APPLICATION NUMBER	TYPE APPL	FILING DATE MONTH	DAY	YEAR	SPECIAL HANDLING	GROUP ART UNIT	CLASS	SHEETS OF DRAWING
m/702911	1	08	26	96	0	2612	358	5

TOTAL CLAIMS	INDEPENDENT CLAIMS	SMALL ENTITY?	FILING FEE	FOREIGN LICENSE	ATTORNEY DOCKET NUMBER
49	5	0	1356	Y	96-8-11

CONTINUITY DATA

CONT CODE	STATUS CODE	PARENT APPLICATION SERIAL NUMBER	PCT APPLICATION SERIAL NUMBER	PARENT PATENT NUMBER	PARENT FILING DATE MONTH	DAY	YEAR
			PCT/				
			PCT/				
			PCT/				
			PCT/				
			PCT/				

PCT/FOREIGN APPLICATION DATA

FOREIGN PRIORITY CLAIMED	COUNTRY CODE	PCT/FOREIGN APPLICATION SERIAL NUMBER	FOREIGN FILING DATE MONTH	DAY	YEAR
N					

☆ U.S. GPO: 1995–401-429

```
=> d his

     (FILE 'USPAT' ENTERED AT 13:35:42 ON 22 SEP 1999)
L1          1120 S MULTIPROCESSOR#/TI,AB
L2          1660 S (MAIN MEMORY)/TI,AB
L3           107 S L1 AND L2
L4         12245 S FIFO
L5          5881 S MEMORY(5A)MANAGEMENT
L6          1048 S L5 AND L4
L7             9 S L6 AND L3
L8            30 S L3 AND L4
L9          5786 S MEMORY CONTROLLER
L10           12 S L9 AND L8
L11            3 S L10 AND L5
```

```
=> d his

     (FILE 'USPAT' ENTERED AT 11:38:46 ON 28 SEP 1999)
L1           51 S (FIFO OR QUEUE)(3A)BYPASSING
L2       141355 S PROCESSOR#
L3        13932 S MAIN MEMORY
L4         5827 S MEMORY CONTROLLER
L5         1670 S L4 AND L3 AND L2
L6            2 S L5 AND L1
L7          189 S (FIFO OR QUEUE OR BUFFER)(3A)BYPASSING
L8           19 S L7 AND L2 AND L3 AND L4
L9       104716 S DECOD####
L10          14 S L9 AND L8
L11          14 S L10 AND (IDENTIF? OR TAG#)
L12          12 S L11 AND EMPTY
L13          12 S L12 AND (FULL)
L14          11 S L11 AND ((BUFFER OR QUEUE OR FIFO)(P)(EMPTY))
L15          11 S L14 AND ((BUFFER OR QUEUE OR FIFO)(P)(FULL))
L16          41 S L2(P)L7
L17          14 S L16 AND L3 AND L4
L18        8334 S (BUFFER OR QUEUE OR FIFO)(P)EMPTY
L19       14117 S (BUFFER OR QUEUE OR FIFO)(P)FULL
L20          10 S L19 AND L18 AND L17
L21          10 S L20 AND L9
```

```
=> d his

     (FILE 'USPAT' ENTERED AT 11:38:46 ON 28 SEP 1999)
L1           51 S (FIFO OR QUEUE)(3A)BYPASSING
L2       141355 S PROCESSOR#
L3        13932 S MAIN MEMORY
L4         5827 S MEMORY CONTROLLER
L5         1670 S L4 AND L3 AND L2
L6            2 S L5 AND L1

=> d l6 1- ti,ccls


US PAT NO:     5,796,413 [IMAGE AVAILABLE]            L6: 1 of 2
TITLE:         Graphics controller utilizing video memory to provide
                 macro command capability and enhanced command buffering
US-CL-CURRENT: 345/522, 516, 521

US PAT NO:     5,530,933 [IMAGE AVAILABLE]            L6: 2 of 2
TITLE:         Multiprocessor system for maintaining cache coherency by
                 checking the coherency in the order of the transactions
                 being issued on the bus
US-CL-CURRENT: 711/141; 364/228.3, 229.2, 238.4, 240.1, 243.4, 243.44,
                 264, 264.4, 264.7, DIG.1; 711/3, 119, 121
```

PROCEEDINGS
SPIE—The International Society for Optical Engineering

Digital Video Compression on Personal Computers: Algorithms and Technologies

Arturo A. Rodriguez
Chair/Editor

7–8 February 1994
San Jose, California

Sponsored by

IS&T—The Society for Imaging Science and Technology

SPIE—The International Society for Optical Engineering

In cooperation with

IEEE Computer Society

Published by
SPIE—The International Society for Optical Engineering

SPIE PROCEEDINGS SERIES

Volume 2187

A high-performance cross-platform MPEG decoder

Hemant Bheda and Partha Srinivasan

Mediamatics Inc.
Santa Clara, CA 95054

pp. 241-8=8
PD = 194

ABSTRACT

We present a high performance implementation of a MPEG decoder, written entirely in a high level language. The decoder implementation fully complies with the MPEG-I standard and decodes all (I, P, B) frame types in MPEG video bitsteams and is portable.

Versions of this decoder are implemented on Windows 3.1, and on Windows NT (X86, MIPS, ALPHA). A comparison of the performance of the decoder between the various platforms is made. We also present a high quality, fast dithering and interpolation algorithm used to convert YCbCr directly into 8 bit palletized images.

We propose a new method called Collaborative Compression, of dealing with compression and decompression tasks at a very low cost to achieve 30 fps SIF performance for desktop applications. Collaborative Compression is a systems approach to partitioning the functionality between CPU-centric (i.e. software) and hardware-assist (VLSI) in order to achieve the optimal cost solution. The CPU provides glue programmability to tie the accelerated and non-accelerated parts of the algorithm together. The advent of high bandwidth, low latency busses (VL Bus and PCI) enable a high speed data pathway between the distributed computational elements.

1. INTRODUCTION

The Motion Picture Experts Group (MPEG) video coding algorithm is a standard for the storage of video and audio data in a compressed digital form. It was defined by the CCITT MPEG group formed with a goal of defining a standard that could compress video and audio to a bandwidth of 1.5Mbit/sec or less. The committee draft dated December 1991[3] has formed the basis for the implementation described in this paper.

The MPEG Decoder we have implemented decodes only the video bitstream. Its primary goal was to explore the possibility of decoding MPEG bitstreams on Personal Computer class platforms. Patel et. al[1] have already presented a software decoder designed primarily for portability across Unix platforms with X Windows. Our software player was designed for portability across PC platforms, with RISC or CISC CPUs and running 16bit or 32bit operating systems, while delivering the highest performance and be fully compliant with the ISO standard. The GUI for the decoder uses the Windows 3.1 API, which makes it work with OS2, Windows NT and Windows 3.1. We have documented the performance of this decoder on Windows 3.1, Windows NT running on X86, MIPS and ALPHA platforms.

Even though the MPEG standard defines one resolution - SIF at 320x240, for the PC environment a defacto standard commonly called QSIF has emerge - at 160x120. Typical PCs do not have enough CPU power to do 30 (or even 15) Frames Per Second (Fps) SIF resolution. So a common practice is to encode a 160x120 (QSIF) resolution image, and then after decoding, to interpolate the output image by a factor of 2 to obtain a 320x240 SIF resolution image. We have also developed a non-real-time MPEG encoder, which is capable of producing bitstreams containing I, P and B frames, with arbitrary M and N parameters. This encoder can also produce video bitstreams with any resolution. Our decoder can also decode any resolution image, and has a user selectable output interpolation factor (1x or 2x).

We have developed a novel method of doing the Color Space Conversion that is especially suited to PC systems using the Windows OS. We present the computational loads presented by the different phases of the MPEG decoding algorithm. Section 3.1 deals with the architecture of the software decoder that allows the core decoder to be ported to any platform that has a 32 bit ANSI-C compiler, and the GUI to be ported to any platform supporting the Windows 3.X API.

0-8194-1482-4/94/$6.00

Section 3.1 presents the dithering and Color Space Conversion algorithms used in this decoder. Section 4.0 presents the performance results obtained on the various platforms.

2. THE MPEG-1 VIDEO CODING STANDARD

In this paper we refer only to the video bitstream when referring to MPEG-I. The MPEG video coding standard specifies the format of the video bitstream. The standard also specifies the decoding process to be used and the errors tolerable in the process. The process of encoding the bitstream is not specified and is left as an area of differentiation for implementers. We shall attempt to present the MPEG-I standard more from a decoding computational load point of view. Details of the actual standard can be found in the standards document[3].

MPEG uses transform coding in conjunction with motion compensation to achieve its compression goals. It performs spatial compression using transforms (specifically the Discrete Cosine Transform, DCT) and temporal compression using motion compensation. MPEG encoded video frames are basically of three types: (i) Intra Frames (I), (ii) Predictive Frames (P) and (iii) Bi-Directional Frames (B). Each frame type is encoded in a different manner. Each frame is first subdivided in square blocks of 16x16 pixels called macroblocks. Each macroblock of RGB pixels is converted to a 16x16 *Y* block and a 8x8 *Cb* block and an 8x8 *Cr* block representing the Luminance (Y) and Chrominance (Cb, Cr) information respectively.

Intra Frames are also called key Frames. They are coded only spatially and decoding them does not require data from any other frame, past or present. P Frames are coded temporally and spatially. Thus they depend on data from the previous I|P frame in the past. B Frames are dependent on the nearest I|P Frames in the past and the future. Each frame type represents a different type of computational load to a typical PC class machine.

The input video data can be assumed as being represented as a two dimensional array of triplets (each triplet is one pixel with the Red, Green and Blue values). It is also possible to have input data in the form of Luminance and Chrominance arrays. Figure. 1. shows the different stages of the video encoding process for Intra Frames. Each macroblock is transform coded using DCT. The coefficient terms are then quantized and run-length coded. The resulting bitstream is then entropy coded using Huffman codes. This is repeated for every block in the image.

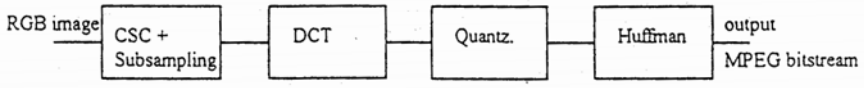


Figure 1.0 Encoding process for Intra Frames

For P and B frames, any macroblock that can be represented from its reference key frame is represented as a motion vector - a tuple representing the relative displacement from its position in the reference frame. In the case of P frames, there is only one reference frame - the nearest I|P frame in the past. For B frames there are two reference frames - the nearest past and future I|P frames. For B frames the current macroblock can be a simple linear function of macroblock from both reference frames. Any block that cannot be so represented is called an Error term, and is coded like a macroblock from an I frame.

2.1 Computational Loads in MPEG

From a computational point of view, each type of frame differs in it computational load. We shall differentiate computational loads as:
(i) arithmetic operations: Those that are predominantly comprised of arithmetic operations (+, -, *) and whose memory access pattern fits in a relatively small cache.
(ii) memory operations: Those whose memory bandwidth utilization is heavy in relation to their arithmetic operation count.

(iii) Bit manipulations: Comprised of manipulating bit fields, extracting, rotating, shifting and masking variable length bit fields. Some processors have special instructions for dealing with bit field operations. Others perform bit field operations by decomposing them into standard arithmetic and logical operations.

The major operations performed in Decoding are:

(1) Variable Length Decoding
(2) Inverse quantization and Zig-Zag scanning
(3) IDCT
(4) Motion Compensation (for P and B frames)
(5) Color Space Conversion (from YCbCr to RGB color space) OPTIONAL
(6) Dithering (reducing from 24 bit RGB color space to 8 bit color space). OPTIONAL

The kind of load presented by each major phase is dependent on the implementation. This in turn allows tradeoffs to be made in order to tune the decoder for different processor architectures.

2.2 Architectural features and their impact on MPEG decoding

As will be seen in the following sections, different architectural features impact the performance of a decoding algorithm implementation. We will attempt to catalog some of the performance axes that influence decoder performance. They are:

1) CPU performance
2) Cache and Memory subsystem performance
3) Bus performance
4) Display subsystem performance

CPU performance affects all compute bound operations such as IDCT, or bit field operations. However if the data required cannot be contained in registers - as is always the case, whether doing IDCT or any other operation, the cache subsystem performance becomes crucial. Operations such as VL decoding, Inverse quantization and IDCT may not fit in the first level cache of the CPU. Second level cache size and performance then become crucial. The motion compensation (frame reconstruction) part is extremely memory dependent. The CPU just constructs the output frame from two input frames, using mostly copying. Given the size of the frames, and the random nature in which the blocks can move, large second level caches are necessary to contain the input and output frames. Once the output frames is ready, it has to be transferred to the display frame buffer. This operation is dependent on the available bandwidth on the bus connecting the display adapter to the CPU. Sometimes, even when adequate bus bandwidth is available, the display adapter itself may not allow efficient access to the display memory from the host bus (e.g. the display memory may be organized to provide higher priority to the graphics accelerator rather than the host CPU bus). We will discuss in Section 3.0, how these architectural features affect our decoder, and what features are best suited to software MPEG decoders.

2.3 Other Software MPEG Decoders

There are a few other software only MPEG compliant video decoders, both commercial and shareware/freeware. Ketan Patel et. al at UC Berkeley have released an excellent portable implementation for Unix platforms into the public domain. There is also a shareware Windows NT based MPEG decoder, which can decode video bitstreams. This is slower than our implementation and also has poor video quality.

Our implementation can decode bitstreams containing any frame type and has been tested with several bitstreams, both from the Internet and from those provided by other collaborators. We also produced bitstreams using our own non-real-time software encoder. This encoder allowed us to play with performance sensitivity to quantization levels, frame type sequencing and so forth.

3. THE SOFTWARE MPEG-I VIDEO DECODER

The primary goal of the decoder was to determine if a full implementation of the decoder would achieve reasonable performance (as measured by frame rate) on a PC class machine. We define this to be a 486Dx2-66 PC, with a 256Kbyte second level cache, 8 or 16 Mbytes of main memory - 70 nS. We also wanted a decoder written in a high level language, for ease of maintenance and portability.

The decoder is partitioned into 2 distinct parts. A GUI based front end, that provides a user friendly player, allowing play, stop, rewind and variable speed fast play functionality in both forward and reverse directions and handles all the display rendering. This GUI front end uses the Windows 3.X API and is portable across all operating systems that provide Windows API servers (such as WABI, OS2, Windows NT). The second part (backend) of the decoder is implemented as a Dynamic Linked Library (DLL).

Windows provides a format called the Device Independent Bitmap (DIB) for representing color bitmaps. It also provides API calls for drawing such DIBs. These routines first convert the DIB from the color system provided to the native color format (eg. 16 bit or 8 bit) and then renders the bitmap.

The percentage of total time spent in the major operations when decoding to a 1x interpolated 8 bit Device Dependent Bitmap (DDB) output format is given. The data was collected on a DEC Alpha system, DECpc AXP 150 running WinNT 3.1 - release build. The compiler used was the release SDK 3.1 compiler for the Alpha architecture.

Major Operation Type	8 bit dithered
VL Decoding	10.5 %
IDCT	16.5%
CSC + Dithering	26.5%
Frame Reconstruction	26.0%
Frame Display	13.5%
Misc.	7%

Table 1. Breakup of time spent in Decoding a video bitstream

The kinds of loads presented by our decoder implementation are as follows:

1) VL Decoding - bit manipulation:
Converted to logical operations, shifting, masking and rotating. This is CPU intensive and register intensive (given the 8 registers on the x86).

2) Inverse quantization and unzigzag:
This stage is performed using table lookups - and is there cache performance sensitive in our implementation.

3) IDCT:
We believe this is sensitive to register pressure in machines with few registers. On machines with hardware single cycle multipliers, this is CPU bound.

4) Color Space Conversion:
We implement this using table lookup - both in the true color (16 bit or 24 bit case) and in the 8 bit dithered output case. This phase is cache and memory latency sensitive. Even though the lookup tables may fit in the primary cache, the reading and writing of the image frame pollutes the cache. Primary write through caches without write buffers suffer in this regard when compared to write through with write buffers. Large primary caches such as those on the MIPS Magnum systems definitely help the performance.

On the whole, our implementation showed a large sensitivity to memory/cache subsystem performance, and to display subsystem speed. For our player the memory to screen bitblt speed is the primary governing factor in display subsystem performance. For this reason - a fast frame buffer access path is better than a very powerful graphics accelerator, coupled with slow host access speeds. This is demonstrated in Section 4.1.

3.1 Dithering

Dithering was a major area where there were large swings in performance depending on the dithering algorithm used. Typical algorithms used for dithering are error diffusion algorithms (Floyd-Steinberg) and ordered dither[2]. We have developed our own dithering algorithm that is similar to the one used by Patel et. al. Windows 3.X and WinNT workstations used for multimedia typically have a 256 color display accelerator card. Out of the 256 colors available, Windows 3.X[4] uses 20 color which occur at pre-defined indices in the color LUT. The first 10 and last 10 indices are used by Windows, ie. colors 0-9 and 246-255. In order to achieve the greatest performance under Windows, the displayed bitmap should used what is called an "Identity Palette". This palette has the 20 fixed Windows colors in their nominal positions i.e 0-9 and 246-255. Only 236 colors at indices 10-245 are available for an application to use.

Typically dithering converts 24 bit RGB images to 8 bit palletized images. In MPEG, the output of the decompression process typically results in a YCbCr image, which is then color converted into an RGB image. This RGB image is then displayed. If the display system cannot accept full color RGB images, the image is then dithered (color sub sampled) to allow for display at lower color resolutions.

Given the additional constraints imposed by Windows 3.X, we finally developed an algorithm that converts directly from YCbCr to a fixed palette with 228 entries in it. This has the advantage of avoiding the intermediate conversion from YCbCr to RGB. This is similar to the algorithm given by Patel, except that we use 228 colors instead of 128. We have also folded the 2X output interpolation into this stage, when we do the look up.

4. PERFORMANCE RESULTS

We present the performance of our decoder as measured in Frames Per second on the different platforms in Table 2. We did not have access to a Pentium based NT platform at the time this was written. The bitstream used had I, P and B frames and a resolution of 320x240 and an average bitrate of 1.0 MBits/sec at 30 frames per second. The output format was 1X interpolated 8 bit dithered output. We also give the performance on QSIF sequence - encoded at 160x120 resolution and displayed with 1X and 2X output interpolation,

CPU-Mhz,Primary Cache, Secondary	OS	320x240	160x120 / 2X	160x120 / 1X
486DX2-66, 8Kb, 256Kb	Win 3.1	5.0	14	26
486DX2-66, 8Kb, 256Kb	Win NT	4.8	13	24
Mips R4400-100, 32Kb, 512Kb	Win NT	10.3	26	42
Alpha AXP-150, 16Kb, 512Kb	Win NT	12.5	29	49

Table 2. Performance in Frames Per Second.

Note: The Mips machine had a direct linear frame buffer, providing the highest display subsystem performance of all the machines. The Intel machines had VESA local bus display adapters. The Alpha machine had an EISA bus based graphics adapter. The source code is the same for all the systems.

We find that none of the machines can do real-time decoding of a SIF frame. However by using bitstreams encoded at QSIF resolution and then by performing a 2X interpolation of the output image, we can perform 30 fps on the RISC platforms. We have not exhausted all the performance gains to be made by playing with aggressive compiler optimization switches. The code is written in 32 bit C and does not utilize the 64 bit data paths available on the MIPS and ALPHA platforms.

4.1 Performance Sensitivity to Memory and Display subsystems

We conducted a side by side performance test of two MIPS based NT machines with identical MIPS R4400 100 Mhz (50 Mhz bus) processors. Both machines had similar Primary caches (on board the R4400). Machine A had a slow 512kb secondary cache and a slow memory controller - identical to those used on 486 Dx2-66 based machines. Machine B had a fast secondary cache of 512Kb and a very fast memory controller. Machine A had an ISA bus based 8 bit graphics card and Machine B had a direct linear frame buffer which the host CPU could access at high speeds. For the same sequence, Machine A had a performance of 6.1 Fps and Machine B had a performance of 10.1 Fps. This was a combination of both the memory subsystem and the display subsystem effects. The gain (Machine B/ Machine A) was 1.65 for this case. We disabled the display of frames to find the effect of memory subsystem effects alone. The speed up dropped to 1.36, still a substantial difference considering the processors are identical and running identical code.

5.0 COLLABORATIVE COMPRESSION

We define collaborative compression to be the optimal balance of software decoding with hardware assist to enable real-time decompression at minimal cost. There are a number of hardware devices on the market that are designed to perform 30 frames per second SIF decoding, such as those from SGS Thompson, C-Cube, IIT etc.

Some of these devices are programmable (IIT) while others are hardwired. Even though these devices themselves are low cost (~ $30), the end cost of a system solution is much higher (~$150). This is due to the extra glue logic required to interface to a PC bus (VL, PCI or ISA), the external memory, DACs etc. On the other hand, we have presented a software only decoder whose performance clearly does not meet real-time requirements. However, it is possible to add a minimum amount of hardware, which when properly designed will together with the existing CPU and display subsystem, will enable real-time full SIF decoding.

5.1 Color Space Conversion and Stretching

The plethora of compression standards in the Windows arena (such as MS Video 1, Cinepak, Motion JPEG) has already led to the emergence of rudimentary forms of hardware assist such as Color Space Converters (CSC) and stretchers. Examples of such devices are made by Weitek (VideoPower) and Videologic, Tseng Labs. All these devices accelerate YCbCr -> RGB conversion, dithering and also stretching bitmaps from QSIF or SIF to full screen proportions. This is a logical first step, because most of the compression algorithms in vogue today can use these functionality.

5.2 IDCT and Huffman Decoding

The next step would be to accelerated compute intensive portions of the algorithm. The next largest gain will be made by performing the IDCT using hardware assist.

It is best to leave random control operations and other logic to the hands of software running on the host CPU. This enables rapid development of the decompressor, reduces time to market. Also, generic blocks such as IDCT, Huffman, can be re-used by other compression algorithms, by merely changing the glue software which ties the various hardware modules together. The requirement of any hardware module designed for collaborative compression are as follows:

(1) They support concurrency. The CPU must be free to perform other tasks after priming the hardware module. This allows us to pipeline the operations (in software).
(2) Data flow must be one-way. If there is too much data movement required of the CPU, for example to move from one module to the other - e.g. from IDCT to CSC, the speedup gained from the hardware module will be lost in the extra work done in shifting data around. The best model to view this is as several functional units - all sharing the same memory as shown in Figure 2.0 below.

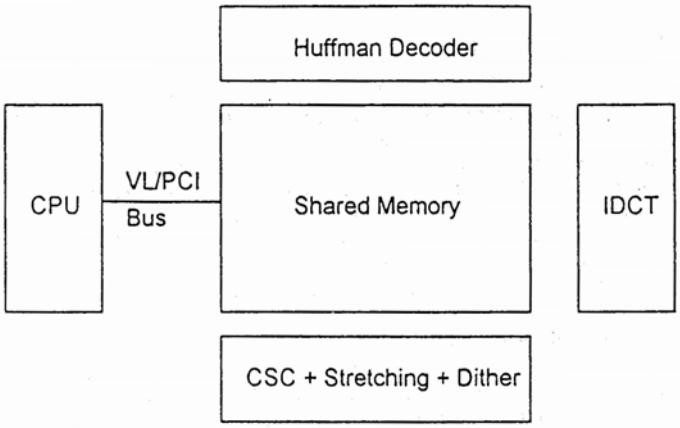


Fig. 2.0 Conceptual view of Collaborative Compression

The CPU performs the task of managing the different units, decoding headers, parsing the bitstream etc. In the initial stages, the data volume is low, and the data resides in CPU main memory anyway (deposited there by a peripheral). In the later stages, as data volume grows, the CPU acts as a re configurable pipeline manager and chains the other functional units using shared memory as the buffer between the units. This shared memory can be on a peripheral card connected to the CPU by a low latency, high bandwidth bus such as PCI.

6.0 CONCLUSION

We have presented the performance of a portable software MPEG player designed for PC platforms. The performance of the player is sensitive to memory/cache system performance and to display subsystem bandwidth. The performance of the software decoder approaches real-time for pseudo-SIF sequences (QSIF interpolated by 2X). IDCT occupies only a sixth of the time, much less than is conventionally expected. The highest performance workstations such as those base on the 300Mhz DEC Alpha should be able to perform real-time decoding of SIF streams. However for volume PC environments, collaborative compression offers the best means of achieving cost effect real-time MPEG video decoding.

7.0 APPENDIX

A. The Decoder Specification

The backend DLL contains all the functionality of the MPEG decoder. It is written entirely in 32bit ANSI-C. The output formats supported are (1) Windows 3.X Device Independent Bitmaps (DIB) which consists of a header and has the first pixel in the lower left corner of the image and (2) a simple array with pixel arranged in row major form, top left corner pixel leading (which we shall call DDB). For both these formats the following bit depths are supported:

(1) 8 bit dithered (DIB and DDB)
(2) 16 bit DIB (5,5,5) and DDB (5,5,5 ; 5,6,5; etc)
(3) 24 bit DIB and DDB
(4) 32 bit DIB and DDB

The following operations are also supported:

Play (I and P only, I, P and B)