UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

DSS TECHNOLOGY MANAGEMENT, INC.
Patent Owner

Case IPR. No. **Unassigned**
U.S. Patent No. 6,784,552
Title: STRUCTURE HAVING REDUCED LATERAL SPACEER EROSION

Declaration of Dr. Richard Fair in Support of
Petition For *Inter Partes* Review of U.S. Patent No. 6,784,552
Under 35 U.S.C. §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123

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I, Richard B. Fair, hereby declare as follows:

I. INTRODUCTION AND QUALIFICATIONS

1. My name is Richard B. Fair. My findings, as set forth herein, are based on my education and background in the fields discussed below.

2. I have been retained on behalf of Petitioner Samsung Electronics Co., Ltd. ("Samsung") to provide this Declaration concerning technical subject matter relevant to the *inter partes* review petition ("Petition") concerning U.S. Patent No. 6,784,552 (the "552 Patent," SAMSUNG-1001). I reserve the right to supplement this Declaration in response to additional evidence that may come to light.

3. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

4. My compensation is not based on the resolution of this matter. My findings are based on my education, experience, and background in the fields discussed below.

5. My background and experience is summarized in my curriculum vitae, a true and correct copy of which is submitted as Exhibit SAMSUNG-1004. Some of the relevant points are described below as well.

6. I received a B.S. in Electrical Engineering from Duke University in 1964, an M.S. in Electrical Engineering from Pennsylvania State University in 1966, and a Ph.D. in Electrical Engineering from Duke University in 1969. My

graduate research was on electron beam systems (scanning electron microscopy) and ion beam systems (ion beam deposition of thin metal films).

7. In 1969, I joined Bell Laboratories working on the fabrication, design, and testing of numerous semiconductor devices and integrated circuits, including metal-oxide-semiconductor (MOS) dynamic memory chips. During my time at Bell Laboratories, I worked on advanced silicon process development and started an effort on mixed signal CMOS integrated circuits. I was employed at Bell Laboratories until 1981, eventually rising to Supervisor.

8. I have been teaching in the Department of Electrical and Computer Engineering at Duke University since 1981. I have been a Professor from 1981 to the present. I am currently the Lord-Chandran Professor of Engineering in the Edmund T. Pratt, Jr. School of Engineering.

9. I also served as the vice president of design research and technology, director of microfabrication technology, executive director, and acting president of Microelectronics Center of North Carolina ("MCNC"), a technology non-profit that builds, owns, and operates a leading-edge broadband infrastructure for North Carolina's research, education, non-profit healthcare, and other community institutions, from 1981 to 1994.

10. While at MCNC I helped setup a state-of-the-art CMOS processing facility and directed research on semiconductor processing including

photolithography, wafer cleaning, annealing, ion implantation, plasma-enhanced CVD of thin films, metallization, and anisotropic etching processes. We conducted research on multi-level metal interconnects, barrier metallurgy, organic and inorganic inter-metal dielectrics, anti-reflective coatings, via and trench etching processes, and selective tungsten deposition for via filling. In 1987 we designed and built the world's first 1 million transistor chip, a parallel processor supercomputer. I also was responsible for the MCNC analytical lab, which included electron microscopy, atomic composition analysis, and sample preparation for reverse engineering studies. I have used such analytical tools to perform reverse engineering of semiconductor devices.

11. In 1994, I returned to Duke University full-time. Since then I have continued to teach courses on (1) the design and analysis of analog and digital integrated circuits, (2) semiconductor devices, (3) the chemistry and physics of transistor and integrated circuit fabrication, and (4) thin-film microfluidic devices, fluid dynamics, and applications. In addition, I have an active funded research program that involves undergraduate and graduate students.

12. I am a Life Fellow of the Institute of Electrical and Electronic Engineers ("IEEE"), a Fellow of the Electrochemical Society, past Editor-in-Chief of the Proceedings of the IEEE, and I have served as Associate Editor of the IEEE Transactions on Electron Devices. I am a recipient of the IEEE Third Millennium

Medal, and I was awarded the Solid State Science and Technology Medal of the Electrochemical Society in April 2003 (Gordon E. Moore Medal).

13. I have published over 170 papers in refereed and peer-reviewed journals and conference proceedings, contributed chapters to 12 books, edited nine books or conference proceedings, given over 130 invited talks in the field of electrical engineering, and I am a named inventor on 30 granted U.S. patents and 24 pending U.S. patent applications.

II. MATERIALS RELIED UPON IN FORMING MY OPINION

14. In addition to reviewing the 552 Patent, I also reviewed and considered the prosecution history of the 552 Patent (SAMSUNG-1002). I also reviewed and considered the prosecution history of U.S. Patent No. 6,066,555, the parent of the 552 Patent (SAMSUNG-1008). I have also reviewed the prior art Kuesters et al., "Self Aligned Bitline Contact For 4 Mbit dRAM," *Proceedings of the First International Symposium on Ultra Large Scale Integration Science and Technology*, 1987, pp. 640-649 ("Kuesters," SAMSUNG-1005), U.S. Patent No. 5,482,894 ("Havemann," SAMSUNG-1006), and U.S. Patent No. 4,686,000 ("Heath," SAMSUNG-1007). I also considered the background materials cited herein.

III. UNDERSTANDING OF THE GOVERNING LAW

15. I understand that a patent claim is invalid if it is anticipated or obvious in view of the prior art. I further understand that invalidity of a claim requires that the claim be anticipated or obvious from the perspective of a person of ordinary skill in the relevant art at the time the invention was made.

16. I have been informed that, in order to render a claimed apparatus obvious, the prior art must enable a person of ordinary skill in the art to make the apparatus. I have been further informed that a reference or combination is enabled if undue experimentation is not required to make the claimed apparatus.

17. I have been informed that it is the Patent Owner's burden to show that a reference or combination is not enabling. I reserve the right to amend or supplement this declaration if the Patent Owner introduces evidence that any references or combinations are not enabling.

18. I have been informed that a person of ordinary skill in the art has ordinary creativity, and is not an automaton.

A. Anticipation

19. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference.

20. I have been informed that a claim is invalid under 35 U.S.C. § 102(b) if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (critical date). I further have been informed that a claim is invalid under 35 U.S.C. § 102(e) if an invention described by that claim was disclosed in a U.S. patent granted on an application for a patent by another that was filed in the U.S. before the date of invention for such a claim.

B. Invalidity by Obviousness

21. I have been informed that a patent claim is invalid as "obvious" under 35 U.S.C. § 103 if it would have been obvious to one of ordinary skill in the art, taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called "secondary considerations" of non-obviousness if they are present. I reserve the right to amend or supplement this declaration if the Patent Owner introduces evidence of any secondary considerations of non-obviousness.

22. My analysis of the prior art is made as of the time the invention was made.

23. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. I further understand that exemplary rationales that may support a conclusion of obviousness include:

(A) Combining prior art elements according to known methods to yield predictable results;

(B) Simple substitution of one known element for another to obtain predictable results;

(C) Use of known technique(s) to improve similar devices (methods, or products) in the same way;

(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) “Obvious to try” – choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;

(F) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;

(G) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

24. I have been informed that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

IV. LEVEL OF ORDINARY SKILL IN THE ART

25. In my opinion, a person of ordinary skill in the art at the time of the claimed inventions would have had a bachelor's degree in electrical engineering, chemistry, materials science, or physics, or a closely related field, along with at least 2-3 years of experience in semiconductor fabrication. An individual with a master's degree in a relevant field, such as electrical engineering, chemistry, materials science, or physics, would require less experience in semiconductor fabrication.

26. I reserve the right to amend or supplement this declaration if the Board adopts a definition of a person of ordinary skill in the art other than that described above, which may change my conclusion or analysis. However, should the Board adopt a higher standard, it would not change my opinion that all of the claims of the 552 Patent ("claims at issue") are invalid.

27. My opinion below explains how a person of ordinary skill in the art would have understood the technology described in the references I have identified herein around the 1995 time period, which is the approximate date when the application to which the 552 Patent claims priority was filed. I was a person of at least ordinary skill in the art in 1995.

V. TECHNOLOGY OVERVIEW AND OVERVIEW OF THE 552 PATENT

28. The 552 Patent was filed on March 31, 2000. The 552 Patent is a division of U.S. Application No. 08/577,751, which was filed on December 22, 1995. Application No. 08/577,751 issued as U.S. Patent No. 6,066,555 ("555 Patent"). The 552 Patent issued on August 31, 2004.

29. The 552 Patent relates generally to a structure with minimal lateral spacer erosion, providing a contact opening with a small alignment tolerance relative to a gate electrode or other structure. SAMSUNG-1001, 552 Patent at Abstract. The claims at issue relate to a structure for a transistor with a self-aligned contact. *Id.*

30. Before discussing the details of the specification of the 552 Patent, I will provide a brief background on the technology of semiconductor fabrication. I will also provide a high-level overview of SEM imaging and the reading of SEM images.

A. Technology Background: Semiconductor Fabrication

31. The relevant aspects of the 552 Patent relate to semiconductor device processes, and more specifically to methods for etching contact openings through insulating layers and semiconductor devices with well-defined contact openings. Before discussing the specifics of the 552 Patent specification, I will discuss the manufacture and etching of semiconductor devices at a high level.

32. Manufacturing very large-scale integrated circuit devices involves the process of simultaneously forming microelectronic structures on a silicon wafer. The microelectronic devices are created through a series of steps which include deposition of thin films of material, patterning of these thin films, etching of these thin films, and modification of the underlying materials.

33. A typical transistor to be crafted on a silicon wafer could look like the following:

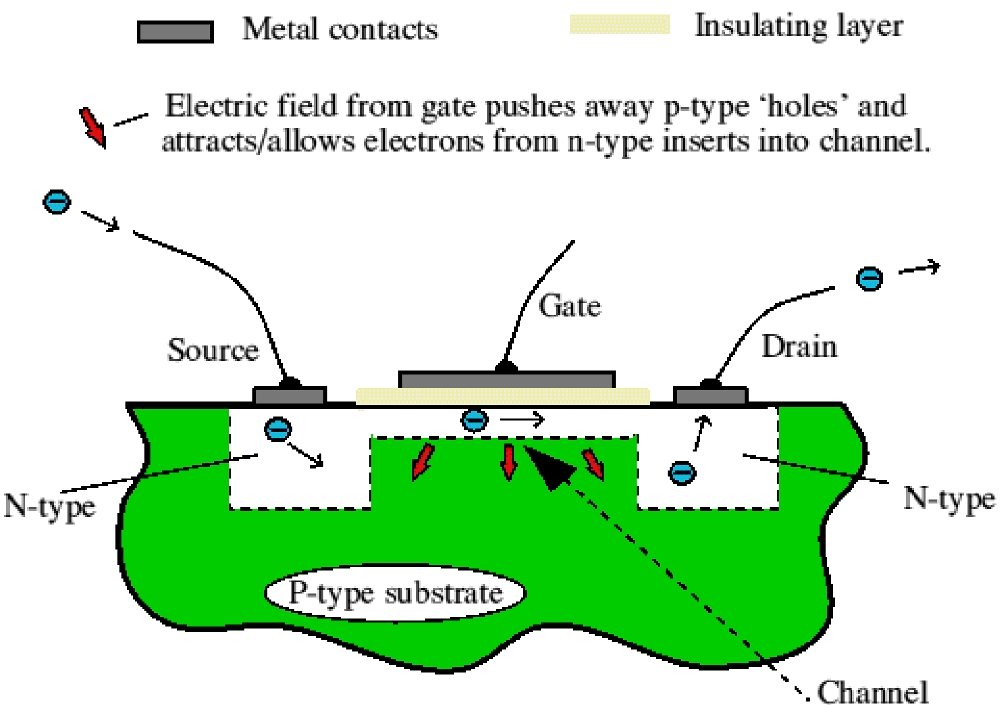


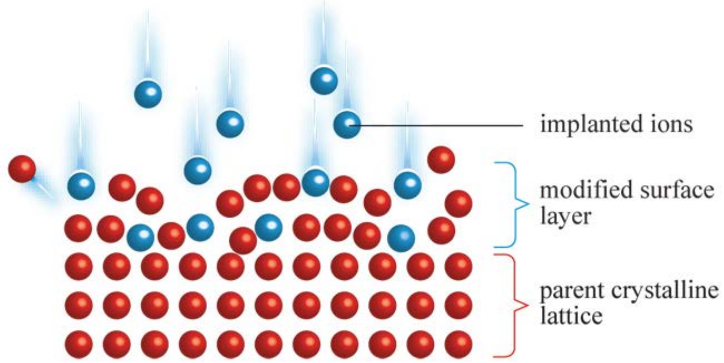
Figure 9.4 N-channel enhancement mode MOSFET.

https://www.st-andrews.ac.uk/~www_pa/Scots_Guide/first11/part9/fig4.gif

34. In this transistor, there are three "metal contacts" or "terminals," the Gate, Source, and Drain. The Gate is a conductive layer formed on a very thin

insulating layer upon the silicon substrate. The Source and Drain contacts are conductive layers in contact with source and drain diffusion regions of the silicon substrate that have been "doped" with the implantation of ions. If a positive voltage is applied to the Gate, a layer between the source and drain called the Channel connecting the source and drain diffusion regions will become more electrically conductive.

35. Diffusion regions are created by implanting ions of different dopants or impurities into the silicon substrate to create conductive regions. A highly energized stream of ions is directed at the substrate and some ions are captured by the substrate surface.



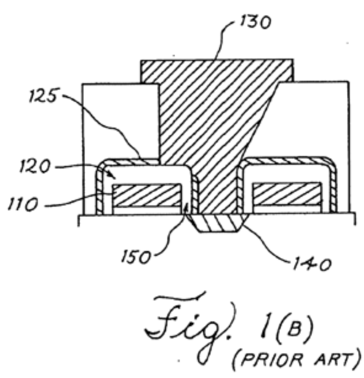
http://www.globalspec.com/learnmore/manufacturing_process_equipment/vacuum_equipment/thin_film_equipment/semiconductor_process_systems_cluster_tools

36. Once diffusion regions have been created, structures can then be created on the silicon substrate by the deposition of thin films of material. There are multiple methods of depositing materials, including chemical vapor deposition (CVD) and physical vapor deposition (PVD). In the CVD process, a gas is heated,

or a plasma is created, to form or "grow" a thin film or coating. This process is typically used for the deposition of dielectric (insulating) films. PVD uses the evaporation or sputtering of atoms to form a condensed film layer on a substrate.

37. For example, in our exemplar transistor, the thin insulating layer upon which the Gate sits can be formed as a thin layer of thermally-grown silicon dioxide. Next, the conductive material of the Gate, such as polysilicon, can be deposited upon the thermally-grown silicon dioxide using CVD.

38. As the 552 Patent describes as admitted prior art, in order to avoid "poor quality contacts" or "a short circuit" between the conductive material of the Gate and the Source and Drain Contacts, additional thin insulative films are deposited. *See* 552 Patent at 2:63-3:2. An exemplar structure can be seen in admitted prior art Figure 1(B) of the 552 Patent:



SAMSUNG-1001, 552 Patent at Figure 1(B)

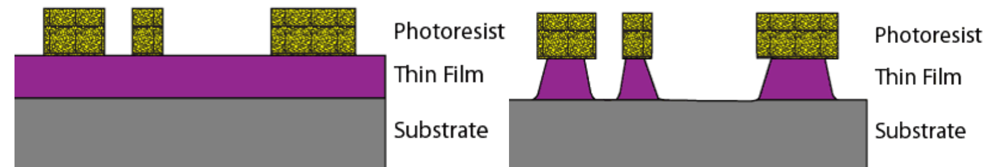
39. In Figure 1(B), region 140 is a diffusion region, 130 is a self-aligned contact region for connection to other devices, 110 is the conductive polysilicon

layer of the gate electrode, and 120 is an encapsulating dielectric layer. In Figure 1(B), layer 120 is intended to provide electrical insulation and to avoid a short circuit.

40. Insulating layer 120, as well as layer 125 and the unlabeled top layer, would be deposited on the substrate after Gate 110, as previously described.

41. In order to make a connection to the diffusion region 140 once these layers have been deposited, it is necessary to etch a contact opening, 130. Etching is the process of removing material. As was well known at the time of filing of the 552 Patent, etching broadly falls into two categories: wet etches, using liquid chemicals, and dry etches, using a gas.

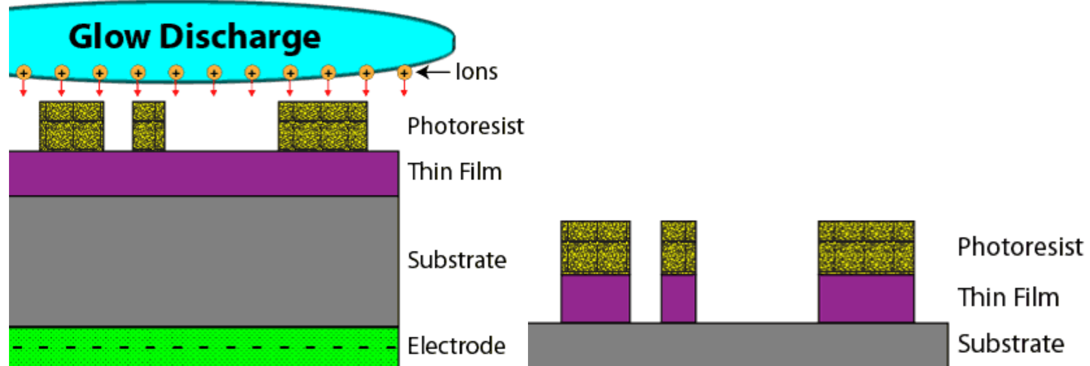
42. In a wet etch process, a liquid chemical dissolves the desired thin film, but not the photoresist used to create the etch pattern, the substrate, or a layer known as an etch stop. Wet etches are generally isotropic, meaning that the etch removes material in both the vertical and horizontal directions simultaneously. Figures depicting a semiconductor before and after a wet etch are shown below:



http://www.aplusphysics.com/courses/honors/microe/processing.html

43. In a dry etch process, a gaseous chemical is placed into a strong electric field, which produces gas ions, gas atoms and electrons in a glow

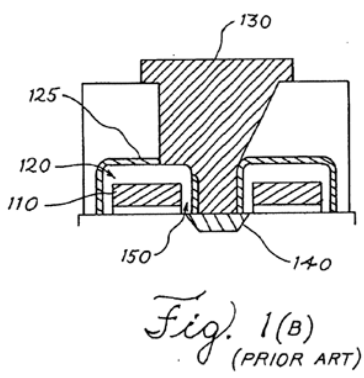
discharge. The gas ions can then be accelerated vertically downward away from the glow discharge toward the substrate. The acceleration of the ions physically and chemically attacks the thin film to be removed. This process is also known as reactive ion etching (RIE). A dry etch will typically create an anisotropic etch profile, meaning it removes materials in the vertical direction only. Figures depicting a dry etch are shown below:



http://www.aplusphysics.com/courses/honors/microe/processing.html

44. As was also well known, in addition to wet or dry etches and isotropic or anisotropic etches, etches may also be selective or non-selective for a specific thin film material. For example, as described in the admitted prior art of the 552 Patent, an etch that is selective for silicon nitride compared to silicon dioxide will effectively etch silicon nitride at a higher rate than silicon dioxide. *See* 552 Patent at 2:11-21. In contrast, a non-selective etch will etch away both types of materials at approximately the same rate. *Id.*

45. As was well known in the art, the selectivity of an etch could be combined with specific layers of materials to create an etch stop layer (e.g., layer 125 in Figure 1(B)).



SAMSUNG-1001, 552 Patent at Figure 1(B)

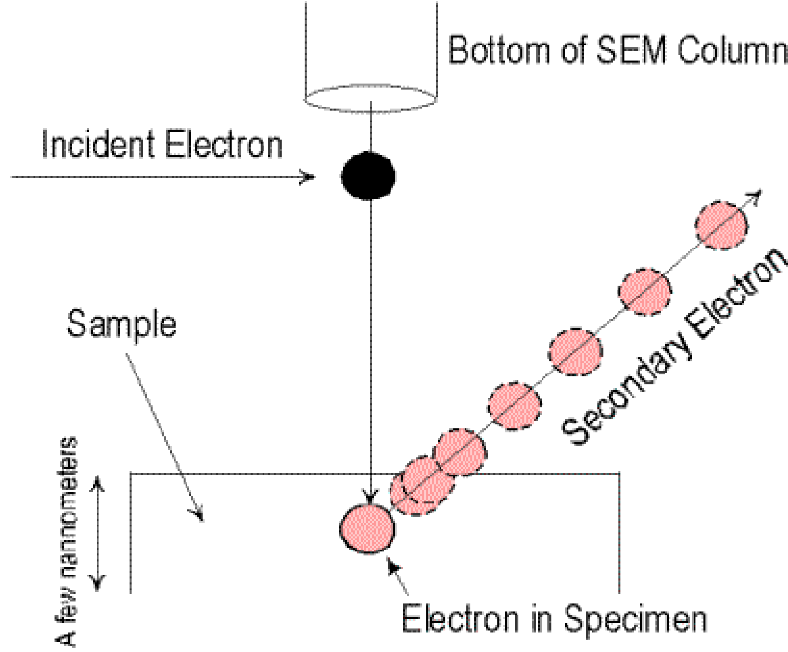
46. The etch stop layer effectively stops an etchant from further removing material beyond the etch stop layer. The "etch stop layer 125 permits subsequent etching of the substrate without risk of exposing the device structures and layers" protected by the etch stop layer. *Id.* at 4:13-18.

B. Technology Background: SEM Imaging

47. The Kuesters prior art reference, SAMSUNG-1005, contains scanning electron microscopy (SEM) images disclosing features of actual semiconductor devices fabricated in accordance with its teachings. In order to understand and read these images, some background is required on the SEM method and the reading of SEM images.

48. SEM is a method for high-resolution imaging of microscopic structures. SEM uses electrons for imaging, much as a light microscope uses visible light. SEM produces images of an object by scanning it with a focused beam of electrons. The electrons interact with atoms in the object, producing various signals that can be detected and that contain information about the object's surface topography and composition.

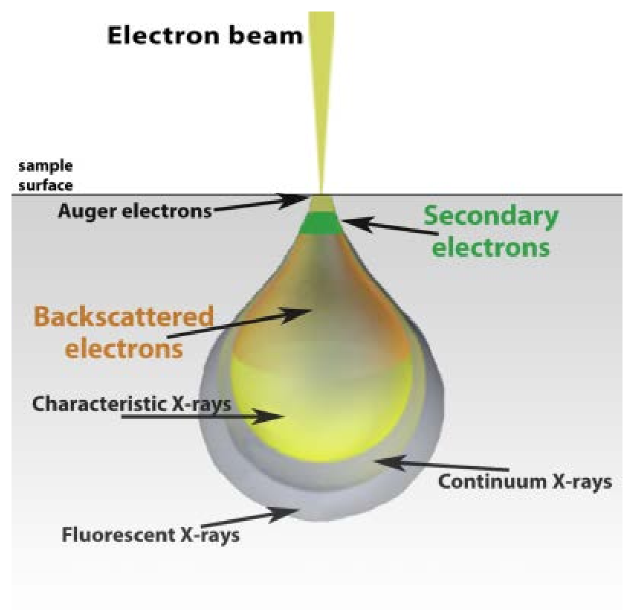
49. A common SEM imaging method is the detection of secondary electrons emitted by atoms excited by the electron beam. By scanning the object and collecting the secondary electrons with a detector, an image displaying the topography of the object is created. The number of secondary electrons that can be detected depends, among other things, on the angle at which the beam meets the surface of the object and the relative distances between the regions of the surface of the object and the electron detector.



A secondary electron is produced when an electron *from the material* is ejected by an incident electron from the beam. Secondary electrons have very low energy (<50 eV) and are emitted from very near the surface of the specimen - indeed probably from the coating.

http://www.geosci.ipfw.edu/cgi-bin/sem/techinfo.cgi?choice=secondelec

50. Secondary electron imaging collects low-energy secondary electrons that are ejected from the atoms of the object by inelastic scattering interactions with beam electrons. These secondary electrons are detected and converted into a two-dimensional intensity distribution that can be viewed and photographed, or converted using an analog-to-digital converter and saved as a digital image.



http://www.nanoscience.com/products/sem/technology-overview/sample-electron-interaction/

51. To create a SEM image, the incident electron beam is scanned in a raster pattern (e.g., left-to-right, top-to-bottom) across the sample’s surface. The emitted electrons are detected for each position in the scanned area by the electron detector. *See* http://www.charfac.umn.edu/sem_primer.pdf.

52. SEM images produced by secondary electrons use a very narrow electron beam. Due to the narrow width of the beam, the resulting SEM images have a large depth of field, yielding a three-dimensional appearance in a two-dimensional image.

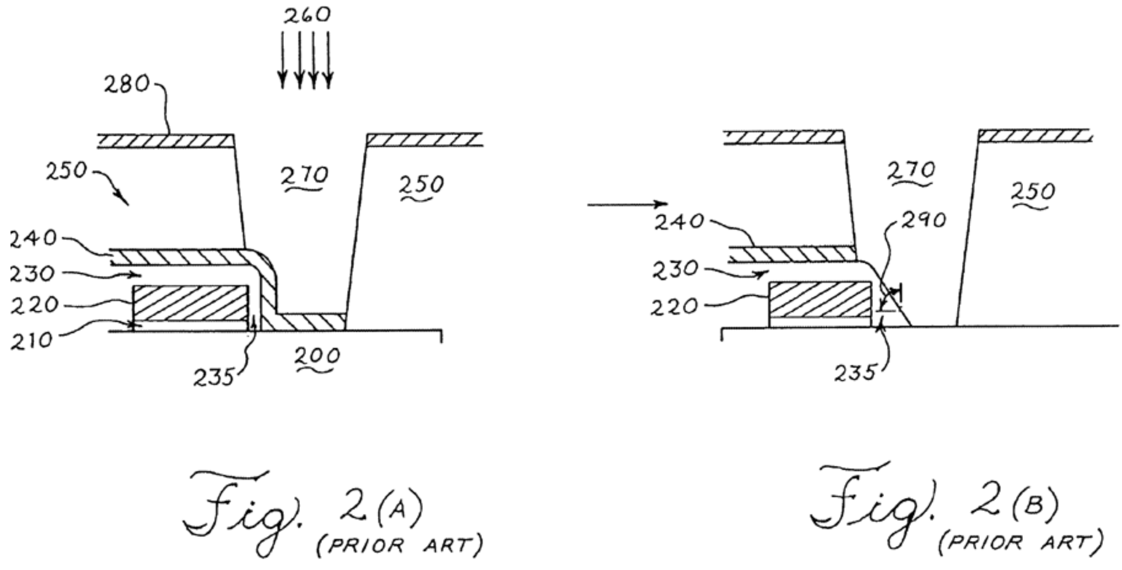
53. The topography of surface features of the object influences the number of electrons that reach the secondary electron detector from any point on

the scanned surface. *See* http://www.mee-inc.com/hamm/scanning-electron-microscopy-sem/. The brightness of the signal depends on the number of secondary electrons reaching the detector. Regions of the object that are closer to the detector will emit more electrons that will be picked up by the detector and thus will appear brighter. Regions of the object further away from the detector will emit fewer electrons that will be picked up by the detector and thus will appear darker. In other words, if the electron beam travels into a depression or hole in the object, the number of secondary electrons that can escape the sample surface is reduced and the image processing places a corresponding dark spot on the image. Conversely, if the electron beam scans across a projection or hill on the sample, more secondary electrons can escape the sample surface and the image processing places a bright spot on the image. *See* http://www.seallabs.com/how-sem-works.html. This local variation in electron intensity creates the image contrast that reveals the surface morphology.

C. The 552 Patent

54. The 552 Patent relates to "semiconductor device processes, and more particularly, to improved methods for etching openings in insulating layers and a semiconductor device with well defined contact openings." 552 Patent at 1:10-13.

55. The 552 Patent discloses the prior art process for fabricating semiconductors discussed briefly above. *See also* Figures 2(A) and 2(B).



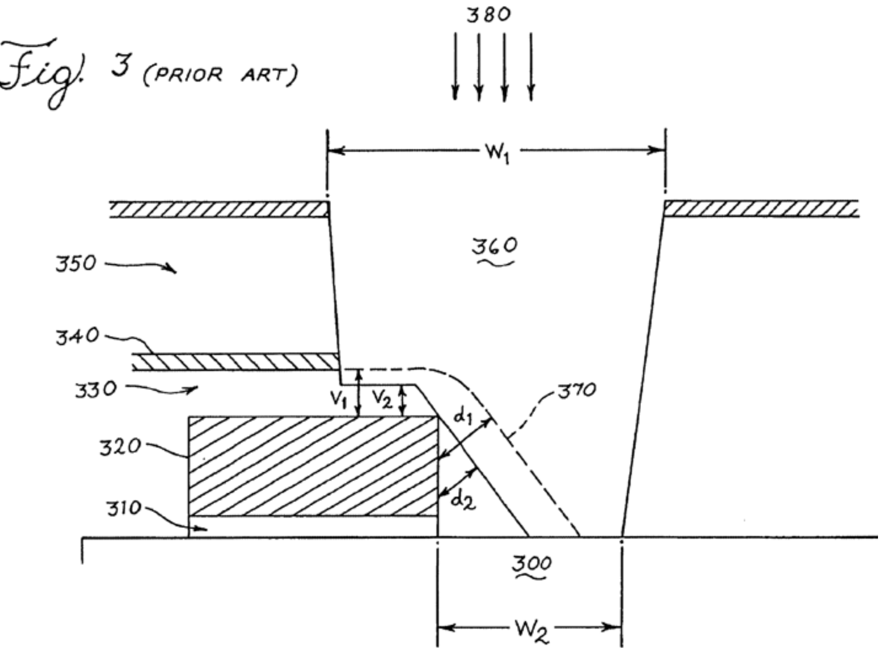
SAMSUNG-1001, 552 Patent at Figures 2(A) and 2(B)

In Figures 2(A) and 2(B), a gate oxide layer 210 is formed on the substrate 200. On the gate oxide, a conductive layer 220 is formed. Over the conductive layer, an insulating layer 230 is deposited. Alongside the conductive layer, the insulating material forms an insulating spacer 235. This insulating spacer protects the conductive layer from any conductive material later added to the contact region 270. Over the insulating layer, insulating spacer, and the bottom of the contact region, an etch stop layer 240 is deposited, and atop the etch stop layer, a further blanket layer 250. *Id.* at 4:48-5:17.

56. The alleged problem that the 552 Patent purports to solve is that existing semiconductor fabrication processes described in the patent causes the insulating spacers alongside the Gate electrode to become sloped. *Id.* at 5:4-17. According to the 552 Patent, when an etch is performed in the contact region 270

to remove the remaining etch stop material 240, the insulating spacer 235 on the sidewall of the gate electrode 220 transforms from "substantially rectangular" to a "sloping or tapered" shape. *Id.* at 5:4-17. The 552 Patent further claims that due to ease of completely filling the contact region 270 and "good step coverage, industry preference is for sloped spacers… similar to that shown in FIG. 2(B)." *Id.* at 5:31-34.

57. The 552 Patent continues by alleging that subsequent etches to clean the contact region will further erode the sloped sidewall spacer, creating additional risk of short circuit. This further erosion is illustrated in Figure 3:



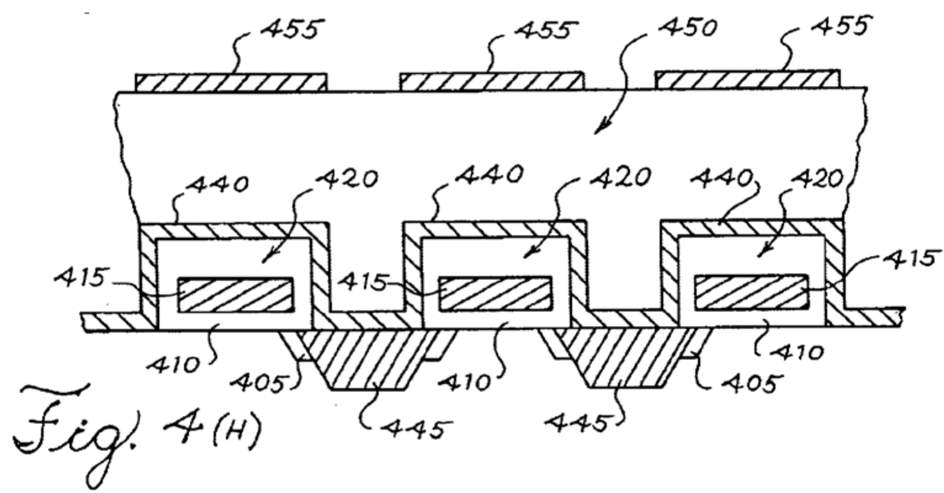
SAMSUNG-1001, 552 Patent at Figure 3

58. In Figure 3, the sloped sidewall spacer has been eroded from the dotted line to the solid line. This can cause the gate electrode 320 to short circuit to the conductive material later deposited in contact region 360. *Id.* at 6:13-21.

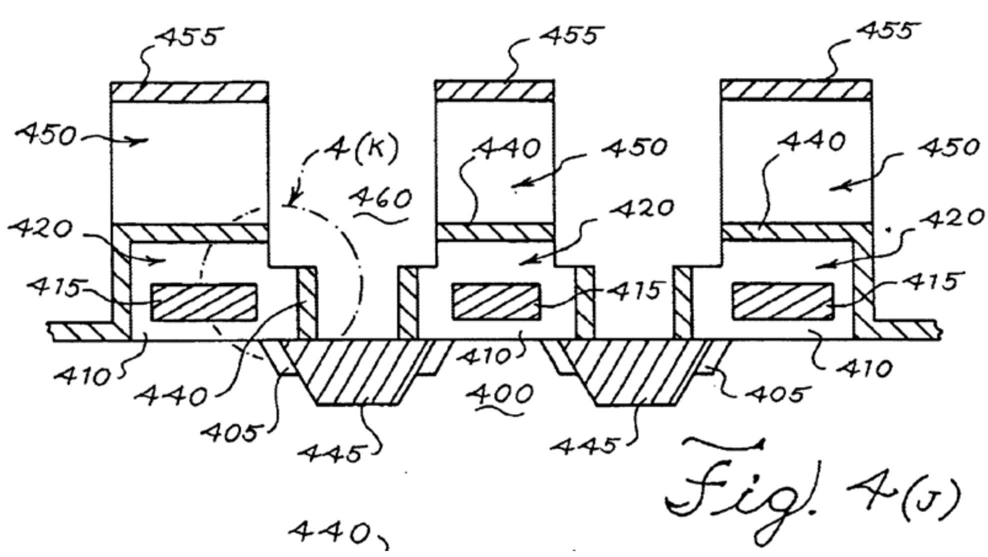
59. Notably, the 552 Patent discloses as existing prior art the use of sidewall spacers to protect a gate electrode, the use of anisotropic etches to remove material in a vertical direction, and the use of etchants generally in combination with the deposition of layers on a substrate to create an integrated circuit device. *See id.* at 1:10-7:13.

60. The alleged inventive concept is to take care "to etch the spacers 435 such that the spacers 435 have a substantially rectangular profile." *Id.* at 11:48-49. The "invention relates to these process conditions as well as others that result in the retention of a boxy spacer." *Id.* at 13:14-16. The 552 Patent accomplishes this through the use of an etch that is "almost completely anisotropic, meaning that the etchant etches in one direction—in this case, vertically (or perpendicular relative to the substrate surface) rather than horizontally." *Id.* at 7:45-48. This etch "retains the substantially rectangular lateral spacer portion of the first insulating layer." *Id.* at 7:49-51.

61. The alleged inventive concept embodied in the independent claims is clearly illustrated in Figures 4(H) and 4(J):



SAMSUNG-1001, 552 Patent at Figure 4(H)



SAMSUNG-1001, 552 Patent at Figure 4(J)

62. Figures 4(H) and 4(J) illustrate "a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the

etch stop layer," a photoresist patterning layer 455, and contact openings 460 to the diffusion regions 405. *Id.* at 9:27-32, 9:41-45. In the figure, a conductive layer corresponding to the gate electrode 415 is deposited by low pressure CVD and was encapsulated by the oxide layer 420. *Id.* at 10:31-65. Region 405 is a conductive region formed in the substrate to create the source and drain diffusion regions. *Id.* at 10:35-36. Over the oxide layer 420 is deposited an etch stop layer of silicon nitride, 440. *Id.* at 11:63-66. On the etch stop layer 440 is deposited a second insulating blanket layer of silicon oxide, 450. *Id.* at 12:21-23. Once these layers have been deposited, the contact regions 460 are etched open. *Id.* at 12:35-43. Once that etch is performed, a second dry etch is performed to remove the horizontal etch stop material from the base of the contact region. *Id.* at 12:44-53. This results in Figure 4(J), with substantially rectangular sidewall spacers. *Id.* at 13:5-6.

63. The dependent claims add minor implementation details, such as additional specificity regarding the materials used for an etch stop (claims 2-3), claims regarding the topography of the sidewall spacers (claims 4-5, 9-10), and claims for additional insulating and conductive layers (claims 6-7, 11-12).

64. Notably, the 552 Patent is clear that it is directed not simply to the disclosed method, but to all process conditions "that result in the retention of a

boxy spacer…. Thus the etch-stop etch conditions should be regarded in an illustrative rather than restrictive sense." *Id.* at 13:13-18.

VI. 552 PATENT PROSECUTION HISTORY

65. I have reviewed the prosecution history of the 552 Patent as well as the prosecution history of its parent, the 555 Patent.

66. I understand that the application that led to the issuance of the 552 Patent was originally filed with 26 claims. SAMSUNG-1002, Mar. 31, 2000 Application at 1002.039-43. In a preliminary amendment filed the same day, claims 1-24 were canceled and new claims 27-39 were added. *Id.,* Mar. 31, 2000 Preliminary Amendment at 1002.066-67. The independent claims were generally directed to a prior art transistor structure comprising a substrate, a conductive material formed in a substrate (i.e. a source/drain region), a conductive layer on the substrate (i.e. a gate), an insulative layer on the conductive layer, a contact region, an insulating spacer, an etch stop material, and a second insulative blanket layer. *See id.* Dependent claims added the limitation that the insulative spacers have "a substantially rectangular cross-sectional shape that is substantially perpendicular to the substrate surface." *Id.*

67. On June 1 2001, the Examiner rejected all claims. The primary point of the rejections was that all claims but one were anticipated by Dennison. The examiner found that Dennison disclosed all of the claim limitations, including the

substantially rectangular profile of the insulative spacers. *Id.,* May 30, 2001 Office Action at 1002.079-81. The Examiner further found that claim 26 (current claim 3) was obvious over Dennison in view of Gonzalez. Gonzalez disclosed that "the etch stop layer is silicon dioxide." *Id.* at 1002.081.

68. In an amendment and response filed October 4, 2001, the applicants responded that Dennison does not disclose an etch stop layer separate from and of a different material than the underlying insulative layer. *Id.,* Oct. 1, 2001 Amendment at 1002.108.

69. On January 4, 2002, the Examiner rejected the applicants' arguments and made the rejection final. *Id*., Jan. 4, 2002 Final Office Action at 1002.138-44.

70. Following an Examiner interview, the applicants amended the claims to expressly require that the etch stop material be of a different material than the insulative spacer. *Id.,* April 29, 2002 Amendment and Response After Final at 1002.151-53. The applicants further argued that the present invention avoids the problem of sloping spacers that "limit the number of structures that can be included on a device" by "retaining the substantially rectangular profile of the insulating spacers." *Id.* at 1002.152.

71. Following a continued prosecution application request, the Examiner again rejected all claims on August 14, 2002. The Examiner rejected the claims as obvious over Dennison in view of Figura and Gonzalez. *Id.* August 14, 2002

Office Action at 1002.170-73. On March 11, 2003, the applicants attempted unsuccessfully to traverse the rejection, and on May 14, 2003 the rejection was made final. *See id.,* March 11, 2003 Request for Reconsideration at 1002.182-85; May 14, 2003 Final Office Action at 1002.187-94.

72. On February 6, 2004, the applicants again amended the independent claims, this time to add the limitation that the insulating spacer "has a substantially rectangular profile in the contact region." *Id.,* Feb. 6, 2004 Amendment at 1002.216.

73. On March 31, 2004, the applicants amended the specification to add "[t]he phrase 'substantially rectangular' means that a side of the spacer has an angle relative to the substrate surface of more than 85°." *Id.,* Mar. 31, 2004 Corrected Amendment at 1002.234. The applicant further amended the independent claims to remove the "substantially rectangular" language and add "wherein a side of the insulating spacer has an angle relative to the substrate surface of more than 85°." *Id.* at 1002.235. Following this amendment, the Examiner allowed the claims. *Id.* Apr. 7, 2004 Notice of Allowability at 1002.239-42.

VII. CLAIM CONSTRUCTIONS

A. Legal Standard

74. I understand that because the 552 Patent has expired, the *Phillips* standard applies for the purposes of claim construction. I further understand that the *Phillips* standard requires that the claim terms be given their plain and ordinary meaning as understood by a person of ordinary skill in the art at the time of the invention in light of the claim language and the patent specification.

75. I further understand that any claim term that lacks a definition in the specification is therefore given its plain and ordinary meaning as understood by one of ordinary skill in the art.

76. I applied the *Phillips* standard to my review of the claims of the 552 Patent discussed below, including, without limitation, the claim term that I specifically discuss below.

B. "contact region/opening" (claims 1, 4, 7, 8, and 12)

77. The terms "contact region" or "contact opening" are limitations of independent claims 1 and 8 of the 552 Patent as well as dependent claims 4, 7, and 12. Specifically, claim 1 requires "a contact region in said first insulating layer." 552 Patent at Claim 1. Similarly, claim 8 requires "a contact opening in a region adjacent to a second electrically conductive material formed on the substrate." *Id.* at Claim 8.

78. A person of ordinary skill in the art would have understood that the plain and ordinary meaning of "contact region" or "contact opening" is a "contact opening or via" in the context of the 552 Patent.

79. The 552 Patent expressly defines "contact opening" and "contact region" as "contact openings and/or via." *Id.* at 1:38-41 ("For purposes of the claimed invention, henceforth 'contact opening' or 'contact region' will be used to refer to contact openings and/or via.").

80. Furthermore, in the pending litigation between the Patent Owner and Intel Corporation, the parties have agreed that the plain and ordinary meaning of the term "contact region" should be construed to mean "contact openings and/or vias." SAMSUNG-1009, Civil Action No. 6:15-cv-130-RWS (E.D. Tex.), *DSS Technology Management, Inc. v. Intel Corporation, et al.*, Dkt. No. 165-1 at 1009.007.

VIII. THE PRIOR ART

A. "Self Aligned Bitline Contact For 4 Mbit dRAM" ("Kuesters")

81. I understand that Kuesters is prior art to the 552 Patent under 35 U.S.C. § 102(b).[1] "Self Aligned Bitline Contact For 4 Mbit dRAM," authored by

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[1] While I understand that it is the Patent Owner's burden to establish that a prior art publication is not enabled, I nonetheless believe that the detailed disclosure in

K.H. Kuesters, H.M. Muehlhoff, G. Enders, E.G. Mohr, and W. Mueller was published in the *Proceedings of the First International Symposium on Ultra Large Scale Integration Science and Technology* in 1987 ("Kuesters," SAMSUNG-1005).

82. Kuesters is directed to a 4 Mbit dRAM cell with a 25% reduction in cell size, "achieved by a self aligned bitline contact, which is fully overlapping gate and field oxide (FOBIC)." SAMSUNG-1005, Kuesters at 1005.003. The dRAM structure comprises a "gate [] encapsulated by oxide using an oxide spacer technique." *Id.* Furthermore, a "thin oxide/nitride/oxide dielectric allows a contact hole etch, which does not significantly affect the oxide insulation of the gate and the field oxide." *Id.* In this structure the "nitride serves as an etch stop for [the] top oxide etch." *Id.*

83. At its core, the Kuesters paper is about a "new technique for etching the dielectric underneath the bitline" that "ensure[s] a good insulation of bitline to

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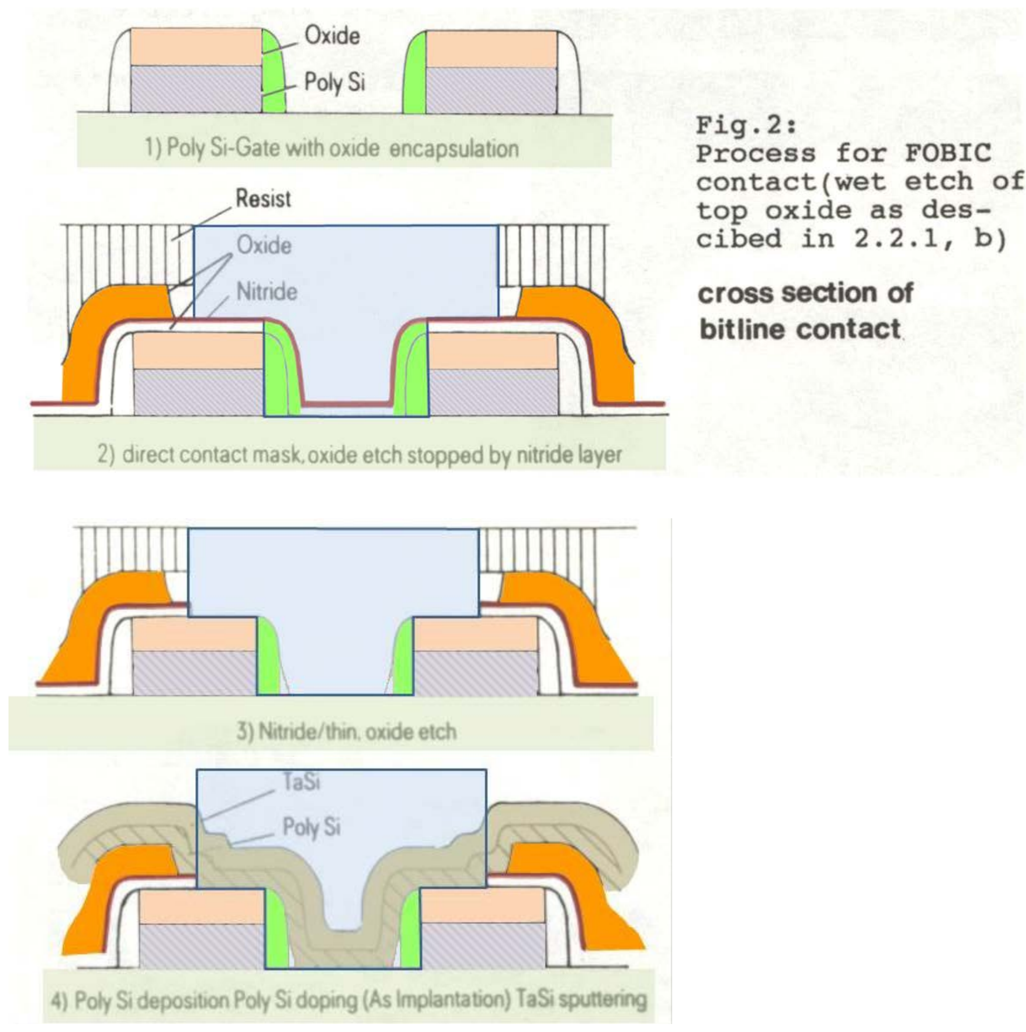
Kuesters would permit a person of ordinary skill in the art to fabricate the disclosed dRAM structures without undue experimentation. As described herein, Kuesters provides significant detail regarding layer chemistries, etching chemistries and conditions, specific measurements for semiconductor layers, and detailed figures and SEM images.

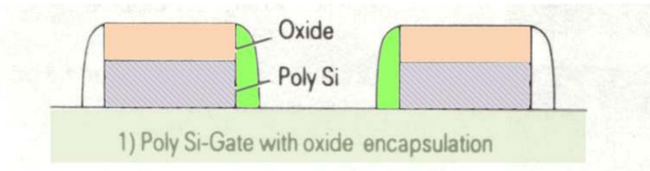
polysilicon gates (wordline) and substrate for the overlapping contacts." *Id.* at 1005.004.

84. The overall fabrication process flow is most easily described in reference to Figures 2 and 4a. The labels and arrows are present in the original publication, while the color annotation has been added for clarity:



SAMSUNG-1005, Kuesters at Figure 2 (with annotations)

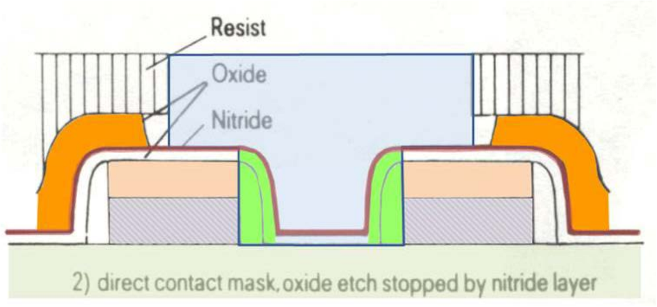
85. First, a double layer of polysilicon (the gate structure in purple and labeled "Poly Si" in Figure 2-1) and oxide (the insulating cap in light orange and labeled "Oxide" in Figure 2-1) is patterned on the surface of a silicon substrate. *Id.* at 1005.004. Then a 0.3 µm tetraethylorthosilicate ("TEOS") oxide sidewall spacer is formed by oxide deposition and RIE etching (in bright green above). *Id.* "A vertical etch profile of poly Si/oxide which can be achieved by sequential oxide etch (CHF_3/O_2) and poly Si etch (Cl_2/He) is essential." *Id.* TEOS is an electrically insulating material used to prevent electrical shorts between conductive layers. This structure is illustrated in Figure 2-1:



SAMSUNG-1005, Kuesters at Figure 2-1 (with annotations)

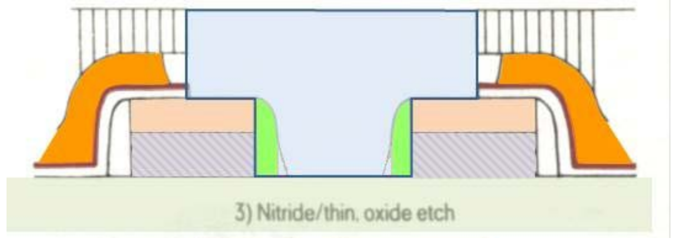
86. Once this structure has been patterned, a "triple layer of thin oxide/nitride/oxide" is deposited over the entire structure ("Oxide" annotated in orange, on "Nitride" annotated in red, on "Oxide" annotated in white in Figure 2-2). *Id.* The nitride layer serves as "an etch stop" and "allows a contact hole etch, which does not significantly affect the field oxide and the oxide insulation of the gate." *Id.* The thin oxide beneath the nitride layer is a liner layer that protects the silicon substrate from the nitride etch stop and becomes part of the insulating spacer. This thin oxide, where it overlays the original oxide spacer, becomes part

of the insulating spacer in the contact regions (in bright green). This thin oxide is the same material as the original oxide spacer, and the two layers are indistinguishable in the SEM imagery. *See id.* at Figure 4a. Over the nitride layer is a top oxide of a PH_3 diffused oxide (in bright orange in Figure 2-2 above). *Id.* "After patterning the contact hole mask, the top oxide is etched using the nitride as an etch stop." *Id.* This structure is illustrated in Figure 2-2:



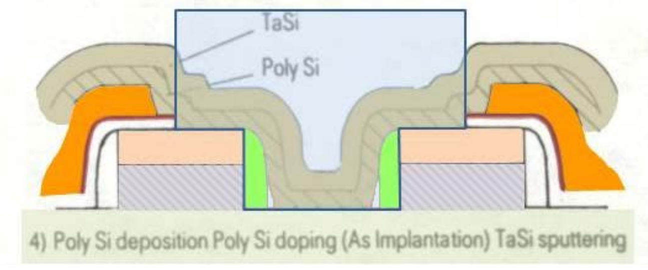
SAMSUNG-1005, Kuesters at Figure 2-2 (with annotations)

87. In Figure 2-2 above, the top oxide layer has been etched using the wet etch process disclosed in Section 2.2.1(b). *Id.* at 1005.005. Once the top oxide has been etched, the nitride is "etched by the same CHF_3/O_2 dry etch step (Fig. 4a)." *Id.* "If any conventional contacts are patterned by the same mask and technique, the contact hole size is not affected by a wet etch step for the top oxide as the underlying nitride/oxide is etched anisotropically." *Id.* "The contact area of the FOBIC contact is defined by gate and field oxide edges." *Id.* This structure is illustrated in Figure 2-3:



SAMSUNG-1005, Kuesters at Figure 2-3 (with annotations)

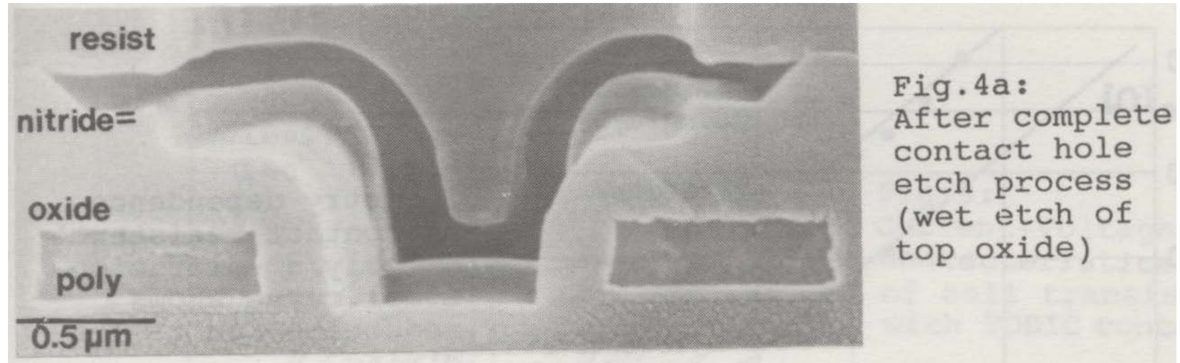
88. Once the contact hole is etched, the bitline is formed by tantalum silicide (labeled "TaSi" and annotated in light brown in Figure 2-4) on top of poly Si (labeled "Poly Si" and annotated in light brown in Figure 2-4). *Id.* at 1005.006. The Poly Si "is doped by As or P implantation." *Id.* A person of ordinary skill in the art would recognize that this bitline is a conductive material intended to provide a contact to the source or drain region. *See id.* This structure is illustrated in Figure 2-4:



SAMSUNG-1005, Kuesters at Figure 2-4 (with annotations)

89. Kuesters further discloses that nitride layer thickness is reduced to 30 nanometers in order to "avoid any effect on leakage current (for all CVD nitride deposition parameters)." *Id.* at 1005.007. This favors the "contact hole etch process including a wet etch step (*see* Section 2.2.1)." *Id.*

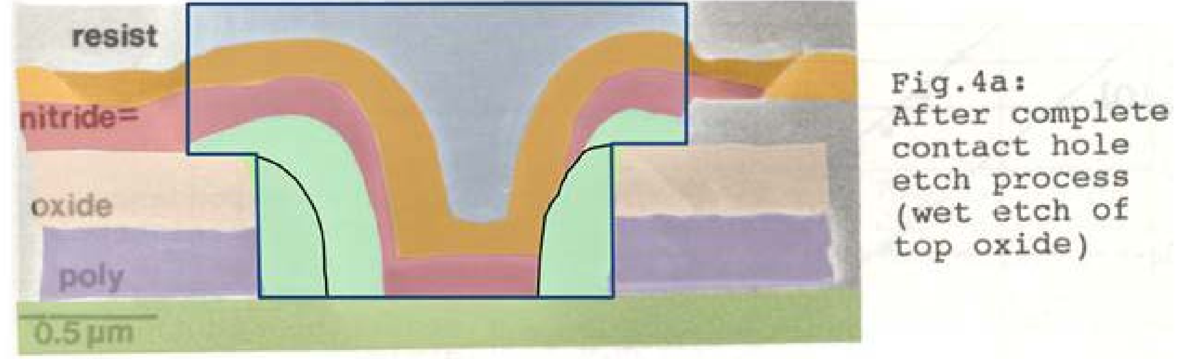
90. In Figure 4a, Kuesters includes a cross-section SEM image of the actual structure created with a wet etch of the top oxide followed by an anisotropic dry etch process as described in Kuesters:



SAMSUNG-1005, Kuesters at Figure 4a

91. As can be seen in Figure 4a as it appears in the original publication, the gradation of brightness reflects the topology of the actual dRAM structure. The front plane of the cross-section SEM image reveals the poly gate (labeled "poly"), the insulating cap oxide (labeled "oxide"), and the oxide sidewall spacer. The back plane of the SEM image reveals the nitride layer where it was not removed by contact etching (labeled "nitride" and appearing grey) sitting beneath the recessed PH_3 diffused oxide (appearing black). Since the back of the contact hole was masked against the contact etch, it shows the initial structure of the deposited thin oxide/nitride/oxide layers. It can be seen that at the back plane of the contact hole the nitride layer remains over the insulating layer, adjacent to the sidewall spacer, and across the source/drain region.

92. The annotated version of Figure 4a includes the same coloring as Figure 2, for illustration of the elements of the structure.



SAMSUNG-1005, Kuesters at Figure 4a (with annotations)

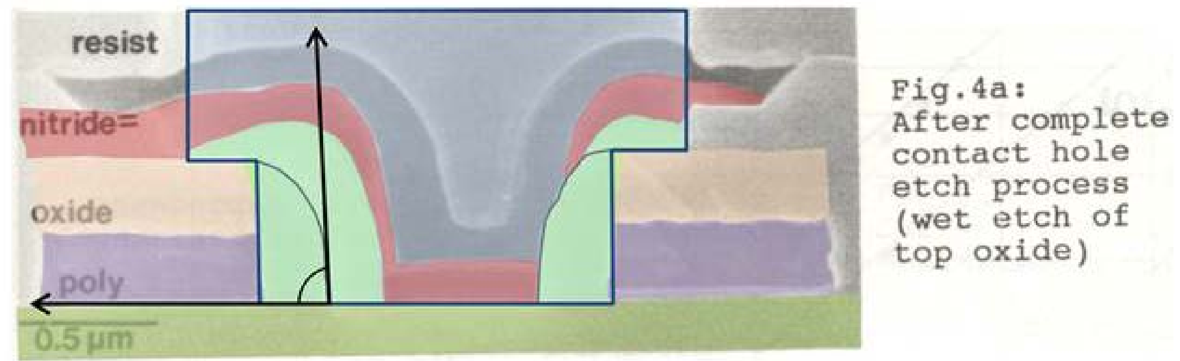
93. Looking to the annotated structure disclosed in Figure 4a, the basic layers of the structure can be observed both at the front plane of the SEM (i.e. the center of the contact hole) as well as at the back plane of the SEM (i.e. the back edge of the contact hole). As seen from the front plane the poly Si gate layer (labeled "poly" in the original Figure 4a) has been annotated in purple. Atop the conductive gate is an oxide layer showing the insulating cap annotated in light orange (labeled "oxide" in the original Figure 4a) and adjacent to the insulating cap and poly Si gate is the oxide insulating spacer annotated in bright green. The black line on the insulating spacer denotes the leading edge of the insulating spacer at the front plane of the SEM image (i.e. the center of the contact hole). Above the black line is an additional section of the insulating spacer annotated in bright green. This region is the sidewall spacer receding into the page toward the back plane of the

contact hole. As described above, the incident angle of the electron beam of the SEM to the surface of the sidewall spacer in this area is not 90°, and so it appears brighter in the original Figure 4a due to the larger number of emitted secondary electrons.

94. Over the insulating layer, adjacent to the insulating spacer, and over the bottom of the contact hole is the silicon nitride etch stop layer at the back plane of the contact hole (annotated in red and labeled "nitride" in the original Figure 4a). This is the nitride etch stop material that was not removed from the back plane of the contact hole as part of the anisotropic etch. This region appears darker in the original Figure 4a because it is recessed into the page and is present at the back plane of the contact hole. This is because the nitride layer has been etched away from most of the center of the contact hole by the anisotropic dry etch process, but the nitride along the back plane was masked and was not substantially attacked. Thus, the nitride along the back plane largely remains in place.

95. Finally, the orange region above the nitride layer is the remaining PH_3 diffused oxide layer. The top oxide layer in the contact hole was wet etched in an isotropic etch process. As a result, the top oxide layer has receded into the wall at the back plane of the contact hole in a fashion similar to how it has receded under the resist layer. This recession is illustrated by the dark region in the original Figure 4a with very few or no collected secondary electrons.

96. The angle of a side of the insulating spacer relative to the substrate surface can be measured where it contacts the pale green of the substrate. I have measured this angle for the left sidewall spacer (as annotated below) and found that the angle was between 86° and 87°. Thus the SEM in Figure 4a clearly discloses an angle of a side of the sidewall spacer relative to the substrate of greater than 85°.



SAMSUNG-1005, Kuesters at Figure 4a (with annotations)

B. U.S. Patent No. 5,482,894 ("Havemann")

97. I understand that Havemann is prior art to the 552 Patent under 35 U.S.C. § 102(e). U.S. Patent No. 5,482,894 ("Havemann," SAMSUNG-1006), entitled "Method of Fabricating a Self-Aligned Contact Using Organic Dielectric Materials," was filed on August 23, 1994. Havemann issued on January 9, 1996 to Robert H. Havemann.

98. Havemann is directed to the "fabrication of semiconductor devices and more particularly to the formation of self-aligned contacts on such devices." SAMSUNG-1006, Havemann at 1:23-25.

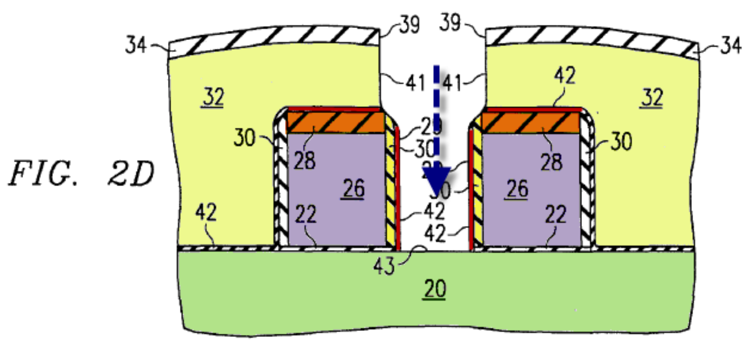
99. Havemann discloses that in order to "facilitate extremely dense circuit layouts, it is desirable at times to fabricate the lowest conductor level (which typically includes transistor gates) with conductors at minimum spacing." *Id.* at 1:42-45. This spacing "may make a self-aligned contact (SACT) necessary for, e.g., electrically connecting to source/drain active regions located in the narrow gaps between the conductors." *Id.* at 1:45-48.

100. The invention of Havemann is a "method of producing a structure for self-aligned contacts on semiconductor devices" that is "capable of reliably forming contacts in narrow, high-aspect ratio gaps." *Id.* at 2:10-14. Furthermore, "the invention may provide advantages for SACTs in general: a high quality conformal dielectric such as thermal oxide may be used as insulation between an SACT and adjacent conductors; this oxide may be made relatively thin for enhancing a capacitive storage node (e.g. DRAM applications)…." *Id.* at 2:15-20.

101. One example of the inventive method of Havemann begins by forming two conductive layers on a substrate each with an insulating cap. *Id.* at 2:40-45. Next, these conductors and the substrate are covered with a conformal dielectric layer. *Id.* at 2:46-49. Next, an organic-containing dielectric layer may

be deposited over the conductors and a further inorganic cap layer may be deposited over the organic layer. *Id.* at 2:52-54.

102. This structure is most easily seen in Figure 2D:



SAMSUNG-1006, Havemann at Figure 2D (with annotations)

103. In Figure 2D, the two conductive regions are the purple shaded polysilicon conductors. *Id.* at 5:10-15, 6:11-14. The insulating cap is the orange shaded region (28) and the sidewall spacer (30) is the yellow shaded region. Both are preferably silicon dioxide, but may also be silicon oxynitride. *Id.* at 5:9-15, 6:14-19. Over these layers is the etch stop layer shaded in red (42), which is preferably silicon nitride, but may be a thermally-grown silicon dioxide. *Id.* at 5:16-21, 6:31-33. Layer 32, shaded in pale yellow is the organic-containing dielectric layer. *Id.* at 6:20-23. Layer 34, unshaded, is the disclosed inorganic cap layer. *Id.* at 6:23-25.

104. Havemann further discloses that the contact holes are created through "anisotropic etch[ing] by known methods to remove conformal dielectric 30 (and

possibly gate oxide 22) from horizontal exposed surfaces." *Id.* at 5:6-9. Havemann discloses that an anisotropic etch is "substantially in one direction, usually vertical." *Id.* at 4:37-40.

105. Once the contact window has been formed through the anisotropic dry etching, a contact plug of a conductive material is deposited in the contact window. *Id.* at 5:40-45.

C. U.S. Patent No. 4,686,000 ("Heath")

106. I understand that Heath is prior art to the 552 Patent under 35 U.S.C. § 102(b). U.S. Patent No. 4,686,000 ("Heath," SAMSUNG-1007), entitled "Self-Aligned Contact Process," was filed on February 19, 1986. Heath issued on August 11, 1987 to Barbara A. Heath.

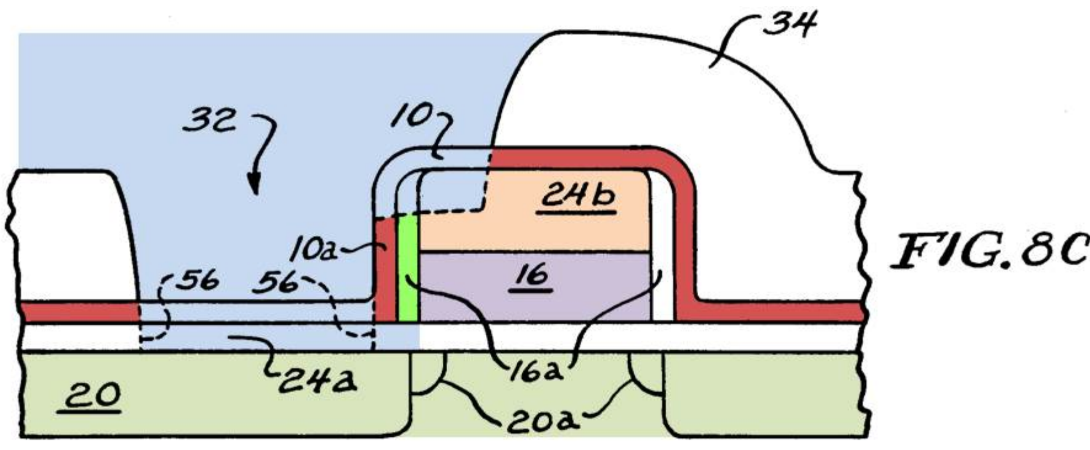
107. Heath is directed to an "improved process for self-aligned contact window formation in an integrated circuit" that "leaves a 'Stick' of etch stop on vertical sidewall surfaces to be protected." SAMSUNG-1007, Heath at Abstract. "The technique includes, in the preferred embodiment, a layer of oxide over active areas and on top of the gate electrode of a transistor." *Id.* "A silicon nitride layer acting as an etch stop is included between the oxide and interlevel dielectric such as BPSG." *Id.*

108. Heath discloses that a use for a "contact window is to provide electrical contact with a source/drain region which has been formed in a substrate."

Id. at 1:32-34. "Near the contact window there will generally be found another element such as a gate electrode" and, "with the increasing density of integrated circuits, the geometries become smaller, and obviously the space separating the contact windows from nearby elements becomes less." *Id.* at 1:34-40.

109. The invention of Heath is a process "for self-aligned contacts in a VLSI circuit which is independent of sidewall processes (on the gate electrode) used to optimize device performance." *Id.* at 4:63-66. The Heath process tolerates "the addition of any amount of oxide to the sidewall for any purpose such as isolation from a later established interconnect or other element…." *Id.* at 5:3-6.

110. This structure is most easily seen in Figure 8C:



SAMSUNG-1007, Heath at Figure 8C (with annotations)

111. In Figure 8C, above, layers 24*a* and 24*b* are an oxide layer that "is relatively thin over the source/drain 20 as show at 24*a*, but is relatively thick on the top of gate electrode 16, as shown at 24*b*." *Id.* at 9:52-55. Layer 16, in purple, is the conductive layer on the substrate (light green layer 20), and layer 24*b*, in

orange, is the insulating layer on the first conductive layer. Layer 16a, in bright green, is "a sidewall spacer" that is "formed illustratively of oxide" and "remains in the structure after completion of the circuit." *Id.* at 10:18-25. Etch stop layer 10, in red, is composed of nitride and stops the etch of the interlevel dielectric layer 34. *Id.* at 9:63-67. An anisotropic dry etch is then performed and "the part of layer 10 between dashed lines 56 is removed" as well as "the then-exposed parts of oxide 24*a* and 24*b*." *Id.* at 10:1-5.

112. Once the anisotropic dry etch is performed, a "metal or other conductive material for interconnects" is added to the contact window. *Id.* at 12:42-43.

IX. OBVIOUSNESS COMBINATIONS – MOTIVATIONS TO COMBINE

A. Kuesters in Combination with Havemann

113. A person of ordinary skill in the art would have been motivated to combine Kuesters with the teachings of Havemann that the sidewall spacer could be silicon oxynitride and the etch stop material could be silicon dioxide for several reasons.

114. First, both Kuesters and Havemann are directed to similar methods to create the same types of structures in the same field. *Compare* Kuesters at 1005.003 (describing a 4 Mbit dRAM cell with a 25% reduction in cell size, "achieved by a self aligned bitline contact") *with* Havemann at 1:23-25 (directed to

the "fabrication of semiconductor devices and more particularly to the formation of self-aligned contacts on such devices") and 2:15-20 (the invention can be used "for enhancing a capacitive storage node (e.g. DRAM applications)…."). Furthermore, the structures of Kuesters and Havemann are extremely similar and would have been compatible. *Compare* Kuesters at Figures 2 and 4a *with* Havemann at Figure 2D. A person of ordinary skill in the art would have been motivated to combine compatible teachings of references that are addressing the same problems in a similar and compatible way to create the same types of devices with the same characteristics.

115. Furthermore, it would have been obvious to one of ordinary skill in the art to make the simple substitution of the etch stop and spacer material chemistries disclosed in Havemann in the context of the Kuesters semiconductor structure. As described above, Kuesters and Havemann both describe using the same preferred materials for their insulating cap, insulating spacer, etch stop, and blanket insulating layers. *See* Kuesters at 1005.004; Havemann at 6:5-34. Havemann further teaches, however, that the simple substitution of using silicon oxynitride for the insulating layers, including the sidewall spacer, and using silicon dioxide for the etch stop layer adjacent to the sidewall spacer would produce predictable and successful results. *See* Havemann at 6:5-34. These were known alternatives and their use would achieve the same results. A person of ordinary

skill in the art would have known that these different materials would have different characteristics that would motivate substitution of compatible materials. *See* SAMSUNG-1011, Sorab K. Ghandhi, *VLSI Fabrication Principles Silicon and Gallium Arsenide* at 1011.003-04 (John Wiley & Sons, 1983) (detailing the benefits and tradeoffs in using silicon nitride). Thus, it would have been obvious to make the same substitution in the similar structure disclosed in Kuesters.

116. Additionally, it would have been obvious to one of ordinary skill in the art to apply the known technique of substituting silicon oxynitride for silicon oxide in insulating layers and silicon dioxide for silicon nitride as an etch stop taught in Havemann to improve the similar device disclosed in Kuesters. Both Havemann and Kuesters are directed to improving semiconductor devices with self-aligned contacts, in one particular example, dRAM devices. *See* Kuesters at 1005.003 (describing a 4 Mbit dRAM cell with a 25% reduction in cell size, "achieved by a self aligned bitline contact"); Havemann at 1:23-25 (directed to the "fabrication of semiconductor devices and more particularly to the formation of self-aligned contacts on such devices"), 2:15-20 (the invention can be used "for enhancing a capacitive storage node (e.g. DRAM applications)…."). As described above, there may be benefits in substituting another material in place of silicon nitride. By substituting silicon oxynitride for silicon oxide in insulating layers and silicon dioxide for silicon nitride as an etch stop in Kuesters, a person of ordinary

skill in the art would only be applying a known technique to improve a similar device in the same way. Thus it would have been an obvious combination.

B. Kuesters in Combination with Heath

117. A person of ordinary skill in the art would have been motivated to combine Kuesters with the teachings of Heath to omit an oxide liner layer for several reasons.

118. First, both Kuesters and Heath are directed to similar methods to create the same types of structures in the same field. *Compare* Kuesters at 1005.003 (describing a 4 Mbit dRAM cell with a 25% reduction in cell size, "achieved by a self aligned bitline contact") *with* Heath at Abstract (directed to an "improved process for self-aligned contact window formation in an integrated circuit") and 6:35-36 (the invention "is especially useful in fabricating CMOS RAMS which are 256K or larger."). Furthermore, the structures of Kuesters and Heath are extremely similar and would have been compatible. *Compare* Kuesters at Figures 2 and 4a *with* Heath at Figure 8C. A person of ordinary skill in the art would have been motivated to combine compatible teachings of references that are addressing the same problems in a similar and compatible way to create the same types of devices with the same characteristics.

119. Furthermore, it would have been obvious to one skilled in the art to apply the known technique of fabricating a self-aligned contact taught in Heath to

improve the similar device disclosed in Kuesters. Both Heath and Kuesters are directed to improving semiconductor devices with self-aligned contacts, in one particular example, dRAM devices. *See* Kuesters at 1005.003 (describing a 4 Mbit dRAM cell with a 25% reduction in cell size, "achieved by a self aligned bitline contact"); Heath at Abstract (directed to an "improved process for self-aligned contact window formation in an integrated circuit") and 6:35-36 (the invention "is especially useful in fabricating CMOS RAMS which are 256K or larger."). The technique taught in Heath produces a structure similar to that of Kuesters (*compare* Kuesters at Figure 2 *with* Heath at Figure 8C) while simplifying the process by omitting the extra thin oxide liner layer employed in Kuesters. Kuesters uses a thin oxide liner layer that protects the silicon substrate from the nitride etch stop and which adds to the thickness of the oxide on top of the poly gate, and the insulating spacer. Heath deposits an oxide liner 24 such that "[i]t is relatively thin over the source drain 20 as shown at 24*a*, but is relatively thick on top of gate electrode 16, as shown at 24*b*." Heath at 9:53-55. Notably the structure in Heath does not overlay the thin oxide 24*a* over the insulating spacer. Heath expressly states that the inventive process is intended to work with an oxide sidewall spacer, as employed by Kuesters. *Id.* at 5:2-6. The technique taught by Heath is able to work with an oxide sidewall spacer, while not using an additional thin oxide liner layer overlaying the insulating spacer, by retaining a thin oxide layer across the

source/drain region to protect the silicon substrate from the nitride etch stop layer. *Id.* at 9:52-55. Using the fabrication method of Heath would, for example, reduce the size of the oxide insulating layer on top of the poly gate as well as the size of the insulating spacer. Furthermore, this improvement might reduce the fabrication time of the process disclosed in Kuesters. Moreover, a person of ordinary skill in the art would know that a thin silicon nitride layer could come in direct contact with the silicon substrate without adverse effects. *See* SAMSUNG-1012, Mehrdad M. Moslehi et al., *Thermal Nitridation of Si and SiO_2 for VLSI*, Vol. SC-20 IEEE Journal of Solid-State Circuits No. 1, 26 (1985) at 1012.001. By applying this technique to the structure in Kuesters, a person of ordinary skill in the art would only be applying a known technique to improve a similar device in the same way.

120. Additionally, it would have been an obvious design decision to employ the process of Heath in fabricating the dRAM cell of Kuesters. As discussed above, the structures of Kuesters and Heath are extremely similar and would have been compatible. *Compare* Kuesters at Figure 2 *with* Heath at Figure 8C. Moreover, both Heath and Kuesters use similar and compatible etch processes to fabricate these structures. *Compare* Kuesters at 1005.005 (describing a two-step etch process using a wet etch of NH_4F/HF followed by an anisotropic dry etch of CHF_3/O_2) *with* Heath at 9:6-20 (describing a two-step etch process using a combination dry and wet etch of hydrofluoric acid followed by an anisotropic dry

etch using O_2 and CHF_3). As both Kuesters and Heath use compatible fabrication processes to produce extremely similar and compatible devices, it would have been a simple and obvious design choice to employ the process of Heath in fabricating the structure of Kuesters. Again, this simply would omit a layer and reduce the fabrication time of the process disclosed in Kuesters. It would have been understood as a design choice and a tradeoff with respect to fabrication time. Thus it would have been an obvious combination.

C. Kuesters in Combination with Heath and Havemann

121. A person of ordinary skill in the art would have been motivated to combine Kuesters with the etch stop deposition teachings of Heath and the alternative materials teachings of Havemann for several reasons.

122. I identified the reasons for combining Kuesters with both Heath and Havemann above. For the same reasons, a person of ordinary skill in the art would have been motivated to combine Kuesters with both Heath and Havemann.

123. Additionally, Heath expressly states that the disclosed invention provides "a self-aligned contact process which is independent of gate dielectric type." Heath at 4:60-62. Therefore, Heath expressly contemplated combination with the teachings of Havemann of using different dielectric or insulating materials. Thus it would have been an obvious combination.

X. GROUNDS OF INVALIDITY

124. I detail how the prior art invalidates the claims at issue in the Appendix A claim chart. In summary, my opinions are as follows:

125. Ground 1: It is my opinion that claims 1, 2, and 4-12 are invalid as anticipated by Kuesters.

126. Ground 2: It is my opinion that claim 3 is invalid as obvious over Kuesters in view of Havemann.

127. Ground 3: It is my opinion that claims 1, 2, and 4-7 are invalid as obvious over Kuesters in view of Heath.

128. Ground 4: It is my opinion that claim 3 is invalid as obvious over Kuesters in view of Heath and Havemann.

XI. DECLARATION IN LIEU OF OATH

129. I understand that willful false statements and the like are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and may jeopardize the validity of the application or any patent issuing thereon. I declare that all statements made of my knowledge are true, and that all statements made on information and belief are believed to be true.

Richard B. Fair

Date: March 18, 2016

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GROUND #1: CLAIMS 1, 2, AND 4-12 ARE ANTICIPATED BY KUESTERS

'552 Patent Language	Kuesters
Claim 1	
[1.0] A structure, comprising:	Kuesters discloses a structure. SAMSUNG-1005, Kuesters at 1005.003 (a "4 Mbit dRAM cell size is achieved by a self aligned bitline contact, which is fully overlapping gate and field oxide (FOBIC)."). For example, Kuesters discloses "a trench capacitor cell with self aligned, fully overlapping bitline contact (FOBIC). The cell design allows the contact hole to overlap gate and field oxide; the contact area is independent [sic] of lithographic alignment tolerances." *Id*. at 640. "The 4 Mbit dRAM is fabricated with a 0.9 μm twin well process. After trench capacitor and LDD transistor formation a low resistivity polycide (poly Si/$TaSi_2$) layer is used for bitlines and local peripheral interconnects. The second interconnect level consists of Ti/TiN/AlSi metallization. For contacts connection the polycide bitline to n+ diffusion (source/drain of transfer gates) the FOBIC process (fig. 2) is employed." *Id.* at 1005.004. Figure 2 is a drawing disclosing the structure of the 4Mbit dRAM FOBIC contact in accordance with the etching methods disclosed in Section 2.2.1(b):

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	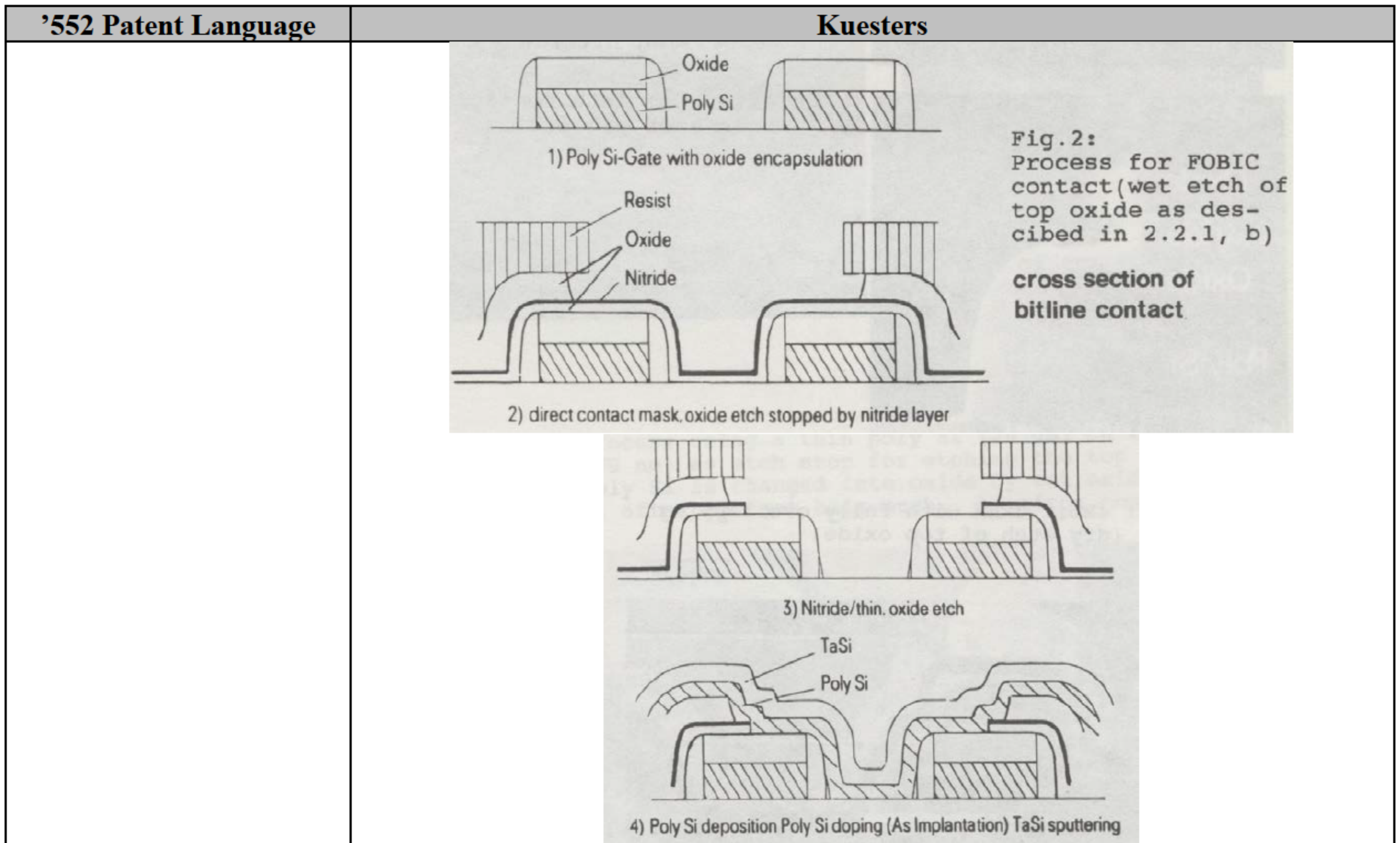

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’552 Patent Language	Kuesters
	SAMSUNG-1005, Kuesters at Figure 2 Figure 4a is a SEM image disclosing the structure of the 4Mbit dRAM FOBIC contact in accordance with the etching methods disclosed in Section 2.2.1(b): **SAMSUNG-1005, Kuesters at Figure 4a** Thus, by disclosing the 4 Mbit dRAM structure, Kuesters discloses a structure.
[1.1] (a) a conductive layer disposed over a substrate;	Kuesters discloses a conductive layer disposed over a substrate. Kuesters at 1005.004 (disclosing a “new technique for etching the dielectric underneath the bitline is used **to ensure a good insulation of bitline to polysilicon gates (wordline) and substrate** for the overlapping contacts.” (emphasis added)). Polysilicon was well known as a conductive material at the time of the filing of the 552 Patent.

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	The substrate is shown annotated in light green in Figure 2 and dark green in Figure 4a below. The conductive gate layer is shown annotated in purple in Figures 2 and 4a below.

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	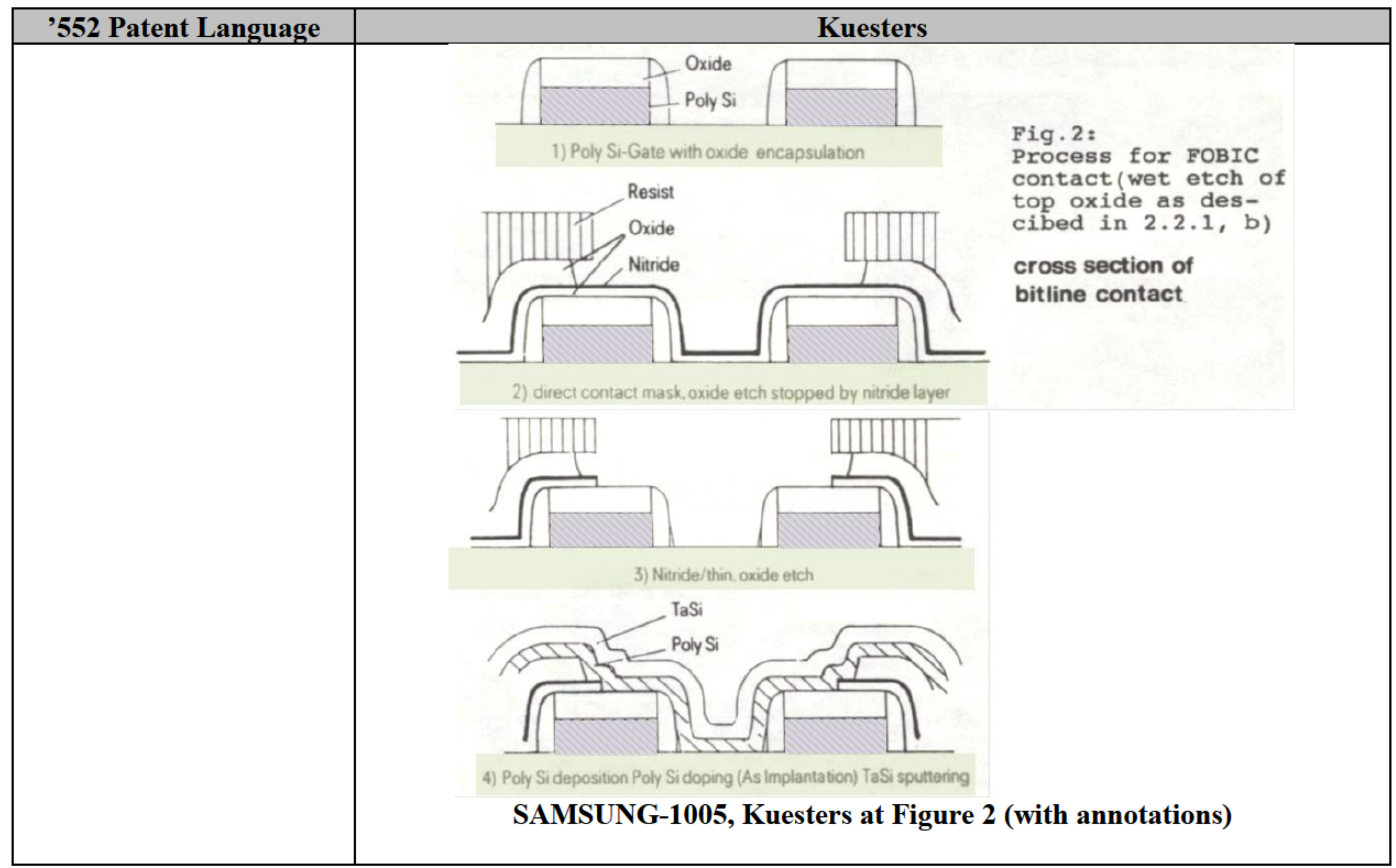 **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)**

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'552 Patent Language	Kuesters
	SAMSUNG-1005, Kuesters at Figure 4a (with annotations) The conductive gate layer is labeled "Poly Si" in Figure 2-1 and labeled "poly" in Figure 4a. Thus, by disclosing a polysilicon gate deposited over the substrate, Kuesters discloses a conductive layer disposed over a substrate
[1.2] (b) a first insulating layer on the conductive layer;	Kuesters discloses a first insulating layer on the conductive layer. Kuesters at 1005.003 (disclosing that the "gate is encapsulated by oxide using an oxide spacer technique."). For example, Kuesters discloses that "[t]he triple layer dielectric allows a contact hole etch, which does not significantly affect the field oxide **and the oxide insulation of the gate (see fig. 2)**." *Id.* at 1005.004 (emphasis added). Kuesters expressly discloses how to encapsulate the gate with an insulating layer: **"2.1 Oxide encapsulation of the gate**

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	After patterning a double layer of poly Si/oxide (0.3 µm TEOS) an oxide spacer is formed by oxide deposition (TEOS) and RIE etching ($CHF_3/0_2$). The spacer width (0.2 µm) is determined by LDD transistor optimization. The poly gate is insulated by at least 0.15 µm oxide. A vertical etch profile of poly Si/oxide which can be achieved by sequential oxide etch ($CHF_3/0_2$) and poly Si etch (Cl_2/He) is essential. The same technique for oxide encapsulation of the gate has also been applied to a polycide gate with an oxide spacer covering the sidewalls of a triple layer of poly Si/$TaSi_2$/oxide." *Id.* at 1005.004, *see also id.* at 1005.005 ("After completing the process (see fig. 3c,4b,4c) **an oxide insulation of the gate > 120 nm is obtained**, the field oxide thinning in the contact hole is at most 50 nm.") The oxide insulating layer is shown on the conductive gate layer as annotated in light orange in Figures 2 and 4a below.

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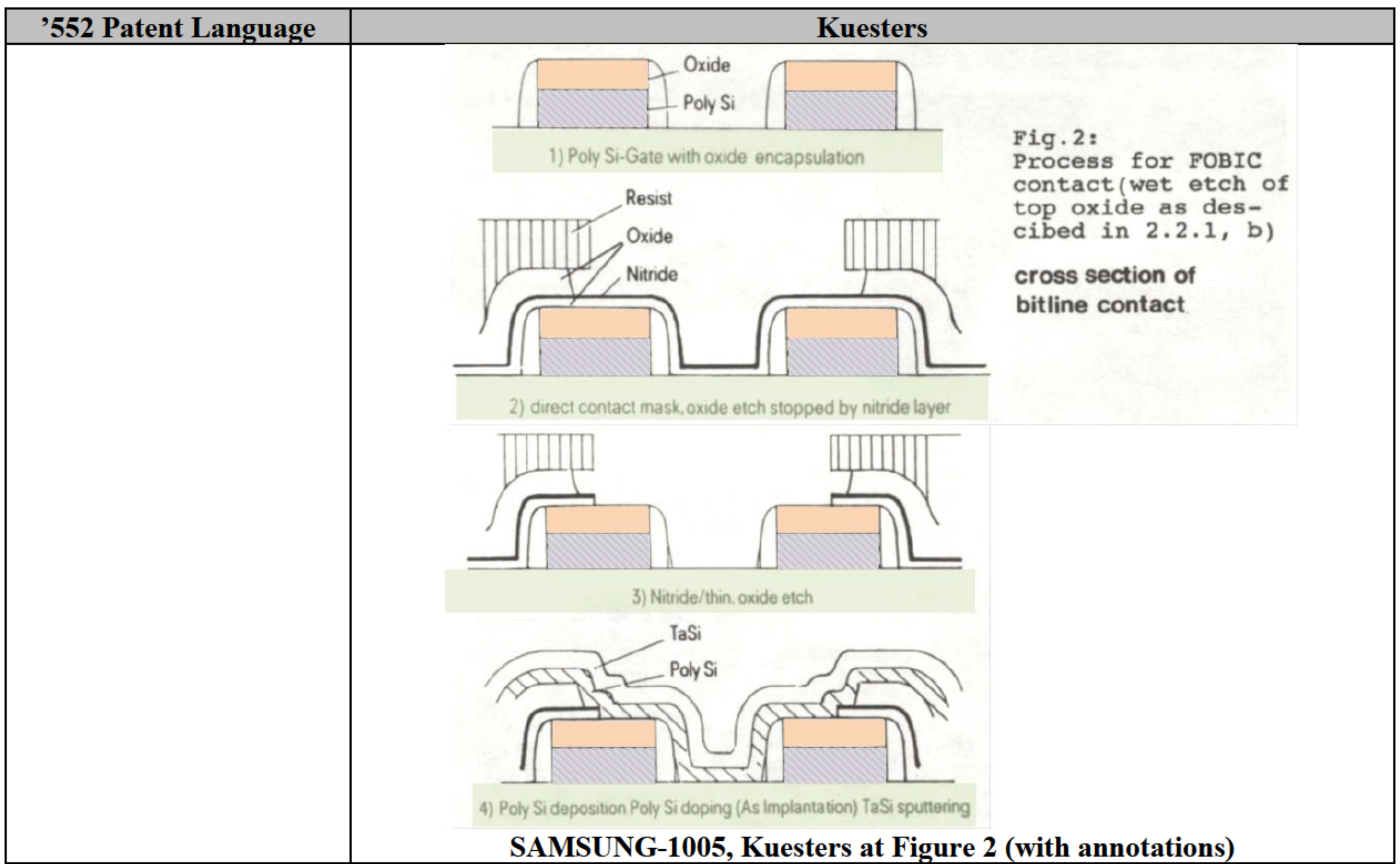
'552 Patent Language	Kuesters
	 **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)**

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	resist nitride= oxide poly 0.5 µm Fig.4a: After complete contact hole etch process (wet etch of top oxide) **SAMSUNG-1005, Kuesters at Figure 4a (with annotations)** The first insulating layer is labeled "Oxide" in Figure 2-1 and "oxide" in Figure 4a. Thus, by disclosing an oxide insulating layer encapsulating the gate layer, Kuesters discloses a first insulating layer on the conductive layer.
[1.3] (c) a contact region in said first insulating layer;	Kuesters discloses a contact region in said first insulating layer. Kuesters at 1005.003 (disclosing that a "thin oxide/nitride/oxide dielectric allows **a contact hole etch**, which does not significantly affect the oxide insulation of the gate and the field oxide." (emphasis added)). For example, Kuesters discloses that the design of the semiconductor structure "allows **the contact hole** to overlap gate and field oxide; [and thus] the contact area is independant [sic] of lithographic alignment tolerances." *Id.* (emphasis added).

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	Furthermore, Kuesters expressly teaches how to etch the contact hole: "**2.2.1 Contact hole etch** The dielectric under the bitline consists of a triple layer of thin oxide/nitride/oxide. For the top oxide a reflow technique (PH_3-diffusion and backetch of the doped oxide) is employed, with a final thickness of 0.2/um. **The triple layer dielectric allows a contact hole etch**, which does not significantly affect the field oxide and the oxide insulation of the gate (see fig. 2). After patterning the contact hole mask the top oxide is etched using the nitride as an etch stop. The oxide etch can be performed a) by dry etching, b) by wet etching, or a combination of both." *Id.* at 1005.004 (emphasis added), *see also id.* at 1005.005 ("After removing the polymer film by Ar plasma, **the contact hole etch continues with etching the nitride** (SF_6 Plasma, fig. 3b) selecti-vely [sic] to the underlying oxide (= 50 nm)." (emphasis added)), *id.* at 1005.005 ("The use of a wet etch step seems also preferable because of a tapering of the contact hole edge. If any conventional contacts are patterned by the same mask and technique, the contact hole size is not affected by a wet etch step for the top oxide as the underlying nitride/oxide is etched anisotropically."), *id.* ("After completing the process (see fig. 3c,4b,4c) an oxide insulation of the gate > 120 nm is obtained, the field oxide thinning in the contact hole is at most 50 nm. **The contact area of the FOBIC contact is defined by gate and field oxide edges.**" (emphasis added)). The contact region is shown annotated in light blue and labeled in Figures 2 and 4a below.

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	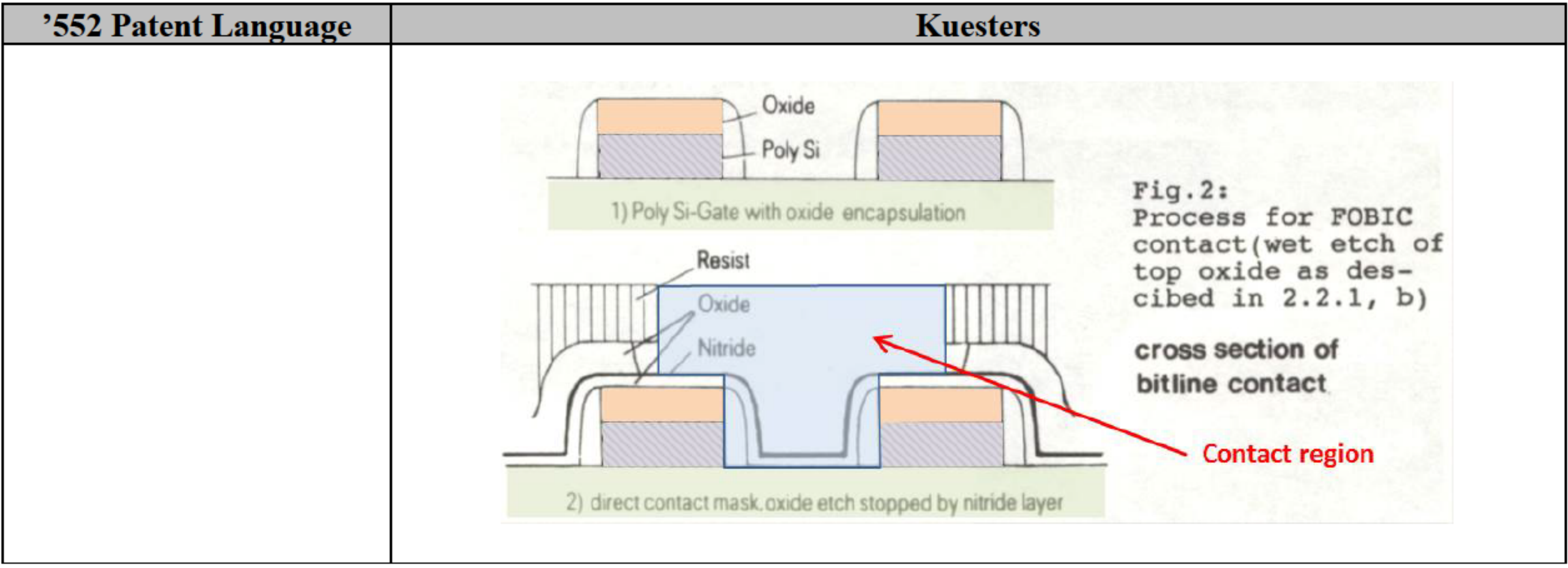

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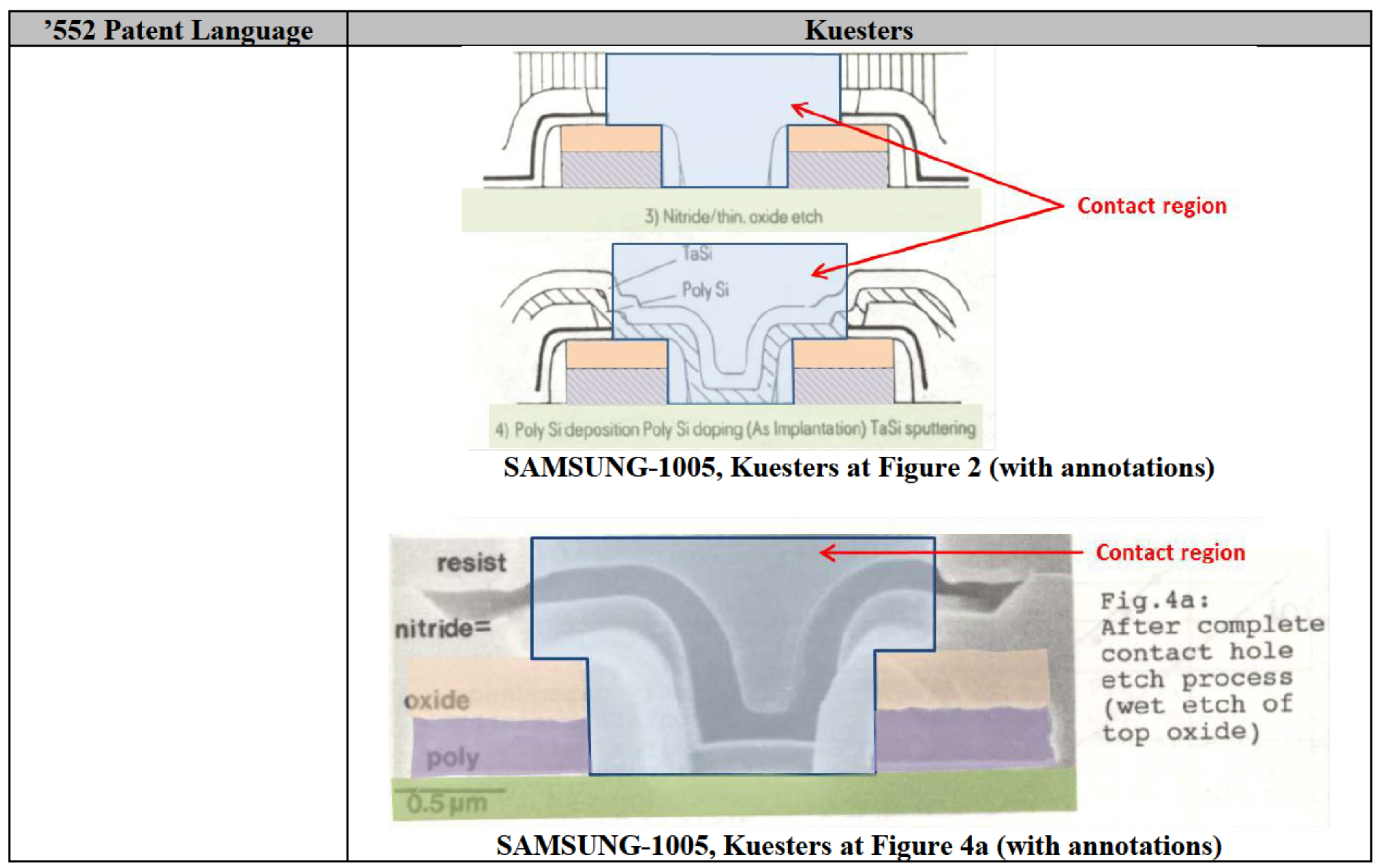
'552 Patent Language	Kuesters
	 **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)** **SAMSUNG-1005, Kuesters at Figure 4a (with annotations)**

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	Thus, by disclosing a contact hole or contact area extending through the oxide encapsulation, Kuesters discloses a contact region in said first insulating layer.
[1.4] (d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and	Kuesters discloses at least one insulating spacer in the contact region adjacent to the first insulating layer. Kuesters at 1005.003 (disclosing that the "gate is encapsulated by oxide using **an oxide spacer technique**." (emphasis added)). For example, Kuesters discloses that "an oxide spacer technique is used because of LDD transistor reliability." *Id.* at 1005.004. In disclosing the method for oxide encapsulation of the gate layer, Kuesters discloses an oxide spacer adjacent to the oxide layer and in the contact region: **"2.1 Oxide encapsulation of the gate** After patterning a double layer of poly Si/oxide (0.3 µm TEOS) an oxide spacer is formed by oxide deposition (TEOS) and RIE etching ($CHF_3/0_2$). The spacer width (0.2 µm) is determined by LDD transistor optimization. The poly gate is insulated by at least 0.15 µm oxide. A vertical etch profile of poly Si/oxide which can be achieved by sequential oxide etch ($CHF_3/0_2$) and poly Si etch (Cl_2/He) is essential. **The same technique for oxide encapsulation of the gate has also been applied to a polycide gate with an oxide spacer** covering the sidewalls of a triple layer of poly Si/$TaSi_2$/oxide." *Id.* at 1005.004 (emphasis added).

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	The oxide liner layer deposited along with the nitride etch stop material is part of the insulating spacer as described in Section VIII(A) above. The oxide spacer is shown annotated in bright green in Figure 2 below.

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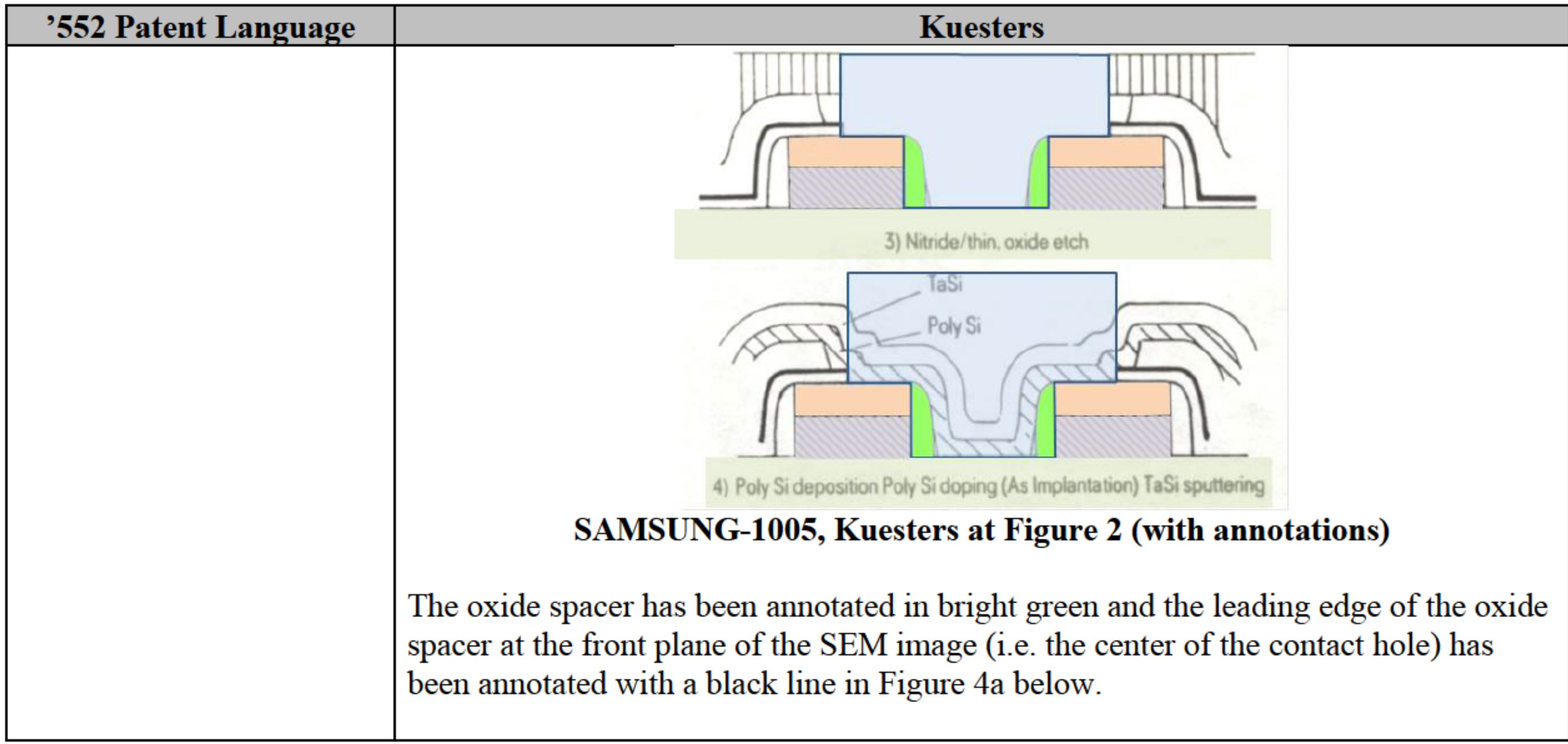
'552 Patent Language	Kuesters
	 **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)** The oxide spacer has been annotated in bright green and the leading edge of the oxide spacer at the front plane of the SEM image (i.e. the center of the contact hole) has been annotated with a black line in Figure 4a below.

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	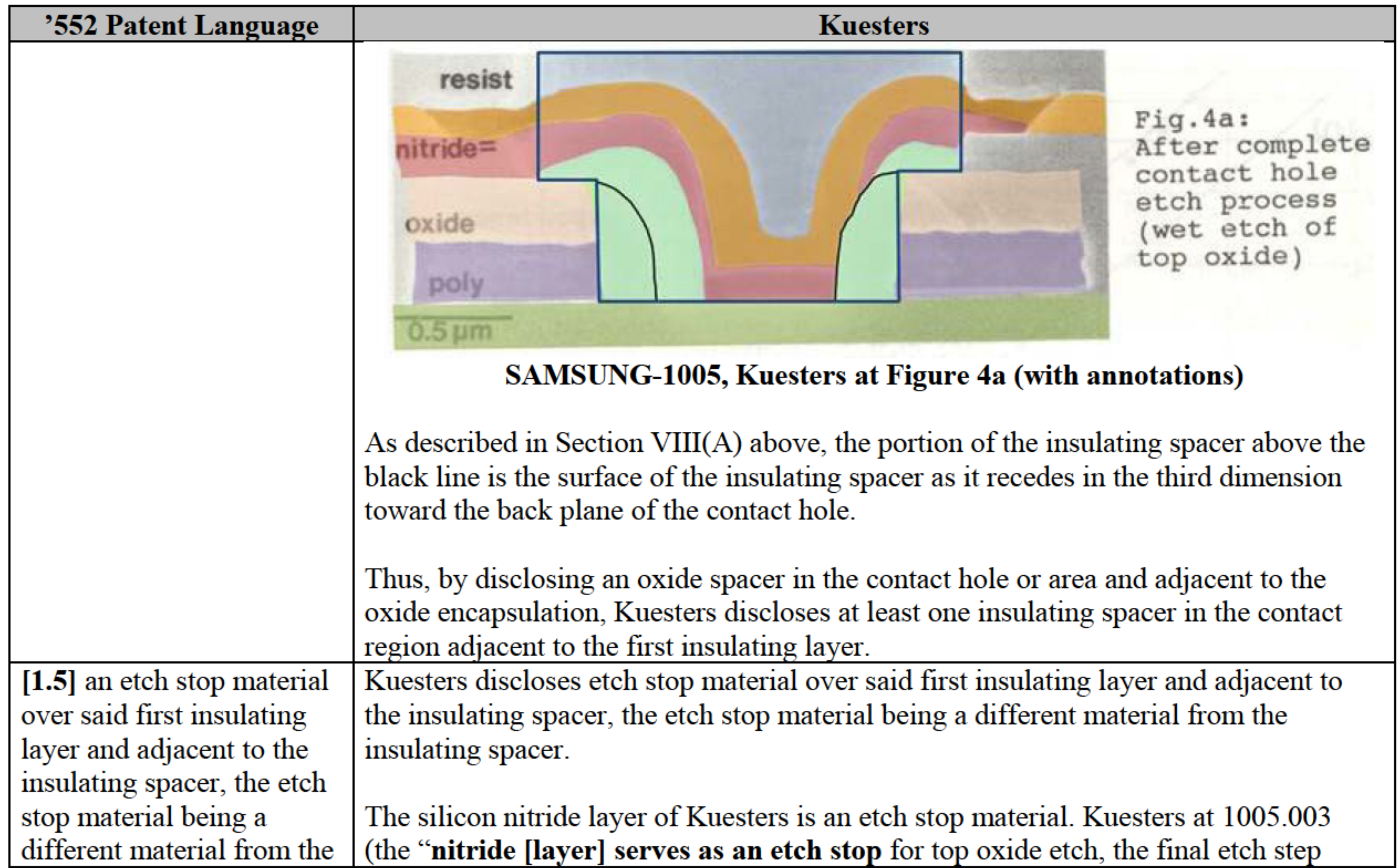 **SAMSUNG-1005, Kuesters at Figure 4a (with annotations)** As described in Section VIII(A) above, the portion of the insulating spacer above the black line is the surface of the insulating spacer as it recedes in the third dimension toward the back plane of the contact hole. Thus, by disclosing an oxide spacer in the contact hole or area and adjacent to the oxide encapsulation, Kuesters discloses at least one insulating spacer in the contact region adjacent to the first insulating layer.
[1.5] an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the	Kuesters discloses etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer. The silicon nitride layer of Kuesters is an etch stop material. Kuesters at 1005.003 (the "**nitride [layer] serves as an etch stop** for top oxide etch, the final etch step

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insulating spacer,	removes only a thin dielectric." (emphasis added)). Furthermore, Kuesters expressly describes the silicon nitride layer as an etch stop layer in discussing the contact region etch processes: "**2.2.1 Contact hole etch** The dielectric under the bitline consists of a triple layer of thin oxide/nitride/oxide. For the top oxide a reflow technique (PH_3-diffusion and backetch of the doped oxide) is employed, with a final thickness of 0.2/um. The triple layer dielectric allows a contact hole etch, which does not significantly affect the field oxide and the oxide insulation of the gate (see fig. 2). After patterning **the contact hole mask the top oxide is etched using the nitride as an etch stop**. The oxide etch can be performed a) by dry etching, b) by wet etching, or a combination of both." *Id.* at 1005.004 (emphasis added). "a) For dry etching a CHF_3 plasma with a selectivity of 4:1 with respect to the nitride is used (fig. 3a). During overetch the nitride etch rate reduces due to an enhanced development of a C rich polymer film on the nitride. The overetch time has to be sufficient (> 70 %) to remove oxide spacers on the nitride. **Therefore a nitride thickness > 70 nm is required as an etch stop.**" *Id.* at 1005.005 (emphasis added). "b) If the top oxide is wet etched (NH_4F/HF), **a nitride layer of > l0nm is sufficient for the etch stop.** The thin nitride and the thin oxide (= 50 nm)

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	underneath are etched by the same CHF_3/O_2 dry etch step (fig. 4a). The use of a rather thin nitride as an etch stop is also possible if combining a dry etch of the top oxide (without long overetch) and a wet etch to remove oxide spacers on the nitride." *Id.* at 1005.005 (emphasis added). The silicon nitride etch stop layer is clearly disclosed as over the oxide encapsulation layer and adjacent to the oxide spacer in the figures and images of Kuesters. The nitride etch stop material is shown annotated in red in Figures 2 and 4a below. Resist Oxide Nitride 2) direct contact mask, oxide etch stopped by nitride layer

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	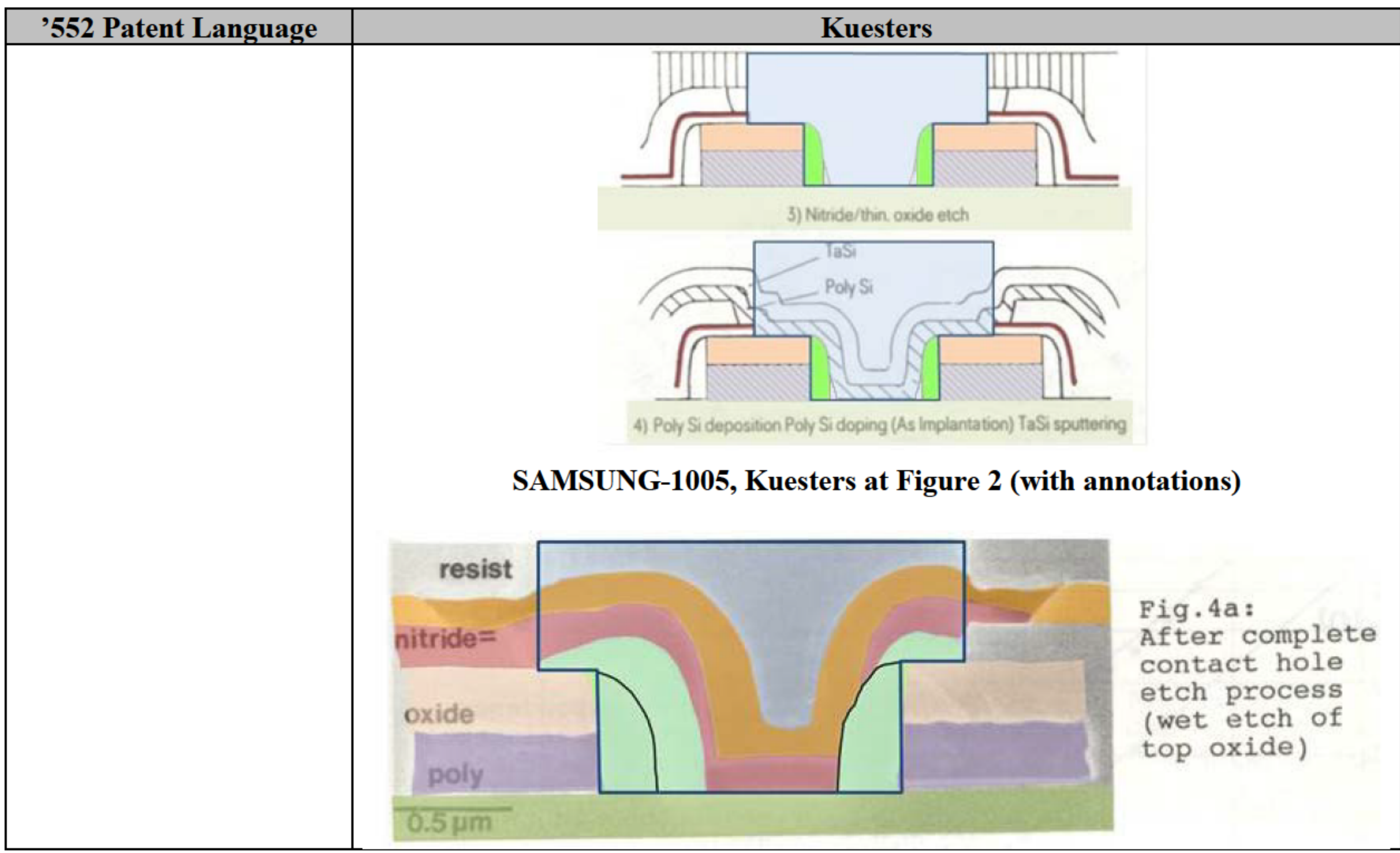 **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)**

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	SAMSUNG-1005, Kuesters at Figure 4a (with annotations) The nitride etch stop material is labeled "Nitride" in Figure 2-2 and "nitride" in Figure 4a. Figure 4 shows the nitride adjacent to the oxide spacer and extending across the center of the contact hole in a darker grey coloring. A person of ordinary skill in the art would understand that this darker coloring indicates that this nitride layer is set further back in the plane of the SEM image relative to the oxide encapsulation and oxide spacer. This indicates that the nitride layer is adjacent to the oxide only along the back plane of the contact hole and not in the center of the contact hole. Thus, by disclosing a silicon nitride etch stop layer that is over the oxide insulation layer and adjacent to the silicon oxide spacer, Kuesters discloses an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer.
[1.6] wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.	Kuesters discloses a side of the insulating spacer having an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°. The SEM images of Kuesters disclose that an actual angle achieved between a side of the oxide spacer and the surface of the substrate is 86 to 87°. I have measured this angle and found it to be within 86 to 87° relative to the substrate surface. The angle is annotated in Figure 4a below.

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	SAMSUNG-1005, Kuesters at Figure 4a (with annotations) Thus, by disclosing a side of an oxide spacer with a measurable angle relative to the substrate surface of 86-87°, Kuesters discloses a side of the insulating spacer with an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.
Claim 2	
[2.0] The semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon nitride.	*See* Claim 1 above. Kuesters discloses the semiconductor apparatus of claim 1 wherein the etch stop material comprises silicon nitride. Kuesters at 1005.003 (the "nitride serves as an etch stop for top oxide etch, the final etch step removes only a thin dielectric."). Furthermore, Kuesters expressly describes the etch stop material as silicon nitride in

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	discussing the contact region etch processes: "**2.2.1 Contact hole etch** The dielectric under the bitline consists of a triple layer of thin oxide/nitride/oxide. For the top oxide a reflow technique (PH_3-diffusion and backetch of the doped oxide) is employed, with a final thickness of 0.2/um. The triple layer dielectric allows a contact hole etch, which does not significantly affect the field oxide and the oxide insulation of the gate (see fig. 2). After patterning **the contact hole mask the top oxide is etched using the nitride as an etch stop**. The oxide etch can be performed a) by dry etching, b) by wet etching, or a combination of both." *Id.* at 1005.004 (emphasis added). "a) For dry etching a CHF_3 plasma with a selectivity of 4:1 with respect to the nitride is used (fig. 3a). During overetch the nitride etch rate reduces due to an enhanced development of a C rich polymer film on the nitride. The overetch time has to be sufficient (> 70 %) to remove oxide spacers on the nitride. **Therefore a nitride thickness > 70 nm is required as an etch stop.**" *Id.* at 1005.005 (emphasis added). "b) If the top oxide is wet etched (NH_4F/HF), **a nitride layer of > l0nm is sufficient for the etch stop.** The thin nitride and the thin oxide (= 50 nm) underneath are etched by the same $CHF_3/0_2$ dry etch step (fig. 4a). The use of a rather thin nitride as an etch stop is also possible if combining a dry etch of the top oxide (without long overetch) and a wet etch to remove oxide spacers on

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	the nitride." *Id.* at 1005.005 (emphasis added). Thus, by disclosing that the etch stop material is silicon nitride, Kuesters discloses the semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon nitride.
Claim 4	
[4.0] The structure of claim 1, wherein the insulating spacer has a surface portion in the contact region without overlying etch stop material.	*See* Claim 1 above. Kuesters discloses the structure of claim 1, wherein the insulating spacer has a surface portion in the contact region without overlying etch stop material. Kuesters illustrates in Figure 2 and the SEM image of Figure 4, that the oxide spacer has a surface portion in the contact region without an overlying nitride layer. The surface portion of the oxide spacer without an overlying nitride layer is annotated with a blue circle in Figures 2 and 4a below.

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	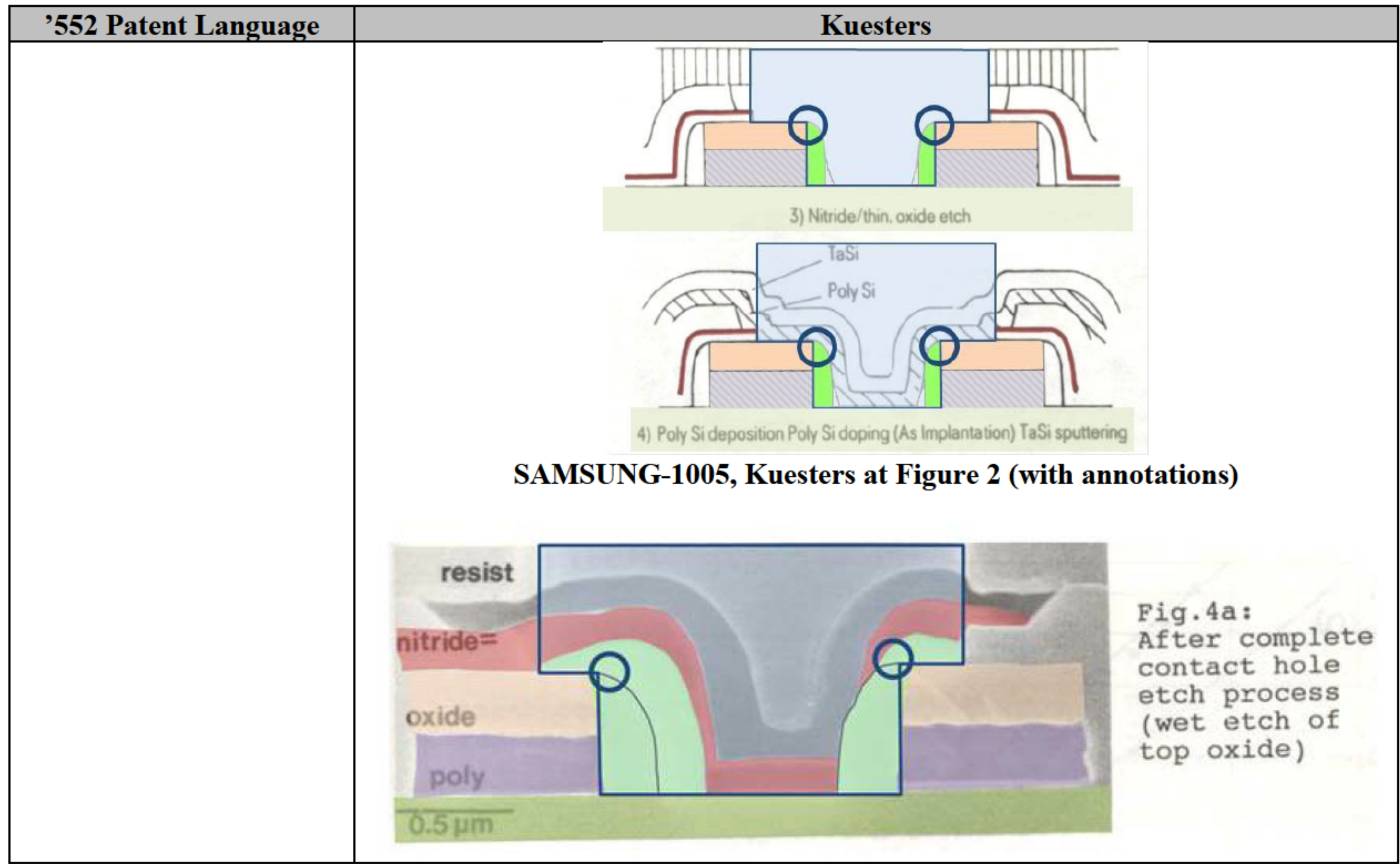 **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)**

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	SAMSUNG-1005, Kuesters at Figure 4a (with annotations) As explained in section [1.5] above, annotated Figure 4a shows the nitride etch stop material (annotated in red and labeled "nitride" in Figure 4a) adjacent to the oxide insulating spacer (bright green) and extending across the center of the contact hole at the back plane of the contact hole. This indicates that the nitride etch stop layer is adjacent to the oxide insulating spacer only along the back plane of the contact hole and not in the center of the contact hole. Thus the surface area at the top edge of the oxide spacer in the contact hole does not have an overlying nitride etch stop layer. This is consistent with the corresponding drawings of Figures 2-3 and 2-4. Thus, by disclosing that the oxide spacer has a surface portion in the contact hole or area without an overlying nitride layer, Kuesters discloses the structure of claim 1, wherein the insulating spacer has a surface portion in the contact region without overlying etch stop material.
Claim 5	
[5.0] The structure of claim 4, wherein the insulating spacer surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said	*See* Claim 4 above. Kuesters discloses the structure of claim 4, wherein the insulating spacer surface portion without overlying etch stop material is the insulating spacer surface portion most distant from said substrate. Kuesters illustrates in Figures 2 and 4a, that there is a surface portion of the oxide spacer in the contact region without an overlying nitride layer is the portion most

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substrate.	distant from the substrate. The surface portion of the oxide spacer without an overlying nitride layer is annotated with a blue circle in Figures 2 and 4a below. **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)**

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	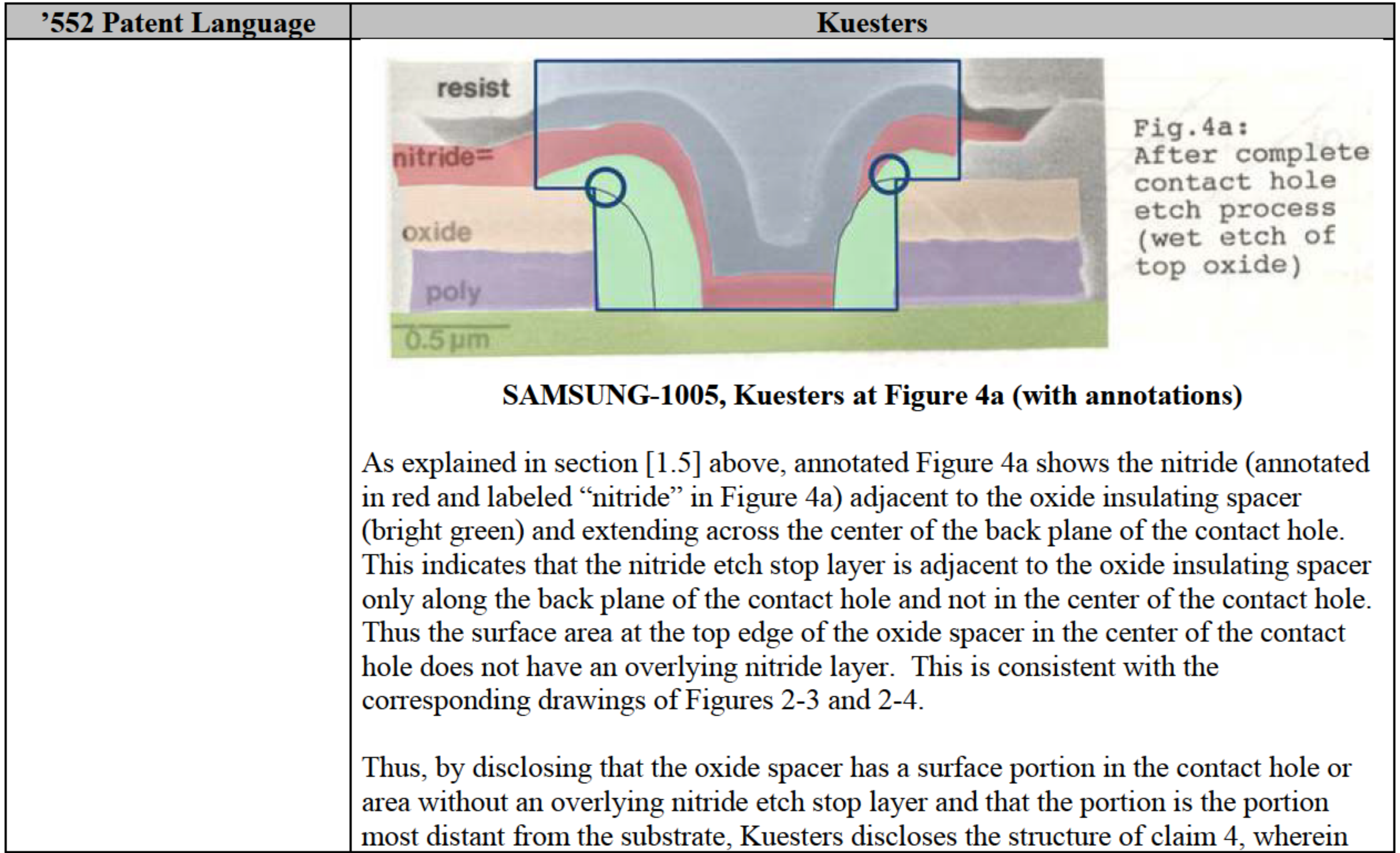 **SAMSUNG-1005, Kuesters at Figure 4a (with annotations)** As explained in section [1.5] above, annotated Figure 4a shows the nitride (annotated in red and labeled "nitride" in Figure 4a) adjacent to the oxide insulating spacer (bright green) and extending across the center of the back plane of the contact hole. This indicates that the nitride etch stop layer is adjacent to the oxide insulating spacer only along the back plane of the contact hole and not in the center of the contact hole. Thus the surface area at the top edge of the oxide spacer in the center of the contact hole does not have an overlying nitride layer. This is consistent with the corresponding drawings of Figures 2-3 and 2-4. Thus, by disclosing that the oxide spacer has a surface portion in the contact hole or area without an overlying nitride etch stop layer and that the portion is the portion most distant from the substrate, Kuesters discloses the structure of claim 4, wherein

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	the insulating spacer surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said substrate.
Claim 6	
[6.0] The structure of claim 1, further comprising a second insulating layer on the etch stop layer and over the conductive layer.	*See* Claim 1 above. Kuesters discloses the structure of claim 1, further comprising a second insulating layer on the etch stop layer and over the conductive layer. Kuesters at 1005.003 ("thin **oxide/nitride/oxide** dielectric allows a contact hole etch, which does not significantly affect the oxide insulation of the gate and the field oxide. The nitride serves as an etch stop for top oxide etch, the final etch step removes only a thin dielectric." (emphasis added)). For example, Kuesters discloses that the structure uses an oxide/nitride/oxide structure, wherein the oxides are a first and second insulating layer and the nitride serves as an etch stop: "**2.2.1 Contact hole etch** The dielectric under the bitline consists of **a triple layer of thin oxide/nitride/oxide**. For the top oxide a reflow technique (PH_3-diffusion and backetch of the doped oxide) is employed, with a final thickness of 0.2/um. The triple layer dielectric allows a contact hole etch, which does not significantly affect the field oxide and the oxide insulation of the gate (see fig. 2)." *Id.* at 1005.004 (emphasis added).

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	"b) If the **top oxide** is wet etched (NH_4F/HF), a nitride layer of > l0nm is sufficient for the etch stop. **The thin nitride and the thin oxide (= 50 nm) underneath** are etched by the same $CHF_3/0_2$ dry etch step (fig. 4a). The use of a rather thin nitride as an etch stop is also possible if combining a dry etch of the top oxide (without long overetch) and a wet etch to remove oxide spacers on the nitride." *Id.* at 1005.005 (emphasis added). The second oxide insulating layer is annotated in bright orange in Figures 2 and 4a below. **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)**

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	SAMSUNG-1005, Kuesters at Figure 4a (with annotations) The second insulating layer is labeled "Oxide" in Figure 2-2 and "oxide" in Figure 4a. Thus, by disclosing a second oxide layer atop the nitride etch stop layer, Kuesters discloses the structure of claim 1, further comprising a second insulating layer on the etch stop layer and over the conductive layer.
Claim 7	
[7.0] The structure of claim 6, further comprising a second conductive material in the contact region.	*See* Claim 6 above. Kuesters discloses the structure of claim 6, further comprising a second conductive material in the contact region. Kuesters at 1005.003 (a "0.9 µm **contact between polycide (TaSi) bitline** and n+ diffusion ($R_c < 50\Omega$), 0.2 µm distance to gate is realized without deterioration of transistor properties."). It was well known to a

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'552 Patent Language	Kuesters
	person of ordinary skill in the art in 1995 that a polycide (TaSi) bitline is a conductive material. For example, Kuesters discloses "**a low resistivity polycide (poly Si/$TaSi_2$) layer is used for bitlines and local peripheral interconnects**. The **second interconnect level consists of Ti/TiN/AlSi metallization**. For contacts connecting the polycide bitline to n+ diffusion (source/drain of transfer gates) the FOBIC process (fig. 2) is employed.") *Id.* at 1005.004 (emphasis added). Furthermore, Kuesters expressly discloses forming a conductive bitline in the contact hole: "**2.3 Polycide interconnect level** After contact hole etch the bitline is formed by $TaSi_2$ (200nm) on top of poly Si (100nm). Poly Si is doped by As or P Implantation." *Id.* at 1005.006. The conductive bitline layer in the contact hole is annotated in light brown in Figure 2 below. **SAMSUNG-1005, Kuesters at Figure 2-4 (with annotations)**

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'552 Patent Language	Kuesters
	The second conductive material is labeled "TaSi" and "Poly Si" in Figure 2-4. Thus, by disclosing a conductive bitline of polysilicon and TaSi in the contact hole, Kuesters discloses the structure of claim 6, further comprising a second conductive material in the contact region.
Claim 8	
[8.0] A structure, comprising:	Kuesters discloses a structure. *See* analysis for Ground 1, Claim [1.0].
[8.1] (a) a first electrically conductive material formed in and/or on a surface of a substrate;	Kuesters discloses a first electrically conductive material formed in and/or on a surface of a substrate. Kuesters at 1005.004 ("a low resistivity polycide (poly Si/$TaSi_2$) layer is used for bitlines and local peripheral interconnects. . . . For contacts connecting the polycide bitline to n+ diffusion (source/drain of transfer gates) the FOBIC process (fig 2.) is employed."). It would have been well known to a person of ordinary skill in the art as of 1995 that n+ diffusion regions, which make up the source and drain of the transfer gates, are electrically conductive regions in the surface of the substrate. The electrically conductive n+ diffusion regions are identified in Figures 2 and 4 below.

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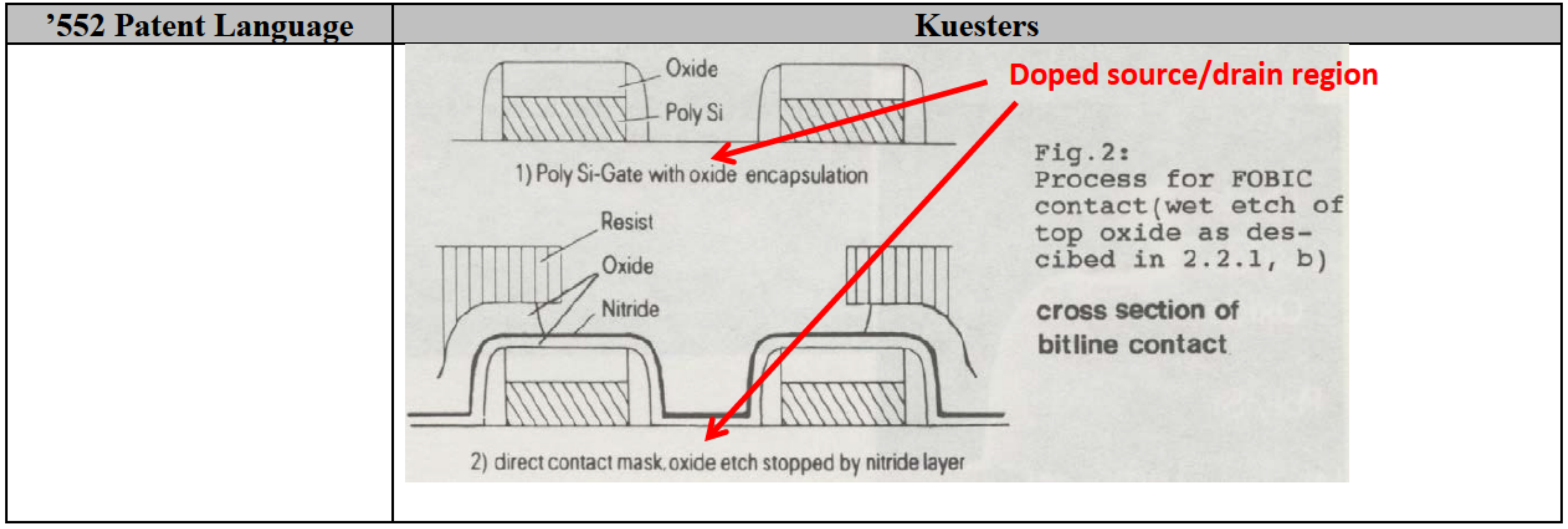
’552 Patent Language	Kuesters
	

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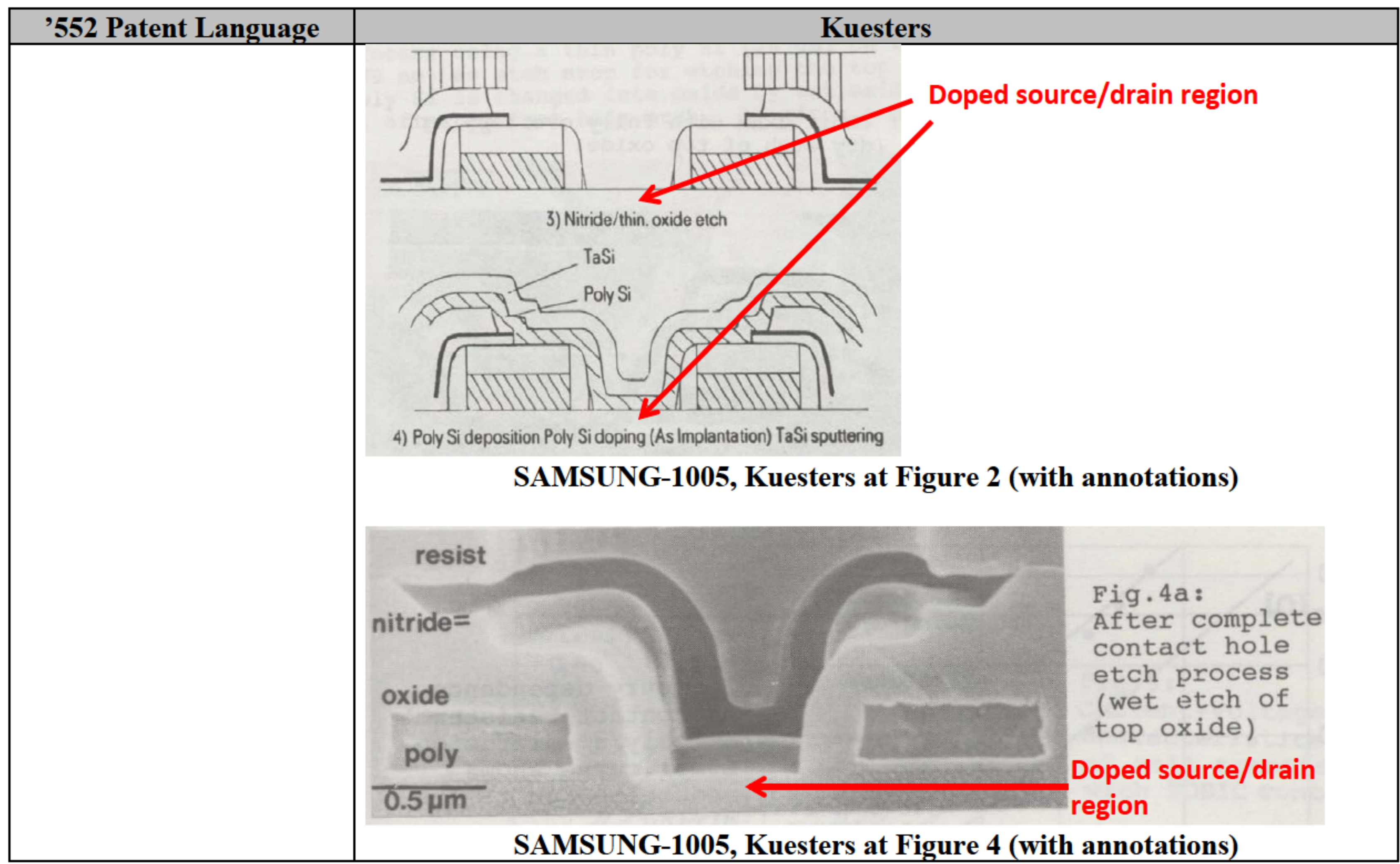
’552 Patent Language	Kuesters
	 **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)** **SAMSUNG-1005, Kuesters at Figure 4 (with annotations)**

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'552 Patent Language	Kuesters
	Thus, by disclosing a conductive n+ diffusion region constituting the source or drain region in the substrate, Kuesters discloses a first electrically conductive material formed in and/or on a surface of a substrate.
[8.2] (b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate;	Kuesters discloses a contact opening in a region adjacent to a second electrically conductive material formed on the substrate. *See* analysis for Ground 1, Claim [1.3]. This element differs with respect to claim element [1.3] only in that it refers to a "second electrically conductive material" instead of a "conductive layer," and that the contact opening must be adjacent to the second electrically conductive material. As annotated in light blue in Figures 2 and 4a below, the contact area is adjacent to the purple electrically conductive gate material.

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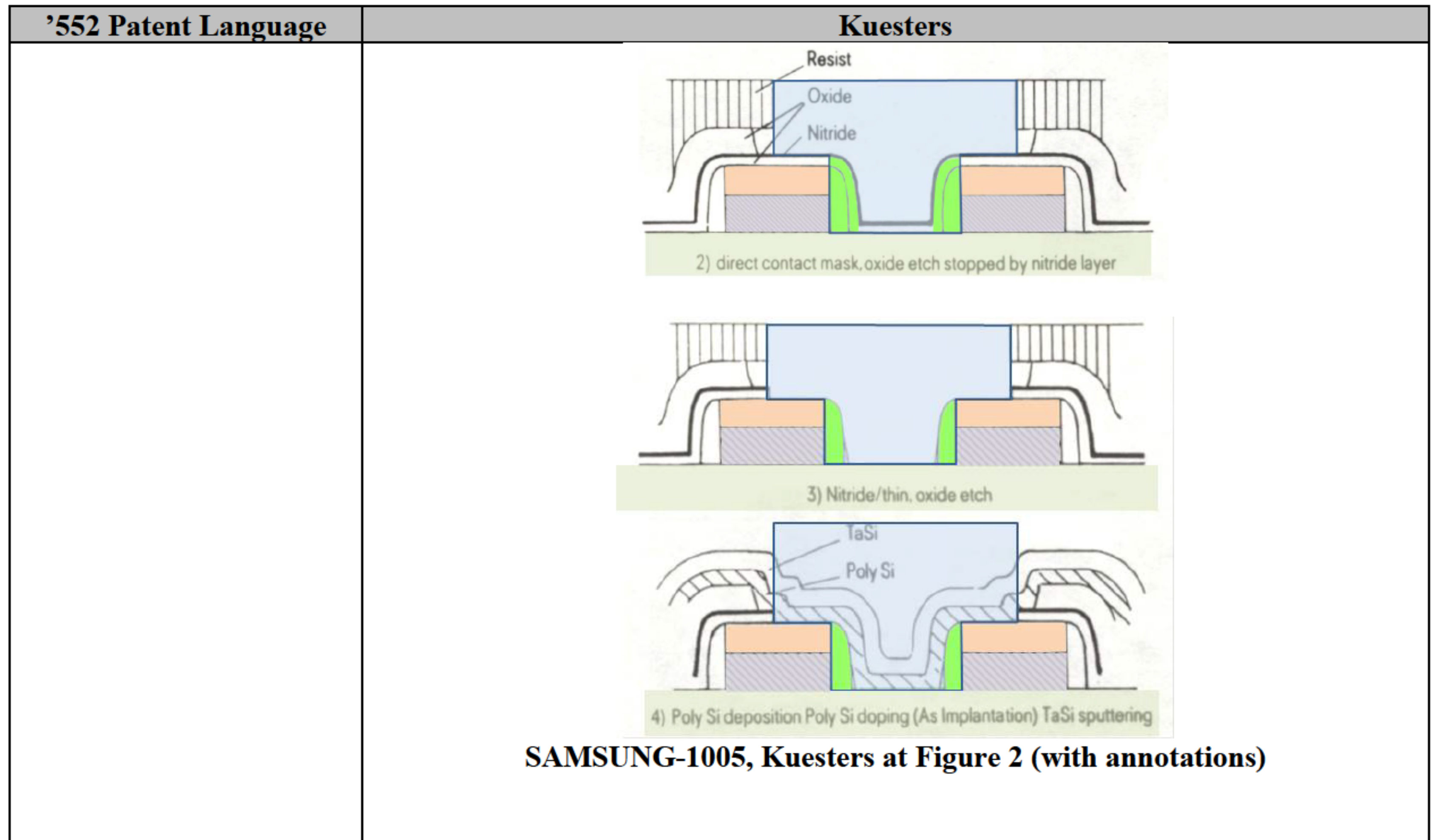
'552 Patent Language	Kuesters
	 **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)**

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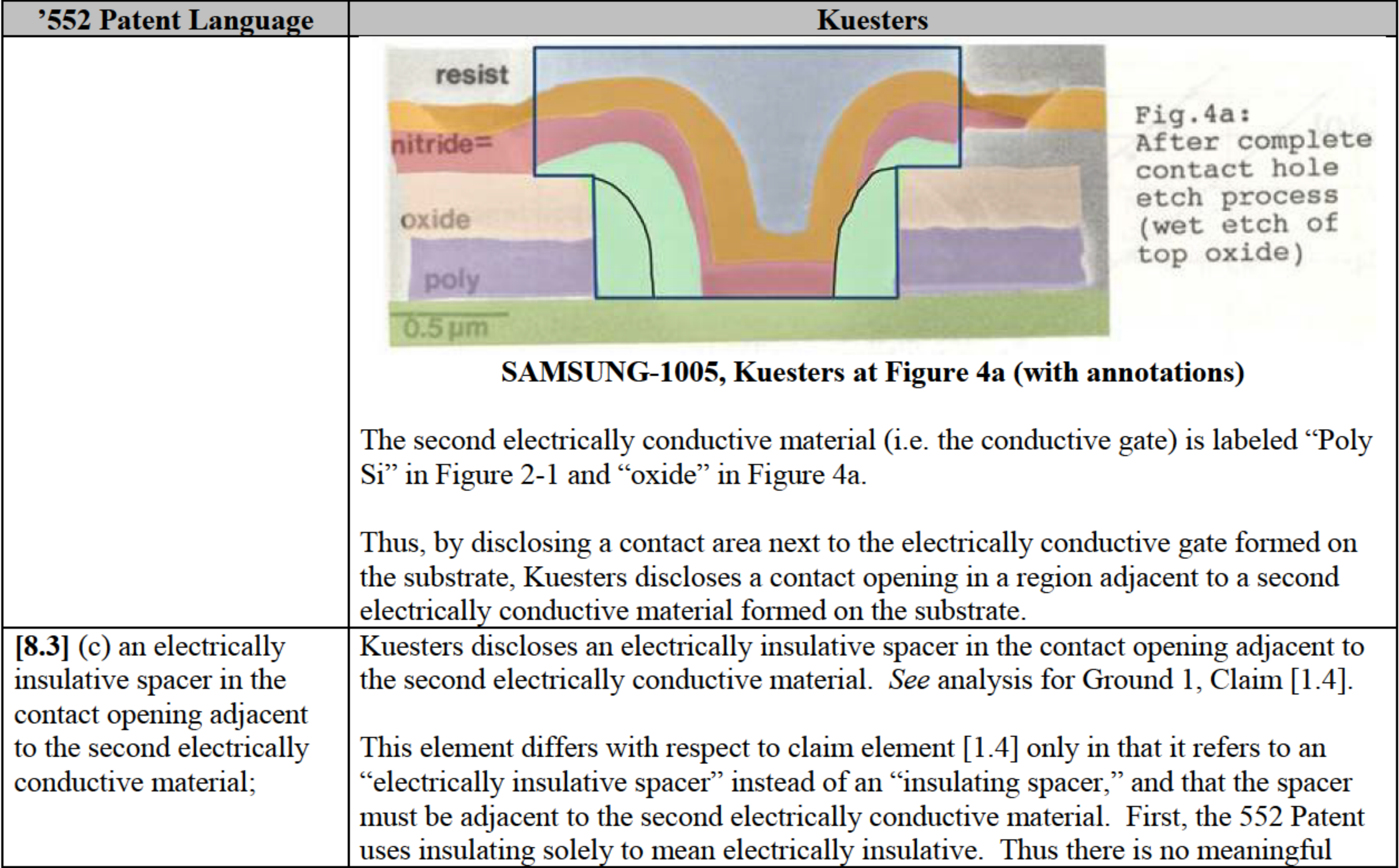
'552 Patent Language	Kuesters
	 **SAMSUNG-1005, Kuesters at Figure 4a (with annotations)** The second electrically conductive material (i.e. the conductive gate) is labeled "Poly Si" in Figure 2-1 and "oxide" in Figure 4a. Thus, by disclosing a contact area next to the electrically conductive gate formed on the substrate, Kuesters discloses a contact opening in a region adjacent to a second electrically conductive material formed on the substrate.
[8.3] (c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material;	Kuesters discloses an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material. *See* analysis for Ground 1, Claim [1.4]. This element differs with respect to claim element [1.4] only in that it refers to an "electrically insulative spacer" instead of an "insulating spacer," and that the spacer must be adjacent to the second electrically conductive material. First, the 552 Patent uses insulating solely to mean electrically insulative. Thus there is no meaningful

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'552 Patent Language	Kuesters
	difference between an "electrically insulative spacer" and an "insulating spacer." Furthermore, it would have been well known to a person of ordinary skill in the art as of 1995 that oxides are electrically insulative materials. Second, as annotated in bright green in Figures 2 and 4a below, the oxide insulating spacer is adjacent to the purple electrically conductive gate material.

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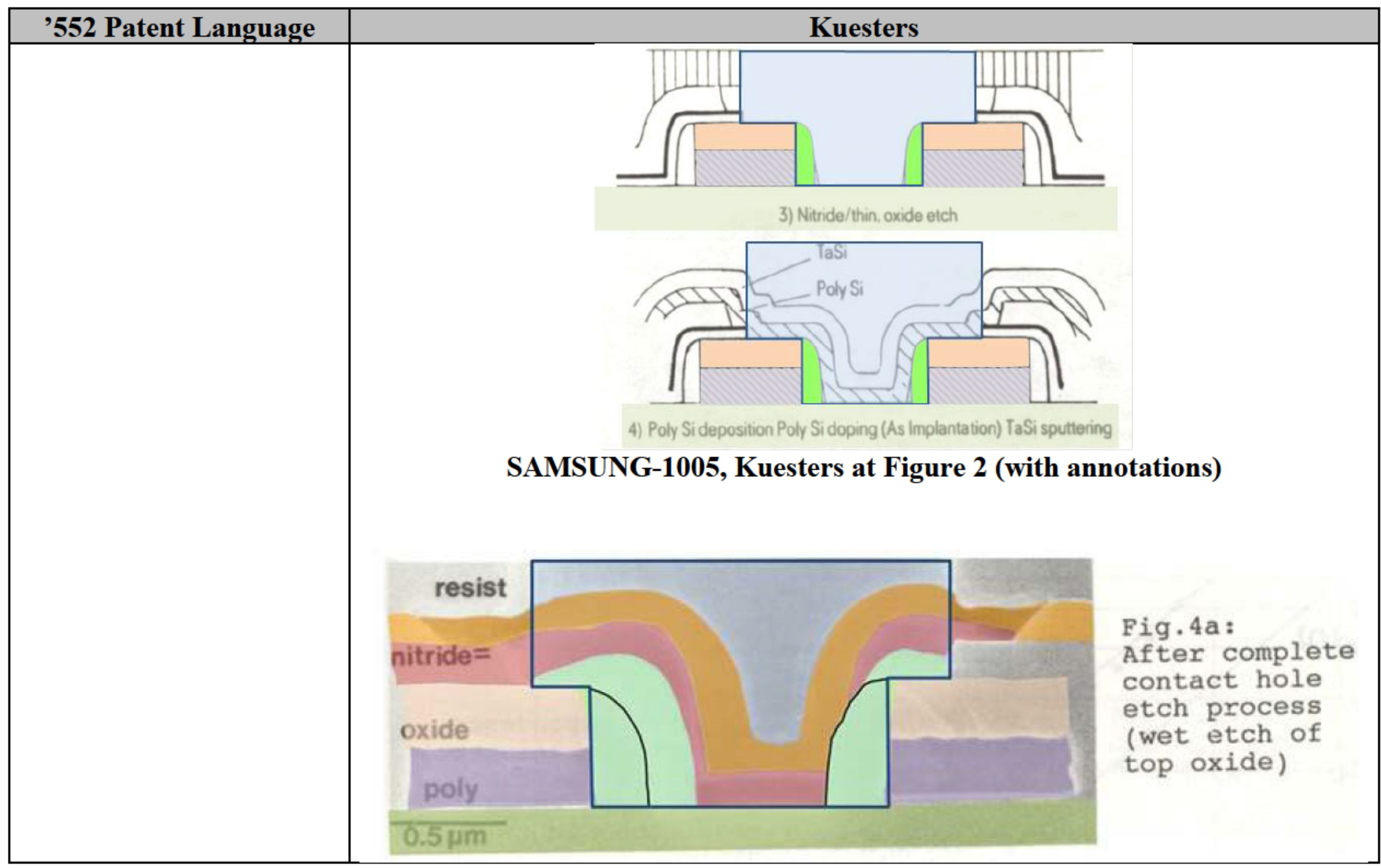
'552 Patent Language	Kuesters
	

SAMSUNG-1005, Kuesters at Figure 2 (with annotations)

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'552 Patent Language	Kuesters
	SAMSUNG-1005, Kuesters at Figure 4a (with annotations) The black line on the insulating spacer denotes the leading edge of the oxide spacer at the front plane of the SEM image (i.e. the center of the contact hole) in Figure 4a. Thus, by disclosing an oxide spacer in the contact area and adjacent to the electrically conductive gate material, Kuesters discloses an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material.
[8.4] (d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer;	Kuesters discloses an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer. *See* analysis for Ground 1, Claim [1.5]. This element differs with respect to claim element [1.5] only in that it requires the etch stop material to be "over the electrically insulative spacer and the first and second electrically conductive materials. As annotated in red in Figure 4a below, the etch stop material extends over the oxide spacer, the gate material, and the n+ doped source/drain regions of the substrate.

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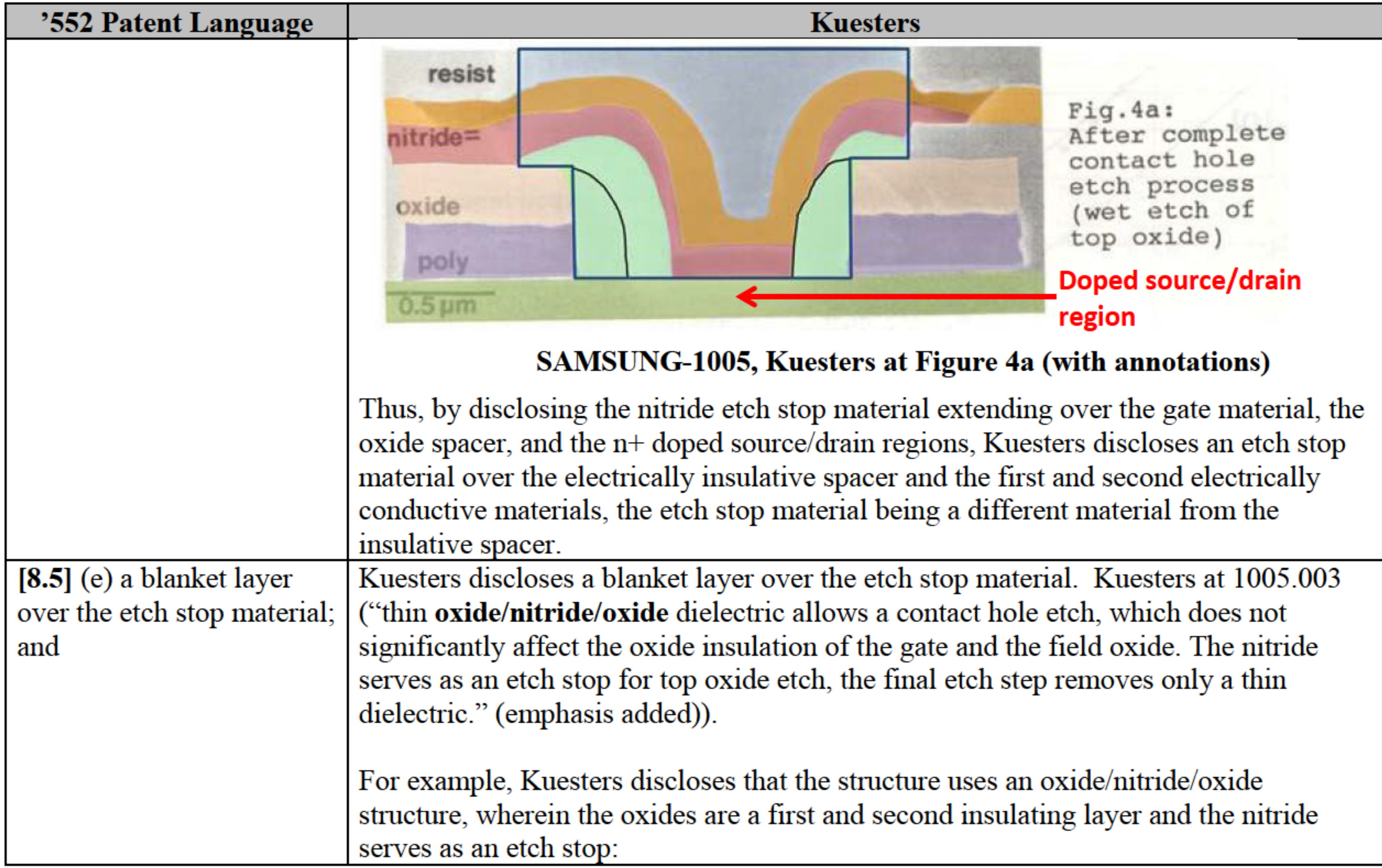
’552 Patent Language	Kuesters
	 **SAMSUNG-1005, Kuesters at Figure 4a (with annotations)** Thus, by disclosing the nitride etch stop material extending over the gate material, the oxide spacer, and the n+ doped source/drain regions, Kuesters discloses an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer.
[8.5] (e) a blanket layer over the etch stop material; and	Kuesters discloses a blanket layer over the etch stop material. Kuesters at 1005.003 (“thin **oxide/nitride/oxide** dielectric allows a contact hole etch, which does not significantly affect the oxide insulation of the gate and the field oxide. The nitride serves as an etch stop for top oxide etch, the final etch step removes only a thin dielectric.” (emphasis added)). For example, Kuesters discloses that the structure uses an oxide/nitride/oxide structure, wherein the oxides are a first and second insulating layer and the nitride serves as an etch stop:

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'552 Patent Language	Kuesters
	"**2.2.1 Contact hole etch** The dielectric under the bitline consists of **a triple layer of thin oxide/nitride/oxide**. For the top oxide a reflow technique (PH_3-diffusion and backetch of the doped oxide) is employed, with a final thickness of 0.2/um. The triple layer dielectric allows a contact hole etch, which does not significantly affect the field oxide and the oxide insulation of the gate (see fig. 2)." *Id.* at 1005.004 (emphasis added). "b) If the **top oxide** is wet etched (NH_4F/HF), a nitride layer of > l0nm is sufficient for the etch stop. T**he thin nitride and the thin oxide (= 50 nm) underneath** are etched by the same $CHF_3/0_2$ dry etch step (fig. 4a). The use of a rather thin nitride as an etch stop is also possible if combining a dry etch of the top oxide (without long overetch) and a wet etch to remove oxide spacers on the nitride." *Id.* at 1005.005 (emphasis added). The second oxide layer is annotated in bright orange in Figures 2 and 4a below. 3) Nitride/thin, oxide etch

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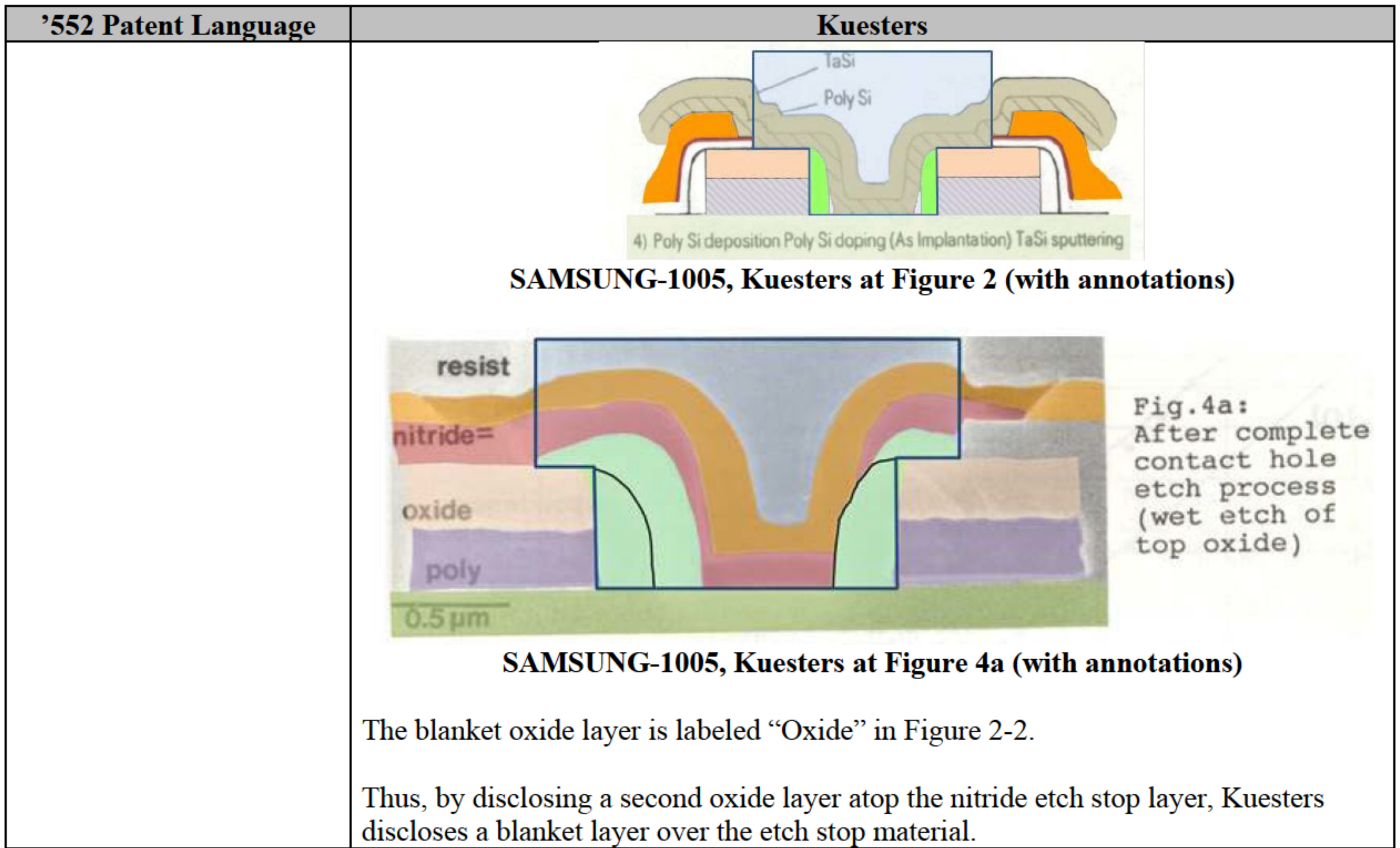
<table>
<tr><th>'552 Patent Language</th><th>Kuesters</th></tr>
<tr><td></td><td>


SAMSUNG-1005, Kuesters at Figure 2 (with annotations)

SAMSUNG-1005, Kuesters at Figure 4a (with annotations)

The blanket oxide layer is labeled "Oxide" in Figure 2-2.

Thus, by disclosing a second oxide layer atop the nitride etch stop layer, Kuesters discloses a blanket layer over the etch stop material.
</td></tr>
</table>

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’552 Patent Language	Kuesters
[8.6] (f) an opening through a first part of the etch stop material to the first electrically conductive material, wherein a side of the electrically insulative spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.	Kuesters discloses an opening through a first part of the etch stop material to the first electrically conductive material, wherein a side of the electrically insulative spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°. After the top blanket oxide layer has been etched using the wet etch process disclosed in Section 2.2.1(b), the nitride etch stop material in the center of the contact hole is etched by an anisotropic "CHF_3/O_2 dry etch step (Fig. 4a)." *Id.* at 1005.005. This anisotropic etch creates an opening through a part of the etch stop material to the electrically conductive n+ diffusion region. The opening through the nitride etch stop layer to the n+ doped diffusion region is annotated in black and labeled in Figure 2 below:

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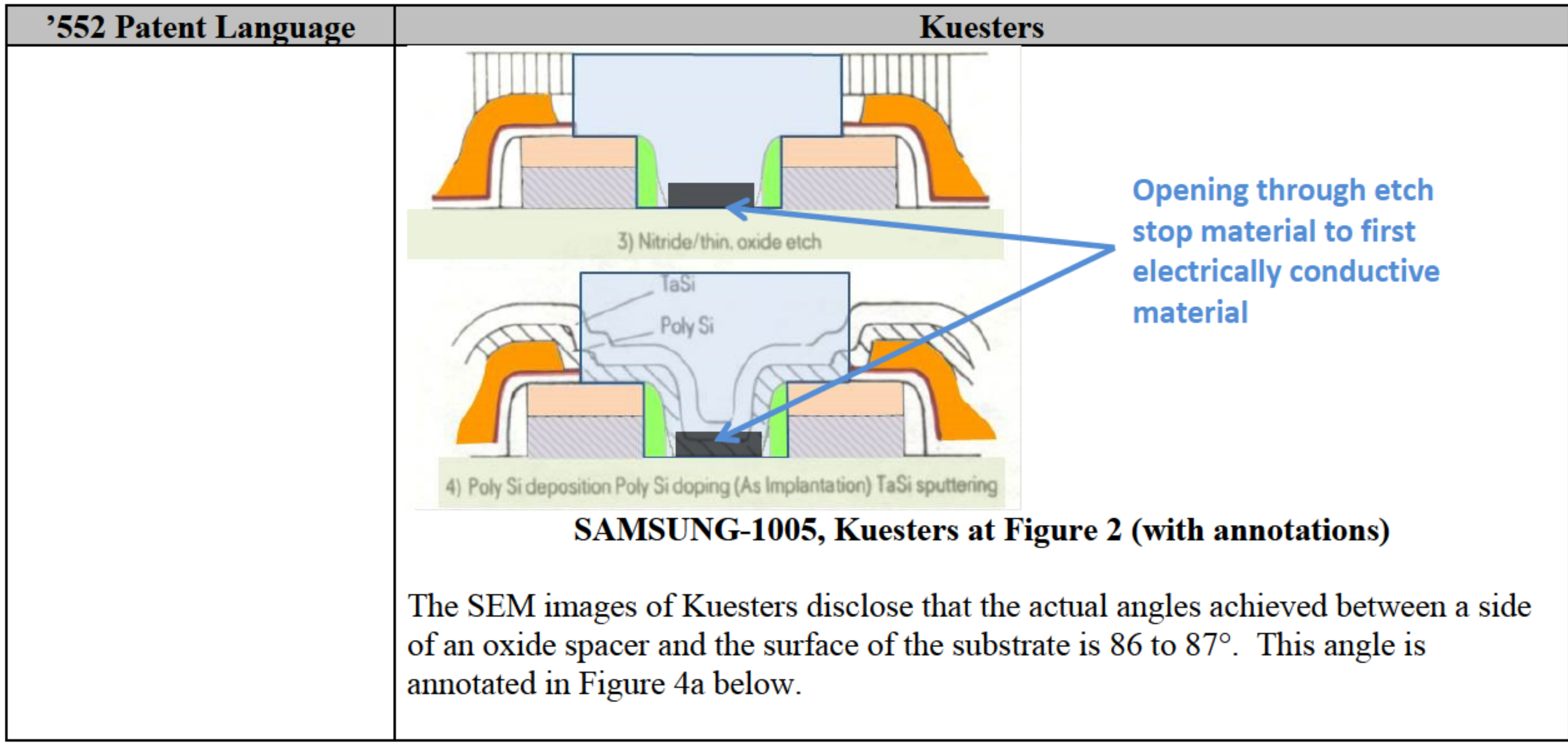
’552 Patent Language	Kuesters
	 **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)** The SEM images of Kuesters disclose that the actual angles achieved between a side of an oxide spacer and the surface of the substrate is 86 to 87°. This angle is annotated in Figure 4a below.

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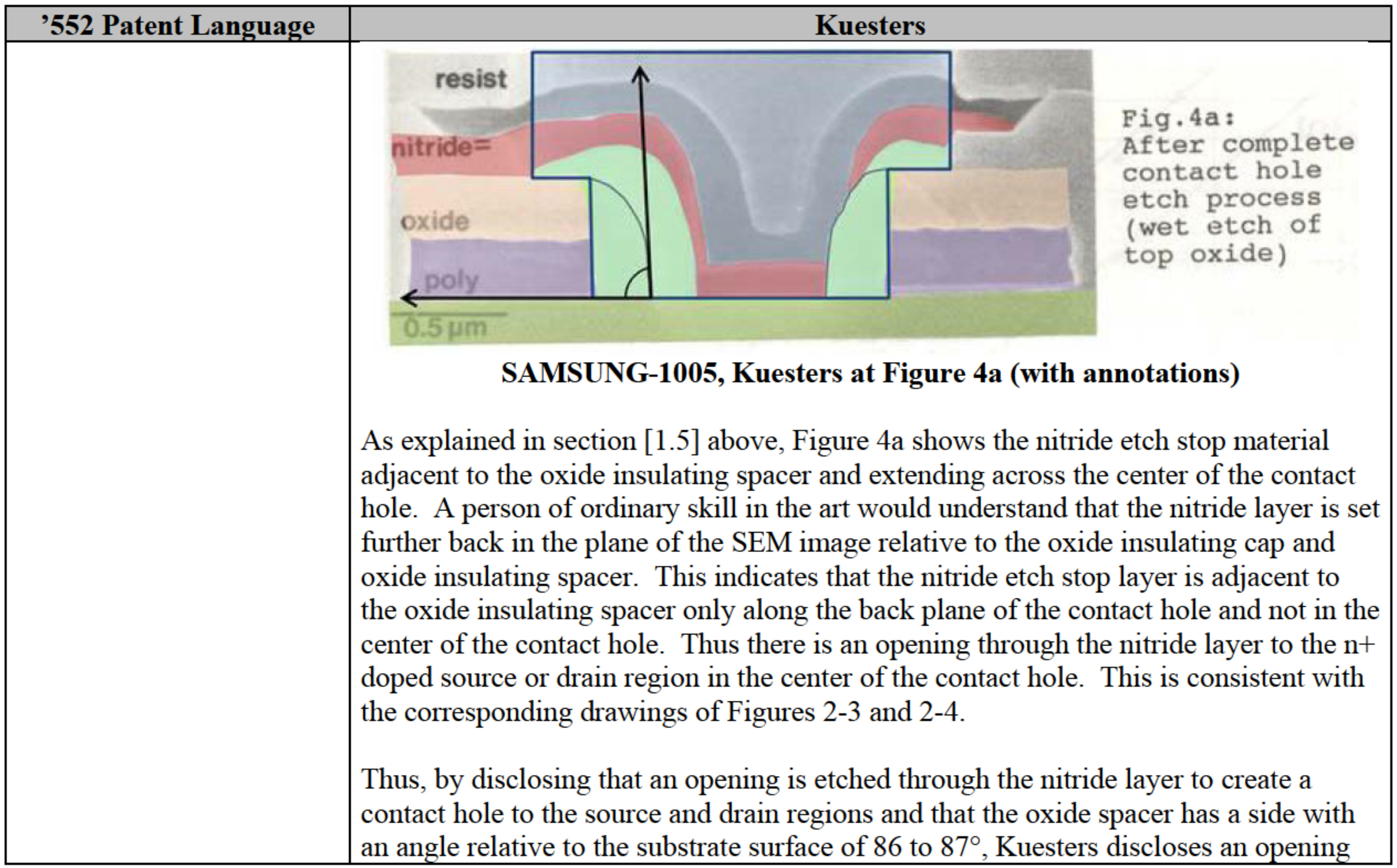
'552 Patent Language	Kuesters
	 **SAMSUNG-1005, Kuesters at Figure 4a (with annotations)** As explained in section [1.5] above, Figure 4a shows the nitride etch stop material adjacent to the oxide insulating spacer and extending across the center of the contact hole. A person of ordinary skill in the art would understand that the nitride layer is set further back in the plane of the SEM image relative to the oxide insulating cap and oxide insulating spacer. This indicates that the nitride etch stop layer is adjacent to the oxide insulating spacer only along the back plane of the contact hole and not in the center of the contact hole. Thus there is an opening through the nitride layer to the n+ doped source or drain region in the center of the contact hole. This is consistent with the corresponding drawings of Figures 2-3 and 2-4. Thus, by disclosing that an opening is etched through the nitride layer to create a contact hole to the source and drain regions and that the oxide spacer has a side with an angle relative to the substrate surface of 86 to 87°, Kuesters discloses an opening

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'552 Patent Language	Kuesters
	through a first part of the etch stop material to the first electrically conductive material, wherein a side of the electrically insulative spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.
Claim 9	
[9.0] The structure of claim **8**, wherein the electrically insulative spacer has a surface portion without overlying etch stop material.	*See* Claim [8.0] Kuesters discloses the structure of claim 8, wherein the electrically insulative spacer has a surface portion without overlying etch stop material. *See* analysis for Ground 1, Claim [4.0]. This element differs with respect to claim element [4.0] only in that it refers to an "electrically insulative spacer" instead of an "insulating spacer," and it eliminates the requirement that the portion "be in the contact region." As explained above in the analysis of Claim [8.3], the 552 Patent uses insulating solely to mean electrically insulative. Thus there is no meaningful difference between an "electrically insulative spacer" and an "insulating spacer."
Claim 10	
[10.0] The structure of claim **9**, wherein the electrically insulative spacer surface portion without overlying etch stop material comprises a	*See* Claim [9.0] Kuesters discloses structure of claim 9, wherein the electrically insulative spacer surface portion without overlying etch stop material comprises a surface portion most distant from the substrate. *See* analysis for Ground 1, Claim [5.0].

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'552 Patent Language	Kuesters
surface portion most distant from the substrate.	This element differs with respect to claim element [5.0] only in that it refers to an "electrically insulative spacer" instead of an "insulating spacer," and it eliminates the requirement that the portion "be in the contact region." As explained above in the analysis of Claim [8.3], the 552 Patent uses insulating solely to mean electrically insulative. Thus there is no meaningful difference between an "electrically insulative spacer" and an "insulating spacer."
Claim 11	
[11.0] The structure of claim **8**, further comprising a second insulating layer on the etch stop layer and over the conductive layer.	*See* Claim [8.0] Kuesters discloses the structure of claim **8**, further comprising a second insulating layer on the etch stop layer and over the conductive layer. *See* analysis of Ground 1, Claim [6.0].
Claim 12	
[12.0] The structure of claim **11**, further comprising a second conductive material in the contact region.	*See* Claim [11.0] Kuesters discloses the structure of claim **11**, further comprising a second conductive material in the contact region. *See* analysis of Ground 1, Claim [7.0].

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GROUND #2: CLAIM 3 IS OBVIOUS OVER KUESTERS IN LIGHT OF HAVEMANN

'552 Patent Claim Language	Kuesters in view of Havemann
Claim 3	
[3.0] The semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon dioxide.	Kuesters discloses all limitations of claim 1. *See* Claim 1 above. Kuesters does not disclose an etch stop material comprised of silicon dioxide. However, this limitation would have been obvious to one skilled in the art in view of the teachings of U.S. Patent No. 5,482,894 to Havemann (SAMSUNG-1006, "Havemann"). Like Kuesters, Havemann discloses a semiconductor structure consisting of a conductive layer over a substrate, an insulating layer on the conductive layer, a contact region in the insulating layer, an insulating spacer in the contact region, and an etch stop material over the insulating layer and adjacent to the insulating spacer, the etch stop material being different from the insulating spacer material. In particular, Havemann discloses a structure in which the insulating spacer material (28) is preferably thermally-grown oxide and the etch stop material (42) is preferably silicon nitride. Havemann at 5:9-21. Havemann further discloses that alternative materials may be used for both of these materials:

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<table>
<tr><th>'552 Patent Claim Language</th><th>Kuesters in view of Havemann</th></tr>
<tr><td></td><td>
The following table provides an overview of some embodiments cross-referenced to the drawings.
<table>
<tr><th>Drawing Element</th><th>Preferred or Specific Examples</th><th>Generic Term</th><th>Other Alternate Examples</th></tr>
<tr><td>20</td><td>Single-crystal silicon</td><td>Substrate</td><td></td></tr>
<tr><td>22</td><td>Thermally-grown oxide (SiO_2)</td><td>Gate oxide</td><td>Silicon nitride</td></tr>
<tr><td>26</td><td>Polysilicon w/ refractory metal silicide overlayer</td><td>Conductors</td><td>Aluminum, copper, tungsten, platinum, titanium</td></tr>
<tr><td>28</td><td>Thermally-grown oxide</td><td>Insulating conductor cap</td><td>CVD oxide, silicon nitride, doped oxides, silicon oxynitride</td></tr>
<tr><td>30</td><td>Thermally-grown oxide</td><td>Conformal dielectric layer</td><td>CVD oxide, silicon nitride, silicon oxynitride</td></tr>
<tr><td>32</td><td>Allied Signal 515 Series SOG</td><td>Organic-containing dielectric layer</td><td>Amorphous Teflon, parylene, polyimide</td></tr>
<tr><td>34</td><td>CVD silicon dioxide</td><td>Inorganic cap layer</td><td>Inorganic SOG, silicon nitride, doped oxides, silicon oxynitride</td></tr>
<tr><td>36</td><td></td><td>Photoresist</td><td></td></tr>
<tr><td>40</td><td>Tungsten w/ refractory metal underlayer</td><td>Contact plug</td><td>Aluminum, polysilicon, copper, titanium, tantalum, titanium nitride, refractory metal silicides</td></tr>
<tr><td>42</td><td>Silicon nitride</td><td>Conformal dielectric overlayer</td><td>Thermal oxide, CVD oxide</td></tr>
</table>
</td></tr>
</table>

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'552 Patent Claim Language	Kuesters in view of Havemann
	Havemann at 6:5-34. As is disclosed in the table of Havemann, it was well known that silicon oxynitride could be used as an insulating spacer, and thermally-grown oxide could be used as an etch stop layer. *See id.* Thermally-grown oxide was well known as a type of silicon dioxide used in semiconductor fabrication at the time of the filing of the 552 Patent. Applying this teaching to Kuesters would result in the structure of claim 1, with an etch stop layer of silicon dioxide and insulating layers and an insulating spacer of silicon oxynitride. It would have been obvious to combine the teachings of Havemann to Kuesters to make a simple substitution of materials with predictable results. I further discuss motivations to combine Kuesters and Havemann in Section IX(A), *supra*. Thus, by Havemann disclosing the use of silicon dioxide as an etch stop material and silicon oxynitride as an insulating material, and by Kuesters disclosing the structure of claim 1, Kuesters in view of Havemann discloses the semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon dioxide.

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GROUND #3: CLAIMS 1, 2, AND 4-7 ARE OBVIOUS OVER KUESTERS IN VIEW OF HEATH

'552 Patent Language	**Kuesters in view of Heath**
Claim 1	
[1.0] A structure, comprising:	Kuesters discloses a structure. *See* analysis for Ground 1, Claim [1.0].
[1.1] (a) a conductive layer disposed over a substrate;	Kuesters discloses a conductive layer disposed over a substrate. *See* analysis for Ground 1, Claim [1.1].
[1.2] (b) a first insulating layer on the conductive layer;	Kuesters discloses a first insulating layer on the conductive layer. *See* analysis for Ground 1, Claim [1.2].
[1.3] (c) a contact region in said first insulating layer;	Kuesters discloses a contact region in said first insulating layer. *See* analysis for Ground 1, Claim [1.3].
[1.4] (d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and	Kuesters discloses at least one insulating spacer in the contact region adjacent to the first insulating layer. *See* analysis for Ground 1, Claim [1.4]. It is my opinion that the insulating spacer including the oxide liner layer as annotated in Ground 1 above is an insulating spacer. However, to the extent the board finds that the oxide liner layer is not a part of the insulating spacer, Kuesters nonetheless discloses at least one insulating spacer in the contact region adjacent to the first insulating layer as annotated in Figure 2 below.

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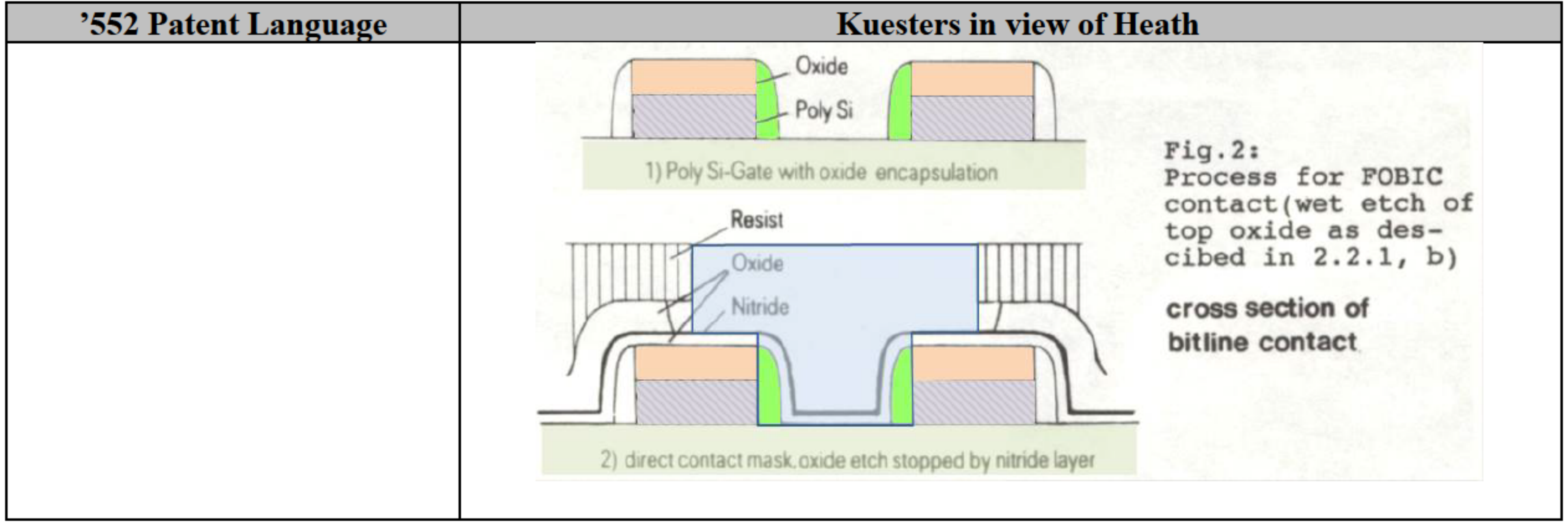
'552 Patent Language	Kuesters in view of Heath
	

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'552 Patent Language	Kuesters in view of Heath
	3) Nitride/thin, oxide etch TaSi Poly Si 4) Poly Si deposition Poly Si doping (As Implantation) TaSi sputtering **SAMSUNG-1005, Kuesters at Figure 2 (with annotations)** Thus, by disclosing an oxide spacer in the contact hole or area and adjacent to the oxide encapsulation, Kuesters discloses at least one insulating spacer in the contact region adjacent to the first insulating layer.
[1.5] an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,	Kuesters in view of Heath discloses etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer. To the extent the board finds that the oxide liner layer is not a part of an insulating spacer, Kuesters nonetheless discloses an etch stop material adjacent to the insulating spacer described in Ground 3, Claim [1.4] above.

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'552 Patent Language	**Kuesters in view of Heath**
	However, to the extent the board finds that the oxide liner layer is not a part of an insulating spacer and that the etch stop material is not adjacent to the insulating spacer described in Ground 3, Claim [1.4] above, Heath teaches a technique for creating a self-aligning contact in a semiconductor structure with the etch stop material in direct contact with the insulating spacer. *See* Heath at 5:26-39: "These and several other objects and advantages are obtained by providing **a self-aligned contact process** which involves establishing gate electrodes and/or isolation edges which are substantially vertical with respect to the substrate surface, **protecting the tops of these elements with an insulating oxide, protecting the top and sides of these structures with a layer to serve as an etch stop, and removing the etch stop in an anisotropic manner, so as not to remove the etch stop from the sidewalls of the gate electrodes or isolation edges.** Such etch stop is established between the relatively thick interlevel dielectric and the oxides covering the gate electrode and substrate. The etch stop preferably is silicon nitride." Like Kuesters, Heath discloses a semiconductor structure consisting of a conductive layer over a substrate, an insulating layer on the conductive layer, a contact region in the insulating layer, an insulating spacer in the contact region, and an etch stop material over the insulating layer and adjacent to the insulating

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'552 Patent Language	Kuesters in view of Heath
	spacer, the etch stop material being different from the insulating spacer material. This structure is disclosed in Figure 8C as annotated below. **SAMSUNG-1007, Heath at Figure 8C (with annotations)** Figure 8C has been annotated in accordance with the annotations for the figures of Kuesters. Specifically, light green denotes the substrate, purple denotes the conductive layer, orange denotes the first insulating layer, blue denotes the contact region, bright green denotes the insulating spacer, and red denotes the etch stop material. In Figure 8C, above, layers 24*a* and 24*b* are an oxide layer that "is relatively thin over the source/drain 20 as show at 24*a*, but is relatively thick on the top of gate

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'552 Patent Language	Kuesters in view of Heath
	electrode 16, as shown at 24*b*." *Id.* at 9:52-55. Layer 16a is "a sidewall spacer" that is "formed illustratively of oxide" and "remains in the structure after completion of the circuit." *Id.* at 10:18-25. Etch stop layer 10 is composed of nitride and stops the etch of the interlevel dielectric layer 34. *Id.* at 9:63-67. An anisotropic dry etch is then performed and "the part of layer 10 between dashed lines 56 is removed" as well as "the then-exposed parts of oxide 24*a* and 24*b*." *Id.* at 10:1-5. Heath differs from Kuesters in that Kuesters uses an additional liner layer of oxide as an insulating spacer and to protect the silicon substrate from the nitride etch-stop layer, whereas Heath uses the previously deposited oxide layer 24 to protect the silicon substrate from the nitride etch-stop layer without the need for an additional oxide liner layer. *See* Heath at 12:10-43: "As mentioned, the process is useful in double poly systems. In such a case, **it is preferred to grow a thin oxide on the sides of poly I to prevent shorts between poly I and poly II.** This oxide, preferably about 500A thick, is not required to make self-aligned contacts. In view of the foregoing lengthy descriptions**, it will suffice to outline the steps of an illustrative method for double polysilicon technology**. Moreover, it will be understood that either of the poly levels can optionally be polycide. Briefly, the process steps in such a system are as follows, it being understood that the process could be CMOS or not and illustratively is: 1. grow thin oxide on silicon substrate;

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'552 Patent Language	Kuesters in view of Heath
	2. deposit and dope Poly I; 3. oxidize, mask and etch Poly I; 4. **grow thin oxide on silicon substrate for Poly II gate oxide and on sides of Poly I electrodes**; 5. deposit, dope and oxidize Poly II; 6. **mask and etch Poly II, leaving some gate oxide in the active area regions**; 7. implant source and drain impurities and heat drive; 8. mask and etch contact windows to Poly I and Poly II but not source/drain regions; 9. **deposit nitride layer**; 10. deposit BPSG (density and reflow BPSG); 11. mask contact windows to poly I and poly II gate electrodes and source/drain regions; 12. **etch through BPSG to nitride layer**; 13. (density and reflow BPSG;) 14. **etch through nitride layer and underlying oxide to source/drain regions, and Poly I and Poly II gate electrodes**; 15. add metal or other conductive material for interconnects." Applying this teaching to Kuesters would result in the same structure as otherwise disclosed in Kuesters, simply without the oxide liner layer beneath the etch-stop layer. It would have been obvious to combine the teachings of Heath to Kuesters to improve the same structure with a known technique with

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'552 Patent Language	Kuesters in view of Heath
	predictable results. I further discuss motivations to combine Kuesters and Heath in Section IX(B), *supra*. Thus, by Heath disclosing the use of a silicon nitride etch stop layer in direct contact with an oxide sidewall spacer and over an oxide insulating layer, Kuesters in view of Heath discloses an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer.
[1.6] wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.	Kuesters discloses a side of the insulating spacer having an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°. *See* analysis for Ground 1, Claim [1.6].
Claim 2	
[2.0] The semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon nitride.	Kuesters in view of Heath discloses the semiconductor apparatus of claim 1 wherein the etch stop material comprises silicon nitride. Kuesters in view of Heath discloses all of the elements of claim 1. *See* Ground 3, Claim 1. Kuesters discloses an etch stop material comprising silicon nitride. *See* analysis for Ground 1, Claim 2.

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'552 Patent Language	Kuesters in view of Heath
Claim 4	
[4.0] The structure of claim 1, wherein the insulating spacer has a surface portion in the contact region without overlying etch stop material.	Kuesters in view of Heath discloses the structure of claim 1, wherein the insulating spacer has a surface portion in the contact region without overlying etch stop material. Kuesters in view of Heath discloses all of the elements of claim 1. *See* Ground 3, Claim 1. Kuesters discloses an insulating spacer having a surface portion in the contact region without overlying etch stop material. *See* analysis for Ground 1, Claim 4.
Claim 5	
[5.0] The structure of claim 4, wherein the insulating spacer surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said substrate.	Kuesters in view of Heath discloses the structure of claim 4, wherein the insulating spacer surface portion without overlying etch stop material is the insulating spacer surface portion most distant from said substrate. Kuesters in view of Heath discloses all of the elements of claim 4. *See* Ground 3, Claim 4. Kuesters discloses an insulating spacer with a surface portion without overlying etch stop material wherein the surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said substrate. *See* analysis for Ground 1, Claim 5.

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'552 Patent Language	Kuesters in view of Heath
Claim 6	
[6.0] The structure of claim 1, further comprising a second insulating layer on the etch stop layer and over the conductive layer.	Kuesters in view of Heath discloses the structure of claim 1, further comprising a second insulating layer on the etch stop layer and over the conductive layer. Kuesters in view of Heath discloses all of the elements of claim 1. *See* Ground 3, Claim 1. Kuesters discloses a second insulating layer on the etch stop layer and over the conductive layer. *See* analysis for Ground 1, Claim 6.
Claim 7	
[7.0] The structure of claim 6, further comprising a second conductive material in the contact region.	Kuesters in view of Heath discloses the structure of claim 6, further comprising a second conductive material in the contact region. Kuesters in view of Heath discloses all of the elements of claim 6. *See* Ground 3, Claim 6. Kuesters discloses a second conductive material in the contact region. *See* analysis for Ground 1, Claim 7.

APPENDIX A

GROUND #4: CLAIM 3 IS OBVIOUS OVER KUESTERS IN LIGHT OF HEATH AND HAVEMANN

'552 Patent Claim Language	Kuesters in view of Heath and Havemann
Claim 3	
[3.0] The semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon dioxide.	Kuesters in view of Heath and Havemann discloses the semiconductor apparatus of claim 1 wherein said etch stop material comprises silicon dioxide. Kuesters in view of Heath discloses all of the elements of claim 1. *See* Ground 3, Claim 1. Havemann discloses an etch stop material comprising silicon dioxide as well as insulating layers and an insulating spacer of silicon oxynitride. *See* analysis for Ground 2, Claim 3. Applying this teaching to Kuesters in view of Heath would result in the structure of claim 1, with an etch stop layer of silicon dioxide and insulating layers and an insulating spacer of silicon oxynitride. It would have been obvious to combine the teachings of Havemann to Kuesters in view of Heath to make a simple substitution of materials with predictable results. I further discuss motivations to combine Kuesters, Heath, and Havemann in Section IX(C), *supra*. Thus, by Havemann disclosing the use of silicon dioxide as an etch stop material and silicon oxynitride as an insulating material, and by Kuesters in view of Heath disclosing the structure of claim 1, Kuesters in view of Heath and Havemann discloses the semiconductor apparatus of claim 1 wherein said etch

APPENDIX A

'552 Patent Claim Language	Kuesters in view of Heath and Havemann
	stop material comprises silicon dioxide.