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APPLICATION FOR UNITED STATES PATENT

FOR

METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

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BACKGROUND OF THE INVENTION

Field of the Invention:

The invention relates to semiconductor device processes, and more particularly, to improved methods for etching openings in insulating layers and a semiconductor device with well defined contact openings.

Background of the Invention

In the fabrication of semiconductor devices, numerous conductive device regions and layers are formed in or on a semiconductor substrate. The conductive regions and layers of the device are isolated from one another by a dielectric. Examples of dielectrics include silicon dioxide, SiO_2, tetraethyl orthosilicate glass ("TEOS"), silicon nitrides, Si_xN_y, silicon oxynitrides, $SiO_xN_y(H_z)$, and silicon dioxide/silicon nitride/silicon dioxide ("ONO"). The dielectrics may be grown, or may be deposited by physical deposition (e.g., sputtering) or by a variety of chemical deposition methods and chemistries (e.g., chemical vapor deposition ("CVD")). Additionally, the dielectrics may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate glass ("BPTEOS").

At several stages of the fabrication of semiconductor devices, it is necessary to make openings in the dielectric to allow for contact to underlying regions or layers. Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and the first metal layer is called a "contact opening", while an opening in other oxide layers such as an opening through an intermetal dielectric layer is referred to as a "via". For purposes

of the claimed invention, henceforth "contact opening" or "contact region" will be used to refer to contact openings and/or via. The opening may expose a device region within the silicon substrate, such as a source or drain, or may expose some other layer or structure, for example, an underlying metallization layer, local interconnect layer, or structure such as a gate. After the opening has been formed exposing a portion of the region or layer to be contacted, the opening is generally cleaned with a sputter etch, e.g., a Radio-Frequency ("RF") sputter etch, and then the opening is filled with a conductive material deposited in the opening and in electrical contact with the underlying region or layer.

To form the openings a patterning layer of photoresist is first formed over the dielectric layer having openings corresponding to the regions of the dielectric where the dielectric layer openings are to be formed. In most modern processes a dry etch is then performed wherein the wafer is exposed to a plasma, formed in a flow of one or more gases. Typically, one or more halocarbons and/or one or more other halogenated compounds are used as the etchant gas. For example, CF_4, CHF_3 (Freon 23), SF_6, NF_3, and other gases may be used as the etchant gas. Additionally, gases such as O_2, Ar, N_2, and others may be added to the gas flow. The particular gas mixture used will depend on, for example, the characteristics of the dielectric being etched, the stage of processing, the etch tool being used, and the desired etch characteristics, i.e., etch rate, sidewall slope, anisotropy, etc.

Many of the etch characteristics are generally believed to be affected by polymer residues that deposit during the etch. For this reason, the fluorine to carbon (F/C) ratio in the plasma is considered an important determinant in the etch. In general, a plasma with a high F/C ratio will have a faster etch rate than a plasma with a low F/C ratio. At very low rates, i.e., high carbon content, polymer deposition occurs and etching ceases. The etch rate as a function of the F/C ratio is

typically different for different materials. The difference is used to create a selective etch, by using a gas mixture that puts the F/C ratio in the plasma at a value that leads to etching at a reasonable rate for one material, and that leads to no etching or polymer deposition for another. For example, an etchant that has an etch rate ratio or a selectivity ratio of two to one for silicon nitride compared to silicon dioxide is an effective stripper of silicon nitride from the semiconductor substrate, because it will selectively strip silicon nitride over silicon dioxide on a substrate surface. An etchant that has an etch rate ratio or a selectivity ratio of 0.85 to one for silicon nitride compared to silicon dioxide is not considered an effective stripper of silicon nitride from the semiconductor substrate because the etchant will not effectively strip silicon nitride to the exclusion of silicon dioxide.

The selectivity of the etch process is a useful parameter for monitoring the process based on the etch rate characteristic of the particular etchant. As noted above, particular etchants or etchant chemistries attack different materials at different etch rates. With respect to dielectrics, for example, particular etchants attack silicon dioxide, BPTEOS, TEOS, and silicon nitride dielectrics at different rates. To make openings in a substrate comprising a contact region surrounded by different dielectric layers, e.g., a dielectric layer of TEOS surrounded by a dielectric layer of silicon nitride, a process will utilize different etchants to make openings through the different dielectrics. Thus, the different etch rates of particular dielectric layers for an etchant may be used to monitor the creation of an opening through a dielectric layer.

Further, by adjusting the feed gases, the taper of the sidewall in the etched opening of the dielectric can be varied. If a low sidewall angle is desired, the chemistry is adjusted to try to cause some polymer buildup on the sidewall. Conversely, if a steep sidewall angle is desired, the chemistry is adjusted to try to

prevent polymer buildup on the sidewall. Varying the etch gas pressure, for example, has a significant effect on the shape of the opening. This is because the etchant ions generally arrive in a direction perpendicular to the substrate surface, and hence strike the bottom surfaces of the unmasked substrate. The sidewalls of etched openings, meanwhile, are subjected to little or no bombardment. By increasing the pressure of the etch gas, the bombardment directed toward the sidewalls is increased; by decreasing the pressure of the etch gas, the bombardment directed toward the sidewalls is decreased. The changing of the etch chemistry is also directly related to selectivity. Etchants that provide a near 90° sidewall angle are generally not highly selective while highly selective etches typically produce a sloped sidewall.

Following the dielectric etch(es) and prior to any conductive material deposition in a contact region, native oxide on top of the conducting layers in the contact region is removed or cleaned through a non-chemical sputter etch, e.g., an RF sputter etch. In addition to alleviating the contact region of native oxide, the sputter etch can erode any insulating dielectric layer or layers. Thus, the parameters of the sputter etch must be carefully monitored so as not to excessively erode the insulating dielectric layer(s) and expose other underlying conductive material. Exposing insulated conductive material adjacent to the conductive material in the contact region results in poor quality contacts or a short circuit through the underlying conductive material. For a thorough discussion of oxide etching, see S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Vol. 1, pp. 539-85 (1986).

The preceding discussion focused on the making of openings, e.g., contact openings, in dielectric material on a semiconductor substrate. The same principles are used in constructing device regions with a dielectric layer or layers. As geometries shrink, the forming of discreet devices on a semiconductor substrate

becomes more specialized. Specialized deposition and etching techniques permit the density of semiconductor elements on a single chip to greatly increase, which translates into larger memory, faster operating speeds, and reduced production costs.

A typical metal oxide semiconductor (MOS) transistor, e.g., NMOS or PMOS transistor, generally includes source/drain regions in a substrate, and a gate electrode formed above the substrate between the source/drain regions and separated from the substrate by a relatively thin dielectric. Contact structures can be inserted to the source/drain regions and interlays can overlie the contact structures and connect neighboring contact structures. These contact structures to the diffusion region are isolated from the adjacent gate by dielectric spacer or shoulder portions. The dielectric spacer or shoulder portions also isolate the gate from the diffusion region.

Conventional contact structures limit the area of the diffusion region, because the contact hole is aligned to these regions with a separate masking step, and extra area must be allocated for misalignment. Proper alignment is necessary to avoid shorting the contact structure to the gate or the diffusion well. The larger contact area means a smaller density of elements on a structure. The larger contact area is also responsible for increased diffusion-to-substrate junction capacitance, which limits device speed.

A self-aligned contact eliminates the alignment problems associated with conventional contact structures and increases the device density of a structure. A self-aligned contact is a contact to a source or drain diffusion region. A self-aligned contact is useful in compact geometries because it can overlap a conducting area to which it is not supposed to make electrical contact and can overlap the edge of a diffusion region without shorting out to the well beneath. Consequently, less

contact area is needed and gates or conductive material lines, e.g., polysilicon lines, can be moved closer together allowing more gates or lines on a given substrate than traditional contacts.

Figure 1 illustrates a self-aligned contact between two gate structures. Figure 1(A) is a planar top view of the contact. Figure 1(B) is a planar cross-sectional view of a self-aligned contact between a pair of gates taken through line 1(B) of Figure 1(A). Figure 1(C) is a planar cross-sectional view of a self-aligned contact between a pair of gates taken through line 1(C) of Figure 1(A).

The self-aligned contact is a contact to a source or drain diffusion region (n+ or p+ silicon) 140 that can overlap the edge of the diffusion region 140 without shorting out to the well beneath the diffusion region 140. This can be seen most illustratively through Figure 1(C). In Figure 1(C), the contact 130 does not lie directly in the diffusion region 140, but is misaligned and slightly overlaps the field oxide. In this illustration, the self-aligned contact is not directly over the diffusion region but extends over (i.e., overlaps) a well portion 170. The self-aligned contact does not short to the well portion 170 because the self-aligned contact is separated from the well 170 by the field oxide.

The self-aligned contact 130 is separated from a conducting polysilicon layer 110 by an encapsulating dielectric layer 120 such that the contact 130 can also overlap the polysilicon layer 110 without making electrical contact to the layer 110 or gate. The polysilicon layer 110 is separated from the source/drain diffusion region 140 by a dielectric spacer or shoulder 150 of the same or different dielectric material as the dielectric layer 120 directly above the conducting polysilicon.

A distinct dielectric etch stop layer 125 overlies the encapsulating dielectric layer 120. The etch stop layer 125 permits subsequent etching of the substrate

without risk of exposing the device structures and layers because the device structuring and layers are protected from excessive etching by the etch stop layer. The diffusion contact is self-aligning because the structure can be etched to the substrate over the source/drain diffusion region 140 while the dielectric spacer 150 protects the polysilicon layer 110. Even if a photoresist that protects the polysilicon layer 110 from the etchant is misaligned with respect to the polysilicon layer 110, the dielectric spacer 150 prevents shorts to the polysilicon layer 110 when the contact 130 is provided for the diffusion region 140.

The current practice with respect to forming contact regions, particularly self-aligned contact regions, that are in electrical contact with gates, interconnect lines, or other structures in small feature size structures utilize etchants with high selectivity to protect underlying regions, like the etch stop layer and the first insulating layer. Figure 2 demonstrates a typical prior art process of forming a self-aligned contact region adjacent to a gate. In Figure 2(A), a gate oxide layer 210 is formed on a substrate 200 with a conducting layer, for example a polysilicon layer 220, overlying the gate oxide layer 210, and an insulating layer, for example a TEOS layer 230, overlying the polysilicon layer 220. Adjacent to the polysilicon layer is a contact opening region 270. The polysilicon layer 220 is separated from the contact region 270 by an insulating spacer portion, for example a TEOS spacer portion 235. A separate insulating or etch stop layer, for example a silicon nitride layer 240 overlies the TEOS layer 230 and the contact region 250. A blanket layer, for example a doped insulating layer like a BPTEOS layer 250, planarly overlies the etch stop layer 240.

A layer of photoresist material 280 overlies the planarized BPTEOS layer 250 to expose the contact opening 270. In Figure 2(A), a contact opening 270 has been opened through the BPTEOS layer 250. The etchant utilized to make the opening had a high selectivity toward BPTEOS relative to silicon nitride. When the contact

opening was through the BPTEOS material, the etchant did not etch or did not effectively etch the silicon nitride layer 240 material. Hence the description of the silicon nitride layer 240 as an etch stop layer. The silicon nitride etch stop layer protected the underlying TEOS layer so that the polysilicon remains completely encapsulated.

Figure 2(A) illustrates an etch 260 to remove the silicon nitride etch stop layer 240. In the etch illustrated in Figure 2(A), a high selectivity etch toward silicon nitride relative to the underlying TEOS layer 230 material is practiced to efficiently etch the silicon nitride layer and to protect the underlying TEOS layer 230 from the etchant. An example of a high selectivity etch recipe to effectively strip silicon nitride as compared to the TEOS layer is 30 sccm CHF_3 and 30 sccm O_2 at 60 mtorr and 100 watts of power. The result of the high selectivity etch is illustrated in Figure 2(B).

Figure 2(B) shows that the silicon nitride selective etch effectively removed silicon nitride 240 from the contact opening 270. The selective etch for silicon nitride compared to TEOS material, however, left the TEOS layer 230 with a spacer portion 235 wherein the spacer portion is sloping or tapered toward the contact opening. This result follows even where the spacer portion 235 is originally substantially rectangular as in Figure 2(A). The properties of the highly selective etch of the overlying etch stop layer will transform a substantially rectangular spacer into a sloped spacer. Figure 2(B) presents a polysilicon layer 220 encapsulated in a TEOS layer 230 with a spacer portion 235 adjacent to the contact opening 270, the spacer portion 235 having an angle 290 that is less than 85°.

In addition to providing stopping points or selectivity between materials, the use of high selectivity etches to form sloped spacer portions is the preferred practice

because the sloped shape will result in good step coverage by the metal that is deposited into it. The filling of contact openings or gaps (i.e., gap fill) is an important consideration because it relates directly to the reliability of a device. If an opening is not completely filled with a insulative material, for example, and a gap is created, a subsequent conductive material deposit can fill the gap which can lead to shorting. Sloped contact openings are easier to completely fill than boxy structures because the transition between sloped structures and openings is smooth compared to the abrupt transitions between boxy structures and openings. Because of concerns for complete gap fill and good step coverage, industry preference is for sloped spacers and planar deposition layers similar to that shown in Figure 2(b).

Once the contact opening is made, the opening is cleaned with a sputter etch, e.g., an RF sputter etch, before conductive material is added to fill the opening or gap. The RF sputter etch that is used to clean the contact opening in the process described above will attack and erode a portion of the insulating spacer surrounding the conducting portion and adjacent to the contact region. Figure 3 presents a prior art substrate with a gate and a contact region undergoing an RF sputter etch. In Figure 3, a gate oxide 310 is formed on a substrate 300 with a polysilicon layer 320 overlying the gate oxide 310 and an insulating layer, for example a TEOS layer 330 overlying the polysilicon layer 320. A distinct insulating layer, for example a silicon nitride etch stop layer 340, overlies the TEOS layer 330 and this etch stop layer 340 is covered by a third insulating layer, for example a BPTEOS blanket layer 350. Adjacent to the gate is a contact region 360. An etch of the silicon nitride etch stop layer 340 with a high selectivity etch for silicon nitride relative to the underlying TEOS layer material produced a gate with a sloping or tapered spacer portion 370 of TEOS material, illustrated in ghost lines. A subsequent RF sputter etch is utilized to clean the contact region 360.

Although brief and designed to clean the contact region, the RF sputter etch will erode a portion of the insulating TEOS spacer. The dynamics of the sputter etch are that it proceeds vertically, directing high-energy particles at the contact region. The sloping or tapered spacer portion adjacent the polysilicon and separating the polysilicon from the diffusion region is struck by the high-energy particles of the RF sputter etch 380. Because the spacer portion 370 is sloping or diagonal, a significant surface area portion of the spacer portion 370 is directly exposed to the high-energy particles from the RF sputter etch 380. Further, with sloping spacers, or spacers having an angle relative to the substrate surface of less than 85° the vertical portion of the dielectric layer ((i.e., that portion above the polysilicon gate) decreases much less than the diagonal portion of the spacer. In terms of measuring TEOS material removal during the RF sputter etch in Figure 3, the difference between d_1 and d_2 is greater than the difference between v_1 and v_2. Thus, in conventional prior art self-aligned contact structures, the diagonal thickness of the TEOS spacer, rather than the vertical thickness of the TEOS layer, determines the minimum insulating layer thickness for the gate.

For gate structures having minimum diagonal insulative spacer portions of 500 Å or less, the result of the sputter etch 380 is that the sputter etch 380 laterally erodes the diagonal portion of the TEOS layer 370 adjacent to the contact region to a point where the polysilicon 320 is no longer isolated from the contact region 360 by an insulating layer. In that case, there is a short circuit through the underlying conductive material when the contact opening is filled with conductive material. This result follows because the conventional RF sputter etch utilized for cleaning the contact region results in an approximately 200-500 Å loss of the spacer material. Further, process margins generally require that the device spacer have a final minimum thickness (after all etches, doping, and deposits) of at least 500 Å. Thus,

to eliminate alignment sensitivity for conventional small feature size structures, including self-aligned contact structures, requires a final (i.e., at the time of contact deposition) minimum insulating spacer of more than 500 Å and preferably on the order of 1000-1500 Å or greater to fulfill requirements for an adequate process margin, complete gap fill, and device reliability.

To construct structures having a minimum insulative spacer portion of more than 500 Å directly effects the number of structures that can be placed on a device, such as a chip. The construction of structures having a minimum insulative spacer portion of more than 500 Å requires that the pre-etch-stop-etch spacer be bigger or thicker to yield an effective spacer after the etching processes. In such cases, the structures must be separated a distance such that the contact area opening is sufficient enough for an effective contact. This spacing requirement directly limits the number of structures that can be included on a device. In small feature size structures, particularly structures utilizing self-aligned contacts, the width of contact openings is approximately 0.6 microns at the top of the planarized layer and 0.2 microns at the base of the contact opening. Figure 3 indicates the difference in contact opening widths for the same contact in prior art structures. w_1 represents the width at the top of the planarized layer and w_2 represents the width at the base of the contact opening. Further, an aspect ratio can be defined as the height of a structure (field oxide plus conductive layer plus first insulative layer plus etch stop layer, if any) relative to the width of the base of a contact opening (i.e., the distance between adjacent spacers). Typical aspect ratios for self-aligned contact structures target ratios of 1.0-2.4. This prior art range is not achievable with any device reliability. To achieve aspect ratios of 1.0-2.4 requires minimum spacer portions of less than 1000 Å and preferably on the order of 500 Å. As noted above, the minimum spacer portions required for aspect ratios of 1.0-2.4 cannot withstand the

sputter etch and will result in the exposure of the underlying polysilicon gate and short circuiting with the contact.

There is a need for cost effective structures wherein the individual devices are as close together as possible while maintaining device reliability and an adequate process margin and assuring complete gap fill. There is a need for a device and for a process to manufacture such a device whereby there is provided a contact opening with no alignment sensitivity relative to a gate electrode or other structure and whereby the gate electrode does not fall within the contact opening but remains isolated from the contact opening by an insulating layer. The process must be compatible with gate electrode insulating spacers of less than 500 Å. The device resulting from the needed process should be capable of maintaining high quality contacts between the conductive material in the contact region and the adjacent conductive gate or other structure.

SUMMARY OF THE INVENTION

The invention relates to a process for minimizing lateral spacer erosion of an insulating layer on an enclosed contact region is disclosed and a device including a contact opening with a small alignment tolerance relative to a gate electrode or other structure. The process provides high quality contacts between a conductive material in the contact region and a device region, such as a source or drain, or some other layer or structure. The process comprises the well known step of forming a conductive layer on the semiconductor body adjacent a contact region. This is followed by the forming of a first insulating layer adjacent said conductive layer and the contact region. A selected area is masked with photoresist and the first insulating layer and the conductive layer are etched to form a device structure, such as a gate, adjacent the contact region. Next, insulating lateral spacers are added to the device structure to isolate the conductive portion of the device. The insulating spacers are etched so that the device comprises an insulating layer overlying a conductive layer with a lateral spacer portion adjacent the contact region wherein the spacer portion has a substantially rectangular profile. A distinct insulating layer or etch stop layer is then formed adjacent to the first insulating layer and over the contact region. A third insulating layer or blanket layer is then optionally formed over the etch stop layer. The blanket layer may or may not be planarized.

If a blanket layer is included, an etchant is utilized to etch a contact opening through the exposed portion of the blanket layer to the etch stop layer. Next, a second etch or etch-stop etch is performed to remove the etch stop layer material from the contact region. The etch-stop etch is also almost completely anisotropic, meaning that the etchant etches in one direction—in this case, vertically (or perpendicular relative to the substrate surface) rather than horizontally. The etch

removes the etch stop insulating layer and retains the substantially rectangular lateral spacer portion of the first insulating layer. The anisotropic etch etches primarily the exposed etch stop material that lies normal to the direction of the etch. Thus, the etch removes the etch stop material covering the area of the contact region but does not significantly etch the etch stop material adjacent to the spacer(s). The etch stop layer on the spacer adds dielectric thickness between the conductive layer and any contacting conductor. In general, the etching conditions utilized for the etch-stop etch have a low selectivity for etching the etch stop layer compared to the underlying insulating material.

The etch-stop etch may be followed by a sputter etch to clean the contact region. Unlike prior art processes whereby the sputter etch erodes the underlying sloping lateral spacer portion of the first insulating layer adjacent to the conducting layer, the sputter etch does not significantly erode the substantially rectangular lateral spacer of the first insulating layer, thus allowing the conductive layer of the device structure to remain completely isolated or insulated by a spacer comprised of the first insulating layer and some etch stop layer material.

The structure contemplated by the invention is an effective device for small feature size structures, particularly self-aligned contacts. The structure consists of first and second conducting layers spaced apart by a region with an area defined in the substrate; an insulating layer encapsulating each conductive layer, wherein the insulating layer includes lateral spacer portions; and an etch stop layer adjacent the insulating layer and over the first and second conducting layers. The invention contemplates that the structure region has a first width between the first and second conducting layers, and a second width between the lateral spacer portions of the insulating layer adjacent to the first and second conducting layers, wherein the region has an aspect ratio of 1.0-2.4. The aspect ratio is defined as the height of the

apparatus relative to the second width of the region. Thus, the invention contemplates larger contact openings for effective contacts, reduced device feature size, and increased device density, while maintaining aspect ratios similar to larger, less dense devices in the prior art. The invention further contemplates that the structure has a minimum insulating layer thickness of 400 Å and that this minimum thickness is determined by the thickness of the insulating layer deposited vertically on the structure.

The device is capable of maintaining high quality, reliable contacts between the conductive material in the contact region and the underlying device region, such as a source or drain, or some other layer or structure. The device contemplates minimum contact opening base widths of 0.2 microns and minimum contact opening widths of 0.5 microns when measured from the top of a planarized layer, and aspect ratios (i.e., height of structure including the etch stop layer relative to the width of the base of a contact opening between the spacers) on the order of 1.0-2.4.

Additional features and benefits of the invention will become apparent from the detailed description, figures, and claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, aspects, and advantages of the present invention will become more thoroughly apparent from the following detailed description, appended claims, and accompanying drawings in which:

Figure 1 is a planar view of a self-aligned contact to diffusion. Figure 1(A) is a planar top view of a self-aligned contact. Figure 1(B) is a cross-sectional planar side view of a self-aligned contact to diffusion through line 1(B) of Figure 1(A). Figure 1(C) is a cross-sectional planar side view of a self-aligned contact to diffusion through line 1(C) of Figure 1(A).

Figure 2 is a cross-sectional side view of the formation of a prior art contact opening formation. Figure 2(A) illustrates a high selectivity etch of an etch stop insulating layer, and Figure 2(B) illustrates the results of that etch.

Figure 3 is a cross-sectional side view of the formation of a prior art contact opening formation during a sputter cleaning etch.

Figure 3 is a cross-sectional view of an example of a semiconductor device during fabrication upon which the invention may be practiced.

Figure 4 presents a cross-sectional planar side view of the preparation of a series of gates on a semiconductor substrate surface.

Figure 4(A) illustrates a cross-sectional planar side view of an insulating layer adjacent to a conducting layer, both layers overlying two diffusion regions.

Figure 4(B) illustrates a cross-sectional planar side view of a series of gates consisting of insulating material adjacent conducting material.

Figure 4(C) illustrates a cross-sectional planar side view of the deposition of additional insulating material over the series of gates, the additional insulating material to be used for the formation of spacer portions adjacent the contact or diffusion regions.

Figure 4(D) illustrates a cross-sectional planar side view of a series of gates completely encapsulated in insulating material wherein the spacers of the insulating material adjacent the contact or diffusion regions have substantially rectangular profiles.

Figure 4(E) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material and an insulating etch stop layer overlying the insulating material.

Figure 4(F) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material and an insulating etch stop layer overlying the insulating material, wherein the diffusion region is implanted to include a silicide.

Figure 4(G) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, and a distinct planarized insulating layer overlying the etch stop layer.

Figure 4(H) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the etch stop layer, and a photoresist patterning layer deposited over the blanket layer.

Figure 4(I) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating

material, a distinct planarized insulating blanket layer overlying the etch stop layer, and contact openings etch through the blanket layer above the diffusion region.

Figure 4(J) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the etch stop layer, and a contact opening to a diffusion region and a second contact opening through the blanket layer but separated from the diffusion region by an etch stop layer.

Figure 4(K) illustrates a close-up cross-sectional planar side view of a circled portion of Figure 4(J), the circled portion labeled 4(K) and illustrating the spacer portion of a contact region following an etch of the etch stop layer from the contact region.

Figure 4(L) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the etch stop layer, and a conductive contact in a contact region extending to a diffusion region in the semiconductor substrate.

DETAILED DESCRIPTION OF THE INVENTION

The invention is a device and a process whereby there is provided a contact opening with a no alignment sensitivity relative to a gate electrode or other structure such that the gate electrode does not fall within the contact opening but remains isolated from the contact opening by an insulating layer. The structure contemplated by the invention is an effective device for small feature size structures, particularly self-aligned contacts, because it is capable of maintaining high quality contacts between the conductive material in the contact region and the underlying device region, such as a source or drain, or some other layer or structure with minimum contact opening base widths (i.e., at the base of the contact openings) of 0.2 microns and minimum contact opening widths of 0.5 microns when measured from the top of a planarized layer, minimum encapsulating layer thicknesses of 400 Å, and aspect ratios (i.e., height of structure including the etch stop layer relative to the width of the base of a contact opening between the spacers) in the range of 1.0-2.4.

In the following description, numerous specific details are set forth such as specific materials, thicknesses, processing steps, process parameters, etc., in order to provide a thorough understanding of the invention. It will be obvious, however, to one skilled in the art that these specific details need not be employed to practice the invention. In other instances, well known materials or methods have not been described in detail in order to avoid unnecessarily obscuring the invention. Furthermore, in the following discussion, several embodiments of the invention are illustrated with respect to specific structures, oxide layers, and oxide layer openings. It will be appreciated that each of the methods described herein can be utilized on a variety of structures and oxide layers, to form any type of opening, and

each of the insulating layer etching methods described herein is not necessarily restricted to the structure and/or insulating layer in conjunction with which it is described. Further, any of the methods described herein may be performed as part of a multistep etch comprising additional etch processes.

Figure 4 presents a cross-sectional view of the preparation of a series of gates or transistors on a semiconductor substrate surface. Referring to Figure 4(A), the semiconductor substrate 400 can be either p- or n-type, and includes diffusion regions 405, such as sources or drains, that are heavily doped with the opposite dopant type of the substrate. An n-type first conducting layer 415 of polysilicon doped by implantation with phosphorous to a resistivity of 50-200 ohms/square is deposited over the diffusion regions. The polysilicon layer 415 is deposited by low pressure CVD ("LPCVD") using an LPCVD tube and SiH_4 gas at 200-400 mtorr with a thickness of 2000-3000 Å. It should be appreciated by those skilled in the art that this conducting layer 415 could instead be a p-type conducting layer or a metallic conductor of, for example, W, Mo, Ta, and/or Ti, or that this conducting layer 320 could also be a silicide, consisting of WSi_2, $MoSi_2$, $TaSi_2$, PtSi, PdSi, or that this conducting layer 320 can further be a layered structure consisting of a silicide on top of doped polysilicon.

The polysilicon layer 415 overlays an insulating dielectric layer 410 such as doped or undoped silicon dioxide. The dielectric layer 410 may comprise a single oxide, or several layers formed by various methods. For example, one or more layers of oxide may be deposited by plasma enhanced chemical vapor deposition ("PECVD"), thermal CVD ("TCVD"), atmospheric pressure CVD ("APCVD"), subatmospheric pressure CVD ("SACVD"), for example utilizing, for example, TEOS and oxygen or TEOS and ozone chemistries. As used herein, reference to, for example, a PECVD TEOS oxide denotes an oxide layer deposited by PECVD utilizing

TEOS chemistry. Additionally, one or more layers of dielectric layer 410 may be a spin-on-glass ("SOG") layer.

A TEOS dielectric layer 420 with a total thickness of approximately 3000 Å overlies the conducting layer 415. It should be appreciated by those of ordinary skill in the art that this TEOS layer 420 could instead be an insulating layer of, for example, silicon dioxide, SiO_2, ONO, silicon nitride (Si_xN_y), or silicon oxynitride (SiO_xN_y). Additionally, the insulating layer 420 may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate ("BPTEOS"). Further, the dielectric layer 420 may comprise a single layer oxide, like TEOS, or several layers formed by various methods.

Referring further to Figure 4(A), a photoresist masking layer 425 is deposited over the TEOS dielectric layer 420. The photoresist masking layer 425 exposes diffusion regions 405 in the semiconductor substrate. Referring to Figure 4(B), a series of photolithographic etches are performed to remove the TEOS layer 420 material and the polysilicon layer 415 from the diffusion or contact regions. The etches are performed using a parallel plate plasma etcher with a power of 200-300 watts. First, a fluorocarbon photolithographic etch, CHF_3/C_2F_6 at 50 mtorr, is performed to remove the insulating TEOS material from areas adjacent to and including the diffusion or contact regions. This is followed by a single polysilicon photolithographic etch using a chlorine plasma (Cl_2/He) to define a polysilicon conducting layer 415 above the transistor or gate regions.

The process described thus far has been described in terms of multiple etching steps involving multiple passes through the etch chamber. It should be recognized

by one of ordinary skill in the art that the etching steps can be combined into a multiple-step etch whereby the etch may be accomplished with one pass through the etch chamber, the etcher changing chemistries and executing the multiple etches sequentially.

Referring to Figure 4(C) and 4(D), spacers are formed between the polysilicon layer 415 of the gates and the contact regions by depositing an additional of conformal layer of TEOS material 430 over the structure and etching spacer portions extending into the contact opening and adjacent to the polysilicon layer 415 approximately 1500 Å in width. The spacer portions 435 of the TEOS layer 430 are demarked by ghost lines in Figure 4(D). The spacers serve to insulate the polysilicon layers 415 from the conducting material that will fill the contact opening and prevent the gates from overlapping the diffusion regions. The spacers 435 serve to completely encapsulate the polysilicon layers 415 of the individual gates. As shown in Figure 4(C), care is taken to etch the spacers 435 such that the spacers 435 have a substantially rectangular profile. This is accomplished using a low bias and high pressure etch (2.8 torr, 140 sccm He, 30 sccm CHF_3, 90 sccm CF_4, and 850 watts power), that results in low polymer formation. At this point, the preferred embodiment of the invention contemplates that the TEOS layer can have a minimum vertical width of approximately 3000 Å and spacers with a minimum width of approximately 1000 Å.

Referring to Figure 4(E), the diffusion regions are next implanted with a suitable dopant utilizing conventional techniques. The dopant may be implants of arsenic, phosphorous, or boron. Subsequently, silicides, for example WSi_2 and $TiSi_2$, may also be formed. Figure 4(E) illustrates silicide formation 445 in the diffusion regions.

Referring to Figure 4(F), overlying the TEOS layer 420 is deposited a second distinct dielectric or etch stop layer 440, in this example, an silicon nitride (Si_xN_y) layer 440, with a total thickness of 700 angstroms. It should again be appreciated by those of ordinary skill in the art that this silicon nitride layer 440 could instead be an insulating layer of, for example, silicon dioxide, SiO_2, ONO, or $SiO_xN_y(H_z)$. Additionally, the silicon nitride etch stop layer 340 may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate ("BPTEOS"). Further, the etch stop layer 440 may comprise a single silicon nitride layer or several layers formed by various methods. It is important that the etch stop layer be different or distinct from the underlying insulating layer.

The invention contemplates that at this point the structure has an aspect ratio of 1.0-2.4. As used herein, an aspect ratio is defined as the ratio of the height of a contact opening to the top of the horizontal portion of the etch stop layer to the base width of the contact opening between the insulating spacers. For example, an embodiment of the invention contemplates contact opening heights of 5300 Å (0.53 µm) relative to widths of 0.32 µm to give aspect ratios of 1.6.

Referring to Figure 4(G), an optional dielectric blanket layer 450 is next deposited adjacent to the etch stop layer 440. The blanket layer 450 may or may not be planarized. In Figure 4(G), the blanket layer 450 is planarized. The planarized blanket layer 450 facilitates the formation of an interconnect layer that might later be deposited over the contact regions. The blanket layer in Figure 4(G) is a doped silicate glass, for example BPTEOS. It should be appreciated by those of ordinary skill in the art that this BPTEOS layer 450 could instead be another doped insulating layer of, for example, BPSG or PSG, or an undoped insulating layer of silicon dioxide,

SiO_2, ONO, or SiO_xN_y. Further, the blanket layer 450 may comprise a single oxide, like BPTEOS, or several layers formed by various methods.

Next, as shown in Figure 4(H), a photoresist pattern or mask layer is deposited adjacent to the blanket layer such that the contact regions overlying the diffusion regions are exposed. This is followed by a photolithographic etch of the BPTEOS blanket layer 450 in the contact regions. The etch is a fluorocarbon photolithographic etch (7 sccm CHF_3, 6 sccm Freon 134a) at 29 mtorr. The etch reveals a pair of contact regions 460 and 465 above the diffusion regions.

Referring to Figure 4(J), a photoresist material 470 is overlayed in contact opening 465 adjacent to the etch stop layer to protect the etch stop material in contact opening 465 from a subsequent photolithographic etch to remove the etch stop layer. Next, a photolithographic etch, (900 mtorr, 100 sccm, He, 85 sccm C_2F_6, and 225 watts power using a Lam 4400 Series plasma etching system) is performed to remove the etch stop layer 440 from contact opening 460. The etch conditions for this etch are low bombardment/high neutral flux conditions.

Figure 4(K) is a close-up view of the cross-sectional portion of contact opening 460 in Figure 4(J). The etch proceeds anisotropically, primarily removing etch stop material lying in a horizontal plane relative to the vertical direction of the etchant ions. The etchant removes material primarily from the base of the contact region 460, and does not remove all of the etch stop material adjacent to the spacer portion of the TEOS layer 420. Thus, the remaining etch stop material adjacent to the spacer portion of the TEOS layer serves as additional spacer material to insulate the polysilicon from a conductive contact that will subsequently be added to the contact region 460.

The etchant utilized to remove silicon nitride from the contact region 460 has a low selectivity for etching the silicon nitride material compared to the underlying TEOS layer. The use of an etchant with a low selectivity for silicon nitride relative to TEOS does not significantly destroy the TEOS layer 420 spacer portion. The low selectivity etch yields a TEOS layer 420 spacer portion that retains a rectangular or "boxy" profile. Figure 4(K) illustrates that only a small portion 475 (illustrated in ghost lines) of the TEOS layer 420 spacer portion is removed during the etch. Of primary significance, the spacer portion of the TEOS layer 420 retains its substantially rectangular profile.

It is to be appreciated that the described etch stop layer etch conditions (i.e., low selectivity, low bombardment/high neutral flax) are exemplary of etch conditions that result in the retention of a boxy spacer. The invention relates to these process conditions as well as others that result in the retention of a boxy spacer. Thus, the etch-stop etch conditions should be regarded in an illustrative rather than restrictive sense.

The silicon nitride etch stop layer 440 etch is followed by a sputter etch to clean the contact opening 460. In a currently preferred embodiment, the sputter etch is carried out in an atmosphere of argon, a 8 mtorr pressure, with a 1000 volt bias. In a currently preferred embodiment, the sputter etch is carried out in a commercially available system such as the Applied Materials Endura 5500 systems. Alternatively, any system having a sputter etch mode may be used to practice the invention. As will be appreciated by a person of ordinary skill in the art, the parameters can be varied considerably while still achieving the objects of the invention. In a currently preferred embodiment, the etch is designed to etch approximately 200 Å per minute as measured on thermal oxide. Because of the retention of a substantially

rectangular or "boxy" spacer portion, the sputter etch does not significantly erode the spacer portion of the TEOS layer.

At this point, the invention contemplates that the minimum encapsulating dielectric layer, i.e., TEOS, thickness will be approximately 400 Å and that this minimum thickness will be at the corner most effected by the etch-stop layer etch and the sputter etch. In Figure 4(K) that minimum thickness is the diagonal denoted *d*.

Figure 4(L) presents a cross-sectional planar side view of the structure of the invention wherein a conductive contacts 480 have been deposited in the contact openings 460.

The process described above yields a structure wherein first and second conductive layers (e.g., polysilicon layers) are separated by a contact region with an area defined in the semiconductor substrate. An insulating layer is adjacent to and encapsulates the first and second conductive layers. The invention contemplates that the insulating layer has spacer portions between the conductive layers and the contact region. The invention contemplates that high quality contacts can be achieved wherein the spacer portions have a minimum insulative material thickness of 400 Å. In the preferred embodiment, the spacer portions of the insulating material further have substantially rectangular profiles. The invention also contemplates that a portion of the etch stop layer material may remain adjacent to the spacer portion of the insulating layer following an anisotropic etch of the etch stop material with a low selectivity etch for the etch stop material relative to the insulating layer material. The result is a contact opening with spacer sidewalls comprised, at least potentially, of a portion of etch stop layer material.

The invention contemplates that effective contact openings may have base widths as small as 0.2 μm (and as small as 0.5 μm when measured from the top of the optional planarized layer), and base areas as small as 0.1 μm^2. Thus, the invention contemplates aspect ratios for effective contact openings of 1.0-2.4, wherein an aspect ratio is defined as the ratio of the height of a contact opening to the top of the horizontal portion of the etch stop layer to the base width of the contact opening between the spacers. Figure 4(L) illustrates a height, h , and a width, w, from which an aspect ratio may be calculated for a contact region, and a height $h1$, and a width, $w1$, from which an aspect ratio may be calculated for a contact region.

In the preceding detailed description, the invention is described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A process for minimizing lateral spacer erosion on a contact region, said process comprising:

encapsulating a conducting layer in an insulating layer on said semiconductor body adjacent said contact region, wherein said insulating layer includes a substantially rectangular spacer portion adjacent said contact region;

depositing an etch stop layer adjacent said insulating layer and adjacent said contact region; and

etching a portion of said etch stop layer adjacent said contact region wherein said etching does not significantly erode said spacer portion of said insulating layer.

2. The process of claim 1, wherein said etching step utilizes a plasma etching system.

3. The process of claim 2, wherein an etching condition for said etching step is a low bombardment/high neutral flux condition.

4. The process of claim 3, wherein said etching condition has a low selectivity for said etch stop layer material relative to said first insulating layer material.

5. The process of claim 4, wherein said selectivity is less than or equal to 1:1.

6. The process of claim 2, wherein said plasma etching system is a Lam 4400 Series plasma etching system.

7. The process of claim 6, wherein said etch stop layer etch is performed using a recipe of 900 mtorr, 100 sccm He, 85 sccm C_2F_6, and 225 watts power.

8. The process of claim 1, including cleaning said exposed portion of said first insulating layer with a sputter etch after said etching of said etch stop layer wherein said spacer portion of said first insulating layer retains its substantially rectangular profile.

9. The process of claim 8, wherein said sputter etch is a radio-frequency sputter etch.

10. The process of claim 1, including depositing a blanket insulating layer adjacent said etch stop layer, forming a patterning layer on said blanket insulating layer wherein said patterning layer exposes said contact region, and etching a portion of said blanket insulating layer over said contact region with a suitable etchant to expose a portion of said etch stop layer prior to said etching of said etch stop layer.

11. The process of Claim 10, wherein the blanket layer is planarized.

12. A process for minimizing lateral spacer erosion on a contact region, said process comprising:

encapsulating a conducting layer in an insulating layer on said semiconductor body adjacent said contact region, wherein said insulating layer includes a substantially rectangular spacer portion adjacent said contact region;

depositing an etch stop layer adjacent said insulating layer and adjacent said contact region; and

etching a portion of said etch stop layer adjacent said contact region wherein said etching delivers a minimal diagonal erosion rate of said spacer portion relative to the vertical erosion rate of said insulating layer.

13. The process of claim 12, wherein said etching step utilizes a plasma etching system.

14. The process of claim 13, wherein an etching condition for said etching step is a low bombardment/high neutral flux condition.

15. The process of claim 14, wherein said etching condition has a low selectivity for said etch stop layer material relative to said first insulating layer material.

16. The process of claim 15, wherein said selectivity is less than or equal to 1:1.

17. The process of claim 13, wherein said plasma etching system is a Lam 4400 series plasma etching system.

18. The process of claim 17, wherein said etch stop layer etch is performed using a recipe of 900 mtorr, 100 sccm He, 85 sccm C_2F_6, and 225 watts power.

19. The process of claim 12, including cleaning said exposed portion of said first insulating layer with a sputter etch after said etching of said etch stop layer wherein said spacer portion of said first insulating layer retains its substantially rectangular profile.

20. The process of claim 19, wherein said sputter etch is a radio-frequency sputter etch.

21. The process of claim 12, including depositing a blanket insulating layer adjacent said etch stop layer, forming a patterning layer on said blanket insulating layer wherein said patterning layer exposes said contact region, and etching a portion of said blanket insulating layer over said contact region with a suitable etchant to expose a portion of said etch stop layer prior to said etching of said etch stop layer.

22. The process of Claim 21, wherein the blanket layer is planarized.

23. A semiconductor apparatus comprising:

first and second conducting layers spaced apart by a region with an area defined in the substrate;

an insulating layer adjacent said first and second conductive layers; and

an etch stop layer adjacent said insulating layer and over said first and second conducting layers, and a second width between said insulating layer adjacent said first and second conducting layers, and wherein said region has an aspect ratio of 1.0-2.4 said aspect ratio defined as the height of said apparatus relative to the second width of said region.

24. The semiconductor apparatus of claim 23, wherein said insulating layer has a spacer portion adjacent said region wherein said spacer portion has a substantially rectangular profile.

25. The semiconductor apparatus of claim 23, wherein said etch stop layer is silicon nitride.

26. The semiconductor apparatus of claim 23, wherein said etch stop layer is silicon dioxide.

ABSTRACT

A process for minimizing lateral spacer erosion of an insulating layer adjacent to a contact region and an apparatus whereby there is provided a contact opening with a small alignment tolerance relative to a gate electrode or other structure are disclosed. The process includes the steps of forming a conductive layer on said semiconductor body then depositing an insulating layer adjacent to the conductive layer. Next, substantially rectangular insulating spacers are formed adjacent to the gate. An etch stop layer is deposited adjacent said insulating layer followed by an etch to remove the etch stop layer material from the contact region. This etch is conducted under conditions wherein the etch removes the etch stop layer but retains the substantially rectangular lateral spacer profile of the first insulating layer. The apparatus is capable of maintaining high quality contacts between the conductive material in the contact region and the underlying device region, such as a source or drain, or some other layer or structure and is an effective structure for small feature size structures, particularly self-aligned contact structures.