

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD.,  
Petitioner,

v.

DSS TECHNOLOGY MANAGEMENT, INC.,  
Patent Owner.

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Case IPR2016-00782  
Patent 6,784,552 B2

Before BRYAN F. MOORE, BRIAN J. McNAMARA, and  
MINN CHUNG, *Administrative Patent Judges*.

CHUNG, *Administrative Patent Judge*.

DECISION  
Institution of *Inter Partes* Review  
*37 C.F.R. § 42.108*

## I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–12 (the “challenged claims”) of U.S. Patent No. 6,784,552 B2 (Ex. 1001, “the ’552 patent”). DSS Technology Management, Inc. (“Patent Owner”) did not file a Preliminary Response. We have jurisdiction under 35 U.S.C. § 314.

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons described below, we conclude Petitioner has established a reasonable likelihood of prevailing in showing the unpatentability of claims 1–12. Accordingly, we institute an *inter partes* review of claims 1–12 of the ’552 patent.

### A. *Real Parties In Interest*

Petitioner identifies itself as the only real party-in-interest. Pet. 2.

### B. *Related Proceedings*

According to Petitioner, the ’552 patent is the subject of the following patent infringement cases: *DSS Tech. Mgmt., Inc. v. Samsung Elec. Co., Ltd.*, Case No. 15-cv-690 (E.D. Tex.); *DSS Tech. Mgmt., Inc. v. Intel, Corp.*, Case No. 15-cv-130 (E.D. Tex.); *DSS Tech. Mgmt., Inc. v. SK Hynix, Inc.*, Case No. 15-cv-691 (E.D. Tex.); and *DSS Tech. Mgmt., Inc. v. Qualcomm, Inc.*, Case No. 15-cv-692 (E.D. Tex.). *Id.*

*C. The '552 Patent*

The '552 patent describes a process of semiconductor device fabrication and a structure of a semiconductor device having “substantially rectangular” lateral insulating spacers adjacent to gate electrodes. Ex. 1001, Abstract. The '552 patent defines the term “substantially rectangular” to mean that “a side of the spacer has an angle relative to the substrate surface of more than 85°.” *Id.* at col. 8, ll. 40–42. Figure 4(D) of the '552 patent is reproduced below.

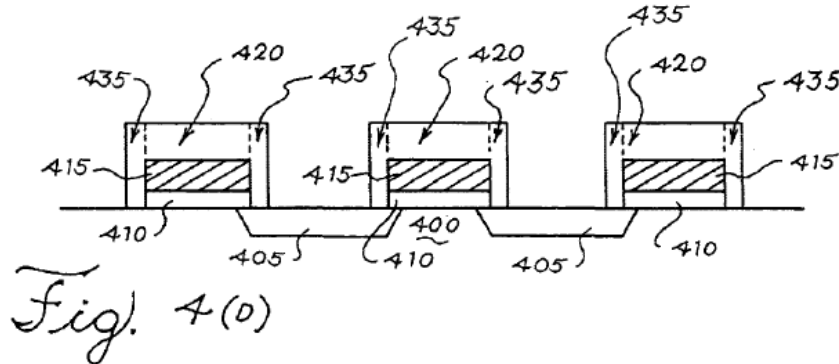


Figure 4(D) illustrates a cross-sectional view of a series of gates 415 (also called conducting layers or polysilicon layers) completely encapsulated in insulating material 420, e.g., TEOS (tetraethyl orthosilicate glass), where spacers 435 of the insulating material adjacent to the gates have substantially rectangular profiles. *Id.* at col. 9, ll. 9–13; col. 11, ll. 40–46. As shown in Figure 4(D), gates 415 are insulated from sources or drains 405 by insulating dielectric layers 410. *See id.* at col. 10, ll. 49–50. The '552 patent describes a process of making high quality contacts to the sources or drains, such as “self-aligned” contacts, by etching structures over substrate 400 and sources or drains 405. *Id.* at col. 7, ll. 19–22; col. 8, ll. 4–6.

Figure 4(I) of the '552 patent is reproduced below.

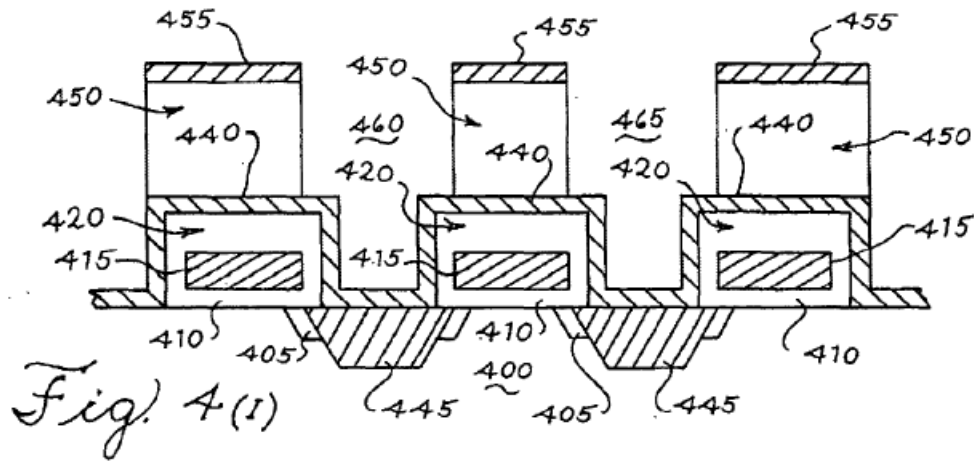
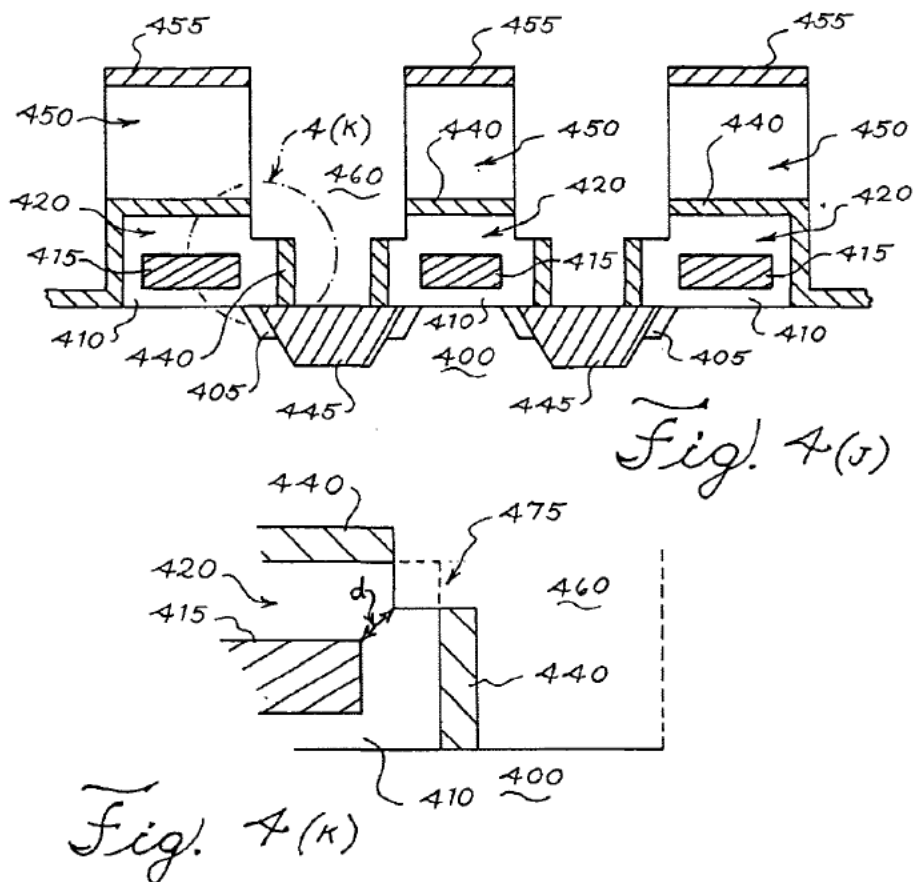


Figure 4(I) illustrates additional structures deposited and etched over the structure described in Figure 4(D), such as second dielectric layer 440 (called etch stop layer), blanket layer 450, and photoresist mask layer 455. *Id.* at col. 9, ll. 33–39; col. 11, ll. 63–65; col. 12, ll. 34–42. According to the '552 patent, etch stop layer 440, e.g., silicon nitride layer 440, depicted in Figure 4(I) is distinct or different from the underlying TEOS insulating layer. *Id.* at col. 12, ll. 10–11. The etch stop layer protects the underlying TEOS layer when blanket layer 450 made of BPTEOS<sup>1</sup> is etched away to create contact openings 460 and 465 above source or drain 445. *See id.* at col. 12, ll. 36–42; col. 4, ll. 41–59.

A second etch is then performed to remove etch stop layer 440 covering source or drain 445 in contact openings 460 and 465. *Id.* at col. 12, ll. 48–52; col. 7, ll. 43–45. The '552 patent describes that the second etch is

<sup>1</sup> BPTEOS is an acronym for borophosphosilicate tetraethyl orthosilicate glass. *See Ex. 1001*, col. 11, ll. 6–7.

“almost completely anisotropic,” which means that the etchant etches in the vertical direction, or perpendicular relative to the substrate surface. *Id.* at col. 7, ll. 45–48; col. 12, ll. 55–58. Hence, the etch removes the etch stop material covering the area of the contact openings or contact regions 460 and 465, but does not significantly etch the etch stop material adjacent to the spacer portions 435. *Id.* at col. 7, ll. 53–55; col. 12, ll. 58–61. Figures 4(J) and 4(K) of the ’552 patent are reproduced below.



Figures 4(J) and 4(K) illustrate the structure of the semiconductor device of the ’552 patent after the second etch for removing the etch stop layer from the contact regions 460 and 465 is completed. As shown in Figures 4(J) and

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