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Paper 18
Entered: September 20, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

DSS TECHNOLOGY MANAGEMENT, INC.,
Patent Owner.

Case IPR2016-00782
Patent 6,784,552 B2

Before BRYAN F. MOORE, BRIAN J. McNAMARA, and MINN CHUNG, *Administrative Patent Judges.*

CHUNG, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. BACKGROUND

A. Introduction

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Samsung Electronics Co., Ltd. ("Petitioner") challenges the patentability of claims 1–12 (the "challenged claims") of U.S. Patent No. 6,784,552 B2 (Ex. 1001, "the '552 patent"), owned by DSS Technology Management, Inc. ("Patent Owner"). The Board has jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. With respect to the grounds instituted in this trial, we have considered the papers submitted by the parties and the evidence cited therein. For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1–12 of the '552 patent are unpatentable.

B. Procedural History

On March 18, 2016, Petitioner filed a Petition (Paper 1, "Pet.") requesting an *inter partes* review of claims 1–12 (the "challenged claims") of U.S. Patent No. 6,784,552 B2 (Ex. 1001, "the '552 patent"). Petitioner also filed the Declaration of Dr. Richard Fair (Ex. 1003, "Fair Decl.") in support of the Petition. Patent Owner did not file a Preliminary Response. On September 23, 2016, we instituted an *inter partes* review of claims 1–12 of the '552 patent based on the following specific grounds (Paper 6, "Dec. on Inst.," 27).

Claim(s) Challenged	Statutory Basis	Reference(s)
1, 2, 4–12	§ 102(b)	Kuesters[1]
3	§ 103(a)	Kuesters and Havemann[2]
1, 2, 4–7	§ 103(a)	Kuesters and Heath[3]
3	§ 103(a)	Kuesters, Heath, and Havemann

After institution, Patent Owner filed a Patent Owner Response (Paper 10, "PO Resp."), to which Petitioner filed a Reply (Paper 12, "Pet. Reply"). Petitioner also filed the Declaration of Dr. Richard Fair in Support of Petitioner's Reply (Ex. 1014, "Fair Reply Decl."). An oral hearing was held on June 20, 2017. A transcript of the hearing is included in the record as Paper 17 ("Tr.").

C. Related Proceedings

According to the parties, the '552 patent is the subject of the following patent infringement cases: *DSS Tech. Mgmt., Inc. v. Samsung Elec. Co., Ltd.*, Case No. 15-cv-690 (E.D. Tex.); *DSS Tech. Mgmt., Inc. v. Intel, Corp.*, Case No. 15-cv-130 (E.D. Tex.); *DSS Tech. Mgmt., Inc. v. SK Hynix, Inc.*, Case No. 15-cv-691 (E.D. Tex.); and *DSS Tech. Mgmt., Inc. v. Qualcomm, Inc.*, Case No. 15-cv-692 (E.D. Tex.). Pet. 2; Paper 5, 2–3.

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[1] Kuesters et al., *Self Aligned Bitline Contact For 4 Mbit dRAM*, PROCEEDINGS OF THE FIRST INTERNATIONAL SYMPOSIUM ON ULTRA LARGE SCALE INTEGRATION SCIENCE AND TECHNOLOGY 640–49 (1987) ("Kuesters") (Ex. 1005).

[2] U.S. Patent No. 5,482,894 (Jan. 9, 1996) ("Havemann") (Ex. 1006).

[3] U.S. Patent No. 4,686,000 (Aug. 11, 1987) ("Heath") (Ex. 1007).

The ’552 patent was also the subject of instituted trial proceedings *Intel Corp. v. DSS Tech. Mgmt., Inc.*, Cases IPR2016-00287 and IPR2016-00288, in which we have entered final written decisions finding all of the claims of the ’552 patent unpatentable.[4] *Intel Corp. v. DSS Tech. Mgmt., Inc.*, Cases IPR2016-00287 and IPR2016-00288 (PTAB June 1, 2017) (Paper 25 in both cases). Patent Owner has timely filed a Notice of Appeal in each of Cases IPR2016-00287 and IPR2016-00288 (Paper 28 in each case).

II. THE ’552 PATENT

A. Described Invention

The ’552 patent describes a process of semiconductor device fabrication and a structure of a semiconductor device having “substantially rectangular” lateral insulating spacers adjacent to gate electrodes. Ex. 1001, Abstract. The ’552 patent defines the term “substantially rectangular” to mean that “a side of the spacer has an angle relative to the substrate surface of more than 85°.” *Id.* at col. 8, ll. 40–42. Figure 4(D) of the ’552 patent is reproduced below.

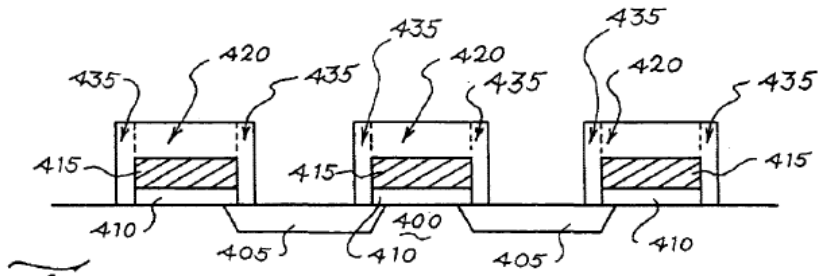

Fig. 4(D)

[4] Cases IPR2016-01311 and IPR2016-01314 have been joined with IPR2016-00287 and IPR2016-00288, respectively.

Figure 4(D) illustrates a cross-sectional view of a series of gates 415 (also called conducting layers or polysilicon layers) completely encapsulated in insulating material 420, e.g., TEOS (tetraethyl orthosilicate glass), where spacers 435 of the insulating material adjacent to the gates have substantially rectangular profiles. *Id.* at col. 9, ll. 9–13; col. 11, ll. 40–46. As shown in Figure 4(D), gates 415 are insulated from sources or drains 405 by insulating dielectric layers 410. *See id.* at col. 10, ll. 49–50. The '552 patent describes a process of making high quality contacts to the sources or drains, such as "self-aligned" contacts, by etching structures over substrate 400 and sources or drains 405. *Id.* at col. 7, ll. 19–22; col. 8, ll. 4–6.

Figure 4(I) of the '552 patent is reproduced below.

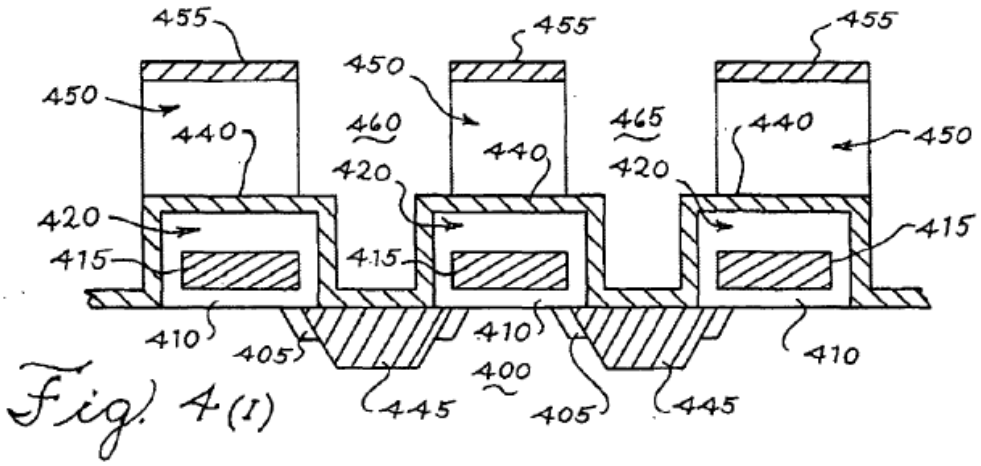

Fig. 4(I)

Figure 4(I) illustrates additional structures deposited and etched over the structure described in Figure 4(D), such as second dielectric layer 440 (called etch stop layer), blanket layer 450, and photoresist mask layer 455. *Id.* at col. 9, ll. 33–39; col. 11, ll. 63–65; col. 12, ll. 34–42. According to the '552 patent, etch stop layer 440, e.g., silicon nitride layer 440, depicted in Figure 4(I) is distinct or different from the underlying TEOS insulating

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