UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. Petitioner

v.

DSS TECHNOLOGY MANAGEMENT, INC. Patent Owner

Case IPR. No. **2016-00782**U.S. Patent No. 6,784,552
Title: STRUCTURE HAVING REDUCED LATERAL SPACER EROSION

REPLY TO PATENT OWNER'S RESPONSE TO PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 6,784,552

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Exhibit List

Samsung Exhibit #	Description
SAMSUNG- 1001	U.S. Patent No. 6,784,552 ("552 Patent")
SAMSUNG- 1002	File History for U.S. Patent No. 6,784,552
SAMSUNG- 1003	Declaration of Dr. Richard Fair ("Fair Decl.")
SAMSUNG- 1004	Curriculum Vitae of Richard Fair
SAMSUNG- 1005	Kuesters et al., "Self Aligned Bitline Contact For 4 Mbit dRAM," Proceedings of the First International Symposium on Ultra Large Scale Integration Science and Technology, 1987, pp. 640-649 ("Kuesters")
SAMSUNG- 1006	U.S. Patent No. 5,482,894 ("Havemann")
SAMSUNG- 1007	U.S. Patent No. 4,686,000 ("Heath")
SAMSUNG- 1008	File History for U.S. Patent No. 6,066,555
SAMSUNG- 1009	Joint Claim Construction Statement, DSS Tech. Mgmt., Inc. v. Intel Corp. et al., 15-cv-130 (E.D. Tex. 2015) (Dkt. No. 165-1)
SAMSUNG- 1010	Declaration of Mariellen F. Calter
SAMSUNG- 1011	Sorab K. Ghandhi, VLSI Fabrication Principles Silicon and Gallium Arsenide 495-96 (John Wiley & Sons, 1983)



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