

EXHIBIT A

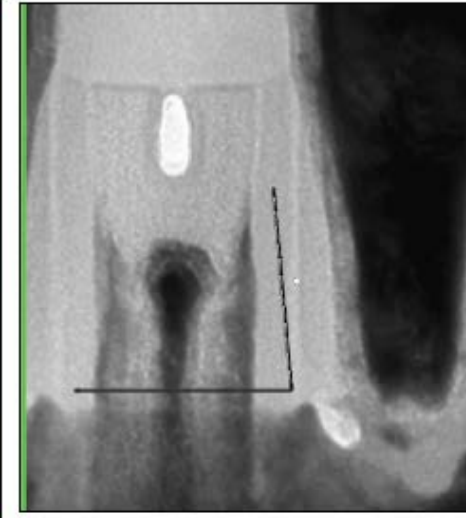
Parties' Proposed Claim Constructions for Claim Terms in U.S. Patent 6,784,552

Claim Term	Plaintiff's Proposed Construction and Support	Defendants' Proposed Construction
<p>“an etch stop material over said first insulating layer” (claim 1)</p>	<p>“an etch stop material around or above said first insulating layer”</p> <p>Generally, an etch stop material has an etch rate that is relatively higher than an adjacent or underlying material exposed to a specific etch process and may prevent etching of the adjacent or underlying material.</p> <p>Abstract; 4:12-17; 12:54-13:20; 13:58-52; 14:10-17; Fig. 4K; Fig. 4L; Claims</p> <p>US 6,004,875</p> <p>Merriam Webster's Collegiate Dictionary (10th Ed. 1994) (“over”)</p>	<p>“a material overlying the first insulating effectively etched by the etchant used to region”</p> <p><u>Specification:</u></p> <p>“A distinct dielectric etch stop layer 125 encapsulating dielectric layer 120. The etch stop layer 125 permits subsequent etching of the substrate 110, exposing the device structures and layers 115. The device structuring and layers are protected from etching by the etch stop layer 125.” ('552 patent 18.)</p> <p>“The etchant utilized to make the opening 270 has selectivity toward BPTEOS relative to silicon nitride. When the contact opening 270 was formed through the BPTEOS material, the etchant did not etch the silicon nitride. Hence, the description of the silicon nitride layer 240 as an etch stop layer. The silicon nitride stop layer 240 protected the underlying TEOS layer 235 and spacer portion 235 so that the polysilicon layer 235 is completely encapsulated.” ('552 patent 18.)</p> <p>“A distinct insulating layer, for example an etch stop layer 340, overlies the TEOS layer 330. The etch stop layer 340 is covered by a third</p>

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		<p>for example a BPTEOS blanket layer 35:46-50.)</p> <p>“FIG. 4(F) illustrates a cross-sectional planar view of a series of gates encapsulated with insulating material, an insulating etch stop layer overlying the insulating material. FIG. 4(G) illustrates a cross-sectional planar view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, and a distinct planarized insulating layer overlying the etch stop layer. FIG. 4(H) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material. . . . FIG. 4(I) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material. . . . FIG. 4(L) . . .” (9:19-56.)</p> <p>“Referring to FIG. 4(F), overlying the TEOS layer, a second dielectric or dielectric layer 440, in this example, a silicon nitride (Si₃N₄) layer, is deposited with a total thickness of 700 angstroms.” (11:63-66.)</p>
<p>“a side of the insulating spacer has an angle relative to the substrate surface that is either a right</p>	<p>Plain and ordinary meaning.</p> <p>Abstract; 12:66-13:18; 13:29-35; 14:10-17; Figs. 4D, 4K, 4L; Claims</p> <p>3/3/03 Amendment and Request for Reconsideration</p>	<p>“a side of the insulating spacer has an angle relative to the horizontal substrate surface that is greater than or equal to 90°”</p> <p><u>Specification:</u></p>

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angle or an acute angle of more than 85° (claim 1)		Fig. 2(A) Fig. 2(B) Fig. 4(K) “FIG. 2(B) shows that the silicon nitride effectively removed silicon nitride layer contact opening 270. The selective etch compared to TEOS material, however, le 230 with a spacer portion 235 wherein th 235 is sloping or tapered toward the cont This result follows even where the space originally substantially rectangular as in properties of the highly selective etch of stop layer 240 will transform a substanti spacer into a sloped spacer. FIG. 2(B) p polysilicon layer 220 encapsulated in a T with a spacer portion 235 adjacent to the 270, the spacer portion 235 having an an than 85°.” (’552 patent at 5:4-17.) “The use of an etchant with a low selecti nitride relative to TEOS does not signific TEOS layer spacer portion 435. The low yields a TEOS layer spacer portion 435 t rectangular or “boxy” profile. FIG. 4(K) only a small portion 475 (illustrated in g TEOS layer spacer portion 435 is remov Of primary significance, the spacer porti TEOS layer 420 retains its substantially

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		<p>profile.” ('552 patent at 13:2-10.)</p> <p>“The phrase ‘substantially rectangular’ means that the spacer has an angle relative to the substrate surface of more than 85°.” ('552 patent at 8:41-43).</p> <p>“Etchants that provide a near 90° sidewall are generally not highly selective while high aspect ratio etchants typically produce a sloped sidewall.” ('552 patent at 5:56.)</p> <p><u>File History:</u></p> <p>“Dennison, et al. describes a method of forming a capacitor over a capacitor array of memory cells. . . . Figure 2 shows a spacer. This portion of the spacer is reproduced below. As illustrated, the spacer is not a rectangular portion, and is not substantially rectangular.” (File History, Amendment, Feb. 6, 2004 at 5.)</p> <p><u>DSS's Infringement Contentions:</u></p>

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		 <p data-bbox="1128 1287 1624 1423">(DSS' Infringement Contentions, Exhibi <i>also id.</i> at 6 (“The sidewall spacer is ste shown reference angle of 85°, shown in l insulating spacer below.”).)</p>
<p data-bbox="228 1457 370 1591">“insulating spacer” (claim 1)</p>	<p data-bbox="448 1457 1094 1591">Plain and ordinary meaning. Abstract; 4:34-56; 13:51-65; 14:10-17; Figs. 4D, 4K, 4L; Claims</p>	<p data-bbox="1128 1457 1624 1528">“lateral spacer that electrically isolates th from the contact region”</p> <p data-bbox="1128 1556 1308 1591"><u>Specification:</u></p> <p data-bbox="1128 1619 1295 1654">Fig. 4(B)-(D)</p> <p data-bbox="1128 1682 1624 1791">“The invention contemplates that the ins spacer portions between the conductive l contact opening.” (’552 patent at 13:51-5</p>

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