Class	Subclass	ISSUE CLASSIFICATION
438	634	

6066555

UTILITY SERIAL NUMBER 08/577751	PATENT DATE MAY 2 3 2000	PATENT NUMBER 6066555

SERIAL NUMBER	FILING DATE	CLASS	SUBCLASS	GROUP ART UNIT	EXAMINER
08/577,751	12/22/95	~~257~~ 438 ~~437~~	634 ~~195~~	~~2508~~ ~~1104~~ 2812	Gurley

APPLICANTS
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CONTINUING DATA*******************
VERIFIED NONE

FOREIGN/PCT APPLICATIONS**********
VERIFIED NONE

CPA

APPLICATION HAS BECOME ABANDONED
THIS NOTICE MAILED:

Not aband'd

FOREIGN FILING LICENSE GRANTED 05/22/96

Foreign priority claimed / 35 USC 119 conditions met / Verified and Acknowledged / Examiner's initials	AS FILED	STATE OR COUNTRY	SHEETS DRWGS.	TOTAL CLAIMS	INDEP. CLAIMS	FILING FEE RECEIVED	ATTORNEY'S DOCKET NO.
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TITLE
METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

U.S. DEPT. OF COMM./ PAT. & TM—PTO-436L (Rev.12-94)

PARTS OF APPLICATION FILED SEPARATELY — Applications Examiner

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
2-3-00	Assistant Examiner	Total Claims 28	Print Claim 1

ISSUE FEE			DRAWING		
Amount Due $1210.00	Date Paid 3/27/00	John F. Niebling, Supervisory Patent Examiner, Technology Center 2800 — Primary Examiner	Sheets Drwg. 8	Figs. Drwg. 18	Print Fig. 4J, 4L

Label Area

PREPARED FOR ISSUE

ISSUE BATCH NUMBER H73

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Form PTO-436A
(Rev. 8/92)

ISSUE FEE IN FILE

Formal Drawings (___shts) set___

(FACE)

08/577751

PATENT APPLICATION

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INITIALS ______

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APPLICATION HAS BEEN ABANDONED THIS NOTICE MAILED

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5-11-98	18.	PTOL-303	May 27, 1998
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33 5/1/00 Formal Drawings 8 sht(s) set 3/14/00

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SEARCHED

Class	Sub.	Date	Exmr.
437	195 190	2/28/97	J.G.
438	595 634 639	11/21/97	J.G.
438	637 738 740	9/14/98	J.G.
Updated	Search	7/16/98	J.G.
"	"	5/10/99	"
"	"	2/2/2000	"

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
438	634 637 639 738 740	2/2/2000	J.G.

SEARCH NOTES

	Date	Exmr.
APS (USPAT)	2/28/97	J.G.

(RIGHT OUTSIDE)

PATENT NUMBER	ORIGINAL CLASSIFICATION				
	CLASS 438	SUBCLASS 634			
APPLICATION SERIAL NUMBER 08/577,751	CROSS REFERENCE(S)				
	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)			
APPLICANT'S NAME (PLEASE PRINT) Nulty et al.	438	639	639	738	740
IF REISSUE, ORIGINAL PATENT NUMBER					

INTERNATIONAL CLASSIFICATION						
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	PRIMARY EXAMINER (PLEASE STAMP OR PRINT FULL NAME)
	John F. Niebling

PTO 270 (REV. 5-91)

ISSUE CLASSIFICATION SLIP

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POSITION		ID NO.	DATE
CLASSIFIER		18	2/7/96
EXAMINER		313	3-3-96
TYPIST		343	5/22/96
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SPEC. HAND			
FILE MAINT.			
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INDEX OF CLAIMS

Claim Final	Claim Original	Date 11/?/96	Date 3/?/97	Date 11/21/97	Date 5/6/98	Date 9/14/98	Date 7/6/99	Date 3/?/2000	
	1	+	✓						
2	2			✓	✓	✓	✓	=	
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SYMBOLS

- ✓ .... Rejected
- = ... Allowed
- \- (Through numberal) Canceled
- \+ .... Restricted
- N .... Non-elected
- I .... Interference
- A .... Appeal
- O .... Objected

(LEFT INSIDE)

PATENT APPLICATION SERIAL NO. 08/577751

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

230 PS 01/22/96 08577751
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08/577751
16820.P097

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Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

1-00
EtAl

Inventor(s): James E. Nulty, Christopher J. Petti

For: **METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING**

Enclosed are:

XXX   8 sheet(s) of Formal/Informal Drawing(s) including 15 figures.
____ An Assignment of the invention to: ____________________
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____ A Declaration and Power of Attorney.
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Basic Fee:	-	-	-	$375.00	-	$750.00
Total Claims:	26	6	x $11.00		x $22.00	132.00
Indep. Claims:	3	0	x $39.00		x $78.00	0
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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 12/22/95

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Sir:

Transmitted herewith for filing is the patent application of:

Inventor(s): James E. Nulty, Christopher J. Petti

For: **METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING**

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For:	No. Filed	No. Extra	RATE	FEE	RATE	FEE
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☐ Multiple Dep. Claim(s) Presented			+ $125.00		+ $250.00	
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Respectfully submitted,

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12/22/95
Tom Schaffer *Date*

Our Reference: 16820.P097

APPLICATION FOR UNITED STATES PATENT

FOR

METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Inventors: JAMES E. NULTY
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Prepared by:

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[signature] 12/22/95

Name Date

SAMSUNG-1008.009

8 882-97 08/577751

BACKGROUND OF THE INVENTION

Field of the Invention:

The invention relates to semiconductor device processes, and more particularly, to improved methods for etching openings in insulating layers and a
5 semiconductor device with well defined contact openings.

Background of the Invention

In the fabrication of semiconductor devices, numerous conductive device regions and layers are formed in or on a semiconductor substrate. The conductive regions and layers of the device are isolated from one another by a dielectric.
10 Examples of dielectrics include silicon dioxide, SiO_2, tetraethyl orthosilicate glass ("TEOS"), silicon nitrides, Si_xN_y, silicon oxynitrides, $SiO_xN_y(H_z)$, and silicon dioxide/silicon nitride/silicon dioxide ("ONO"). The dielectrics may be grown, or may be deposited by physical deposition (e.g., sputtering) or by a variety of chemical deposition methods and chemistries (e.g., chemical vapor deposition ("CVD")).
15 Additionally, the dielectrics may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate glass ("BPTEOS").

At several stages of the fabrication of semiconductor devices, it is necessary to
20 make openings in the dielectric to allow for contact to underlying regions or layers. Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and ~~the~~ a first metal layer is called a "contact opening", while an opening in other oxide layers such as an opening through an intermetal dielectric layer is referred to as a "via". For purposes

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of the claimed invention, henceforth "contact opening" or "contact region" will be used to refer to contact openings and/or via. The opening may expose a device region within the silicon substrate, such as a source or drain, or may expose some other layer or structure, for example, an underlying metallization layer, local
5 interconnect layer, or structure such as a gate. After the opening has been formed exposing a portion of the region or layer to be contacted, the opening is generally cleaned with a sputter etch, e.g., a Radio-Frequency ("RF") sputter etch, and then the opening is filled with a conductive material deposited in the opening and in electrical contact with the underlying region or layer.

10 To form the openings a patterning layer of photoresist is first formed over the dielectric layer having openings corresponding to the regions of the dielectric where the dielectric layer openings are to be formed. In most modern processes a dry etch is then performed wherein the wafer is exposed to a plasma, formed in a flow of one or more gases. Typically, one or more halocarbons and/or one or more other
15 halogenated compounds are used as the etchant gas. For example, CF_4, CHF_3 (Freon 23), SF_6, NF_3, and other gases may be used as the etchant gas. Additionally, gases such as O_2, Ar, N_2, and others may be added to the gas flow. The particular gas mixture used will depend on, for example, the characteristics of the dielectric being etched, the stage of processing, the etch tool being used, and the desired etch
20 characteristics, i.e., etch rate, sidewall slope, anisotropy, etc.

Many of the etch characteristics are generally believed to be affected by polymer residues that deposit during the etch. For this reason, the fluorine to carbon (F/C) ratio in the plasma is considered an important determinant in the etch. In general, a plasma with a high F/C ratio will have a faster etch rate than a plasma
25 with a low F/C ratio. At very low rates, i.e., high carbon content, polymer deposition occurs and etching ceases. The etch rate as a function of the F/C ratio is

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typically different for different materials. The difference is used to create a selective etch, by using a gas mixture that puts the F/C ratio in the plasma at a value that leads to etching at a reasonable rate for one material, and that leads to no etching or polymer deposition for another. For example, an etchant that has an etch rate ratio or a selectivity ratio of two to one for silicon nitride compared to silicon dioxide is an effective stripper of silicon nitride from the semiconductor substrate, because it will selectively strip silicon nitride over silicon dioxide on a substrate surface. An etchant that has an etch rate ratio or a selectivity ratio of 0.85 to one for silicon nitride compared to silicon dioxide is not considered an effective stripper of silicon nitride from the semiconductor substrate because the etchant will not effectively strip silicon nitride to the exclusion of silicon dioxide.

The selectivity of the etch process is a useful parameter for monitoring the process based on the etch rate characteristic of the particular etchant. As noted above, particular etchants or etchant chemistries attack different materials at different etch rates. With respect to dielectrics, for example, particular etchants attack silicon dioxide, BPTEOS, TEOS, and silicon nitride dielectrics at different rates. To make openings in a substrate comprising a contact region surrounded by different dielectric layers, e.g., a dielectric layer of TEOS surrounded by a dielectric layer of silicon nitride, a process will utilize different etchants to make openings through the different dielectrics. Thus, the different etch rates of particular dielectric layers for an etchant may be used to monitor the creation of an opening through a dielectric layer.

Further, by adjusting the feed gases, the taper of the sidewall in the etched opening of the dielectric can be varied. If a low sidewall angle is desired, the chemistry is adjusted to try to cause some polymer buildup on the sidewall. Conversely, if a steep sidewall angle is desired, the chemistry is adjusted to try to

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prevent polymer buildup on the sidewall. Varying the etch gas pressure, for example, has a significant effect on the shape of the opening. This is because the etchant ions generally arrive in a direction perpendicular to the substrate surface, and hence strike the bottom surfaces of the unmasked substrate. The sidewalls of
5 etched openings, meanwhile, are subjected to little or no bombardment. By increasing the pressure of the etch gas, the bombardment directed toward the sidewalls is increased; by decreasing the pressure of the etch gas, the bombardment directed toward the sidewalls is decreased. The changing of the etch chemistry is also directly related to selectivity. Etchants that provide a near 90° sidewall angle are
10 generally not highly selective while highly selective etches typically produce a sloped sidewall.

Following the dielectric etch(es) and prior to any conductive material deposition in a contact region, native oxide on top of the conducting layers in the contact region is removed or cleaned through a non-chemical sputter etch, e.g., an
15 RF sputter etch. In addition to alleviating the contact region of native oxide, the sputter etch can erode any insulating dielectric layer or layers. Thus, the parameters of the sputter etch must be carefully monitored so as not to excessively erode the insulating dielectric layer(s) and expose other underlying conductive material. Exposing insulated conductive material adjacent to the conductive material in the
20 contact region results in poor quality contacts or a short circuit through the underlying conductive material. For a thorough discussion of oxide etching, see S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Vol. 1, pp. 539-85 (1986).

The preceding discussion focused on the making of openings, e.g., contact openings, in dielectric material on a semiconductor substrate. The same principles
25 are used in constructing device regions with a dielectric layer or layers. As
a geometries shrink, the forming of discrete devices on a semiconductor substrate

SAMSUNG-1008.013

becomes more specialized. Specialized deposition and etching techniques permit the density of semiconductor elements on a single chip to greatly increase, which translates into larger memory, faster operating speeds, and reduced production costs.

A typical metal oxide semiconductor (MOS) transistor, e.g., NMOS or PMOS transistor, generally includes source/drain regions in a substrate, and a gate electrode formed above the substrate between the source/drain regions and separated from the substrate by a relatively thin dielectric. Contact structures can be inserted to the source/drain regions and interlays can overlie the contact structures and connect neighboring contact structures. These contact structures to the diffusion region are isolated from the adjacent gate by dielectric spacer or shoulder portions. The dielectric spacer or shoulder portions also isolate the gate from the diffusion region.

Conventional contact structures limit the area of the diffusion region, because the contact hole is aligned to these regions with a separate masking step, and extra area must be allocated for misalignment. Proper alignment is necessary to avoid shorting the contact structure to the gate or the diffusion well. The larger contact area means a smaller density of elements on a structure. The larger contact area is also responsible for increased diffusion-to-substrate junction capacitance, which limits device speed.

A self-aligned contact eliminates the alignment problems associated with conventional contact structures and increases the device density of a structure. A self-aligned contact is a contact to a source or drain diffusion region. A self-aligned contact is useful in compact geometries because it can overlap a conducting area to which it is not supposed to make electrical contact and can overlap the edge of a diffusion region without shorting out to the well beneath. Consequently, less

contact area is needed and gates or conductive material lines, e.g., polysilicon lines, can be moved closer together allowing more gates or lines on a given substrate than traditional contacts.

Figure 1 illustrates a self-aligned contact between two gate structures. Figure 1(A) is a planar top view of the contact. Figure 1(B) is a planar cross-sectional view of a self-aligned contact between a pair of gates taken through line 1(B) of Figure 1(A). Figure 1(C) is a planar cross-sectional view of a self-aligned contact between a pair of gates taken through line 1(C) of Figure 1(A).

The self-aligned contact is a contact to a source or drain diffusion region (n+ or p+ silicon) 140 that can overlap the edge of the diffusion region 140 without shorting out to the well beneath the diffusion region 140. This can be seen most illustratively through Figure 1(C). In Figure 1(C), the contact 130 does not lie directly in the diffusion region 140, but is misaligned and slightly overlaps the field oxide. In this illustration, the self-aligned contact is not directly over the diffusion region but extends over (i.e., overlaps) a well portion 170. The self-aligned contact does not short to the well portion 170 because the self-aligned contact is separated from the well 170 by the field oxide.

The self-aligned contact 130 is separated from a conducting polysilicon layer 110 by an encapsulating dielectric layer 120 such that the contact 130 can also overlap the polysilicon layer 110 without making electrical contact to the layer 110 or gate. The polysilicon layer 110 is separated from the source/drain diffusion region 140 by a dielectric spacer or shoulder 150 of the same or different dielectric material as the dielectric layer 120 directly above the conducting polysilicon.

A distinct dielectric etch stop layer 125 overlies the encapsulating dielectric layer 120. The etch stop layer 125 permits subsequent etching of the substrate

SAMSUNG-1008.015

without risk of exposing the device structures and layers because the device structuring and layers are protected from excessive etching by the etch stop layer. The diffusion contact is self-aligning because the structure can be etched to the substrate over the source/drain diffusion region 140 while the dielectric spacer 150 protects the polysilicon layer 110. Even if a photoresist that protects the polysilicon layer 110 from the etchant is misaligned with respect to the polysilicon layer 110, the dielectric spacer 150 prevents shorts to the polysilicon layer 110 when the contact 130 is provided for the diffusion region 140.

The current practice with respect to forming contact regions, particularly self-aligned contact regions, that are in electrical contact with gates, interconnect lines, or other structures in small feature size structures utilize etchants with high selectivity to protect underlying regions, like the etch stop layer and the first insulating layer. Figure 2 demonstrates a typical prior art process of forming a self-aligned contact region adjacent to a gate. In Figure 2(A), a gate oxide layer 210 is formed on a substrate 200 with a conducting layer, for example a polysilicon layer 220, overlying the gate oxide layer 210, and an insulating layer, for example a TEOS layer 230, overlying the polysilicon layer 220. Adjacent to the polysilicon layer is a contact opening region 270. The polysilicon layer 220 is separated from the contact region 270 by an insulating spacer portion, for example a TEOS spacer portion 235. A separate insulating or etch stop layer, for example a silicon nitride layer 240 overlies the TEOS layer 230 and the contact region 250. A blanket layer, for example a doped insulating layer like a BPTEOS layer 250, planarly overlies the etch stop layer 240.

A layer of photoresist material 280 overlies the planarized BPTEOS layer 250 to expose the contact opening 270. In Figure 2(A), a contact opening 270 has been opened through the BPTEOS layer 250. The etchant utilized to make the opening had a high selectivity toward BPTEOS relative to silicon nitride. When the contact

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opening was through the BPTEOS material, the etchant did not etch or did not effectively etch the silicon nitride layer 240 material. Hence the description of the silicon nitride layer 240 as an etch stop layer. The silicon nitride etch stop layer protected the underlying TEOS layer so that the polysilicon remains completely encapsulated.

Figure 2(A) illustrates an etch 260 to remove the silicon nitride etch stop layer 240. In the etch illustrated in Figure 2(A), a high selectivity etch toward silicon nitride relative to the underlying TEOS layer 230 material is practiced to efficiently etch the silicon nitride layer and to protect the underlying TEOS layer 230 from the etchant. An example of a high selectivity etch recipe to effectively strip silicon nitride as compared to the TEOS layer is 30 sccm CHF_3 and 30 sccm O_2 at 60 mtorr and 100 watts of power. The result of the high selectivity etch is illustrated in Figure 2(B).

Figure 2(B) shows that the silicon nitride selective etch effectively removed silicon nitride 240 from the contact opening 270. The selective etch for silicon nitride compared to TEOS material, however, left the TEOS layer 230 with a spacer portion 235 wherein the spacer portion is sloping or tapered toward the contact opening. This result follows even where the spacer portion 235 is originally substantially rectangular as in Figure 2(A). The properties of the highly selective etch of the overlying etch stop layer will transform a substantially rectangular spacer into a sloped spacer. Figure 2(B) presents a polysilicon layer 220 encapsulated in a TEOS layer 230 with a spacer portion 235 adjacent to the contact opening 270, the spacer portion 235 having an angle 290 that is less than 85°.

In addition to providing stopping points or selectivity between materials, the use of high selectivity etches to form sloped spacer portions is the preferred practice

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because the sloped shape will result in good step coverage by the metal that is deposited into it. The filling of contact openings or gaps (i.e., gap fill) is an important consideration because it relates directly to the reliability of a device. If an opening is not completely filled with a insulative material, for example, and a gap is created, a subsequent conductive material deposit can fill the gap which can lead to shorting. Sloped contact openings are easier to completely fill than boxy structures because the transition between sloped structures and openings is smooth compared to the abrupt transitions between boxy structures and openings. Because of concerns for complete gap fill and good step coverage, industry preference is for sloped spacers and planar deposition layers similar to that shown in Figure 2(b).

Once the contact opening is made, the opening is cleaned with a sputter etch, e.g., an RF sputter etch, before conductive material is added to fill the opening or gap. The RF sputter etch that is used to clean the contact opening in the process described above will attack and erode a portion of the insulating spacer surrounding the conducting portion and adjacent to the contact region. Figure 3 presents a prior art substrate with a gate and a contact region undergoing an RF sputter etch. In Figure 3, a gate oxide 310 is formed on a substrate 300 with a polysilicon layer 320 overlying the gate oxide 310 and an insulating layer, for example a TEOS layer 330 overlying the polysilicon layer 320. A distinct insulating layer, for example a silicon nitride etch stop layer 340, overlies the TEOS layer 330 and this etch stop layer 340 is covered by a third insulating layer, for example a BPTEOS blanket layer 350. Adjacent to the gate is a contact region 360. An etch of the silicon nitride etch stop layer 340 with a high selectivity etch for silicon nitride relative to the underlying TEOS layer material produced a gate with a sloping or tapered spacer portion 370 of TEOS material, illustrated in ghost lines. A subsequent RF sputter etch is utilized to clean the contact region 360.

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Although brief and designed to clean the contact region, the RF sputter etch will erode a portion of the insulating TEOS spacer. The dynamics of the sputter etch are that it proceeds vertically, directing high-energy particles at the contact region. The sloping or tapered spacer portion adjacent the polysilicon and separating the polysilicon from the diffusion region is struck by the high-energy particles of the RF sputter etch 380. Because the spacer portion 370 is sloping or diagonal, a significant surface area portion of the spacer portion 370 is directly exposed to the high-energy particles from the RF sputter etch 380. Further, with sloping spacers, or spacers having an angle relative to the substrate surface of less than 85° the vertical portion of the dielectric layer (i.e., that portion above the polysilicon gate) decreases much less than the diagonal portion of the spacer. In terms of measuring TEOS material removal during the RF sputter etch in Figure 3, the difference between d_1 and d_2 is greater than the difference between v_1 and v_2. Thus, in conventional prior art self-aligned contact structures, the diagonal thickness of the TEOS spacer, rather than the vertical thickness of the TEOS layer, determines the minimum insulating layer thickness for the gate.

For gate structures having minimum diagonal insulative spacer portions of 500 Å or less, the result of the sputter etch 380 is that the sputter etch 380 laterally erodes the diagonal portion of the TEOS layer 370 adjacent to the contact region to a point where the polysilicon 320 is no longer isolated from the contact region 360 by an insulating layer. In that case, there is a short circuit through the underlying conductive material when the contact opening is filled with conductive material. This result follows because the conventional RF sputter etch utilized for cleaning the contact region results in an approximately 200-500 Å loss of the spacer material. Further, process margins generally require that the device spacer have a final minimum thickness (after all etches, doping, and deposits) of at least 500 Å. Thus,

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to eliminate alignment sensitivity for conventional small feature size structures, including self-aligned contact structures, requires a final (i.e., at the time of contact deposition) minimum insulating spacer of more than 500 Å and preferably on the order of 1000-1500 Å or greater to fulfill requirements for an adequate process margin, complete gap fill, and device reliability.

To construct structures having a minimum insulative spacer portion of more than 500 Å directly effects the number of structures that can be placed on a device, such as a chip. The construction of structures having a minimum insulative spacer portion of more than 500 Å requires that the pre-etch-stop-etch spacer be bigger or thicker to yield an effective spacer after the etching processes. In such cases, the structures must be separated a distance such that the contact area opening is sufficient enough for an effective contact. This spacing requirement directly limits the number of structures that can be included on a device. In small feature size structures, particularly structures utilizing self-aligned contacts, the width of contact openings is approximately 0.6 microns at the top of the planarized layer and 0.2 microns at the base of the contact opening. Figure 3 indicates the difference in contact opening widths for the same contact in prior art structures. w_1 represents the width at the top of the planarized layer and w_2 represents the width at the base of the contact opening. Further, an aspect ratio can be defined as the height of a structure (field oxide plus conductive layer plus first insulative layer plus etch stop layer, if any) relative to the width of the base of a contact opening (i.e., the distance between adjacent spacers). Typical aspect ratios for self-aligned contact structures target ratios of 1.0-2.4. This prior art range is not achievable with any device reliability. To achieve aspect ratios of 1.0-2.4 requires minimum spacer portions of less than 1000 Å and preferably on the order of 500 Å. As noted above, the minimum spacer portions required for aspect ratios of 1.0-2.4 cannot withstand the

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sputter etch and will result in the exposure of the underlying polysilicon gate and short circuiting with the contact.

There is a need for cost effective structures wherein the individual devices are as close together as possible while maintaining device reliability and an adequate
5 process margin and assuring complete gap fill. There is a need for a device and for a process to manufacture such a device whereby there is provided a contact opening with no alignment sensitivity relative to a gate electrode or other structure and whereby the gate electrode does not fall within the contact opening but remains isolated from the contact opening by an insulating layer. The process must be
10 compatible with gate electrode insulating spacers of less than 500 Å. The device resulting from the needed process should be capable of maintaining high quality contacts between the conductive material in the contact region and the adjacent conductive gate or other structure.

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SUMMARY OF THE INVENTION

The invention relates to a process for minimizing lateral spacer erosion of an insulating layer on an enclosed contact region, ~~is disclosed~~ and a device including a contact opening with a small alignment tolerance relative to a gate electrode or other structure. The process provides high quality contacts between a conductive material in the contact region and a device region, such as a source or drain, or some other layer or structure. The process comprises the well known step of forming a conductive layer on the semiconductor body adjacent a contact region. This is followed by the forming of a first insulating layer adjacent said conductive layer and the contact region. A selected area is masked with photoresist and the first insulating layer and the conductive layer are etched to form a device structure, such as a gate, adjacent the contact region. Next, insulating lateral spacers are added to the device structure to isolate the conductive portion of the device. The insulating spacers are etched so that the device comprises an insulating layer overlying a conductive layer with a lateral spacer portion adjacent the contact region wherein the spacer portion has a substantially rectangular profile. A distinct insulating layer or etch stop layer is then formed adjacent to the first insulating layer and over the contact region. A third insulating layer or blanket layer is then optionally formed over the etch stop layer. The blanket layer may or may not be planarized.

If a blanket layer is included, an etchant is utilized to etch a contact opening through the exposed portion of the blanket layer to the etch stop layer. Next, a second etch or etch-stop etch is performed to remove the etch stop layer material from the contact region. The etch-stop etch is also almost completely anisotropic, meaning that the etchant etches in one direction--in this case, vertically (or perpendicular relative to the substrate surface) rather than horizontally. The etch

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removes the etch stop insulating layer and retains the substantially rectangular lateral spacer portion of the first insulating layer. The anisotropic etch etches primarily the exposed etch stop material that lies normal to the direction of the etch. Thus, the etch removes the etch stop material covering the area of the contact
5 region but does not significantly etch the etch stop material adjacent to the spacer(s). The etch stop layer on the spacer adds dielectric thickness between the conductive layer and any contacting conductor. In general, the etching conditions utilized for the etch-stop etch have a low selectivity for etching the etch stop layer compared to the underlying insulating material.

10 The etch-stop etch may be followed by a sputter etch to clean the contact region. Unlike prior art processes whereby the sputter etch erodes the underlying sloping lateral spacer portion of the first insulating layer adjacent to the conducting layer, the sputter etch does not significantly erode the substantially rectangular lateral spacer of the first insulating layer, thus allowing the conductive layer of the
15 device structure to remain completely isolated or insulated by a spacer comprised of the first insulating layer and some etch stop layer material.

The structure contemplated by the invention is an effective device for small feature size structures, particularly self-aligned contacts. The structure consists of first and second conducting layers spaced apart by a region with an area defined in
20 the substrate; an insulating layer encapsulating each conductive layer, wherein the insulating layer includes lateral spacer portions; and an etch stop layer adjacent the insulating layer and over the first and second conducting layers. The invention contemplates that the structure region has a first width between the first and second conducting layers, and a second width between the lateral spacer portions of the
25 insulating layer adjacent to the first and second conducting layers, wherein the region has an aspect ratio of 1.0-2.4. The aspect ratio is defined as the height of the

apparatus relative to the second width of the region. Thus, the invention contemplates larger contact openings for effective contacts, reduced device feature size, and increased device density, while maintaining aspect ratios similar to larger, less dense devices in the prior art. The invention further contemplates that the
5 structure has a minimum insulating layer thickness of 400 Å and that this minimum thickness is determined by the thickness of the insulating layer deposited vertically on the structure.

The device is capable of maintaining high quality, reliable contacts between the conductive material in the contact region and the underlying device region,
10 such as a source or drain, or some other layer or structure. The device contemplates minimum contact opening base widths of 0.2 microns and minimum contact opening widths of 0.5 microns when measured from the top of a planarized layer, and aspect ratios (i.e., height of structure including the etch stop layer relative to the width of the base of a contact opening between the spacers) on the order of 1.0-2.4.

15 Additional features and benefits of the invention will become apparent from the detailed description, figures, and claims set forth below.

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BRIEF DESCRIPTION OF THE DRAWINGS

The features, aspects, and advantages of the present invention will become more thoroughly apparent from the following detailed description, appended claims, and accompanying drawings in which:

Figure 1 is ~~a planar view of~~ a self-aligned contact to diffusion. Figure 1(A) is a planar top view of a self-aligned contact. Figure 1(B) is a cross-sectional planar side view of a self-aligned contact ~~to diffusion~~ through line 1(B) of Figure 1(A). Figure 1(C) is a cross-sectional planar side view of a self-aligned contact to diffusion through line 1(C) of Figure 1(A).

Figure 2 is a cross-sectional side view of the formation of a prior art contact opening ~~formation~~. Figure 2(A) illustrates a high selectivity etch of an etch stop insulating layer, and Figure 2(B) illustrates the results of that etch.

Figure 3 is a cross-sectional side view ~~of the formation~~ of a prior art contact opening ~~formation~~ during a sputter cleaning etch.

~~Figure 3 is a cross-sectional view of an example of a semiconductor device during fabrication upon which the invention may be practiced.~~

Figure 4 presents a cross-sectional planar side view of the preparation of a series of gates on a semiconductor substrate surface.

Figure 4(A) illustrates a cross-sectional planar side view of an insulating layer adjacent to a conducting layer, both layers overlying two diffusion regions.

Figure 4(B) illustrates a cross-sectional planar side view of a series of gates consisting of insulating material adjacent conducting material.

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Figure 4(C) illustrates a cross-sectional planar side view of the deposition of additional insulating material over the series of gates, the additional insulating material to be used for the formation of spacer portions adjacent the contact or diffusion regions.

Figure 4(D) illustrates a cross-sectional planar side view of a series of gates completely encapsulated in insulating material wherein the spacers of the insulating material adjacent the contact or diffusion regions have substantially rectangular profiles.

Figure 4(E) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material ~~and an insulating etch stop layer overlying the insulating material~~.

Figure 4(F) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material and an insulating etch stop layer overlying the insulating material~~, wherein the diffusion region is implanted to include a silicide~~.

Figure 4(G) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, and a distinct planarized insulating layer overlying the etch stop layer.

Figure 4(H) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the etch stop layer, and a photoresist patterning layer deposited over the blanket layer.

Figure 4(I) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating

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material, a distinct planarized insulating blanket layer overlying the etch stop layer, and contact openings etch through the blanket layer above the diffusion region.

Figure 4(J) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating
5 material, a distinct planarized insulating blanket layer overlying the etch stop layer, and a contact opening to a diffusion region and a second contact opening through the blanket layer but separated from the diffusion region by an etch stop layer.

Figure 4(K) illustrates a close-up cross-sectional planar side view of a circled portion of Figure 4(J), the circled portion labeled 4(K) and illustrating the spacer
10 portion of a contact region following an etch of the etch stop layer from the contact region.

Figure 4(L) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the etch stop layer,
15 and a conductive contact in a contact region extending to a diffusion region in the semiconductor substrate.

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DETAILED DESCRIPTION OF THE INVENTION

The invention is a device and a process whereby there is provided a contact opening with a no alignment sensitivity relative to a gate electrode or other structure such that the gate electrode does not fall within the contact opening but remains isolated from the contact opening by an insulating layer. The structure contemplated by the invention is an effective device for small feature size structures, particularly self-aligned contacts, because it is capable of maintaining high quality contacts between the conductive material in the contact region and the underlying device region, such as a source or drain, or some other layer or structure with minimum contact opening base widths (i.e., at the base of the contact openings) of 0.2 microns and minimum contact opening widths of 0.5 microns when measured from the top of a planarized layer, minimum encapsulating layer thicknesses of 400 Å, and aspect ratios (i.e., height of structure including the etch stop layer relative to the width of the base of a contact opening between the spacers) in the range of 1.0-2.4.

In the following description, numerous specific details are set forth such as specific materials, thicknesses, processing steps, process parameters, etc., in order to provide a thorough understanding of the invention. It will be obvious, however, to one skilled in the art that these specific details need not be employed to practice the invention. In other instances, well known materials or methods have not been described in detail in order to avoid unnecessarily obscuring the invention. Furthermore, in the following discussion, several embodiments of the invention are illustrated with respect to specific structures, oxide layers, and oxide layer openings. It will be appreciated that each of the methods described herein can be utilized on a variety of structures and oxide layers, to form any type of opening, and

each of the insulating layer etching methods described herein is not necessarily restricted to the structure and/or insulating layer in conjunction with which it is described. Further, any of the methods described herein may be performed as part of a multistep etch comprising additional etch processes.

5 Figure 4 presents a cross-sectional view of the preparation of a series of gates or transistors on a semiconductor substrate surface. Referring to Figure 4(A), the semiconductor substrate 400 can be either p- or n-type, and includes diffusion regions 405, such as sources or drains, that are heavily doped with the opposite dopant type of the substrate. An n-type first conducting layer 415 of polysilicon 10 doped by implantation with phosphorous to a resistivity of 50-200 ohms/square is deposited over the diffusion regions 405. The polysilicon layer 415 is deposited by low pressure CVD ("LPCVD") using an LPCVD tube and SiH_4 gas at 200-400 mtorr with a thickness of 2000-3000 Å. It should be appreciated by those skilled in the art that this conducting layer 415 could instead be a p-type conducting layer or a metallic 15 conductor of, for example, W, Mo, Ta, and/or Ti, or that this conducting layer ~~320~~ 415 could also be a silicide, consisting of WSi_2, $MoSi_2$, $TaSi_2$, PtSi, PdSi, or that this conducting layer ~~320 can~~ 415 could further be a layered structure consisting of a silicide on top of doped polysilicon.

The polysilicon layer 415 overlays an insulating dielectric layer 410 such as 20 doped or undoped silicon dioxide. The dielectric layer 410 may comprise a single oxide, or several layers formed by various methods. For example, one or more layers of oxide may be deposited by plasma enhanced chemical vapor deposition ("PECVD"), thermal CVD ("TCVD"), atmospheric pressure CVD ("APCVD"), subatmospheric pressure CVD ("SACVD"), ~~for example~~ utilizing, for example, 25 TEOS and oxygen, or TEOS and ozone chemistries. As used herein, reference to, for example, a PECVD TEOS oxide denotes an oxide layer deposited by PECVD utilizing

TEOS chemistry. Additionally, one or more layers of dielectric layer 410 may be a spin-on-glass ("SOG") layer.

A TEOS dielectric layer 420 with a total thickness of approximately 3000 Å overlies the conducting layer 415. It should be appreciated by those of ordinary skill in the art that this TEOS layer 420 could instead be an insulating layer of, for example, silicon dioxide, SiO_2, ONO, silicon nitride (Si_xN_y), or silicon oxynitride (SiO_xN_y). Additionally, the insulating layer 420 may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate ("BPTEOS"). Further, the dielectric layer 420 may comprise a single layer oxide, like TEOS, or several layers formed by various methods.

Referring further to Figure 4(A), a photoresist masking layer 425 is deposited over the TEOS dielectric layer 420. The photoresist masking layer 425 exposes diffusion regions 405 in the semiconductor substrate. Referring to Figure 4(B), a series of photolithographic etches are performed to remove the TEOS layer 420 material and the polysilicon layer 415 from the diffusion or contact regions. The etches are performed using a parallel plate plasma etcher with a power of 200-300 watts. First, a fluorocarbon photolithographic etch, CHF_3/C_2F_6 at 50 mtorr, is performed to remove the insulating TEOS material from areas adjacent to and including the diffusion or contact regions. This is followed by a single polysilicon photolithographic etch using a chlorine plasma (Cl_2/He) to define a polysilicon conducting layer 415 above the transistor or gate regions.

The process described thus far has been described in terms of multiple etching steps involving multiple passes through the etch chamber. It should be recognized

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by one of ordinary skill in the art that the etching steps can be combined into a multiple-step etch whereby the etch may be accomplished with one pass through the etch chamber, the etcher changing chemistries and executing the multiple etches sequentially.

5 Referring to Figure 4(C) and 4(D), spacers are formed between the polysilicon layer 415 of the gates and the contact openings by depositing an additional of conformal layer of TEOS material 430 over the structure and etching spacer portions extending into the contact openings and adjacent to the polysilicon layer 415 approximately 1500 Å in width. The spacer portions 435 of the TEOS layer 430 are 10 demarked by ghost lines in Figure 4(D). The spacers 435 serve to insulate the polysilicon layers 415 from the conducting material that will fill the contact openings and prevent the gates from overlapping the diffusion regions 405. The spacers 435 serve to completely encapsulate the polysilicon layers 415 of the individual gates. As shown in Figure 4(C), care is taken to etch the spacers 435 such that the spacers 435 have a 15 substantially rectangular profile. This is accomplished using a low bias and high pressure etch (2.8 torr, 140 sccm He, 30 sccm CHF_3, 90 sccm CF_4, and 850 watts power), that results in low polymer formation. At this point, the preferred embodiment of the invention contemplates that the TEOS layer can have a minimum vertical width of approximately 3000 Å and spacers with a minimum 20 width of approximately 1000 Å.

Referring to Figure 4(E), the diffusion regions 405 are next implanted with a suitable dopant utilizing conventional techniques. The dopant may be implants of arsenic, phosphorous, or boron. Subsequently, silicides, for example WSi_2 and $TiSi_2$, may also be formed. Figure 4(E) illustrates silicide formation 445 in the 25 diffusion regions 405.

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Referring to Figure 4(F), overlying the TEOS layer 420 is deposited a second distinct dielectric or etch stop layer 440, in this example, an silicon nitride (Si_xN_y) layer 440, with a total thickness of 700 angstroms. It should again be appreciated by those of ordinary skill in the art that this silicon nitride layer 440 could instead be an insulating layer of, for example, silicon dioxide, SiO_2, ONO, or $SiO_xN_y(H_z)$. Additionally, the silicon nitride etch stop layer 340 may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate ("BPTEOS"). Further, the etch stop layer 440 may comprise a single silicon nitride layer or several layers formed by various methods. It is important that the etch stop layer be different or distinct from the underlying insulating layer.

The invention contemplates that at this point the structure has an aspect ratio of 1.0-2.4. As used herein, an aspect ratio is defined as the ratio of the height of a contact opening to the top of the horizontal portion of the etch stop layer to the base width of the contact opening between the insulating spacers. For example, an embodiment of the invention contemplates contact opening heights of 5300 Å (0.53 μm) relative to widths of 0.32 μm to give aspect ratios of 1.6.

Referring to Figure 4(G), an optional dielectric blanket layer 450 is next deposited adjacent to the etch stop layer 440. The blanket layer 450 may or may not be planarized. In Figure 4(G), the blanket layer 450 is planarized. The planarized blanket layer 450 facilitates the formation of an interconnect layer that might later be deposited over the contact regions. The blanket layer in Figure 4(G) is a doped silicate glass, for example BPTEOS. It should be appreciated by those of ordinary skill in the art that this BPTEOS layer 450 could instead be another doped insulating layer of, for example, BPSG or PSG, or an undoped insulating layer of silicon dioxide,

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SiO_2, ONO, or SiO_xN_y. Further, the blanket layer 450 may comprise a single oxide, like BPTEOS, or several layers formed by various methods.

Next, as shown in Figure 4(H), a photoresist pattern or mask layer is deposited adjacent to the blanket layer such that the contact regions overlying the diffusion regions are exposed. This is followed by a photolithographic etch of the BPTEOS blanket layer 450 in the contact regions. The etch is a fluorocarbon photolithographic etch (7 sccm CHF_3, 6 sccm Freon 134a) at 29 mtorr. The etch reveals a pair of contact regions 460 and 465 above the diffusion regions.

Referring to Figure 4(J), a photoresist material 470 is overlayed in contact opening 465 adjacent to the etch stop layer to protect the etch stop material in contact opening 465 from a subsequent photolithographic etch to remove the etch stop layer. Next, a photolithographic etch, (900 mtorr, 100 sccm, He, 85 sccm C_2F_6, and 225 watts power using a Lam 4400 Series plasma etching system) is performed to remove the etch stop layer 440 from contact opening 460. The etch conditions for this etch are low bombardment/high neutral flux conditions.

Figure 4(K) is a close-up view of the cross-sectional portion of contact opening 460 in Figure 4(J). The etch proceeds anisotropically, primarily removing etch stop material lying in a horizontal plane relative to the vertical direction of the etchant ions. The etchant removes material primarily from the base of the contact region 460, and does not remove all of the etch stop material adjacent to the spacer portion of the TEOS layer 420. Thus, the remaining etch stop material adjacent to the spacer portion of the TEOS layer serves as additional spacer material to insulate the polysilicon from a conductive contact that will subsequently be added to the contact region 460.

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The etchant utilized to remove silicon nitride from the contact region 460 has a low selectivity for etching the silicon nitride material compared to the underlying TEOS layer. The use of an etchant with a low selectivity for silicon nitride relative to TEOS does not significantly destroy the TEOS layer 420 spacer portion. The low selectivity etch yields a TEOS layer 420 spacer portion that retains a rectangular or "boxy" profile. Figure 4(K) illustrates that only a small portion 475 (illustrated in ghost lines) of the TEOS layer 420 spacer portion is removed during the etch. Of primary significance, the spacer portion of the TEOS layer 420 retains its substantially rectangular profile.

It is to be appreciated that the described etch stop layer etch conditions (i.e., low selectivity, low bombardment/high neutral flax) are exemplary of etch conditions that result in the retention of a boxy spacer. The invention relates to these process conditions as well as others that result in the retention of a boxy spacer. Thus, the etch-stop etch conditions should be regarded in an illustrative rather than restrictive sense.

The silicon nitride etch stop layer 440 etch is followed by a sputter etch to clean the contact opening 460. In a currently preferred embodiment, the sputter etch is carried out in an atmosphere of argon, a 8 mtorr pressure, with a 1000 volt bias. In a currently preferred embodiment, the sputter etch is carried out in a commercially available system such as the Applied Materials Endura 5500 systems. Alternatively, any system having a sputter etch mode may be used to practice the invention. As will be appreciated by a person of ordinary skill in the art, the parameters can be varied considerably while still achieving the objects of the invention. In a currently preferred embodiment, the etch is designed to etch approximately 200 Å per minute as measured on thermal oxide. Because of the retention of a substantially

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rectangular or "boxy" spacer portion 435, the sputter etch does not significantly erode the spacer portion 435 of the TEOS layer 420.

At this point, the invention contemplates that the minimum encapsulating dielectric layer, i.e., TEOS, thickness will be approximately 400 Å and that this
5 minimum thickness will be at the corner most effected by the etch-stop layer etch and the sputter etch. In Figure 4(K) that minimum thickness is the diagonal denoted *d*.

Figure 4(L) presents a cross-sectional planar side view of the structure of the invention wherein conductive contacts 480 have been deposited in the contact
10 openings 460.

The process described above yields a structure wherein first and second conductive layers (e.g., polysilicon layers) are separated by a contact opening with an area defined in the semiconductor substrate. An insulating layer is adjacent to and encapsulates the first and second conductive layers. The invention contemplates
15 that the insulating layer has spacer portions between the conductive layers and the contact region. The invention contemplates that high quality contacts can be achieved wherein the spacer portions have a minimum insulative material thickness of 400 Å. In the preferred embodiment, the spacer portions of the insulating material further have substantially rectangular profiles. The invention
20 also contemplates that a portion of the etch stop layer material may remain adjacent to the spacer portion of the insulating layer following an anisotropic etch of the etch stop material with a low selectivity etch for the etch stop material relative to the insulating layer material. The result is a contact opening with spacer sidewalls comprised, at least potentially, of a portion of etch stop layer material.

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The invention contemplates that effective contact openings may have base widths as small as 0.2 μm (and as small as 0.5 μm when measured from the top of the optional planarized layer), and base areas as small as 0.1 μm^2. Thus, the invention contemplates aspect ratios for effective contact openings of 1.0-2.4, wherein an aspect ratio is defined as the ratio of the height of a contact opening to the top of the horizontal portion of the etch stop layer to the base width of the contact opening between the spacers. Figure 4(L) illustrates a height, h, and a width, w, from which an aspect ratio may be calculated for a contact region~~, and a height h_1, and a width, w_1, from which an aspect ratio may be calculated for a contact region~~.

In the preceding detailed description, the invention is described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

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<u>CLAIMS</u>

What is claimed is:

1 1. A process for minimizing lateral spacer erosion on a contact region,
2 said process comprising:

3 encapsulating a conducting layer in an insulating layer on said
4 semiconductor body adjacent said contact region, wherein said insulating layer
5 includes a substantially rectangular spacer portion adjacent said contact region;

6 depositing an etch stop layer adjacent said insulating layer and adjacent
7 said contact region; and

8 etching a portion of said etch stop layer adjacent said contact region
9 wherein said etching does not significantly erode said spacer portion of said
10 insulating layer.

1 2. The ~~process~~ method of claim ~~1~~ 21, wherein said anisotropically etching step utilizes a plasma
2 etching system.

1 3. The ~~process~~ method of claim 2, wherein an etching condition for said anisotropically etching
2 step ~~is~~ comprises a low bombardment/high neutral flux condition.

1 4. The process of claim 3, wherein said etching condition has a low
2 selectivity for said etch stop layer material relative to said first insulating layer
3 material.

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1 5. The process of claim 4, wherein said selectivity is less than or equal to
2 1:1.

1 6. The process of claim 2, wherein said plasma etching system is a Lam
2 4400 Series plasma etching system.

1 7. The process of claim 6, wherein said etch stop layer etch is performed
2 using a recipe of 900 mtorr, 100 sccm He, 85 sccm C_2F_6, and 225 watts power.

1 8. The process of claim 1, including cleaning said exposed portion of said
2 first insulating layer with a sputter etch after said etching of said etch stop layer
3 wherein said spacer portion of said first insulating layer retains its substantially
4 rectangular profile.

1 9. The process of claim 8, wherein said sputter etch is a radio-frequency
2 sputter etch.
1

1 10. The process of claim 1, including depositing a blanket insulating layer
2 adjacent said etch stop layer, forming a patterning layer on said blanket insulating
3 layer wherein said patterning layer exposes said contact region, and etching a
4 portion of said blanket insulating layer over said contact region with a suitable
5 etchant to expose a portion of said etch stop layer prior to said etching of said etch
6 stop layer.

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1 11. The process of Claim 10, wherein the blanket layer is planarized.

1 12. A process for minimizing lateral spacer erosion on a contact region,
2 said process comprising:

3 encapsulating a conducting layer in an insulating layer on said
4 semiconductor body adjacent said contact region, wherein said insulating layer
5 includes a substantially rectangular spacer portion adjacent said contact region;

6 depositing an etch stop layer adjacent said insulating layer and adjacent
7 said contact region; and

8 etching a portion of said etch stop layer adjacent said contact region
9 wherein said etching delivers a minimal diagonal erosion rate of said spacer portion
10 relative to the vertical erosion rate of said insulating layer.

Sub a4

1 13. The process of claim 12, wherein said etching step utilizes a plasma
2 etching system.

1 14. The process of claim 13, wherein an etching condition for said etching
2 step is a low bombardment/high neutral flux condition.

1 15. The process of claim 14, wherein said etching condition has a low
2 selectivity for said etch stop layer material relative to said first insulating layer
3 material.

SAMSUNG-1008.039

1 16. The process of claim 15, wherein said selectivity is less than or equal to
2 1:1.

1 17. The process of claim 13, wherein said plasma etching system is a Lam
2 4400 series plasma etching system.

1 18. The process of claim 17, wherein said etch stop layer etch is performed
2 using a recipe of 900 mtorr, 100 sccm He, 85 sccm C_2F_6, and 225 watts power.

1 19. The process of claim 12, including cleaning said exposed portion of said
2 first insulating layer with a sputter etch after said etching of said etch stop layer
3 wherein said spacer portion of said first insulating layer retains its substantially
4 rectangular profile.

1 20. The process of claim 19, wherein said sputter etch is a radio frequency
2 sputter etch.
1

1 21. The process of claim 12, including depositing a blanket insulating layer
2 adjacent said etch stop layer, forming a patterning layer on said blanket insulating
3 layer wherein said patterning layer exposes said contact region, and etching a
4 portion of said blanket insulating layer over said contact region with a suitable
5 etchant to expose a portion of said etch stop layer prior to said etching of said etch
6 stop layer.

SAMSUNG-1008.040

a 1 22. The method ~~process~~ of Claim 37, wherein the blanket layer is planarized.

1 23. A semiconductor apparatus comprising:

2 first and second conducting layers spaced apart by a region with an area
3 defined in the substrate;

4 an insulating layer adjacent said first and second conductive layers; and

5 an etch stop layer adjacent said insulating layer and over said first and second
6 conducting layers, and a second width between said insulating layer adjacent said
7 first and second conducting layers, and wherein said region has an aspect ratio of 1.0-
8 2.4 said aspect ratio defined as the height of said apparatus relative to the second
9 width of said region.
1

1 24. The semiconductor apparatus of claim 23, wherein said insulating layer
2 has a spacer portion adjacent said region wherein said spacer portion has a
3 substantially rectangular profile.
1

1 25. The semiconductor apparatus of claim 23, wherein said etch stop layer
2 is silicon nitride.
1

1 26. The semiconductor apparatus of claim 23, wherein said etch stop layer
2 is silicon dioxide.

add a[6]

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ABSTRACT

A process for minimizing lateral spacer erosion of an insulating layer adjacent to a contact region and an apparatus whereby there is provided a contact opening with a small alignment tolerance relative to a gate electrode or other structure are disclosed. The process includes the steps of forming a conductive layer on said semiconductor body, then depositing an insulating layer adjacent to the conductive layer. Next, substantially rectangular insulating spacers are formed adjacent to the gate. An etch stop layer is deposited adjacent said insulating layer, followed by an etch to remove the etch stop layer material from the contact region. This etch is conducted under conditions wherein the etch removes the etch stop layer, but retains the substantially rectangular lateral spacer profile of the first insulating layer. The apparatus is capable of maintaining high quality contacts between the conductive material in the contact region and the underlying device region, such as a source or drain, or some other layer or structure, and is an effective structure for small feature size structures, particularly self-aligned contact structures.

SAMSUNG-1008.042

Our Ref.: 16820.P097

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

the specification of which

XXX is attached hereto.
____ was filed on ____________ as
Application Serial No. ____________
and was amended on ____________
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I do not know and do not believe that the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119, of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) — Priority Claimed

(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

SAMSUNG-1008.043

(Application Serial No.) (Filing Date) (Status -- patented, pending, abandoned)

(Application Serial No.) (Filing Date) (Status -- patented, pending, abandoned)

(Application Serial No.) (Filing Date) (Status -- patented, pending, abandoned)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, a firm including: Aloysius T.C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. P39,591; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Thomas M. Coester, Reg. No. P39,637; William D. Davis, Reg. No. 38,428; Daniel M. De Vos, Reg. No. 37,813; Karen L. Feisthamel, Reg. No. P40,264; Scot A. Griffin, Reg. No. 38,167; David R. Halvorson, Reg. No. 33,395; Brian D. Hickman, Reg. No. 35,894; Eric Ho, Reg. No. P39,711; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Jeff D. Jacobs, Reg. No. P40,029; Dag H. Johansen, Reg. No. 36,172; Stephen L. King, Reg. No. 19,180; Daniel C. Mallery, Reg. No. 33,532; Michael J. Mallie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Edward W. Scott IV, Reg. No. 36,000; Maria E. Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; David R. Stevens, Reg. No. 38,626; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. P40,216; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Roland B. Cortes, Reg. No. 39,152; Gary B. Goates, Reg. No. 35,159; Thomas X. Li, Reg. No. 37,079; and Edwin A. Sloane, Reg. No. 34,728; my patent agents, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor James E. Nulty

Inventor's Signature ____________________ Date ____________

Residence ____________________ Citizenship ____________
(City, State) (Country)

Post Office Address ____________________

Full Name of Second/Joint Inventor Christopher J. Petti

Inventor's Signature ____________________ Date ____________

Residence ____________________ Citizenship ____________
(City, State) (Country)

Post Office Address ____________________

SAMSUNG-1008.044

line 1(C)

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line 1(B)

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FIGURE 1

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08/577751

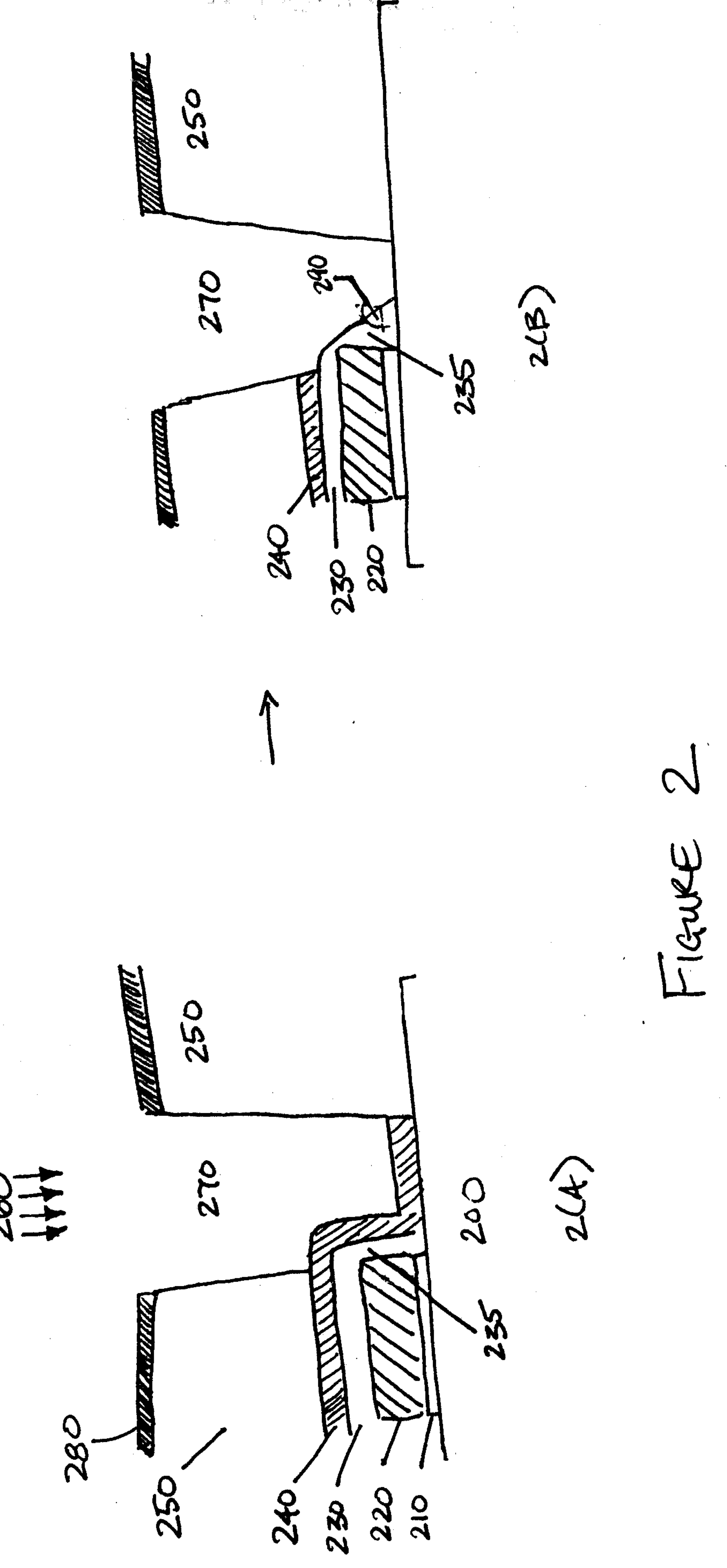

FIGURE 2

08/577751

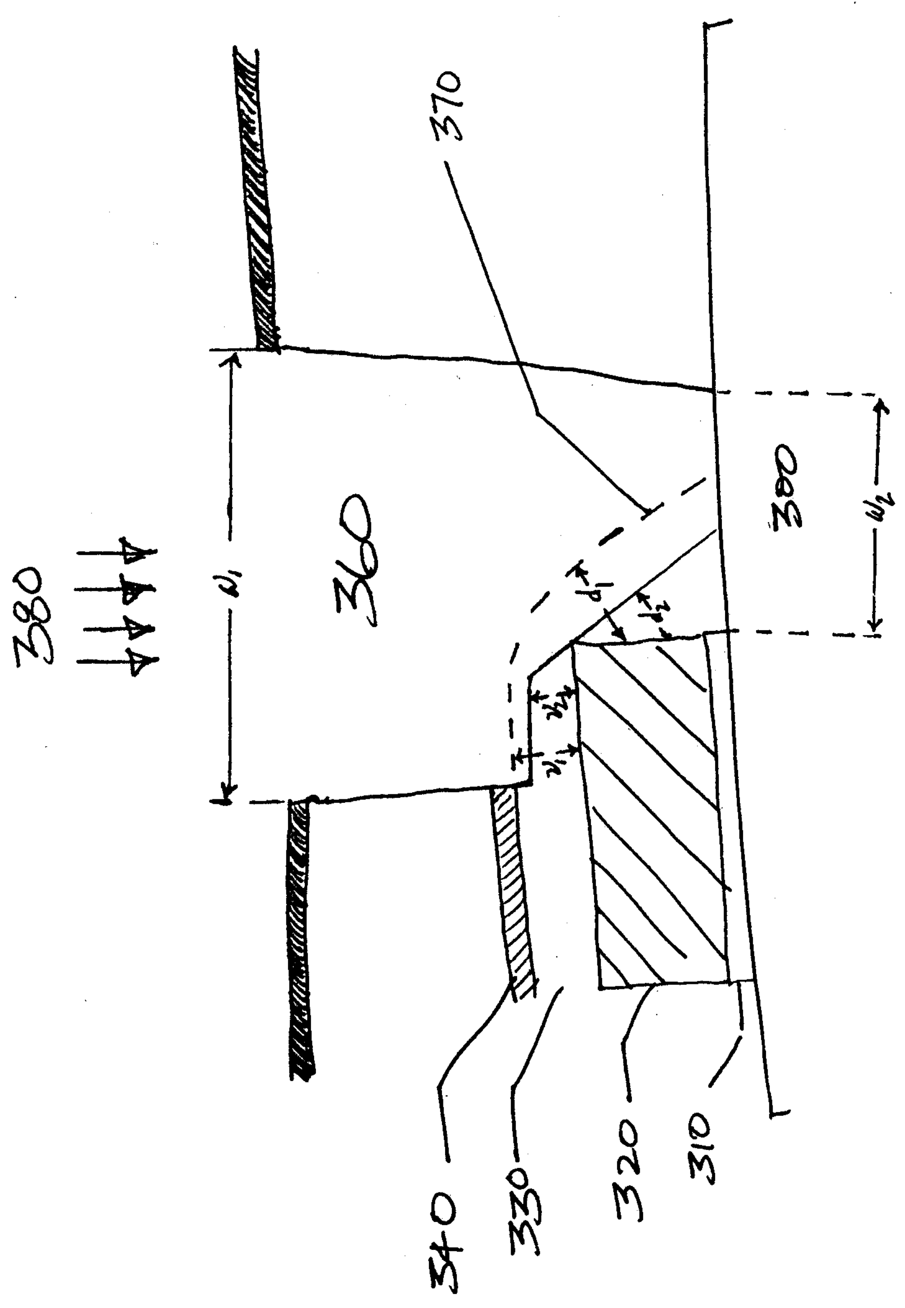

FIGURE 3

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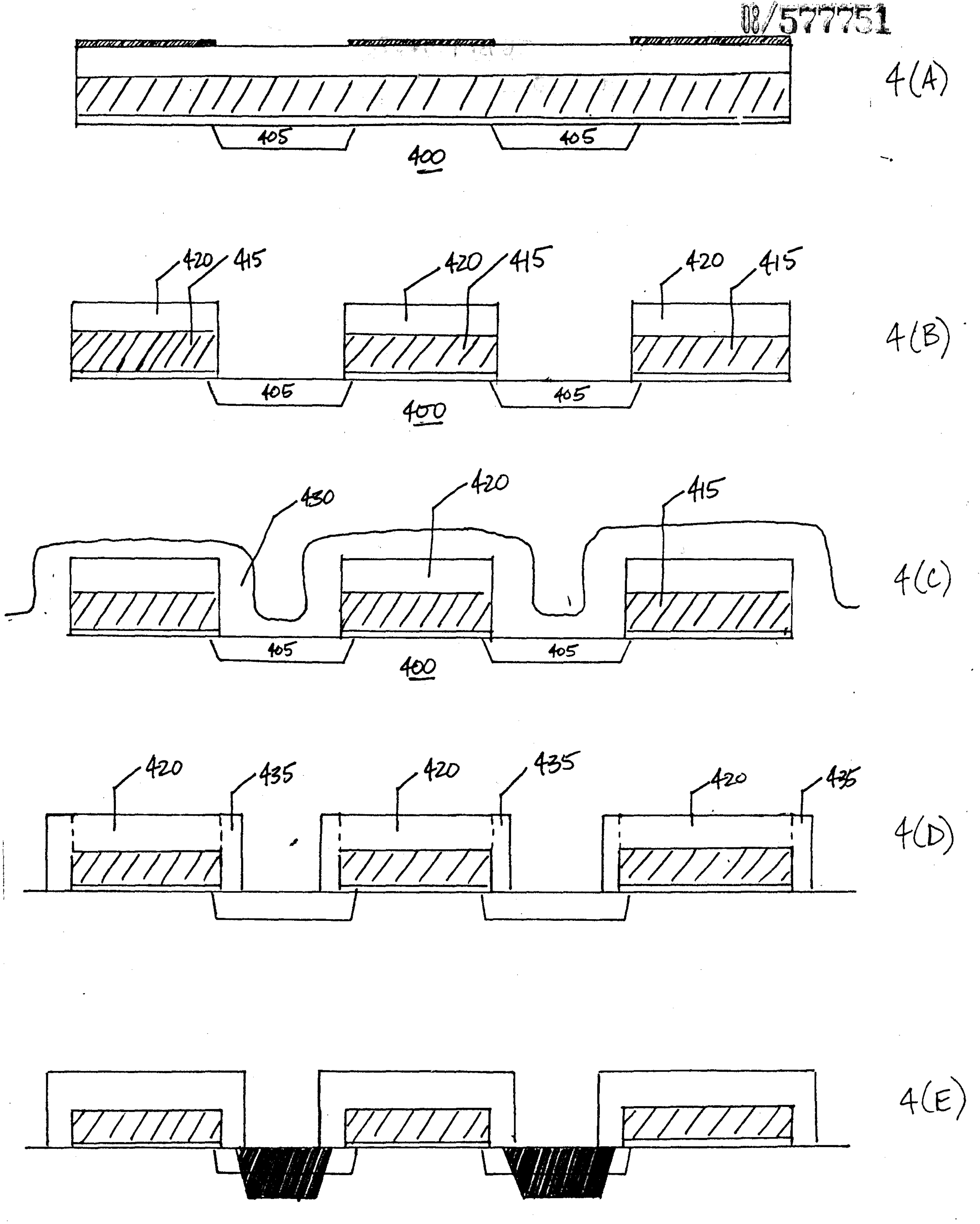

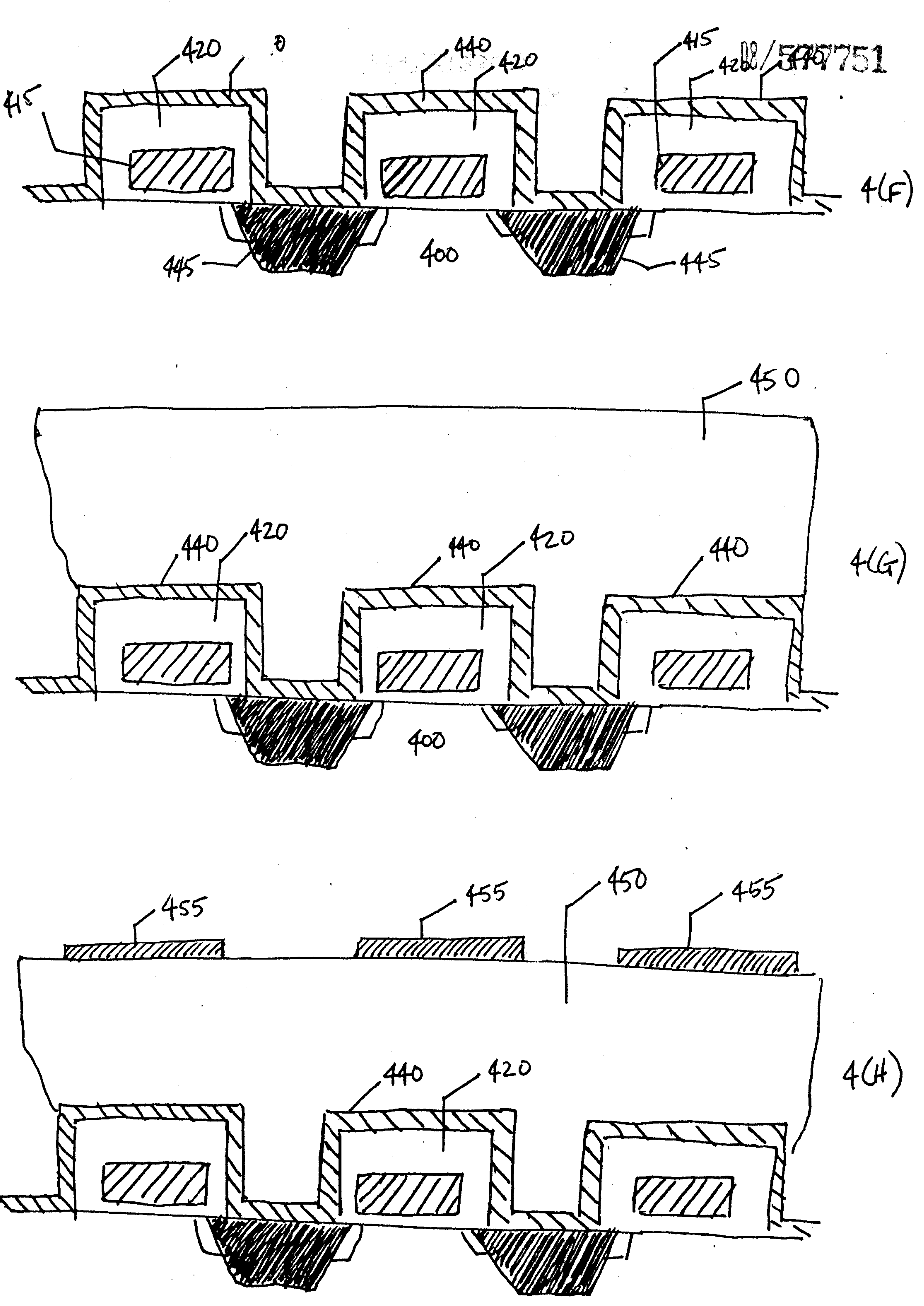

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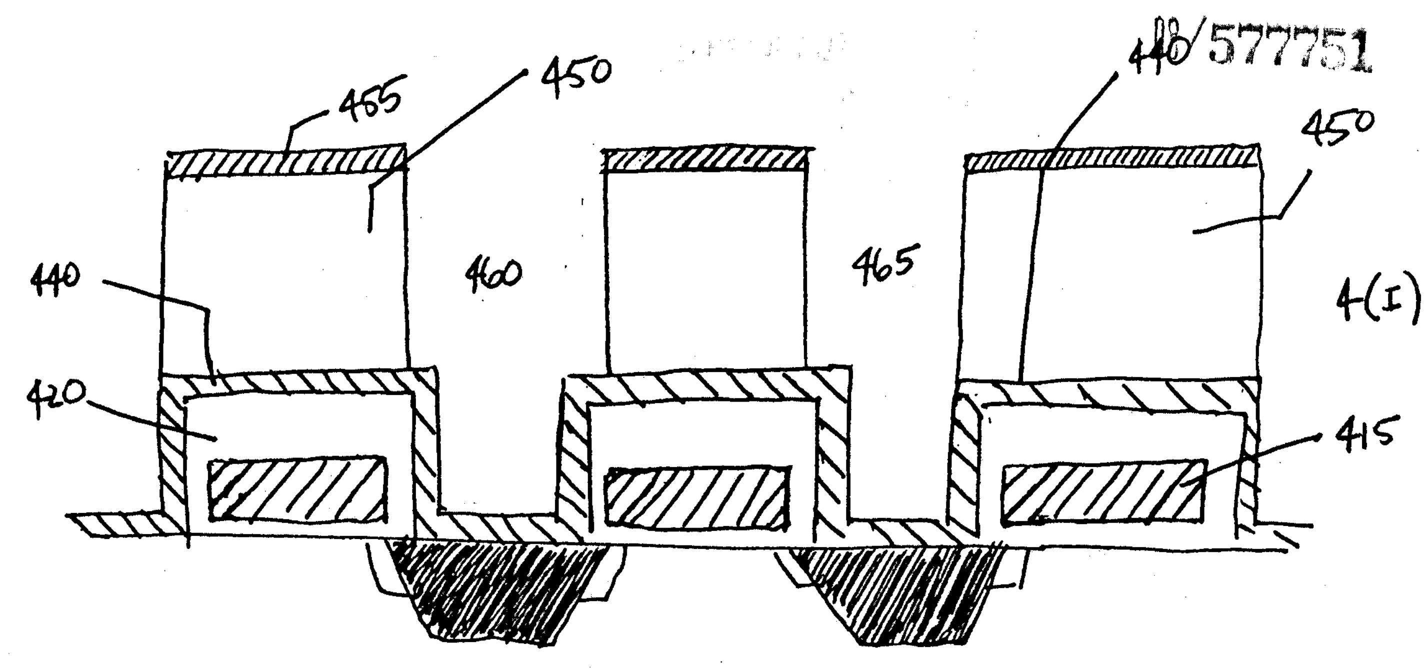

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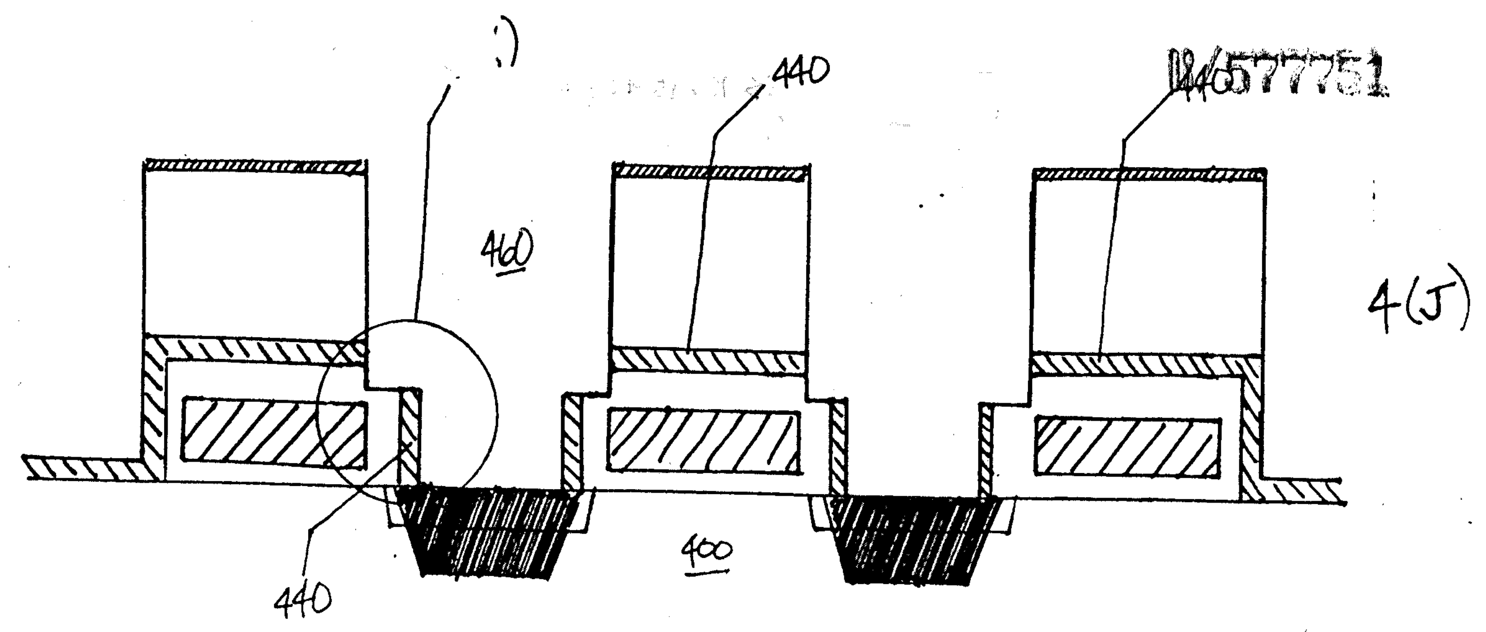
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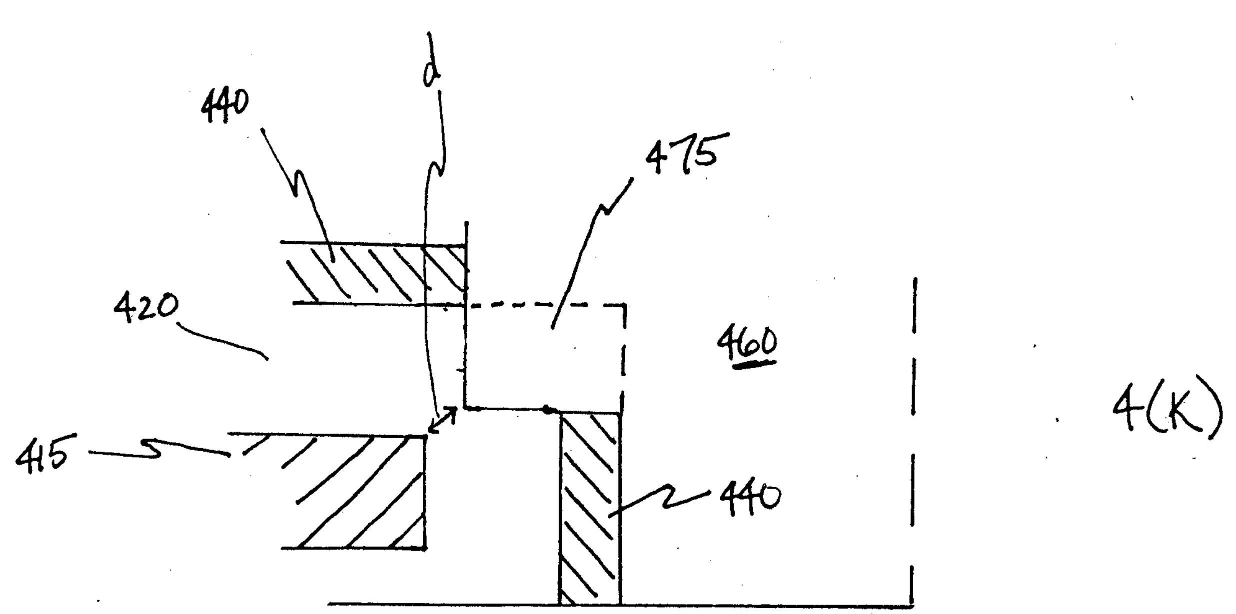
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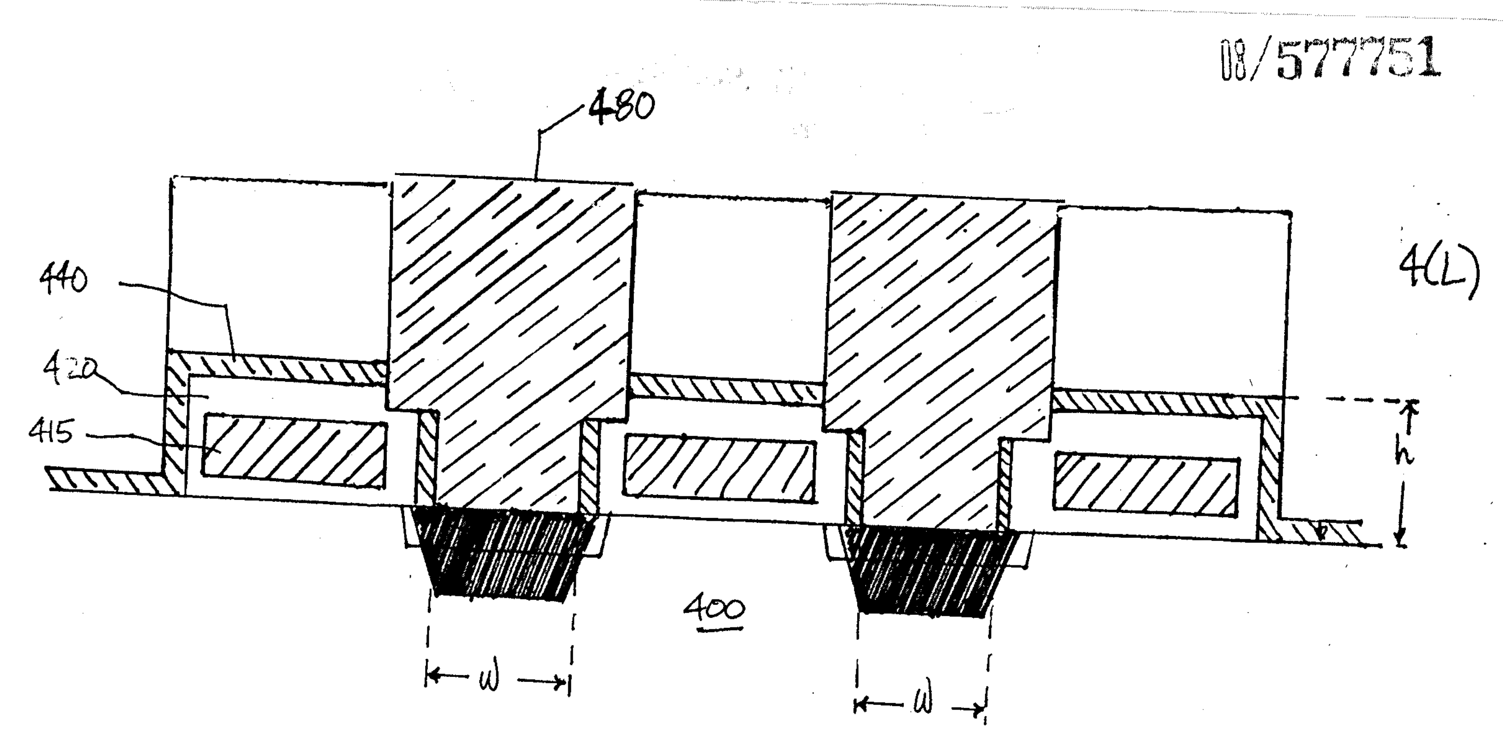
08/577751



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08/577751

257/433
Abraham

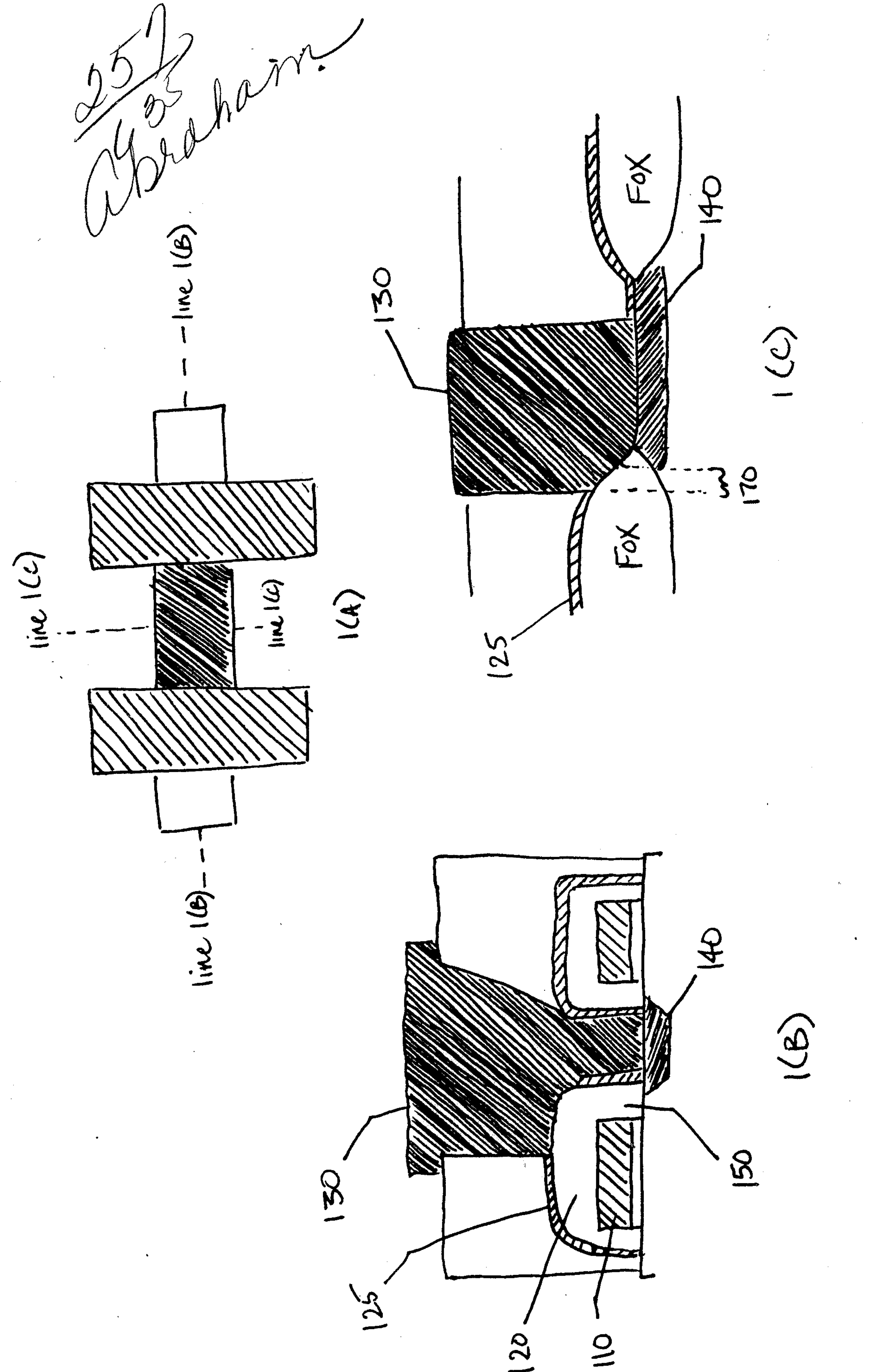

FIGURE 1

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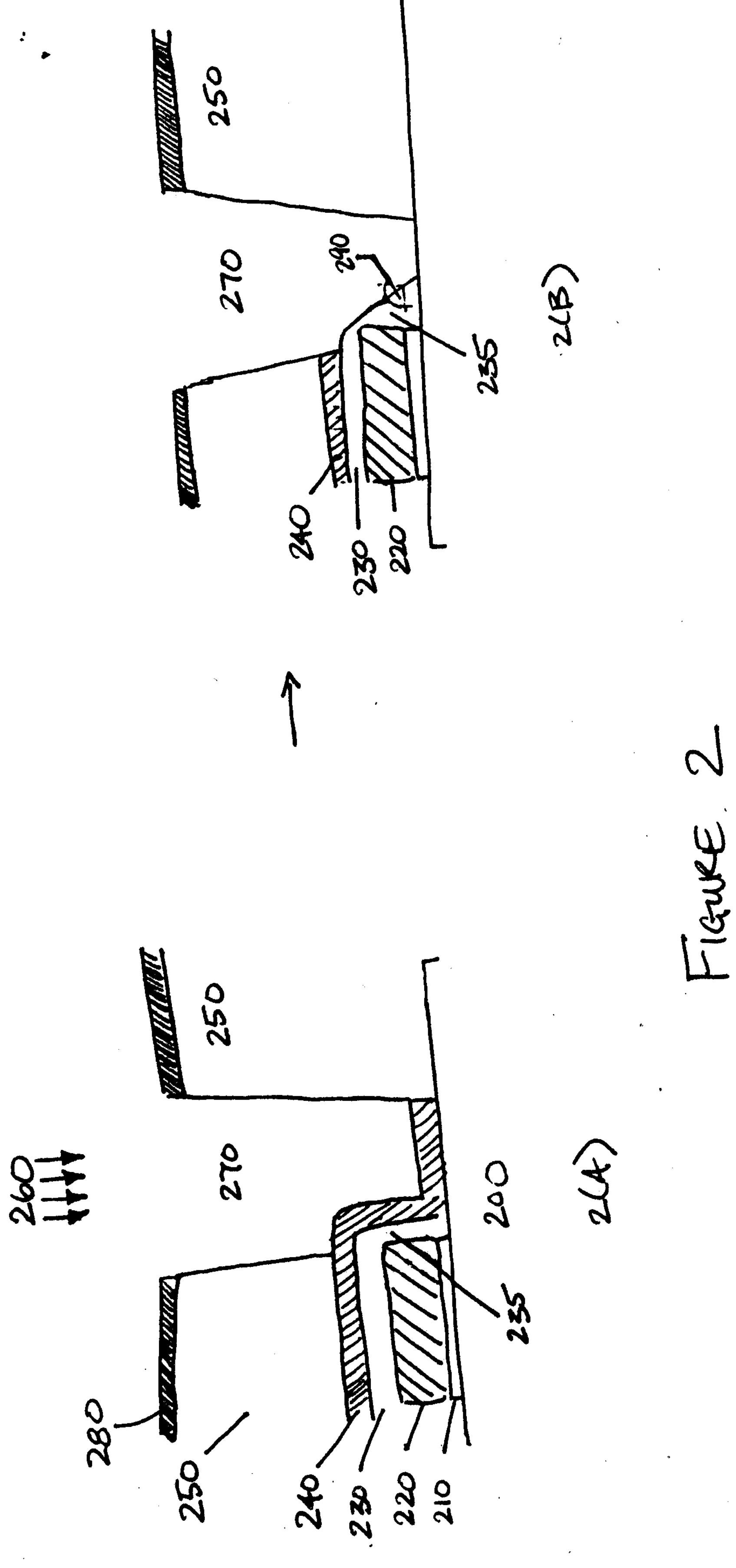

FIGURE 2

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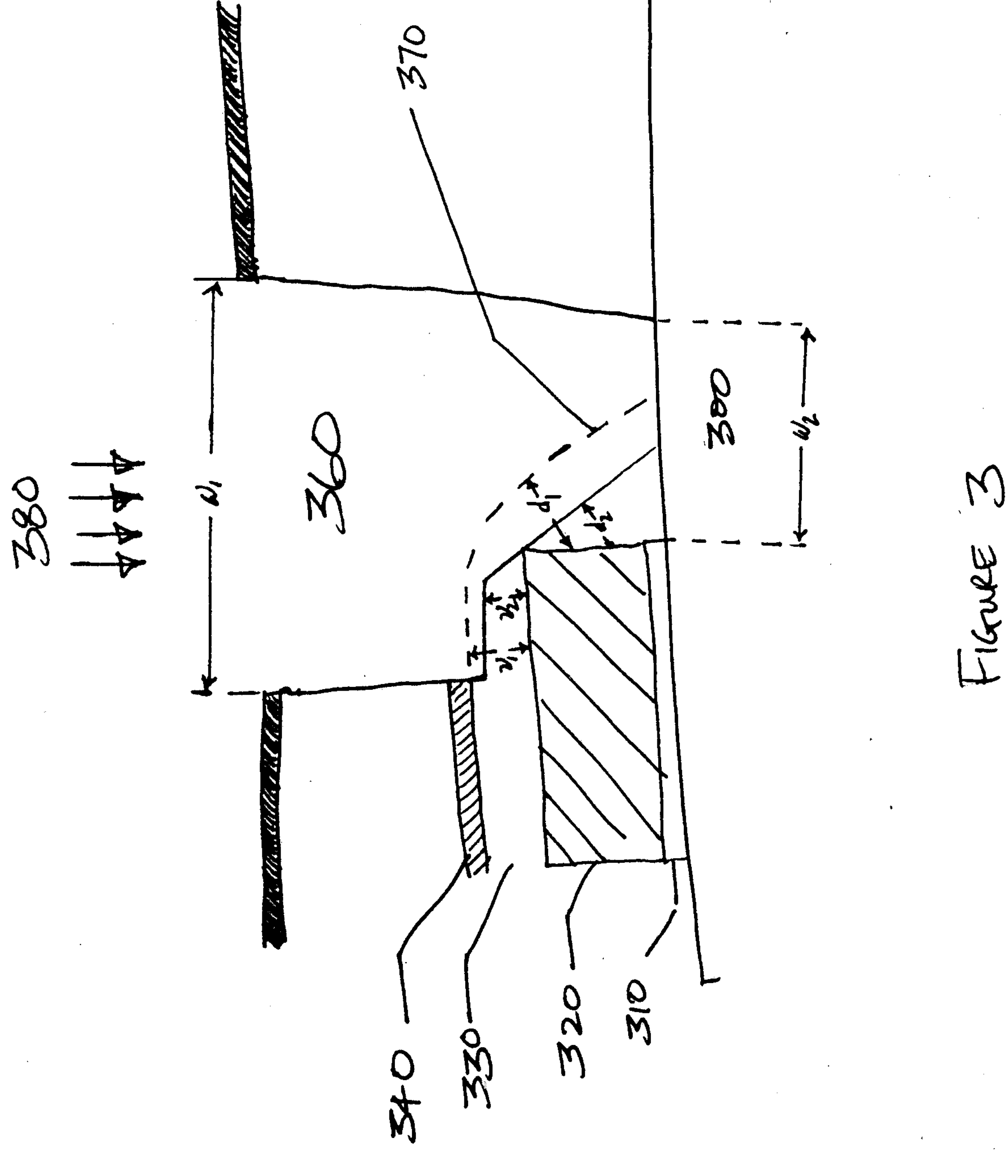

FIGURE 3

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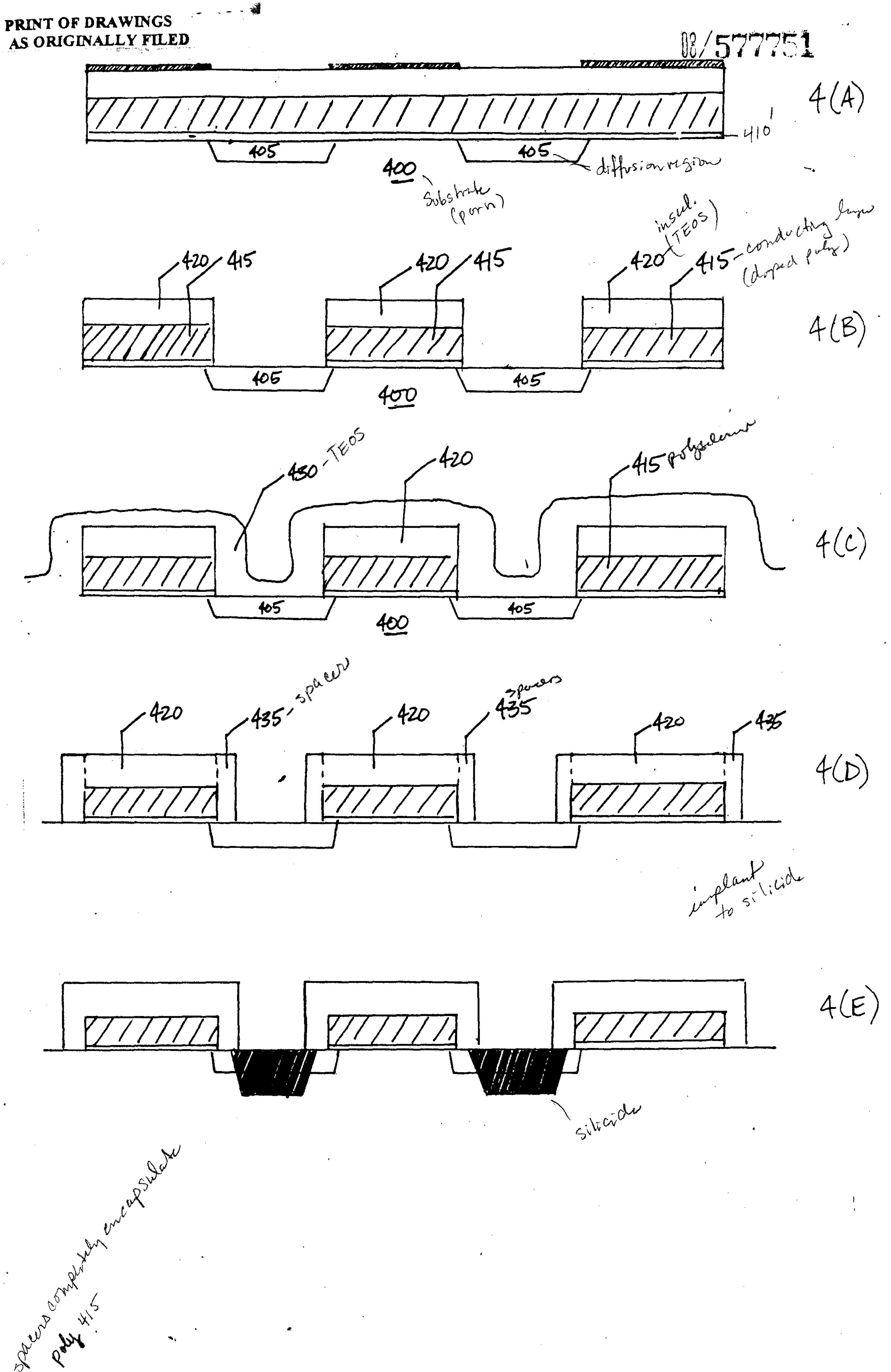

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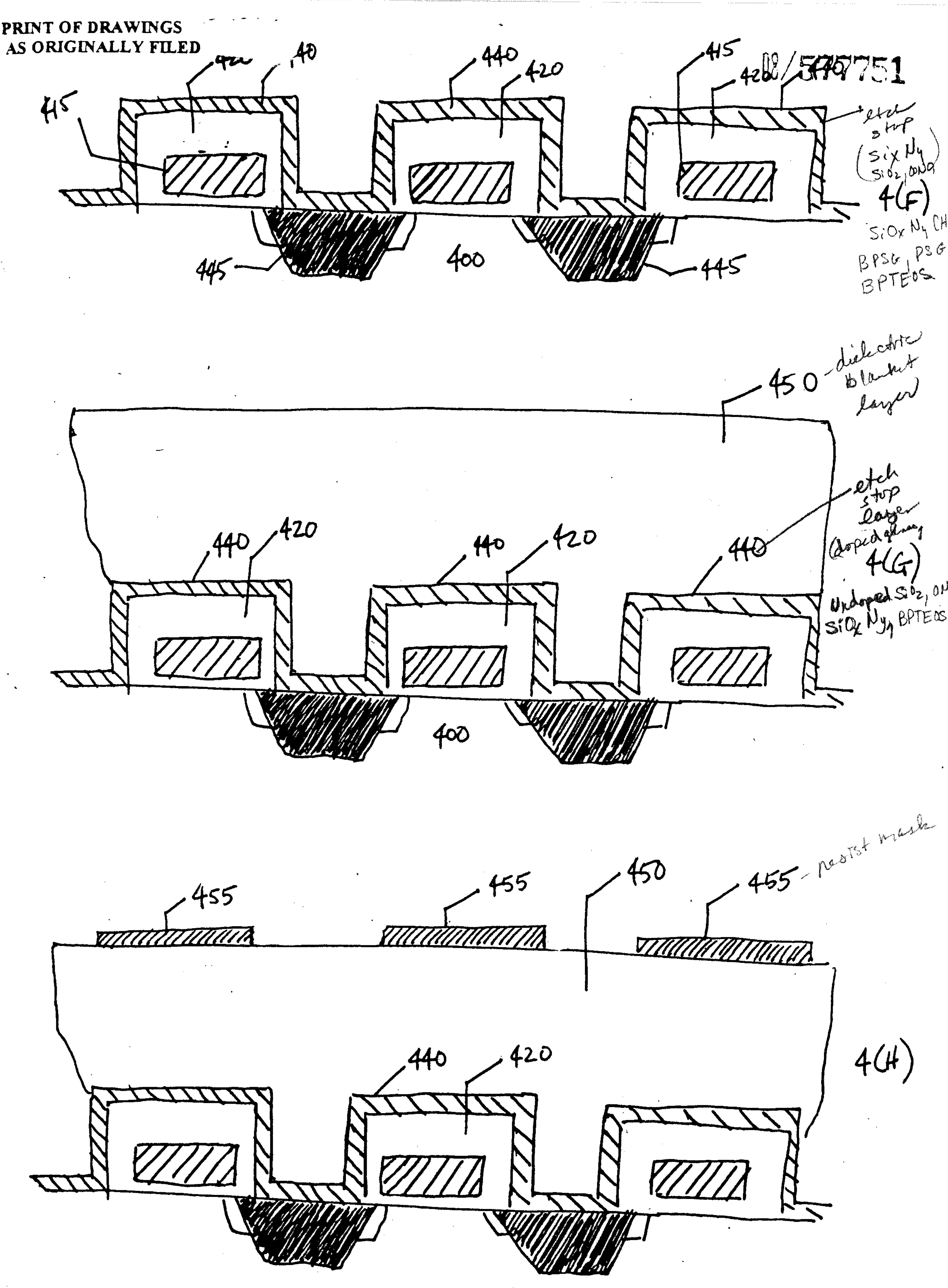

FIGURE 4 (cont.)

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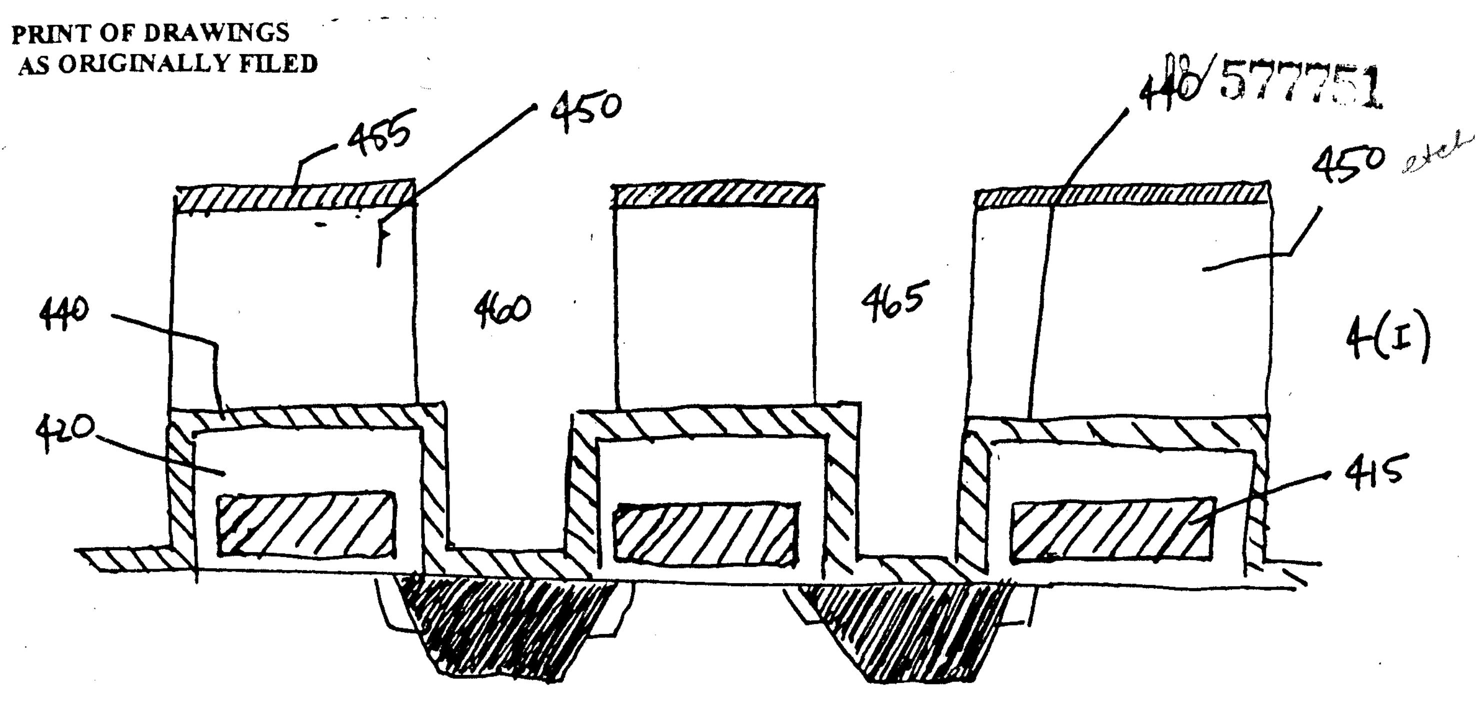
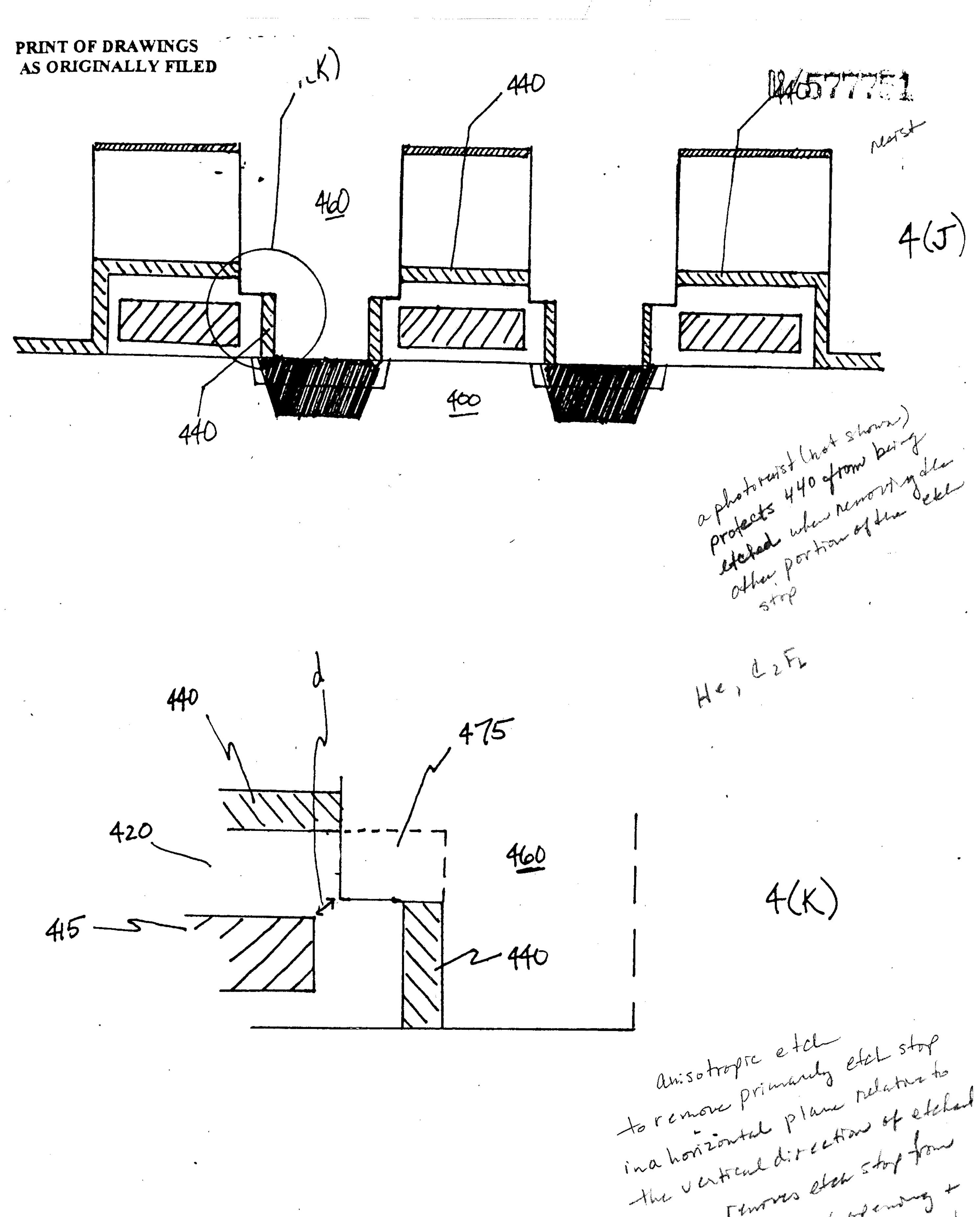


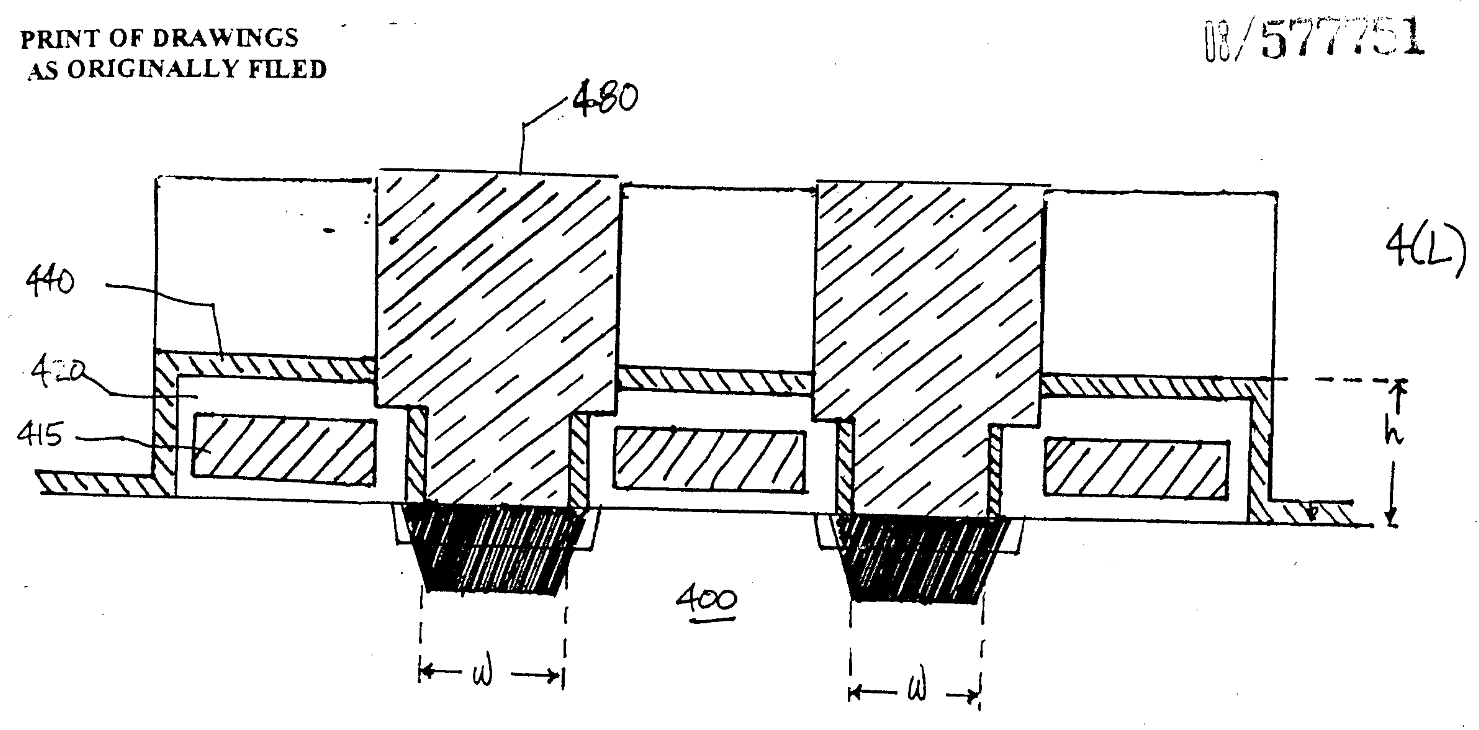
FIGURE 4 (cont.)



anisotropic etch to remove primarily etch stop in a horizontal plane relative to the vertical direction of etchant ions, removes etch stop from base of contact opening + does not remove all of etch stop material adjacent to the spacer portion of the TEOS layer 420

PRINT OF DRAWINGS
AS ORIGINALLY FILED

08/577751



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
08/577,751	12/22/95	NULTY J	16820.P097

0252/0403

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BLVD
SEVENTH FLOOR
LOS ANGELES CA 90025

0000

DATE MAILED: 04/03/96

NOTICE TO FILE MISSING PARTS OF APPLICATION
FILING DATE GRANTED

An Application Number and Filing Date have been assigned to this application. However, the items indicated below are missing. The required items and fees identified below must be timely submitted **ALONG WITH THE PAYMENT OF A SURCHARGE** for items 1 and 3-6 only of $ 130 for large entities or $ 65 for small entities who have filed a verified statement claiming such status. The surcharge is set forth in 37 CFR 1.16(e).

If all required items on this form are filed within the period set below, the total amount owed by applicant as a ☑ large entity, ☐ small entity (verified statement filed), is $ 130.

Applicant is given **ONE MONTH FROM THE DATE OF THIS LETTER, OR TWO MONTHS FROM THE FILING DATE** of this application, **WHICHEVER IS LATER,** within which to file all required items and pay any fees required above to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

1. ☐ The statutory basic filing fee is: ☐ missing ☐ insufficient. Applicant as a ☐ large entity ☐ small entity, must submit $______ to complete the basic filing fee.

2. ☐ Additional claim fees of $______ as a ☐ large entity, ☐ small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

3. ☐ The oath or declaration:
   ☐ is missing.
   ☐ does not cover items omitted at time of execution.

   An oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date is required.

4. ☐ The oath or declaration does not identify the application to which it applies. An oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

5. ☑ The signature(s) to the oath or declaration is/are: ☑ missing; ☐ by a person other than the inventor or a person qualified under 37 CFR 1.42, 1.43, or 1.47. A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

6. ☐ The signature of the following joint inventor(s) is missing from the oath or declaration:

   ______ An oath or declaration listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

7. ☐ The application was filed in a language other than English. Applicant must file a verified English translation of the application and a fee of $______ under 37 CFR 1.17(k), unless this fee has already been paid.

8. ☐ A $______ processing fee is required since your check was returned without payment. (37 CFR 1.21(m)).

9. ☐ Your filing receipt was mailed in error because your check was returned without payment.

10. ☐ The application does not comply with the Sequence Rules. See attached Notice to Comply with Sequence Rules 37 CFR 1.821-1.825.

11. ☐ Other.

Direct the response and any questions about this notice to, Attention: Application Processing Division, Special Processing and Correspondence Branch (703) 308-1202.

#3

Our Ref.: 16820.P097

MAIL ROOM
MAY 6 1996
47 PAT. & TRADEMARK OFF.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

James E. Nulty, Christopher J. Petti

Serial No.: 08/577,751

Filed: December 22, 1995

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Examiner:

Art Group:

RESPONSE TO NOTICE TO FILE MISSING PARTS OF APPLICATION

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Sir:

In response to the communication from the Patent Office dated April 3, 1996, on the above-referenced utility patent application, enclosed herewith are Form PTO-1533, the executed Declaration and Power of Attorney, and our check numbered 2600 in the amount of one hundred thirty dollars ($130.00) as the total amount owed for a large entity. Please charge any additional fees to Deposit Account No. 02-2666. A duplicate of this sheet is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: 5/3/96

By: William T Babbitt
William Thomas Babbitt; Reg. No. 39,591

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on May 3, 1996.

Nadya Gordon 5/3/96
Nadya Gordon *Date*

Restriction to one of the following inventions is required under 35 U.S.C. § 121:

I. Claims 23-26, drawn to a semiconductor device or devices and a precursor for coating such devices, classified in Class 257, subclass 635.

II. Claims 1-22, drawn to a process or processes for making semiconductor devices, classified in Class 437, subclass 228.

The inventions are distinct, each from the other, because of the following reason:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different products, or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case unpatentability of the Group I invention would not necessarily imply unpatentability of the Group II invention, because the device of the Group I invention could be made by a process or process materially different from that/those of the Group II invention. For example, the layers claimed could be made by a process which includes an etching step which does significantly erode the spacer.

SAMSUNG-1008.063

Because these inventions are distinct for the reason given above, and as shown by the above different classifications, the fields of search are not co-extensive and separate examination would be required, restriction for examination purposes as indicated is proper.

Applicant is advised that the response to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR § 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR § 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently-filed petition under 37 CFR § 1.48(b) and by the fee required under 37 CFR § 1.17(h).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham , whose telephone number is (703) 305-3793.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, whose telephone number is (703) 308-0956.

130./105 #3

Our Ref.: 16820.P097

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Examiner:
James E. Nulty, Christopher J. Petti	Art Group:
Serial No.: 08/577,751	
Filed: December 22, 1995	
For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING	

RESPONSE TO NOTICE TO FILE MISSING PARTS OF APPLICATION

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Sir:

In response to the communication from the Patent Office dated April 3, 1996, on the above-referenced utility patent application, enclosed herewith are Form PTO-1533, the executed Declaration and Power of Attorney, and our check numbered 2600 in the amount of one hundred thirty dollars ($130.00) as the total amount owed for a large entity. Please charge any additional fees to Deposit Account No. 02-2666. A duplicate of this sheet is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: 5/3/96

By: [signature]
William Thomas Babbitt; Reg. No. 39,591

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on May 3, 1996.

[signature] 5/3/96
Nadya Gordon *Date*

070 WJ 05/13/96 08577751

1 105 130.00 CK

Restriction to one of the following inventions is required under 35 U.S.C. § 121:

I. Claims 23-26, drawn to a semiconductor device or devices and a precursor for coating such devices, classified in Class 257, subclass 635.

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Because these inventions are distinct for the reason given above, and as shown by the above different classifications, the fields of search are not co-extensive and separate examination would be required, restriction for examination purposes as indicated is proper.

Applicant is advised that the response to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR § 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR § 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently-filed petition under 37 CFR § 1.48(b) and by the fee required under 37 CFR § 1.17(h).

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Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, whose telephone number is (703) 308-0956.

#3

MAIL ROOM
MAY 6 1996
PAT. & TRADEMARK OFC.

Our Ref.: 016820.P097

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

the specification of which

______ is attached hereto.
XXXX was filed on December 22, 1995 as
Application Serial No. 08/577,751
and was amended on ______________
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I do not know and do not believe that the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119, of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) — Priority Claimed

(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

SAMSUNG-1008.068

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, a firm including: Keith G. Askoff, Reg. No. 33,828; Aloysius T.C. AuYeung, Reg. No. 35,432; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; William D. Davis, Reg. No. 38,428; Daniel M. De Vos, Reg. No. 37,813; Scot A. Griffin, Reg. No. 38,167; David R. Halvorson, Reg. No. 33,395; Brian D. Hickman, Reg. No. 35,894; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; Stephen L. King, Reg. No. 19,180; Daniel C. Mallery, Reg. No. 33,532; Michael J. Mallie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Edward W. Scott IV, Reg. No. 36,000; Maria E. Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; John C. Stattler, Reg. No. 36,285; David R. Stevens, Reg. No. 38,626; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Gary B. Goates, Reg. No. 35,159; Thomas X. Li, Reg. No. 37,079; and Edwin A. Sloane, Reg. No. 34,728; my patent agents, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

34

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1-00

Full Name of Sole/First Inventor James E. Nulty

Inventor's Signature [signature] Date 4/26/96

Residence San Jose, California 95128 Ca Citizenship U.S.A.
(City, State) (Country)

Post Office Address 1037 Lenor Way
San Jose, California 95128

SAMSUNG-1008.069

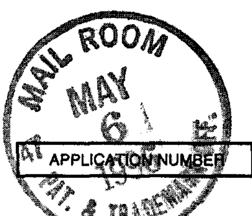
Full Name of Sole/First Inventor Christopher J. Petti

Inventor's Signature [signature] Date 4/26/96

Residence Mountain View, California 94041 Ca Citizenship U.S.A.
(City, State) (Country)

Post Office Address 660 Sierra Avenue
Mountain View, California 94041

SAMSUNG-1008.070



#3

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
08/577,751	12/22/95	NULTY	J 16820.P09

0252/0403

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BLVD
SEVENTH FLOOR
LOS ANGELES CA 90025

DATE MAILED: 0000

04/03/96

NOTICE TO FILE MISSING PARTS OF APPLICATION
FILING DATE GRANTED

An Application Number and Filing Date have been assigned to this application. However, the items indicated below are missing. The required items and fees identified below must be timely submitted **ALONG WITH THE PAYMENT OF A SURCHARGE** for items 1 and 3-6 only of $ 130 for large entities or $ 65 for small entities who have filed a verified statement claiming such status. The surcharge is set forth in 37 CFR 1.16(e).

If all required items on this form are filed within the period set below, the total amount owed by applicant as a ☑ large entity, ☐ small entity (verified statement filed), is $ 130 .

Applicant is given **ONE MONTH FROM THE DATE OF THIS LETTER, OR TWO MONTHS FROM THE FILING DATE** of this application, **WHICHEVER IS LATER,** within which to file all required items and pay any fees required above to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

1. ☐ The statutory basic filing fee is: ☐ missing ☐ insufficient. Applicant as a ☐ large entity ☐ small entity, must submit $________ to complete the basic filing fee.

2. ☐ Additional claim fees of $________ as a ☐ large entity, ☐ small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.

3. ☐ The oath or declaration:
   ☐ is missing.
   ☐ does not cover items omitted at time of execution.

   An oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date is required.

4. ☐ The oath or declaration does not identify the application to which it applies. An oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

5. ☑ The signature(s) to the oath or declaration is/are: ☑ missing; ☐ by a person other than the inventor or a person qualified under 37 CFR 1.42, 1.43, or 1.47. A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

6. ☐ The signature of the following joint inventor(s) is missing from the oath or declaration:

   ________ An oath or declaration listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

7. ☐ The application was filed in a language other than English. Applicant must file a verified English translation of the application and a fee of $________ under 37 CFR 1.17(k), unless this fee has already been paid.

8. ☐ A $________ processing fee is required since your check was returned without payment. (37 CFR 1.21(m)).

9. ☐ Your filing receipt was mailed in error because your check was returned without payment.

10. ☐ The application does not comply with the Sequence Rules. See attached Notice to Comply with Sequence Rules 37 CFR 1.821-1.825.

11. ☐ Other.

Direct the response and any questions about this notice to, Attention: Application Processing Division, Special Processing and Correspondence Branch (703) 308-1202.

A copy of this notice MUST be returned with the response.

MAIL ROOM
AUG 19 1996
39
PAT. & TRADEMARK OFF.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#4

Applicant: James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

Serial No.: 08/577,751 Filed: December 22, 1995

Examiner: Unknown Group Art Unit: 2503

Attorney Docket No.: 16820.P097

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D. C. 20231

RECEIVED
SEP 04 1996
GROUP 2500

REVOCATION OF POWER OF ATTORNEY
AND APPOINTMENT OF NEW ATTORNEY

Sir:

Cypress Semiconductor Corporation ("Assignee") represents that it is the owner of the entire right, title and interest throughout the world in the above-cited application by virtue of an assignment, a copy of which is attached hereto, executed on April 26, 1996. Pursuant to 37 C.F.R. § 3.73(b), Assignee certifies that the evidentiary documents evidencing Assignee's ownership of the above-cited application have been reviewed and that, to the best of Assignee's knowledge and belief, title is in Assignee.

Assignee hereby revokes the Power of Attorney given on April 26, 1996, to Keith G. Askoff, Reg. No. 33,828; Aloysius T.C. AuYeung, Reg. No. 35,432; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; William Davis, Reg. No. 38,428;

Daniel M. De Vos, Reg. No. 37,813; Scot A. Griffin, Reg. No. 38,167; David R. Halvorson, Reg. No. 33,395; Brian D. Hickman, Reg. No. 35,894; George W. Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; Stephen L. King, Reg. No. 19,180; Daniel C. Mallery, Reg. No. 33,532; Michael J. Mallie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Edward W. Scott IV, Reg. No. 36,000; Maria E. Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; John C. Stattler, Reg. No. 36,285; David R. Stevens, Reg. No. 38,626; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; Ben J. Yorks, Reg. No. 33,609; Norman Zafman, Reg. No. 26,250; Gary B. Goates, Reg. No. 35,159; Thomas X. Li, Reg. No. 37,079; and Edwin A. Sloane, Reg. No. 34,728 of the law firm of Blakely, Sokoloff, Taylor & Zafman, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 to prosecute the above-cited application for letters patent and hereby appoints the following attorney, with full power: David R. Graham, Reg. No. 36,150. The appointed attorney is to have full power to prosecute said application; to make alterations and amendments therein; to receive all notices, communications and said Letters Patent at the address indicated above; and to transact all business in the U.S Patent and Trademark Office in connection therewith.

Please address all further correspondence in this application to:

PA1\527138.01

David R. Graham, Esq.
GRAY CARY WARE & FREIDENRICH
400 Hamilton Avenue
Palo Alto, CA 94301

I, Andrew D. Fortney, represent that I am Manager, Intellectual Property of Cypress Semiconductor Corporation and am a representative authorized to sign on behalf of Cypress Semiconductor Corporation. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: August 12, 1996

By: [signature]
Andrew D. Fortney, Ph.D., Esq.
Manager, Intellectual Property
Cypress Semiconductor Corporation
3901 N. First Street
San Jose, CA 95134

PA1\527138.01

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/577,751	12/22/95	James E. Chulty	

EXAMINER	
Abraham	
ART UNIT	PAPER NUMBER
2508	5

DATE MAILED: Sept. 25, 1996

This is in response to the Power of Attorney filed August 19, 1996.

☐ 1. The Power of Attorney to you in this application **has been revoked** by the applicant. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.

☐ 2. The Power of Attorney to you in this application **has been revoked** by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record. (37 CFR 1.33).

☐ 3. The withdrawal as attorney in this application **has been accepted.** Future correspondence will be mailed to the new address of record. 37 CFR 1.33.

This is a communication from the
Patent and Trademark Office

☐ 4. The Power of Attorney in this application **is accepted.** Correspondence in this application will be mailed to the below-noted address as provided by 37 CFR 1.33.

☑ 5. The Power of Attorney in this application **is not accepted** for the reason(s) checked below:

☑ a. The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73 (b) has not been received.

☐ b. The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.

☐ c. The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.

☐ d. The signature of ______, a co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor.

☐ e. The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent & Trademark Office.

☐ f. The revocation is not signed by the applicant, the assignee of the entire interest, or <u>one</u> particular principal attorney having the authority to revoke.

David R. Graham, Esq.
Gary Cary Ware & Freidenrich
400 Hamilton Ave.
Palo Alto, CA 94301

Lavonna Murphy

This is a communication from the
Patent and Trademark Office

ATTORNEYS AT LAW
400 HAMILTON AVENUE
PALO ALTO, CA 94301-1825
TEL (415) 328-6561
FAX (415) 327-3699
http://www.gcwf.com

#6

FAX TRANSMISSION COVER SHEET

October 11, 1996

To:	Firm/Company/Telephone:	Fax Number:
Jawonna Murphy	Patent and Trademark Office 703/308-4929	703/308-7722

From: Denise Lade

Client-Matter Number: 1030917-991120

Re: Rev. of Power of Attorney

Pages: - 8 - (including this form)

Original: ☐ will be mailed ☒ will not be mailed

If there is a problem with this transmission, please call (415) 833-2200
Fax Operator/Ext.

Message:

Ms. Murphy

Per our conversation of October 10, 1996, I am faxing you copies of PTOL-305, return receipt postcard and Revocation of Power of Attorney and Appointment of New Attorney along with a copy of the Assignment that was inadvertently left out of the mailing to the PTO on August 15, 1996.

Per our conversation of October 10, 1996, you said this would be sufficient to have the Revocation of Power of Attorney and Appointment of New Attorney accepted. If more information is needed, please give me a call.

FAX COPY RECEIVED
OCT 1 1 1996
GROUP 2500

CONFIDENTIALITY NOTICE

This communication is ONLY for the person named above. Unless otherwise indicated, it contains information that is confidential, privileged or exempt from disclosure under applicable law. If you are not the person named above, or responsible for delivering it to that person, be aware that disclosure, copying, distribution or use of this communication is strictly PROHIBITED. If you have received it in error, or are uncertain as to its proper handling, please immediately notify us by collect telephone and mail the original to us at the above address. Thank you.

(Form Rev. 6/10/96)

1030917-991120

RECEIVED SEP 27 1996 GRAY CARY WARE & FREIDENRICH

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/577,751	12/22/95	James E. Chutty	

RECEIVED SEP 30 1996 GRAY CARY WARE & FREIDENRICH

EXAMINER	
Abraham	
ART UNIT	PAPER NUMBER
2508	5

DATE MAILED: Sept. 05, 1996

This is in response to the Power of Attorney filed August 19, 1996.

☐ 1. The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.

☐ 2. The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record. (37 CFR 1.33).

☐ 3. The withdrawal as attorney in this application has been accepted. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.

This is a communication from the Patent and Trademark Office

☐ 4. The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the below-noted address as provided by 37 CFR 1.33.

☑ 5. The Power of Attorney in this application is not accepted for the reason(s) checked below:

☑ a. The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73 (b) has not been received.

☐ b. The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.

☐ c. The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.

☐ d. The signature of __________, a co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor.

☐ e. The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent & Trademark Office.

☐ f. The revocation is not signed by the applicant, the assignee of the entire interest, or one particular principal attorney having the authority to revoke.

PATENT DOCKET
U.S.: FOREIGN:
DOCKETED: 9/30/96 BY: [illegible]
ACTION: [illegible]
DUE DATES: [illegible] 6/22/97
ATTY: DRG C/M #:

David R. Graham, Esq.
Gray Cary Ware & Freidenrich
400 Hamilton Ave.
Palo Alto, CA 94301

Lawrence Murphy
This is a communication from the Patent and Trademark Office

FORM PTOL-308 (REV. 10-84) THIS COY FOR NEW ATTORNEY/AGENT COPY C

: Commissioner of Patents and Trademarks
Washington, D.C. 20231

FILE COPY

Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Serial No.: 08/577,751
Filing Date: December 22, 1995
Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

Enclosed:

Revocation of Power of Attorney and Appointment of New Attorney (3 pgs) and Return Postcard

1030917-991120 (16820.P097)
DRG:dml August 15, 1996

: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Serial No.: 08/577,751
Filing Date: December 22, 1995
Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

RECEIVED
SEP 03 1996

Enclosed:

Revocation of Power of Attorney and Appointment of New Attorney (3 pgs) and Return Postcard

1030917-991120 (16820.P097)
DRG:dml August 15, 1996

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

Serial No.: 08/577,751 Filed: December 22, 1995

Examiner: Unknown Group Art Unit: 2503

Attorney Docket No.: 16820.P097

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D. C. 20231

REVOCATION OF POWER OF ATTORNEY
AND APPOINTMENT OF NEW ATTORNEY

Sir:

Cypress Semiconductor Corporation ("Assignee") represents that it is the owner of the entire right, title and interest throughout the world in the above-cited application by virtue of an assignment, a copy of which is attached hereto, executed on April 26, 1996. Pursuant to 37 C.F.R. § 3.73(b), Assignee certifies that the evidentiary documents evidencing Assignee's ownership of the above-cited application have been reviewed and that, to the best of Assignee's knowledge and belief, title is in Assignee.

Assignee hereby revokes the Power of Attorney given on April 26, 1996, to Keith G. Askoff, Reg. No. 33,828; Aloysius T.C. AuYeung, Reg. No. 35,432; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; William Davis, Reg. No. 38,428;

SAMSUNG-1008.079

Daniel M. De Vos, Reg. No. 37,813; Scot A. Griffin, Reg. No. 38,167; David R. Halvorson, Reg. No. 33,395; Brian D. Hickman, Reg. No. 35,894; George W. Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; Stephen L. King, Reg. No. 19,180; Daniel C. Mallery, Reg. No. 33,532; Michael J. Mallie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Edward W. Scott IV, Reg. No. 36,000; Maria E. Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; John C. Stattler, Reg. No. 36,285; David R. Stevens, Reg. No. 38,626; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; Ben J. Yorks, Reg. No. 33,609; Norman Zafman, Reg. No. 26,250; Gary B. Goates, Reg. No. 35,159; Thomas X. Li, Reg. No. 37,079; and Edwin A. Sloane, Reg. No. 34,728 of the law firm of Blakely, Sokoloff, Taylor & Zafman, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 to prosecute the above-cited application for letters patent and hereby appoints the following attorney, with full power: David R. Graham, Reg. No. 36,150. The appointed attorney is to have full power to prosecute said application; to make alterations and amendments therein; to receive all notices, communications and said Letters Patent at the address indicated above; and to transact all business in the U.S Patent and Trademark Office in connection therewith.

Please address all further correspondence in this application to:

SAMSUNG-1008.080

David R. Graham, Esq.
GRAY CARY WARE & FREIDENRICH
400 Hamilton Avenue
Palo Alto, CA 94301

I, Andrew D. Fortney, represent that I am Manager, Intellectual Property of Cypress Semiconductor Corporation and am a representative authorized to sign on behalf of Cypress Semiconductor Corporation. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: August 12, 1996

By: [signature]
Andrew D. Fortney, Ph.D., Esq.
Manager, Intellectual Property
Cypress Semiconductor Corporation
3901 N. First Street
San Jose, CA 95134

PA1\527138.01

Our Docket No.: 16820.P097

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

James E. Nulty, Christopher J. Petti

Serial No.: 08/577,751

Filed: December 22, 1995

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Examiner:

Art Group:

ASSIGNMENT SUBMITTAL

Recordation Form Cover Sheet - Patent Application (Previously Filed)

The Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

Submitted herewith is an Assignment for filing in connection with the above-captioned application. The parties assigning the interest are as follows:

Name(s): James E. Nulty and Christopher J. Petti

The party receiving the interest (Assignee) is as follows:

Name: CYPRESS SEMICONDUCTOR CORPORATION
Address: 3901 North First Street, San Jose, California 95134

The Assignment was executed on April 26, 1996.

The recordation fee of $40.00 for the recordation of one (1) Assignment is submitted herewith. Please charge any additional amounts due or credit any over-payment to Deposit Account 02-2666.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Correspondence concerning this document should be mailed to the undersigned.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

By: [signature]
William Thomas Babbitt; Reg. No. 39,591

Dated: 5/3/96

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington D.C. 20231 on May 3, 1996.

[signature] 5/3/96
Nadya Gordon Date

Total number of pages including cover sheet, attachments and document: 2

ASSIGNMENT

In consideration of good and valuable consideration, the receipt of which is hereby acknowledged, We, the undersigned, James E. Nulty and Christopher J. Petti

Hereby sell, assign, and transfer to: CYPRESS SEMICONDUCTOR CORPORATION a corporation of Delaware, having a principal place of business at: 3901 North First Street, San Jose, California 95134 ("Assignee"); its successors, assigns and legal representatives, the entire right, title and interest for the United States and all foreign countries, in and to any and all improvements which are disclosed in the application for United States Letters Patent,

[ ] which has been executed by the undersigned concurrently herewith,

[X] which was filed December 22, 1995 and assigned Serial No. 08/577,751

and is entitled: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

and in and to said application and all divisional, continuing, substitute, renewal, reissue, and all other applications for Letters Patent which have been or shall be filed in the United States and all foreign countries on any of said improvements; and in and to all original and reissued patents which have been or shall be issued in the United States and all foreign countries on said improvements; and in and to all rights of priority resulting from the filing of said United States application;

Agree that said Assignee may apply for and receive Letters Patent for said improvements in its own name; and that, when requested, without charge to, but at the expense of, said Assignee, its successors, assigns and legal representatives, to carry out in good faith the intent and purpose of this Assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all said improvements; execute all rightful oaths, assignments powers of attorney and other papers; communicate to said Assignee, its successors, assigns, and representatives, all facts known to the undersigned relating to said improvements and the history thereof; and generally do everything possible which said Assignee, its successors, assigns or representatives shall consider desirable for aiding in securing and maintaining proper patent protection for said improvements and for vesting title to said improvements and all applications for patents and all patents on said improvements, in said Assignee, its successors, assigns and legal representatives; and

Covenant with said Assignee, its successors, assigns and legal representatives that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

Date: 4/26/96 — Name: James E. Nulty

Date: 4/26/96 — Name: Christopher J. Petti

Docket No. 016820.P097

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/577751	12/22/95	NULTY	16820.P097

EXAMINER: ABRAHAM, FETSUM

ART UNIT / PAPER NUMBER: 2508 / 7

DAVID R. GRAHAM, ESQ.
GARY CARY WARE & FREIDENRICH
400 HAMILTON AVENUE
PALO ALTOES CA 94301

DATE MAILED: 10/22/96

This is in response to the Power of Attorney filed 10/11/96.

☐ 1. The Power of Attorney to you in this application **has been revoked** by the applicant. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.

☑ 2. The Power of Attorney to you in this application **has been revoked** by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record. (37 CFR 1.33).

☐ 3. The withdrawal as attorney in this application **has been accepted.** Future correspondence will be mailed to the new address of record. 37 CFR 1.33.

This is a communication from the Patent and Trademark Office

☑ 4. The Power of Attorney in this application **is accepted.** Correspondence in this application will be mailed to the below-noted address as provided by 37 CFR 1.33.

☐ 5. The Power of Attorney in this application **is not accepted** for the reason(s) checked below:

☐ a. The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73 (b) has not been received.

☐ b. The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.

☐ c. The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.

☐ d. The signature of ______________________, a co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor.

☐ e. The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent & Trademark Office.

☐ f. The revocation is not signed by the applicant, the assignee of the entire interest, or <u>one</u> particular principal attorney having the authority to revoke.

DAVID R. GRAHAM, ESQ.
GARY CARY WARE & FREIDENRICH
400 HAMILTON AVENUE
PALO ALTOS CA 94301

This is a communication from the Patent and Trademark Office

UNITED ST 'S DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
08/577,751	12/22/95	NULTY J	16820.P097

EXAMINER: ABRAHAM, F

B5M2/1112

DAVID R. GRAHAM, ESQ.
GARY CARY WARE & FREIDENRICH
400 HAMILTON AVENUE
PALO ALTOS CA 94301

ART UNIT	PAPER NUMBER
2508	8

DATE MAILED: 11/12/96

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☐ Responsive to communication(s) filed on ______.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire one month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-26 is/are pending in the application.
Of the above, claim(s) ______ is/are withdrawn from consideration.
☐ Claim(s) ______ is/are allowed.
☐ Claim(s) ______ is/are rejected.
☐ Claim(s) ______ is/are objected to.
☒ Claim(s) 1-26 are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
☐ The drawing(s) filed on ______ is/are objected to by the Examiner.
☐ The proposed drawing correction, filed on ______ is ☐ approved ☐ disapproved.
☐ The specification is objected to by the Examiner.
☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.
☐ received in Application No. (Series Code/Serial Number) ______.
☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: ______.

☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of Reference Cited, PTO-892
☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). ______
☐ Interview Summary, PTO-413
☐ Notice of Draftperson's Patent Drawing Review, PTO-948
☐ Notice of Informal Patent Application, PTO-152

08/577,751

--SEE OFFICE ACTION ON THE FOLLOWING PAGES--

Serial Number: 08/577,751

Art Unit: 2508

RESTRICTION REQUIREMENT

Restriction to one of the following inventions is required under 35 U.S.C. § 121:

I. Claims 23-26, drawn to a device, classified in Class 257, subclass 635.

II. Claims 1-22, drawn to a method of making a device, classified in Class 437, subclass 50.

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, instead of etching a portion of said etch stop layer, the same could have been removed by mechanical means.

Because these inventions are distinct for the reasons given above and as shown by the above different classifications, the fields of search are not co-extensive and separate examination would be required for examination purposes and the restriction requirement as indicated is proper.

Any inquiry concerning this communication should be directed to Fetsum Abraham at telephone number (703) 305-3793.

Fr
Fetsum Abraham

11/5/96

Wael Fahmy
WAEL FAHMY
PRIMARY EXAMINER
GROUP 2500

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PAT. & TRADEMARK OFC.

2508
RECEIVED
DEC 19 1996
GROUP 2500

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Serial No.: 08/577,751 Filing Date: December 22, 1995

Examiner: F. Abraham Art Unit: 2508

Attorney Docket No.: 16820.P097

#9
12/20/96

****

Palo Alto, California
December 3, 1996

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

RESPONSE TO RESTRICTION REQUIREMENT UNDER 35 U.S.C. § 121

Sir:

In response to the Office Action dated November 12, 1996, in the above-referenced application, Applicants provisionally elect, with traverse, Group II, Claims 1-22.

There are two criteria for proper restriction:

(1) The inventions must be independent or distinct as claimed;

(2) There must be a serious burden on the examiner if restrictions is not required (MPEP § 803).

Accordingly, restriction is proper only when the restricted inventions are independent and patentably distinct (MPEP § 803). Further, the burden is on the Examiner to provide reasons and/or examples in support of restriction (MPEP § 803).

It has been asserted that the application contains claims directed to two patentably distinct inventions: 1) Invention I, covered by Claims 23-26, drawn to a device, and 2) Invention II, covered by Claims 1-22, drawn to a method of making a device. It has been further asserted that:

SAMSUNG-1008.087

> Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, instead of etching a portion of said etch stop layer, the same could have been removed by mechanical means.

Applicants respectfully traverse the restriction requirement. The Examiner has not adequately met the burden of showing that restriction is proper in this application.

For example, though the Examiner has stated that "instead of etching a portion of said etch stop layer, the same could have been removed by mechanical means," the Examiner has failed to cite any reference or provide adequate proof supporting such assertion. Thus, the Examiner has not convincingly shown that removing a portion of the etch stop layer by mechanical means would produce a device as claimed.

Consequently, the restriction requirement is considered improper because the burden of providing plausible reasons and/or examples in support of restriction has not been met. Thus, it appears that the premise of patentable distinctness between the restricted groups has merely been restated as the conclusion for finding the same.

Reconsideration and withdrawal of the restriction requirement is respectfully requested under 37 C.F.R. § 1.143.

If the Examiner wishes to discuss any aspect of this application, the Examiner is invited to telephone Applicants' undersigned attorney at 415-833-2415.

Respectfully submitted,

[signature]

David R. Graham
Attorney for Applicant
Reg. No. 36,150

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on December 3, 1996.

[signature]
Signature

PA\571158-1

MAIL ROOM
JAN 13 1997
PAT. & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE #10

Applicants: James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Serial No.: 08/577,751 Filed: December 22, 1995

Examiner: F. Abraham Group Art Unit: ~~2508~~ 1104

Attorney Docket No.: CYP-002 (formerly 16820.P097)

Milpitas, California
January 6, 1997

RECEIVED
JAN 24 1997
GROUP 2500

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D. C. 20231

CHANGE OF CORRESPONDENCE ADDRESS

Sir:

Effective immediately, please address all further correspondence in connection with the above-identified application to:

David R. Graham, Esq.
1337 Chewpon Ave.
Milpitas, CA 95035

If there are any questions regarding this request, please contact the undersigned attorney at (408) 945-9912.

Respectfully submitted,

David R. Graham
David R. Graham
Attorney for Applicants
Reg. No. 36,150

UNITED STAT... DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/577,751	12/22/95	NULTY J	16820.P097

D1M1/0307

DAVID R. GRAHAM, ESQ.
1337 CHEWPON AVE.
MILPITAS CA 95035

EXAMINER	
GURLEY, L	
ART UNIT	PAPER NUMBER
1104	11

DATE MAILED: 03/07/97

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 12/6/96.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-26 is/are pending in the application.

Of the above, claim(s) 23-26 is/are withdrawn from consideration.

☐ Claim(s) ______ is/are allowed.

☐ Claim(s) ______ is/are rejected.

☐ Claim(s) ______ is/are objected to.

☐ Claims ______ are subject to restriction or election requirement.

Application Papers

☑ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on ______ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on ______ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) ______.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: ______.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☑ Notice of Reference Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). ______

☐ Interview Summary, PTO-413

☑ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

-- SEE OFFICE ACTION ON THE FOLLOWING PAGES --

Serial Number: 08/577,751

Art Unit: 1104

Part III DETAILED ACTION

Election/Restriction

1. Applicant's election with traverse of claims 1-22 in Paper No. 9 is acknowledged. The traversal is on the ground(s) that the Examiner has not shown any reference or adequate proof that the etch stop layer could be removed by CMP instead of by etching. This is not found persuasive because no reference or proof is necessary. CMP is a well known alternative for etching to remove a layer. Additionally, selective deposition of the etch stop layer could have been performed as well so that the etching step is no longer required to produce the claimed structure.

The requirement is still deemed proper and is therefore made FINAL.

Drawings

2. The drawings are objected to because Figures 1-3 are not designated by a legend such as "Prior Art". The legend is necessary in order to clarify what applicant's invention is. MPEP § 608.02(g). Correction is required.

3. The drawings are objected to because they do not include certain reference signs mentioned in the description. 37 CFR § 1.84(f) states, "Reference signs not mentioned in the description shall not appear in the drawing and vice versa." The following reference signs are not included in the drawings: BPTEOS blanket layer "350" (p. 9, line 21); "conducting layer

320" is not shown in Fig. 4(B) (p. 20, line 15); "insulating dielectric layer 410" is not shown in Fig. 4 (p. 20, lines 19-20); "masking layer 425" is not shown in Fig. 4(A) (p. 21, line 13); "445" is not shown in Fig. 4(E) (p. 22, line 24); "photoresist material 470" is not shown in Fig. 4(J) (p. 24, line 9). Correction is required.

Note that the drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 250 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because it contains the word "said" (lines 4 and 7). Correction is required. See MPEP § 608.01(b).

6. The disclosure is objected to because of the following informalities: There are two descriptions of Fig. 3 in the "Brief Description of the Drawings" which should be consolidated; "455" in Fig. 4(H) is not described (p. 24, lines 3-8); Fig. 4(I) is not discussed (p. 24). Appropriate correction is required.

Note that the specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

7. Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention.

In claims 1 and 12: "said semiconductor body" lacks antecedent basis (lines 3-4). "substantially" is vague (line 5).

In claims 4 and 15: "low selectivity" is vague (line 1); "said etch stop layer material" and "said first insulating layer material" lack antecedent basis (lines 2-3).

In claims 7 and 18: "said etch stop layer etch" lacks antecedent basis (line 1).

In claims 8 and 19: "said exposed portion" and "said first insulating layer" lack antecedent basis (lines 1-2).

In claims 11 and 22: "the blanket layer" lacks antecedent basis (line 1).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

9. Claims 1 and 12 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Jun (5,587,331, dated 12/24/96, filed 12/17/93).

Jun shows the method as claimed, in Figs. 1-2 and corresponding text, as encapsulating a conducting layer in an insulating layer on the semiconductor body adjacent the contact region, wherein the insulating layer includes a substantially rectangular spacer portion adjacent the contact region; depositing an etch stop layer adjacent the insulating layer and adjacent the contact region; and etching a portion of the etch stop layer adjacent the contact region wherein the etching does not significantly erode the spacer portion of the insulating layer (claims 1 and 12).

10. Claims 1, 2 and 12-13 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Tsai et al. (5,521,121, dated 5/28/96, filed 4/3/95).

Tsai shows the method as claimed in Figs. 1-2 and corresponding text. A LAM etcher model 4720 is used to etch the etch stop layer.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2-11 and 13-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun (5,587,331, dated 12/24/96, filed 12/17/93).

Jun shows the method substantially as claimed and as described in the preceding paragraph.

Jun lacks anticipation only in not teaching the particulars of the etching system such as plasma, low bombardment/high neutral flux, low selectivity for the etch stop in comparison to the insulating layer, the specific type of etching apparatus, the pressure, flow rates and power parameters, a cleaning sputter etch for cleaning the insulating layer after etching the etch stop and etching a blanket insulating layer over the contact region prior to etching the etch stop layer.

It would have been obvious to one of ordinary skill in the art to have varied the etching parameters and to have used a plasma for the anisotropic etch in Jun and to have cleaned the insulating layer with a sputter etch after etching the etch stop such as would be done by routine experimentation to obtain the desired contact.

13. Claims 3-11 and 14-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. (5,521,121, dated 5/28/96, filed 4/3/95).

Tsai shows the method substantially as claimed and as described in the preceding paragraph.

Tsai lacks anticipation only in not teaching the particulars of the etching system such as plasma, low bombardment/high neutral flux, low selectivity for the etch stop in comparison to the insulating layer, the specific type of etching apparatus, the pressure, flow rates and power parameters, a cleaning sputter etch for cleaning the insulating layer after etching the etch stop and etching a blanket insulating layer over the contact region prior to etching the etch stop layer.

It would have been obvious to one of ordinary skill in the art to have varied the etching parameters and to have used a plasma for the anisotropic etch in Tsai and to have cleaned the insulating layer with a sputter etch after etching the etch stop such as would be done by routine experimentation to obtain the desired contact.

SAMSUNG-1008.096

Field of Search

This office action has been created under the Patent and Trademark Office Semiconductor Technology Quality Assurance Pilot Program. It incorporates the examination quality standards set as a result of customer focus sessions with the semiconductor industry. The listing of the field of search to follow is one of these standards.

Field of Search	Date
U.S. Class and subclass: 437/195,190	2/28/97
Other Documentation:	
Electronic data base(s): APS (USPAT)	2/28/97

Prior Art of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Nulty (5562801), Yano et al. (5569628), Lur et al. (5364817) and Davis et al. (5164330) for contact structures with substantially vertical spacer portions and etchback of an etch stop layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is (703) 305-3474. The examiner can normally be reached on Monday-Friday from 9:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached on (703) 308-2417. The fax phone number for this Group is (703) 305-3599.

Serial Number: 08/577,751

Art Unit: 1104

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0661.

lg

March 3, 1997

CHARLES L. BOWERS, JR.
SUPERVISORY PATENT EXAMINER
GROUP 1100

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP-APART AND RBON

FORM PTO-892 (REV. 2-92)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

NOTICE OF REFERENCES CITED

SERIAL NO. 08/577,751 | GROUP ART UNIT 1104 | ATTACHMENT TO PAPER NUMBER 11

APPLICANT(S) Nulty et al.

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	5562801	10/8/96	Nulty	156	643.1	12/7/94
	B	5569628	10/29/96	Yano et al.	437	190	1/25/94
	C	5164330	11/17/92	Davis et al.	437	190	—
	D	5364817	11/15/94	Lur et al.	437	190	—
	E	5521121	5/28/96	Tsai et al.	437	190	4/3/95
	F	5587331	12/24/96	Jun	437	190	12/17/93
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

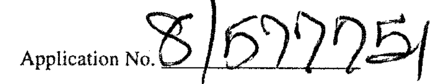
*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER Lynne A. Gurley [signature] | DATE 3/3/97

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)

Form PTO 948 (Rev. 10-94) U.S. DEPARTMENT OF COMMERCE - Patent and Trademark Office Application No. 

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

PTO Draftpersons review all originally filed drawings regardless of whether they are designated as formal or informal. Additionally, patent Examiners will review the drawings for compliance with the regulations. Direct telephone inquiries concerning this review to the Drawing Review Branch, 703-305-8404.

The drawings filed (insert date) 12/22/95, are
A. ___ not objected to by the Draftsperson under 37 CFR 1.84 or 1.152.
B. ✓ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawings must be submitted according to the instructions on the back of this Notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color.
   - ___ Not black solid lines. Fig(s)______
   - ___ Color drawings are not acceptable until petition is granted. Fig(s)______
2. PHOTOGRAPHS. 37 CFR 1.84(b)
   - ___ Photographs are not acceptable until petition is granted. Fig(s)______
   - ___ Photographs not properly mounted (must use brystol board or photographic double-weight paper). Fig(s)______
   - ___ Poor quality (half-tone). Fig(s)______
3. GRAPHIC FORMS. 37 CFR 1.84 (d)
   - ___ Chemical or mathematical formula not labeled as separate figure. Fig(s)______
   - ___ Group of waveforms not presented as a single figure, using common vertical axis with time extending along horizontal axis. Fig(s)______
   - ___ Individuals waveform not identified with a separate letter designation adjacent to the vertical axis. Fig(s)______
4. TYPE OF PAPER. 37 CFR 1.84(c)
   - ___ Paper not flexible, strong, white, smooth, nonshiny, and durable. Sheet(s)______
   - ___ Erasures, alterations, overwritings, interlineations, cracks, creases, and folds copy machine marks not accepted. Fig(s)______
   - ___ Mylar, velum paper is not acceptable (too thin). Fig(s)______
5. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
   - 21.6 cm. by 35.6 cm. (8 1/2 by 14 inches)
   - 21.6 cm. by 33.1 cm. (8 1/2 by 13 inches)
   - 21.6 cm. by 27.9 cm. (8 1/2 by 11 inches)
   - 21.0 cm. by 29.7 cm. (DIN size A4)
   - ___ All drawing sheets not the same size. Sheet(s)______
   - ___ Drawing sheet not an acceptable size. Sheet(s)______
6. MARGINS. 37 CFR 1.84(g): Acceptable margins:

Paper size

	21.6 cm. X 35.6 cm. (8 1/2 X 14 inches)	21.6 cm X 33.1 cm. (8 1/2 X 13 inches)	21.6 cm. X 27.9 cm. (8 1/2 X 11 inches)	21.0 cm. X 29.7 cm. (DIN size A4)
T	5.1 cm. (2")	2.5 cm. (1")	2.5 cm. (1")	2.5 cm.
L	.64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	2.5 cm.
R	.64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	1.5 cm.
B	.64 cm. (1/4")	.64 cm. (1/4")	.64 cm. (1/4")	1.0 cm.

✓ Margins do not conform to chart above. Sheet(s) 2-4
___ Top (T) ___ Left (L) ___ Right (R) ___ Bottom (B)

7. VIEWS. 37 CFR 1.84(h)
   REMINDER: Specification may require revision to correspond to drawing changes.
   - ___ All views not grouped together. Fig(s)______
   - ___ Views connected by projection lines or lead lines. Fig(s)______
   - Partial views. 37 CFR 1.84(h) 2
   - ✓ View and enlarged view not labled separately or properly. Fig(s) 1, 2, 4
   - Sectional views. 37 CFR 1.84 (h) 3
   - ___ Hatching not indicated for sectional portions of an object. Fig(s)______
   - ___ Cross section not drawn same as view with parts in cross section with regularly spaced parallel oblique strokes. Fig(s)______
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   - ___ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s)______
9. SCALE. 37 CFR 1.84(k)
   - ___ Scale not large enough to show mechanism with crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s)______
   - ___ Indication such as "actual size" or scale 1/2" not permitted. Fig(s)______
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)
   - ✓ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (except for color drawings). Fig(s) 1-24
11. SHADING. 37 CFR 1.84(m)
   - ___ Solid black shading areas not permitted. Fig(s)______
   - ___ Shade lines, pale, rough and blurred. Fig(s)______
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
   - ✓ Numbers and reference characters not plain and legible. 37 CFR 1.84(p)(l) Fig(s) 1-24
   - ___ Numbers and reference characters not oriented in same direction as the view. 37 CFR 1.84(p)(l) Fig(s)______
   - ___ English alphabet not used. 37 CFR 1.84(p)(2) Fig(s)______
   - ___ Numbers, letters, and reference characters do not measure at least .32 cm. (1/8 inch) in height. 37 CFR(p)(3) Fig(s)______
13. LEAD LINES. 37 CFR 1.84(q)
   - ___ Lead lines cross each other. Fig(s)______
   - ___ Lead lines missing. Fig(s)______
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
   - ___ Sheets not numbered consecutively, and in Arabic numerals, beginning with number 1. Sheet(s)______
15. NUMBER OF VIEWS. 37 CFR 1.84(u)
   - ___ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s)______
   - ___ View numbers not preceded by the abbreviation Fig. Fig(s)______
16. CORRECTIONS. 37 CFR 1.84(w)
   - ___ Corrections not made from prior PTO-948. Fig(s)______
17. DESIGN DRAWING. 37 CFR 1.152
   - ___ Surface shading shown not appropriate. Fig(s)______
   - ___ Solid black shading not used for color contrast. Fig(s)______

COMMENTS:

5/28/96

SAMSUNG-1008.100

REMINDER

Drawing changes may also require changes in the specification, e.g., if Fig. 1 is changed to Fig. 1A, Fig. 1B, Fig. 1C, etc., the specification, at the Brief Description of the Drawings, must likewise be changed. Please make such changes by 37 CFR 1.312 Amendment at the time of submitting drawing changes.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. **Correction of Informalities--37 CFR 1.85**

   File new drawings with the changes incorporated therein. The application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application, should be placed on the back of each sheet of drawings in accordance with 37 CFR 1.84(c). Applicant may delay filing of the new drawings until receipt of the Notice of Allowability (PTOL-37). Extensions of time may be obtained under the provisions of 37 CFR1.136. The drawing should be filed as a separate paper with a transmittal letter addressed to the Drawing Review Branch.

2. **Timing of Corrections**

   Applicant is required to submit **acceptable** corrected drawings within the three-month shortened statutory period set in the Notice of Allowability (PTOL-37). If a correction is determined to be unacceptable by the Office, applicant must arrange to have acceptable correction resubmitted within the original three-month period to avoid the necessity of obtaining as extension of time and paying the extension fee. Therefore, applicant should file corrected drawings as soon as possible.

   Failure to take corrective action within set (or extended) period will result in **ABANDONMENT** of the Application.

3. **Corrections other than Informalities Noted by the Drawing Review Branch on the Form PTO 948**

   All changes to the drawings, other than informalities noted by the Drawing Review Branch, **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

#Grp. 2508

Attorney Docket No.: CYP-002

OIPE
67366
AUG 11 1997
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
August 7, 1997

#12

Assistant Commissioner for Patents
Washington, D. C. 20231

Re: Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning
Serial No.: 08/577,751
Filed: December 22, 1995
Examiner: F. Abraham
Group Art Unit: 2508

RECEIVED
SEP 03 1997
GROUP 2500

Transmitted herewith are the following documents in the above-identified application:

(1) A Response to Office Action (24 pages);
(2) A Petition for Extension of Time (1 page);
(3) Corrected drawings (8 pages) - FIGS. 1(A), 1(B), 1(C), 2(A), 2(B), 3, 4(A), 4(B), 4(C), 4(D), 4(E), 4(F), 4(G), 4(H), 4(I), 4(J), 4(K) and 4(L);
(4) A check for $456.00 (Check No. 1075);
(5) An Information Disclosure Statement (2 pages);
(6) A Form PTO-1449;
(7) Copies of 6 references cited in Information Disclosure Statement;
(8) A check for $230.00 (Check No. 1076);
(9) A return receipt postcard;
(10) This sheet in duplicate.

RECEIVED
SEP 4 1997
GROUP 1100

The fee is calculated as follows (small entity status is not claimed):

CLAIMS AS AMENDED

	Claims After Amendment		Highest Number Paid For		Additional Claims		Rate		Fee
Total Claims:	29	-	26	=	3	X	$22	= $	66.00
Independent Claims:	3	-	3	=	0	X	$80	= $	0.00
___ First filing of one or more multiple dependent claims ($260 total fee)								$	0.00
_X_ Fee for Request for Extension of Time (2 months)								$	390.00
TOTAL FEE:								**$**	**456.00**

08/29/1997 SCARTER 00000010 08577751
01 FC:103 66.00 OP
02 FC:116 390.00 OP

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on August 7, 1997.

8-7-97 David R. Graham
Date David R. Graham

Respectfully submitted,

David R. Graham

David R. Graham
Reg. No. 36,150
Attorney for Applicants
1337 Chewpon Ave.
Milpitas, CA 95035

Attorney Docket No.: CYP-002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
August 7, 1997

OIPE
67366
AUG 11 1997

Assistant Commissioner for Patents
Washington, D. C. 20231

Re: Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning
Serial No.: 08/577,751
Filed: December 22, 1995
Examiner: F. Abraham
Group Art Unit: 2508

RECEIVED
SEP 03 1997
GROUP 2500

Transmitted herewith are the following documents in the above-identified application:

(1) A Response to Office Action (24 pages);
(2) A Petition for Extension of Time (1 page);
(3) Corrected drawings (8 pages) - FIGS. 1(A), 1(B), 1(C), 2(A), 2(B), 3, 4(A), 4(B), 4(C), 4(D), 4(E), 4(F), 4(G), 4(H), 4(I), 4(J), 4(K) and 4(L);
(4) A check for $456.00 (Check No. 1075);
(5) An Information Disclosure Statement (2 pages);
(6) A Form PTO-1449;
(7) Copies of 6 references cited in Information Disclosure Statement;
(8) A check for $230.00 (Check No. 1076);
(9) A return receipt postcard;
(10) This sheet in duplicate.

RECEIVED
SEP 4 1997
GROUP 1100

The fee is calculated as follows (small entity status is not claimed):

CLAIMS AS AMENDED

	Claims After Amendment		Highest Number Paid For		Additional Claims		Rate		Fee
Total Claims:	29	-	26	=	3	X	$22	= $	66.00
Independent Claims:	3	-	3	=	0	X	$80	= $	0.00
___ First filing of one or more multiple dependent claims ($260 total fee)								$	0.00
X Fee for Request for Extension of Time (2 months)								$	390.00
TOTAL FEE:								**$**	**456.00**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on August 7, 1997.

8-7-97 [signature]
Date David R. Graham

Respectfully submitted,

[signature]
David R. Graham
Reg. No. 36,150
Attorney for Applicants
1337 Chewpon Ave.
Milpitas, CA 95035

OIPE
67366
AUG 11 1997
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

Serial No.: 08/577,751 Filed: December 22, 1995

Examiner: F. Abraham Group Art Unit: 2508

Attorney Docket No.: CYP-002 (formerly 16820.P097)

Milpitas, California
August 7, 1997

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

PETITION FOR EXTENSION OF TIME

Sir:

Applicants hereby petition for a two month extension of time to respond to the Office Action mailed March 7, 1997, in the above-referenced application, such extension giving Applicants until August 7, 1997, to respond.

Respectfully submitted,

David R. Graham
David R. Graham
Registration No. 36,150
Attorney for Applicants

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on August 7, 1997.

Date: 8-7-97 David R. Graham
David R. Graham

SAMSUNG-1008.104

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#13/A mR 9/10/97

O I P E 67366 AUG 11 1997 PATENT & TRADEMARK OFFICE

Applicants: James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

Serial No.: 08/577,751 Filed: December 22, 1995

Examiner: F. Abraham Group Art Unit: 2508

Attorney Docket No.: CYP-002 (formerly 16820.P097)

Milpitas, California
August 7, 1997

RECEIVED SEP 03 1997 GROUP 2500

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

RESPONSE TO OFFICE ACTION

Sir:

Please enter the following response to the Office Action dated March 7, 1997, in the above-identified application.

RECEIVED SEP 4 1997 GROUP 1100

IN THE SPECIFICATION

At page 1, line 22, delete "the" and substitute --a--.

At page 4, line 26, delete "discreet" and substitute --discrete--.

At page 6, line 4, after "contact", insert --130--;

line 5, after "contact", insert --130--;

line 6, delete "a" (first occurrence) and substitute --the--;

after "contact", insert --130--;

A

line 7, delete "a" (second occurrence) and substitute --the--;

after "contact", insert --130--;

line 9, after "contact" (first occurrence), insert --130--;

line 11, delete "the" (first occurrence) and substitute --a--;

line 13, after "oxide", insert --(designated by FOX in FIG. (1C);

line 14, after "contact", insert --130--;

after "region", insert --140--;

line 15, after "contact", insert --130--;

line 16, after "contact", insert --130--;

line 23, after "polysilicon", insert --layer 110--.

At page 7, line 2, after "layer", insert --125--;

line 11, after "structures" (second occurrence), insert --is to--;

line 13, delete "demonstrates" and substitute --illustrates--;

line 17, after "layer" (second occurrence), insert --220--;

line 21, delete "250" and substitute --270--.

At page 8, line 1, after "opening", insert --270--;

after "was", insert --formed--;

line 2, after "Hence", insert --,--;

delete "the description of";

A

SAMSUNG-1008.106

line 3, after "240", insert --is described--;

after "layer" (third occurrence), insert --240--;

line 4, after "layer", insert --230 and spacer portion 235--;

delete "remains" and substitute --layer 220 remained--;

line 7, after "etch" (first occurrence), insert --260--;

line 9, after "layer" (first occurrence), insert --240--;

line 15, after "nitride", insert --layer--;

line 17, after "portion", insert --235--;

line 18, after "opening", insert --270--;

line 20, after "layer", insert --240--.

At page 9, line 4, delete "a" (first occurrence) and substitute --an--;

line 15, delete "presents" and substitute --illustrates--;

line 16, after "etch", insert --380--;

line 25, after "etch", insert --380--.

At page 10, line 1, after "etch", insert --380--;

line 2, after "spacer", insert --portion 370--;

after "etch", insert --380--;

line 4, after "portion", insert --370--;

after "polysilicon", insert --layer 320--;

line 5, after "polysilicon", insert --layer
320--;
delete "diffusion" and substitute
--contact--;
after "region", insert --360--;

line 10, delete "(" (first occurrence);
delete "gate" and substitute --layer
320--;

line 12, after "etch", insert --380--;

line 14, after "spacer", insert --portion 370--;

line 15, after "layer" (first occurrence), insert
--330--;

line 19, delete "layer" and substitute --spacer
portion--;

line 20, after "polysilicon", insert --layer--;

line 22, delete "opening" and substitute --region
360--;

line 23, after "etch", insert --380--;

line 24, after "region", insert --360--.

At page 11, line 1, delete "to eliminate" and substitute
--eliminating--;

line 19, delete "opening" and substitute
--region 360--.

At page 13, line 3, delete "is disclosed" and substitute
--,--.

SAMSUNG-1008.108

At page 16, line 5, delete "is a planar view of" and substitute --illustrates--;
after "to", insert --a--;
after "diffusion", insert --region--;

line 6, delete "a" (first occurrence) and substitute --the--;

line 7, delete "a" and substitute --the--;
delete "to diffusion" and substitute --taken--;

line 8, delete "a" (first occurrence) and substitute --the--;
delete "to diffusion" and substitute --taken--;

line 10, delete "of" and substitute --illustrating--;

line 11, delete "formation";

line 13, delete "of the formation";

line 15-16, delete entirety of both lines.

At page 17, lines 10-11, delete "and an insulating etch stop layer overlying the insulating material" and substitute --, wherein the diffusion regions are implanted with, for example, a silicide--;

lines 14-15, delete ", wherein the diffusion region is implanted to include a silicide".

33

At page 18, line 2, delete "etch" and substitute --etched--;

delete "region" and substitute

--regions, but separated from the

diffusion regions by the etch stop layer--;

a2

line 6, delete "a (first occurrence)";

delete "opening" and substitute

--openings--;

delete "a" (second occurrence) and

substitute --the--;

lines 6-7, delete "region and a second contact

opening through the blanket layer but

separated from the diffusion region by an

etch stop layer" and substitute

--regions--.

At page 19, line 3, delete "a" (first occurrence).

At page 20, line 11, after "regions", insert --405--;

line 15, delete "320" and substitute --415--;

line 17, delete "320 can" and substitute

--415 could--;

line 24, delete "for example";

line 25, after "oxygen", insert --,--.

At page 21, line 14, delete "exposes" and substitute

--is patterned to enable exposure of--;

a3

line 17, delete "or" and substitute --regions 405

to form--;

delete "regions" and substitute

--openings--;

34

line 21, delete "or contact";

after "regions", insert --405--.

At page 22, line 6, delete "regions" and substitute --openings--;

line 8, delete "opening" and substitute --openings--;

line 10, after "spacers", insert --435--;

line 11, delete "opening" and substitute --openings--;

line 12, after "regions", insert --405--;

line 21, after "regions", insert --405--;

line 25, after "regions", insert --405--.

At page 23, line 6, delete "340" and substitute --440--;

line 11, after "layer", insert --440--;

line 15, after "opening", insert --(measured--;

after "layer", insert --440)--;

line 16, after "spacers", insert --435--;

line 23, after "layer", insert --450--.

At page 24, line 3, after "layer", insert --455--;

line 4, after "layer", insert --450--;

delete "the contact regions overlying";

line 5, delete "are" and substitute --405 can be--;

line 6, delete "regions" and substitute --openings--;

A

line 8, delete "regions" (first occurrence) and
substitute --openings--;
after "regions" (second occurrence),
insert --405, as shown in FIG. 4(I)--;

line 9, delete "470" and substitute
--(not shown)--;

line 10, after "layer", insert --440--;

line 12, after "layer", insert --440--;

line 19, delete "region" and substitute
--opening--;

line 20, after "portion", insert --435--;

line 22, after "portion", insert --435--;
after "layer", insert --420--;

line 23, after "polysilicon", insert --layer
415--;

line 24, delete "region" and substitute
--opening--;

At page 25, line 1, delete "region" and substitute
--opening--;

line 3, after "layer", insert --420--;

line 4, delete "420";
after "portion", insert --435--;

line 5, delete "420";
after "portion", insert --435--;

line 7, delete "420";
after "portion", insert --435--;

line 8, after "portion", insert --435--;

A

line 16, delete "440".

At page 26, line 1, after "portion", insert --435--;

line 2, after "portion", insert --435--;

after "layer", insert --420--;

line 9, delete "a";

line 12, delete "region" and substitute --opening--;

line 16, delete "region" and substitute --opening--.

At page 27, line 5, after "opening", insert --(measured--;

line 6, after "layer", insert --440)--;

lines 8-9, delete ", and a height $\underline{h}_1$, and a width, $\underline{w}_1$, from which an aspect ratio may be calculated for a contact region".

IN THE DRAWINGS

Applicants request permission to amend Figures 1(A), 1(B), 1(C), 2(A), 2(B), 3, 4(A), 4(B), 4(C), 4(D), 4(E), 4(F), 4(G), 4(H), 4(I), 4(J), 4(K) and 4(L) as shown in red on the attached copies of Figures 1(A), 1(B), 1(C), 2(A), 2(B), 3, 4(A), 4(B), 4(C), 4(D), 4(E), 4(F), 4(G), 4(H), 4(I), 4(J), 4(K) and 4(L) as originally filed.

IN THE CLAIMS

Please cancel Claims 1, 4, 8, 10-12, 19, 21 and 23-26.

SAMSUNG-1008.113

Please amend the claims as follows:

In Claim 2, line 1, delete "process" and substitute
--method--;
delete "1" and substitute --27--;
after "said", insert --anisotropically--.

In Claim 3, line 1, delete "process" and substitute
--method--;
after "said", insert --anisotropically--;
line 2, delete "is" and substitute --comprises--.

In Claim 5, line 1, delete "process" and substitute
--method--;
delete "4" and substitute --27--.

In Claim 6, line 1, delete "process" and substitute
--method--.

In Claim 7, line 1, delete "process" and substitute
--method--;
delete "etch stop layer etch" and
substitute --anisotropically etching step--.

In Claim 9, line 1, delete "process" and substitute

--method--;

delete "8" and substitute --34--;

delete "sputter etch" and substitute

--cleaning step--;

delete "radio-frequency".

14 13. (Amended) The [process] method of claim [12] 35 15, wherein [said etching] the step of etching the etch stop layer utilizes a plasma etching system.

17 14. (Amended) The [process] method of claim 13 16, wherein an etching condition for [said etching] the step of etching the etch stop layer [is] comprises a low bombardment/high neutral flux condition.

18 15. (Amended) The [process] method of claim [14] 13 16, wherein [said etching condition] an etchant used in the step of etching the etch stop layer has a [low] selectivity for [said] the etch stop layer [material] relative to [said first insulating layer material] the electrically insulative spacer that is sufficiently low to retain the substantially rectangular cross-sectional shape of the spacer.

In Claim 16, line 1, delete "process" and substitute

--method--;

delete "said" and substitute --the--.

SAMSUNG-1008.115

In Claim 17, line 1, delete "process" and substitute --method--;

delete "said" and substitute --the--.

~~18~~ 20. (Amended) The [process] method of claim ~~17~~ 20, wherein [said] the step of etching the etch stop layer [etch] is performed using a recipe of 900 mtorr, 100 sccm He, 85 sccm C_2F_6 and 225 watts power.

In Claim 20, line 1, delete "process" and substitute --method--;

delete "19" and substitute --41--;

delete "said sputter etch" and substitute --the cleaning step--;

delete "radio-frequency".

In Claim 22, line 1, delete "process" and substitute --method--;

delete "21" and substitute --35--;

Please enter the following new claims:

27. (New) A method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of said devices comprising a conductive layer disposed over said substrate and a first insulating layer on said conductive layer, and at least two of said devices being interspaced by a contact region, said method comprising:

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etching a conformal second insulating layer overlying said at least two devices and said contact region under conditions providing insulating spacers in said contact region such that said insulating spacers have a substantially rectangular profile; and subsequently

anisotropically etching said structure having said insulating spacers in said contact region with an etchant having a selectivity for an etch stop material relative to said second insulating layer sufficiently low to retain the substantially rectangular profile of said insulating spacers, said etch stop material being distinct from said second insulating layer.

28. (New) The method of Claim 27, wherein said conditions include a bias sufficiently low and a pressure sufficiently high to provide said insulating spacers in said contact region having said substantially rectangular profile.

29. (New) The method of Claim 28, wherein said pressure is at least 120 sccm.

30. (New) The method of Claim 27, wherein said etching step is performed with a mixture comprising CHF_3 and CF_4.

31. (New) The method of Claim 27, wherein said anisotropically etching step is performed with an etchant comprising C_2F_6.

SAMSUNG-1008.117

32. (New) The method of Claim 27, further comprising, after said etching step and before said anisotropically etching step, depositing an etch stop layer over said structure having said ~~insulating spacers~~ in said contact region.

12
~~33~~. (New) The method of Claim ~~32~~ 11, wherein said contact region has a base, and said anisotropically etching step removes said etch stop layer from the base of said contact region.

13
~~34~~. (New) The method of Claim ~~27~~ 1, further comprising, after said anisotropically etching step, cleaning said structure having said insulating spacers in said contact region.

35. (New) A method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

forming an etch stop layer over the spacer and the first and second electrically conductive regions;

forming a blanket layer over the etch stop layer;

selectively etching the blanket layer to form an

38

opening to a first part of the etch stop layer that is formed over the first electrically conductive region;

etching the etch stop layer to remove a second part of the etch stop layer that is formed over the first electrically conductive region, wherein the step of etching the etch stop layer is performed under conditions that etch the material of the etch stop layer adjacent to the spacer and the spacer such that the substantially rectangular cross-sectional shape of the spacer is maintained.

36. (New) The method of Claim 35, wherein the step of forming an electrically insulative spacer further comprises etching a layer of electrically insulative material formed over the second electrically conductive material under conditions that form the spacer having the substantially rectangular cross-sectional shape.

37. (New) The method of Claim 36, wherein the conditions include a bias sufficiently low and a pressure sufficiently high to form the spacer having the substantially rectangular cross-sectional shape.

38. (New) The method of Claim 37, wherein the pressure is at least 120 sccm.

39. (New) The method of Claim 36, wherein the step of etching a layer of electrically insulative material is performed

with a mixture comprising CHF_3 and CF_4.

40. (New) The method of Claim 35, wherein the step of etching the etch stop layer is performed with an etchant comprising C_2F_6.

41. (New) The method of Claim 35, further comprising, after the step of etching the etch stop layer, cleaning the contact opening.

IN THE ABSTRACT

Line 5, delete "said" and substitute --a--.

Line 6, after "body", insert --,--.

Line 8, after "gate", insert --electrode--;

delete "said" and substitute --the--;

after "layer" (second occurrence), insert --,--.

Line 10, after "layer", insert --,--.

Line 13, delete "the (second occurrence)" and substitute --an--.

Line 14, after "structure" (first occurrence), insert --,--.

REMARKS

Claims 1-26 were filed. Claims 23-26 have been withdrawn from consideration as a result of the Examiner's restriction requirement, leaving Claims 1-22 pending. Claims 1-22 were rejected under 35 U.S.C. § 112. Claims 1, 2, 12 and 13 were rejected under 35 U.S.C. § 102. Claims 2-11 and 13-22 were

rejected under 35 U.S.C. § 103. Claims 2, 3, 5-7, 9, 13-18, 20 and 22 have been amended. Claims 1, 4, 8, 10-12, 19, 21 and 23-26 have been canceled. Claims 27-41 have been added. Reconsideration and allowance of Claims 2, 3, 5-7, 9, 13-18, 20 and 22, and allowance of Claims 27-41 is requested.

Objection to the Drawings

The Examiner objected to the drawings because "Figures 1-3 are not designated by a legend such as 'Prior Art'." Applicants request permission to amend Figures 1-3 (as shown in red on copies of Figures 1-3, as originally filed, that accompany this response) to include the words "Prior Art" enclosed in parentheses beneath the figure number on each of those figures.

The Examiner also objected to the drawings because "[t]he following reference signs are not included in the drawings: BPTEOS blanket layer '350' (p. 9, line 21); 'conducting layer 320' is not shown in Fig. 4(B) (p. 20, line 15); 'insulating dielectric layer 410' is not shown in Fig. 4 (p. 20, lines 19-20); 'masking layer 425' is not shown in Fig. 4(A) (p. 21, line 13); '445' is not shown in Fig. 4(E) (p. 22, line 24); 'photoresist material 470' is not shown in Fig. 4(J) (p. 24, line 9)." The Examiner also stated that "the drawings have not been checked to the extent necessary to determine the presence of all possible minor errors." Applicants request permission to amend Figures 3 and 4(A)-4(L) (as shown in red on copies of Figures 3 and 4(A)-4(L), as originally filed, that accompany this response) to add to those Figures various

reference numerals used throughout the specification. The addition of these reference numerals addresses most of the Examiner's above-quoted bases for objecting to the drawings. Additionally, the reference to conducting layer 320 at page 20, line 15 is incorrect; the specification has been amended to replace the incorrect numeral 320 with the correct numeral 415. Further, the reference to photoresist material 470 at page 24, line 9 has been amended to reflect the fact that the photoresist material is not illustrated in Figure 4(J).

Applicants have also amended portion 475 in Figure 4(K) to make the illustration of portion 475 consistent with the description in Applicants' specification at page 25, lines 6-7.

In view of the above, Applicants request withdrawal of the Examiner's objections to the drawings.

Objection to the Abstract and the Disclosure

The Examiner objected to the abstract of the disclosure "because it contains the word 'said' (lines 4 and 7)." Applicants have amended the abstract to replace the two occurrences of the word "said" with either the indefinite article "a" or the definite article "the," as appropriate.

The Examiner also objected to the disclosure because of several informalities. First, the Examiner noted that there are two descriptions of Figure 3 in the brief description of the drawings. Applicants have amended the specification to delete the second description of Figure 3 in the Brief Description of the Drawings. The Examiner also noted that the numeral 455 is

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not used in the description of Figure 4(H). Applicants have amended the specification at page 24, line 3 to add the numeral 455 to describe the mask layer shown in Figure 4(H). Finally, the Examiner noted that Figure 4(I) is not discussed in the specification. Applicants have amended page 24, line 8 of the specification to make reference to Figure 4(I) which is described at that location in the specification.

The Examiner also stated that "the specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification." As can be seen, Applicants have made numerous amendments to the specification to correct spelling, idiomatic and grammatical errors, as well as to add appropriate reference numerals at various places in the specification.

In view of the foregoing, Applicants request withdrawal of the Examiner's objection to the disclosure and the abstract of the disclosure.

Rejection of Claims under 35 U.S.C. § 112

The Examiner rejected Claims 1-22 under 35 U.S.C. § 112, second paragraph, noting, in particular, certain language in Claims 1, 4, 7, 8, 11, 12, 15, 18, 19 and 22 that the Examiner deemed deficient. Applicants have canceled Claims 1, 4, 8, 11, 12, 19 and 22, thereby obviating the Examiner's rejection insofar as the rejection depended upon the perceived problems noted with respect to those claims. In Claim 7, "said etch stop layer etch"

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has been changed to "said anisotropically etching step," thereby overcoming the antecedent basis problem noted by the Examiner. In Claim 15, "low selectivity" has been changed to "selectivity ... that is sufficiently low to retain the substantially rectangular cross-sectional shape of the spacer." Applicants submit that the new language of Claim 15 is not vague. Claim 15 has also been amended to change "said etch stop layer material" to "the etch stop layer" and to change "said first insulating layer material" to "the electrically insulative spacer," thereby overcoming the antecedent basis problems noted by the Examiner. In Claim 18, "said etch stop layer etch" has been changed to "the step of etching the etch stop layer," thereby overcoming the antecedent basis problem noted by the Examiner. Claim 22 has been amended to depend from Claim 35 instead of Claim 21, thereby overcoming the antecedent basis problem noted by the Examiner. In view of the foregoing, it is requested that the rejection of Claims 1-22 under 35 U.S.C. § 112 be withdrawn.

Rejection of Claims under 35 U.S.C. §§ 102 and 103

The Examiner rejected Claims 1 and 12 under 35 U.S.C. § 102(e) as being anticipated by Jun, and Claims 2-11 and 13-22 under 35 U.S.C. § 103 as being unpatentable over Jun. Additionally, the Examiner rejected Claims 1, 2, 12 and 13 under 35 U.S.C. § 102(e) as being anticipated by Tsai et al., and Claims 3-11 and 14-22 under 35 U.S.C. § 103 as being unpatentable over Tsai et al.

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Claims 1, 4, 8, 10-12, 19 and 21 have been canceled, thereby obviating the Examiner's rejection with respect to those claims.

New Claim 27 recites a method of forming a contact opening in a structure including a step of "etching a conformal second insulating layer ... under conditions providing insulating spacers in [a] contact region such that said insulating spacers have a substantially rectangular profile." Jun teaches forming a side wall spacer 26 (column 3, lines 58-63) by depositing and selectively anisotropically etching a silicon oxide layer. However, Jun is silent as to the etching conditions used to produce the spacer 26. Thus, it cannot be assumed that such etching conditions are established so as to form a spacer having a substantially rectangular profile, as recited in Claim 27. This is particularly so since conventional etching techniques used to form spacers at or about the time that the Jun application was filed did not produce spacers having a substantially rectangular profile. (See, e.g., U.S. Patent No. 5,382,483, issued to Young on January 17, 1995, element 15 in FIG. 3E, col. 3, lines 37-39, col. 5, lines 24-36; U.S. Patent No. 5,384,281, issued to Kenney et al. on January 24, 1995, elements 13-15 in Figs. 6-7, col. 5, lines 18-23 and col. 8, lines 28-33; U.S. Patent No. 5,562,801, issued to Nulty on October 8, 1996, col. 7, lines 28-34, col. 9, lines 16-21 and 53-61, col. 12, lines 11-15, col. 13, lines 16-26, col. 15, lines 32-43; Givens et al., Table I, p. 429, bottom of righthand column, Table II, and p. 431, top of righthand column; and Shih et al., p. 2131, lefhand column, first full paragraph lines 3-9;

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copies of which have been submitted with an Information Disclosure Statement that accompanies this response.) Rather, such spacers typically had a sloping sidewall, as shown, for example, in FIGS. 2B and 3 of Applicants' drawings. There has been no motivation to provide substantially rectangular spacers as in Claim 27, rather than sloped spacers, for several reasons. First, the latter were thought desirable to produce adequate filling of the contact opening. Second, the contact opening width at the bottom of the contact opening has historically been of paramount importance; whether the spacer sidewall was sloping or vertical was not of particular concern.

Claim 27 also recites a step of "anisotropically etching said structure ... with an etchant having a selectivity for an etch stop material relative to said second insulating layer sufficiently low to retain the substantially rectangular profile of said insulating spacers, said etch stop material being distinct from said second insulating layer." As stated in Applicants' specification at page 25, lines 1-9, such an etchant yields a spacer that retains a rectangular or "boxy" profile. Jun does not teach or suggest performing an anisotropic etch using such an etchant.

Nor does Tsai et al. teach or suggest the above two steps in the method of Claim 27. Tsai et al., like Jun, are silent regarding the conditions used to produce the spacer (which is unnumbered in Tsai et al.). Thus, as in Jun, it cannot be assumed that such conditions are established so as to form a spacer having a substantially rectangular profile, as recited in

Claim 27. To the contrary, the conventional understanding in the art was to form spacers having a sloped profile, as discussed above.

Claim 35 recites "forming an electrically insulative spacer adjacent to [a] second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to [a] substrate surface." As discussed above with respect to Claim 27, neither Jun nor Tsai et al. teach or suggest such a spacer. Nor do Tsai et al. teach or suggest the remaining steps in Claim 35, i.e., "forming an etch stop layer," "forming a blanket layer over the etch stop layer," "selectively etching the blanket layer to form an opening," and "etching the etch stop layer to remove a second part of the etch stop layer that is formed over the first electrically conductive region ... under conditions ... such that the substantially rectangular cross-sectional shape of the spacer is maintained." As discussed further above, the understanding in the art has been that sloped spacers are desirable.

Claims 2, 3, 5-7, 9 and 28-34 are each dependent claims having Claim 27 as base claim and so are allowable over Jun or Tsai et al. for at least the reasons given above with respect to Claim 27. Similarly, Claims 13-18, 20, 22 and 27-41 are each dependent claims having Claim 35 as base claim and so are allowable over Jun or Tsai et al. for at least the reasons given above with respect to Claim 35.

In view of the foregoing, it is requested that the rejections of Claims 1-22 under 35 U.S.C. §§ 102 and 103 be

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withdrawn, and that Claims 2, 3, 5-7, 9, 13-18, 20, 22 and 27-41 be allowed.

CONCLUSION

Claims 1-22 were pending. Claims 1-22 were rejected. Claims 1, 4, 8, 10-12, 19, 21 and 23-26 have been canceled. Claims 2, 3, 5-7, 9, 13-18, 20 and 22 have been amended. Claims 27-41 have been added. In view of the foregoing amendments and remarks, it is requested that Claims 2, 3, 5-7, 9, 13-18, 20, 22 and 27-41 be allowed. If the Examiner wishes to discuss any aspect of this application, the Examiner is invited to telephone Applicants' undersigned attorney at (408) 945-9912.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on August 7, 1997.

8-7-97 David R. Graham
Date Signature

Respectfully submitted,

David R. Graham
David R. Graham
Reg. No. 36,150
Attorney for Applicants

SAMSUNG-1008.128

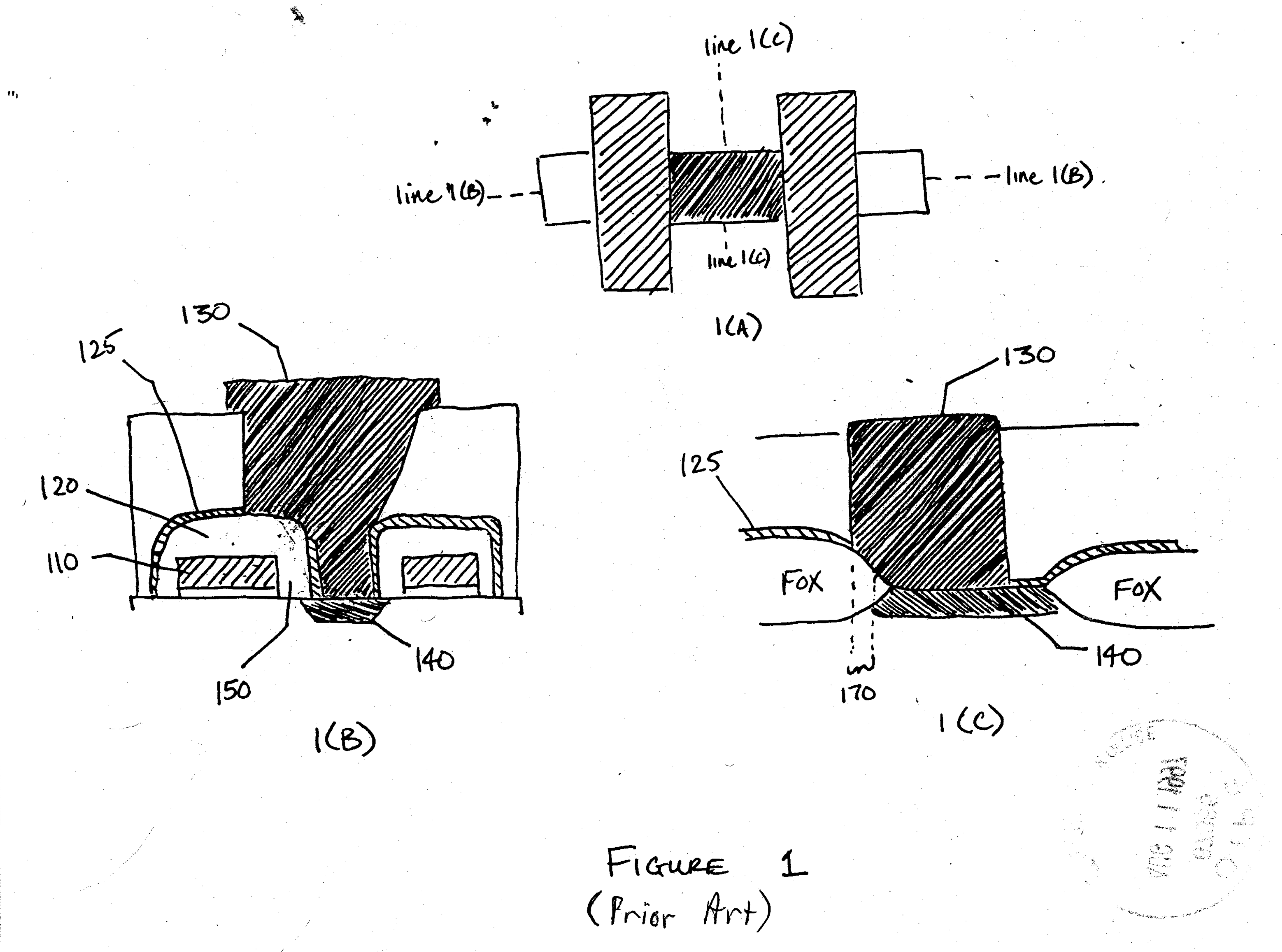


FIGURE 1
(Prior Art)

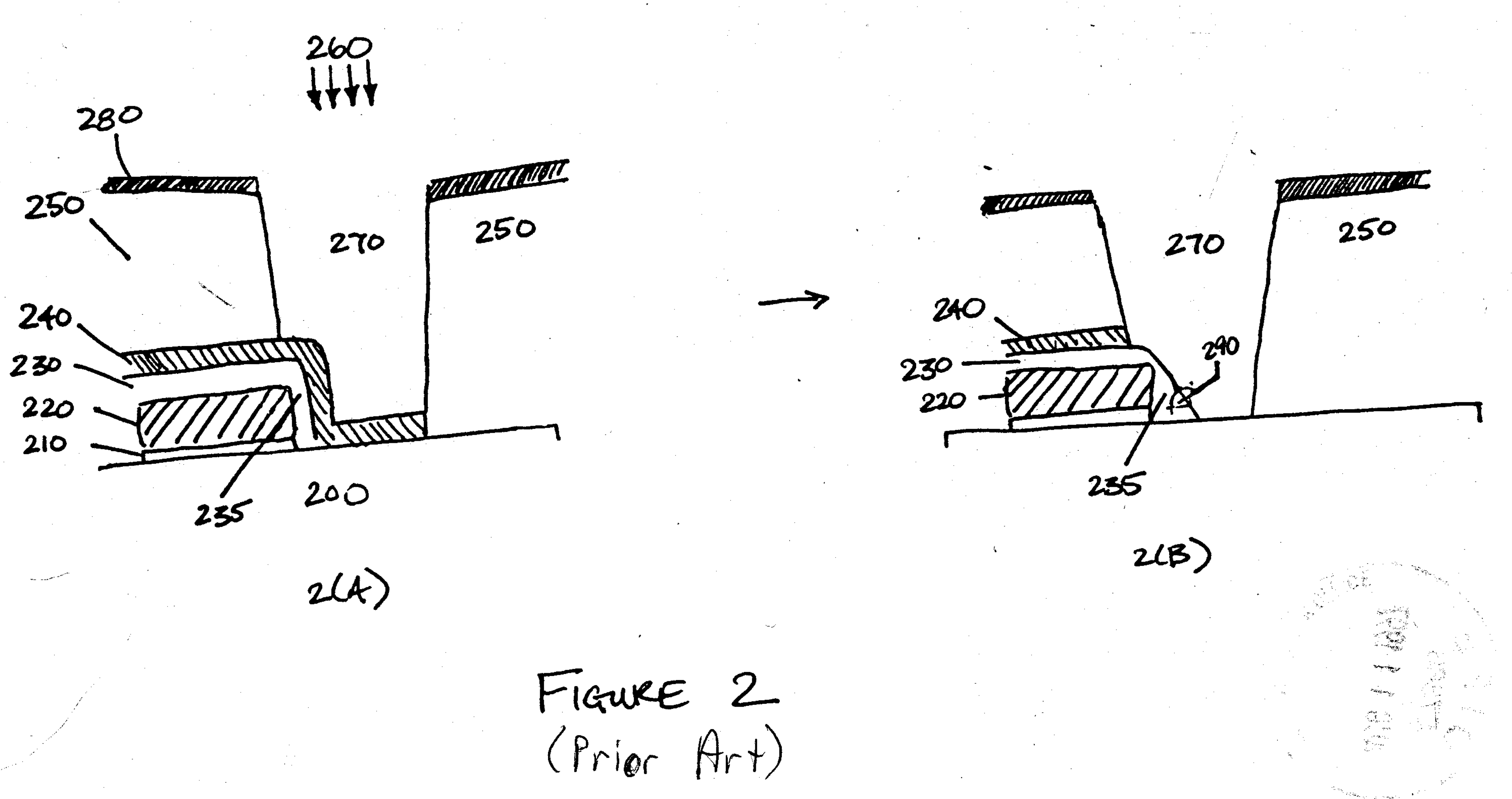


FIGURE 2
(Prior Art)

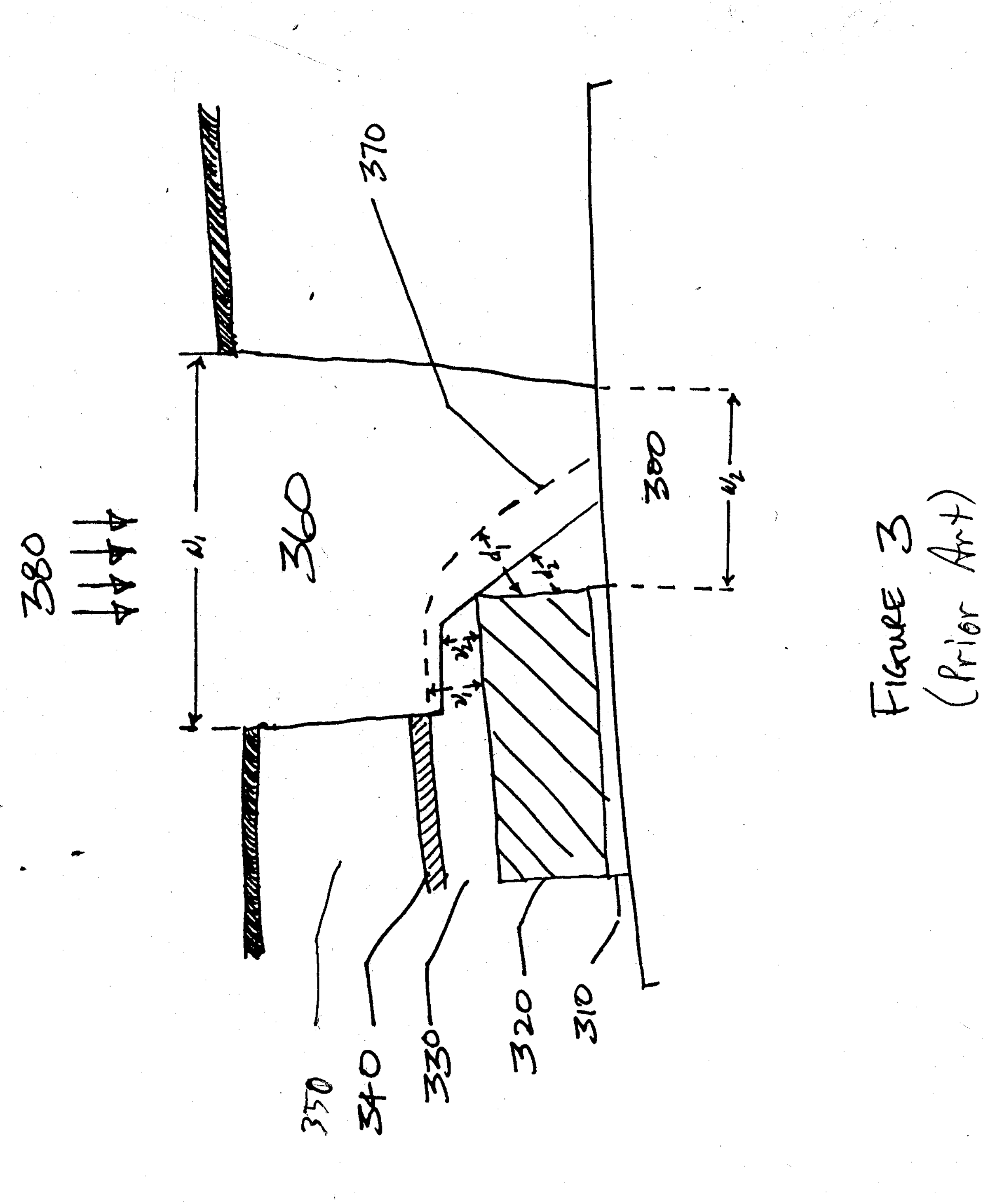
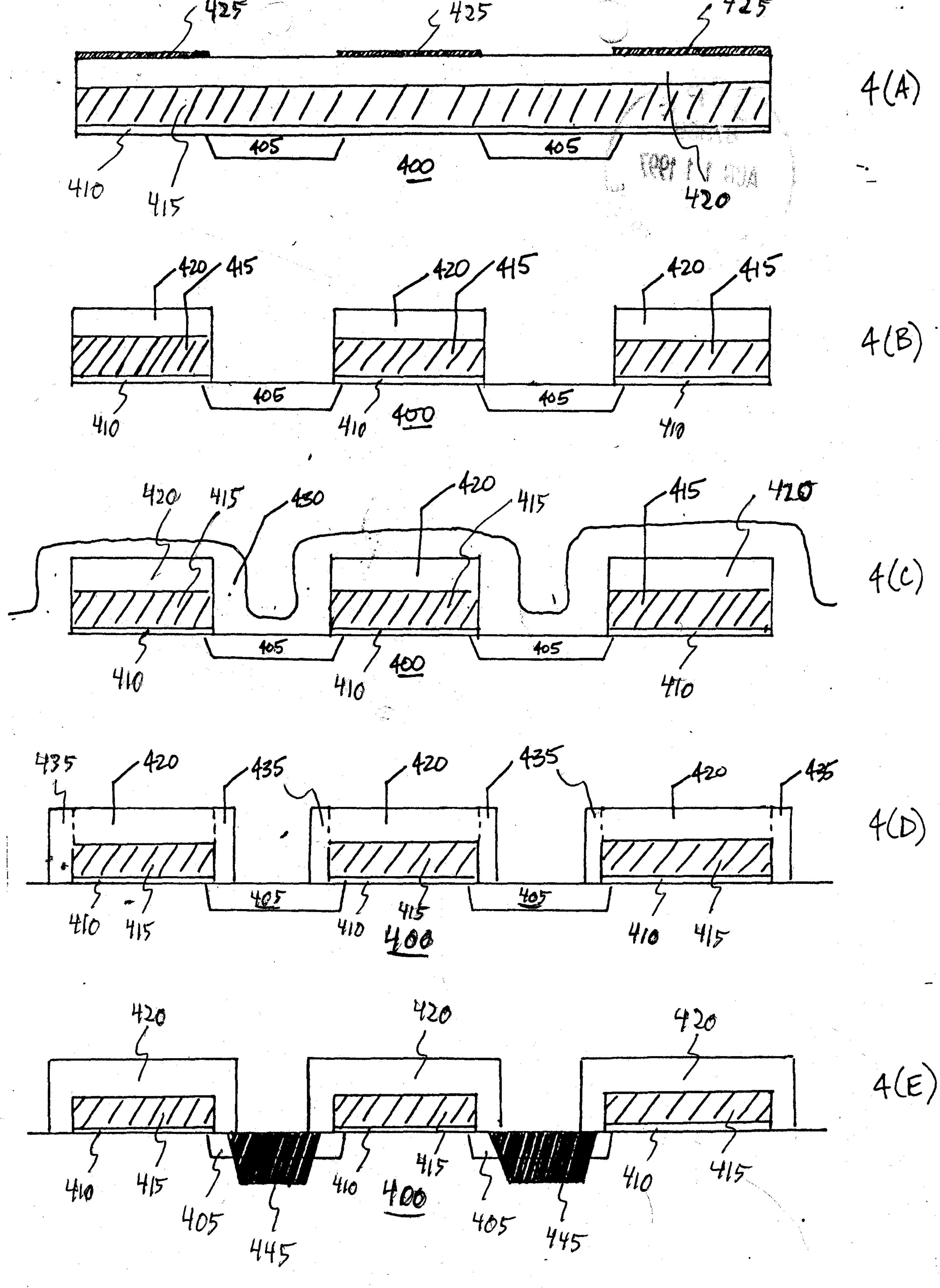


FIGURE 3
(Prior Art)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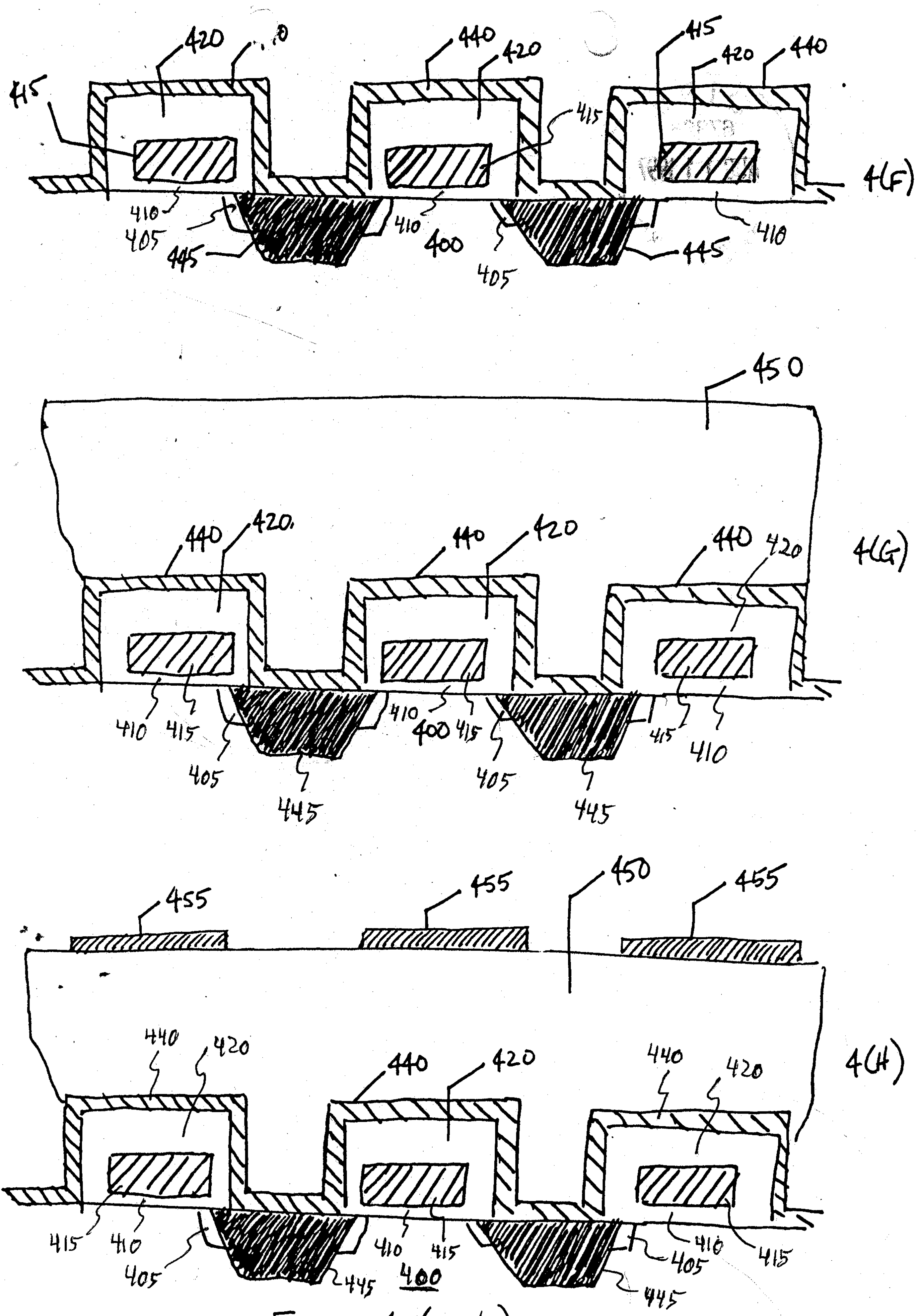


FIGURE 4 (cont.)

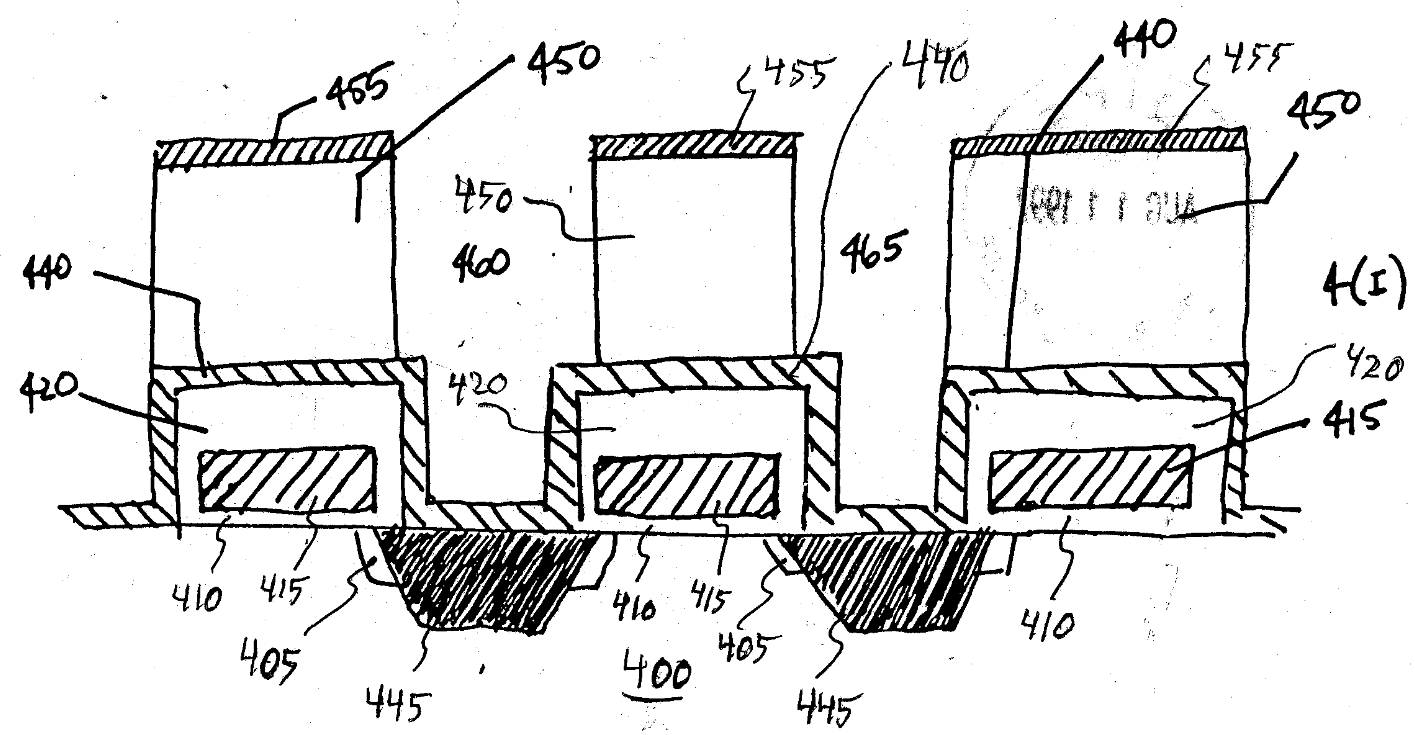
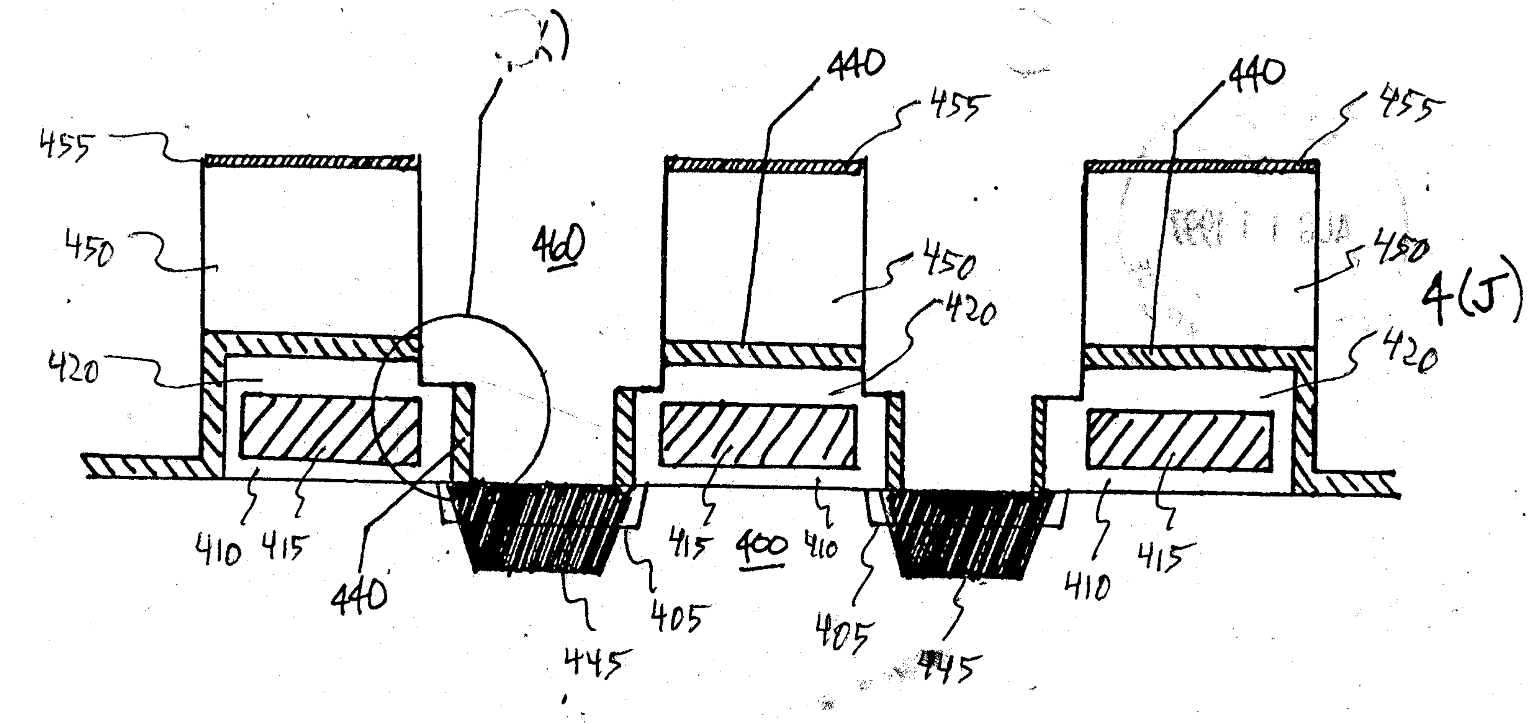


FIGURE 4 (cont.)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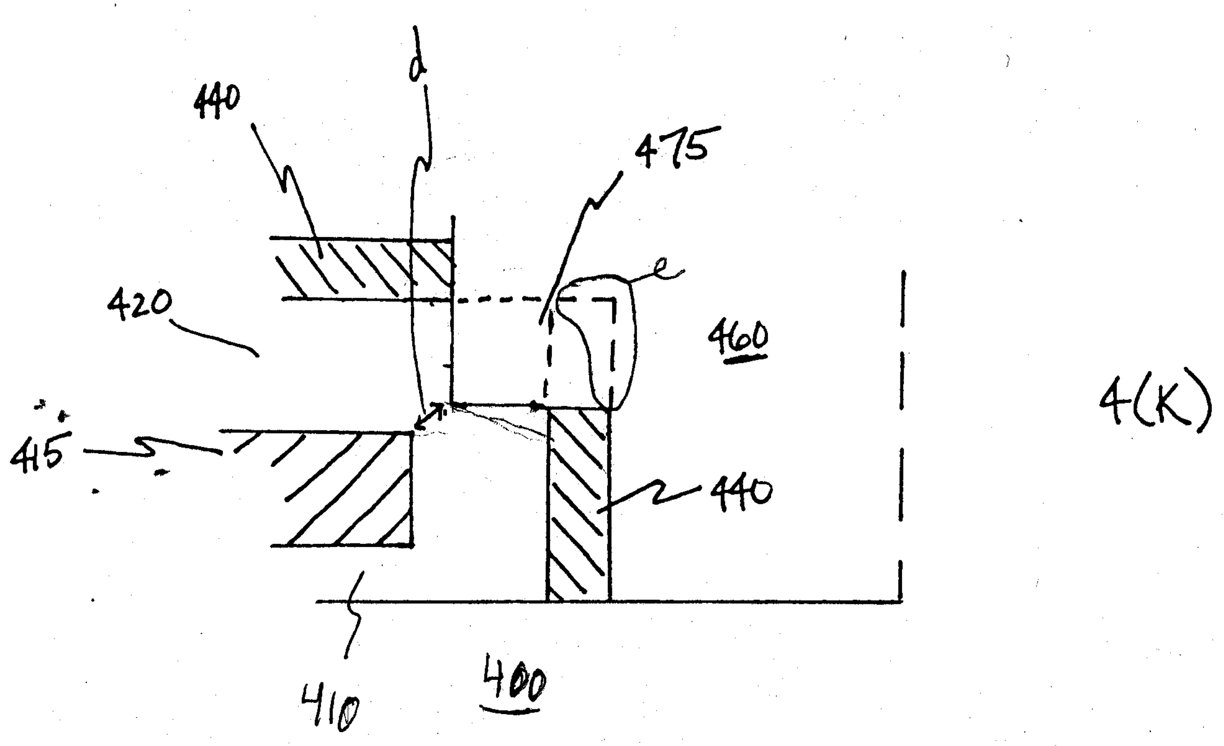
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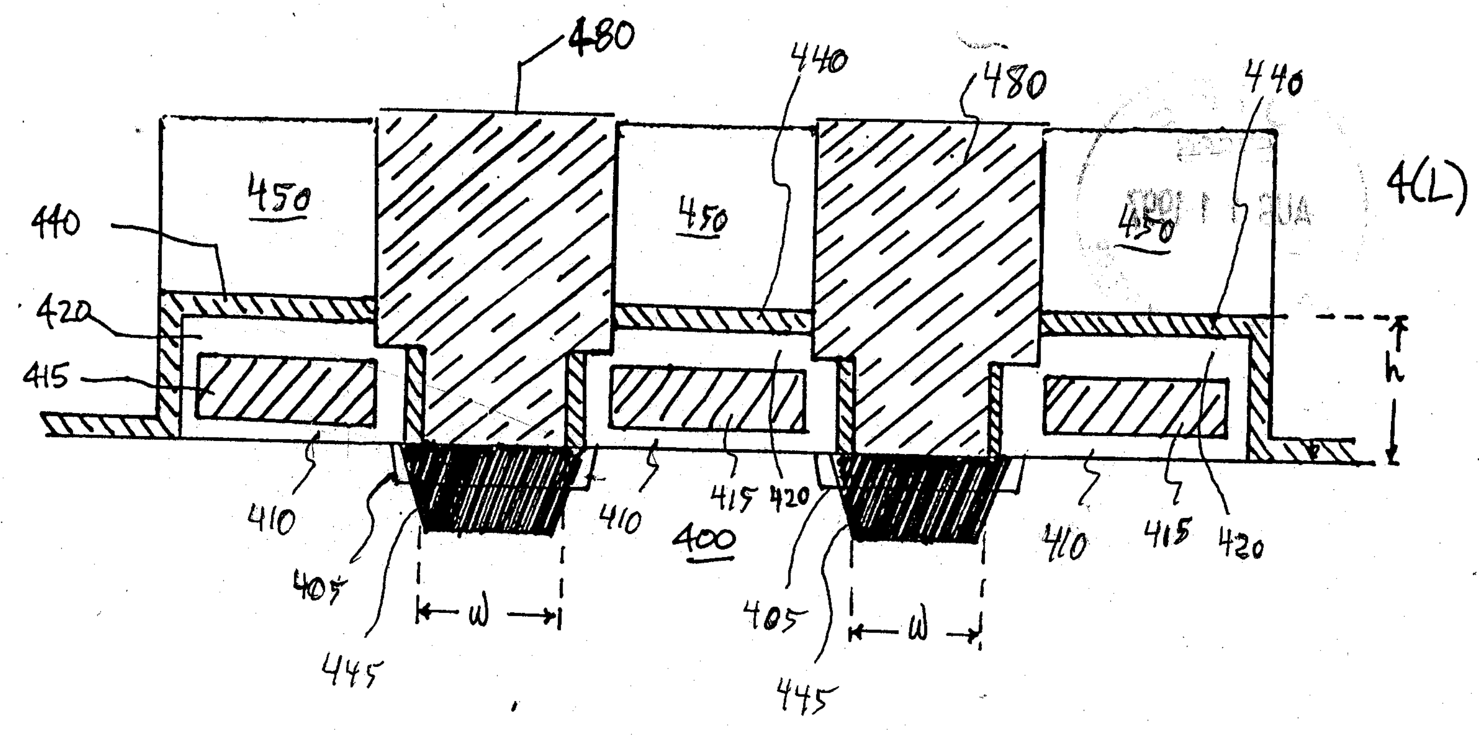
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#14

OIPE 67356 AUG 11 1997 PATENT & TRADEMARK OFFICE

Applicant(s): James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

Serial No.: 08/577,751 Filed: December 22, 1995

Examiner: F. Abraham Group Art Unit: 2508

Attorney Docket No.: CYP-002 (formerly 16820.P097)

Milpitas, California
August 7, 1997

Assistant Commissioner for Patents
Washington, D. C. 20231

INFORMATION DISCLOSURE STATEMENT
WITH FEE UNDER 37 C.F.R. § 1.17(p)

Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, Applicants bring the documents (copies enclosed) listed on the enclosed Form PTO-1449 to the Examiner's attention in the above-identified application. Citation of these documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Also, citation of these documents shall not be construed as an admission that the information disclosed therein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

08/29/1997 SCARMICH 00000010 08577751
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Enclosed is a check (Check No.1076) for $230.00 for the fee under 37 C.F.R. § 1.17(p). This paper is being submitted in duplicate.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents Washington, D.C. 20231, on August 7, 1997.

8-7-97 David R. Graham
Date David R. Graham

Respectfully submitted,

David R. Graham
David R. Graham
Reg. No. 36,150
Attorney for Applicant(s)

U.S. DEPT OF COMMERCE - PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)	ATTORNEY DOCKET NO.: [illegible]002	SERIAL NO.: 08/577,751
	APPLICANT(S): James E. Nulty et al.	
	FILING DATE: December 22, 1995	GROUP ART UNIT: 2508

OIPE
AUG 1 1 1997
PATENT & TRADEMARK OFFICE

U.S. PATENTS

EXAMINER'S INITIALS	PATENT NUMBER	ISSUE DATE	INVENTOR(S)	CLASS	SUB-CLASS	FILING DATE
Y.H.	5,306,952	4/26/94	Matsuura et al.	257	165	10/13/92
Y.H.	5,366,929	11/22/94	Cleeves et al.	437	195	5/28/93
Y.H.	5,382,483	1/17/95	Young	430	5	1/13/92
Y.H.	5,384,281	1/24/95	Kenney et al.	437	189	12/29/92

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	PUBLICATION DATE	NAME(S)	COUNTRY	TRANSLATION?	
					YES	NO

COMMONLY OWNED, CO-PENDING U.S. PATENT APPLICATIONS

EXAMINER'S INITIALS	SERIAL NUMBER	ATTORNEY DOCKET NO.	APPLICANT(S)	CLASS	SUB-CLASS	FILING DATE

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR(S), TITLE, DATE, PERTINENT PAGES, ETC.
Y.H.	J. Givens et al., "Selective dry etching in a high density plasma for 0.5 μm complementary metal-oxide-semiconductor technology," J. Vac. Sci. Technol. B 12(1), Jan/Feb 1994, pp. 427-432.
Y.H.	K.K. Shih et al., "Hafnium dioxide etch-stop layer for phase-shifting masks," J. Vac. Sci. Technol. B 11(6), Nov/Dec 1993, pp. 2130-2131.

EXAMINER: Lynne A. Gurley	DATE CONSIDERED: 11/20/97

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

Form PTO-1449

GAU2508

OIPE 64477 SEP 11 1997 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James E. Nulty, et al.

Assignee: Cypress Semiconductor Corp.

Serial No.:	08/577,751	Group Art Unit:	2508
Filed:	December 22, 1995	Examiner:	F. Abraham

Title: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

REQUEST FOR WITHDRAWAL AS ATTORNEY

RECEIVED SEP 22 1997 GROUP 2500

RECEIVED SEP 25 1997 GROUP 110

Hon. Commissioner of Patents and Trademarks
Washington, DC 20231

Sir:

The following attorney(s) or agent(s) apply to withdraw in the above-identified application:

Barry N. Young (Reg. No. 27,774); Timothy W. Lohse (Reg. No. 35,255); Marnie Wright Barnhorst (Reg. No. 36,740); and any other members of the law firm of Gray Cary Ware & Freidenrich.

Please change the correspondence address and direct all future correspondence to:

David R. Graham, Esq.
1337 Chewpon Avenue
Milpitas, CA 95035
(408) 263-7278

Respectfully submitted,

Dated: Sept 10, 1997

Barry N. Young
Reg. No. 27,774

GRAY CARY WARE & FREIDENRICH
400 Hamilton Avenue
Palo Alto, CA 94301
Telephone: (650) 833-2245

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UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
08/577,751	12/22/95	NULTY J	16820.P097

D1M1/1202

DAVID R. GRAHAM, ESQ.
1337 CHEWPON AVE.
MILPITAS CA 95035

EXAMINER	
GURLEY, L	
ART UNIT	PAPER NUMBER
1104	15

DATE MAILED: 12/02/97

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 8/11/97.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 2-3, 5-7, 9, 13-18, 20 and 27-41 is/are pending in the application.
Of the above, claim(s) ______ is/are withdrawn from consideration.
☐ Claim(s) ______ is/are allowed.
☒ Claim(s) 2-3, 5-7, 9, 13-18, 20 and 27-41 is/are rejected.
☐ Claim(s) ______ is/are objected to.
☐ Claim(s) ______ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
☐ The drawing(s) filed on ______ is/are objected to by the Examiner.
☐ The proposed drawing correction, filed on ______ is ☐ approved ☐ disapproved.
☐ The specification is objected to by the Examiner.
☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☐ received.
☐ received in Application No. (Series Code/Serial Number) ______.
☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: ______.

☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of Reference Cited, PTO-892
☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 14
☐ Interview Summary, PTO-413
☐ Notice of Draftperson's Patent Drawing Review, PTO-948
☐ Notice of Informal Patent Application, PTO-152

--SEE OFFICE ACTION ON THE FOLLOWING PAGES--

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

2. Claims 27 and 35 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Jun (5,587,331, dated 12/24/96, filed 12/17/93) or Son et al. (5,264,391, dated 11/23/93).

Jun and Son show the method as claimed, in Figs. 1-2 and corresponding text and in Figs. 1-6 and corresponding text, respectively, as a method of forming a contact opening in a structure comprising substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising: etching a conformal second insulating layer overlying the at least two devices and the contact region under conditions providing insulating spacers in the contact region such that the insulating spacers have a substantially rectangular profile; and subsequently anisotropically etching the structure having the insulating spacers in the contact region with an etchant having a selectivity for an etch stop material relative to the second insulating layer sufficiently low to retain the

substantially rectangular profile of the insulating spacers, the etch stop material being distinct from the second insulating layer (claims 27 and 35).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-3, 5-7, 9, 13-18, 20, 28-34 and 36-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun (5,587,331, dated 12/24/96, filed 12/17/93) or Son et al. (5,264,391, dated 11/23/93).

Jun and Son show the method substantially as claimed and as described in the preceding paragraph.

Jun and Son lacks anticipation only in not teaching the particulars of the etching system such as plasma, low bombardment/high neutral flux, low selectivity for the etch stop in comparison to the insulating layer, the specific type of etching apparatus, the pressure, flow rates and power parameters, a cleaning sputter etch for cleaning the insulating layer after etching the etch stop and etching a blanket insulating layer over the contact region prior to etching the etch stop layer.

It would have been obvious to one of ordinary skill in the art to have varied the etching parameters and to have used a plasma for the anisotropic etch in Jun and to have cleaned the insulating layer with a sputter etch after etching the etch stop such as would be done by routine experimentation to obtain the desired contact.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Field of Search

This office action has been created under the Patent and Trademark Office Semiconductor Technology Quality Assurance Pilot Program. It incorporates the examination quality standards set as a result of customer focus sessions with the semiconductor industry. The listing of the field of search to follow is one of these standards.

Field of Search	Date
U.S. Class and subclass: 437/195,190; 438/595,634,639	2/28/97; 11/21/97
Other Documentation:	
Electronic data base(s): APS (USPAT)	2/28/97

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO Form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is (703) 305-3474. The examiner can normally be reached on Monday-Friday from 9:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached on (703) 308-2417. The fax phone number for this Group is (703) 305-3599.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0661.

Lynne A. Gurley
lg

November 21, 1997

Charles L. Bowers
CHARLES L. BOWERS, JR.
SUPERVISORY PATENT EXAMINER
GROUP 1100

Notice of References Cited

Application No.	Applicant(s)
08/577,751	Nulty et al.

Examiner	Group Art Unit	Page
L. Gurley	1104	Page 1 of 1

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
	A	5,264,391	11/23/93	Son et al.	438	595
	B	5,100,838	3/31/92	Dennison	438	639
	C	Re. 35,111	12/5/95	Liou et al.	438	595
	D	4,806,201	2/21/89	Mitchell et al.	438	595
	E	4,660,276	4/28/87	Hsu	438	595
	F	5,166,096	11/24/92	Cote et al.	438	595
	G	5,378,646	1/3/95	Huang et al.	438	595
	H	5,482,894	1/9/96	Havemann	438	639
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

*		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	U		
	V		
	W		
	X		

* A copy of this reference is not being funished with this Office action.
(See Manual of Patent Examining Procedure, Section 707.05(a).)

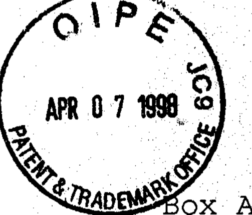
U.S. Patent and Trademark Office
PTO-892 (Rev. 9-96)

Part of Paper No. 15

*U.S. GPO: 1997-422-601/60010

AF/GAU 1104 $

Attorney Docket No.: CYP-002



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

April 2, 1998

Box AF
Assistant Commissioner for Patents
Washington, D. C. 20231

Re: Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning
Serial No.: 08/577,751
Filed: December 22, 1995
Examiner: L. Gurley
Group Art Unit: 1104

RECEIVED
APR 14 1998
GROUP 2200

Transmitted herewith are the following documents in the above-identified application:

(1) A Response Under 37 C.F.R. 1.116 (13 pages);
(2) A Petition for Extension of Time (1 page);
(3) Copies of 4 references cited in Response Under 37 C.F.R. 1.116;
(4) A check for $110.00 (Check No. 1188);
(5) A return receipt postcard;
(6) This sheet in duplicate.

The fee is calculated as follows (small entity status is not claimed):

CLAIMS AS AMENDED

	Claims After Amendment		Highest Number Paid For		Additional Claims		Rate		Fee
Total Claims:	29	-	29	=	0	X	$22	=	$ 0.00
Independent Claims:	3	-	3	=	0	X	$82	=	$ 0.00
___ First filing of one or more multiple dependent claims ($260 total fee)									$ 0.00
X Fee for Petition for Extension of Time (1 month)									$ 110.00
TOTAL FEE:									**$ 110.00**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on April 2, 1998.

4-2-98 — Date
David R. Graham (signature) — David R. Graham

Respectfully submitted,

David R. Graham (signature)

David R. Graham
Reg. No. 36,150
Attorney for Applicants
1337 Chewpon Ave.
Milpitas, CA 95035

Attorney Docket No.: CYP-002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

April 2, 1998

Box AF
Assistant Commissioner for Patents
Washington, D. C. 20231

Re: Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning
Serial No.: 08/577,751
Filed: December 22, 1995
Examiner: L. Gurley
Group Art Unit: 1104

RECEIVED
APR 14 1998
GROUP 2200

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(5) A return receipt postcard;
(6) This sheet in duplicate.

The fee is calculated as follows (small entity status is not claimed):

CLAIMS AS AMENDED

	Claims After Amendment		Highest Number Paid For		Additional Claims		Rate		Fee
Total Claims:	29	-	29	=	0	X	$22	=	$ 0.00
Independent Claims:	3	-	3	=	0	X	$82	=	$ 0.00
___ First filing of one or more multiple dependent claims ($260 total fee)									$ 0.00
_X_ Fee for Petition for Extension of Time (1 month)									$ 110.00
TOTAL FEE:									**$ 110.00**

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4-2-98 — Date
David R. Graham (signature) — David R. Graham

Respectfully submitted,

David R. Graham (signature)

David R. Graham
Reg. No. 36,150
Attorney for Applicants
1337 Chewpon Ave.
Milpitas, CA 95035

OIPE
APR 0 7 1998
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#16 / 4/14/98

Applicants: James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

Serial No.: 08/577,751 Filed: December 22, 1995

Examiner: L. Gurley Group Art Unit: 1104

Attorney Docket No.: CYP-002

Milpitas, California
April 2, 1998

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APR 14 1998
GROUP 2200

Box AF
Assistant Commissioner for Patents
Washington, D. C. 20231

PETITION FOR EXTENSION OF TIME

Sir:

Applicants hereby petition for a one month extension of time to respond to the Office Action mailed December 2, 1997, in the above-referenced application, such extension giving Applicants until April 2, 1998, to respond.

04/08/1998 PALLEN 00000134 08577751
01 FC:115 110.00 OP

Respectfully submitted,

David R. Graham
David R. Graham
Registration No. 36,150
Attorney for Applicants

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on April 2, 1998.

Date: 4-2-98 David R. Graham
David R. Graham

SAMSUNG-1008.149

CYP-002/PM95012

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 1104

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TRADEMARK OFFICE

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17/Rev.
4/14/98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751 Group Art Unit: 1104

Filed: December 22, 1995 Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

RECEIVED
14
GROUP 2200

Assistant Commissioner for Patents
Washington, D.C. 20231

RESPONSE UNDER 37 C.F.R. 1.116

Responsive to the Official Action dated December 2, 1997, in the above-identified application, reconsideration is respectfully requested in view of the following remarks.

REMARKS

Claims 2, 3, 5-7, 9, 13-18, 20, 22 and 27-41 are pending in the present application. **Careful review and consideration of the following remarks is earnestly solicited.**

The present invention concerns, in one embodiment, a method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: BOX AF, Assistant Commissioner for Patents, Washington, D.C., 20231, on 4-2 , 1998.

David R. Graham 4-2-98
Signature Date

etching a conformal second insulating layer overlaying the devices and the contact region under conditions providing insulating spacers having a substantially rectangular profile in the contact region; and subsequently

anisotropically etching the structure having the substantially rectangular insulating spacers in the contact region with an etchant having a selectivity for an etch stop material relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop material being distinct form the second insulating layer (Claim 27 and claims depending therefrom).

In a second embodiment, the present invention concerns a method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

forming an etch stop layer over the spacer and the first and second electrically conductive regions;

forming a blanket layer over the etch stop layer;

selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region;

etching the etch stop layer to remove part of the etch stop layer formed over the first electrically conductive region, under conditions that etch (i) the material of the etch stop layer adjacent to

the spacer and (ii) the spacer such that the substantially rectangular cross-sectional shape of the spacer is maintained (Claim 35 and claims depending therefrom).

The present claims are fully patentable over the cited references.

THE REJECTIONS UNDER 35 U.S.C. 102(e)

The rejection of Claims 27 and 35 under 35 U.S.C. 102(e) as being anticipated by Jun or Son et al. is respectfully traversed.

CLAIM 27 IS NOT ANTICIPATED BY JUN

Claim 27 recites a method of forming a contact opening in a structure including a step of "etching a conformal second insulating layer ... under conditions providing insulating spacers having a substantially rectangular profile." Jun teaches forming a side wall spacer 26 (column 3, lines 58-63) by depositing and selectively anisotropically etching a silicon oxide layer. However, Jun is silent as to the etching conditions used to produce the spacer 26. Thus, it cannot be assumed that such etching conditions are established so as to form a spacer having a substantially rectangular profile, as recited in Claim 27.

Nor can it be presumed that the etching conditions used by Jun (whatever they might have been) would have inherently produced a spacer having a substantially rectangular profile. This is particularly so since conventional etching techniques used to form spacers at or about the time that the Jun application was filed did not produce spacers having a substantially rectangular profile. (See, e.g., U.S. Patent No. 5,382,483, issued to Young on January 17, 1995, element 15 in FIG. 3E, col. 3, lines 37-39, col. 5, lines 24-36; U.S. Patent No. 5,384,281, issued to Kenney et al. on January 24, 1995, elements 13-15 in Figs. 6-7, col. 5, lines 18-23 and col. 8, lines 28-33; U.S. Patent No. 5,562,801, issued to Nulty on

October 8, 1996, col. 7, lines 28-34, col. 9, lines 16-21 and 53-61, col. 12, lines 11-15, col. 13, lines 16-26, col. 15, lines 32-43; Givens et al., Table I, p. 429 bottom of right-hand column, Table II, and p. 431, top of right-hand column; and Shih et al., p. 2131, left-hand column, first full paragraph lines 3-9; copies of which were submitted with an Information Disclosure Statement that accompanied the response filed August 11, 1997.) Rather, such spacers typically had a sloping sidewall, as shown, for example, in FIGS. 2B and 3 of Applicants' drawings. Thus, this ground of rejection is deficient for two reasons: (1) the rejection presumes, rather than shows, that the reference discloses a spacer having a substantially rectangular spacer; and (2) no motivation has been shown in the prior art to produce a spacer having a substantially rectangular shape under conditions that do so.

The art provides no motivation to form substantially rectangular spacers as in Claim 27, rather than sloped spacers, for several reasons. First, sloped or non-rectangular spacers were thought to be desirable to produce adequate filling of the contact opening and avoid the so-called "cusping" or "breadloafing" effect (see, e.g., Ong, U.S. Patent No. 5,371,042, showing pronounced cusping in contact holes having vertical sidewalls [Fig.1] and offering faceted sidewalls [Fig.2] as a means to avoid formation of voids in the contacts; Wang, U.S. Patent No. 5,108,570, showing pronounced cusping even in contact holes having sloped sidewalls [Fig.1]; Tracy, U.S. Patent No. 4,970,176, col. 1, ll. 48-51, stating that flared or tiered vias reduce cusping at the cost of increased area; and Robinson, "Al hits sub-0.25 micron vias," *Electrical Engineering Times*, Feb. 3, 1997, showing that even after the filing date of the present application, cusping and voids are a problem when filling small diameter, high aspect ratio via holes; copies of each reference are submitted herewith). Second, the contact opening width at the bottom of the contact openings historically been of paramount important; whether the spacer sidewall was sloping or vertical was typically of less concern.

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Consequently, any presumption that the etching conditions used by Jun (whatever they might have been) either (i) actually produced or (ii) would have inherently produced a spacer having a substantially rectangular profile is not accurate. Furthermore, the art does not appear to provide motivation to produce a substantially rectangular sidewall spacer, which would be expected to lead to increased cusping and void formation in subsequently formed contacts, both of which in turn are expected to lead to increased defect and/or failure rates.

Claim 27 also recites a step of "anisotropically etching said structure ... with an etchant having a selectivity for an etch stop material relative to said second insulating layer sufficiently low to retain the substantially rectangular profile of said insulating spacers". As stated in Applicants' specification at page 25, lines 1-9, such an etchant yields a spacer that retains its rectangular or "boxy" profile. Jun does not reach or suggest performing an anisotropic etch using such an etchant.

For example, as shown in Fig. 4(J) and 4(K), anisotropic etch of the structure having insulating spacers in the contact region with an etchant having a selectivity for an etch stop material relative to the second insulating layer (which, in one embodiment, can be the insulating spacer; see, for example, Figs. 4(B) and 4(C), and the corresponding text in the specification from page 21, line 15, through page 22, line 20) sufficiently low to retain the substantially rectangular profile of the insulating spacers may etch the insulating spacer material at about the same rate as it etches the etch stop material. Thus, in one embodiment, a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacers may be as low as one (essentially no selectivity).

By contrast, the etch steps or processes of Jun appear to show complete selectivity (see col. 4, lines 11-14, 21-25, 27-32 and 59-66, and Figs. 2 (F)-(H) and Fig. 2 (K)). Consequently it appears that the etch steps or processes disclosed by Jun actually teach away from the present invention.

As a result, Jun does not anticipate the present Claim 27.

Even further, the rejection is based on mere conclusory assertion(s) and completely lacks factual support. No particular disclosures or teachings in any reference, including the reference presently applied against claim 27, have been cited in support of the conclusory assertions. Consequently, a *prima facie* case of anticipation has not been established.

The conclusory style of examination practiced in the present application becomes readily apparent when reviewing this ground of rejection. The rejection consists of mere assertions that Jun shows the method as claimed. The entire reference is relied upon, without indicating whether any particular part of the disclosure is relevant to the claim or any particular element in the claim, much less that such particular portions of the disclosure are relevant to particular elements of the claim.

Furthermore, as explained above, Jun fails to disclose any of the following features of claim 27:

- Etching a conformal insulating layer under conditions providing insulating spacers having a substantially rectangular profile; and/or
- Subsequently anisotropically etching the structure with an etchant having a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacer.

It is quite clear from a cursory review of the record that a *prima facie* ground of rejection has not been established. Consequently, claim 27 is fully patentable over Jun. Therefore, this ground of rejection should be withdrawn, and claim 27 should be allowed.

CLAIM 35 IS NOT ANTICIPATED BY JUN

Claim 35 recites "forming an electrically insulative spacer adjacent to [a] second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape..." As discussed above with respect to Claim 27, Jun neither teaches or suggests such a spacer. Furthermore, Jun neither teaches or suggests other features in Claim 35; e.g., "etching the etch stop layer ... under conditions ...

such that the substantially rectangular cross-sectional shape of the spacer is maintained." As discussed above, the art does not appear to suggest the desirability of, or provide the motivation to make, substantially rectangular spacers as recited in the present claims.

Consequently, Jun does not anticipate the present Claim 35.

Furthermore, the rejection is based on mere conclusory assertion(s) and completely lacks factual support. No particular disclosures or teachings in any reference, including the reference presently applied against claim 35, have been cited in support of the conclusory assertions. Consequently, a *prima facie* case of anticipation has not been established.

The conclusory style of examination practiced in the present application becomes readily apparent when reviewing this ground of rejection. The rejection consists of mere assertions that Jun shows the method as claimed. The entire reference is relied upon, without indicating whether any particular part of the disclosure is relevant to the claim or any particular element in the claim, much less that such particular portions of the disclosure are relevant to particular elements of the claim.

As explained above, Jun fails to disclose any of the following features of claim 35:

- Forming an electrically insulative spacer having a substantially rectangular cross-sectional shape in a plane substantially perpendicular to the substrate surface; and/or
- Etching an etch stop layer with an etchant having a selectivity sufficiently low to maintain the substantially rectangular cross-sectional shape of the insulating spacer.

It is quite clear from a cursory review of the record that a *prima facie* ground of rejection has not been established. Consequently, claim 35 is fully patentable over Jun. Therefore, this ground of rejection should be withdrawn, and claim 35 should be allowed.

CLAIM 27 IS NOT ANTICIPATED BY SON ET AL.

Son et al. disclose a method of forming a contact region in which a second conductive layer is deposited onto an insulating layer overlying a gate, and a portion of the second conductive layer is etched to form an etch protective layer over a portion of the insulating layer (see Fig. 1 and col. 2, lines 4-10). A portion of the etch protective layer, the insulating layer and the first conducting (gate) layer are then etched to form gate electrodes (see Fig. 2, col. 2, lines 10-19). Sidewall spacers are then formed from a second insulating layer deposited over the gate electrodes (see Fig. 4, col. 2, lines 21-31).

Even if one assumes for the sake of argument that the spacers of Son et al. are "substantially rectangular" (which, in view of the above remarks regarding the patentability of claim 27 over Jun, is not inherently the case), Son et al. do not perform an anisotropic etch step after forming the insulating sidewall spacers (see from col. 2, line 32 through col. 4, line 49). As a result, Son et al. do not perform the second step of Claim 27. Consequently, Son et al. do not anticipate Claim 27.

Even further, the rejection is based on mere conclusory assertion(s) and completely lacks factual support. No particular disclosures or teachings in any reference, including the references presently applied against claim 27, have been cited in support of the conclusory assertions. Consequently, a *prima facie* case of anticipation has not been established.

The conclusory style of examination practiced in the present application becomes readily apparent when reviewing this ground of rejection. The rejection consists of mere assertions that Son et al. shows the method as claimed. The entire reference is relied upon, without indicating whether any particular part of the disclosure is relevant to the claim or any particular element in the claim, much less that such particular portions of the disclosure are relevant to particular elements of the claim.

Furthermore, as explained above, Son et al. fails to disclose any of the following features of claim 27:

SAMSUNG-1008.157

- Etching a conformal insulating layer under conditions providing insulating spacers having a substantially rectangular profile; and/or
- Subsequently anisotropically etching the structure, much less doing so with an etchant having a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacer.

It is quite clear from a cursory review of the record that a *prima facie* ground of rejection has not been established. Consequently, claim 27 is fully patentable over Son et al. Therefore, this ground of rejection should be withdrawn, and claim 27 should be allowed.

CLAIM 35 IS NOT ANTICIPATED BY SON ET AL.

As discussed above, Son et al. form the etch stop layer before forming the insulating spacer. As a result, Son et al. cannot (i) form an etch stop layer over the spacer or (ii) remove a second part of the etch stop layer under conditions that maintain the substantially rectangular cross-sectional shape of the spacer.

Therefore, Son et al. cannot anticipate the present Claim 35.

Furthermore, the rejection is based on mere conclusory assertion(s) and completely lacks factual support. No particular disclosures or teachings in any reference, including the references presently applied against claim 35, have been cited in support of the conclusory assertions. Consequently, a *prima facie* case of anticipation has not been established.

The conclusory style of examination practiced in the present application becomes readily apparent when reviewing this ground of rejection. The rejection consists of mere assertions that Son et al. shows the method as claimed. The entire reference is relied upon, without indicating whether any

particular part of the disclosure is relevant to the claim or any particular element in the claim, much less that such particular portions of the disclosure are relevant to particular elements of the claim.

As explained above, Son et al. fails to disclose any of the following features of claim 35:

- Forming an electrically insulative spacer having a substantially rectangular cross-sectional shape in a plane substantially perpendicular to the substrate surface; and/or
- Etching an etch stop layer with an etchant having a selectivity sufficiently low to maintain the substantially rectangular cross-sectional shape of the insulating spacer.

It is quite clear from a cursory review of the record that a *prima facie* ground of rejection has not been established. Consequently, claim 35 is fully patentable over Jun. Therefore, this ground of rejection should be withdrawn, and claim 35 should be allowed.

THE REJECTIONS UNDER 35 U.S.C. 103(a)

The rejection of Claims 2, 3, 5-7, 9, 13-18, 20, 22, 27-34 and 36-41 under 35 U.S.C. 103(a) as being unpatentable over Jun or Son et al. is respectfully traversed.

CLAIMS 2, 3, 5-7, 9, 13-18, 20, 22, 27-34 AND 36-41 ARE PATENTABLE OVER JUN

As explained above, Jun neither suggests nor provides the motivation to form substantially rectangular insulating spacers or perform subsequent etching steps under conditions that maintain such substantially rectangular insulating spacers. As a result, the claims that depend from Claims 27 and 35, which necessarily contain one or more limitations above and beyond those recited in Claims 27 and 35, cannot be suggested or rendered obvious by Jun. On this basis alone, Claims 2,3, 5-7, 9, 13-18, 20, 22, 27-34 and 36-41 are patentable over Jun.

However, as the application notes, substantially rectangular insulating spacers provide advantages over conventional spacers in that subsequent sputter etch cleaning of contact holes containing such substantially rectangular insulating spacers may be conducted without sufficiently eroding the spacers. (See, for example, from page 25, line 16, through page 26, line 24, of the specification). As a result, high quality contacts may be formed in such contact holes provided by the present invention.

Jun is silent with regard to sputter etch cleaning of contact holes. Consequently, Jun cannot appreciate the advantages of, or the results provided by, the presently claimed method.

Even further, the rejection is based on mere conclusory assertion(s) and completely lacks factual support. No particular disclosures or teachings in any reference, including the references presently applied against the claims, have been cited in support of such conclusory assertions. Consequently, a *prima facie* case of obviousness has not been established.

The conclusory style of examination practiced in the present application becomes readily apparent when reviewing this ground of rejection. The rejection consists of mere assertions that routine experimentation would have been done to arrive at the desired contact. (Interestingly, and further evidencing the conclusory nature of examination in the present case, neither the contact *per se* nor any step that directly results in formation of a contact is an element of any of the present claims.)

For example, the last two paragraphs on page 3 of the Office Action states that the references "show the method substantially as claimed" and that the cited art "lacks anticipation only in not teaching the particulars of the etching system such as plasma..., low selectivity..., a cleaning sputter etch for cleaning the [structure] after etching..." The first paragraph on page 4 of the Office action then asserts that "(i)t would have been obvious to one of ordinary skill in the art to have vary the etching parameters and to have used a plasma... and to have cleaned the insulating layer with a sputter etch after etching the etch stop... to obtain desired contact." However, no factual basis for this assertion, such a column and

line numbers of a reference, are provided in support. If modification of such parameters and inclusion of such additional steps would have been routine and obvious, surely art exists that shows or suggests such modification. However, no such art has been cited in support of the conclusory assertions on which the present rejections are based. Consequently, a *prima facie* case of obviousness has been established.

Furthermore, as shown above, Son et al. fail to disclose any of the following features of the claims:

- Etching a conformal insulating layer under conditions providing insulating spacers having a substantially rectangular profile;
- Subsequently anisotropically etching the structure with an etchant having a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacer;
- Forming an electrically insulative spacer having a substantially rectangular cross-sectional shape in a plane substantially perpendicular to the substrate surface;
- Etching an etch stop layer with an etchant having a selectivity sufficiently low to maintain the substantially rectangular cross-sectional shape of the insulating spacer;

much less the features recited in the dependent claims.

If is quite clear from a cursory review of the record that *prima facie* grounds of rejections have not been established. Consequently, the rejections should be withdrawn, and the application should be allowed.

CLAIMS 2, 3, 5-7, 9, 13-18, 20, 22, 27-34 AND 36-41 ARE PATENTABLE OVER SON ET AL.

For the sake of brevity, all of the above arguments are incorporated herein in support of the patentability of the claims over Son et al. However, in addition to these arguments, Son et al. neither

perform nor suggest anisotropic etching after the insulating spacer formed. In addition, similar to Jun, Son et al. teach that etching selectivity for their third insulating layer and the underlying protective layers are considerably different from each other (see, e.g., col. 4, lines 14-22). By contrast, in the claimed method, the selectivity for etch stop material relative to an insulating layer is sufficiently low to retain the substantially rectangular profile of the insulating spacer. In the example shown in the figures, this selectivity is as low as one (essentially no selectivity). Therefore it appear that Son et al. also lead one away from the claimed method rather than towards it. **This is the antithesis of obviousness.**

Consequently, Claims 2, 3, 5-7, 9, 13-18, 20, 22, 27-34 and 36-41 are patentable over Son et al.

CONCLUSION

In view of the above remarks, the present claims are fully patentable over the cited references. Consequently, these grounds of rejections should be withdrawn.

The present application is in condition for allowance. Early notice to that effect is earnest solicited.

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08/577,751	12/22/95	NULTY	J	16820.P097

MM21/0527

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1337 CHEWPON AVE.
MILPITAS CA 95035

EXAMINER	
GURLEY,L	
ART UNIT	**PAPER NUMBER**
2814	18

DATE MAILED: 05/27/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)
*U.S. GPO: 1998-437-638/80022

1- File Copy

Advisory Action	Application No. 08/577,751	Applicant(s) Nulty et al.
	Examiner Lynne Gurley	Group Art Unit 2814

THE PERIOD FOR RESPONSE: [check only a) or b)]

a) [X] expires 4 months from the mailing date of the final rejection.

b) [ ] expires either three months from the mailing date of the final rejection, or on the mailing date of this Advisory Action, whichever is later. In no event, however, will the statutory period for the response expire later than six months from the date of the final rejection.

Any extension of time must be obtained by filing a petition under 37 CFR 1.136(a), the proposed response and the appropriate fee. The date on which the response, the petition, and the fee have been filed is the date of the response and also the date for the purposes of determining the period of extension and the corresponding amount of the fee. Any extension fee pursuant to 37 CFR 1.17 will be calculated from the date of the originally set shortened statutory period for response or as set forth in b) above.

[ ] Appellant's Brief is due two months from the date of the Notice of Appeal filed on ______ (or within any period for response set forth above, whichever is later). See 37 CFR 1.191(d) and 37 CFR 1.192(a).

Applicant's response to the final rejection, filed on *Apr 7, 1998* **has been considered with the following effect, but is NOT deemed to place the application in condition for allowance:**

[X] The proposed amendment(s):

[X] will be entered upon filing of a Notice of Appeal and an Appeal Brief.

[ ] will not be entered because:

[ ] they raise new issues that would require further consideration and/or search. (See note below).

[ ] they raise the issue of new matter. (See note below).

[ ] they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal.

[ ] they present additional claims without cancelling a corresponding number of finally rejected claims.

NOTE: ______

[ ] Applicant's response has overcome the following rejection(s): ______

[ ] Newly proposed or amended claims ______ would be allowable if submitted in a separate, timely filed amendment cancelling the non-allowable claims.

[X] The affidavit, exhibit or request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See Attachment A.

[ ] The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

[X] For purposes of Appeal, the status of the claims is as follows (see attached written explanation, if any):

Claims allowed: ______

Claims objected to: ______

Claims rejected: *2, 3, 5-7, 9, 13-18, 20, and 27-41*

[ ] The proposed drawing correction filed on ______ [ ] has [ ] has not been approved by the Examiner.

[ ] Note the attached Information Disclosure Statement(s), PTO-1449, Paper No(s). ______ .

[ ] Other

Attachment A -- To Advisory Action, Paper No. 14
(Response To After Final Response Filed Under 37 C.F.R. 1.116)

In response to Applicant's Remarks in Paper No. 17, pages 3-5, in as much as the word "substantially" can be interpreted, the spacers "26" in Jun, are "substantially" rectangular, as Applicant has claimed. Applicant does not claim "substantially rectangular" sidewall spacers to mean "perfectly rectangular" sidewall spacers and has not defined the word "substantially", substantially enough to preclude the shape of the spacers in Jun. Instead, Applicant has defined the width of the spacers, rather than their shape (specification, page 22). Therefore, Applicant does not appear to provide a concrete definition for the word "substantially"which would preclude the Examiner from using the broadest meaning of the term "substantially" when considering the prior art of record.

In response to Applicant's Remarks in Paper No. 17, page 5, lines 7-10, a "rectangular" or "boxy" profile is not claimed. A "substantially" rectangular shape is claimed, and is shown to be retained during subsequent processing steps, including an anisotropic etch (Jun, Figures 2(G)-2(H), column 4, lines 21-25). Also, the phrase "sufficiently low", regarding the etch selectivity, in the condition "sufficiently low to retain the substantially rectangular profile" is shown in Jun since Applicant has not defined the meaning of "sufficiently low" to preclude the process in Jun where the etch stop "29" is anisotropically etched by a method which retains the substantially rectangular profile "26".

In response to Applicant's Remarks in Paper No. 17, page 6, last paragraph to page 8, Jun shows, in Figures 2(A)-2(H), a "substantially rectangular spacer" for the same reasons given in the previous paragraphs. No assertion has been made, in as much as "substantially rectangular" can be interpreted.

In response to Applicant's Remarks in Paper No. 17, page 8, Son shows a "substantially rectangular spacer" "6a" for the reasons pertaining to Jun above. An anisotropic plasma etch in Figure 6, using a mask ("the blanket layer"; column 4, lines 1-14) is used to etch the etch stop layer "7". No conclusory assertion has been made here. Again, regarding the condition "sufficiently low to retain the substantially rectangular profile", Son shows retention of the "substantially rectangular" sidewall spacer "6a"for the reasons of record.

In conclusion, the prior art of record shows the claimed invention as previously rejected, and for the reasons of record. Specifically, Son shows the first and second electrically conductive regions "3" in Figure 2; the first insulating layer on top "4"; the contact region in between (Figure 2); the second conformal insulating layer "6" which is formed into insulating spacers "6a"; an etch stop material "7" and an anisotropic etch using a mask ("blanket layer"; column 4, lines 1-14) where the spacers "6a" retain their "substantially rectangular" shape and the first and second electrically conductive regions are exposed (Figure 6, "10"). Jun shows the first and second electrically conductive regions "23' " in Figure 2; the first insulating layer on top "14"; the contact region in between "15"; the second conformal insulating layer (column 1, lines 34-41) which is formed into insulating spacers "16"; an etch stop material "29" and an anisotropic etch using a blanket layer "210" where the spacers "16" retain their "substantially rectangular" shape and the first and second electrically conductive regions are exposed (Figure 2(H)).

Olik Chaudhuri
Supervisory Patent Examiner
Technology Sector 2800

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

NO-19

In re Application of
NULTY, et al.
Serial No.: 08/577,751
Filing Date: December 22, 1995
For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

REQUEST FOR WITHDRAWAL AS ATTORNEY

This decision is in response to the "REQUEST FOR WITHDRAWAL AS ATTORNEY", filed September 11, 1997, in the above-captioned patented file. No petition fee is required.

The petition is **DISMISSED** as **MOOT**.

A review of the patent file record reveals that there is no indication that any of the attorneys identified in the present Notice were attorneys of record. Accordingly, it is appropriate to dismiss the present request as moot. The original Notice will remain in the application file and no further action will be taken.

A change of correspondence address was received on January 13, 1997, in which the correspondence address had been changed to:

David R. Graham, Esq.
1337 Chewpon Avenue
Milpitas, CA 95035

MAILED
JUN 30 1998
OFFICE OF THE DIRECTOR
GR[illegible] 2500

The application is being returned to Central Files for Technology Center 2800 awaiting response to the final Office action mailed December 2, 1997.

Brian W. Brown
Special Program Examiner
Technology Center 2800
Physics, Optics, Systems Components,
and Electrical Engineering
(703) 308-6452

Barry N. Young
Gray Cary Ware & Freidenrich
400 Hamilton Avenue
Palo Alto, CA 94301

David R. Graham, Esq.
1337 Chewpon Avenue
Milpitas, CA 95035

BWB/CKO:cko

05/04/98 GC585 U.S. PTO

119
116

11F/GP2814 $

Attorney Docket No.: CYP-002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

April 29, 1998

Box AF
Assistant Commissioner for Patents
Washington, D. C. 20231

Re: Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning
Serial No.: 08/577,751
Filed: December 22, 1995
Examiner: L. Gurley
Group Art Unit: 2814

Transmitted herewith are the following documents in the above-identified application:

(1) Notice of Appeal (1 page);
(2) Petition for Extension of Time - 2 months (1 page);
(3) Check for $710.00 (Check No. 1206);
(4) Return receipt postcard; and
(5) This sheet in duplicate.

The fee is calculated as follows (small entity status is not claimed):

_x_	Fee for Notice of Appeal	$ 310.00
_x_	Fee for Petition for Extension of Time (2 months)	$ 400.00
TOTAL FEE:		**$ 710.00**

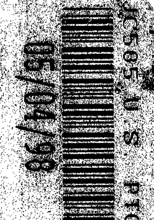
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on April 29, 1998.

4-29-98 David R. Graham
Date Signature

Respectfully submitted,

David R. Graham

David R. Graham
Reg. No. 36,150
Attorney for Applicants
1337 Chewpon Ave.
Milpitas, CA 95035



Attorney Docket No.: CYP-002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

April 29, 1998

Box AF
Assistant Commissioner for Patents
Washington, D. C. 20231

Re: Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning
Serial No.: 08/577,751
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Examiner: L. Gurley
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x	Fee for Notice of Appeal	$ 310.00
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TOTAL FEE:		**$ 710.00**

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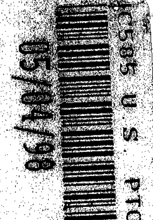
4-29-98 David R. Graham
Date Signature

Respectfully submitted,

David R. Graham

David R. Graham
Reg. No. 36,150
Attorney for Applicants
1337 Chewpon Ave.
Milpitas, CA 95035



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

Serial No.: 08/577,751 Filed: December 22, 1995

Examiner: L. Gurley Group Art Unit: 2814

Attorney Docket No.: CYP-002

Milpitas, California
April 29, 1998

Box AF
Assistant Commissioner for Patents
Washington, D. C. 20231

PETITION FOR EXTENSION OF TIME

Sir:

Applicants hereby petition for a two month extension of time to respond to the Office Action mailed December 2, 1997, in the above-referenced application, such extension giving Applicants until May 4, 1998, to respond.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on April 29, 1998.

4-29-98 David R. Graham
Date Signature

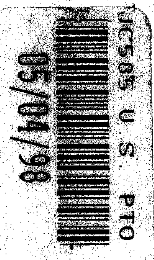
05/07/1998 ZABRAHA 00000036 08577751

02 FC:116 400.00 OP

Respectfully submitted,

David R. Graham

David R. Graham
Reg. No. 36,150
Attorney for Applicants



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

Serial No.: 08/577,751 Filed: December 22, 1995

Examiner: L. Gurley Group Art Unit: 2814

Attorney Docket No.: CYP-002

21/Notice of Appeal C. Stanley 8-27-98

Milpitas, California
April 29, 1998

Box AF
Assistant Commissioner for Patents
Washington, D. C. 20231

NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicants hereby appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner dated December 2, 1997, rejecting Claims 2, 3, 5-7, 9, 13-18, 20, 22 and 27-41.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on April 29, 1998.

4-29-98 David R. Graham
Date Signature

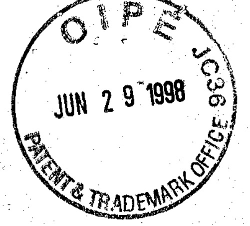
Respectfully submitted,

David R. Graham
David R. Graham
Reg. No. 36,150
Attorney for Applicants

05/07/1998 ZABRAHA 00000036 08577751
01 FC:119 310.00 OP

SAMSUNG-1008.172

GAU 2814



Attorney Docket No.: CYP-002-C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

June 29, 1998

22/Rey. for CPA G. Stanley 8-27-98

Box CPA
Assistant Commissioner for Patents
Washington, D. C. 20231

This is a request to file a _x_ continuation ___ divisional application under 37 C.F.R. § 1.53(d), i.e., a continued prosecution application (CPA), of the following prior application:

Serial No.: 08/577,751
Filing Date: December 22, 1995
Title (as originally filed): Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning
Title (as last amended): Not amended
Inventors: (as originally filed) James E. Nulty and Christopher J. Petti
Inventors (as last amended): Not amended
Assignee: Cypress Semiconductor Corporation
Examiner: L. Gurley
Group Art Unit: 2814

The anticipated classification of this application is:
Class _________
SubClass _________

RECEIVED
JUL 08 1998
GROUP 2100

_x_ Enter all unentered amendments requested pursuant to 37 C.F.R. § 1.116 in the prior application. A copy of each such amendment is enclosed.

___ A preliminary amendment is enclosed.

___ Please cancel the following claims in this application: ________________.

___ Priority of ___________ Application No. ___________, filed on ___________ in ___________ is claimed under 35 U.S.C. § 119.

___ A certified copy of that application has been submitted in the prior application.

07/06/1998 SLUANG 00000012 08577751
01 FC:131 290.00 OP
02 FC:103 198.00 OP

___ Delete the following individuals as inventors in this application as a result of a change in the claimed subject matter: ________________.

_x_ The power of attorney in the prior application is to David R. Graham, Esq., Reg. No. 36,150.

___ A Revocation of Power of Attorney and Appointment of New Attorney is included.

___ A verified statement establishing small entity status is enclosed.

It is understood that secrecy under 35 U.S.C. §122 is hereby waived to the extent that if information or access is available to any one of the applications in the file wrapper of a CPA application, be it either this application or a prior application in the same file wrapper, the Patent and Trademark Office may provide similar information or access to all the other applications in the same file wrapper.

The filing fee is calculated as follows (small entity status is not claimed), based upon the claims existing in the prior application as amended by any amendment indicated above:

CLAIMS AS FILED

	Number Filed				Number Extra		Rate			Fee
Basic Filing Fee:									$	790.00
Total Claims:	29	-	20	=	9	X	$22	=	$	198.00
Independent Claims:	3	-	3	=	0	X	$82	=	$	00.00
___ Application contains one or more multiple dependent claims ($270 total fee)									$	0.00
TOTAL FILING FEE:									**$**	**988.00**

_x_ A check for $988.00 is enclosed (Check No. 1236).

___ A Petition For Extension Of Time (with duplicate copy) in the prior application is enclosed, together with a check for $_____ (Check No._____)for the fee due.

_x_ A return receipt postcard and this sheet in duplicate are also enclosed.

Please address all future correspondence regarding this application to: David R. Graham, 1337 Chewpon Avenue, Milpitas, California 95035

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on June 29, 1998.
Express Mail Receipt No. EM124203986US

David R. Graham (signature) 6-29-98
David R. Graham Date

Respectfully submitted,

(signature)
David R. Graham
Reg. No. 36,150
Attorney for Applicants

Attorney Docket No.: CYP-002-C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

June 29, 1998

Box CPA
Assistant Commissioner for Patents
Washington, D. C. 20231

This is a request to file a _x_ continuation ___ divisional application under 37 C.F.R. § 1.53(d), i.e., a continued prosecution application (CPA), of the following prior application:

Serial No.: 08/577,751
Filing Date: December 22, 1995
Title (as originally filed): Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning
Title (as last amended): Not amended
Inventors: (as originally filed) James E. Nulty and Christopher J. Petti
Inventors (as last amended): Not amended
Assignee: Cypress Semiconductor Corporation
Examiner: L. Gurley
Group Art Unit: 2814

The anticipated classification of this application is:
Class _________
SubClass _________

_x_ Enter all unentered amendments requested pursuant to 37 C.F.R. § 1.116 in the prior application. A copy of each such amendment is enclosed.

___ A preliminary amendment is enclosed.

___ Please cancel the following claims in this application: ____________________.

___ Priority of __________ Application No. __________, filed on __________ in __________ is claimed under 35 U.S.C. § 119.
___ A certified copy of that application has been submitted in the prior application.

___ Delete the following individuals as inventors in this application as a result of a change in the claimed subject matter: ____________________.

_x_ The power of attorney in the prior application is to David R. Graham, Esq., Reg. No. 36,150.
___ A Revocation of Power of Attorney and Appointment of New Attorney is included.

___ A verified statement establishing small entity status is enclosed.

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JUL 0 8 1998
GROUP 2100

It is understood that secrecy under 35 U.S.C. §122 is hereby waived to the extent that if information or access is available to any one of the applications in the file wrapper of a CPA application, be it either this application or a prior application in the same file wrapper, the Patent and Trademark Office may provide similar information or access to all the other applications in the same file wrapper.

The filing fee is calculated as follows (small entity status is not claimed), based upon the claims existing in the prior application as amended by any amendment indicated above:

CLAIMS AS FILED

	Number Filed				Number Extra		Rate			Fee
Basic Filing Fee:									$	790.00
Total Claims:	29	-	20	=	9	X	$22	=	$	198.00
Independent Claims:	3	-	3	=	0	X	$82	=	$	00.00
___ Application contains one or more multiple dependent claims ($270 total fee)									$	0.00
TOTAL FILING FEE:									**$**	**988.00**

_x_ A check for $988.00 is enclosed (Check No. 1236).
___ A Petition For Extension Of Time (with duplicate copy) in the prior application is enclosed, together with a check for $_____ (Check No.____)for the fee due.
_x_ A return receipt postcard and this sheet in duplicate are also enclosed.

Please address all future correspondence regarding this application to: David R. Graham, 1337 Chewpon Avenue, Milpitas, California 95035

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on June 29, 1998.
Express Mail Receipt No. EM124203986US

David R. Graham [signature] 6-29-98
David R. Graham Date

Respectfully submitted,

David R. Graham [signature]
David R. Graham
Reg. No. 36,150
Attorney for Applicants

CYP-002/PM95012

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 1104

OIPE JC36
JUN 29 1998
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751 Group Art Unit: 1104

Filed: December 22, 1995 Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Assistant Commissioner for Patents
Washington, D.C. 20231

RESPONSE UNDER 37 C.F.R. 1.116

Responsive to the Official Action dated December 2, 1997, in the above-identified application, reconsideration is respectfully requested in view of the following remarks.

REMARKS

Claims 2, 3, 5-7, 9, 13-18, 20, 22 and 27-41 are pending in the present application. **Careful review and consideration of the following remarks is earnestly solicited.**

The present invention concerns, in one embodiment, a method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising:

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JUL 08 1998
GROUP 2100

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: BOX AF, Assistant Commissioner for Patents, Washington, D.C., 20231, on 4-2, 1998.

David R. Graham 4-2-98
Signature Date

etching a conformal second insulating layer overlaying the devices and the contact region under conditions providing insulating spacers having a substantially rectangular profile in the contact region; and subsequently

anisotropically etching the structure having the substantially rectangular insulating spacers in the contact region with an etchant having a selectivity for an etch stop material relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop material being distinct form the second insulating layer (Claim 27 and claims depending therefrom).

In a second embodiment, the present invention concerns a method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

forming an etch stop layer over the spacer and the first and second electrically conductive regions;

forming a blanket layer over the etch stop layer;

selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region;

etching the etch stop layer to remove part of the etch stop layer formed over the first electrically conductive region, under conditions that etch (i) the material of the etch stop layer adjacent to

the spacer and (ii) the spacer such that the substantially rectangular cross-sectional shape of the spacer is maintained (Claim 35 and claims depending therefrom).

The present claims are fully patentable over the cited references.

THE REJECTIONS UNDER 35 U.S.C. 102(e)

The rejection of Claims 27 and 35 under 35 U.S.C. 102(e) as being anticipated by Jun or Son et al. is respectfully traversed.

CLAIM 27 IS NOT ANTICIPATED BY JUN

Claim 27 recites a method of forming a contact opening in a structure including a step of "etching a conformal second insulating layer ... under conditions providing insulating spacers having a substantially rectangular profile." Jun teaches forming a side wall spacer 26 (column 3, lines 58-63) by depositing and selectively anisotropically etching a silicon oxide layer. However, Jun is silent as to the etching conditions used to produce the spacer 26. Thus, it cannot be assumed that such etching conditions are established so as to form a spacer having a substantially rectangular profile, as recited in Claim 27.

Nor can it be presumed that the etching conditions used by Jun (whatever they might have been) would have inherently produced a spacer having a substantially rectangular profile. This is particularly so since conventional etching techniques used to form spacers at or about the time that the Jun application was filed did not produce spacers having a substantially rectangular profile. (See, e.g., U.S. Patent No. 5,382,483, issued to Young on January 17, 1995, element 15 in FIG. 3E, col. 3, lines 37-39, col. 5, lines 24-36; U.S. Patent No. 5,384,281, issued to Kenney et al. on January 24, 1995, elements 13-15 in Figs. 6-7, col. 5, lines 18-23 and col. 8, lines 28-33; U.S. Patent No. 5,562,801, issued to Nulty on

October 8, 1996, col. 7, lines 28-34, col. 9, lines 16-21 and 53-61, col. 12, lines 11-15, col. 13, lines 16-26, col. 15, lines 32-43; Givens et al., Table I, p. 429 bottom of right-hand column, Table II, and p. 431, top of right-hand column; and Shih et al., p. 2131, left-hand column, first full paragraph lines 3-9; copies of which were submitted with an Information Disclosure Statement that accompanied the response filed August 11, 1997.) Rather, such spacers typically had a sloping sidewall, as shown, for example, in FIGS. 2B and 3 of Applicants' drawings. Thus, this ground of rejection is deficient for two reasons: (1) the rejection presumes, rather than shows, that the reference discloses a spacer having a substantially rectangular spacer; and (2) no motivation has been shown in the prior art to produce a spacer having a substantially rectangular shape under conditions that do so.

The art provides no motivation to form substantially rectangular spacers as in Claim 27, rather than sloped spacers, for several reasons. First, sloped or non-rectangular spacers were thought to be desirable to produce adequate filling of the contact opening and avoid the so-called "cusping" or "breadloafing" effect (see, e.g., Ong, U.S. Patent No. 5,371,042, showing pronounced cusping in contact holes having vertical sidewalls [Fig.1] and offering faceted sidewalls [Fig.2] as a means to avoid formation of voids in the contacts; Wang, U.S. Patent No. 5,108,570, showing pronounced cusping even in contact holes having sloped sidewalls [Fig.1]; Tracy, U.S. Patent No. 4,970,176, col. 1, ll. 48-51, stating that flared or tiered vias reduce cusping at the cost of increased area; and Robinson, "Al hits sub-0.25 micron vias," *Electrical Engineering Times*, Feb. 3, 1997, showing that even after the filing date of the present application, cusping and voids are a problem when filling small diameter, high aspect ratio via holes; copies of each reference are submitted herewith). Second, the contact opening width at the bottom of the contact openings historically been of paramount important; whether the spacer sidewall was sloping or vertical was typically of less concern.

Consequently, any presumption that the etching conditions used by Jun (whatever they might have been) either (i) actually produced or (ii) would have inherently produced a spacer having a substantially rectangular profile is not accurate. Furthermore, the art does not appear to provide motivation to produce a substantially rectangular sidewall spacer, which would be expected to lead to increased cusping and void formation in subsequently formed contacts, both of which in turn are expected to lead to increased defect and/or failure rates.

Claim 27 also recites a step of "anisotropically etching said structure ... with an etchant having a selectivity for an etch stop material relative to said second insulating layer sufficiently low to retain the substantially rectangular profile of said insulating spacers". As stated in Applicants' specification at page 25, lines 1-9, such an etchant yields a spacer that retains its rectangular or "boxy" profile. Jun does not reach or suggest performing an anisotropic etch using such an etchant.

For example, as shown in Fig. 4(J) and 4(K), anisotropic etch of the structure having insulating spacers in the contact region with an etchant having a selectivity for an etch stop material relative to the second insulating layer (which, in one embodiment, can be the insulating spacer; see, for example, Figs. 4(B) and 4(C), and the corresponding text in the specification from page 21, line 15, through page 22, line 20) sufficiently low to retain the substantially rectangular profile of the insulating spacers may etch the insulating spacer material at about the same rate as it etches the etch stop material. Thus, in one embodiment, a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacers may be as low as one (essentially no selectivity).

By contrast, the etch steps or processes of Jun appear to show complete selectivity (see col. 4, lines 11-14, 21-25, 27-32 and 59-66, and Figs. 2 (F)-(H) and Fig. 2 (K)). Consequently it appears that the etch steps or processes disclosed by Jun actually teach away from the present invention.

As a result, Jun does not anticipate the present Claim 27.

Even further, the rejection is based on mere conclusory assertion(s) and completely lacks factual support. No particular disclosures or teachings in any reference, including the reference presently applied against claim 27, have been cited in support of the conclusory assertions. Consequently, a *prima facie* case of anticipation has not been established.

The conclusory style of examination practiced in the present application becomes readily apparent when reviewing this ground of rejection. The rejection consists of mere assertions that Jun shows the method as claimed. The entire reference is relied upon, without indicating whether any particular part of the disclosure is relevant to the claim or any particular element in the claim, much less that such particular portions of the disclosure are relevant to particular elements of the claim.

Furthermore, as explained above, Jun fails to disclose any of the following features of claim 27:

- Etching a conformal insulating layer under conditions providing insulating spacers having a substantially rectangular profile; and/or
- Subsequently anisotropically etching the structure with an etchant having a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacer.

It is quite clear from a cursory review of the record that a *prima facie* ground of rejection has not been established. Consequently, claim 27 is fully patentable over Jun. Therefore, this ground of rejection should be withdrawn, and claim 27 should be allowed.

CLAIM 35 IS NOT ANTICIPATED BY JUN

Claim 35 recites "forming an electrically insulative spacer adjacent to [a] second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape..." As discussed above with respect to Claim 27, Jun neither teaches or suggests such a spacer. Furthermore, Jun neither teaches or suggests other features in Claim 35; e.g., "etching the etch stop layer ... under conditions ...

such that the substantially rectangular cross-sectional shape of the spacer is maintained." As discussed above, the art does not appear to suggest the desirability of, or provide the motivation to make, substantially rectangular spacers as recited in the present claims.

Consequently, Jun does not anticipate the present Claim 35.

Furthermore, the rejection is based on mere conclusory assertion(s) and completely lacks factual support. No particular disclosures or teachings in any reference, including the reference presently applied against claim 35, have been cited in support of the conclusory assertions. Consequently, a *prima facie* case of anticipation has not been established.

The conclusory style of examination practiced in the present application becomes readily apparent when reviewing this ground of rejection. The rejection consists of mere assertions that Jun shows the method as claimed. The entire reference is relied upon, without indicating whether any particular part of the disclosure is relevant to the claim or any particular element in the claim, much less that such particular portions of the disclosure are relevant to particular elements of the claim.

As explained above, Jun fails to disclose any of the following features of claim 35:

- Forming an electrically insulative spacer having a substantially rectangular cross-sectional shape in a plane substantially perpendicular to the substrate surface; and/or
- Etching an etch stop layer with an etchant having a selectivity sufficiently low to maintain the substantially rectangular cross-sectional shape of the insulating spacer.

It is quite clear from a cursory review of the record that a *prima facie* ground of rejection has not been established. Consequently, claim 35 is fully patentable over Jun. Therefore, this ground of rejection should be withdrawn, and claim 35 should be allowed.

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CLAIM 27 IS NOT ANTICIPATED BY SON ET AL.

Son et al. disclose a method of forming a contact region in which a second conductive layer is deposited onto an insulating layer overlying a gate, and a portion of the second conductive layer is etched to form an etch protective layer over a portion of the insulating layer (see Fig. 1 and col. 2, lines 4-10). A portion of the etch protective layer, the insulating layer and the first conducting (gate) layer are then etched to form gate electrodes (see Fig. 2, col. 2, lines 10-19). Sidewall spacers are then formed from a second insulating layer deposited over the gate electrodes (see Fig. 4, col. 2, lines 21-31).

Even if one assumes for the sake of argument that the spacers of Son et al. are "substantially rectangular" (which, in view of the above remarks regarding the patentability of claim 27 over Jun, is not inherently the case), Son et al. do not perform an anisotropic etch step after forming the insulating sidewall spacers (see from col. 2, line 32 through col. 4, line 49). As a result, Son et al. do not perform the second step of Claim 27. Consequently, Son et al. do not anticipate Claim 27.

Even further, the rejection is based on mere conclusory assertion(s) and completely lacks factual support. No particular disclosures or teachings in any reference, including the references presently applied against claim 27, have been cited in support of the conclusory assertions. Consequently, a *prima facie* case of anticipation has not been established.

The conclusory style of examination practiced in the present application becomes readily apparent when reviewing this ground of rejection. The rejection consists of mere assertions that Son et al. shows the method as claimed. The entire reference is relied upon, without indicating whether any particular part of the disclosure is relevant to the claim or any particular element in the claim, much less that such particular portions of the disclosure are relevant to particular elements of the claim.

Furthermore, as explained above, Son et al. fails to disclose any of the following features of claim 27:

- Etching a conformal insulating layer under conditions providing insulating spacers having a substantially rectangular profile; and/or
- Subsequently anisotropically etching the structure, much less doing so with an etchant having a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacer.

It is quite clear from a cursory review of the record that a *prima facie* ground of rejection has not been established. Consequently, claim 27 is fully patentable over Son et al. Therefore, this ground of rejection should be withdrawn, and claim 27 should be allowed.

CLAIM 35 IS NOT ANTICIPATED BY SON ET AL.

As discussed above, Son et al. form the etch stop layer before forming the insulating spacer. As a result, Son et al. cannot (i) form an etch stop layer over the spacer or (ii) remove a second part of the etch stop layer under conditions that maintain the substantially rectangular cross-sectional shape of the spacer.

Therefore, Son et al. cannot anticipate the present Claim 35.

Furthermore, the rejection is based on mere conclusory assertion(s) and completely lacks factual support. No particular disclosures or teachings in any reference, including the references presently applied against claim 35, have been cited in support of the conclusory assertions. Consequently, a *prima facie* case of anticipation has not been established.

The conclusory style of examination practiced in the present application becomes readily apparent when reviewing this ground of rejection. The rejection consists of mere assertions that Son et al. shows the method as claimed. The entire reference is relied upon, without indicating whether any

particular part of the disclosure is relevant to the claim or any particular element in the claim, much less that such particular portions of the disclosure are relevant to particular elements of the claim.

As explained above, Son et al. fails to disclose any of the following features of claim 35:

- Forming an electrically insulative spacer having a substantially rectangular cross-sectional shape in a plane substantially perpendicular to the substrate surface; and/or
- Etching an etch stop layer with an etchant having a selectivity sufficiently low to maintain the substantially rectangular cross-sectional shape of the insulating spacer.

It is quite clear from a cursory review of the record that a *prima facie* ground of rejection has not been established. Consequently, claim 35 is fully patentable over Jun. Therefore, this ground of rejection should be withdrawn, and claim 35 should be allowed.

THE REJECTIONS UNDER 35 U.S.C. 103(a)

The rejection of Claims 2, 3, 5-7, 9, 13-18, 20, 22, 27-34 and 36-41 under 35 U.S.C. 103(a) as being unpatentable over Jun or Son et al. is respectfully traversed.

CLAIMS 2, 3, 5-7, 9, 13-18, 20, 22, 27-34 AND 36-41 ARE PATENTABLE OVER JUN

As explained above, Jun neither suggests nor provides the motivation to form substantially rectangular insulating spacers or perform subsequent etching steps under conditions that maintain such substantially rectangular insulating spacers. As a result, the claims that depend from Claims 27 and 35, which necessarily contain one or more limitations above and beyond those recited in Claims 27 and 35, cannot be suggested or rendered obvious by Jun. On this basis alone, Claims 2,3, 5-7, 9, 13-18, 20, 22, 27-34 and 36-41 are patentable over Jun.

However, as the application notes, substantially rectangular insulating spacers provide advantages over conventional spacers in that subsequent sputter etch cleaning of contact holes containing such substantially rectangular insulating spacers may be conducted without sufficiently eroding the spacers. (See, for example, from page 25, line 16, through page 26, line 24, of the specification). As a result, high quality contacts may be formed in such contact holes provided by the present invention.

Jun is silent with regard to sputter etch cleaning of contact holes. Consequently, Jun cannot appreciate the advantages of, or the results provided by, the presently claimed method.

Even further, the rejection is based on mere conclusory assertion(s) and completely lacks factual support. No particular disclosures or teachings in any reference, including the references presently applied against the claims, have been cited in support of such conclusory assertions. Consequently, a *prima facie* case of obviousness has not been established.

The conclusory style of examination practiced in the present application becomes readily apparent when reviewing this ground of rejection. The rejection consists of mere assertions that routine experimentation would have been done to arrive at the desired contact. (Interestingly, and further evidencing the conclusory nature of examination in the present case, neither the contact *per se* nor any step that directly results in formation of a contact is an element of any of the present claims.)

For example, the last two paragraphs on page 3 of the Office Action states that the references "show the method substantially as claimed" and that the cited art "lacks anticipation only in not teaching the particulars of the etching system such as plasma..., low selectivity..., a cleaning sputter etch for cleaning the [structure] after etching..." The first paragraph on page 4 of the Office action then asserts that "(i)t would have been obvious to one of ordinary skill in the art to have vary the etching parameters and to have used a plasma... and to have cleaned the insulating layer with a sputter etch after etching the etch stop... to obtain desired contact." However, no factual basis for this assertion, such a column and

line numbers of a reference, are provided in support. If modification of such parameters and inclusion of such additional steps would have been routine and obvious, surely art exists that shows or suggests such modification. However, no such art has been cited in support of the conclusory assertions on which the present rejections are based. Consequently, a *prima facie* case of obviousness has been established.

Furthermore, as shown above, Son et al. fail to disclose any of the following features of the claims:

- Etching a conformal insulating layer under conditions providing insulating spacers having a substantially rectangular profile;
- Subsequently anisotropically etching the structure with an etchant having a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacer;
- Forming an electrically insulative spacer having a substantially rectangular cross-sectional shape in a plane substantially perpendicular to the substrate surface;
- Etching an etch stop layer with an etchant having a selectivity sufficiently low to maintain the substantially rectangular cross-sectional shape of the insulating spacer;

much less the features recited in the dependent claims.

If is quite clear from a cursory review of the record that *prima facie* grounds of rejections have not been established. Consequently, the rejections should be withdrawn, and the application should be allowed.

CLAIMS 2, 3, 5-7, 9, 13-18, 20, 22, 27-34 AND 36-41 ARE PATENTABLE OVER SON ET AL.

For the sake of brevity, all of the above arguments are incorporated herein in support of the patentability of the claims over Son et al. However, in addition to these arguments, Son et al. neither

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perform nor suggest anisotropic etching after the insulating spacer formed. In addition, similar to Jun, Son et al. teach that etching selectivity for their third insulating layer and the underlying protective layers are considerably different from each other (see, e.g., col. 4, lines 14-22). By contrast, in the claimed method, the selectivity for etch stop material relative to an insulating layer is sufficiently low to retain the substantially rectangular profile of the insulating spacer. In the example shown in the figures, this selectivity is as low as one (essentially no selectivity). Therefore it appear that Son et al. also lead one away from the claimed method rather than towards it. **This is the antithesis of obviousness.**

Consequently, Claims 2, 3, 5-7, 9, 13-18, 20, 22, 27-34 and 36-41 are patentable over Son et al.

CONCLUSION

In view of the above remarks, the present claims are fully patentable over the cited references. Consequently, these grounds of rejections should be withdrawn.

The present application is in condition for allowance. Early notice to that effect is earnest solicited.

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF

28C2

9/10/98

65506

GURLEY, LYNNE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

Serial No.: 08/577,751 Filed: December 22, 1995

Examiner: L. Gurley Group Art Unit: 2814

Attorney Docket No.: CYP-002

98 JUN 29 P3:54

Milpitas, California
June 22, 1998

Attn.: Refund Section, Accounting Division, Office of Finance
Assistant Commissioner for Patents
Washington, D. C. 20231

REQUEST FOR REFUND UNDER 37 C.F.R. § 1.26

Sir:

On April 2, 1998, Applicants submitted a Response under 37 CFR 1.116 in response to the Office Action mailed December 2, 1997, in the above-referenced application, as shown by the transmittal letter sent with the Response (a copy of which is attached hereto as Exhibit A). As also shown by the enclosed copy of the transmittal letter (Exhibit A), with the Response, Applicants also submitted a Petition For Extension of Time to request a one month extension of time to respond to the Office Action, together with a check for $110.00 (a copy of which is attached hereto as Exhibit B).

Subsequently, on April 29, 1998, Applicants submitted a Notice Of Appeal in the above-referenced application, as shown by the transmittal letter sent with the Notice of Appeal (a copy of

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which is attached hereto as Exhibit C). As also shown by the enclosed copy of that transmittal letter (Exhibit C), with the Notice of Appeal, Applicants also submitted a Petition For Extension of Time to request a two month extension of time to respond to the outstanding Office Action, together with a check for $710.00 (a copy of which is attached hereto as Exhibit D) to pay the fees for filing the Notice of Appeal and requesting a two month extension of time. However, since Applicants had previously paid $110.00 for a one month extension of time to respond to the outstanding Office Action, the amount of this check (Exhibit D) should have been $600.00, instead of $710.00. Applicants inadvertently neglected to make the appropriate adjustment when calculating the fee due.

In view of the foregoing, Applicants request a refund of $110.00, reflecting the amount of the two month extension of time fee that had previously been paid. Applicants further request that the refund be paid by check made out to David R. Graham. If there are any questions about this Request for Refund, please telephone Applicants' undersigned attorney at (408) 945-9912.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on June 22, 1998.

6-22-98 David R. Graham
Date Signature

Respectfully submitted,

David R. Graham

David R. Graham
Reg. No. 36,150
Attorney for Applicants

SAMSUNG-1008.191

EXHIBIT A

Attorney Docket No.: CYP-002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

April 2, 1998

Box AF
Assistant Commissioner for Patents
Washington, D. C. 20231

Re: Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning
Serial No.: 08/577,751
Filed: December 22, 1995
Examiner: L. Gurley
Group Art Unit: 1104

Transmitted herewith are the following documents in the above-identified application:

(1) A Response Under 37 C.F.R. 1.116 (13 pages);
(2) A Petition for Extension of Time (1 page);
(3) Copies of 4 references cited in Response Under 37 C.F.R. 1.116;
(4) A check for $110.00 (Check No. 1188);
(5) A return receipt postcard;
(6) This sheet in duplicate.

The fee is calculated as follows (small entity status is not claimed):

CLAIMS AS AMENDED

	Claims After Amendment		Highest Number Paid For		Additional Claims		Rate		Fee
Total Claims:	29	-	29	=	0	X	$22	=	$ 0.00
Independent Claims:	3	-	3	=	0	X	$82	=	$ 0.00
___ First filing of one or more multiple dependent claims ($260 total fee)									$ 0.00
X Fee for Petition for Extension of Time (1 month)									$ 110.00
TOTAL FEE:									**$ 110.00**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on April 2, 1998.

4-2-98 — David R. Graham
Date — David R. Graham

Respectfully submitted,

David R. Graham

David R. Graham
Reg. No. 36,150
Attorney for Applicants
1337 Chewpon Ave.
Milpitas, CA 95035

EXHIBIT B

DAVID R. GRAHAM
1337 CHEWPON AVE.
MILPITAS, CA 95035
408-945-9912

1188

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1211

PAY TO THE ORDER OF Commissioner of Patents and Trademarks $ 110.00

One hundred ten + 00/100 DOLLARS

COMERICA
COMERICA BANK - CALIFORNIA
1289 SOUTH PARK VICTORIA DRIVE
MILPITAS, CALIFORNIA 95035

FOR CYP-002

David Graham

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EXHIBIT C

Attorney Docket No.: CYP-002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

April 29, 1998

Box AF
Assistant Commissioner for Patents
Washington, D. C. 20231

Re: Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning
Serial No.: 08/577,751
Filed: December 22, 1995
Examiner: L. Gurley
Group Art Unit: 2814

Transmitted herewith are the following documents in the above-identified application:

(1) Notice of Appeal (1 page);
(2) Petition for Extension of Time - 2 months (1 page);
(3) Check for $710.00 (Check No. 1206);
(4) Return receipt postcard; and
(5) This sheet in duplicate.

The fee is calculated as follows (small entity status is not claimed):

_x_	Fee for Notice of Appeal	$	310.00
_x_	Fee for Petition for Extension of Time (2 months)	$	400.00
TOTAL FEE:		**$**	**710.00**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on April 29, 1998.

4-29-98 (Date) David R. Graham (Signature)

Respectfully submitted,

David R. Graham

David R. Graham
Reg. No. 36,150
Attorney for Applicants
1337 Chewpon Ave.
Milpitas, CA 95035

EXHIBIT D

DAVID R. GRAHAM
1337 CHEWPON AVE.
MILPITAS, CA 95035
408-945-9912

30-3752/866
1211

1206

4-29 1998

PAY TO THE ORDER OF Commissioner of Patents and Trademarks $ 710.00

Seven hundred ten + 00/100 DOLLARS

COMERICA
COMERICA BANK - CALIFORNIA
1289 SOUTH PARK VICTORIA DRIVE
MILPITAS, CALIFORNIA 95035

FOR CYP-002 Not. Appl. Ext time

David Graham

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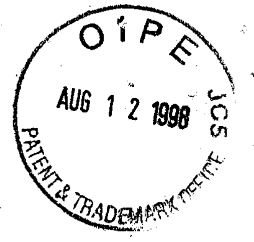

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Attorney Docket No.: CYP-002-C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

August 7, 1998

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Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Title: Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning
Serial No.: 08/577,751
Filed: December 22, 1995
Examiner: L. Gurley
Group Art Unit: 2814

Transmitted herewith are the following documents in the above-identified application:

(1) Preliminary Remarks (12 pages);
(2) Declaration Under 37 C.F.R. 1.132 (7 pages) with Appendix 1 (5 pages)
(3) Return receipt postcard; and
(4) This sheet in duplicate.

The fee is calculated as follows (small entity status is not claimed):

CLAIMS AS AMENDED

	Claims After Amendment		Highest Number Paid For		Additional Claims		Rate		Fee
Total Claims:	29	-	29	=	0	X	$22	= $	0.00
Independent Claims:	3	-	3	=	0	X	$82	= $	0.00
___ First filing of one or more multiple dependent claims ($270 total fee)								$	0.00
___ Fee for Petition for Extension of Time (___ months)								$	0.00
TOTAL FEE:								**$**	**0.00**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on August 7, 1998.

8-7-98 David R. Graham
Date Signature

Respectfully submitted,

David R. Graham

David R. Graham
Reg. No. 36,150
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1337 Chewpon Ave.
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Tel. No.: (408) 945-9912

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PATENT & TRADEMARK OFFICE

Attorney Docket No.: CYP-002-C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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AUG 17 1998
GROUP 2200

August 7, 1998

Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Applicants: James E. Nulty et al.
Assignee: Cypress Semiconductor Corporation
Title: Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning
Serial No.: 08/577,751
Filed: December 22, 1995
Examiner: L. Gurley
Group Art Unit: 2814

Transmitted herewith are the following documents in the above-identified application:

(1) Preliminary Remarks (12 pages);
(2) Declaration Under 37 C.F.R. 1.132 (7 pages) with Appendix 1 (5 pages)
(3) Return receipt postcard; and
(4) This sheet in duplicate.

The fee is calculated as follows (small entity status is not claimed):

CLAIMS AS AMENDED

	Claims After Amendment		Highest Number Paid For		Additional Claims		Rate		Fee
Total Claims:	29	-	29	=	0	X	$22	=	$ 0.00
Independent Claims:	3	-	3	=	0	X	$82	=	$ 0.00
___ First filing of one or more multiple dependent claims ($270 total fee)									$ 0.00
___ Fee for Petition for Extension of Time (___ months)									$ 0.00
TOTAL FEE:									$ 0.00

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on August 7, 1998.

8-7-98 David R. Graham
Date Signature

Respectfully submitted,

David R. Graham

David R. Graham
Reg. No. 36,150
Attorney for Applicants
1337 Chewpon Ave.
Milpitas, CA 95035
Tel. No.: (408) 945-9912

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2212

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751

Group Art Unit: 1104

Filed: December 22, 1995

Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

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GROUP 2200

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY REMARKS

Prior to examination of the above-identified application on the merits, entry and consideration of the following remarks are respectfully requested.

REMARKS

The present claims concern, in one aspect,

a) a method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising the steps of:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on August 7, 1998, 1998.

David R. [signature] 8-7-98
Signature Date

i) etching a conformal second insulating layer overlaying the devices and the contact region under conditions providing insulating spacers having a substantially rectangular profile in the contact region; and subsequently

ii) anisotropically etching the structure having the substantially rectangular insulating spacers in the contact region with an etchant having a selectivity for an etch stop material relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop material being distinct from the second insulating layer (see Claim 27 and claims depending therefrom),

and in a second aspect,

b) a method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

i) forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

ii) forming an etch stop layer over the spacer and the first and second electrically conductive regions;

iii) forming a blanket layer over the etch stop layer;

iv) selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region;

v) etching the etch stop layer to remove part of the etch stop layer formed over the first electrically conductive region, under conditions that etch (i) the material of the etch stop layer adjacent to the spacer and (ii) the spacer such that the substantially rectangular cross-sectional shape of the spacer is maintained (Claim 35 and claims depending therefrom; hereinafter, paragraphs (a)(i)-(b)(v) are collectively referred to as "the presently claimed invention").

The present application is a CPA, filed to gain entry and consideration of the accompanying executed Declaration under 37 C.F.R. 1.132, an unexecuted copy of which was filed with the CPA request papers on June 29, 1998. The Declaration addresses the bases for the rejections in the Office Action dated December 2, 1997, on their technical and logical merits. The Declaration also sets forth factual and logical bases for the conclusion that the presently claimed invention is neither anticipated by nor obvious to one of ordinary skill in the art in view of the cited references (Jun and Son et al.).

THE PRESENTLY CLAIMED INVENTION IS NOT ANTICIPATED BY THE CITED <u>REFERENCES</u>

For example, paragraph (a)(i) above (see Claim 27) recites a method of forming a contact opening in a structure including a step of "etching a conformal second insulating layer... under

conditions providing insulating spacers having a substantially rectangular profile." (See paragraph 6 of the accompanying executed Declaration).

Jun teaches forming a sidewall spacer 26 (column 3, lines 58-63) by depositing and selectively anisotropically etching a silicon oxide layer. However, Jun is silent as to the etching conditions used to produce the spacer 26. Thus, it cannot be assumed that such etching conditions are established so as to form a spacer having a substantially rectangular profile, as recited in paragraph (a)(i) above. (See paragraph 7 of the accompanying executed Declaration).

Furthermore, it cannot be presumed that the etching conditions used by Jun (whatever they might have been) would have inherently produced a spacer having a substantially rectangular profile. This is particularly so since conventional etching techniques used to form spacers at or about the time that the Jun application was filed did not produce spacers having a substantially rectangular profile. (See, e.g., U.S. Patent No. 5,382,483, issued to Young on January 17, 1995, element 15 in FIG. 3E, col. 3, lines 37-39, and col. 5, lines 24-36; U.S. Patent No. 5,384,281, issued to Kenney et al. on January 24, 1995, elements 13 and 15 in Figs. 4-7, col. 5, lines 18-23 and col. 8, lines 28-33; U.S. Patent No. 5,562,801, issued to Nulty on October 8, 1996, col. 7, lines 28-34, col. 9, lines 16-21 and 53-61, col. 12, lines 11-15, col. 13, lines 16-26, and col. 15, lines 32-43; and Givens et al., p. 429, bottom of the right-hand column, Table I, and p. 431, top of the right-hand column, Table II; each of which was submitted with the Information Disclosure Statement filed on August 11, 1997). Rather, such spacers typically had a sloping, beveled or rounded sidewall, as shown, for example, in FIGS. 2B and 3 of the drawings for the present patent application. (See paragraph 8 of the accompanying executed Declaration).

Sloped or non-rectangular spacers were thought to be desirable to produce adequate filling of the contact opening and avoid the so-called "cusping" or "breadloafing" effect. For example, Ong, U.S. Patent No. 5,371,042 (submitted with the Response filed on April 2, 1998), shows pronounced cusping in contact holes having vertical sidewalls (Fig. 1). Ong teaches that faceted sidewalls (Fig. 2) avoid formation of voids in the contacts. Wang, U.S. Patent No. 5,108,570 (submitted with the Response filed on April 2, 1998), shows pronounced cusping even in contact holes having sloped sidewalls (Fig. 1). Tracy, U.S. Patent No. 4,970,176 (submitted with the Response filed on April 2, 1998), states that flared or tiered vias reduce cusping, but at the cost of increased area (col. 1, ll. 48-51). Robinson, "Al hits sub-0.25 micron vias," Electrical Engineering Times, Feb. 3, 1997 (submitted with the Response filed on April 2, 1998), teaches that cusping and voids are a problem when filling small diameter, high aspect ratio via holes. (See paragraph 9 of the accompanying executed Declaration).

In addition, the contact opening width at the bottom of the contact openings has historically been of paramount important. Whether the spacer sidewall was sloping, rounded, faceted or vertical was typically of less concern. Consequently, any presumption that the etching conditions used by Jun (whatever they might have been) either (i) actually produced or (ii) would have inherently produced a spacer having a substantially rectangular profile is not accurate. (See paragraphs 10-11 of the accompanying executed Declaration).

Thus, Jun does not disclose the subject matter of paragraphs (a)(i)-(ii) above for a number of reasons:

a) Jun is silent with regard to anisotropic etch conditions and the shape of the spacer 26;

b) The references in paragraph 8 above demonstrate that spacers may have a sloping, beveled or rounded sidewall, and that etch conditions may be controlled to form spacers having such a shape;

c) The references in paragraphs 8-9 above demonstrate the desirability of forming spacers having a sloping, beveled, faceted or rounded sidewall; and

d) One therefore cannot presume that Jun inherently discloses a spacer having a substantially rectangular shape, or an etching process or etch conditions that inherently form such a spacer. (See paragraph 12 of the accompanying executed Declaration).

Paragraph (a)(ii) above recites a step of "anisotropically etching said structure... with an etchant having a selectivity for an etch stop material relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers." As stated in the present patent application at page 25, lines 1-9, such an etchant yields a spacer that retains its rectangular or "boxy" profile. Jun does not teach or suggest performing an anisotropic etch using such an etchant. (See paragraphs 13-14 of the accompanying executed Declaration).

For example, as shown in Fig. 4(J) and 4(K) of the above-captioned patent application, an etchant having a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacers may etch the insulating spacer material at about the same rate as it etches the etch stop material. Thus, in one embodiment, a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacers may be as low as one (essentially no selectivity; see paragraph 15 of the accompanying executed Declaration).

By contrast, the etch steps or processes of Jun appear to show **complete** selectivity (see col. 4, lines 11-14, 21-25, 27-32 and 59-66, and Figs. 2 (F)-(H) and Fig. 2 (K) of Jun). Consequently, it appears that the etch steps or processes disclosed by Jun actually teach away from the present invention. As a result, Jun does not disclose the subject matter of paragraphs 4(a)(i)-(ii) above. (See paragraphs 16-17 of the accompanying executed Declaration).

Paragraph (b)(i) above recites "forming an electrically insulative spacer adjacent to [a] second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape..." As discussed above with respect to the subject matter of paragraphs (a)(i)-(ii) above, Jun neither teaches or suggests such an electrically insulative spacer. (See paragraph 18 of the accompanying executed Declaration).

Furthermore, Jun neither teaches nor suggests other features in paragraphs (b)(i)-(v) above, such as "etching the etch stop layer... under conditions such that the substantially rectangular cross-sectional shape of the spacer is maintained" (paragraph (b)(v)). Consequently, Jun does not explicitly or inherently disclose the subject matter described in paragraphs (b)(i)-(v) above. (See paragraphs 19-20 of the accompanying executed Declaration).

Furthermore, Son et al. disclose a method of forming a contact region in which a second conductive layer is deposited onto an insulating layer overlying a gate. A portion of the second conductive layer is then etched to form an etch protective layer over a portion of the insulating layer (see Fig. 1 and col. 2, lines 4-10). A portion of the etch protective layer, the insulating layer and the first conducting (gate) layer are then etched to form gate electrodes (see Fig. 2, col. 2, lines 10-19). Sidewall spacers are then formed from a second insulating layer deposited over the

gate electrodes (see Fig. 4, and col. 2, lines 21-31; see also paragraph 21 of the accompanying executed Declaration).

For the sake of argument, let us assume that the spacers of Son et al. are "substantially rectangular" (although, in view of the above remarks, this is clearly not the case). However, even if we make this assumption, Son et al. do not perform an anisotropic etch step after forming the insulating sidewall spacers (see from col. 2, line 32 through col. 4, line 49 of Son et al.). As a result, Son et al. do not describe the step recited in paragraph 4(a)(ii) above. Consequently, Son et al. cannot disclose the method recited in paragraphs 4(a)(i)-(ii) above. (See paragraphs 22-23 of the accompanying executed Declaration).

Furthermore, as discussed above, Son et al. form the etch stop layer before forming the insulating spacer. As a result, Son et al. cannot (i) form an etch stop layer over the spacer or (ii) remove a second part of the etch stop layer under conditions that maintain the substantially rectangular cross-sectional shape of the spacer. (See paragraph 24 of the accompanying executed Declaration).

Therefore, Son et al. do not describe the steps recited in paragraphs 4(b)(ii) and 4(b)(v) above, and cannot disclose the subject matter described in paragraphs 4(b)(i)-(v) above. (See paragraph 25 of the accompanying executed Declaration).

THE PRESENTLY CLAIMED INVENTION IS NOT OBVIOUS IN VIEW OF THE <u>CITED REFERENCES</u>

Neither Jun nor Son et al. provide motivation to form substantially rectangular spacers as described in paragraphs (a)(i)-(ii) above, rather than sloped spacers, for the reasons given in paragraphs 8-10 of the accompanying executed Declaration. Furthermore, as demonstrated by the

references cited in paragraphs 8-9 of the Declaration, the art as a whole does not appear to provide the motivation to produce a substantially rectangular sidewall spacer. (See paragraphs 26-27 of the accompanying executed Declaration).

Substantially rectangular sidewall spacers would be expected to lead to increased cusping and void formation in subsequently formed contacts. In turn, increased cusping and void formation would be expected to lead to increased defect and/or failure rates in subsequently formed integrated circuits. (See paragraph 27 of the accompanying executed Declaration).

Therefore, neither Jun nor Son et al. suggest or provide the motivation to form substantially rectangular insulating spacers or perform subsequent etching steps under conditions that maintain such substantially rectangular insulating spacers. As a result, the presently claimed invention is not suggested by either Jun or Son et al. to one of ordinary skill in the art(s) most relevant to the presently claimed invention. (See paragraph 28 of the accompanying executed Declaration).

In addition, as the present application notes, substantially rectangular insulating spacers provide advantages over conventional spacers. Subsequent sputter etch cleaning of contact holes containing such substantially rectangular insulating spacers may be conducted without sufficiently eroding the spacers. (See, for example, from page 25, line 16, through page 26, line 24, of the present application). As a result, high quality contacts may be formed in contact holes formed by the presently claimed invention. (See paragraph 29 of the accompanying executed Declaration).

Both Jun and Son et al. are silent with regard to sputter etch cleaning of contact holes. Consequently, neither Jun nor Son et al. appreciate or suggest the advantages of and/or the

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results provided by the presently claimed invention. (See paragraph 30 of the accompanying executed Declaration).

Furthermore, no particular disclosures or teachings in any reference, including Jun and Son et al., have been cited in support of the conclusory assertions. Consequently, the rejection appears to be based on mere conclusory assertion(s) and appears to completely lack factual support. (See also paragraph 31 of the accompanying executed Declaration).

When reviewing the grounds for rejection in the Office Action dated December 12, 1997, one reads only unsupported assertions that Jun and/or Son et al. shows the method as claimed. The entire reference (i.e., either Jun or Son et al.) is relied upon, without indicating whether any particular part of the disclosure is relevant to the claims or any particular element in the claims, much less that particular portions of the disclosure are relevant to particular elements of the claims. (See also paragraph 32 of the accompanying executed Declaration).

For example, the last two paragraphs on page 3 of the Office Action state that the references "show the method substantially as claimed" and that the cited art "lacks anticipation only in not teaching the particulars of the etching system such as plasma..., low selectivity..., a cleaning sputter etch for cleaning the [structure] after etching..." The first paragraph on page 4 of the Office action then asserts that "(i)t would have been obvious to one of ordinary skill in the art to have varied the etching parameters and to have used a plasma... and to have cleaned the insulating layer with a sputter etch after etching the etch stop... to obtain the desired contact." However, no factual basis for this assertion, such as column and line numbers of a reference, are provided in support of the assertion. (See also paragraph 33 of the accompanying executed Declaration).

If modification of such parameters and inclusion of such additional steps would have been routine and obvious, references that show or suggest such modification should be easily found. However, no such references have been cited in support of the conclusory assertions on which the present rejections are based. Rather, the references cited in paragraphs 8-9 of the accompanying Declaration support the opposite conclusion; i.e., that it would not be obvious to form a spacer having a substantially rectangular profile and/or maintain the substantially rectangular profile of such a spacer after its formation. (See also paragraphs 34-35 of the accompanying executed Declaration).

In addition to the above, Son et al. neither perform nor suggest anisotropic etching after the insulating spacer is formed. In addition, similar to Jun, Son et al. teach that etching selectivity for their third insulating layer and the underlying protective layers are considerably different from each other (see, e.g., col. 4, lines 14-22 of Son et al.; see also paragraph 36 of the accompanying executed Declaration).

By contrast, in the invention described in paragraphs (a)(i)-(ii) above, the selectivity for etch stop material relative to an insulating layer is sufficiently low to retain the substantially rectangular profile of the insulating spacer. In the example shown in the figures, this selectivity is as low as one (essentially no selectivity; see paragraph 37 of the accompanying executed Declaration).

Furthermore, in the invention described in paragraphs (b)(i)-(v) above, the last step is performed under conditions that maintain the substantially rectangular shape of the spacer. Therefore, it appears that Son et al. also lead one away from the presently claimed invention, rather than towards it. (See paragraphs 38-39 of the accompanying executed Declaration).

Consequently, it is the Declarant's opinion that the presently claimed invention is not suggested to one of ordinary skill in the art in view of the teachings of Jun and Son et al. (See paragraph 40 of the accompanying executed Declaration).

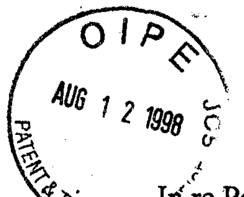
CONCLUSION

As a result, the present claims are fully patentable over the cited references. Therefore, the present grounds of rejection are unsustainable, and should be withdrawn.

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751 Group Art Unit: 1104

Filed: December 22, 1995 Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Assistant Commissioner for Patents
Washington, D.C. 20231

DECLARATION UNDER 37 C.F.R. 1.132

I, James E. Nulty, hereby declare and state that:

1. I am a named inventor in the above-identified patent application.

2. My professional history is attached hereto as Appendix I.

3. I have read and I understand the above-identified patent application; the Office Action dated December 12, 1997; the response to the Office Action filed on April 2, 1998; and the references cited hereunder.

4. I understand that the invention presently claimed in the above-identified U.S. patent application concerns, in one aspect,

   a) a method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising the steps of:

      i) etching a conformal second insulating layer overlaying the devices and the contact region under conditions providing insulating spacers having a substantially rectangular profile in the contact region; and subsequently

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on August 7, 1998, 1998.

David R. Graham 8-7-98
Signature Date

ii) anisotropically etching the structure having the substantially rectangular insulating spacers in the contact region with an etchant having a selectivity for an etch stop material relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop material being distinct from the second insulating layer (see Claim 27 and claims depending therefrom),

and in a second aspect,

b) a method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

i) forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

ii) forming an etch stop layer over the spacer and the first and second electrically conductive regions;

iii) forming a blanket layer over the etch stop layer;

iv) selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region;

v) etching the etch stop layer to remove part of the etch stop layer formed over the first electrically conductive region, under conditions that etch (i) the material of the etch stop layer adjacent to the spacer and (ii) the spacer such that the substantially rectangular cross-sectional shape of the spacer is maintained (Claim 35 and claims depending therefrom; hereinafter, the subject matter of this paragraph 4 in its entirety is collectively referred to as "the presently claimed invention").

5. In my opinion, the presently claimed invention is neither anticipated by nor obvious to one of ordinary skill in the art in view of the cited references (Jun and Son et al.).

THE PRESENTLY CLAIMED INVENTION IS NOT ANTICIPATED BY THE CITED REFERENCES

6. For example, paragraph 4(a)(i) above recites a method of forming a contact opening in a structure including a step of "etching a conformal second insulating layer... under conditions providing insulating spacers having a substantially rectangular profile."

7. Jun teaches forming a sidewall spacer 26 (column 3, lines 58-63) by depositing and selectively anisotropically etching a silicon oxide layer. However, Jun is silent as to the etching conditions used to produce the spacer 26. Thus, it cannot be assumed that such etching conditions are established so as to form a spacer having a substantially rectangular profile, as recited in paragraph 4(a)(i) above.

8. Furthermore, it cannot be presumed that the etching conditions used by Jun (whatever they might have been) would have inherently produced a spacer having a substantially rectangular profile. This is particularly so since conventional etching techniques used to form spacers at or about the time that the Jun application was filed did not produce spacers having a substantially rectangular profile. (See, e.g., U.S. Patent No. 5,382,483, issued to Young on January 17, 1995, element 15 in FIG. 3E, col. 3, lines 37-39, and col. 5, lines 24-36; U.S. Patent No. 5,384,281, issued to Kenney et al. on January 24, 1995, elements 13 and 15 in Figs. 4-7, col. 5, lines 18-23 and col. 8, lines 28-33; U.S. Patent No. 5,562,801, issued to Nulty on October 8, 1996, col. 7, lines 28-34, col. 9, lines 16-21 and 53-61, col. 12, lines 11-15, col. 13, lines 16-26, and col. 15, lines 32-43; and Givens et al., p. 429, bottom of the right-hand column, Table I, and p. 431, top of the right-hand column, Table II). Rather, such spacers typically had a sloping, beveled or rounded sidewall, as shown, for example, in FIGS. 2B and 3 of the drawings for the present patent application.

9. Sloped or non-rectangular spacers were thought to be desirable to produce adequate filling of the contact opening and avoid the so-called "cusping" or "breadloafing" effect. For example, Ong, U.S. Patent No. 5,371,042, shows pronounced cusping in contact holes having vertical sidewalls (Fig. 1). Ong teaches that faceted sidewalls (Fig. 2) avoid formation of voids in the contacts. Wang, U.S. Patent No. 5,108,570, shows pronounced cusping even in contact holes having sloped sidewalls (Fig. 1). Tracy, U.S. Patent No. 4,970,176, states that flared or tiered vias reduce cusping, but at the cost of increased area (col. 1, ll. 48-51). Robinson, "Al hits sub-0.25 micron vias," *Electrical Engineering Times*, Feb. 3, 1997, teaches that cusping and voids are a problem when filling small diameter, high aspect ratio via holes.

10. In addition, the contact opening width at the bottom of the contact openings has historically been of paramount important. Whether the spacer sidewall was sloping, rounded, faceted or vertical was typically of less concern.

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11. Consequently, any presumption that the etching conditions used by Jun (whatever they might have been) either (i) actually produced or (ii) would have inherently produced a spacer having a substantially rectangular profile is not accurate.

12. Thus, Jun does not disclose the subject matter of paragraphs 4(a)(i)-(ii) above for a number of reasons:

    a) Jun is silent with regard to anisotropic etch conditions and the shape of the spacer 26;

    b) The references in paragraph 8 above demonstrate that spacers may have a sloping, beveled or rounded sidewall, and that etch conditions may be controlled to form spacers having such a shape;

    c) The references in paragraphs 8-9 above demonstrate the desirability of forming spacers having a sloping, beveled, faceted or rounded sidewall; and

    d) One therefore cannot presume that Jun inherently discloses a spacer having a substantially rectangular shape, or an etching process or etch conditions that inherently form such a spacer.

13. Paragraph 4(a)(ii) above recites a step of "anisotropically etching said structure... with an etchant having a selectivity for an etch stop material relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers."

14. As stated in the present patent application at page 25, lines 1-9, such an etchant yields a spacer that retains its rectangular or "boxy" profile. Jun does not teach or suggest performing an anisotropic etch using such an etchant.

15. For example, as shown in Fig. 4(J) and 4(K) of the above-captioned patent application, an etchant having a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacers may etch the insulating spacer material at about the same rate as it etches the etch stop material. Thus, in one embodiment, a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacers may be as low as one (essentially no selectivity).

16. By contrast, the etch steps or processes of Jun appear to show **complete** selectivity (see col. 4, lines 11-14, 21-25, 27-32 and 59-66, and Figs. 2 (F)-(H) and Fig. 2 (K) of Jun). Consequently, it appears that the etch steps or processes disclosed by Jun actually teach away from the present invention.

17. As a result, Jun does not disclose the subject matter of paragraphs 4(a)(i)-(ii) above.

18. Paragraph 4(b)(i) above recites "forming an electrically insulative spacer adjacent to [a] second electrically conductive material, the spacer having a substantially rectangular

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cross-sectional shape..." As discussed above with respect to the subject matter of paragraphs 4(a)(i)-(ii) above, Jun neither teaches or suggests such an electrically insulative spacer.

19. Furthermore, Jun neither teaches or suggests other features in paragraphs 4(b)(i)-(v) above, such as "etching the etch stop layer... under conditions such that the substantially rectangular cross-sectional shape of the spacer is maintained" (paragraph 4(b)(v)).

20. Consequently, Jun does not explicitly or inherently disclose the subject matter described in paragraphs 4(b)(i)-(v) above.

21. Son et al. disclose a method of forming a contact region in which a second conductive layer is deposited onto an insulating layer overlying a gate. A portion of the second conductive layer is then etched to form an etch protective layer over a portion of the insulating layer (see Fig. 1 and col. 2, lines 4-10). A portion of the etch protective layer, the insulating layer and the first conducting (gate) layer are then etched to form gate electrodes (see Fig. 2, col. 2, lines 10-19). Sidewall spacers are then formed from a second insulating layer deposited over the gate electrodes (see Fig. 4, and col. 2, lines 21-31).

22. For the sake of argument, let us assume that the spacers of Son et al. are "substantially rectangular" (although, in view of the above remarks, this is clearly not the case). However, even if we make this assumption, Son et al. do not perform an anisotropic etch step after forming the insulating sidewall spacers (see from col. 2, line 32 through col. 4, line 49 of Son et al.).

23. As a result, Son et al. do not describe the step recited in paragraph 4(a)(ii) above. Consequently, Son et al. cannot disclose the method recited in paragraphs 4(a)(i)-(ii) above.

24. Furthermore, as discussed above, Son et al. form the etch stop layer before forming the insulating spacer. As a result, Son et al. cannot (i) form an etch stop layer over the spacer or (ii) remove a second part of the etch stop layer under conditions that maintain the substantially rectangular cross-sectional shape of the spacer.

25. Therefore, Son et al. do not describe the steps recited in paragraphs 4(b)(ii) and 4(b)(v) above, and cannot disclose the subject matter described in paragraphs 4(b)(i)-(v) above.

THE PRESENTLY CLAIMED INVENTION IS NOT OBVIOUS IN VIEW OF THE CITED REFERENCES

26. Neither Jun nor Son et al. provide motivation to form substantially rectangular spacers as described in paragraphs 4(a)(i)-(ii) above, rather than sloped spacers, for the reasons given in paragraphs 8-10 above.

27. Furthermore, as demonstrated by the references cited in paragraphs 8-9 above, the art as a whole does not appear to provide the motivation to produce a substantially rectangular sidewall spacer. Substantially rectangular sidewall spacers would be expected to lead to increased cusping and void formation in subsequently formed contacts. In turn, increased cusping and void formation would be expected to lead to increased defect and/or failure rates in subsequently formed integrated circuits.

28. Therefore, neither Jun nor Son et al. suggest or provide the motivation to form substantially rectangular insulating spacers or perform subsequent etching steps under conditions that maintain such substantially rectangular insulating spacers. As a result, the subject matter in paragraph 4 above is not suggested by either Jun nor Son et al. to one of ordinary skill in the art(s) most relevant to the presently claimed invention.

29. However, as the present application notes, substantially rectangular insulating spacers provide advantages over conventional spacers. Subsequent sputter etch cleaning of contact holes containing such substantially rectangular insulating spacers may be conducted without sufficiently eroding the spacers. (See, for example, from page 25, line 16, through page 26, line 24, of the present application). As a result, high quality contacts may be formed in contact holes formed by the presently claimed invention.

30. Both Jun and Son et al. are silent with regard to sputter etch cleaning of contact holes. Consequently, neither Jun nor Son et al. appreciate or suggest the advantages of and/or the results provided by the presently claimed invention.

31. Furthermore, no particular disclosures or teachings in any reference, including Jun and Son et al., have been cited in support of the conclusory assertions. Consequently, the rejection appears to be based on mere conclusory assertion(s) and appears to completely lack factual support.

32. When reviewing the grounds for rejection in the Office Action dated December 12, 1997, one reads only unsupported assertions that Jun and/or Son et al. shows the method as claimed. The entire reference (i.e., either Jun or Son et al.) is relied upon, without indicating whether any particular part of the disclosure is relevant to the claims or any particular element in the claims, much less that particular portions of the disclosure are relevant to particular elements of the claims.

33. For example, the last two paragraphs on page 3 of the Office Action state that the references "show the method substantially as claimed" and that the cited art "lacks

anticipation only in not teaching the particulars of the etching system such as plasma..., low selectivity..., a cleaning sputter etch for cleaning the [structure] after etching..." The first paragraph on page 4 of the Office action then asserts that "(i)t would have been obvious to one of ordinary skill in the art to have varied the etching parameters and to have used a plasma... and to have cleaned the insulating layer with a sputter etch after etching the etch stop... to obtain the desired contact." However, no factual basis for this assertion, such a column and line numbers of a reference, are provided in support.

34. If modification of such parameters and inclusion of such additional steps would have been routine and obvious, references that show or suggest such modification should be easily found. However, no such references have been cited in support of the conclusory assertions on which the present rejections are based.

35. Rather, the references cited in paragraphs 8-9 above support the opposite conclusion; i.e., that it would not be obvious to form a spacer having a substantially rectangular profile and/or maintain the substantially rectangular profile of such a spacer after its formation.

36. In addition to the above, Son et al. neither perform nor suggest anisotropic etching after the insulating spacer is formed. In addition, similar to Jun, Son et al. teach that etching selectivity for their third insulating layer and the underlying protective layers are considerably different from each other (see, e.g., col. 4, lines 14-22).

37. By contrast, in the invention described in paragraphs 4(a)(i)-(ii) above, the selectivity for etch stop material relative to an insulating layer is sufficiently low to retain the substantially rectangular profile of the insulating spacer. In the example shown in the figures, this selectivity is as low as one (essentially no selectivity).

38. Furthermore, in the invention described in paragraphs 4(b)(i)-(v) above, the last step is performed under conditions that maintain the substantially rectangular shape of the spacer.

39. Therefore, it appears that Son et al. also lead one away from the presently claimed invention, rather than towards it.

40. Consequently, it is my opinion that the presently claimed invention is not suggested to one of ordinary skill in the art in view of the teachings of Jun and Son et al.

Date: 7-25-98

James E. Nulty

ADF

APPENDIX 1

Attorney's Docket No.:

Patent

OIPE
AUG 12 1998
PATENT & TRADEMARK

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

James E. Nulty

Serial No:

Filed:

For:

Examiner:

Art Unit:

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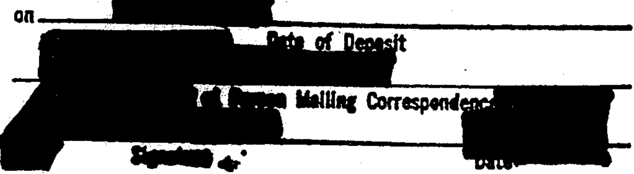

Commissioner of
Patents and Trademarks
Washington, D.C. 20231

DECLARATION OF JAMES E. NULTY UNDER 37 C.F.R. § 1.132

I, James E. Nulty hereby declare that:

1. I am a citizen of the United States, and I am currently a resident of the city of Campbell, in the state of California.

2. I am the inventor of application (Serial No.) entitled,

3. I am presently employed as Director of Technology Development at Cypress Semiconductor. I have been employed at Cypress Semiconductor since 1993. I manage all aspects of the

state-of-the-art CMOS process development, etch, photo, thin films, diffusion and metals. I have a department of 25 people that report in to me. As part of my job, I also maintain industry contacts and keep abreast of current process capabilities. In addition, I am a recognized expert in oxide etching. I developed the first oxide: nitride process known to run in production and that has been proven manufacturable in the world. I have a total of 15 years of experience in the semiconductor manufacturing industry.

4. I received a B.S. Degree in Organic (Carbon) Chemistry from the University of Santa Clara in 1980.

5. Prior to working at Cypress Semiconductor, I worked as Director of Technology at Drytek from 1989 to 1993. Drytek is a plasma etch manufacturer and it focuses exclusively on silicon dioxide (SiO_2) etching. I directed all aspects of the business, including development, mechanical and electrical engineering departments, among others. In addition, I traveled around the world conferring with plasma engineers, presenting papers, and developing new state-of-the-art equipment and processes.

From 1984 to 1989, I was a Principal Etch Engineer at VLSI Technology, where I developed various plasma etch processes.

From 1980 to 1984, I worked as a Plasma Etch Engineer at National Semiconductor. I worked in metal and poly-etch development where I used N_2 chemistry to reduce carbon polymers from an aluminum etch process.

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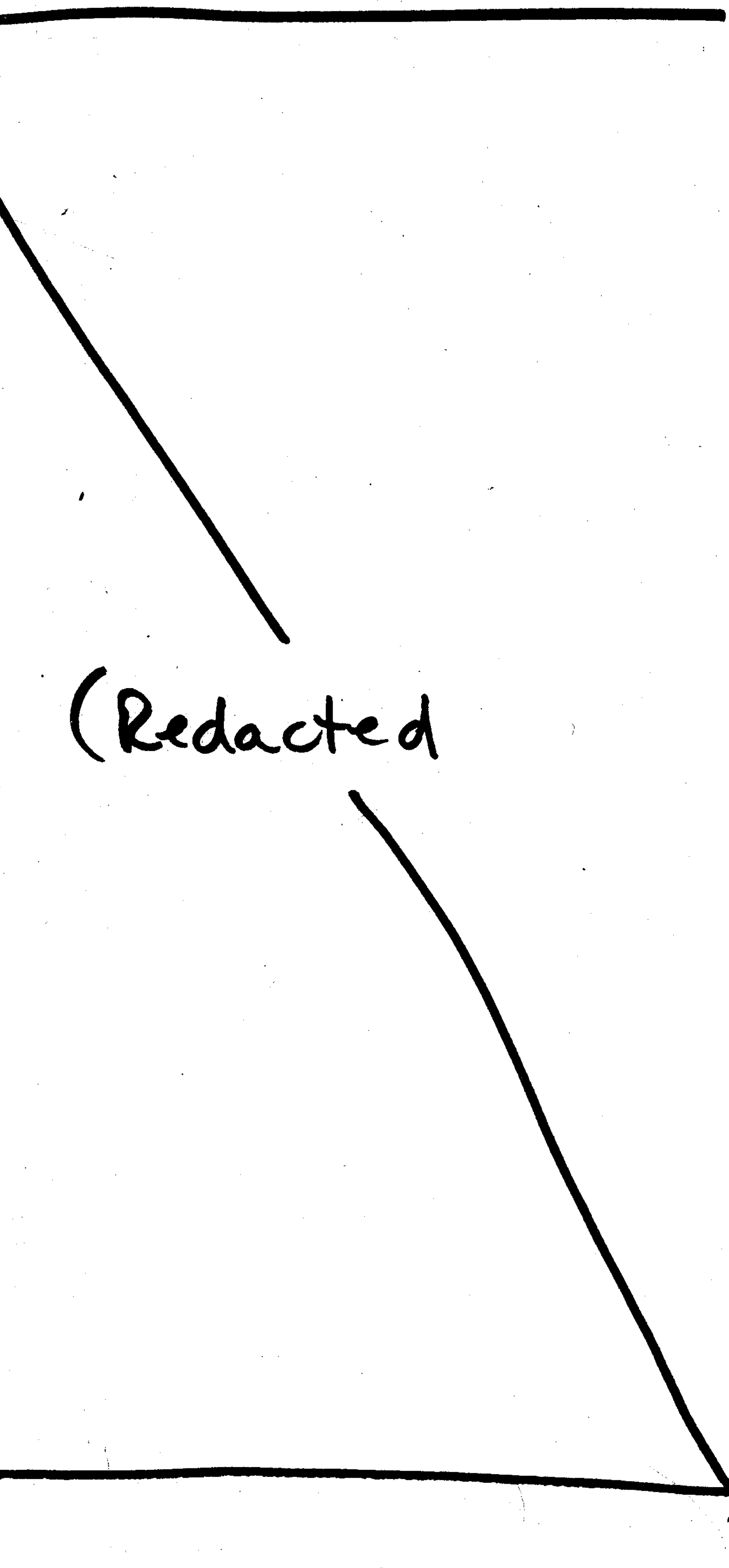
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief I believe to be true; and further that the statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon.

Executed on [redacted] in San Jose, California.

By [signature]

Interview Summary	Application No. 08/577,751	Applicant(s) Nulty et al.
	Examiner Lynne Gurley	Group Art Unit 2812

All participants (applicant, applicant's representative, PTO personnel):

(1) *Lynne Gurley* (3)

(2) *David R. Graham* (4)

Date of Interview *Sep 3, 1998*

Type: ☒ Telephonic ☐ Personal (copy is given to ☐ applicant ☐ applicant's representative).

Exhibit shown or demonstration conducted: ☐ Yes ☒ No. If yes, brief description:

Agreement ☐ was reached. ☒ was not reached.

Claim(s) discussed: *27 and 35*

Identification of prior art discussed:
Armacost, Mele, Son and Jun

Description of the general nature of what was agreed to if an agreement was reached, or any other comments:
Allowable subject matter was discussed pertaining to incorporation of the etch stop layer being etched simultaneously with the insulating spacers and that the etch stop layer is retained on the sidewall after the etch.

(A fuller description, if necessary, and a copy of the amendments, if available, which the examiner agreed would render the claims allowable must be attached. Also, where no copy of the amendents which would render the claims allowable is available, a summary thereof must be attached.)

1. ☒ It is not necessary for applicant to provide a separate record of the substance of the interview.

Unless the paragraph above has been checked to indicate to the contrary, A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION IS NOT WAIVED AND MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a response to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW.

2. ☐ Since the Examiner's interview summary above (including any attachments) reflects a complete response to each of the objections, rejections and requirements that may be present in the last Office action, and since the claims are now allowable, this completed form is considered to fulfill the response requirements of the last Office action. Applicant is not relieved from providing a separate record of the interview unless box 1 above is also checked.

Examiner Note: You must sign and stamp this form unless it is an attachment to a signed Office action.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08/577,751	12/22/95	NULTY	J	16820.P097

MM31/0922

DAVID R. GRAHAM, ESQ.
1337 CHEWPON AVE.
MILPITAS CA 95035

EXAMINER
GURLEY,L

ART UNIT	PAPER NUMBER
2812	24

DATE MAILED: 09/22/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)
*U.S. GPO: 1998-437-638/80022

1- File Copy

Office Action Summary	Application No. 08/577,751	Applicant(s) Nulty et al.
	Examiner Lynne Gurley	Group Art Unit 2812

☒ Responsive to communication(s) filed on *Jun 29, 1998*.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *2, 3, 5-7, 9, 13-18, 20, and 27-41* is/are pending in the application.

Of the above, claim(s) ______ is/are withdrawn from consideration.

☐ Claim(s) ______ is/are allowed.

☒ Claim(s) *2, 3, 5-7, 9, 13-18, 20, and 27-41* is/are rejected.

☐ Claim(s) ______ is/are objected to.

☐ Claims ______ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on ______ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on ______ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐All ☐Some* ☐None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) ______.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: ______.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). ______

☒ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

SAMSUNG-1008.224

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 6/29/98for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 08/577,751 is acceptable and a CPA has been established. An action on the CPA follows.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims 27 and 35 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Mele et al. (5,037,777, dated 8/6/91).

Mele shows the method as claimed, in Figs. 4B-5C, as a method of forming a contact opening in a structure comprising substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the

method comprising: etching a conformal second insulating layer overlying the at least two devices and the contact region under conditions providing insulating spacers in the contact region such that the insulating spacers have a substantially rectangular profile; and subsequently anisotropically etching the structure having the insulating spacers in the contact region with an etchant having a selectivity for an etch stop material relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop material being distinct from the second insulating layer (claims 27 and 35).

4. Claims 35-37 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Armacost et al. (5,759,867, dated 6/2/98, filed 4/21/95).

Armacost shows the method as claimed, in Figs. 1-3, as a method of forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface; forming an etch stop layer over the spacer and the first and second electrically conductive regions; forming a blanket layer over the etch stop layer; selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region; etching the etch stop layer to remove a second part of the etch stop layer that is formed over the first electrically conductive region, wherein the step of etching the etch stop layer is performed under conditions that etch the material of the etch stop

layer adjacent to the spacer and the spacer such that the substantially rectangular cross-sectional shape of the spacer is maintained.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-3, 5-7, 9, 13-18, 20 and 28-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mele et al. (5,037,777, dated 8/6/91).

Mele shows the method substantially as claimed and as described in the preceding paragraph.

Mele lacks anticipation only in not teaching the particulars of the etching system such as plasma, low bombardment/high neutral flux, low selectivity for the etch stop in comparison to the insulating layer, the specific type of etching apparatus, the pressure, flow rates and power parameters, and a cleaning sputter etch for cleaning the insulating layer after etching the etch stop.

It would have been obvious to one of ordinary skill in the art to have varied the etching parameters and to have used a plasma for the anisotropic etch in Mele and to have cleaned the

insulating layer with a sputter etch after etching the etch stop such as would be done by routine experimentation to obtain the desired contact.

7. Claims 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Armacost et al. (5,759,867, dated 6/2/98, filed 4/21/95).

Armacost shows the method substantially as claimed and as described in the preceding paragraphs.

Armacost lacks anticipation only in not teaching the particulars of the etching system such as plasma, low bombardment/high neutral flux, low selectivity for the etch stop in comparison to the insulating layer, the specific type of etching apparatus, the pressure, flow rates and power parameters, and a cleaning sputter etch for cleaning the insulating layer after etching the etch stop.

It would have been obvious to one of ordinary skill in the art to have varied the etching parameters and to have used a plasma for the anisotropic etch in Armacost and to have cleaned the insulating layer with a sputter etch after etching the etch stop such as would be done by routine experimentation to obtain the desired contact.

Prior Art Of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO Form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is (703) 305-3474. The examiner can normally be reached on Monday-Friday from 9:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F. Niebling, can be reached on (703) 308-3325. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

lg

September 14, 1998

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800

Notice of References Cited	Application No. 08/577,751	Applicant(s) Nulty et al.	
	Examiner Lynne Gurley	Group Art Unit 2812	Page 1 of 1

U.S. PATENT DOCUMENTS

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A	5,759,867	4/21/95 06/1998	Armacost et al.	~~437~~ 438	~~195~~ 634
B	5,037,777	8/6/91	Mele et al.	43~~7~~	~~195~~ 639
C	5,466,636	11/14/95	Cronin et al.	43~~7~~	~~187~~ 639
D	5,275,972	1/4/94	Ogawa et al.	43~~7~~	~~195~~ 639
E					
F					
G					
H					
I					
J					
K					
L					
M					

FOREIGN PATENT DOCUMENTS

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
N						
O						
P						
Q						
R						
S						
T						

NON-PATENT DOCUMENTS

	DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
U		
V		
W		
X		

GP 2812/#

February 22, 1999

OIPE JCO1
FEB 2 5 1999
PATENT & TRADEMARK OFFICE

Assistant Commissioner for Patents
Washington, D.C. 20231

VIA FIRST CLASS MAIL

Applicant(s): James E. Nulty et al.
Serial No.: 08/577,751
Filing Date: December 22, 1995
For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING
Attorney Docket No.: PM95012

Dear Sir:

Enclosed are the following items for filing in connection with the above-identified application:

Amendment; Petition for Extension of Time; Decalarartion (with attachment); Check Nos. 225906, 228118 and 228119 for $150.00, $150.00 and $110.00

Please direct all communications to Applicant's undersigned representative.

RECEIVED
99 MAR 16 AM 9:29

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on Feb. 22, 1999.

Andrew D. Fortney, Ph.D. — Date 2/22/99

3901 NORTH FIRST STREET SAN JOSE, CA 95134-1599 408•943•2600

Recycled paper.

#25
3-19-99
Roberts
Ext of time

OIPE JC67
FEB 2 5 1999

Atty. Ref. No. PM95012

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: James E. NULTY et al.

Serial No.: 08/577,751 Group Art Unit: 2812

Filed: December 22, 1995 Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Assistant Commissioner for Patents
Washington, D.C. 20231

PETITION FOR EXTENSION OF TIME TO RESPOND TO OUTSTANDING PATENT OFFICE ACTION (37 CFR 1.136(a))

Sir:

This is a petition for an extension of time for filing a Response to the Office Action dated September 22, 1998. The communication in connection with the matter for which this extension is requested is filed herewith.

	Total Months Requested	Fee
	one month	$110.00
X	two months	$400.00
	three months	$950.00
	four months	$1,510.00

[X] Three checks in the total amount of $**410.00** to cover the extension fee are attached.

99 MAR 13 AM 9:29
TECHNOLOGY CENTER
RECEIVED

03/04/1999 SLUANG 00000056 08577751
01 FC:116 380.00 OP

Refund Ref:
03/04/1999 SLUANG 00000786800

CHECK Refund Total: $30.00

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600
CYPRESS SEMICONDUCTOR CORPORATION
3939 N. First Street
San Jose, California 95134

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on Feb. 22, 1999.

Andrew D. Fortney, Ph.D. 2/22/99
Date

#26
3-19-99
Roberts
Declaration

PM95012

OIPE
FEB 25 1999
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751 | Group Art Unit: 2812

Filed: December 22, 1995 | Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Assistant Commissioner for Patents
Washington, D.C. 20231

DECLARATION UNDER 37 C.F.R. 1.131

I, **James E. Nulty**, hereby declare and state that:

1. I am an inventor of the above-identified patent application.

2. I have read and I understand (a) the above-identified patent application, (b) the Declaration Under 37 C.F.R. 1.132 dated July 25, 1998 and the references cited therein, (c) the Office Action dated September 22, 1998, (d) U.S. Patent No. 5,759,867 to Armacost et al. (hereinafter, "Armacost et al."), filed on April 21, 1995, and (e) the attached documentation in non-redacted form.

3. I understand that the above-identified application for patent claims, in one aspect:

a) a method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on Feb. 22, 1999.

[signature] 2/22/99
Signature Date

i) forming an etch stop layer over insulating spacers in the contact region, wherein the insulating spacers have a substantially rectangular profile; and subsequently

ii) anisotropically etching the structure having the insulating spacers and the etch stop layer in the contact region with an etchant having a selectivity for the etch stop layer relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop layer being different from the second insulating layer;

and, in a second aspect,

b) a method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

i) forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

ii) forming an etch stop layer over the spacer and the first and second electrically conductive regions;

iii) forming a blanket layer over the etch stop layer;

iv) selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region;

v) etching the etch stop layer to remove part of the etch stop layer formed over the first electrically conductive region, under conditions that etch (i) the material of the etch stop layer adjacent to the spacer and (ii) the spacer such that the substantially rectangular cross-sectional shape of the spacer

is maintained (hereinafter, paragraphs (a)(i)-(b)(v) are collectively referred to as "the presently claimed invention").

4. The attached documentation provides evidence of the conception and reduction to practice of at least one working embodiment of the presently claimed invention prior to April 21, 1995.

5. For example, a structure was made by an embodiment of the presently claimed invention prior to April 21, 1995 (see item 4a, "Construction of the Device," on the first page of the attached documentation).

6. The date on the micrograph of a structure made by an embodiment of the presently claimed invention is prior to April 21, 1995 (see "Method Comparison -- Invention" in the attached documentation).

7. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

8. Further Declarant saith not.

____
James E. Nulty

____
Date

ADF

INVENTION DISCLOSURE FORM

Disclosure No.________

1. INVENTOR(S)

OIPE JC69
FEB 25 1999
PATENT & TRADEMARK OFFICE

A. Name James E Nulty Empl. No. [redacted] Ext. No. [redacted]

Home Mailing Address 1037 Lenor Wy San Jose CA 95128 Home No [redacted]

Citizenship USA

B. Name Christopher J. Petti Empl. No. [redacted] Ext. No. [redacted]

Home Mailing Address 660 Sierra Ave Mountain View, CA 94041

Citizenship USA

C. Division, Dept. or Subsidiary ________

2. TITLE OF INVENTION Method for Eliminating lateral shoulder erosion on enclosed contact topographies during RF Sputter Cleaning

3. CONCEPTION OF INVENTION

a. Date of first drawing or drawings ________

Where can first drawing be found? ________

b. Date of first written description ________

Where is description found? ________

c. Date of first oral disclosure to others ________

To whom? ________

4. CONSTRUCTION OF DEVICE a.) Date Completed [redacted]

b. Was prototype made? yes

c. By whom made? James Nulty

d. Where can the prototype be found? [redacted] SEM's on JEN Computer [redacted]

5. TEST OF DEVICE a.) Date: ________ b.) Witness(s): ________

c. Results: ________

6. SALE a.) Was invention sold or offered for sale? Yes ____ No ____ b.) Date of first sale ________

Inventor(s) [signature] Date [redacted]

[signature] Date [redacted]

Witness, Read, and Understood by:

[redacted] Date [redacted]

[redacted] Date [redacted]

(Each page upon which information is entered should be signed and witnessed.)

INVENTION DISCLOSURE FORM

7. USE a. Is invention presently being used? Yes X No ______.

b. Are there specific plans for its use in near future? yes

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS. ______

9. WAS INVENTION Conceived (Yes____ (No X____ During performance of
Constructed (Yes____ (No X____ Government contract?
Tested (Yes____ (No X____

a. Contract Number ______________________
(Give Full Contract Number)

This description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as reports of any nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the description of contruction and operation.

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
2. Describe old method(s), if any, of performing the function of the invention.
3. Indicate the disadvantages of the old method(s). What problem(s) is your invention trying to solve?
4. Describe the construction of your invention, showing the changes, additions and improvements over the old method.
5. Give details of the operation if not already described under 4.
6. State the advantages of your invention over what has been done before.
7. Indicate any alternate method of construction.

______________________ Date ______
Inventor

______________________ Date ______

Witness, Read, and Understood by:

______________________ Date ______

______________________ Date ______

(Each page upon which information is entered should be signed and witnessed.)

INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

9. Features which are believed to be new.

11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet.

Inventor — Date

Witness, Read, and Understood by: — Date

Date

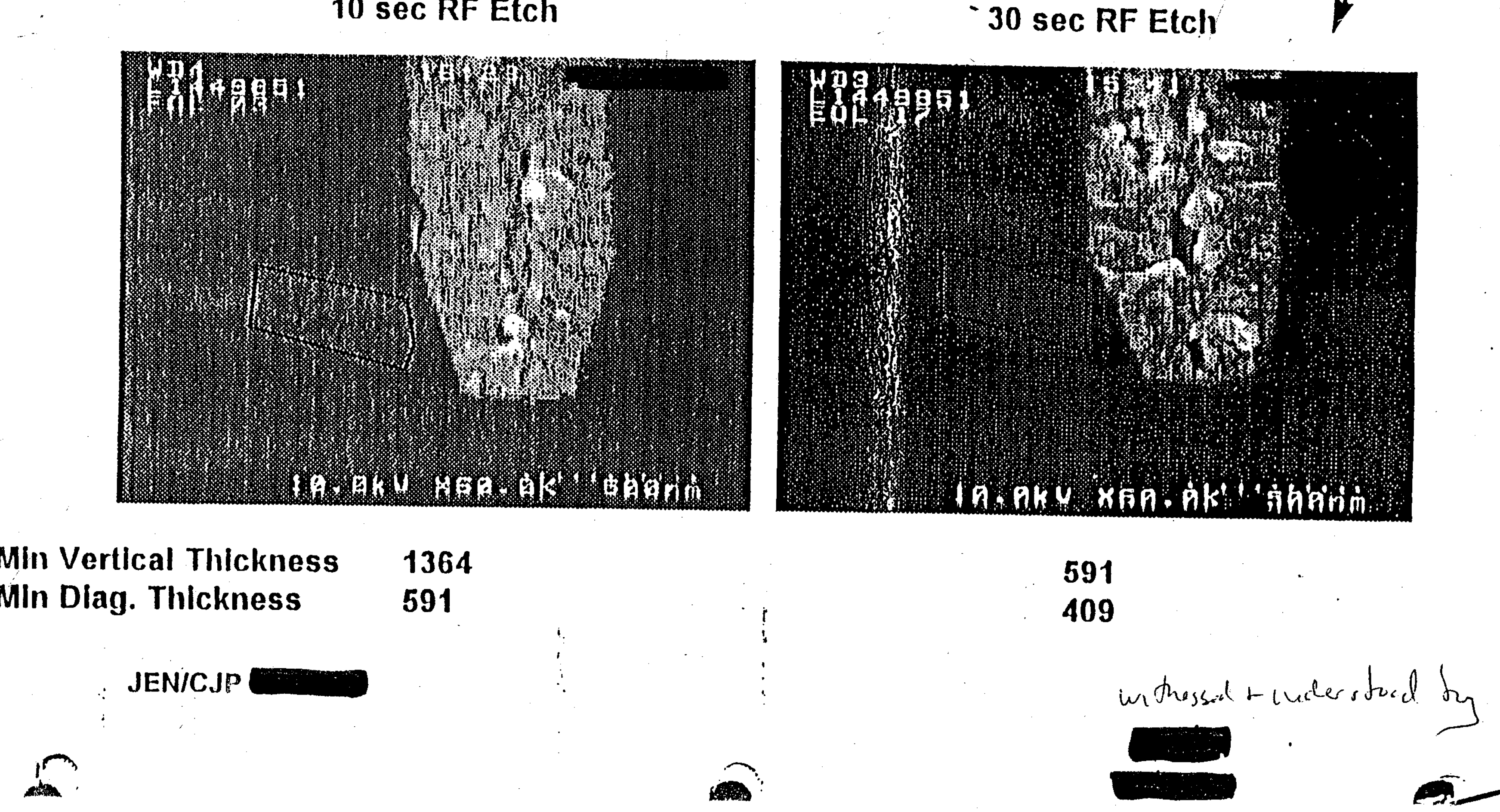
Date

(Each page upon which information is entered should be signed and witnessed.)

High Contact Resistance at LICM1E

Effect of RF Etch on Shoulder

Correlates to [redacted]



10 sec RF Etch

30 sec RF Etch

	10 sec RF Etch	30 sec RF Etch
Min Vertical Thickness	1364	591
Min Diag. Thickness	591	409

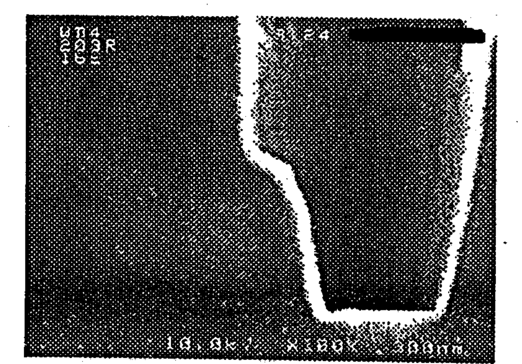
JEN/CJP [redacted]

witnessed + understood by

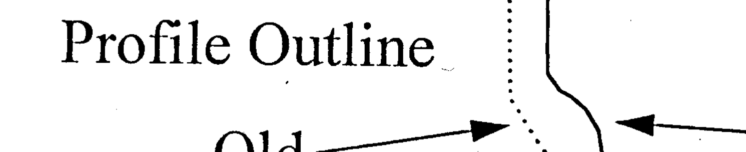
Method Comparison

Old

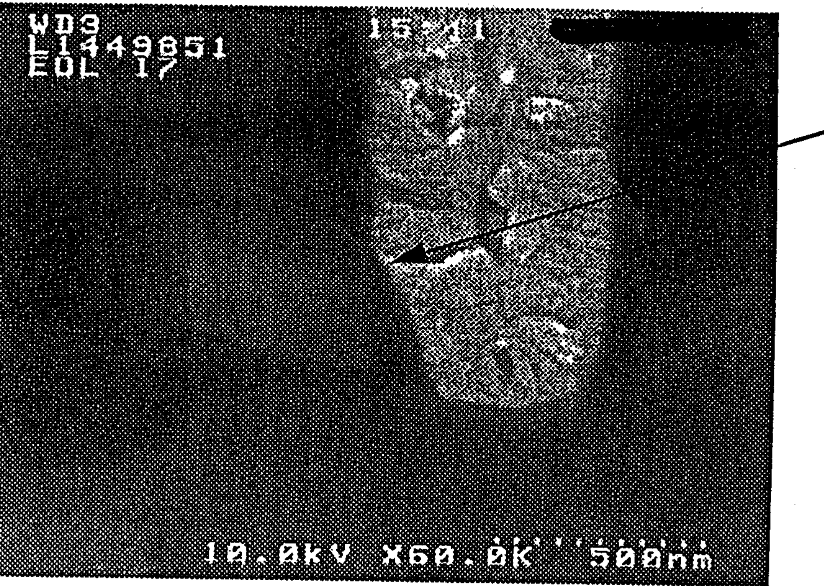
Invention

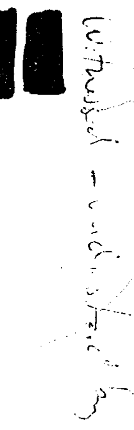


Profile Outline



Lateral Erosion Location





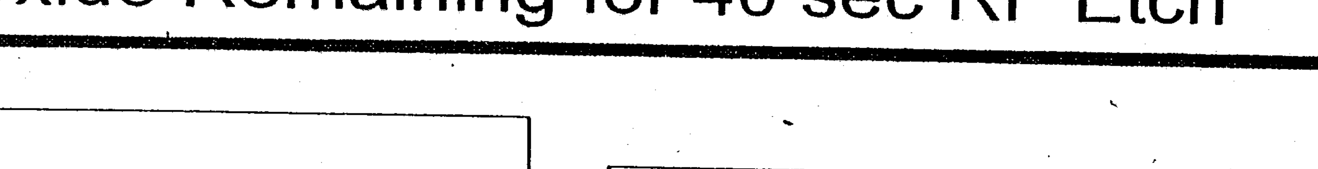
Invention Form Answers

- Old Method - selective Nit:Ox etch, leaving rounded shoulder profile. Wet etch, completely removing nitride
- Diadvantage of old methods: Leave shoulder susceptible to lateral erosion during RF Sputter etch
- Advantages of Operation: Thicker minimum oxide following RF Etch, Easy process sustaining, only have to control vertical oxide thickness. Nitride on sidewall gives thicker insulator than just oxide spacer. Larger process window; higher reliability/yield.
- Alternate methods - Different RF Etch technique which does not erode sidewall shoulder. Alternate spacer material which is not eroded by RF Etch. Alternate spacer material which may be thin following RF Etch with no yield/rel issues.
- [redacted]
- New features - Spacer profile. Most advanced etch tools facet spacer shoulder, making them susceptible to RF Etch lateral erosion. Using high pressure, poor selective Nit:Ox etch gives best profile.
- Date first written - [redacted] Meeting Minutes.
- Date first orally disclosed - [redacted] Meeting
- Value is high; yield/rel improvement; manufacturing cost reduction due to less scrap material.

witnessed + understood by

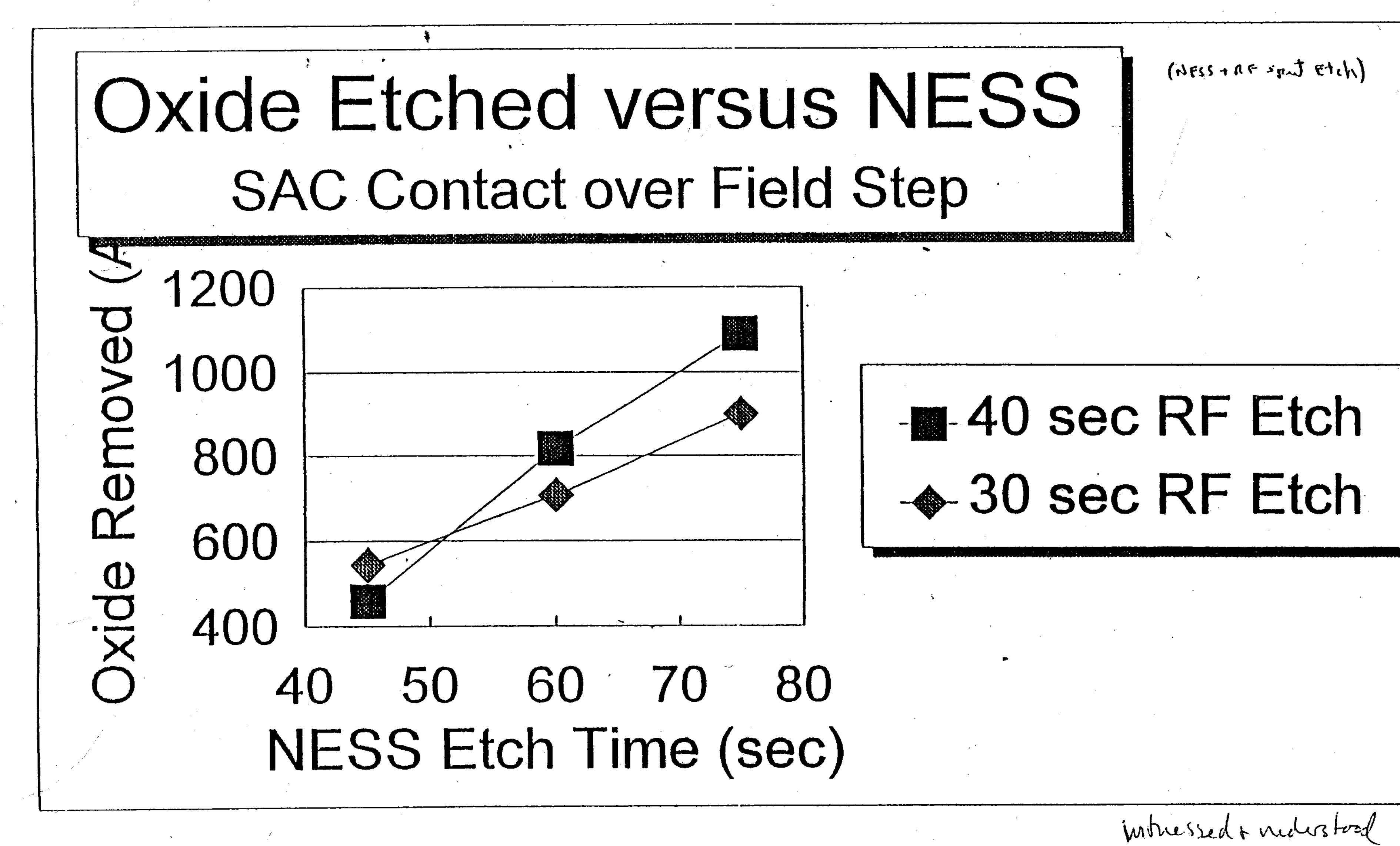
Corners Tolerance of RF Etch - SA

Min. Oxide Remaining for 40 sec RF Etch



Normalized for 1600 A NPOX @ Nit9

Witnessed & understood



witnessed + understood

#27/B 3-19-99 Robertson amdt

FEB 25 1999

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751

Group Art Unit: 2812

Filed: December 22, 1995

Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

Responsive to the Office Action dated September 22, 1998, in the above-identified application, entry and consideration of the following amendments and remarks are respectfully requested.

RECEIVED MAR 16 1999 TECHNOLOGY CENTER 2800

IN THE CLAIMS

Please amend the remaining claims as follows:

B1

1/27. (Amended) A method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of said devices comprising a conductive layer disposed over said substrate and a first insulating layer on said conductive layer, and at least two of said devices being interspaced by a contact region, said method comprising:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on Feb 22, 1999.

Signature 2/22/99 Date

41

[etching a conformal second insulating layer overlying said at least two devices and said contact region under conditions providing] forming an etch stop layer over insulating spacers in said contact region, wherein [such that] said insulating spacers have a substantially rectangular profile; and subsequently

anisotropically etching said structure having said insulating spacers and said etch stop layer in said contact region with an etchant having a selectivity for [an] said etch stop [material] layer relative to said insulating spacers ~~second insulating layer~~ sufficiently low to retain said substantially rectangular profile of said insulating spacers, said etch stop [material] layer being [distinct] different from said insulating spacer ~~second insulating layer~~.--

11. 32. (Amended) The method of Claim 27, [further comprising, after said etching step and before said anisotropically etching step, depositing an] wherein said etch stop layer is formed over the entirety of said structure having said insulating spacers in said contact region.--

15. 35. (Amended) A method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

forming an etch stop layer over the spacer and the first and second electrically conductive regions;

forming a blanket layer over the etch stop layer;

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selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region; and

etching the etch stop layer to remove a second part of the etch stop layer that is formed over the first electrically conductive region, wherein the step of etching the etch stop layer is performed under conditions that etch (i) the spacer and (ii) the material of the etch stop layer adjacent to the spacer [and the spacer] such that the substantially rectangular cross-sectional shape of the spacer is maintained.--

Cont'd B3 D2 Ins. D2

REMARKS

Claims 2, 3, 5-7, 9, 13-18, 20 and 27-41 remain active in the present application.

The present claims concern, in one aspect, a method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising:

(a) forming an etch stop layer over insulating spacers in the contact region, wherein the insulating spacers have a substantially rectangular profile; and subsequently

(b) anisotropically etching the structure having the insulating spacers and the etch stop layer in the contact region with an etchant having a selectivity for the etch stop layer relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop layer being different from the second insulating layer (Claim 27 and claims depending therefrom);

and in a second aspect, a method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a

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SAMSUNG-1008.247

region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

i) forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

ii) forming an etch stop layer over the spacer and the first and second electrically conductive regions;

iii) forming a blanket layer over the etch stop layer;

iv) selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region;

v) etching the etch stop layer to remove part of the etch stop layer formed over the first electrically conductive region, under conditions that etch (i) the material of the etch stop layer adjacent to the spacer and (ii) the spacer such that the substantially rectangular cross-sectional shape of the spacer is maintained (Claim 35 and claims depending therefrom; hereinafter, collectively referred to as "the presently claimed invention").

Applicants and their undersigned representative thank Examiner Gurley for the helpful and courteous discussions held from September 2, 1998,through September 4, 1998, and for withdrawing the previous grounds of rejection. The new grounds of rejection are traversed in part

by the present amendment and remarks and obviated in part by the accompanying Declaration under 37 C.F.R. 1.131 (the executed copy of which will be filed at the earliest opportunity).

MELE ET AL DOES NOT ANTICIPATE THE PRESENTLY CLAIMED INVENTION.

Mele et al. discloses a method for forming a multilayer semiconductor using selective planarization. Mele et al. disclose forming spacers 56 from insulating layer 48 (see col. 4, ll. 26-36; col. 5, ll. 3-6; and Figs. 3B, 3C, and 4A-4C). Alternatively, Mele et al. form spacers 60 from an unseen insulating layer (perhaps similar to insulating layer 48; see col. 5, l. 67 through col. 6, l. 1 and Fig. 5A). In the embodiment(s) shown in Figs. 3A-4D, after forming the spacers, Mele et al. do not form anything other than contact 59 in the space 58 between conductive members 42 (see col. 5, ll. 7-10, 29-31 and 50-54).

However, in the embodiment shown in Figs. 5A-5C, Mele et al. deposit a second insulating layer 52 after forming spacers 60 (see col. 6, ll. 1-3). This second insulating layer 52 is then etched, during which spacers 60 and dielectric layer 44 may also be etched (col. 6, ll. 5-12). Mele et al. disclose that the amount of etching of these materials can be controlled through proper material selection and etch chemistry (col. 6, ll. 12-14), thereby hinting that spacers 60 and dielectric layer 44 could effectively function as an etch stop for second insulating layer 52.

The alternative process shown by Mele et al. in Fig. 5A-5C does not anticipate the claimed invention. For example, Mele et al. clearly form the dielectric layer 44 over only conductive layer/region 42. Therefore, dielectric layer 44 cannot form an etch stop layer over the spacer and the first and second electrically conductive regions as recited in the second step of

Claim 35. Needless to say, spacer 60 does not form an etch stop layer over itself and the first and second electrically conductive regions. Consequently, Mele et al. do not anticipate Claim 35.

Claim 27 affirmatively recites that the etch stop layer is different from the spacer. Therefore, the spacer of Mele et al. cannot serve as the etch stop layer of Claim 27. Further, similar to Claim 35, dielectric layer 44, formed over only conductive layer/region 42, cannot form an etch stop layer over the spacer as recited in the first step of Claim 27.

Therefore, the presently claimed invention is not anticipated by Mele et al.

THE PRESENTLY CLAIMED INVENTION IS NOT OBVIOUS IN VIEW OF MELE ET AL.

The discussion above is incorporated herein in support of the patentability of the presently claimed invention.

As discussed above, Mele et al. are silent with regard to an etch stop layer over the spacer. Consequently, Mele et al. cannot disclose or suggest etching insulating spacers and an etch stop layer with an etchant having a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacers (see the second step of Claim 27 and the fifth step of Claim 35).

Therefore, the presently claimed invention is fully patentable over Mele et al.

THE PRESENTLY CLAIMED INVENTION IS NEITHER ANTICIPATED BY NOR OBVIOUS IN VIEW OF ARMACOST ET AL.

The application corresponding to Armacost et al. was filed on April 21, 1995. However, the documentation attached to the accompanying Declaration includes evidence that the presently

claimed invention was reduced to practice prior to April 21, 1995 (see paragraph 4 of the accompanying Declaration).

For example, a structure was made by an embodiment of the presently claimed invention prior to April 21, 1995 (see paragraph 5 of the accompanying Declaration and item 4a, "Construction of the Device," on the first page of the documentation attached to the accompanying Declaration). Furthermore, the date on the micrograph of a structure made by an embodiment of the presently claimed invention is prior to April 21, 1995 (see paragraph 6 of the accompanying Declaration and "Method Comparison -- Invention" in the documentation attached to the accompanying Declaration).

Therefore, the presently claimed invention was conceived and reduced to practice before the filing date of the application corresponding to Armacost et al. Consequently, Armacost et al. is not available as a reference against the presently claimed invention.

CONCLUSION

The new grounds of rejection, being traversed or overcome, are unsustainable, and should be withdrawn. As a result, the present claims are fully patentable over the cited references. Therefore, the present application is in condition for allowance. Early notice to that effect is earnestly solicited.

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF

CYPRESS SEMICONDUCTOR CORPORATION
FACSIMILE TRANSMISSION COVER SHEET

Re-faxed

DATE April 28, 1999

TO: EXAMINER GURLEY
GROUP ART UNIT 2812

FAX# (703) 308-7722

FROM: ANDREW D. FORTNEY, Ph.D., Esq.
CYPRESS SEMICONDUCTOR CORPORATION
FAX #: (408) 232-4447
PHONE: (408) 232-4437

PAGE 1 OF 16

COMMENTS: Cover letter, Amendment, Rule 131 Declaration for USSN 08/577,751

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THANK YOU.

CYPRESS SEMICONDUCTOR CORPORATION
FACSIMILE TRANSMISSION COVER SHEET

DATE April 28, 1999

TO: Examiner Gurley
Group Art Unit 2812

FAX# (703) 308-7722

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FROM: ANDREW D. FORTNEY, Ph.D., Esq.
CYPRESS SEMICONDUCTOR CORPORATION
FAX #: (408) 232-4447
PHONE: (408) 232-4437

PAGE 1 OF 16

COMMENTS: Cover letter, Amendment, Rule 131 Declaration for USSN 08/577,751

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THANK YOU.

April 28, 1999

Assistant Commissioner for Patents
Washington, D.C. 20231

VIA FACSIMILE

Applicant(s): James E. NULTY et al.
Serial No.: 08/577,751
Filing Date: December 22, 1995
Group Art Unit: 2812
Examiner: GURLEY, L.
For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING
Attorney Docket No.: CYP-002/PM95012C

FAX COPY RECEIVED
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TECHNOLOGY CENTER 2800

Dear Sir:

Enclosed are the following items for filing in connection with the above-identified application:

AMENDMENT
EXECUTED DECLARATION UNDER 37 C.F.R. 1.131

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF

I hereby certify that this correspondence is being transmitted by facsimile to: Assistant Commissioner for Patents. Washington, D.C., 20231, on April 28, 1999.

Andrew D. Fortney, Ph.D. 4/28/99
Date

3901 NORTH FIRST STREET SAN JOSE, CA 95134-1599 408•943•2600

#28/C w/decl. attach. V. Brown 5-5-99

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751

Group Art Unit: 2812

Filed: December 22, 1995

Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

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Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

Further to the Amendment filed February 22, 1999, in the above-identified application, and further to the discussion between Examiner Gurley and Applicants' undersigned representative, entry and consideration of the following amendments and remarks are respectfully requested.

IN THE CLAIMS

Please amend the claims as follows:

Claim 27, lines 11 and 13, change "second insulating layer" to --insulating spacers--.

28. (Amended) The method of Claim 27, [wherein said] further comprising forming said insulating spacers under conditions that include a bias sufficiently low and a pressure

C1

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Signature 4/28/99 Date

44

sufficiently high to provide said insulating spacers in said contact region having said substantially rectangular profile.--

--36. (Amended) The method of Claim 27, wherein said [etching] forming step [is performed] comprises etching with a mixture comprising CHF_3 and CF_4.--

REMARKS

Applicants' undersigned representative thanks Examiner Gurley for the helpful and courteous discussion held on April 26, 1999, and for indicating the allowability of Claim 27 as amended above and of Claim 35 outright. Applicants' undersigned representative has taken the opportunity to amend claims depending from Claim 27 for consistency. Applicants' undersigned representative also completes the record by submitting the executed Declaration under 37 CFR 1.131 of James E. Nulty herewith.

Therefore, the present claims are fully patentable and in condition for allowance. Applicants' undersigned representative earnestly solicits early notice to that effect.

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF

45

PM95012

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751 Group Art Unit: 2812

Filed: December 22, 1995 Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Assistant Commissioner for Patents
Washington, D.C. 20231

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DECLARATION UNDER 37 C.F.R. 1.131

I, **James E. Nulty**, hereby declare and state that:

1. I am an inventor of the above-identified patent application.

2. I have read and I understand (a) the above-identified patent application, (b) the Declaration Under 37 C.F.R. 1.132 dated July 25, 1998 and the references cited therein, (c) the Office Action dated September 22, 1998, (d) U.S. Patent No. 5,759,867 to Armacost et al. (hereinafter, "Armacost et al."), filed on April 21, 1995, and (e) the attached documentation in non-redacted form.

3. I understand that the above-identified application for patent claims, in one aspect:

a) a method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising:

I hereby certify that this correspondence is being ~~deposited with the United States Postal Service as first class mail in an envelope addressed~~ transmitted by facsimile to: Assistant Commissioner for Patents, Washington, D.C., 20231, on April 28, 1999.

[signature] 4/28/99
Signature Date

ADF 4/28/99

i) forming an etch stop layer over insulating spacers in the contact region, wherein the insulating spacers have a substantially rectangular profile; and subsequently

ii) anisotropically etching the structure having the insulating spacers and the etch stop layer in the contact region with an etchant having a selectivity for the etch stop layer relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop layer being different from the second insulating layer;

and, in a second aspect,

b) a method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

i) forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

ii) forming an etch stop layer over the spacer and the first and second electrically conductive regions;

iii) forming a blanket layer over the etch stop layer;

iv) selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region;

v) etching the etch stop layer to remove part of the etch stop layer formed over the first electrically conductive region, under conditions that etch (i) the material of the etch stop layer adjacent to the spacer and (ii) the spacer such that the substantially rectangular cross-sectional shape of the spacer

is maintained (hereinafter, paragraphs (a)(i)-(b)(v) are collectively referred to as "the presently claimed invention").

4. The attached documentation provides evidence of the conception and reduction to practice of at least one working embodiment of the presently claimed invention prior to April 21, 1995.

5. For example, a structure was made by an embodiment of the presently claimed invention prior to April 21, 1995 (see item 4a, "Construction of the Device," on the first page of the attached documentation).

6. The date on the micrograph of a structure made by an embodiment of the presently claimed invention is prior to April 21, 1995 (see "Method Comparison -- Invention" in the attached documentation).

7. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

8. Further Declarant saith not.

James E. Nulty

2/24/99
Date

ADF

INVENTION DISCLOSURE FORM Disclosure No.________

1. INVENTOR(S)

A. Name James E Nulty Empl. No. ████ Ext. No. ████

Home Mailing Address 1037 Lenor Wy San Jose CA 95128 Home No. ████

Citizenship USA

B. Name Christopher J. Petti Empl. No. ████ Ext. No. ████

Home Mailing Address 660 Sierra Ave Mountain View, CA 94041

Citizenship USA

C. Division, Dept. or Subsidiary ________

2. TITLE OF INVENTION Method for Elliminating lateral shoulder erosion on enclosed contact topographies during RF Sputter Cleaning

3. CONCEPTION OF INVENTION

a. Date of first drawing or drawings ________

Where can first drawing be found? ________

b. Date of first written description ________

Where is description found? ________

c. Date of first oral disclosure to others ________

To whom? ________

4. CONSTRUCTION OF DEVICE a.) Date Completed ████

b. Was prototype made? yes

c. By whom made? James Nulty

d. Where can the prototype be found? ████ IEM's on JEN Complete ████

5. TEST OF DEVICE a.) Date: ________ b.) Witness(s): ________

c. Results: ________

6. SALE a.) Was invention sold? or offered for sale. Yes ____ No ____ b.) Date of first sale ________

Inventor(s) [signature] Date ████

[signature] Date ████

Witness, Read, and Understood by:

████ Date ████

████ Date ████

(Each page upon which information is entered should be signed and witnessed.)

INVENTION DISCLOSURE FORM

7. USE a. Is invention presently being used? Yes X No ______.

b. Are there specific plans for its use in near future? yes

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS. ______

9. WAS INVENTION Conceived (Yes___ (No X___ During performance of
Constructed (Yes___ (No X___ Government contract?
Tested (Yes___ (No X___

a. Contract Number ______________________
(Give Full Contract Number)

This description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as reports of any nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the description of contruction and operation.

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
2. Describe old method(s), if any, of performing the function of the invention.
3. Indicate the disadvantages of the old method(s). What problem(s) is your invention trying to solve?
4. Describe the construction of your invention, showing the changes, additions and improvements over the old method.
5. Give details of the operation if not already described under 4.
6. State the advantages of your invention over what has been done before.
7. Indicate any alternate method of construction.

______________________ Date ______
Inventor

______________________ Date ______

Witness, Read, and Understood by:

______________________ Date ______

______________________ Date ______

(Each page upon which information is entered should be signed and witnessed.)

INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

9. Features which are believed to be new.

11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet.

Inventor — Date

Witness, Read, and Understood by: — Date

Date

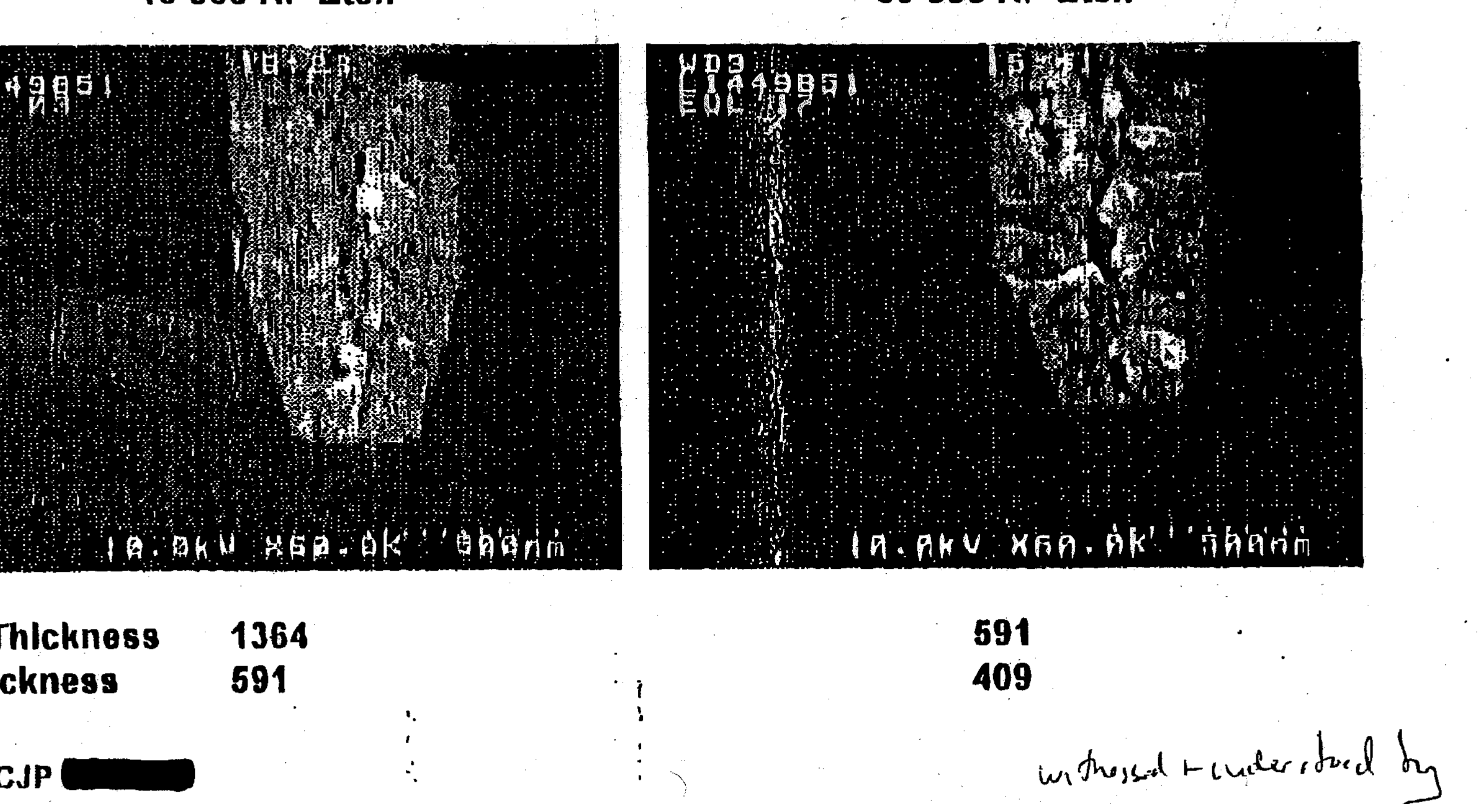
Date

(Each page upon which information is entered should be signed and witnessed.)

High Contact Resistance at LICM1E

Effect of RF Etch on Shoulder

Correlates to [redacted]



	10 sec RF Etch	30 sec RF Etch
Min Vertical Thickness	1364	591
Min Diag. Thickness	591	409

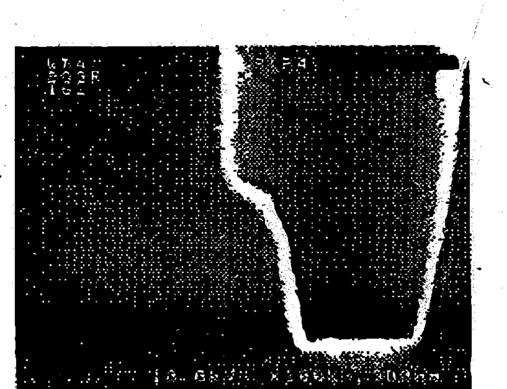
JEN/CJP [redacted]

witnessed + understood by [redacted]

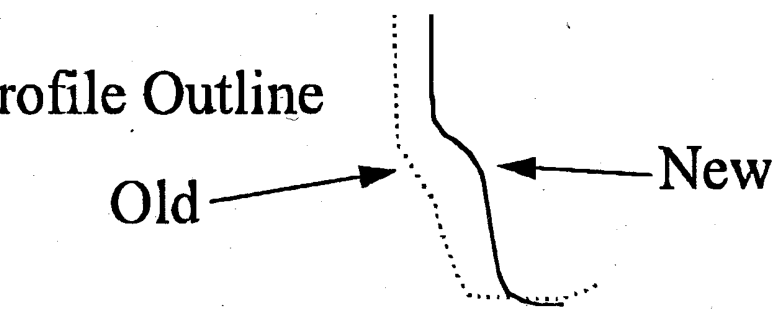
Method Comparison

Old

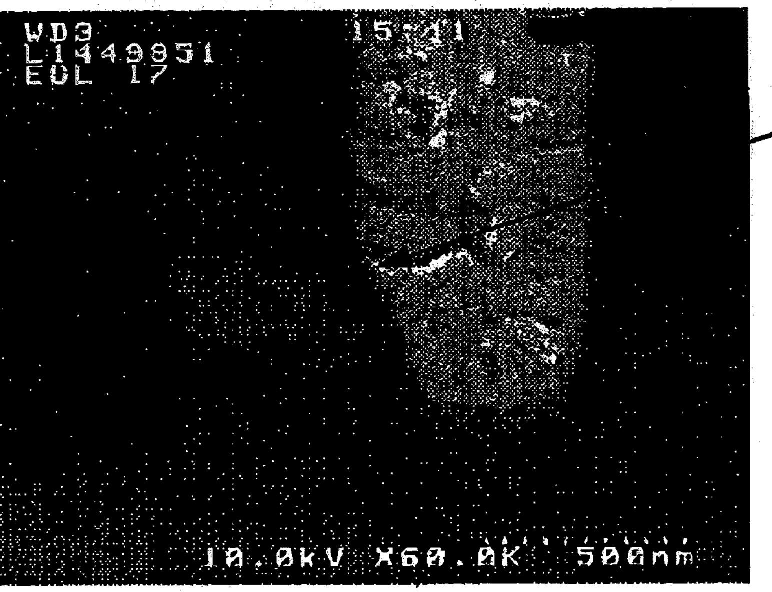
Invention



Profile Outline



Lateral Erosion Location



Direction of Lateral Erosion

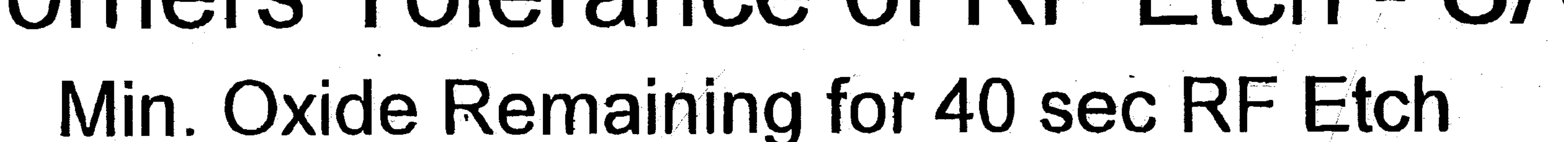
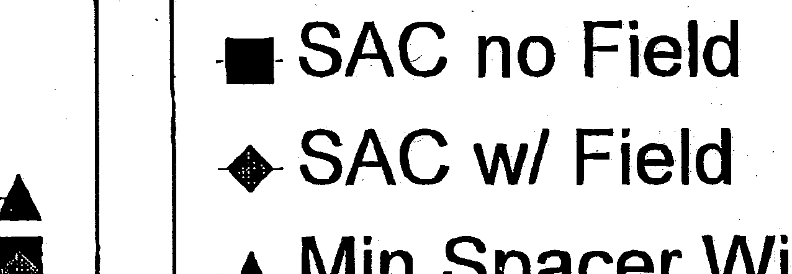
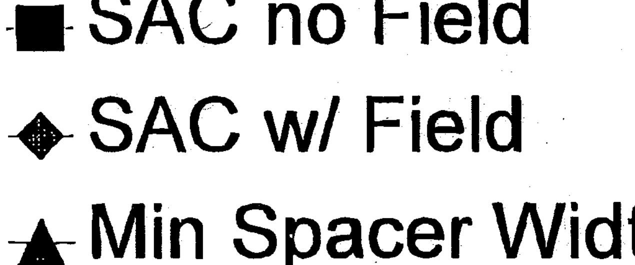
Invention Form Answers

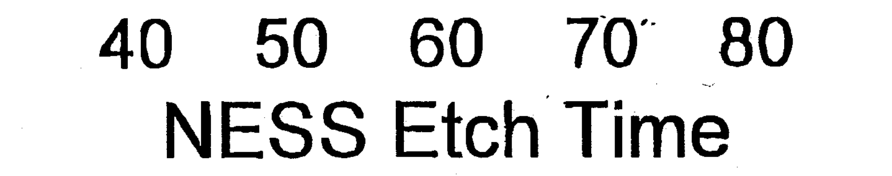
- Old Method - selective Nit:Ox etch, leaving rounded shoulder profile. Wet etch, completely removing nitride
- Diadvantage of old methods: Leave shoulder susceptible to lateral erosion during RF Sputter etch
- Advantages of Operation: Thicker minimum oxide following RF Etch, Easy process sustaining, only have to control vertical oxide thickness. Nitride on sidewall gives thicker insulator than just oxide spacer. Larger process window, higher reliability/yield.
- Alternate methods - Different RF Etch technique which does not erode sidewall shoulder. Alternate spacer material which is not eroded by RF Etch. Alternate spacer material which may be thin following RF Etch with no yield/rel issues.
- [redacted]
- New features - Spacer profile. Most advanced etch tools facet spacer shoulder, making them susceptible to RF Etch lateral erosion. Using high pressure, poor selective Nit:Ox etch gives best profile.
- Date first written - [redacted] Meeting Minutes.
- Date first orally disclosed - [redacted] Meeting
- Value is high; yield/rel improvement; manufacturing cost reduction due to less scrap material.

witnessed + understood by

Corners Tolerance of RF Etch - SA

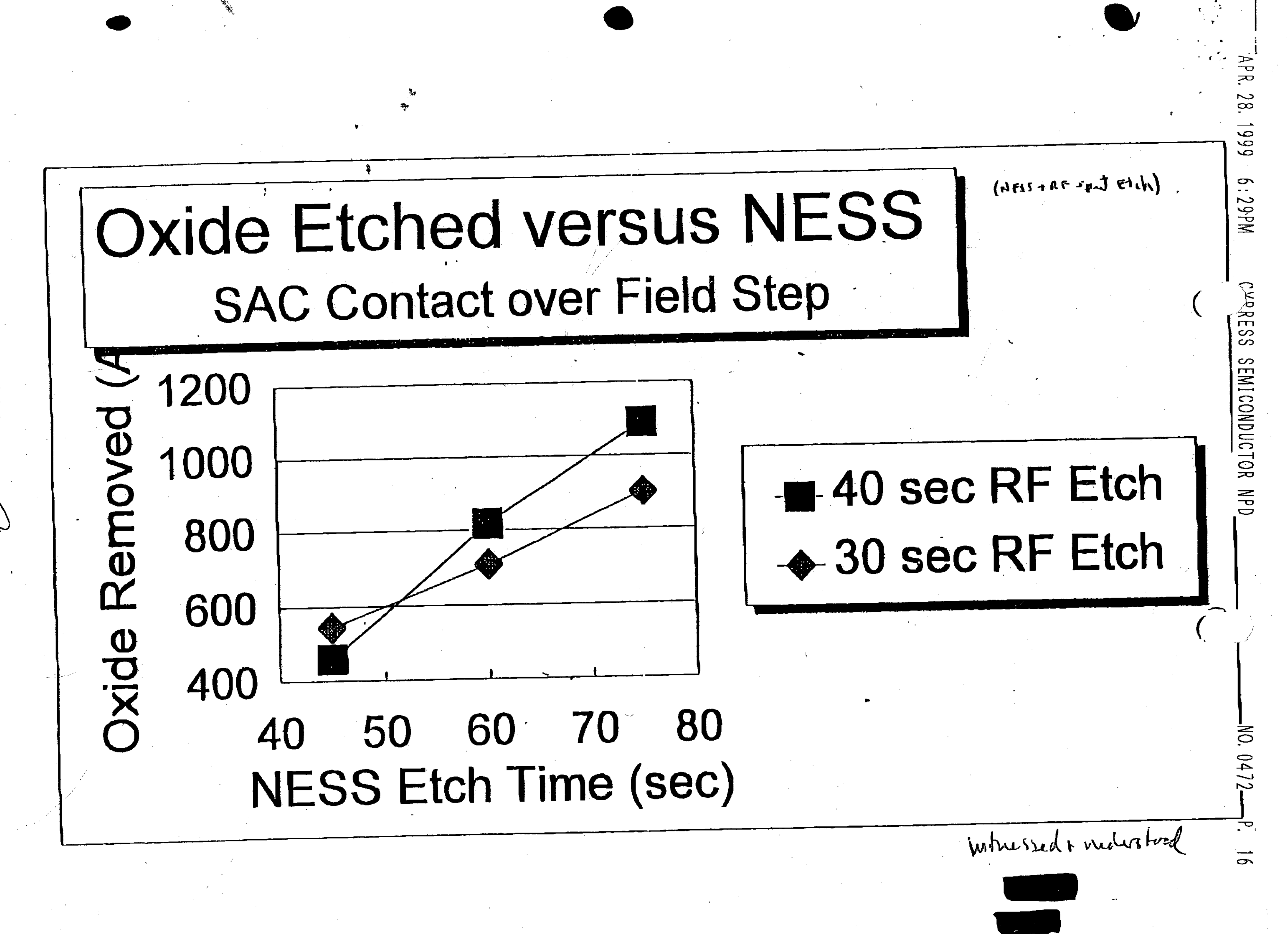
Min. Oxide Remaining for 40 sec RF Etch



Normalized for 1600 A NPOX @ Nit9

witnessed & understood


Oxide Etched versus NESS
SAC Contact over Field Step
(NESS + RF sput Etch)
Oxide Removed (A
1200
1000
800
600
400
40
50
60
70
80
NESS Etch Time (sec)
40 sec RF Etch
30 sec RF Etch
witnessed & understood

* * * COMMUNICATION RESULT REPORT (APR. 29. 1999 2:23PM) * * *

TTI CYPRESS SEMICONDUCTOR NPD

FILE MODE	OPTION	ADDRESS (GROUP)	RESULT	PAGE
0485 MEMORY TX		917033087722	OK	16/16

REASON FOR ERROR
E-1) HANG UP OR LINE FAIL
E-2) BUSY
E-3) NO ANSWER
E-4) NO FACSIMILE CONNECTION

CYPRESS SEMICONDUCTOR CORPORATION
FACSIMILE TRANSMISSION COVER SHEET

Re-fax

DATE: April 28, 1999

TO: Examiner Gurley
Group Art Unit 2812

FAX# (703) 308-7722

FROM: ANDREW D. FORTNEY, Ph.D., Esq.
CYPRESS SEMICONDUCTOR CORPORATION
FAX #: (408) 232-4447
PHONE: (408) 232-4437

PAGE 1 OF 16

* * * COMMUNICATION RESULT REPORT (APR. 28. 1999 6:29PM) * * *

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0472 MEMORY TX		917033087722	OK	16/16

Copy David Graham

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E-2) BUSY
E-4) NO FACSIMILE CONNECTION

CYPRESS SEMICONDUCTOR CORPORATION
FACSIMILE TRANSMISSION COVER SHEET

DATE April 28, 1999

TO: EXAMINER GURLEY
GROUP ART UNIT 2812

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FROM: ANDREW D. FORTNEY, Ph.D., Esq.
CYPRESS SEMICONDUCTOR CORPORATION
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PHONE: (408) 232-4437

PAGE 1 OF 16

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08/577,751	12/22/95	NULTY	J	16820.P097

MM42/0719

DAVID R. GRAHAM, ESQ.
1337 CHEWPON AVE.
MILPITAS CA 95035

EXAMINER	
GURLEY, L	
ART UNIT	PAPER NUMBER
2812	29

DATE MAILED: 07/19/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

# Office Action Summary	Application No. 08/577,751	Applicant(s) Nulty et al.
	Examiner Lynne Gurley	Group Art Unit 2812

☒ Responsive to communication(s) filed on *Apr 28, 1999*.

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *2, 3, 5-7, 9, 13-18, 20, and 27-41* is/are pending in the application.

Of the above, claim(s) ______ is/are withdrawn from consideration.

☐ Claim(s) ______ is/are allowed.

☒ Claim(s) *2, 3, 5-7, 9, 13-18, 20, and 27-41* is/are rejected.

☐ Claim(s) ______ is/are objected to.

☐ Claims ______ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on ______ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on ______ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) ______.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: ______.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). ______

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

2. The rejection of claims 27 and 35 under 35 U.S.C. 102(b) as being clearly anticipated by Mele et al. (5,037,777, dated 8/6/91) has been maintained for the reasons of record.

Mele shows the method as claimed, in Figs. 4B-5C, as a method of forming a contact opening in a structure comprising substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising: etching a conformal second insulating layer overlying the at least two devices and the contact region under conditions providing insulating spacers in the contact region such that the insulating spacers have a substantially rectangular profile; and subsequently anisotropically etching the structure having the insulating spacers in the contact region with an

etchant having a selectivity for an etch stop material relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop material being distinct from the second insulating layer (claims 27 and 35).

3. The rejectionof claims 35-37 under 35 U.S.C. 102(e) as being clearly anticipated by Armacost et al. (5,759,867, dated 6/2/98, filed 4/21/95) has been maintained for the reasons of record.

Armacost shows the method as claimed, in Figs. 1-3, as a method of forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface; forming an etch stop layer over the spacer and the first and second electrically conductive regions; forming a blanket layer over the etch stop layer; selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region; etching the etch stop layer to remove a second part of the etch stop layer that is formed over the first electrically conductive region, wherein the step of etching the etch stop layer is performed under conditions that etch the material of the etch stop layer adjacent to the spacer and the spacer such that the substantially rectangular cross-sectional shape of the spacer is maintained.

SAMSUNG-1008.274

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The rejection of claims 2-3, 5-7, 9, 13-18, 20 and 28-34 under 35 U.S.C. 103(a) as being unpatentable over Mele et al. (5,037,777, dated 8/6/91) has been maintained for the reasons of record.

Mele shows the method substantially as claimed and as described in the preceding paragraph.

Mele lacks anticipation only in not teaching the particulars of the etching system such as plasma, low bombardment/high neutral flux, low selectivity for the etch stop in comparison to the insulating layer, the specific type of etching apparatus, the pressure, flow rates and power parameters, and a cleaning sputter etch for cleaning the insulating layer after etching the etch stop.

It would have been obvious to one of ordinary skill in the art to have varied the etching parameters and to have used a plasma for the anisotropic etch in Mele and to have cleaned the insulating layer with a sputter etch after etching the etch stop such as would be done by routine experimentation to obtain the desired contact.

6. The rejection of claims 38-41 under 35 U.S.C. 103(a) as being unpatentable over Armacost et al. (5,759,867, dated 6/2/98, filed 4/21/95) has been maintained for the reasons of record.

Armacost shows the method substantially as claimed and as described in the preceding paragraphs.

Armacost lacks anticipation only in not teaching the particulars of the etching system such as plasma, low bombardment/high neutral flux, low selectivity for the etch stop in comparison to the insulating layer, the specific type of etching apparatus, the pressure, flow rates and power parameters, and a cleaning sputter etch for cleaning the insulating layer after etching the etch stop.

It would have been obvious to one of ordinary skill in the art to have varied the etching parameters and to have used a plasma for the anisotropic etch in Armacost and to have cleaned the insulating layer with a sputter etch after etching the etch stop such as would be done by routine experimentation to obtain the desired contact.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is (703) 305-3474. The examiner can normally be reached on Monday-Friday from 9:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F. Niebling, can be reached on (703) 308-3325. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

lg

July 16, 1999

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800

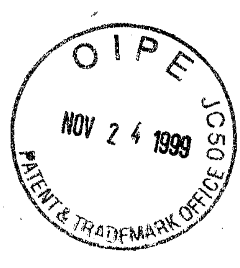
GP 2812 AF $

November 19, 1999

Corres. and Mail
BOX AF

Assistant Commissioner for Patents
Washington, D.C. 20231

VIA FIRST CLASS MAIL



Applicant(s): James E. Nulty et al.
Serial No.: 08/577,751
Filing Date: December 22, 1995
For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING
Attorney Docket No.: CYP-002/PM95012

Dear Sir:

Enclosed are the following items for filing in connection with the above-identified application:

Response After Final Rejection; Petition for Extension of Time; Filing Receipt; Copy of Amendment Filed February 22, 1999; Copy of Response Filed April 28, 1999; Copy of Declaration of James Nulty dated 2/24/99 (with Exhibits); Copy of Facsimile Transmission Report; Check No. 954 for $110.00

Please direct all communications to Applicant's undersigned representative.

RECEIVED
NOV 29 1999
TC 2800 MAIL ROOM

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on November 19, 1999.

Andrew D. Fortney, Ph.D. 11/19/99
Date

3901 NORTH FIRST STREET SAN JOSE, CA 95134-1599 408•943•2600

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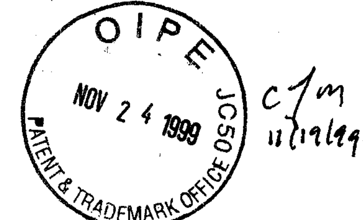

Atty. Ref. No. CYP-002/PM95012

c/m 11/19/99

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: James E. NULTY et al.

Serial No.: 08/577,751 Group Art Unit: 2812

Filed: December 22, 1995 Examiner: GURLEY

#30/EXT 12-10-99 JProctor

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Assistant Commissioner for Patents
Washington, D.C. 20231

PETITION FOR EXTENSION OF TIME TO RESPOND TO OUTSTANDING PATENT OFFICE ACTION (37 CFR 1.136(a))

Sir:

This is a petition for an extension of time for filing a Response to the Office Action dated July 19, 1999. The communication in connection with the matter for which this extension is requested is filed herewith.

	Total Months Requested	Fee
X	one month	$110.00
	two months	$380.00
	three months	$870.00
	four months	$1,360.00

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[X] A check in the total amount of $110.00 to cover the extension fee is attached.

11/29/1999 DVUONG 00000012 08577751
01 FC:115 110.00 OP

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600
CYPRESS SEMICONDUCTOR CORPORATION
3939 N. First Street
San Jose, California 95134

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on **November 19, 1999**.

Andrew D. Fortney, Ph.D. 11/19/99 Date

CYP-002/PM95012

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 2812

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OIPE NOV 2 4 1999 JC50 PATENT & TRADEMARK OFFICE

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751 — Group Art Unit: 2812

Filed: December 22, 1995 — Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

RECEIVED NOV 29 1999 TC 2800 MAIL ROOM

Assistant Commissioner for Patents
Washington, D.C. 20231

RESPONSE AFTER FINAL REJECTION

Responsive to the final Office Action dated July 19, 1999, entry and consideration of the following remarks are respectfully requested.

REMARKS

The Office Action dated July 19, 1999 fails to address (1) the merits of the Amendment filed February 22, 1999, in the above-identified application, (2) the executed Declaration under 37 C.F.R. 1.131 of James E. Nulty filed April 28, 1999, in the above-identified application, and (3) the discussion between Examiner Gurley and Applicants' undersigned representative held on April 26, 1999, in which Examiner Gurley indicated the allowability of Claim 27 as amended on February 22, 1999, and the allowability of Claim 35 outright. Applicants' undersigned

---

I hereby certify that this correspondence is being transmitted by first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on **November 19, 1999**.

Signature — 11/19/99 — Date

representative includes courtesy copies of all correspondence filed on those dates for the Examiner's convenience. However, Applicants make the following remarks to ensure completeness of the record.

The present claims concern, in one aspect,

a) a method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising the steps of:

   i) forming an etch stop layer over insulating spacers in the contact region, wherein the insulating spacers have a substantially rectangular profile; and subsequently

   ii) anisotropically etching the structure having the insulating spacers and the etch stop layer in the contact region with an etchant having a selectivity for the etch stop material relative to the insulating spacers sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop material being different from the insulating spacers (see Claim 27 and claims depending therefrom),

and in a second aspect,

b) a method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a

region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

i) forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

ii) forming an etch stop layer over the spacer and the first and second electrically conductive regions;

iii) forming a blanket layer over the etch stop layer;

iv) selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region; and

v) etching the etch stop layer to remove a second part of the etch stop layer formed over the first electrically conductive region, wherein the step of etching the etch stop layer is performed under conditions that etch (i) the spacer and (ii) the material of the etch stop layer adjacent to the spacer such that the substantially rectangular cross-sectional shape of the spacer is maintained (Claim 35 and claims depending therefrom; hereinafter, paragraphs (a)(i)-(b)(v) are collectively referred to as "the presently claimed invention").

As explained in the Amendment filed February 22, 1999, the rejections of Claims 35-37 under 35 U.S.C. 102(e) and of Claims 38-41 under 35 U.S.C. 103(a) as being anticipated by or

unpatentable over Armacost et al. has been obviated by the executed Declaration under 37 C.F.R. 1.131 of James E. Nulty filed April 28, 1999, establishing a date of the reduction of practice for the presently claimed invention prior to the effective filing date of Armacost et al. (see the attached copy of said Declaration). Therefore, these grounds of rejection are unsustainable, and should be withdrawn.

As also explained in the Amendment filed February 22, 1999, the rejections of Claims 27 and 35 under 35 U.S.C. 102(b) and of Claims 2-3, 5-7, 9, 13-18, 20 and 28-34 under 35 U.S.C. 103(a) as being anticipated by or unpatentable over Mele et al. is traversed.

Mele et al. form a first dielectric layer 44 over only the conductive layer/region 42. Therefore, dielectric layer 44 cannot form an etch stop layer over spacers 56 or 60 (see pages 5-6 of the Amendment filed February 22, 1999), and Mele et al. cannot anticipate either Claim 27 or Claim 35.

Similarly, since Mele et al. are silent with regard to forming an etch stop layer over insulating spacers, Mele et al. can neither disclose nor suggest etching both (1) substantially rectangular insulating spacers and (2) an etch stop layer over the insulating spacers with an etchant having a selectivity sufficiently low to maintain the substantially rectangular shape of the insulating spacers (see the second step of Claim 27 and the fifth step of Claim 35). Consequently, Mele et al. cannot render the present Claims 2-3, 5-7, 9, 13-18, 20 and 28-34 obvious.

Therefore, the present claims are fully patentable and in condition for allowance. Applicants' undersigned representative earnestly solicits early notice to that effect.

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF

February 22, 1999

Assistant Commissioner for Patents
Washington, D.C. 20231

VIA FIRST CLASS MAIL

Applicant(s): James E. Nulty et al.
Serial No.: 08/577,751
Filing Date: December 22, 1995
For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING
Attorney Docket No.: PM95012

Dear Sir:

Enclosed are the following items for filing in connection with the above-identified application:

Amendment; Petition for Extension of Time; Decalarartion (with attachment); Check Nos. 225906, 228118 and 228119 for $150.00, $150.00 and $110.00

Please direct all communications to Applicant's undersigned representative.

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on Feb. 22, 1999.

Andrew D. Fortney, Ph.D. — Date 2/22/99

3901 NORTH FIRST STREET SAN JOSE, CA 95134-1599 408•943•2600

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Atty. Ref. No. PM95012

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: James E. NULTY et al.

Serial No.: 08/577,751 Group Art Unit: 2812

Filed: December 22, 1995 Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Assistant Commissioner for Patents
Washington, D.C. 20231

PETITION FOR EXTENSION OF TIME TO RESPOND TO OUTSTANDING PATENT OFFICE ACTION (37 CFR 1.136(a))

Sir:

This is a petition for an extension of time for filing a Response to the Office Action dated September 22, 1998. The communication in connection with the matter for which this extension is requested is filed herewith.

	Total Months Requested	Fee
	one month	$110.00
X	two months	$400.00
	three months	$950.00
	four months	$1,510.00

[X] Three checks in the total amount of $410.00 to cover the extension fee are attached.

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600
CYPRESS SEMICONDUCTOR CORPORATION
3939 N. First Street
San Jose, California 95134

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on Feb. 22, 1999.

Andrew D. Fortney, Ph.D. 2/22/99
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751

Group Art Unit: 2812

Filed: December 22, 1995

Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

Responsive to the Office Action dated September 22, 1998, in the above-identified application, entry and consideration of the following amendments and remarks are respectfully requested.

IN THE CLAIMS

Please amend the remaining claims as follows:

--27. (Amended) A method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of said devices comprising a conductive layer disposed over said substrate and a first insulating layer on said conductive layer, and at least two of said devices being interspaced by a contact region, said method comprising:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C., 20231, on Feb. 22, 1999.

Signature: [signature] Date: 2/22/99

[etching a conformal second insulating layer overlying said at least two devices and said contact region under conditions providing] forming an etch stop layer over insulating spacers in said contact region, wherein [such that] said insulating spacers have a substantially rectangular profile; and subsequently

anisotropically etching said structure having said insulating spacers and said etch stop layer in said contact region with an etchant having a selectivity for [an] said etch stop [material] layer relative to said second insulating layer sufficiently low to retain said substantially rectangular profile of said insulating spacers, said etch stop [material] layer being [distinct] different from said second insulating layer.-- said etch stop layer being removed from a base of said contact while being retained on said insulating spacer.

--32. (Amended) The method of Claim 27, [further comprising, after said etching step and before said anisotropically etching step, depositing an] wherein said etch stop layer is formed over the entirety of said structure having said insulating spacers in said contact region.--

--35. (Amended) A method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

forming an etch stop layer over the spacer and the first and second electrically conductive regions;

forming a blanket layer over the etch stop layer;

SAMSUNG-1008.288

selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region; and

etching the etch stop layer to remove a second part of the etch stop layer that is formed over the first electrically conductive region, wherein the step of etching the etch stop layer is performed under conditions that etch (i) the spacer and (ii) the material of the etch stop layer adjacent to the spacer [and the spacer] such that the substantially rectangular cross-sectional shape of the spacer is maintained.--

REMARKS

Claims 2, 3, 5-7, 9, 13-18, 20 and 27-41 remain active in the present application.

The present claims concern, in one aspect, a method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising:

(a) forming an etch stop layer over insulating spacers in the contact region, wherein the insulating spacers have a substantially rectangular profile; and subsequently

(b) anisotropically etching the structure having the insulating spacers and the etch stop layer in the contact region with an etchant having a selectivity for the etch stop layer relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop layer being different from the second insulating layer (Claim 27 and claims depending therefrom);

and in a second aspect, a method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a

region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

i) forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

ii) forming an etch stop layer over the spacer and the first and second electrically conductive regions;

iii) forming a blanket layer over the etch stop layer;

iv) selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region;

v) etching the etch stop layer to remove part of the etch stop layer formed over the first electrically conductive region, under conditions that etch (i) the material of the etch stop layer adjacent to the spacer and (ii) the spacer such that the substantially rectangular cross-sectional shape of the spacer is maintained (Claim 35 and claims depending therefrom; hereinafter, collectively referred to as "the presently claimed invention").

Applicants and their undersigned representative thank Examiner Gurley for the helpful and courteous discussions held from September 2, 1998,through September 4, 1998, and for withdrawing the previous grounds of rejection. The new grounds of rejection are traversed in part

by the present amendment and remarks and obviated in part by the accompanying Declaration under 37 C.F.R. 1.131 (the executed copy of which will be filed at the earliest opportunity).

MELE ET AL DOES NOT ANTICIPATE THE PRESENTLY CLAIMED INVENTION.

Mele et al. discloses a method for forming a multilayer semiconductor using selective planarization. Mele et al. disclose forming spacers 56 from insulating layer 48 (see col. 4, ll. 26-36; col. 5, ll. 3-6; and Figs. 3B, 3C, and 4A-4C). Alternatively, Mele et al. form spacers 60 from an unseen insulating layer (perhaps similar to insulating layer 48; see col. 5, l. 67 through col. 6, l. 1 and Fig. 5A). In the embodiment(s) shown in Figs. 3A-4D, after forming the spacers, Mele et al. do not form anything other than contact 59 in the space 58 between conductive members 42 (see col. 5, ll. 7-10, 29-31 and 50-54).

However, in the embodiment shown in Figs. 5A-5C, Mele et al. deposit a second insulating layer 52 after forming spacers 60 (see col. 6, ll. 1-3). This second insulating layer 52 is then etched, during which spacers 60 and dielectric layer 44 may also be etched (col. 6, ll. 5-12). Mele et al. disclose that the amount of etching of these materials can be controlled through proper material selection and etch chemistry (col. 6, ll. 12-14), thereby hinting that spacers 60 and dielectric layer 44 could effectively function as an etch stop for second insulating layer 52.

The alternative process shown by Mele et al. in Fig. 5A-5C does not anticipate the claimed invention. For example, Mele et al. clearly form the dielectric layer 44 over only conductive layer/region 42. Therefore, dielectric layer 44 cannot form an etch stop layer over the spacer and the first and second electrically conductive regions as recited in the second step of

Claim 35. Needless to say, spacer 60 does not form an etch stop layer over itself and the first and second electrically conductive regions. Consequently, Mele et al. do not anticipate Claim 35.

Claim 27 affirmatively recites that the etch stop layer is different from the spacer. Therefore, the spacer of Mele et al. cannot serve as the etch stop layer of Claim 27. Further, similar to Claim 35, dielectric layer 44, formed over only conductive layer/region 42, cannot form an etch stop layer over the spacer as recited in the first step of Claim 27.

Therefore, the presently claimed invention is not anticipated by Mele et al.

THE PRESENTLY CLAIMED INVENTION IS NOT OBVIOUS IN VIEW OF MELE ET AL.

The discussion above is incorporated herein in support of the patentability of the presently claimed invention.

As discussed above, Mele et al. are silent with regard to an etch stop layer over the spacer. Consequently, Mele et al. cannot disclose or suggest etching insulating spacers and an etch stop layer with an etchant having a selectivity sufficiently low to retain the substantially rectangular profile of the insulating spacers (see the second step of Claim 27 and the fifth step of Claim 35).

Therefore, the presently claimed invention is fully patentable over Mele et al.

THE PRESENTLY CLAIMED INVENTION IS NEITHER ANTICIPATED BY NOR OBVIOUS IN VIEW OF ARMACOST ET AL.

The application corresponding to Armacost et al. was filed on April 21, 1995. However, the documentation attached to the accompanying Declaration includes evidence that the presently

claimed invention was reduced to practice prior to April 21, 1995 (see paragraph 4 of the accompanying Declaration).

For example, a structure was made by an embodiment of the presently claimed invention prior to April 21, 1995 (see paragraph 5 of the accompanying Declaration and item 4a, "Construction of the Device," on the first page of the documentation attached to the accompanying Declaration). Furthermore, the date on the micrograph of a structure made by an embodiment of the presently claimed invention is prior to April 21, 1995 (see paragraph 6 of the accompanying Declaration and "Method Comparison -- Invention" in the documentation attached to the accompanying Declaration).

Therefore, the presently claimed invention was conceived and reduced to practice before the filing date of the application corresponding to Armacost et al. Consequently, Armacost et al. is not available as a reference against the presently claimed invention.

CONCLUSION

The new grounds of rejection, being traversed or overcome, are unsustainable, and should be withdrawn. As a result, the present claims are fully patentable over the cited references. Therefore, the present application is in condition for allowance. Early notice to that effect is earnestly solicited.

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF

April 28, 1999

Assistant Commissioner for Patents
Washington, D.C. 20231

VIA FACSIMILE

Applicant(s): James E. NULTY et al.
Serial No.: 08/577,751
Filing Date: December 22, 1995
Group Art Unit: 2812
Examiner: GURLEY, L.
For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING
Attorney Docket No.: CYP-002/PM95012C

Dear Sir:

Enclosed are the following items for filing in connection with the above-identified application:

AMENDMENT
EXECUTED DECLARATION UNDER 37 C.F.R. 1.131

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF

I hereby certify that this correspondence is being transmitted by facsimile to: Assistant Commissioner for Patents, Washington, D.C., 20231, on **April 28, 1999**.

Andrew D. Fortney, Ph.D. 4/28/99
Date

3901 NORTH FIRST STREET SAN JOSE, CA 95134-1599 408•943•2600

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751 | Group Art Unit: 2812

Filed: December 22, 1995 | Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

Further to the Amendment filed February 22, 1999, in the above-identified application, and further to the discussion between Examiner Gurley and Applicants' undersigned representative, entry and consideration of the following amendments and remarks are respectfully requested.

IN THE CLAIMS

Please amend the claims as follows:

Claim 27, lines 11 and 13, change "second insulating layer" to --insulating spacers--.

--28. (Amended) The method of Claim 27, [wherein said] <u>further comprising forming said insulating spacers under</u> conditions <u>that</u> include a bias sufficiently low and a pressure

---

I hereby certify that this correspondence is being transmitted by facsimile to: Assistant Commissioner for Patents, Washington, D.C., 20231, on **<u>April 28, 1999</u>**.

[signature] 4/28/99
Signature Date

sufficiently high to provide said insulating spacers in said contact region having said substantially rectangular profile.--

--30. (Amended) The method of Claim 27, wherein said [etching] forming step [is performed] comprises etching with a mixture comprising CHF_3 and CF_4.--

REMARKS

Applicants' undersigned representative thanks Examiner Gurley for the helpful and courteous discussion held on April 26, 1999, and for indicating the allowability of Claim 27 as amended above and of Claim 35 outright. Applicants' undersigned representative has taken the opportunity to amend claims depending from Claim 27 for consistency. Applicants' undersigned representative also completes the record by submitting the executed Declaration under 37 CFR 1.131 of James E. Nulty herewith.

Therefore, the present claims are fully patentable and in condition for allowance. Applicants' undersigned representative earnestly solicits early notice to that effect.

Respectfully submitted,

Andrew D. Fortney, Ph.D., Esq.
Registration No. 34,600

ADF

PM95012

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

James E. NULTY et al.

Serial No.: 08/577,751 — Group Art Unit: 2812

Filed: December 22, 1995 — Examiner: GURLEY

For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Assistant Commissioner for Patents
Washington, D.C. 20231

DECLARATION UNDER 37 C.F.R. 1.131

I, **James E. Nulty**, hereby declare and state that:

1. I am an inventor of the above-identified patent application.

2. I have read and I understand (a) the above-identified patent application, (b) the Declaration Under 37 C.F.R. 1.132 dated July 25, 1998 and the references cited therein, (c) the Office Action dated September 22, 1998, (d) U.S. Patent No. 5,759,867 to Armacost et al. (hereinafter, "Armacost et al."), filed on April 21, 1995, and (e) the attached documentation in non-redacted form.

3. I understand that the above-identified application for patent claims, in one aspect:

a) a method of forming a contact opening in a structure comprising a substrate and a plurality of devices thereon, each of the devices comprising a conductive layer disposed over the substrate and a first insulating layer on the conductive layer, and at least two of the devices being interspaced by a contact region, the method comprising:

I hereby certify that this correspondence is being ~~deposited with the United States Postal Service as first class mail in an envelope addressed~~ transmitted by facsimile to: Assistant Commissioner for Patents, Washington, D.C., 20231, on April 28, 1999.

[signature] 4/28/99
Signature — Date

ADF 4/28/99

i) forming an etch stop layer over insulating spacers in the contact region, wherein the insulating spacers have a substantially rectangular profile; and subsequently

ii) anisotropically etching the structure having the insulating spacers and the etch stop layer in the contact region with an etchant having a selectivity for the etch stop layer relative to the second insulating layer sufficiently low to retain the substantially rectangular profile of the insulating spacers, the etch stop layer being different from the second insulating layer;

and, in a second aspect,

b) a method for forming a contact opening to a first electrically conductive material formed in and/or on a surface of a substrate, the contact opening being formed in a region adjacent to a second electrically conductive material formed on the substrate, comprising the steps of:

i) forming an electrically insulative spacer adjacent to the second electrically conductive material, the spacer having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface;

ii) forming an etch stop layer over the spacer and the first and second electrically conductive regions;

iii) forming a blanket layer over the etch stop layer;

iv) selectively etching the blanket layer to form an opening to a first part of the etch stop layer that is formed over the first electrically conductive region;

v) etching the etch stop layer to remove part of the etch stop layer formed over the first electrically conductive region, under conditions that etch (i) the material of the etch stop layer adjacent to the spacer and (ii) the spacer such that the substantially rectangular cross-sectional shape of the spacer

is maintained (hereinafter, paragraphs (a)(i)-(b)(v) are collectively referred to as "the presently claimed invention").

4. The attached documentation provides evidence of the conception and reduction to practice of at least one working embodiment of the presently claimed invention prior to April 21, 1995.

5. For example, a structure was made by an embodiment of the presently claimed invention prior to April 21, 1995 (see item 4a, "Construction of the Device," on the first page of the attached documentation).

6. The date on the micrograph of a structure made by an embodiment of the presently claimed invention is prior to April 21, 1995 (see "Method Comparison -- Invention" in the attached documentation).

7. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

8. Further Declarant saith not.

James E. Nulty

2/24/99
Date

ADF

INVENTION DISCLOSURE FORM Disclosure No.________

1. INVENTOR(S)

A. Name James E Nulty Empl. No. [redacted] Ext. No. [redacted]

Home Mailing Address 1037 Lenor Wy San Jose CA 95128 Home No [redacted]

Citizenship USA

B. Name Christopher J. Petti Empl. No. [redacted] Ext. No. [redacted]

Home Mailing Address 660 Sierra Ave Mountain View, CA 94041

Citizenship USA

C. Division, Dept. or Subsidiary ________

2. TITLE OF INVENTION Method for Elliminating lateral shoulder erosion on enclosed contact topographies during RF Sputter Cleaning

3. CONCEPTION OF INVENTION

a. Date of first drawing or drawings ________

Where can first drawing be found? ________

b. Date of first written description ________

Where is description found? ________

c. Date of first oral disclosure to others ________

To whom? ________

4. CONSTRUCTION OF DEVICE a.) Date Completed [redacted]

b. Was prototype made? yes

c. By whom made? James Nulty

d. Where can the prototype be found? [redacted] SEM's on JEN Computer [redacted]

5. TEST OF DEVICE a.) Date:________ b.) Witness(s):________

c. Results:________

6. SALE a.) Was invention sold or offered for sale? Yes____ No____ b.) Date of first sale________

Inventor(s) [signature] Date [redacted]

[signature] Date [redacted]

Witness, Read, and Understood by:

[redacted] Date [redacted]

[redacted] Date [redacted]

(Each page upon which information is entered should be signed and witnessed.)

INVENTION DISCLOSURE FORM

7. USE a. Is invention presently being used? Yes X No ______.

b. Are there specific plans for its use in near future? yes

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS. ______

9. WAS INVENTION Conceived (Yes ____ (No X During performance of
Constructed (Yes ____ (No X Government contract?
Tested (Yes ____ (No X

a. Contract Number ______
(Give Full Contract Number)

This description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as reports of any nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the description of contruction and operation.

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.

2. Describe old method(s), if any,of performing the function of the invention.

3. Indicate the disadvantages of the old method(s). What problem(s) is your invention trying to solve?

4. Describe the construction of your invention, showing the changes, additions and improvements over the old method.

5. Give details of the operation if not already described under 4.

6. State the advantages of your invention over what has been done before.

7. Indicate any alternate method of construction.

______ Date ______
Inventor

______ Date ______

Witness, Read, and Understood by:

______ Date ______

______ Date ______

(Each page upon which information is entered should be signed and witnessed.)

INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

9. Features which are believed to be new.

11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet.

Inventor — Date

Witness, Read, and Understood by: — Date

Date

Date

(Each page upon which information is entered should be signed and witnessed.)

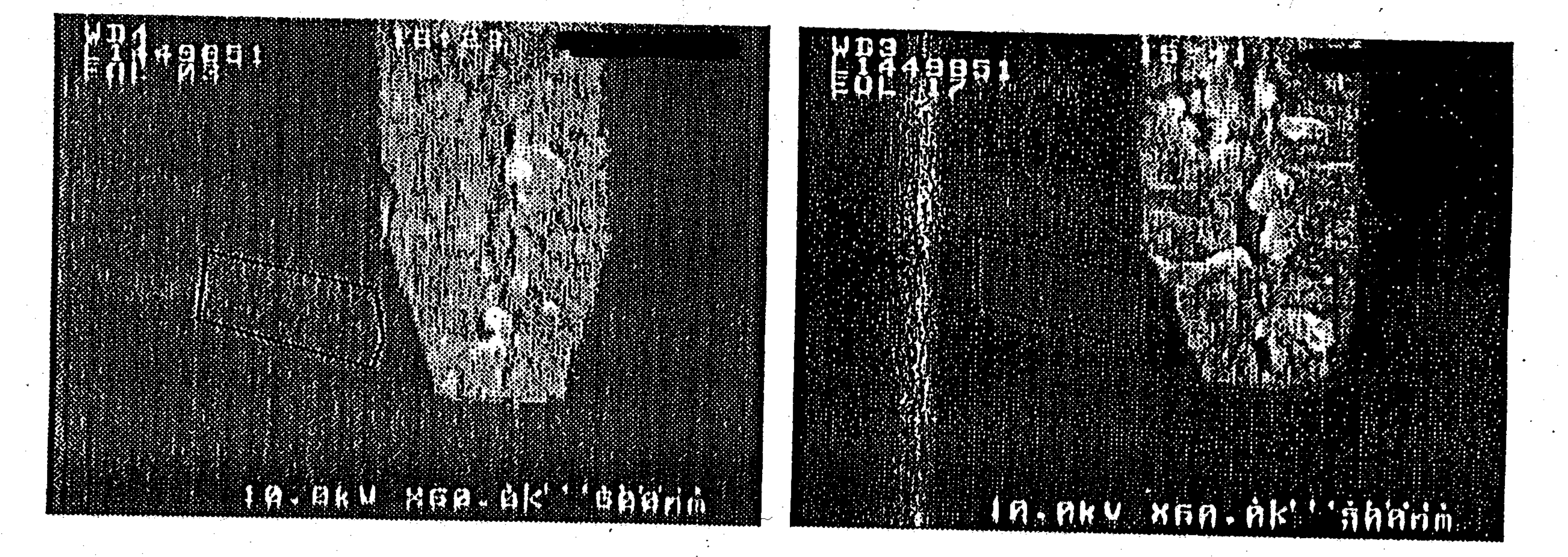
High Contact Resistance at LICM1E

Effect of RF Etch on Shoulder

Correlates to [redacted]

10 sec RF Etch

~30 sec RF Etch



	10 sec RF Etch	~30 sec RF Etch
Min Vertical Thickness	1364	591
Min Diag. Thickness	591	409

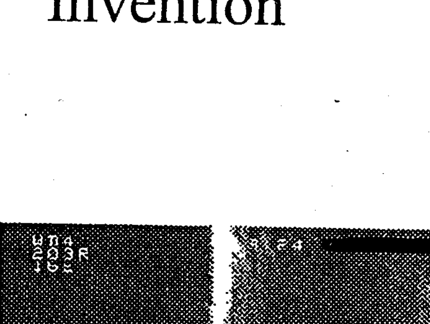
JEN/CJP [redacted]

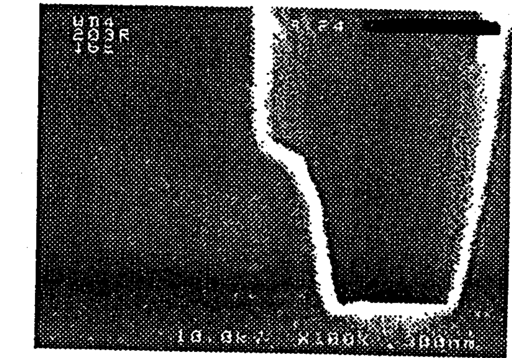
witnessed + understood by

Method Comparison

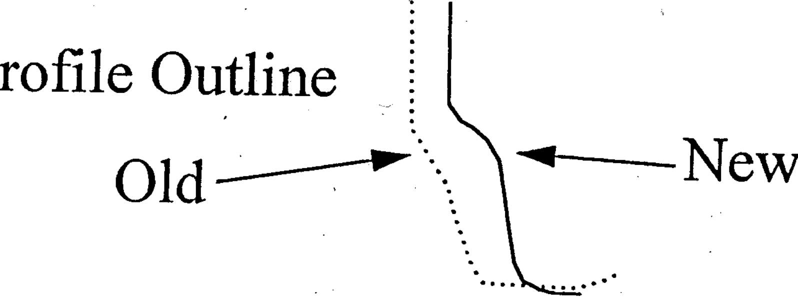
Old

Invention



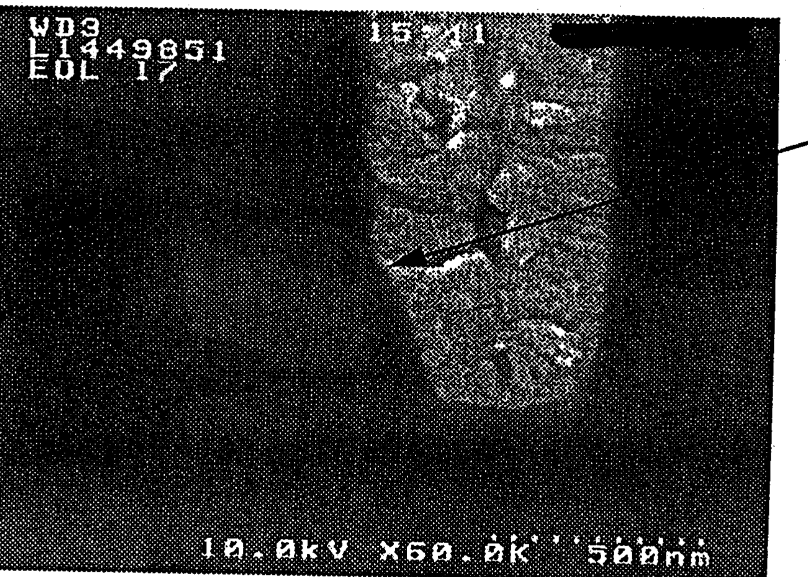


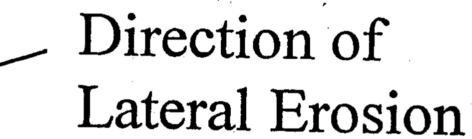
Profile Outline



witnessed & understood by

Lateral Erosion Location





Invention Form Answers

- Old Method - selective Nit:Ox etch, leaving rounded shoulder profile. Wet etch, completely removing nitride
- Diadvantage of old methods: Leave shoulder susceptible to lateral erosion during RF Sputter etch
- Advantages of Operation: Thicker minimum oxide following RF Etch, Easy process sustaining, only have to control vertical oxide thickness. Nitride on sidewall gives thicker insulator than just oxide spacer. Larger process window; higher reliability/yield.
- Alternate methods - Different RF Etch technique which does not erode sidewall shoulder. Alternate spacer material which is not eroded by RF Etch. Alternate spacer material which may be thin following RF Etch with no yield/rel issues.
- [illegible]
- New features - Spacer profile. Most advanced etch tools facet spacer shoulder, making them susceptible to RF Etch lateral erosion. Using high pressure, poor selective Nit:Ox etch gives best profile.
- Date first written - [illegible] Meeting Minutes.
- Date first orally disclosed - [illegible] Meeting
- Value is high; yield/rel improvement; manufacturing cost reduction due to less scrap material.

witnessed + understood by

[illegible]

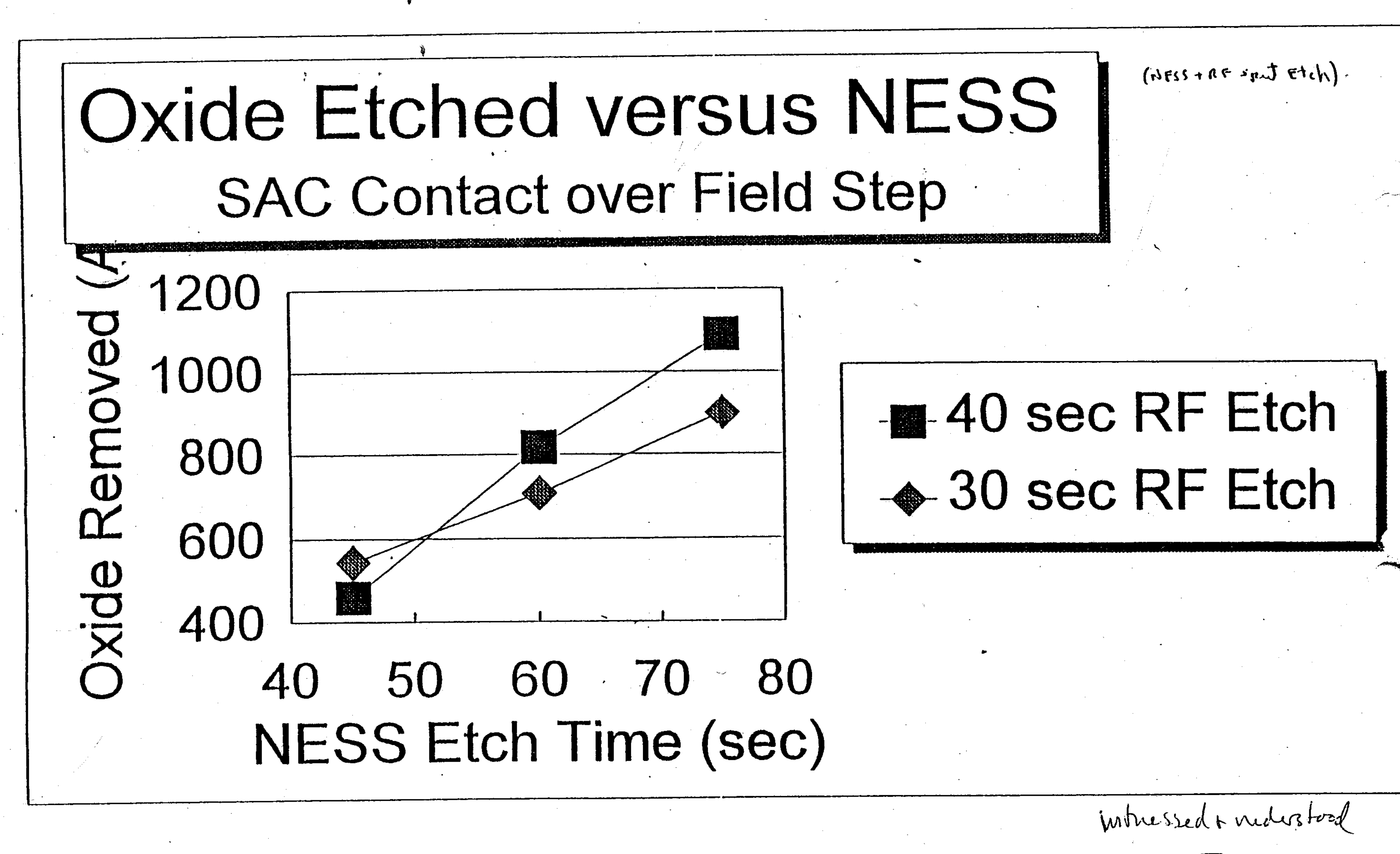
[illegible]

Corners Tolerance of RF Etch - SA

Min. Oxide Remaining for 40 sec RF Etch

Normalized for 1600 A NPOX @ Nit9

Witnessed & understood


Oxide Etched versus NESS
SAC Contact over Field Step
Oxide Removed (A
1200
1000
800
600
400
40
50
60
70
80
NESS Etch Time (sec)
40 sec RF Etch
30 sec RF Etch

Please date-stamp and return this postcard acknowledging receipt of the following:

USPTO Cover Letter; Amendment; Declaration (with attachment); Petition for Extension of Time; Check Nos. 225906, 228118 and 228119 for $150.00, $150.00 and $110.00

Applicant(s): James E. NULTY et al.
Serial No.: 08/577,751
Filing Date: December 22, 1995
For: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING
Attorney Ref. No.: PM95012

Via First Class Mail on **February 22, 1999**.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/577,751	12/22/95	NULTY	J 16820.P097

MM22/0203

DAVID R. GRAHAM, ESQ.
1337 CHEWPON AVE.
MILPITAS CA 95035

EXAMINER	
GURLEY,L	
ART UNIT	PAPER NUMBER
2812	32/D

DATE MAILED: 02/03/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

Notice of Allowability	Application No. 08/577,751	Applicant(s) Nulty et al.	
	Examiner Lynne Gurley	Group Art Unit 2812	

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to *the amendment filed 4/28/99 and the interview dated 2/2/2000* .

☒ The allowed claim(s) is/are *2, 3, 5-7, 9, 13-18, 20, and 27-41* .

☐ The drawings filed on ______ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

- ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
  - ☐ received.
  - ☐ received in Application No. (Series Code/Serial Number) ______ .
  - ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: ______ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

- ☐ because the originally filed drawings were declared by applicant to be informal.
- ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. *11* .
- ☒ including changes required by the proposed drawing correction filed on *Aug 11, 1997* , which has been approved by the examiner.
- ☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal lettter addressed to the Official Draftsperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

- ☒ Notice of References Cited, PTO-892
- ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). ______
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Notice of Informal Patent Application, PTO-152
- ☒ Interview Summary, PTO-413
- ☒ Examiner's Amendment/Comment
- ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
- ☐ Examiner's Statement of Reasons for Allowance

D

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Andrew D. Fortney on 5/10/99 and 2/2/2000.

2. The application has been amended as follows:

In claim 27, line 13, --and said etch stop layer being removed from a base of said contact opening while being retained on said insulating spacers in the contact opening after the anisotropic etching step--has been inserted after "insulating spacer";

D1

In claim 35, line 17, -- said etch stop layer being removed from a base of said contact opening while being retained on said electrically insulating spacer in the contact opening after the step of etching the etch stop layer--has been inserted after "spacer is maintained".

D2

Changes To The Drawings

3. The following changes to the drawings have been approved by the examiner and agreed upon by applicant: See the PTO Form 892 in Paper No. 11. In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

46

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is (703) 305-3474. The examiner can normally be reached on Monday-Thursday from 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F. Niebling, can be reached on (703) 308-3325. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Lg

February 2, 2000

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800

D

Notice of References Cited

Application No.	Applicant(s)		
08/577,751	Nulty et al.		
Examiner		Group Art Unit	
Lynne Gurley		2812	Page 1 of 1

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
x	A	4,956,312	9/1990	Van Laarhoven	437	180
x	B	5,756,396	5/1998	Lee et al.	438	622
x	C	5,100,838	3/1992	Dennison	437	195
x	D	5,482,894	1/1996	Havemann	437	195
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

*		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	U		
	V		
	W		
	X		

* A copy of this reference is not being furnished with this Office action.
(See Manual of Patent Examining Procedure, Section 707.05(a).)

U. S. Patent and Trademark Office
PTO-892 (Rev. 9-95)

Notice of References Cited

Part of Paper No. 33

Interview Summary	Application No. 08/577,751	Applicant(s) Nulty et al.
	Examiner Lynne Gurley	Group Art Unit 2812

All participants (applicant, applicant's representative, PTO personnel):

(1) *Lynne Gurley* (3) ______

(2) *Andrew D. Fortney* (4) ______

Date of Interview *Feb 2, 2000*

Type: ☒ Telephonic ☐ Personal (copy is given to ☐ applicant ☐ applicant's representative).

Exhibit shown or demonstration conducted: ☐ Yes ☒ No. If yes, brief description:

Agreement ☒ was reached. ☐ was not reached.

Claim(s) discussed: *27 and 35*

Identification of prior art discussed:
N/A

Description of the general nature of what was agreed to if an agreement was reached, or any other comments:
See Examiner's Amendment. The limitations inserted into the allowed claims were proposed on 5/10/1999.

(A fuller description, if necessary, and a copy of the amendments, if available, which the examiner agreed would render the claims allowable must be attached. Also, where no copy of the amendents which would render the claims allowable is available, a summary thereof must be attached.)

1. ☒ It is not necessary for applicant to provide a separate record of the substance of the interview.

Unless the paragraph above has been checked to indicate to the contrary, A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION IS NOT WAIVED AND MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a response to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW.

2. ☒ Since the Examiner's interview summary above (including any attachments) reflects a complete response to each of the objections, rejections and requirements that may be present in the last Office action, and since the claims are now allowable, this completed form is considered to fulfill the response requirements of the last Office action. Applicant is not relieved from providing a separate record of the interview unless box 1 above is also checked.

Examiner Note: You must sign and stamp this form unless it is an attachment to a signed Office action.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

MM22/0203

DAVID R. GRAHAM, ESQ.
1337 CHEWPON AVE.
MILPITAS CA 95035

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
08/577,751	12/22/95	028	GURLEY, L	2812	02/03/00

First Named Applicant NULTY, 35 USC 154(b) term ext. = 0 Days.

TITLE OF INVENTION METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
16820.P097	438-634.000	H73	UTILITY	NO	$1210.00	05/03/00

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTO-85 (REV. 10-96) Approved for use through 06/30/99. (0651-0033)

*U.S. GPO: 1999-454-457/24601

B

#33 ML

OIPE JC78
MAR 14 2000
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: James E. Nulty et al.

Assignee: Cypress Semiconductor Corporation

Title: Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies During RF Sputter Cleaning

Serial No.: 08/577,751 Filed: December 22, 1995

Examiner: L. Gurley Group Art Unit: 2812

Batch No.: H73 Allowed: February 3, 2000

Attorney Docket No.: CYP-002

Milpitas, California
March 7, 2000

Box Issue Fee
Assistant Commissioner for Patents
Washington, D.C. 20231

SUBMISSION OF FORMAL DRAWINGS

Sir:

In a Notice of Allowability dated February 3, 2000, in the above-identified application, Applicants were required to submit formal drawings. Applicants submit herewith eight (8) sheets of formal drawings consisting of FIGS. 1A, 1B, 1C, 2A, 2B, 3, 4A, 4B, 4C, 4D, 4E, 4F, 4G, 4H, 4I, 4J, 4K and 4L. The Official Draftsperson is requested to telephone Applicants' undersigned attorney at (408) 945-9912 if there are any questions or problems with the enclosed formal drawings.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on March 7, 2000.

3-7-00 David R Graham
Date Signature

Respectfully submitted,

David R. Graham
David R. Graham
Reg. No. 36,150
Attorney for Applicants

SAMSUNG-1008.317

6066555

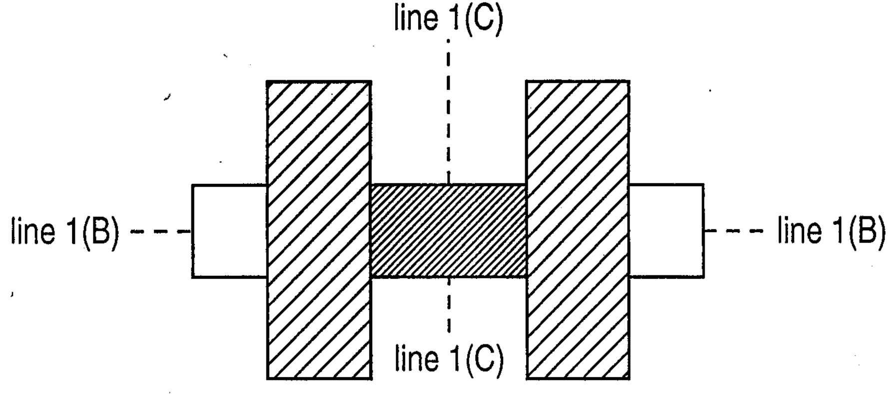


Figure 1A
(PRIOR ART)

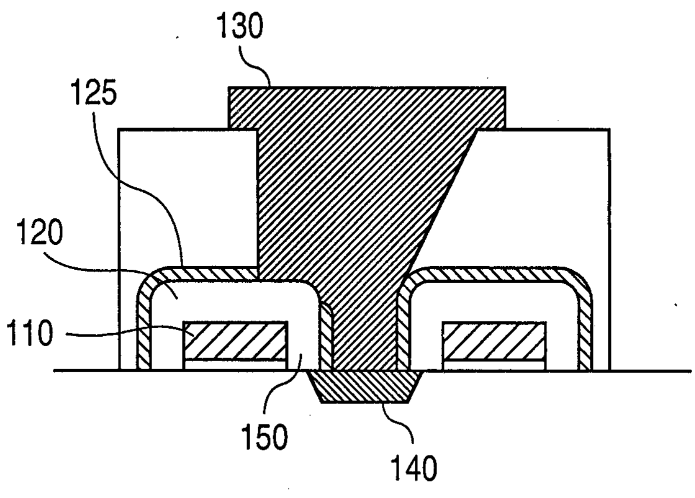


Figure 1B
(PRIOR ART)

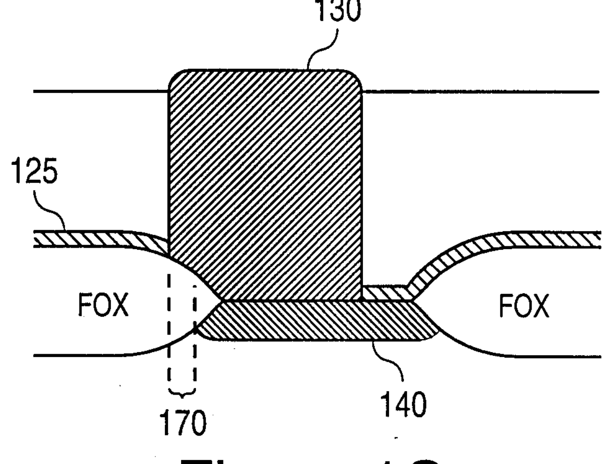


Figure 1C
(PRIOR ART)

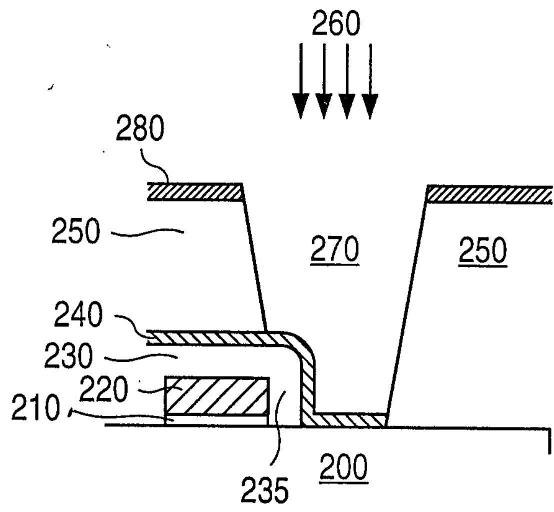


Figure 2A
(PRIOR ART)

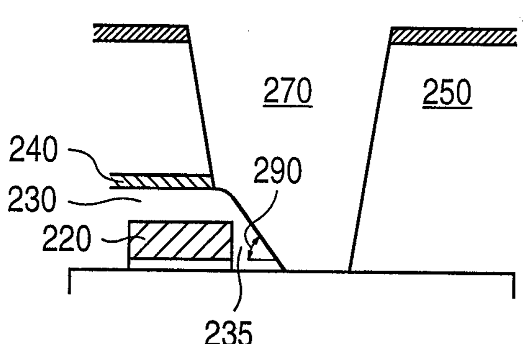


Figure 2B
(PRIOR ART)

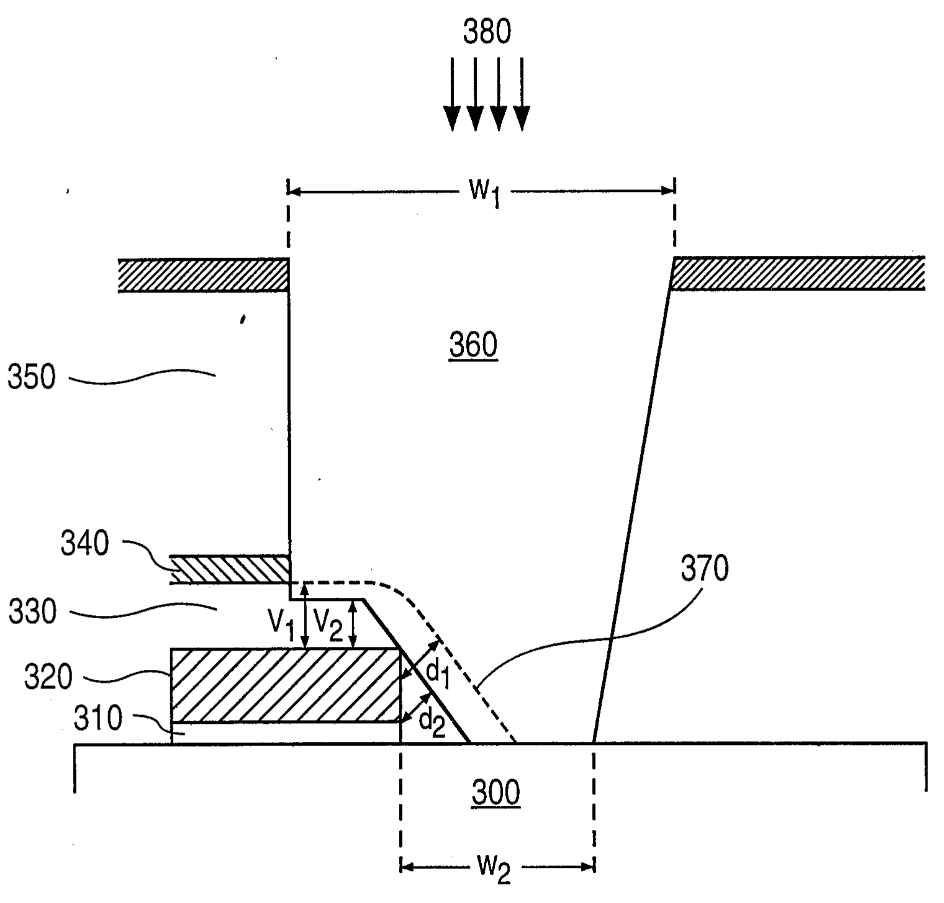


Figure 3
(PRIOR ART)

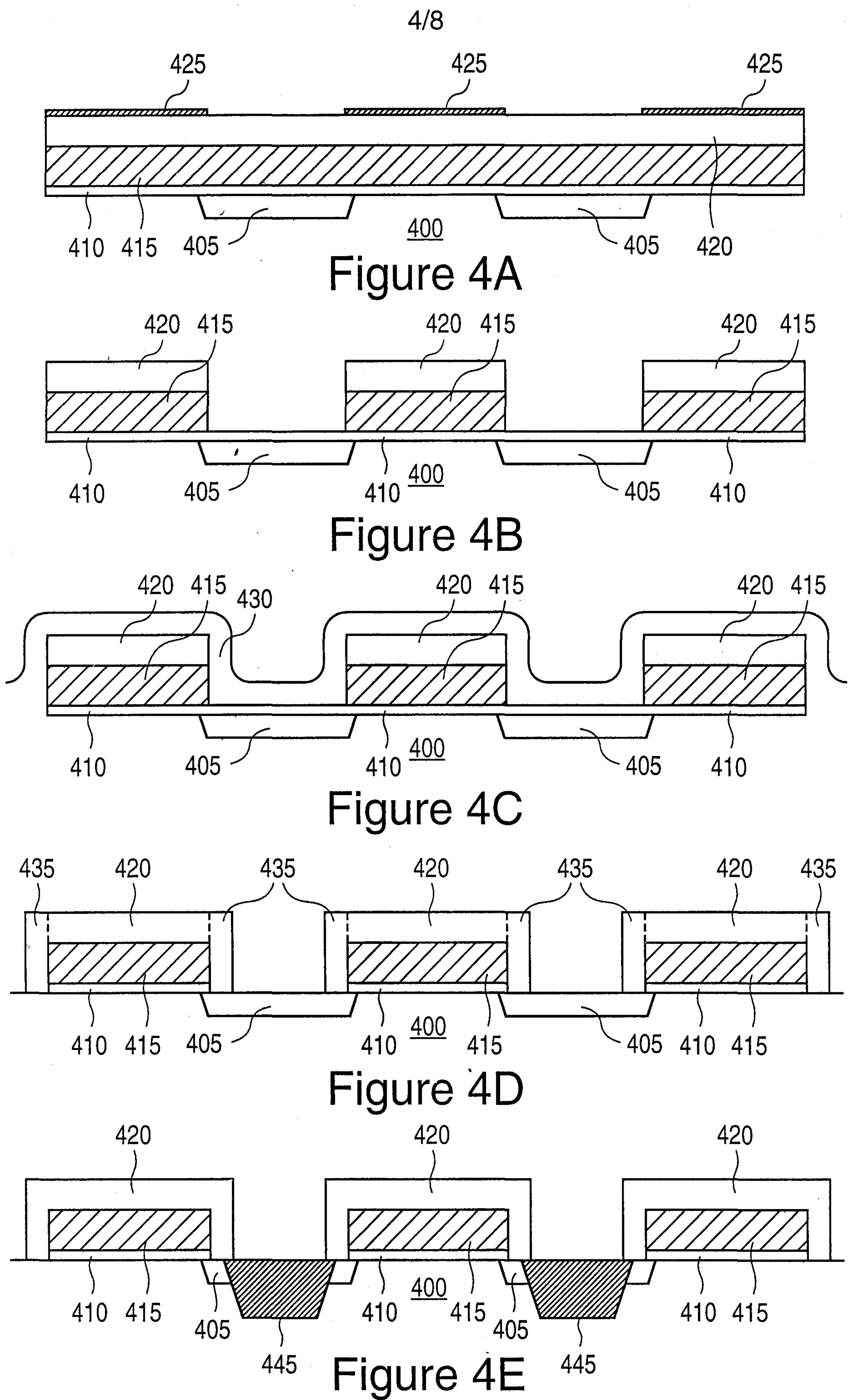


Figure 4A

Figure 4B

Figure 4C

Figure 4D

Figure 4E

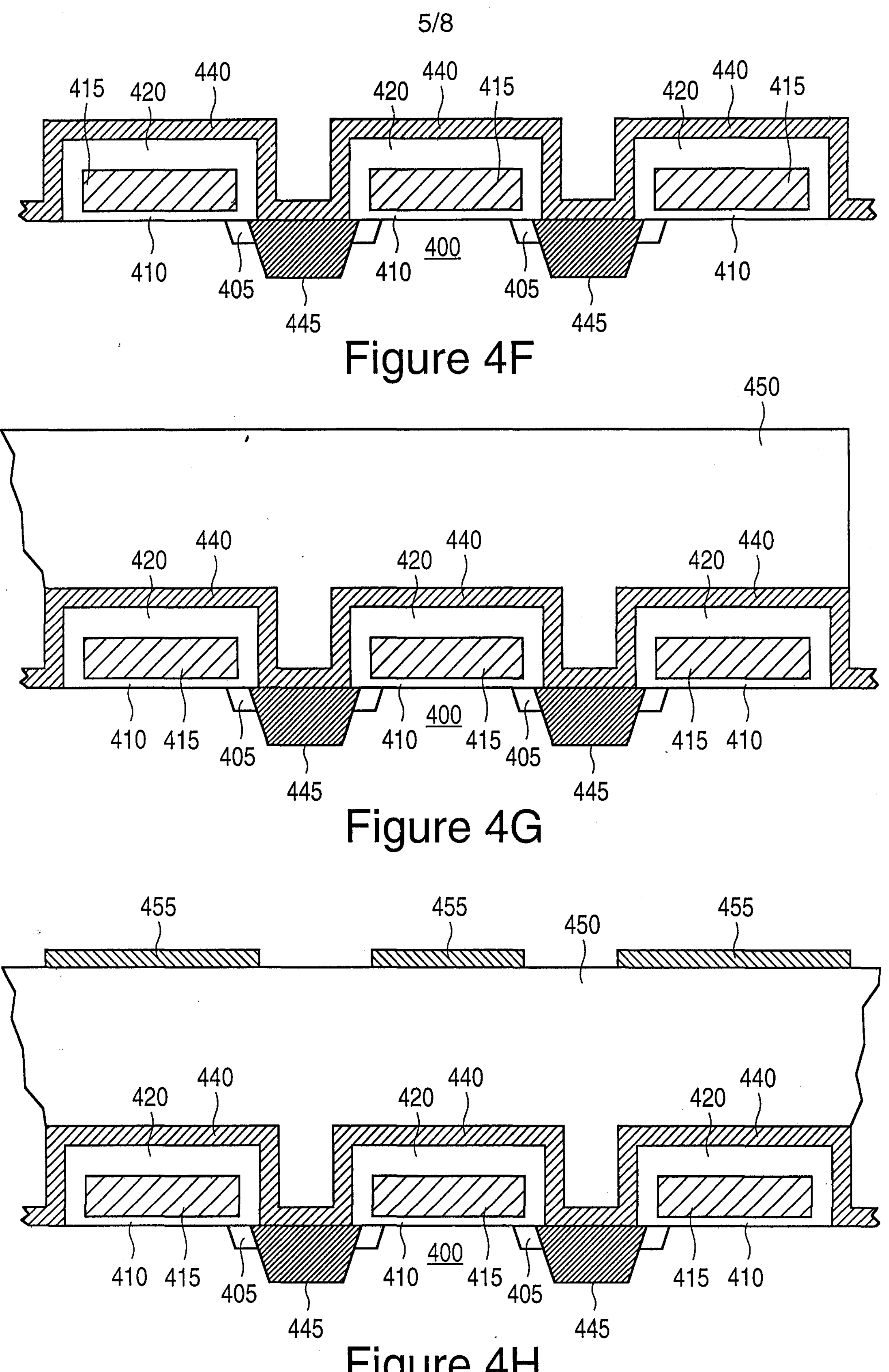


Figure 4F

Figure 4G

Figure 4H

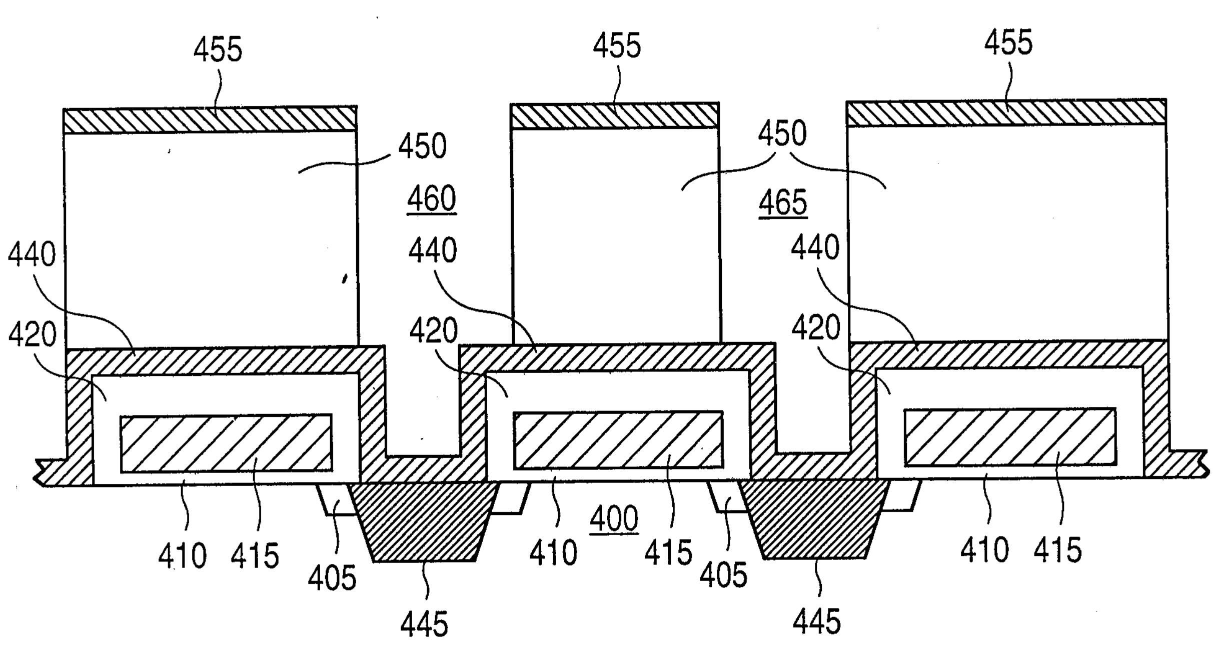


Figure 4I

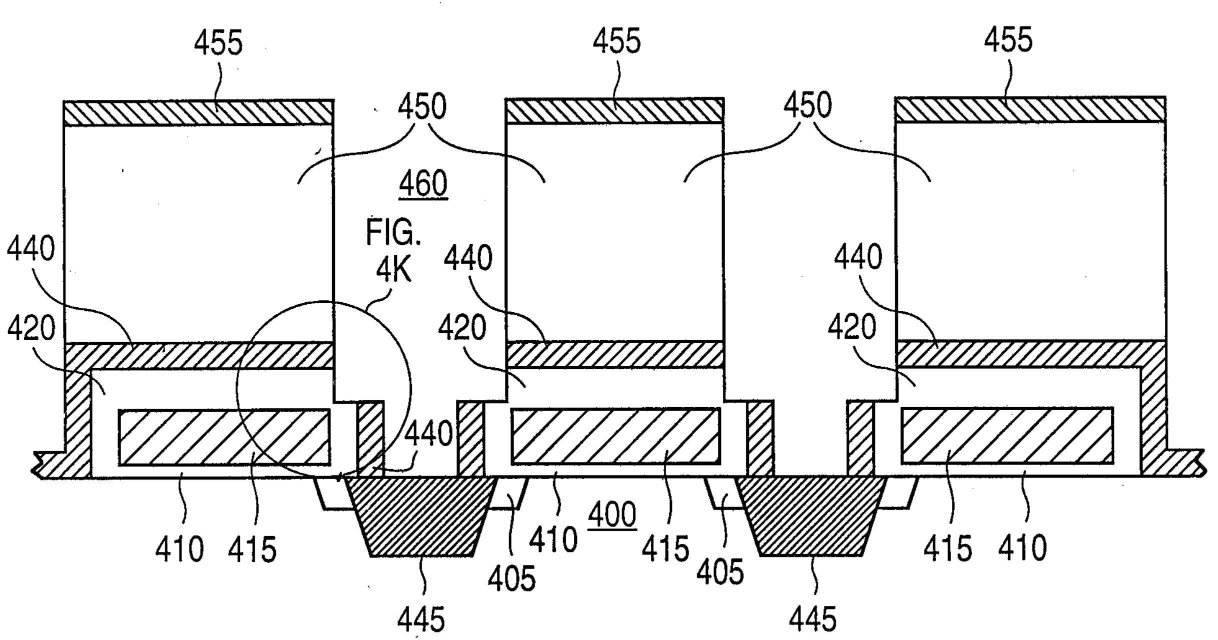


Figure 4J

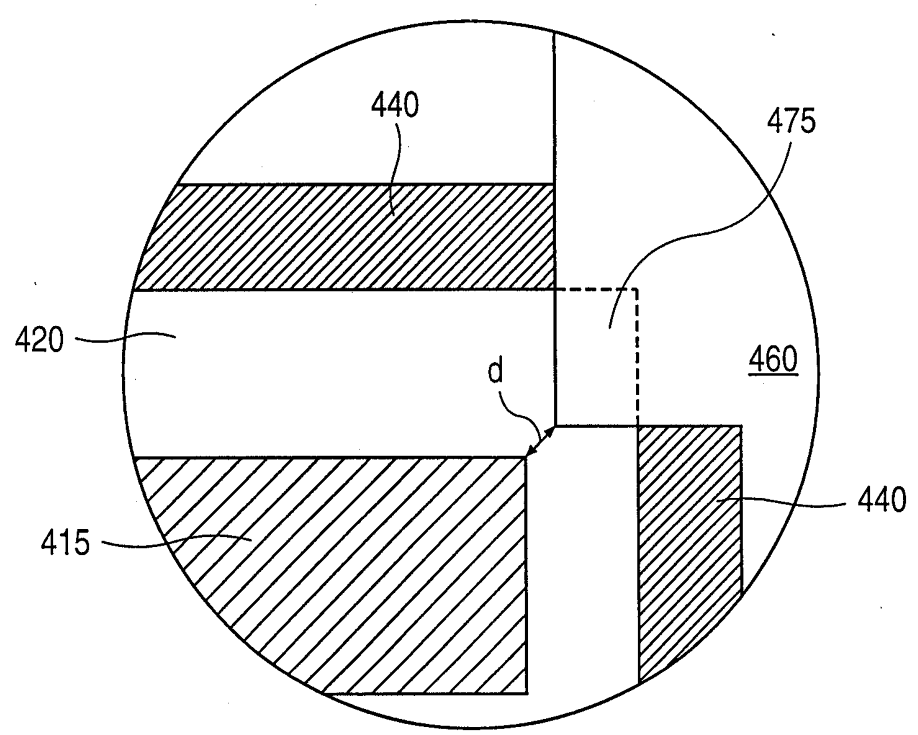


Figure 4K

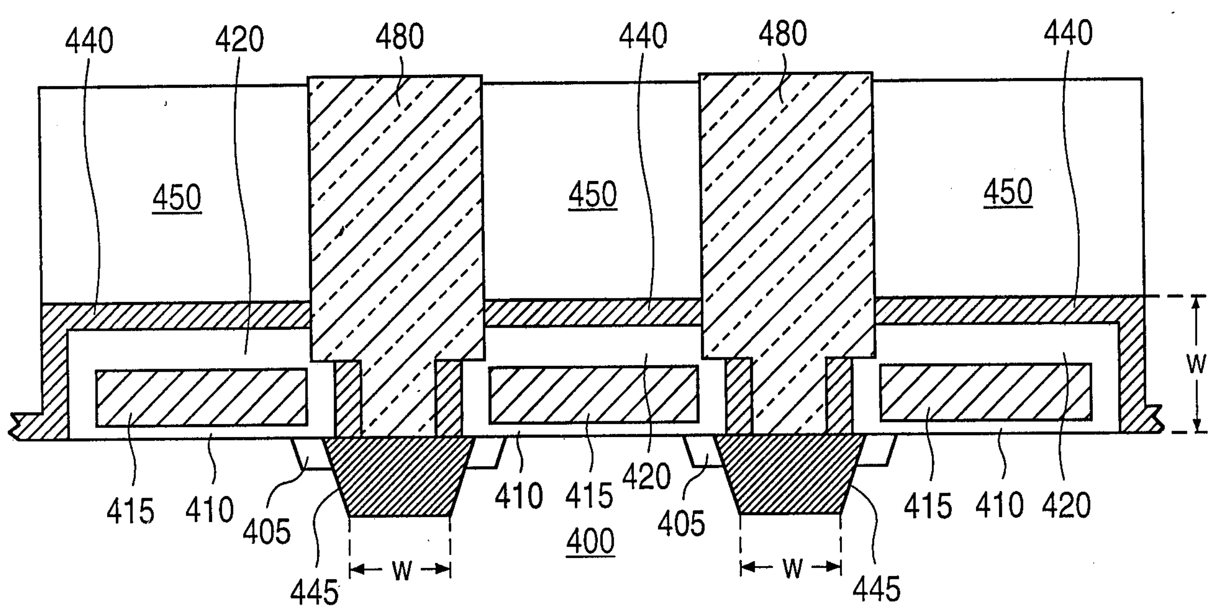


Figure 4L

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David R. Graham (Depositor's name)
David R. Graham (Signature)
March 17, 2000 (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
08/577,751	12/22/95	028	GURLEY, L	2812	02/03/00

First Named Applicant: NULTY, 35 USC 154(b) term ext. = 0 Days.

TITLE OF INVENTION: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
1 16820.P097	438-634.000	H73	UTILITY	NO	$1210.00	05/03/00

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

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(A) NAME OF ASSIGNEE Cypress Semiconductor Corporation

(B) RESIDENCE: (CITY & STATE OR COUNTRY) San Jose, California

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PATENT APPLICATION FEE DETERMINATION RECORD Effective October 1, 1995	Application or Docket Number 577751

CLAIMS AS FILED - PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE				375.00	OR		750.00
TOTAL CLAIMS	26 minus 20 =	* 6	x$11=		OR	x$22=	132
INDEPENDENT CLAIMS	3 minus 3 =	* 0	x39=		OR	x78=	
MULTIPLE DEPENDENT CLAIM PRESENT			+125=		OR	+250=	
			TOTAL		OR	TOTAL	882

* If the difference in column 1 is less than zero, enter "0" in column 2

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AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total	*	Minus	**	=	x$11=		OR	x$22=	
Independent	*	Minus	***	=	x39=		OR	x78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+125=		OR	+250=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total	*	Minus	**	=	x$11=		OR	x$22=	
Independent	*	Minus	***	=	x39=		OR	x78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+125=		OR	+250=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total	*	Minus	**	=	x$11=		OR	x$22=	
Independent	*	Minus	***	=	x39=		OR	x78=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+125=		OR	+250=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

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08/577751	1	12 22 95	0	2503	257	008

TOTAL CLAIMS	INDEPENDENT CLAIMS	SMALL ENTITY?	FILING FEE	FOREIGN LICENSE	ATTORNEY DOCKET NUMBER
026	003			Y	16820.P097.

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			PCT/ /		
			PCT/ /		
			PCT/ /		
			PCT/ /		
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PCT/FOREIGN APPLICATION DATA

FOREIGN PRIORITY CLAIMED	COUNTRY CODE	PCT/FOREIGN APPLICATION SERIAL NUMBER	FOREIGN FILING DATE (MONTH DAY YEAR)

☆ U.S. GPO: 1995-401-429

1C2B
4E,L

CPA   Filing Date: 6-29-98

Reminder: UP Date Docket #

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1997

Application or Docket Number: Place in Case of Adm 08/577757

CLAIMS AS FILED - PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	SMALL ENTITY TYPE ☐ RATE	FEE	OR	OTHER THAN SMALL ENTITY RATE	FEE
BASIC FEE				395.00	OR		790.00
TOTAL CLAIMS	29 minus 20 =	* 9	x$11=		OR	x$22=	198.00
INDEPENDENT CLAIMS	2 minus 3 =	*	x41=		OR	x82=	
MULTIPLE DEPENDENT CLAIM PRESENT			+135=		OR	+270=	
			TOTAL		OR	TOTAL	988.00

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CLAIMS AS AMENDED - PART II

AMENDMENT A

	CLAIMS REMAINING AFTER AMENDMENT (Column 1)		HIGHEST NUMBER PREVIOUSLY PAID FOR (Column 2)	PRESENT EXTRA (Column 3)	SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
Total	* 29	Minus	** 29	=	x$11=		OR	x$22=	
Independent	* 2	Minus	*** 3	=	x41=		OR	x82=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+135=		OR	+270=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

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Total	*	Minus	**	=	x$11=		OR	x$22=	
Independent	*	Minus	***	=	x41=		OR	x82=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+135=		OR	+270=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

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Total	*	Minus	**	=	x$11=		OR	x$22=	
Independent	*	Minus	***	=	x41=		OR	x82=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM					+135=		OR	+270=	
					TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

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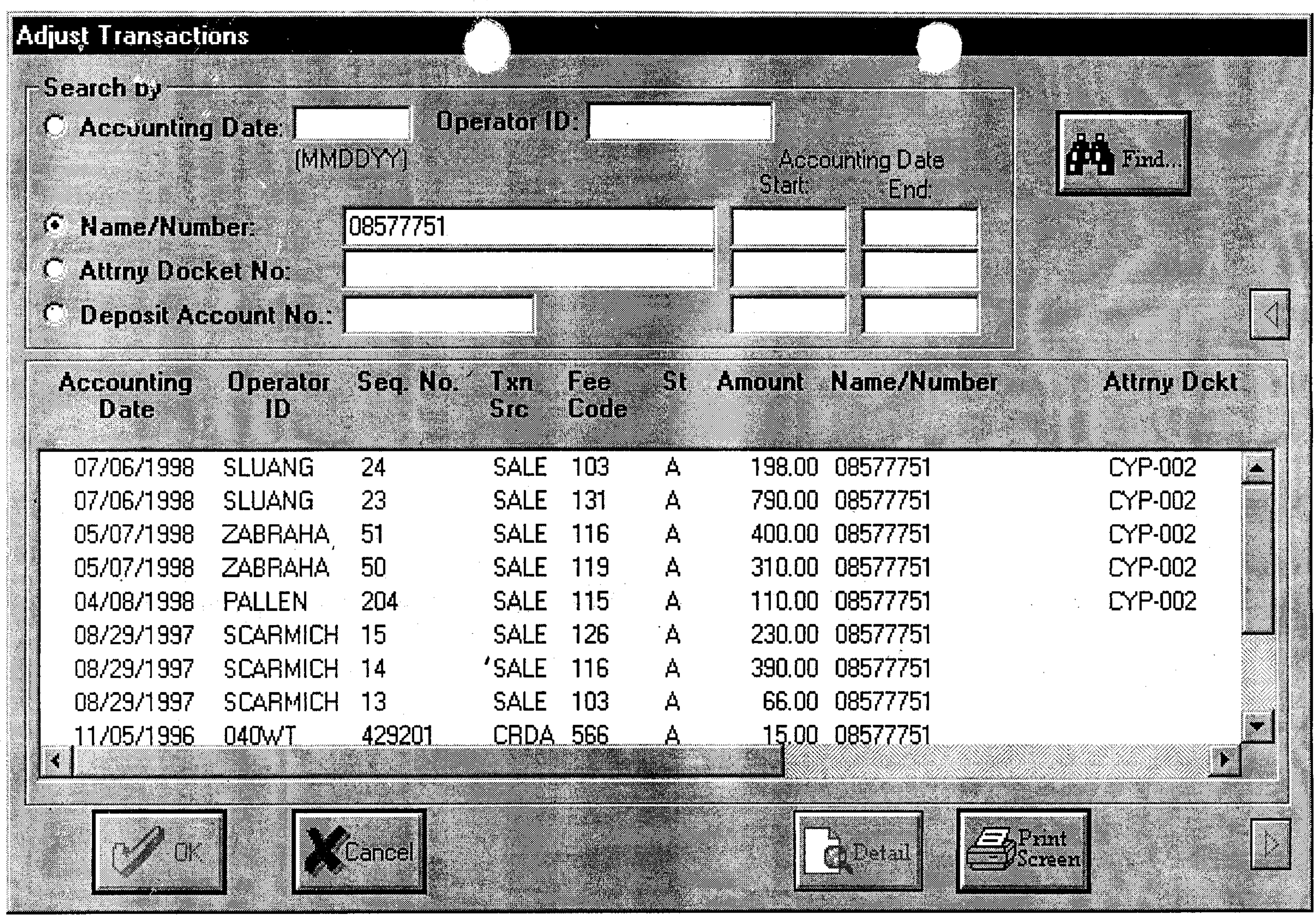

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05/07/1998	ZABRAHA	50	SALE	119	A	310.00	08577751	CYP-002
04/08/1998	PALLEN	204	SALE	115	A	110.00	08577751	CYP-002
08/29/1997	SCARMICH	15	SALE	126	A	230.00	08577751	
08/29/1997	SCARMICH	14	SALE	116	A	390.00	08577751	
08/29/1997	SCARMICH	13	SALE	103	A	66.00	08577751	
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  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
=> s low bombardment and high neutral flux and etch?
        978406 LOW
         10391 BOMBARDMENT

            45 LOW BOMBARDMENT
                 (LOW(W)BOMBARDMENT)
       1253083 HIGH
        109944 NEUTRAL

         68959 FLUX
             1 HIGH NEUTRAL FLUX
                 (HIGH(W)NEUTRAL(W)FLUX)
         80995 ETCH?
L1           0 LOW BOMBARDMENT AND HIGH NEUTRAL FLUX AND ETCH?
=> s low bombardment and etch? and plasma
        978406 LOW
         10391 BOMBARDMENT

            45 LOW BOMBARDMENT
                 (LOW(W)BOMBARDMENT)
         80995 ETCH?
         63386 PLASMA
L2          43 LOW BOMBARDMENT AND ETCH? AND PLASMA
=> s neutral flux and etch? and plasma
        109944 NEUTRAL
         68959 FLUX
            35 NEUTRAL FLUX
                 (NEUTRAL(W)FLUX)
         80995 ETCH?
         63386 PLASMA
L3           4 NEUTRAL FLUX AND ETCH? AND PLASMA
=> s (l2 or l3) and lam 4400
           953 LAM
          2823 4400/BI
          1006 4,400/BI
          3765 4400
                 ((4400 OR 4,400)/BI)
             3 LAM 4400
                 (LAM(W)4400)
L4           0 (L2 OR L3) AND LAM 4400
=> s (l2 or l3) and lam
```

953 LAM
L5 1 (L2 OR L3) AND LAM
=> d l5

1 5,562,801, Oct. 8, 1996, Method of **etching** an oxide layer; James E. Nulty, 156/643.1, 657.1, 659.11; 216/37, 67; 437/228 [IMAGE AVAILABLE]
=> d kwic l5

US PAT NO: 5,562,801 [IMAGE AVAILABLE] L5: 1 of 1
TITLE: Method of **etching** an oxide layer

ABSTRACT:
A method of **etching** an oxide layer is disclosed. First, a resist layer is formed on an oxide layer on a substrate. Next, a. . . removed. The exposed regions may overlie a nitride layer, and may overlie a structure such as a polysilicon gate. The **etch** is performed such that polymer deposits on the photosensitive layer, thus eliminating interactions between the photosensitive layer and the **plasma**. In this way, a simple **etch** process allows for good control of the **etch**, resulting in reduced aspect ratio dependent **etch** effects, high oxide:nitride selectivity, and good wall angle profile control.

SUMMARY:

BSUM(3)

The present invention relates to the field of semiconductor device fabrication and more particularly to improved methods for **etching** openings in oxide layers.

SUMMARY:

BSUM(7)

To . . . the regions of the oxide where the oxide layer openings are to be formed. In most modern processes a dry **etch** is performed wherein the wafer is exposed to a **plasma**, formed in a flow of one or more gases. Typically, one or more halocarbons and/or one or more other halogenated compounds are used as the **etchant** gas. For example, CF.sub.4, CHF.sub.3 (Freon 23), SF.sub.6, NF.sub.3, and other gases may be used as the **etchant** gas. Additionally, gases such as O.sub.2, Ar, N.sub.2, and others may be added to the gas flow. The particular gas mixture used will depend on, for example, the characteristics of the oxide being **etched**, the stage of processing, the **etch** tool being used, and the desired **etch** characteristics such as, **etch** rate, wall slope, anisotropy, etc.

SUMMARY:

BSUM(8)

Various **etch** parameters such as the gas mixture, temperature, RF power, pressure, and gas flow rate, among others, may be varied to achieve the desired **etch** characteristics described above. However, there are invariably tradeoffs between the various desired characteristics. For example, most high performance **etches** exhibit aspect ratio dependent **etch** effects (ARDE effects). That is, the rate of oxide removal is dependent upon the aspect ratio of the opening, which can be defined as the ratio of the depth of the opening to the diameter. In general, the oxide **etch** rate, in terms of linear depth **etched** per unit time, is much greater for low aspect ratio openings than for high aspect ratio openings. Referring to FIG.. . . substrate 100 represents a semiconductor substrate and any device layers or structures underlying the oxide layer 101 through which the **etch** is to be performed. For example, there may be a silicon nitride layer (Si.sub.3 N.sub.4) underlying oxide layer 101. Herein,. . .

SUMMARY:

BSUM(9)

As . . . aspect ratio due to its small diameter. As a result of this, as shown in FIG. 1, the prior art **etch** process causes opening 121 through the oxide layer 101 to be fully **etched** prior to opening 122. In the prior art, this aspect ratio dependency may be overcome by adjusting the feed gas. . . methods of minimizing the aspect ratio dependency typically result in a tradeoff between ARDE effects and other characteristics such as **etch** rate, selectivity, and profile control, for example. Recently, use of high density **plasma** (HDP) systems has been proposed to compensate for the ARDE effect. However, these HDP systems are not yet proven in a production mode, and they entail significant capital costs. It should be noted that more advanced technologies demand high **etch** performance in high aspect ratio features, and demand high **etch** performance in layers having features with a wide range of aspect ratios. Thus, the ARDE effect constitutes a significant hurdle. . .

SUMMARY:

BSUM(10)

Many of the **etch** characteristics are generally believed to be affected by polymer residues which deposit during the **etch**. For this reason, the fluorine to carbon ration (F/C) in the **plasma** is

considered an important determinant in the **etch**. In general, a **plasma** with a high F/C ratio will have a faster **etch** rate than a **plasma** with a low F/C ratio. At very low ratios, (i.e., high carbon content) polymer deposition occurs and **etching** ceases. The **etch** rate as a function of the F/C ratio is typically different for different materials. This difference is used to create a selective **etch**, by attempting to use a gas mixture which puts the F/C ratio in the **plasma** at a value that leads to **etching** at a reasonable rate for one material, and that leads to no **etching** or polymer deposition for another. For a more thorough discussion of oxide **etching**, see S. Wolf and R. N. Tauber, Silicon Processing for the VLSI ERA, Volume 1, pp 539-585 (1986).

SUMMARY:

BSUM(11)

By . . . is desired, the chemistry is adjusted to try to prevent buildup on the sidewall. An important problem with changing the **etch** chemistry is that there is a tradeoff between wall angle and selectivity. That is, **etches** which provide a near 90.degree. wall angle are typically not highly selective between oxide and an underlying silicon or silicon nitride layer, for example, while highly selective **etches** typically have a low wall angle.

SUMMARY:

BSUM(12)

FIG. . . . patterning layer 210 with opening 211 therein. Opening 221 in the oxide layer 201 is shown during formation. In the **etch** illustrated in FIG. 2, high selectivity may be desired to protect an underlying region of, for example, silicon nitride on. . . be maintained, the resulting opening 221 will have a taper as shown by angle 206. Often, in a prior art **etch** with acceptable selectivity, the angle 206 is less than 85.degree.. This tradeoff is particularly severe in **etches** through thick oxide layers. For example, if the process is engineered to allow for a steep wall profile through a. . . the selectivity will be very poor. While adjustments can be made to improve the wall angle, such as by changing **etch** chemistry, and other parameters, all processes will suffer from the selectivity tradeoff to some degree. Additionally, such changes will affect. . . above, adjustment to the process parameters will have some effect on the ARDE effect. Furthermore, even if adjustments to the **etch** parameters are found which enhance selectivity without a severe impact on wall angle, such adjustments will involve other tradeoffs. For example, there is typically a tradeoff between selectivity and **etch** rate, so that

increased selectivity may only be had at the expense of throughput. As can be seen, though some adjustments can be made, it is extremely difficult to design an oxide **etch** which meets all necessary goals. Additionally, it will be appreciated that while the general effects of certain process conditions are. . . and the existence of certain tradeoffs can be predicted, it is far from a straightforward matter to precisely tailor an **etch** or precisely predict the effects changes in the parameters will have. Furthermore, it is often difficult to prevent other undesired. . .

SUMMARY:

BSUM(13)

FIG. 3 illustrates the effect of polymer buildup during a typical prior art **etch** process. Polymer buildup along the regions 307 along the sidewalls of opening 321 cause the wall profile to be different than a straight **etch** profile, shown dashed. Additionally, polymer buildup in the region 308 at the center of the bottom of the opening prevents **etching** of a portion of the nitride layer 302. However, **etching** does occur around the outer edges. Thus, the result of the prior art process is poorly controlled wall profile, and. . . non-uniformity of the nitride layer 302 in the bottom of the opening 321. Again, changing the gas chemistry and other **etch** parameters may be used to improve the **etch**, but some tradeoffs are inevitable. Additionally, for example, attempts to improve the oxide :nitride selectivity often lead to nonstable **plasma** conditions, and involve high polymer chemistries, which in turn leads to dirty reactors requiring extensive maintenance, and particle generation which. . .

SUMMARY:

BSUM(14)

The above described difficulties in oxide **etching** make it extremely difficult to form openings over corners of structures. Referring to FIG. 4, opening 411 in patterning layer. . . be, for example, a gate, an interconnect line, or other structure. As shown, structure 404 is covered by silicon nitride **etch** stop layer 403. Typically, the opening 421 is designed to partially overlie structure 404 to a certain extent. Note that as the **etch** proceeds, opening 421 will extend to the corner of the structure 404 prior to the completion of the **etch** to the bottom of the opening at 432. As shown, due to the difficulty in achieving a highly selective **etch**, the nitride layer 403 is removed from structure 404 on the top 430 and side 431, which are exposed to the **etch** for a significant time before the **etch** reaches the bottom 432. This problem is particularly severe if the opening 411 is misaligned

such that the opening in. . . a reduction in the micro-loading effect, which in turn causes the now reduced area of nitride layer 403 to be **etched** at a much faster rate.

SUMMARY:

BSUM(15)

What is needed is a method or methods of **etching** oxide with reduced ARDE effect, which exhibit a high oxide to nitride selectivity, and which provide control of wall profile.. . . that any such methods do not suffer from severe tradeoffs between and among these and other performance goals such as **etch** rate, so that highly selective **etches** with reduced sidewall taper and/or reduced ARDE effects, may be achieved. The method or methods should enable the formation of openings which lie on or over other structures, such as in a self-aligned contact **etch**. Finally, the method or methods should allow for increased opening depth, especially in process steps requiring the formation of deep openings of different depths, without an unacceptable sacrifice in performance. The method or methods should provide the above described **etch** characteristics without requiring extensive redesign of the process or process tools, unacceptable performance or process maintenance tradeoffs, costly and unproven. . .

SUMMARY:

BSUM(17)

A method of **etching** openings such as contact openings or via openings in an oxide layer is disclosed. The method of the present invention may be used for a wide variety of **etches**, including **etches** with openings having different aspect ratios, over flat structures, over steep topography, and in **etches** having all of these. In the present invention, the ARDE effect is reduced or eliminated, improved oxide:nitride selectivity is achieved,. . . eliminated. In one embodiment, a hard mask layer of, for example, polysilicon is used as a mask for the oxide **etch**. A patterned photoresist layer, exposing regions of the hard mask corresponding to the openings to be formed in the oxide layer is formed on the hard mask. An **etch** of the hard mask in the exposed regions is then performed. It has been found that the interaction of the photoresist mask, and more particularly it is believed the carbon from the photoresist mask, with the **plasma** **etch** chemistry has a dominant effect on the aspect ratio dependency of the **etch**. Therefore, in one embodiment, the photoresist mask is removed prior to the completion of the oxide **etch**. The elimination of the photoresist/**etch** chemistry interaction has been found to greatly reduce or eliminate aspect ratio dependent **etch** effects.

Additionally, the hard mask is found to interact with the **etch** chemistry to improve the oxide:nitride selectivity. In another embodiment of the present invention, the oxide **etch** is carried out at an elevated temperature, allowing for increased selectivity without a tradeoff with wall angle. In a further embodiment, Freon 134a is used as an additive to the **etchant** gas allowing for improved oxide:nitride selectivity. In a further embodiment, the hard mask, Freon 134a, and elevated temperature are used to perform **etches** providing a selective oxide:nitride **etch** over both flat surfaces and corner topography. In additional embodiments, the **etches** may be carried out in two steps. In the case of a thick oxide layer, this allows for a high **etch** rate, and selectivity, while leaving a uniform nitride underlayer. In one two step **etch** process, a clean step is performed to remove any built up polymers before proceeding with the second **etch** step.

SUMMARY:

BSUM(18)

In a further embodiment of the present invention, an **etch** is performed using a photoresist mask. This **etch** is carried out such that a polymer deposits on the resist surface, and additionally, the side walls of the openings as they are being formed. In this way, the photoresist mask does not interact with the **plasma**, thus providing for greatly reduced or eliminated aspect ratio dependent **etch** effects. Further, the **etch** chemistry results in improved oxide:nitride selectivity. This **etch** may be used over both flat or cornered topographies without the need for a separate hard mask deposition and **etch** step.

DRAWING DESC:

DRWD(3)

FIG. 1 illustrates aspect ratio dependent **etching** of a prior art oxide **etch** process.

DRAWING DESC:

DRWD(4)

FIG. 2 illustrates wall profile in a prior art oxide **etch** process.

DRAWING DESC:

DRWD(5)

FIG. 3 illustrates poor oxide:nitride selectivity in a prior art **etch** process.

DRAWING DESC:

DRWD(6)

FIG. 4 illustrates a prior art **etch** process over a structure.

DRAWING DESC:

DRWD(8)

FIG. 6 illustrates the structure of FIG. 5 after the **etch** of the hard mask.

DRAWING DESC:

DRWD(9)

FIG. 7 illustrates the oxide **etch** performed on the structure of FIG. 6 in an embodiment of the present invention, just prior to completion.

DRAWING DESC:

DRWD(11)

FIG. 9 illustrates the result of an oxide **etch** in accordance with an embodiment of the present invention.

DRAWING DESC:

DRWD(12)

FIG. 10A illustrates the molecular structure of an **etchant** used in an embodiment of the present invention.

DRAWING DESC:

DRWD(14)

FIG. 11 shows the result of an oxide **etch** using a chemistry comprising the **etchant** shown in FIG. 10.

DRAWING DESC:

DRWD(15)

FIG. 12 illustrates a cross-sectional elevation view of a structure on which an oxide **etch** according to an embodiment of the present invention is to be performed.

DRAWING DESC:

DRWD(16)

FIG. 13 illustrates the structure of FIG. 12 after **etching** of the hard mask of an embodiment of the present invention.

DRAWING DESC:

DRWD(17)

FIG. 14 illustrates the structure of FIG. 13 after an oxide **etch** according to an embodiment of the present invention.

DRAWING DESC:

DRWD(18)

FIG. 15 illustrates a cross-sectional elevation view of a structure to be **etched** in an embodiment of the present invention.

DRAWING DESC:

DRWD(19)

FIG. 16 shows the structure of FIG. 15 after a first **etch** step and a clean step.

DRAWING DESC:

DRWD(20)

FIG. 17 illustrates the structure of FIG. 16 after a second **etch** step.

DRAWING DESC:

DRWD(21)

FIG. 18 illustrates a cross-sectional elevation view of a structure to be **etched** in a further embodiment of the present invention.

DRAWING DESC:

DRWD(22)

FIG. 19 illustrates the structure of FIG. 18 during the **etch**.

DRAWING DESC:

DRWD(23)

FIG. 20 illustrates the structure of FIGS. 18 and 19 at the completion of the **etch**.

DETDESC:

DETD(2)

A method of **etching** an oxide layer is disclosed. In the following description, numerous specific details are set forth such as specific materials, thicknesses,. . . utilized on a variety of structures and oxide layers, to form any type of opening, and each of the oxide **etching** methods described herein is not necessarily restricted to the structure and/or oxide layer in conjunction with which it is described. Further, any of the methods described herein may be performed as a part of a multistep **etch** comprising additional **etch** processes. Several exemplary multistep processes are described below.

DETDESC:

DETD(4)

In . . . the wafer may be formed simultaneously with those shown in the Figures. Next, in step 815 the hard mask is **etched** using an **etchant** appropriate for the material of which hard mask 505 is composed, and patterning layer 510 is removed in step 820.. . . that opening 516 has a much higher aspect ratio. As described earlier, this typically leads to a much slower oxide **etch** rate in the region of opening 516. However, with use of the hard mask 505 this is avoided in thee present invention. The structure of FIG. 6 is next subjected to an oxide **etch** in step 805 to form openings in the oxide layer corresponding to hard mask openings 515 and 516. Referring to FIG. 7, openings 521 and 522 in the oxide layer 501 during the **etch**, at a time just prior to completion of the **etch**, are shown. As can be seen, the openings 521 and 522 extend approximately the same distance through the oxide layer. . . the hard mask of the present invention has been found to reduce or eliminate the aspect ratio dependency of the **etch**.

DETDESC:

DETD(5)

Although the use of hard mask 505 is advantageous in any **etch** process, one embodiment of the present invention is carried out in the **LAM** 384T Dry **Etch** System Which is an RIE/Triode system. For 6" (150 mm) wafers, the **etch** is Carried out in a flow comprising 2.5 standard cubic centimeters per minute (SCCM) Freon 134a and 10 SCCM CHF.sub.3 (Freon 23). The **etch** is carried out at 600 watts (W) with a DC bias of approximately 1400 volts (V). The **etch** is performed at a pressure in the range of approximately 10-40 mTorr. The lower electrode water coolant temperature is set. . . C., and the upper chamber temperature is set at 50.degree. C. It will be appreciated that although the above described **etch** was performed in a single step after removal of the photoresist layer 510, the **etch** may be carded out in two steps, with a first portion of the oxide layer **etched** with resist layer 510 intact, followed by resist strip, and then a high performance final **etch** step With just the hard mask remaining to define the openings. For example, in one embodiment a high **etch** rate, non-selective **etch** step designed to **etch** the undoped oxide layer and some of the doped layer, such that there remains approximately 2000 .ANG. of oxide in the thinnest area of the wafer, is first performed, followed by a second **etch** step similar to that described above. As will be described in a further embodiment of the present invention, a clean step may be performed between the **etch** steps.

DETDESC:

DETD(6)

The use of hard mask 505 as described above is beneficial in any existing oxide **etch** process. The invention is believed to provide for minimized ARDE effect by eliminating the photoresist contribution to the total carbon content of the **plasma**. As described earlier, polymer residue formed from carbon in the **plasma** has a strong effect on **etch** characteristics such as selectivity and wall profile. However, it is heretofore not been recognized that the photoresist layer has such a dominant effect on **etch** characteristics such as the ARDE effect. Because this dominant effect from the photoresist is removed, considerable process latitude is achieved, since the selection of the **etch** gas chemistry is no longer constrained by the requirement that it be adjusted to minimize the ARDE effect, and can instead be adjusted to achieve other performance goals such as **etch** rate, selectivity, profile control, etc. As described above, the benefits of the present invention are believed to be achieved by eliminating the interaction of

the photoresist, and most likely the carbon from the photoresist, with the **plasma** chemistry. Therefore, in alternative embodiments of the present invention, a photosensitive layer which has been treated to become relatively inert to the **plasma** chemistry may be used as the sole masking layer. For example, a silylated photoresist layer, formed by, for example, a. . . in these papers. A photosensitive layer treated in this or a similar manner, which does not significantly react with the **etch** chemistry, and therefore does not overwhelm the carbon content of the **plasma**, may be used in place of the hard mask layer described herein. In this case, there is no need for. . . layer as described above. By inclusion of hard mask 505, or by making the photosensitive layer substantially inert to the **plasma** chemistry, an existing oxide **etch** process need not be reengineered, performed on new equipment, etc., and many of the tradeoffs associated therewith can be avoided or minimized. In the present invention, the **etch** can be tailored without the problem of carbon from the photoresist overwhelming the **etch** characteristics. As will be seen, embodiments of the present invention further include methods of minimizing the selectivity/wall angle tradeoff, improved oxide:nitride selectivity, improved selectivity in **etches** requiring openings to extend over corners, and methods of **etching** deep openings in the oxide layer. The methods of the present invention may be used to achieve the various performance. . .

DETDESC:

DETD(7)

As is well known, in the prior art methods of **etching** an oxide layer, considerable heat is generated by collisions of the ions and/or electrons in the **plasma** with the substrate. As is known, the amount of energy generated in this way will be dependent upon the various. . . in the present invention, as shown in FIG. 6, the resist layer may be removed prior to performing the oxide **etch**. Therefore, in a further embodiment of the present invention the temperature is adjusted (by appropriate adjustment of the backside coolant flow) above the resist reticulation temperature if desired. For example, in one embodiment performed in the above described **etch** system, the backside helium pressure is reduced to approximately 2 Torr, which typically results in a helium flow of approximately. . .

DETDESC:

DETD(8)

FIG. . . . to be formed. As before, a plurality of openings may be formed having different diameters and/or different aspect ratios. The **etch** is performed with the above described helium flow and pressure.

In one embodiment the **etch** is performed in a flow comprising approximately 1.5 SCCM Freon 134a and approximately 47 SCCM CHF.sub.3. The **etch** is carried out at a power of 600 W, a pressure of 30 mTorr, and a DC bias of approximately. . . the increased temperature causes all types of oxides to be less "sticky" than other layers, particularly nitride, so that high **etch** selectivity of oxide to silicon, silicon nitride, titanium silicide, etc. may be achieved. Further, the use of a higher temperature. . . the selectivity is improved or remains the same, at the higher temperature a greater process latitude results. For example, selective **etches** of relatively thick layers of BPSG, with good profile control may be achieved. Furthermore, the temperature increase generally increases the **etch** rate, so that throughput is higher. In addition to this improved wall angle, the embodiment illustrated in FIG. 9 also. . .

DETDESC:

DETD(9)

In the present invention it has been found that by the addition of Freon 134a to any **etch** chemistry, improved oxide:nitride selectivity is achieved, even in chemistries that do not otherwise exhibit oxide:nitride selectivity. Freon 134a has the. . . F.sub.4. An illustration of the Freon 134a molecule 1002 is shown in FIG. 10A. In a currently preferred embodiment, the **etch** is performed in a mixture comprising Freon 134a, and Freon 23 (CHF.sub.3). In one embodiment, the **etch** is performed with a Freon 134a flow rate of approximately 1.5 SCCM, a CHF.sub.3 flow rate of approximately 47 SCCM,. . . previously, and oxide layer 1101 is generally similar to oxide layer 501. Hard mask layer 1105 has been patterned and **etched** to form an opening 1111 therein. An **etch** is performed as described above, and opening 1121 is shown during the **etch** process. As can be seen, the oxide sidewalls 1130 have minimal polymer deposition, while the bottom 1107 has some polymer. . .

DETDESC:

DETD(10)

Although . . . combination with the polysilicon hard mask to reduce free fluorine (F) neutrals and ions, to reduce their concentration in the **plasma**, thus decreasing the F/C ratio at nitride surfaces as compared to oxide surfaces. This brings the **etch** into the regime where oxide **etching** is still at an acceptable rate, while little **etching** occurs on the nitride. It is further believed that the increased selectivity may result from the presence of a three. . .

DETDESC:

DETD(11)

The . . . found to work on a wide vadety of different feature sizes, can be employed in a variety of processes and **etch** tools. Further, the improved selectivity can be achieved with minimal or no tradeoff with other performance goals. Additionally, the selectivity provided by the present invention can be achieved without resort to processes having unstable **plasma** conditions and without resort to high polymer chemistries, thus avoiding the problems of difficult reactor maintenance, particle generation, and reduced wall profile control. For an existing **etch** process chemistry, varying amounts of Freon 134a may be added, depending upon the particular situation. For example, typically, Freon 134a. . .

DETDESC:

DETD(12)

It . . . prior art processes with high selectivity, in addition to the wall profile control problem, it is often difficult to completely **etch** the oxide layer, especially in deep openings. However in the present invention, since the carbon contribution from the photoresist is. . . removed, the selectivity is achieved without the problem of excessive polymer buildup in the bottom, so that openings may be **etched** to completion. Additionally, in the present invention, it has been found that due to the sticking of polymer to nitride, nearly infinite selectivity to nitride is achieved. That is, after a small initial amount is **etched**, polymer buildup begins so that regardless of the length of the **etch**, nitride **etching** does not continue after the small initial amount is **etched**.

DETDESC:

DETD(13)

As . . . it is further difficult to achieve nitride uniformity within the bottom of the contact and to avoid removing the nitride **etch** stop layer from the structure 404. FIGS. 12-14 illustrate a further embodiment of the present invention overcoming this problem. Referring. . . 1211 which is aligned to form an opening in the oxide which will partially overlie the structure 1204, i.e., the **etch** must extend over a corner. For example, the process step illustrated in FIG. 12 may be a self-aligned contact **etch**. Referring now to FIG. 13, hard mask 1205 is **etched** in the region exposed by opening 1211, to form opening 1216. After forming opening 1216, photoresist layer 1210 is removed.

DETDESC:

DETD(14)

In a currently preferred embodiment, an oxide **etch** is performed through hard mask 1205, utilizing a gas chemistry comprising Freon 134a at high temperature. In a currently preferred embodiment, the **etch** is performed in a flow comprising 10 SCCM CHF.sub.3 and 2.5 SCCM Freon 134a, at a power of 600 W.. . . step. In one embodiment, nitride layer 1202 and 1203 have a thickness of approximately 700 .ANG.. With the above described **etch** characteristics, the present invention provides improved results for structures such as that shown in FIGS. 12-14. Because the present invention. . . nitride uniformity is maintained over both corners and flat surfaces, the present invention can be used to perform an oxide **etch** wherein there are openings that overlie corners and openings that overlie flat surfaces. Additionally, since hard mask 1205 minimizes the. . . from one another. Note that these results are achieved with existing reactor technology, and without requiring substantial reengineering of the **etch** process. The present invention provides for an improved process window for an **etch** over topography and flat surfaces, and of course provides greater process latitude in any type of **etch**.

DETDESC:

DETD(15)

A further embodiment of the present invention allows for increased **etch** depth to be achieved without sacrificing **etch** performance. Referring to FIG. 15, patterning layer 1510 having openings 1511 and 1512 is formed on hard mask layer 1505. . . overlying one or more BPSG layers with a total thickness of approximately 10,000 .ANG.-20,000 .ANG.. Typically, it is difficult to **etch** through such a thick layer completely due to polymer buildup in the bottom of the forming opening. Further, for the reasons described previously, it is difficult to maintain the **etch** wherein the openings have different aspect ratios, and wherein some openings may be overlying structures.

DETDESC:

DETD(16)

Therefore, in a further embodiment of the present invention, an **etch** is performed through hard mask layer 1505 to form openings 1516 and 1517 shown in FIG. 15. Next, with resist layer 1510 in place, a high **etch** rate oxide **etch** is performed which is preferably designed to **etch** one or more layers of the uppermost portion of oxide layer 1501. For

example, in one embodiment the **etch** is tailored to **etch** the undoped layer and some of the doped layer. In one embodiment the **etch** is performed in a flow comprising 70 SCCM CHF.sub.3 and 20 SCCM C.sub.2 F.sub.6 (Freon 116). The **etch** is performed at a power of 600 W, and a pressure of 50 mTorr. A helium coolant pressure of 8. . . . is set a 17.degree. C. Next, a polymer removal step is performed. The polymer may be ashed in an oxygen **plasma**, for example, or a wet chemical **etch** may be performed. For example, in one embodiment a first clean step in an IPC barrel ash system, performed in. . .

DETDESC:

DETD(17)

FIG. . . . layer 1501 has been removed. Additionally, all polymer has been removed from the openings. Next, one of the above described **etches** of the present invention, such as that described in conjunction with FIGS. 12-14, comprising Freon 134a, and at high temperature is performed. The structure of FIG. 16 after the second **etch** step is shown in FIG. 17. As shown, openings 1521 and 1522 extend all the way through oxide layer 1501. . . . bottom of the opening. Additionally, nitride layer 1503 overlying structure 1504 remains intact. As described above, the temperature of the **etch** can be varied for the desired taper. For example, an angle 1506 of 85.degree.-90.degree. can be achieved by reducing the. . .

DETDESC:

DETD(18)

As described earlier, use of a hard mask during the oxide **etch** process eliminates the interaction of the photoresist with the **etch** chemistry. By forming a structure such as that shown in FIG. 13, a variety of **etch** chemistries and conditions may be explored to determine polymer formation under these conditions and in the absence of interference from. . . was found to occur on the top, horizontal surface of a hard mask such as hard mask 1205 during the **etch** process. In the prior art, although polymer deposition on the sidewalls, nitride surfaces within openings, and the bottoms of trenches. . .

DETDESC:

DETD(20)

In a currently preferred embodiment, the **etch** is carried out in a **LAM** 384T dry **etch** system. In a system designed for 8 inch wafers, the **etch** is carried out in a flow comprising approximately 3 SCCM

Freon 134a and 10 SCCM CHF.sub.3. The **etch** is carried out at a power in the range of approximately 300-400 W, and preferably approximately 350 W, with a DC bias of approximately 1200 volts. In one embodiment, the **etch** is performed at a pressure in the range of approximately 20-50 mTorr, and preferably approximately 35 mTorr. Also in a. . .

DETDESC:

DETD(21)

Furthermore, . . . lower electrodes. This grid may have a voltage applied thereto or may, as in one embodiment, be grounded during the **etch**. A typical opening size in the grid is approximately 9 mm. However, in one embodiment an opening size of approximately 15 mm is used. The use of larger openings decreases the dark space, and results in a more intense **plasma**. Further, in one embodiment, the electrode spacing was in the range of approximately 1.3-1.8 inches, and preferably approximately 1.6 inch.. . .

DETDESC:

DETD(22)

Referring now to FIG. 19, the substrate of FIG. 18 is shown after the beginning of the above-described **etch** process. As shown, a thin layer 1901 of polymer has formed on the upper surface of resist layer 1810, as well as the sidewalls of opening 1811. This polymer deposition essentially encapsulates the resist layer, such that resist/**plasma** interaction is eliminated. With this encapsulation, an essentially infinite oxide:resist **etch** rate is achieved, so that the resist mask remains intact for the duration of the **etch**. Although the upper surface of the resist layer 1810 receives polymer deposition, **etching** of the oxide layer 1801 in the region exposed by opening 1811 continues to occur. It is believed that polymer deposition occurs on the surface of resist layer 1810 due to an increased neutral:charged ion ratio in the **plasma** of the present invention, as well as other factors resulting in polymer formation/sticking at the surface of resist layer 1810.. . . for example, polysilicon, an oxide layer does not see a net polymer deposition, even in the presence of a high **neutral** **flux**, due to the reactivity of the oxide layer in the presence of ion bombardment, as compared with these other layers.

DETDESC:

DETD(23)

Typically, . . . may occur, polymer deposition on the upper surface

of a resist layer does not occur. Because of this, the resist **etches** at some finite rate in the prior art due to the ion bombardment. Further, the corners typically pull back slightly as the resist layer is **etched**. For example, dashed lines 1905 illustrate the **etching** of photoresist layer 1810, near the opening in a prior art process. Eventually, as the **etch** proceeds, this pulling back of the corners may result in an excessively tapered opening. In contrast, in the present invention,. . . the upper surface of layer 1810 as well as the sidewalls of opening 1811. Additionally, because the resist remains intact, **etches** through relatively thick oxide layers may be performed.

DETDESC:

DETD(24)

Referring to FIG. 20, the substrate of FIG. 19 is shown at the completion of the **etch**. As shown, polymer layer 1901, in addition to encapsulating photosensitive layer 1810, also adheres to nitride layer 1802, and oxide. . . amount of polymer on an oxide sidewall such as sidewall 1801 will be dependent upon process conditions, especially temperature and **etch** chemistry. In a preferred embodiment, although the polymer layer 1901 forms on the sidewall 1801, the temperature of the above-described embodiment is sufficiently high such that an acceptable wall angle is obtained. Additionally, as described earlier, the **etch** chemistry leads to preferential buildup on nitride surfaces, giving good oxide:nitride selectivity. With the formation of polymer layer 1901 on nitride layer 1802, no **etching** of the nitride layer 1802 occurs on top or side surfaces, so that the corner of structure 1804 remains intact. Therefore, as with other embodiments of the present invention, high selectivity, even over corners of structures, and in long **etches** through thick oxide layers, may be maintained.

DETDESC:

DETD(25)

The use of the process described in conjunction with FIGS. 18-20 is advantageous in that it eliminates the deposition and **etch** of a hard mask, and eliminates the removal of photoresist, and any clean steps in the earlier described hard mask. . .

DETDESC:

DETD(26)

As . . . set of conditions may be used in an embodiment having a

photoresist mask, since the polymer deposition will quickly eliminate resist/**plasma** interaction. It will be appreciated that while the earlier described **etch** parameters provide for the encapsulated resist layer, other process conditions may be utilized, in accordance with the guidelines described below,. . .

DETDESC:

DETD(27)

By . . . example, as mentioned above, in one embodiment the openings in the grid were increased. This provides for a more efficient **plasma**, leading to more noncharged chemical species in the **plasma**. This results in a **plasma** that is more likely to deposit polymer on the resist layer 1810 surface than a **plasma** with a higher flux of ions, which is more likely to cause **etching** of the resist. Further, the increase in the electrode spacing, by making the wafer slightly more distant from the **plasma** discharge, has the same effect by decreasing the ion flux at the resist surface. Thus, one of skill in the art may use these considerations to make adjustment to the equipment if desired, to achieve a **plasma** that deposits a polymer on the resist layer while **etching** the oxide layer. Additionally, adjustments to the **etch** chemistry or other process parameters, in addition to or instead of modification to the equipment may be made. For example, increasing the concentration of one or more **etchants** such as Freon 134a, CHF.sub.3, H.sub.2, which are known to lead to increased polymer formation may be used.

DETDESC:

DETD(29)

Thus, a method of **etching** an oxide layer has been described. Although specific embodiments, including specific equipment, parameters, methods, and materials have been described, various. . .

CLAIMS:

CLMS(1)

What is claimed is:

1. A method of **etching** an oxide layer comprising:
forming a photosensitive layer on said oxide layer which is on a substrate;
forming a first opening in said photosensitive layer to expose a portion of said oxide layer;

exposing said substrate to a **plasma**, said **plasma** **etching** said exposed portion of said oxide layer and forming a first layer on said photosensitive layer, wherein the combined thickness. . .

CLAIMS:

CLMS(3)

3. The method as described in claim 1 wherein said **plasma** is formed in a flow comprising C.sub.2 H.sub.2 F.sub.4.

CLAIMS:

CLMS(5)

5. The method as described in claim 1 wherein said **plasma** is formed using an RF power in the range of approximately 300-400 W.

CLAIMS:

CLMS(6)

6. The method as described in claim 1 wherein said **plasma** is formed between two electrodes having a spacing in the range of approximately 1.3-1.8 inches.

CLAIMS:

CLMS(7)

7. The method as described in claim 3 wherein said **plasma** is formed between two electrodes having a spacing in the range of approximately 1.3-1.8 inches.

ELECTRONIC ENGINEERING

EE TIMES®

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Issue 939 — The industry newspaper for engineers and technical management — Monday February 3, 1997

What's Hot

SYNTHESIS VENDORS RESHUFFLE
Strategic realignments in synthesis are under way. Synopsys Inc. said last week it will sell its FPGA Express through VeriBest Inc. and Synario Design Automation. That will mark the first time it has gone outside its own sales force. Exemplar Logic, meanwhile, is trying an end-run around Synopsys with ASIC-library support and an OEM agreement with Fujitsu for Leonardo, a Windows-based FPGA product. See story online at *techweb.cmp.com/eet/news/97/939news/fpga.html.*

PROCESS PROMISE FOR DENSE DRAMS
The Sematech consortium is developing a low-cost interconnect process that could extend aluminum/copper technology several generations beyond current limitations. The process fills deep via holes using only physical vapor deposition. The technology may prove a boon for 256-Mbit and denser DRAMs. Page 37.

STARTUP ROLLS SEARCH ENGINE
A new Internet search engine hits the Web today. Semio Corp. (*www.semio.com*) says its engine grabs Web URLs, indexes them and then performs a proprietary step that homes in on key concepts and categories.

HERMAN TAKES HELM AT VIEWLOGIC
Longtime chief executive officer Alain Hanover has turned over the day-to-day leadership of Viewlogic Systems Inc. to Will Herman, who adds chief executive officer to the president's title he assumed two years ago. Hanover, who has been with Viewlogic since its 1984 inception, will remain chairman until May.

CEO Will Herman

Logic analyzer sets stage for high-speed comm networks

Tektronix aims to bust measurement bottleneck plaguing digital video

Data and clocks — 250-MHz clock (internal) — Oversampler (2 GHz) — MagniVu memory — Clock edge detector and data selection — Glitch detector — Setup/hold violation detector — Trigger machine — Word and range recognizers — Timestamp generator — Memory (512K at 250 MHz)

Tek's asynchronous digital oversampling architecture, MagniVu, enables hundreds of signals to be analyzed at the highest attainable clock speeds. Story, page 4.

Battle lines drawn for fast Internet protocols

Switched setups could signal the end for the standard router

By Alexander Wolfe and Loring Wirbel

ANALYSIS

WASHINGTON – The biggest change in networking technology since routers emerged in the 1980s could catch fire at the ComNet '97 conference here this week.

The catalyst is a new generation of fast protocols that could boost Internet data-transmission speeds tenfold. Already, four networking powerhouses–Cisco, 3Com, Ipsilon and IBM–have set forth competing architectures in a bid to dominate the new technology.

"This is not a little, incremental shift," said Larry Blair, vice president of marketing at Ipsilon Networks Inc. (Palo Alto, Calif.). "It's a major disruption of everything that's going on in the industry."

Industry experts are waiting to see what happens when products implementing the new technology emerge in force later this year. (Ipsilon said it is already shipping its offering.) Experts point to shifting sands of alliances, claims and counterclaims.

"What you're seeing is architectural responses to an anticipated requirement for increased scalability and increased performance," said Martin McNealis, IP product manager at Cisco Systems Inc. (San Jose, Calif.). "Everybody knows that the Internet's got to scale and got to accommodate faster bandwidth."

The new approaches essential-

►CONTINUED ON PAGE 14

TI's fixed-point C6X hits 1,600 Mips

VLIW design takes DSPs to new high

By Martin Gold and Ashok Bindra

SHIFT TO SOFTWARE
- Advanced tools will move the focus of DSP system designs off hardware
- Programmers will need only a basic understanding of the VLIW architecture

HOUSTON – In a bold move to stake out the high ground in digital signal processing, Texas Instruments Inc. today will introduce a fixed-point DSP family based on unconventional very-long-instruction-word (VLIW) architecture.

The first device using the TMS320C6X architecture features a whopping 1,600-Mips performance and targets the high-channel-density telecom-infrastructure market.

In addition to the VLIW architecture, which enables a tenfold improvement in performance compared with today's high-end DSPs, the initial 32-bit programmable device is accompanied by design-automation tools that greatly improve C-compiler efficiency and by an assembly optimizer that could cut software-development time in half.

The tools are intended to make the C6X architecture more inviting to users. "The ability to tap into this much signal-processing performance from high-level language programs is simply without precedent," said Mike Hames, worldwide DSP manager and vice president of TI's Semiconductor Group. "These tools will shift the emphasis of DSP systems design from hardware to software," said Ray Simar, chief architect of the C6X and program manager of the Semiconductor Group's DSP operation.

For TI, the chip is a move to outdistance once again its primary competitors–Analog Devices Inc., Motorola Inc. and Lucent Technologies–all of whom are working on new DSP silicon.

The C6X platform arrives at a time when TI's mature 320C4X floating-point DSP is running out of gas and users of the well-established devices are eyeing alterna-

►CONTINUED ON PAGE 126

Engineering, medical worlds coalesce on chip-implant experiments

A heady proposition

First of two parts
By Larry Lange

STANFORD, CALIF. – It was only 30 years ago that sci-fi author Philip K. Dick wrote the short story "We Can Get It For You Wholesale," but little could he have known how swiftly real-world technologies would make his fantastic scenario almost true today. The story, which became the basis for the movie *Total Recall*, centered on embedding signal-controlled microprocessors in miniature devices and surgically implanting them in the human cerebral cortex, where thought and language are processed. Or, to make it a sound bite: Arnold Schwarzenegger gets a chip in his brain.

How close are we? *EE Times*'s look into the state of the art suggests the mix of electrical engineering and medical technologies to do *Total Recall* for real is here, being funded, researched and experimented with. Implant work on human eyes and ears, and animal brains, has been conducted by Stanford University, MIT and companies. And human brain-implant

►CONTINUED ON PAGE 20

Copy-protection questions delay digital rollouts

By Junko Yoshida

SAN JOSE, CALIF. – The lack of a secure mechanism for digital transport of copyrighted content is stalling the rollout of a host of next-generation consumer-electronics devices, from DVD to digital VHS (D-VHS) and digital video-cassette (DVC) recorders.

Absent an acceptably secure transport scheme, movie studios have been loath to open their film vaults to the new technologies, forcing manufacturers to shelve completed systems. And none of the consumer devices developed thus far has fully exploited the IEEE-1394 serial interface, in ef-

►CONTINUED ON PAGE 124

TECHNOLOGY

More-uniform fill extends life of a standard metal interconnect

Al hits sub-0.25 micron vias

By Gail Robinson

AUSTIN, TEXAS – A novel, low-cost interconnect process being developed here by Sematech may make it possible to extend aluminum/copper deposition technology several generations beyond its current limitations.

By combining pressure and moderate heat–below 450°C–with existing technology, researchers were able to fill deep via holes using only physical vapor deposition (PVD). They recently fabricated completely filled sub-half-micron interconnect aluminum plugs of high aspect ratio–up to 4:1.

With the ability to move to 0.25 micron and a strong likelihood of reaching 0.18 micron, the technology may prove a boon for ICs based on three-level processes, such as 256-Mbit and denser DRAMs. Scientists from the Sematech manufacturing consortium are working with a team at Varian Associates (Palo Alto, Calif.) on the project.

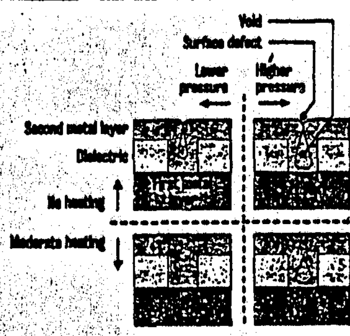
"In the DRAM sector, aluminum is the number-one goal to implement for production," said Max Biberger, a researcher at Varian. "So the process has a great future, because everyone wants to do aluminum."

The results, presented at the International Electron Devices Meeting last December, target the problems of using PVD to fill very deep via holes and trenches. When the aspect ratio exceeds 4:1 or 5:1, conventional PVD-sputtered aluminum, by its nature, has difficulty getting good step coverage. The seemingly inherent problems have led many manufacturers to plan a move to chemical vapor deposition (CVD), which would require high development outlays.

However, the Sematech/Varian project shows that making the aluminum flow like a liquid overcomes several PVD limitations, allowing for the deep trenches that are necessary for sub-half-micron technology.

"An analogy would be what phase-shift masks did for lithography," said Biberger. "We are extending what is already there to beyond where people thought they could take it."

Typically, when aluminum is sputtered on a substrate, it makes contact as a solid and the via is covered in such a way that uniform step coverage is not achieved. Experiments in sputtering the alu-



minum at elevated temperatures showed that under the right conditions, the metal could flow.

"Basically, the process reflows the aluminum into the hole, giving a flat surface, and nothing special is done to planarize it," said Peter (P.K.) Vasudev, a senior fellow and director of strategic technology at Sematech. "Normally, when you sputter, you end up with a little divot or a bump where the via was. With the reflow, the surface tension pulls it flat."

The work could be crucial for IC development in memory and logic devices, Vasudev said. One way to improve the speed of a logic device is to reduce the resistivity of the material, such as going from tungsten to aluminum, which has a lower resistivity. Going from aluminum to copper improves the speed by at least 30 percent.

Since signal delay is directly proportional to both resistance and capacitance, the short-term remedy giving the best performance boost has been to reduce the capacitance of the interlayer dielectric. By changing from standard oxides with dielectric constants of 4 to low-k dielectrics with dielectric constants down to 2 to 2 1/2, the efficiency of the interconnect can be improved as much as 70 or 80 percent.

To attack the metal-interconnect problem directly, the project

▶CONTINUED ON PAGE 42

Associative chip drives image board

By Glenda Derman

RAANANA, ISRAEL – Associative processing–the technique of providing memory access based on content, rather than on address computation–is a mature concept whose complexity and cost have kept it out of the mainstream. The chip architects at Associated Computing Ltd. (ACL) are among those hoping to change that, in ACL's case with a second-generation associative processor that is claimed to perform 3 billion search operations per second, peak, for enhanced cost/performance in electronic imaging applications.

Capable of simultaneous input, output and processing, the Xium-2 chip contains 2,048 simple processing elements working in parallel, each with 128 intelligent bits that can perform read, write and compare operations. ACL presented a machine-vision board based on the architecture in December at the International Technical Exhibition on Image Technology, held in Japan. The development adds to the growing ranks of associative processing-based products (see Aug. 26, page 43).

The notion of linking memory access to content to perform sequences of "search for and modify" operations is roughly 50 years old. But the memory design is complex, requiring the integration of additional logic with each cell, and

ACL'S PROCESSOR
- Performs parallel match operation in one cycle for a 3-Bops throughput
- Targets demanding image-recognition applications

the cost involved in developing and establishing a new chip architecture has been prohibitive.

ACL's processor uses a new memory cell consisting of a standard memory and two to five transistors for logic. Based on a "compare" operation, the processing approach requests identification of a value and a write operation, which stores the new content. When a search condition is established and broadcast to all cells, each cell of Associated Computing's chip, operating in parallel, uses its processing logic

▶CONTINUED ON PAGE 40

Tech Files

Carbon aerogel leads to supercapacitors

DUBLIN, CALIF. – An electronic application for a class of materials known as aerogels is being put into practice here at Polystor Corp., which just introduced a high-performance carbon-aerogel capacitor.

Called an aerocapacitor, the component can deliver 4,000 W/k of weight due to the high surface area per volume of the aerogel. Along with a high charge/discharge rate, the supercapacitor has an energy density close to that of batteries, thus promising new application areas. The aerocapacitors fit the footprint of AA batteries and charge in the same 2.5- to 4-V range.

The carbon aerogel was developed at Lawrence Livermore National Laboratory. Polystor extended that research by finding a cost-effective manufacturing method for producing it, according to the company.

Aerogels are essentially materials with a large number of air bubbles that dramatically increase their effective surface area; for example, 4 cm^2 of aerogel material has the same surface area as a football field. That characteristic explains the high charge density of the material.

Polystor is offering aerocapacitor-evaluation kits to OEMs.

PolySi R&D looks to large-area circuits

REDHILL, ENGLAND – Processing techniques being tried at Philips Research Laboratories here are producing polysilicon thin-film-transistor characteristics that rival single-crystal silicon in quality. That holds out prospects for building large-area electronic circuits with fairly complex functions.

The work has integrated a 16 x 16 array of polysilicon E^2PROM transistors with thin-film FETs on a glass substrate. The process temperature for the circuit was low enough to permit fabrication of the devices on a plastic substrate. Once in production, the process could result in plastic smart cards that could not only retain and process data but also display it and link with wireless networks.

Imager gives glimpse into photosynthesis

BERKELEY, CALIF. – An ultrafast imaging technique devised at the University of California is yielding insight into the chemical-optical-electronic behavior underlying the photosynthetic process. Observations of the electronic response of ruthenium metal complexes following the absorption of a photon were obtained over a 300-fs interval. The extremely fast dynamics of the metal complexes resemble biological processes.

The information fits no existing models of how the systems transform light into chemical energy, hinting at a new understanding. Better models could aid research into harnessing photosynthetic processes for photovoltaics and high-speed optoelectronic devices.

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Al process fills 0.25-micron vias

▶CONTINUED FROM PAGE 37

targeted low-pressure sputtering, modifying the heating of the wafer and cleaning up the entire system to remove gaseous and metal impurities.

A few years ago, Varian developed a two-step planarization process that, in terms of thermal budget, allowed for lower temperature. But even that temperature was too high for low-k dielectrics, and the fill capabilities were not adequate for vias with a higher aspect ratio—the bottom width vs. the oxide thickness of the vias. The process stopped at an aspect ratio of 2 1/2 or 3.

Exploring modifications, the researchers came up with a low-pressure deposition technique. In a PVD sputter system, the pressure is usually in the range of 2 to 5 millitorr. But at that level, the mean free path—the flight path of a sputtered aluminum or titanium atom—is relatively short, because it collides with other gas atoms. Consequently, the direct line of sight is disturbed because the pressure is too high.

The goal was pressures below 0.8 millitorr, which would allow a mean free path at least as long as the distance from the target to the wafer surface. Modifying the sputter source and adding ring magnets allowed for equilibrium sputter pressures of approximately 0.65 millitorr. The result is a mean free path much longer than the distance between target surface and wafer.

"Now we have an assurance that the atom that comes off the target surface truly has a line of sight directly down to the wafer," said Vasudev. "We get a very directional deposition. That in itself allows us to fill the relatively high via holes required for high-end logic devices."

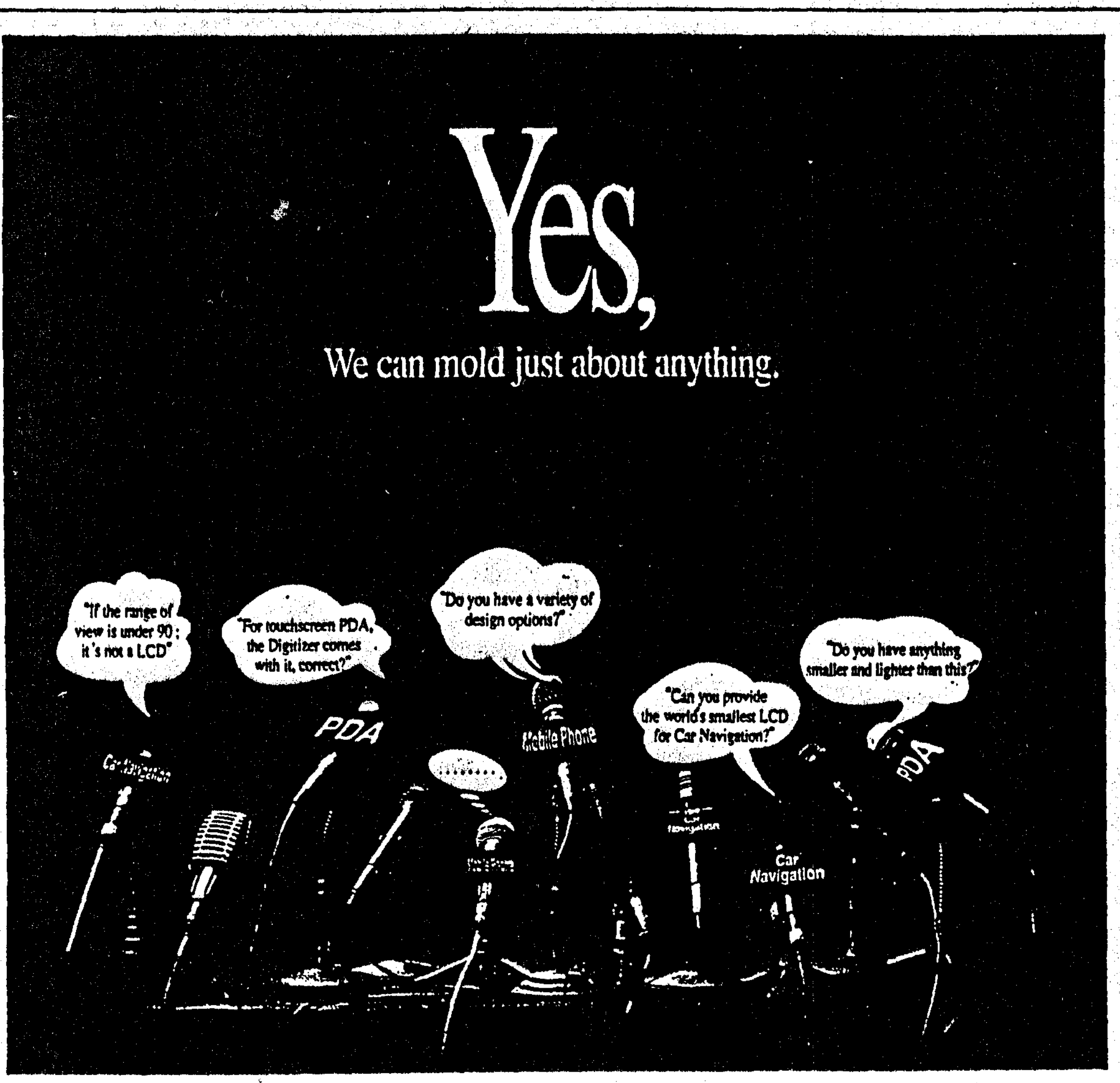
Key factor

Another key factor was developing a new heating method for the wafer. About 15 years ago, Varian devised the so-called "backside argon" heating method, in which gaskets introduced under the wafer created a gas cushion behind it with a pressure above 1 torr. In this case, the thermal conductance of the gas was high enough to heat a wafer by thermal conductivity.

"Radiation heating is a lot gentler than backside argon, which reaches the plateau temperature within 60 seconds," said Biberger. "Radiation heating can take up 2 minutes."

Also, cold aluminum doesn't move around as fast as hot or warm aluminum, and the initial sputter process occurs on a cold wafer. The aluminum strikes the wafer vertically, offering an immediate processing advantage because it makes a coating inside the hole. "It fills up the hole nicely," said Biberger. "Only at the end of the process, as the temperature reaches its maximum, does the diffusion of aluminum atoms fill the hole completely."

While the work was proven on a Varian system, it can be extended to any system currently used in IC production. Since many companies have several PVD systems in their manufacturing lines, the researchers expect to see people retrofit their systems to reproduce this process. "We assume that some companies will probably push it all the way into manufacturing," said Biberger, who expects the trend to first go to logic with aluminum and standard oxide and, initially, subtractive etch. "We expect to see the same trend in DRAMs, but with a time lag of one generation," he said. He also foresees combining PVD aluminum with CVD aluminum at some point, as well as extending it to copper, further extending the process to smaller features.



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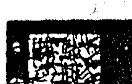

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#22

Selective dry etching in a high density plasma for 0.5 μm complementary metal–oxide–semiconductor technology

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(Received 6 August 1993; accepted 7 October 1993)

0.5 μm complementary metal–oxide–semiconductor structures were utilized to investigate the selective nature of a high density plasma reactor. The formation of borderless contacts and local interconnects by the selective etch stop film approach was discussed and shown to be affected by topography, planarization, and nonuniformities. A factorial design of experiments determined the optimum conditions of the selective oxide etch chemistry. The resulting etch chemistry was characterized by measurable quantities such as an oxide etch rate of 1200 nm/min, a patterned (0.5 μm image) etch-rate ratio for oxide:nitride >100:1 and 5%-3σ uniformity. And, finally, an integrated *in situ* oxide etch/resist strip/nitride etch was presented.

I. INTRODUCTION

The reduced cell size of static random access memory (SRAM) and desired enhancements in logic performance necessitate the use of borderless contacts and local interconnects in very high performance 0.5 μm complementary metal–oxide–semiconductor (CMOS) technologies. After device fabrication, local interconnects and borderless contacts can be formed simultaneously using a tungsten damascene stud process.[1] One such approach utilizes a silicon nitride film (as an etch stop) coupled with a highly selective oxide:nitride etch chemistry. Using a plasma enhanced chemical vapor deposition (PECVD) for the nitride film provides a low temperature ($T_{max} \approx 600\,°C$) metallization scheme with its inherent advantages.[2]

The key to the etch stop approach is the use of a selective oxide:nitride etch process. This selective etch is difficult to achieve since both materials behave similarly. Oxide selectivities have been obtained by combining polymer deposition and high ion bombardment.[3,4] However, in conventional reactive ion etch (RIE) and magnetically enhanced RIE (MERIE) reactors, the control of polymer deposition and ion bombardment energy is limited. Thus, the etch process is marginal for both maintaining selectivity to nitride and sustaining the oxide etch rate.

This article presents the etch process window for a selective oxide: nitride etch chemistry which could be used for the above application. Experiments were performed using realistic semiconductor structures (0.5 μm feature sizes) utilizing a PECVD nitride film as the etch stop layer. All experiments were done in a high density plasma (HDP) etch system and correlations between the HDP conditions and etching characteristics are presented.

II. EXPERIMENT

The experiments for this study were processed in a HDP chamber schematically shown in Fig. 1. The plasma source region of the process chamber is a nonresonant, multiple turn antenna wound around a quartz cylinder. The antenna is capable of delivering up to 3000 W of rf power to the chamber to generate a very high plasma density. The biased electrode is used to extract ions from the plasma. A rf bias voltage, coupled through a solid state matching network, as is the source voltage, is capacitively coupled to the wafer to control ion energy. In addition to being operated "off resonance," this configuration improves upon established helical resonator technology with the inclusion of a top electrode in the source region. This electrode provides a large area dc grounded reference for the plasma which minimizes the likelihood of chamber wall sputtering and provides for a stable discharge over a wide range of operating conditions. The chamber is pumped using a 600 ℓ/s turbomolecular pump allowing the process to operate at <10 mTorr. Ion densities in excess of $1E12$ have been recorded using Langmuir probe techniques to measure an argon plasma discharge at a pressure of 10 mTorr with a source power of 2500 W.[5]

III. RESULTS AND DISCUSSION

A. Borderless contact process window

The implementation of borderless contacts/local interconnects requires a determination of the process window. The silicon nitride etch stop approach has been evaluated with the basis of the analysis being the selectivity calculation, i.e., etch-rate ratio (ERR). The feasibility of this approach relies on the following two ERRs:

(1) selectively etching oxide insulator layer to nitride film;
(2) selectively etching nitride film to silicon and oxide.

These two etches are performed in succession, respectively. Intuitively, the selectivity required for etching oxide to nitride is inversely proportional to the nitride thickness, whereas, the selectivity needed for etching nitride to silicon and oxide is proportional to the nitride thickness. As one can infer, the silicon nitride etch stop thickness must be optimized based on the empirical results of the selective etch chemistries. For this article, we shall concentrate on the selective etching of oxide to nitride in our calculations.

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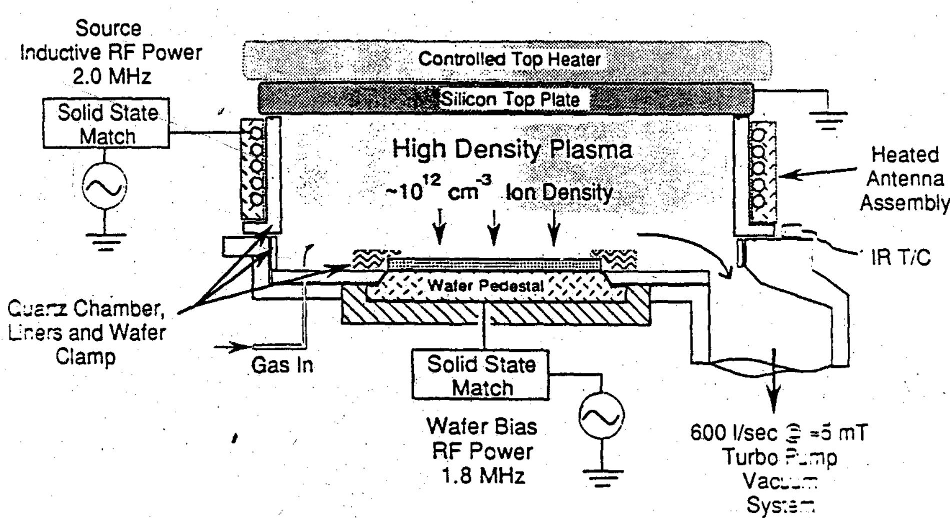

FIG. 1. Schematic of the high density plasma reactor used for this study.

When analyzing the etch stop process, the first factor to be considered is the degree of functionality offered to the technology. In other words, what type of contact or interconnect is to be made? Will the contact be bordered (protective spacing added) or borderless (eliminates critical lithographic alignment) to the gate and/or device isolation? The most difficult application is the source/drain contact which is borderless to the gate. This particular contact is permitted to land on the gate structure, but remain electrically isolated from the gate, while making electrical connection to the source and drain. A contact that is borderless to the gate contact demands the largest ERR. Figure 2 depicts the borderless to gate (a) and borderless to diffusion (b) contacts.

After examining the process functionality, one must evaluate the process steps and their relationship to the ERR calculation. The important parameters to consider are the device topography and tolerance, nitride thickness and tolerance, insulator thickness and tolerance, percent planarization, and percent overetch and etch tolerance. A statistical analysis of the 3-σ process window is depicted in Figs. 3, 5, and 6.

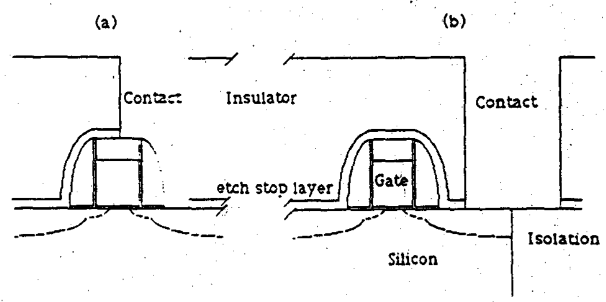

FIG. 2. Schematic of the physical cross sections for a borderless to gate (a) contact and a borderless to diffusion (b) contact.

Figure 3 shows the effect of etch stop thickness on the selectivity required for the borderless contact. This calculation has assumed a gate stack of 5500 and 8250 Å of insulator. The significance of the graph is the inverse relationship of the ERR to nitride film thickness and the dramatic effect of planarization on the required selectivity. The inverse ERR relationship is a critical parameter for integration concerns. When removing the nitride etch stop, minimizing the removal of device isolation oxide is the main objective. One obvious technique is to thin the etch stop thickness for a given nitride etch process thus moving the oxide loss distribution to lower values. However, the generation of large, controllable oxide:nitride selectivities is very difficult in conventional RIE and MERIE systems.[6] Therefore, a realistic

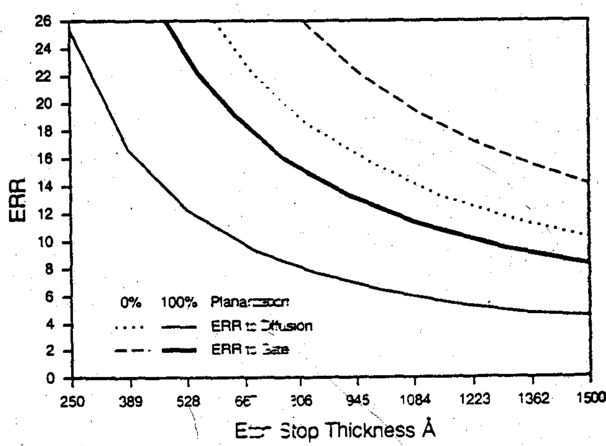

FIG. 3. Graph of the ERR as a function of the etch-stop layer thickness. Depicted in this figure is the inverse relationship of the ERR to nitride film thickness and the dramatic effect of planarization on the required selectivity. The calculation has assumed a stack height of 5500 and 8250 Å of insulator.

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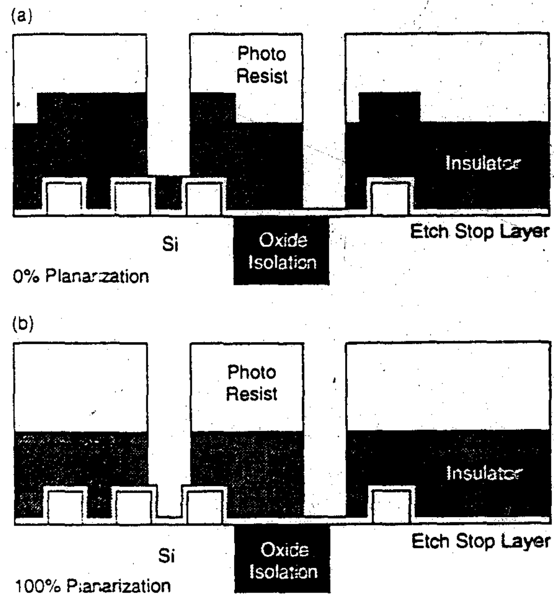

FIG. 4. Illustration of the effect of planarization. Planarization removes the insulator thickness differences between dense and isolated structures.

evaluation of the overall process window must account for both oxide:nitride selectivity and subsequent device isolation loss. (The process must minimize nitride remaining after the oxide etch and minimize nitride overetch in the nitride etch.)

Also shown in Fig. 3 is the dramatic effect of planarization on the required selectivity. Planarization produces a significant reduction in the ERR requirement and opens the process window to allow for a decrease in the etch stop thickness. This improvement is accomplished by reducing the oxide thickness differences between highly dense semiconductor devices and isolated structures which in turn reduces the amount of overetch on the nitride film in the isolated areas thus decreasing the necessary selectivity. Figure 4 illustrates the effect of planarization.

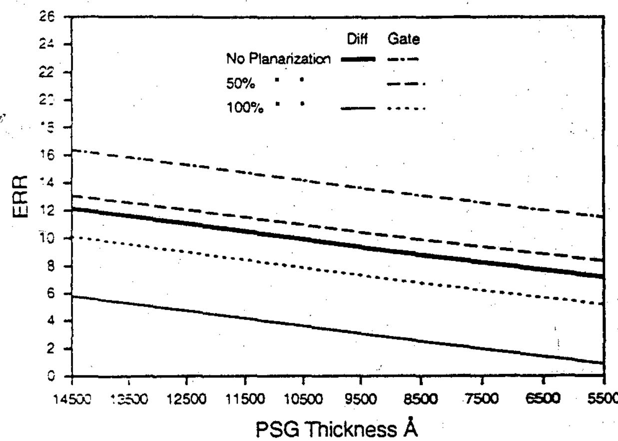

FIG. 5. This graph of the ERR vs the PSG (insulator) thickness shows a linear dependence as calculated. This is a direct result of selectivity being proportional to the tolerances (nonuniformities) of the process. A 1500 Å etch stop film and 5500 Å stack height are assumed.

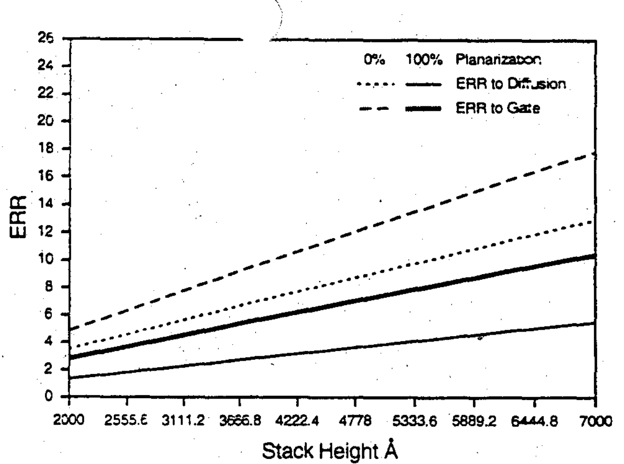

FIG. 6. The ERR as a function of the underlying stack height (gate topography). The selectivity necessary to fabricate borderless contacts is proportional to the gate topography. The analysis assumed a 1500 Å nitride film and PSG thickness given by 1.5× the stack height.

Figure 5 shows the ERR as a function of insulator thickness. IBM uses phosphosilicate glass (PSG) as the insulator. A 1500 Å etch stop film and 5500 Å gate stack are assumed. The graph presents the linear dependence of the selectivity on the PSG thickness. (The ERR is also proportional to the tolerances of the overall process.) From this graph, one can see the need to optimize the PSG thickness for a reduction in the selectivity requirement. Also shown again is the improvement in process margin afforded by planarization.

The relationship of selectivity and gate stack topography is shown in Fig. 6. The analysis assumed a 1500 Å nitride film and PSG thickness given by 1.5× the stack height. The significance of the graph is that the selectivity necessary to fabricate the borderless contacts is proportional to the gate topography. Also, with increasing topography, planarization provides a large reduction in the ERR requirements of the process.

From the preceding analysis, the relationships between insulator thickness, etch stop thickness, and gate stack height and the required ERR were revealed. Optimization of these parameters, coupled with planarization, provides an enlargement of the process window for the selective etch chemistry and reduction in the ERR. Conversely, utilization of a highly

TABLE I. Oxide etch process trend summary. A dash means parameter is not function of change in process variable.

Parameters	Oxide ER	Nitride ER	Profile	μ loading
C_2F_6 flow	↗	↑	—	↘
Pressure	↗	↗	More taper	↗
Source power	↘	↓	More vertical	↘
Bias power	↑	↗	More vertical	↗
Si top plate temperature	↗	↓	—	—

TABLE II. Oxide and nitride etch comparison.

	Conventional RIE	HDP etch
Oxide etch rate (4 wt % PSG)	4000 Å/min	12 000 Å/min
Selectivity (PSG: nitride) (Meas. 0.5 μm hole)	8.1	100:1
Uniformity	9%-3sigma	5%-3sigma
Critical dimension slope	86–88 deg	88–90 deg
Nitride etch rate (PECVD nitride)	500 Å/min	2500 Å/min
Selectivity (Blanket) (Nitride: TEOS)	3:1	7:1[a]
Uniformity	6%-1sigma	15%-1sigma[a]

[a]Preliminary results.

selective oxide etch would increase the processing latitude for each of these parameters.

B. HDP oxide etch

The key to generating a highly selective oxide:nitride etch is the reduction of fluorine in the polymer by-product generated during the etch process. This has been accomplished by using a heated Si top plate and a high C:F ratio fluorocarbon in the HDP reactor.[5]

A computer aided design of experiments was performed to characterize the HDP process parameters. The experiments consisted of two matrices comprising a two level fractional factorial with four factors and one center point each. The five variables studied were: C_2F_6 flow, pressure, source power, bias power, and Si top-plate temperature. The measured responses were: oxide etch rate, nitride etch rate, profile angle, and microloading. Oxide and nitride wafers patterned with a deep ultraviolet (UV) resist at 0.5 μm dimensions were used as monitors. Etch rates were determined by scanning electron microscopy (SEM) cross-sectional measurements in 0.5 μm structures on 200 mm wafers.

Table I provides a summary of the trends generated by the factorial experiments. The C_2F_6 flow, and source power are shown to have a strong effect on the nitride etch rate, while

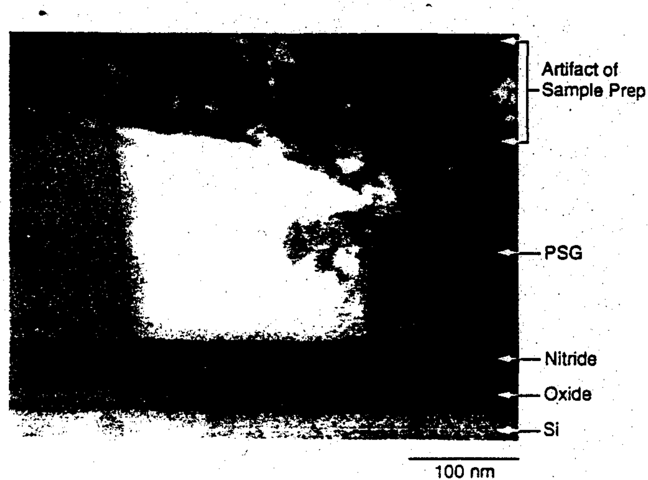

FIG. 7. Cross-sectional TEM micrograph depicting the selectivity of the HDP oxide etch process. The empirical selectivity of PSG (4 wt %) to PECVD nitride was determined to be greater than 100:1.

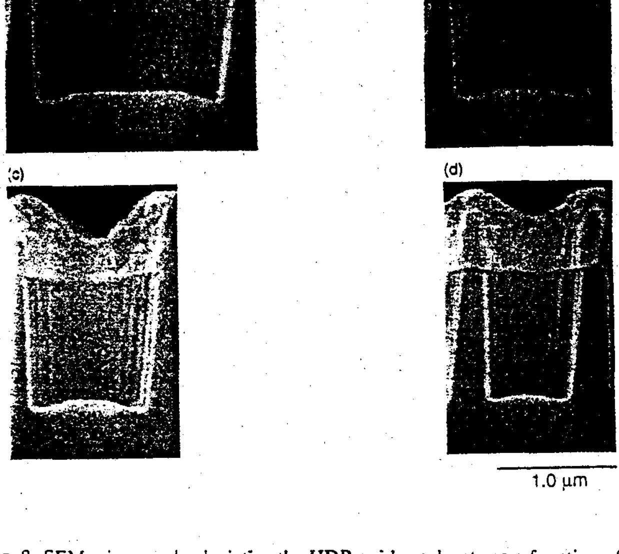

FIG. 8. SEM micrographs depicting the HDP oxide etch rate as a function of contact image size. The etch rate is constant for all image sizes (smallest feature=0.5 μm).

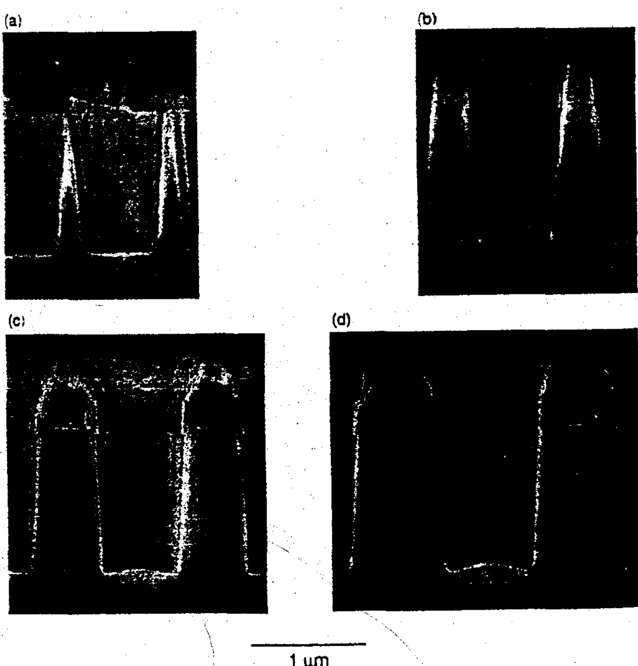

FIG. 9. The oxide etch rate is shown to be constant with variable spacing between contacts. The SEM micrographs also show that enhanced resist sputtering can occur with minimal image spacing.

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the oxide etch rate is very sensitive to changes in the bias power. Using the results of the matrix, the process was optimized for the measured responses. The resultant conditions were

35 sccm C_2F_6, 4 mTorr, 2700 W source,

1400 W bias, 250 °C.

Table II presents the measured properties of the optimized HDP oxide etch process as compared to conventional RIE/MERIE. Readily seen from this data are the improvements in oxide etch rate, selectivity, uniformity, and anisotropy.

Figure 7 is a transmission electron microscopy (TEM) cross section of a patterned structure which has been etched with the optimized conditions. The PSG (4 wt % phosphorus) has been etched down to the PECVD (480 °C deposition process) silicon nitride. The nitride was subjected to 100% overetch and exhibited ≈125 Å loss. A conservative estimate of the selectivity (PSG etch divided by nitride etch rate) yields 100:1. The selectivity is conservative because it is independent of the overetch. An initial material loss no etch rate is observed on the nitride film. After the etch clears the PSG and exposes the nitride, the nitride initially etches but this process is rapidly terminated as deposition of the carbon rich polymer begins on the nitride.

The effect of pattern factor on microloading is shown in the scanning electron microscopy (SEM) cross sections of Figs. 8 and 9. This experiment also used the optimized etch process. Figure 8 presents microloading as a function of variable contact size. No degradation in the etch rate is observed with the decreasing contact diameter (smallest feature=0.5 μm). Figure 9 shows that the HDP etch rate does not change with variable spacing between images. However, at very small spacing, the resist experiences enhanced sputtering. This is a geometric phenomenon stemming from the resist having a triangular profile rather than the expected rectangular shape. The scalloping depicted in the micrographs is currently being investigated. The microloading results are in agreement with earlier work.

TABLE III. Nitride process trend summary. A dash means nitride ER≠f(CO_2 pressure).

Parameters	Nitride ER	Oxide ER	Profile
CH_3F	↘	↗	More taper
CO_2	↘	↓	
Pressure	—	↘	More taper
Source	↗	↘	
Bias	↘	↗	

C. HDP nitride etch

In order to examine the feasibility of etching nitride selectively to oxide, a two level fractional factorial with five factors and one center point was performed. The five variables studied were: CH_3F flow, CO_2 flow, pressure, source power, and bias power. The measured responses were nitride etch rate, oxide etch rate, and profile angle. Unpatterned oxide and nitride wafers were used as planar etch rate monitors. The oxide film was an undensified low-pressure chemical vapor deposition (LPCVD) tetraethylorthosilicate (TEOS) and the nitride was deposited by PECVD (480 °C process). Nitride wafers patterned with a deep-UV resist at 0.5 μm dimensions were used as profile monitors. Etch rates were determined by spectral reflectivity measurements on the 200 mm wafer surfaces.

Table III provides a summary of the trends generated by the factorial experiment. The CO_2 flow is shown to have a strong effect on the oxide etch rate, while the oxide etch rate is very sensitive to changes in the bias power. The results of the matrix revealed a process which selectively etched nitride to oxide with a ratio of 7:1. The resultant conditions were

34 sccm CH_3F, 92 sccm CO_2, 25 mTorr,

2700 W source, 150 W bias.

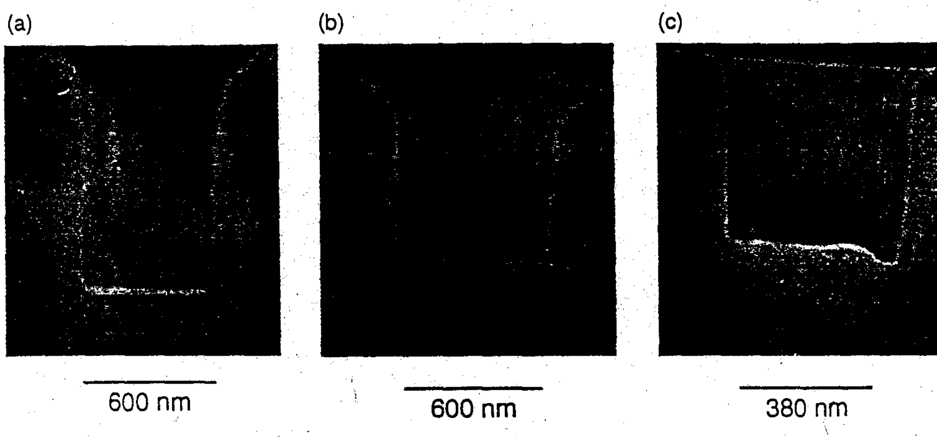

FIG. 10. SEM micrographs showing the HDP *in situ* process flow. (a) The oxide etch removes the insulator and selectively stops on the nitride layer. (b) The polymer generated at the bottom of the contact and the remaining resist are removed by an O_2 plasma. (c) The nitride etch stop is etched selectively to the underlying silicide and oxide isolation.

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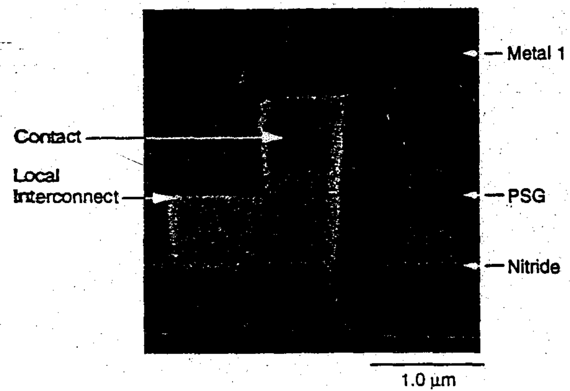

FIG. 11. SEM cross section of a local interconnect borderless to the device isolation. The interconnect is wired to the metal 1 layer thru a contact stud.

More experiments examining the process and patterned selectivity are in progress. The preliminary results for this process are shown in Table II.

The significance of the cursory nitride evaluation is that an integrated, highly selective, *in situ* etch solution was now possible. Figure 10 is a sequence of SEM micrographs showing the HDP *in situ* process flow. The sequence of processes within the HDP reactor are shown to be the following.

(a) The oxide etch removes the insulator and selectively stops on the nitride etch stop layer.

(b) The polymer generated at the bottom of the contact and the remaining resist are removed by an O_2 plasma.

(c) The nitride layer is etched selectively to the underlying silicide and oxide isolation. The dip shown in the bottom right corner of the micrograph is the materials interface between the device silicon and the planarized oxide isolation.

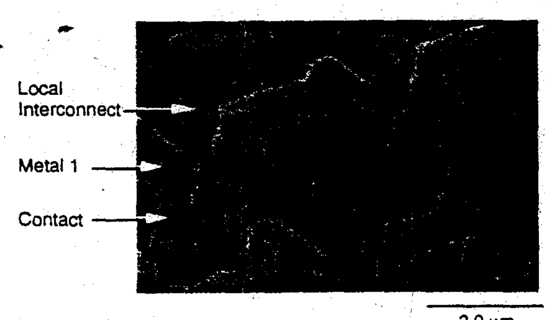

FIG. 12. SRAM wiring is shown in this SEM micrograph. Extensive local interconnect usage is apparent. The passivating and insulating layers have been removed by sample preparation.

TABLE IV. Electrical improvements for HDP over conventional RIE.

Parameter	Improvement	Physical correlation
Junction leakage	10×[a]	Silicide damage isolation loss
R_s[b]	33%[a]	CD control
Contact resistance	25%[a]	Silicide damage CD control

[a]Distribution tails reduced.
[b]Sheet resistance.

The discontinuity is due to device processing and not the result of plasma etch trenching.

D. Electrical characterization

The HDP selective oxide etch was utilized as part of the tungsten damascene stud process for contact and interconnect formation. Figures 11 and 12 are SEM micrographs depicting typical W interconnect structures. The electrical data for the HDP oxide etch is compared to conventional RIE results in Table IV. The highly selective nature of the HDP process caused less silicide damage and isolation loss which translated into a 10X improvement in diffusion junction leakage for the borderless contacts. Improvements in etch uniformity and contact profile were electrically characterized by reductions in sheet resistance and contact resistance. The full benefit of the HDP process cannot be realized until both the oxide and nitride are removed in this reactor.

IV. SUMMARY

0.5 μm CMOS structures were utilized to investigate the selective nature of a high density plasma (HDP) reactor. The formation of borderless contacts and local interconnects by the selective etch stop film approach was discussed and shown to be affected by topography, planarization, and nonuniformities. A factorial design of experiments determined the optimum conditions of the selective oxide etch chemistry. The resulting etch chemistry was characterized by measurable quantities such as an oxide etch rate of 1200 nm/min, an ERR for oxide:nitride>100:1, and 5%-3σ uniformity. And finally, an integrated *in situ* oxide etch/resist strip nitride etch was presented.

[1]C. Kaanta *et al.*, IEDM Tech. Dig. **1987**, 209.
[2]F. White *et al.*, IEDM Tech. Dig. **1992**, 302.
[3]J. W. Butterbaugh, D. C. Gray, and H. H. Sawin, J. Vac. Sci. Technol. B **9**, 1461 (1991).
[4]N. Ikegami *et al.*, Jpn. J. Appl. Phys. **31**, 2020 (1992).
[5]J. Marks *et al.*, Proc. SPIE, 1803 (1992).
[6]P. Burke, D. Garner, and J. Givens, IBM Internal Publication, 1991.
[7]M. Armacost and J. Marks, J. Electrochem. Soc. (in press).

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#24

Hafnium dioxide etch-stop layer for phase-shifting masks

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Phase-shift masks were prepared using sputter deposited films for the phase-shift layer and etch stop layer on fused quartz silica substrates. It has been found that the combination of SiO_2 for the phase-shift layer and HfO_2 for the etch-stop layer offers a unique combination of properties advantageous for the preparation of phase-shift masks. The optical transmission properties of HfO_2 layers with or without a SiO_2 phase-shifting layer on quartz substrates are presented.

The use of the phase shift approach to increase the resolution of lithography has been reported.[1–4] Several methods have been reported for obtaining the 180° optical phase-shift pattern. Etching into the surface of the quartz plate has a number of advantages but requires great care in etching uniformly to the correct depth. Spin-on-glass layers have also been reported. These require special thermal processing to achieve the desired properties. We have investigated the use of sputtered films of SiO_2. In order to etch the phase-shift layer without etching the quartz substrates, an etch-stop layer is necessary. Al_2O_3 (Ref. 5) has been recommended as an etch-stop layer because it has good optical transmission at *i* line and in the deep UV, and it also has good etch selectively for the SiO_2 phase-shift layer. We have found that it is difficult to produce Al_2O_3 films that are resistant to typical chemical cleaning process (e.g., 4:1 H_2SO_4: H_2O_2 at 90 °C). Also the films are typically highly stressed, which is very undesirable for the phase-shift mask (PSM) application due to the high level of flatness required of the substrates. Although methods can be found to produce high-quality films,[6] alternative materials were sought for this application. We have reviewed the literature and found that HfO_2 films have good UV transmission properties and are difficult to etch. Since the other properties of HfO_2 films are not well known, it is of interest to study them and to determine whether HfO_2 films are good etch-stop layers for PSMs.

We then discovered that HfO_2 films not only have good optical transmission at *i* line and deep UV, good etch selectivity with the SiO_2 phase-shifting layer, low film stress on quartz substrates, but are also not attacked by the chemical cleaning solution at 90 °C. The HfO_2 films were deposited by a rf sputtering process. The sputtering system was evacuated to less than 10^{-7} Torr by a turbomolecular pump prior to the introduction of the argon–oxygen gas mixture. 5 in.^{2} fused silica plates were used as substrates and were mounted on a water-cooled 8 in. diam plate. During the deposition input power was between 200 and 400 W. Argon–oxygen gas mixture was used, and the total pressure was 5 mTorr. The oxygen content in the sputtering gas was ~10%; oxygen contents as high as 40% have been used with no significant effects on deposited films. After deposition, thicknesses were determined by a Tencor Alpha-step Profilometer. Films were grown with thicknesses varying from ~50 to 105 nm. For some of the samples, SiO_2 phase-shifting layers were deposited on top of some HfO_2 films for the study of their optical properties. Optical transmission was measured using a Varian DMS-

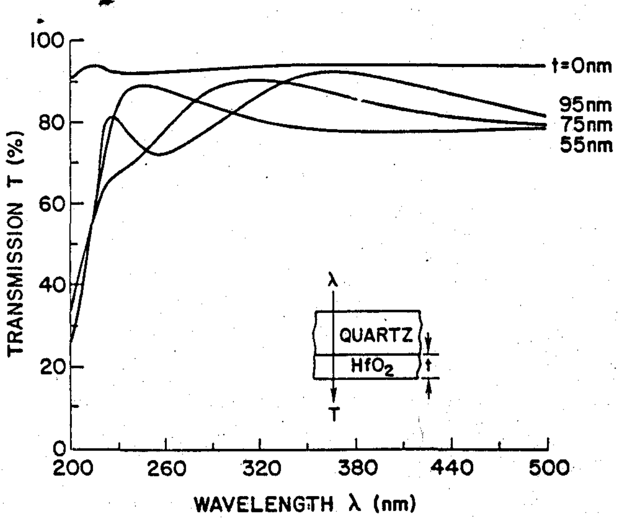

FIG. 1. Optical transmission of HfO_2 films with different thickness on fused quartz substrates.

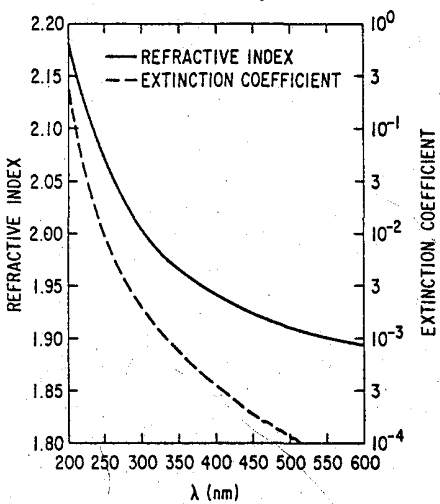

FIG. 2. Refractive index of HfO_2 on quartz substrates between 200 and 600 nm.

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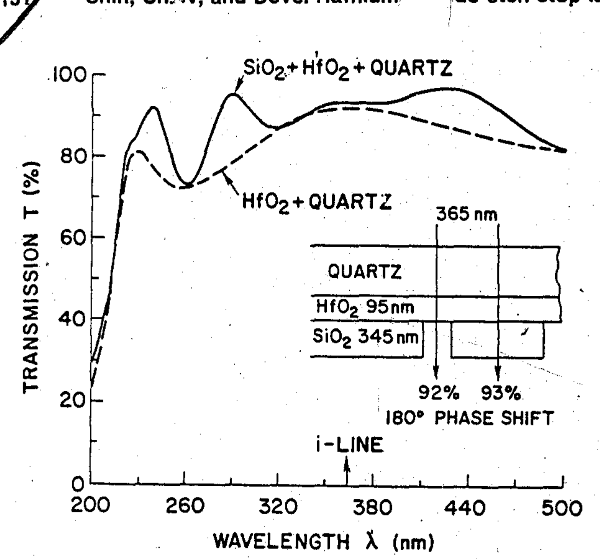

FIG. 3. Optical transmission spectra of a PSM designed for an *i*-line (365 nm) stepper.

FIG. 4. Optical transmission spectra of a PSM designed for a deep-UV (248 nm) stepper.

200 UV visible spectrophotometer. The film stress was measured by observing interference fringes between the surface of the silica plate and an optical flat plate before and after film deposition.

The stress of HfO_2 films is sufficiently low that no more than two fringes between the coated substrates and the optical flat plate was observed. The HfO_2 film etch rate was evaluated using reactive ion etching (RIE) employed for patterning the SiO_2 layer. We tested the etch rate on a Plasma-Therm RIE system using CHF_3 gas at 100 W power and 50–100 mTorr pressure. A series of runs was carried out to determine the optimum SiO_2 etching conditions. It was found that the ratio of etch rate for HfO_2 to SiO_2 is better than 1 to 16. These results of etch studies will be reported in detail in another article.[7]

The transparency of HfO_2 films deposited on quartz substrates was measured from 200 to 500 nm as a function of film thickness, and the results are shown in Fig. 1. As shown in Fig. 1, for *i*-line application, a film with a thickness of $\sim$95 nm had an optical transmission of $\sim$92% at 365 nm. With decreasing thickness, the peak shifts to lower wavelength. The optical transmission is $\sim$89% at 248 nm at a film thickness of $\sim$55 nm.

The refractive index and extinction coefficient of films on quartz between 200 and 600 nm were calculated using a computer fit to the optical transmission curves for the given thickness of the films. The results are shown in Fig. 2.

Figure 3 shows the measured optical transmission spectra of a PSM designed for an *i*-line stepper. The thickness of the etch-stop layer was $\sim$95 nm and that of the phase-shifting layer was $\sim$345 nm. A small transparency difference of $\sim$1% was observed. Figure 4 shows the measured optical transmission spectra of a PSM designed for deep UV at 248 nm. In this case, the thickness of the etch-stop layer is $\sim$55 nm and the phase-shifting layer $\sim$215 nm. Also, there is a small difference between the transmission with and without the SiO_2 layer at 248 nm. We have made a series of PSMs using these materials with etched patterns on 5 and 6 in.[2] quartz substrates. Details of design and fabrication of these masks will be published later.[7]

In summary, we have found that HfO_2 films can be used as etch-stop layers for PSMs. The films have good optical transmission at 365 and 248 nm and high etching selectively compared to SiO_2 film. This material also is chemically stable and not attacked by chemical cleaning solutions. In general, the sputtered HfO_2 films have been found to be very reproducible and are easily prepared in the chemically resistant, low stress condition.

[1]M. D. Levenson, N. S. Viswanathan, and R. A. Simpson, IEEE Trans. Electron Devices **ED-29**, 1828 (1982).
[2]T. Terasawa, N. Hasegawa, T. Kurosaki, and T. Tanaka, Proc. SPIE **1088**, 25 (1989).
[3]P. D. Buck and M. L. Rieger, Proc. SPIE **1090** (1991).
[4]B. J. Lin, Microelectron. Eng. **17**, 79 (1992).
[5]I. Hanyu, M. Nunokawa, S. Asai, and Masayuki, Proc. SPIE **1090** (1991).
[6]K. K. Shih (unpublished).
[7]T. C. Chieu, K. K. Shih, and D. B. Dove (unpublished).

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