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SELF ALIGNED BITLINE CONTACT FOR 4 MBIT DRAM

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A 25 % reduction in 4 Mbit dRAM cell size is achieved by a self aligned bitline contact, which is fully overlapping gate and field oxide(FOBIC). No additional masks are required. The gate is encapsulated by oxide using an oxide spacer technique. A thin oxide/nitride/oxide dielectric allows a contact hole etch, which does not significantly affect the oxide insulation of the gate and the field oxide. The nitride serves as an etch stop for top oxide etch, the final etch step removes only a thin dielectric.
A 0.9 µm contact between polycide (TaSi) bitline and n^+ diffusion (R_c <50Ω), 0.2 µm distance to gate is realized without deterioration of transistor properties. No yield reduction due to gate/bitline shorts occurs. No influence of nitride on device properties is observed for nitride thickness <50nm.

1. Introduction:

4M DRAM concepts are based on 3 dimensional cell structures such as trench capacitor cell (1) and stacked capacitor cell. Their integration into the process flow and the realization of sub micron design rules set new demands for process development. However to obtain a chip size of less than 100 mm^2 further innovations are necessary.
In this paper we report a trench capacitor cell with self aligned, fully overlapping bitline contact (FOBIC). The cell design allows the contact hole to overlap gate and field oxide; the contact area is independant of lithographic alignment tolerances. The registration tolerance for bitline contacts is eliminated (see fig. 1). Thus the cell area can be shrunk by 25 % compared to a conventional contact technique.
The proposed process is different from previous concepts for self aligned contacts (2-5) in which the thermal oxide of gate polysilicon is used as an interlevel insulator between

gates and interconnections. The process has to match the requirements of reliable submicron LDD transistors, which are deteriorated by a strong reoxidation of gate polysilicon.
In contrast with a recent self aligned contact technology (6) which uses nitride LDD spacers and gate encapsulation, an oxide spacer technique is used because of LDD transistor reliability.
A new technique for etching the dielectric underneath the bitline is used to ensure a good insulation of bitline to polysilicon gates (wordline) and substrate for the overlapping contacts. The FOBIC contact process is integrated into the 4 Mbit process flow without additional masks.

2. Process flow

The 4 Mbit dRAM is fabricated with a 0.9 µm twin well process. After trench capacitor and LDD transistor formation a low resistivity polycide (poly Si/$TaSi_2$) layer is used for bitlines and local peripheral interconnects. The second interconnect level consists of Ti/TiN/AlSi metallization. For contacts connecting the polycide bitline to n+ diffusion (source/drain of transfer gates) the FOBIC process (fig. 2) is employed.

2.1 Oxide encapsulation of the gate

After patterning a double layer of poly Si/oxide (0.3 µm TEOS) an oxide spacer is formed by oxide deposition (TEOS) and RIE etching (CHF_3/O_2). The spacer width (0.2 µm) is determined by LDD transistor optimization. The poly gate is insulated by at least 0.15 µm oxide. A vertical etch profile of poly Si/oxide which can be achieved by sequential oxide etch (CHF_3/O_2) and poly Si etch (Cl_2/He) is essential.

The same technique for oxide encapsulation of the gate has also been applied to a polycide gate with an oxide spacer covering the sidewalls of a triple layer of poly Si/$TaSi_2$/oxide.

2.2.1 Contact hole etch

The dielectric under the bitline consists of a triple layer of thin oxide/nitride/oxide. For the top oxide a reflow technique (PH_3-diffusion and backetch of the doped oxide) is employed, with a final thickness of 0.2 µm.
The triple layer dielectric allows a contact hole etch, which does not significantly affect the field oxide and the oxide insulation of the gate (see fig. 2). After patterning the contact hole mask the top oxide is etched using the nitride as an etch stop. The oxide etch can be performed a) by dry etching, b) by wet etching, or a combination of both.

a) For dry etching a CHF_3 plasma with a selectivity of 4:1 with respect to the nitride is used (fig. 3a). During overetch the nitride etch rate reduces due to an enhanced development of a C rich polymer film on the nitride. The overetch time has to be sufficient (> 70 %) to remove oxide spacers on the nitride. Therefore a nitride thickness > 70 nm is required as an etch stop. After removing the polymer film by Ar plasma, the contact hole etch continues with etching the nitride (SF_6 Plasma, fig. 3b) selecti-vely to the underlying oxide (= 50 nm). To avoid any nitride spacers along the gates an overetch of 70 % is necessary. The remaining thin oxide is removed by a short dry etch step (CHF_3/O_2).

b) If the top oxide is wet etched (NH_4F/HF), a nitride layer of > 10nm is sufficient for the etch stop. The thin nitride and the thin oxide (= 50 nm) underneath are etched by the same CHF_3/O_2 dry etch step (fig. 4a). The use of a rather thin nitride as an etch stop is also possible if combining a dry etch of the top oxide (without long overetch) and a wet etch to remove oxide spacers on the nitride. The use of a wet etch step seems also preferable because of a tapering of the contact hole edge. If any conventional contacts are patterned by the same mask and technique, the contact hole size is not affected by a wet etch step for the top oxide as the underlying nitride/oxide is etched anisotropically.

After completing the process (see fig. 3c,4b,4c) an oxide insulation of the gate > 120 nm is obtained, the field oxide thinning in the contact hole is at most 50 nm. The contact area of the FOBIC contact is defined by gate and field oxide edges. The distance of the contact to the gate is only 0.2 µm.

2.2.2 Contact hole etch-alternative process

The essential feature of the contact hole etch proposed in 2.2.1 is the use of an etch stop layer for the top oxide. Only a thin dielectric is left for the final etch step by which the oxide insulation of the gate and the field oxide can be thinned. Because in the case of a pure dry etch of top oxide the required nitride thickness is > 70 nm, an alternative process allowing the use of a thinner nitride even for a pure dry etch process has been investigated. Instead of nitride a double layer of nitride (20 nm) and poly-Si (30 nm) is used. Poly Si is a very efficient etch stop for etching oxide in a CHF_3/O_2 plasma (selectivity > 20:1). However, a continous layer of poly Si can cause shorts or problems when etching contact holes from the second metallization level to source/drain areas. Therefore - after top oxide etch, poly Si etch (wet or Cl_2/He plasma), and resist stripping - the poly Si is changed into oxide by wet oxidation (900°C,20 min). The poly Si can be oxidized although buried under the top oxide because the top oxide

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