UNITED STATES PATENT AND TRADEMARK OFFICE
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BEFORE THE PATENT TRIAL AND APPEAL BOARD
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SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

DSS TECHNOLOGY MANAGEMENT, INC.
Patent Owner

_____

Case IPR. No. **Unassigned**
U.S. Patent No. 6,784,552
Title: STRUCTURE HAVING REDUCED LATERAL SPACEER EROSION
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**Declaration of Dr. Richard Fair in Support of
Petition For *Inter Partes* Review of U.S. Patent No. 6,784,552
Under 35 U.S.C. §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123**

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I, Richard B. Fair, hereby declare as follows:

I.   INTRODUCTION AND QUALIFICATIONS

1.   My name is Richard B. Fair. My findings, as set forth herein, are based on my education and background in the fields discussed below.

2.   I have been retained on behalf of Petitioner Samsung Electronics Co., Ltd. ("Samsung") to provide this Declaration concerning technical subject matter relevant to the *inter partes* review petition ("Petition") concerning U.S. Patent No. 6,784,552 (the "552 Patent," SAMSUNG-1001). I reserve the right to supplement this Declaration in response to additional evidence that may come to light.

3.   I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

4.   My compensation is not based on the resolution of this matter. My findings are based on my education, experience, and background in the fields discussed below.

5.   My background and experience is summarized in my curriculum vitae, a true and correct copy of which is submitted as Exhibit SAMSUNG-1004. Some of the relevant points are described below as well.

6.   I received a B.S. in Electrical Engineering from Duke University in 1964, an M.S. in Electrical Engineering from Pennsylvania State University in 1966, and a Ph.D. in Electrical Engineering from Duke University in 1969. My

graduate research was on electron beam systems (scanning electron microscopy) and ion beam systems (ion beam deposition of thin metal films).

7.   In 1969, I joined Bell Laboratories working on the fabrication, design, and testing of numerous semiconductor devices and integrated circuits, including metal-oxide-semiconductor (MOS) dynamic memory chips. During my time at Bell Laboratories, I worked on advanced silicon process development and started an effort on mixed signal CMOS integrated circuits. I was employed at Bell Laboratories until 1981, eventually rising to Supervisor.

8.   I have been teaching in the Department of Electrical and Computer Engineering at Duke University since 1981. I have been a Professor from 1981 to the present. I am currently the Lord-Chandran Professor of Engineering in the Edmund T. Pratt, Jr. School of Engineering.

9.   I also served as the vice president of design research and technology, director of microfabrication technology, executive director, and acting president of Microelectronics Center of North Carolina ("MCNC"), a technology non-profit that builds, owns, and operates a leading-edge broadband infrastructure for North Carolina's research, education, non-profit healthcare, and other community institutions, from 1981 to 1994.

10.   While at MCNC I helped setup a state-of-the-art CMOS processing facility   and   directed   research   on   semiconductor   processing   including

photolithography, wafer cleaning, annealing, ion implantation, plasma-enhanced CVD of thin films, metallization, and anisotropic etching processes. We conducted research on multi-level metal interconnects, barrier metallurgy, organic and inorganic inter-metal dielectrics, anti-reflective coatings, via and trench etching processes, and selective tungsten deposition for via filling. In 1987 we designed and built the world's first 1 million transistor chip, a parallel processor supercomputer. I also was responsible for the MCNC analytical lab, which included electron microscopy, atomic composition analysis, and sample preparation for reverse engineering studies. I have used such analytical tools to perform reverse engineering of semiconductor devices.

11.   In 1994, I returned to Duke University full-time. Since then I have continued to teach courses on (1) the design and analysis of analog and digital integrated circuits, (2) semiconductor devices, (3) the chemistry and physics of transistor and integrated circuit fabrication, and (4) thin-film microfluidic devices, fluid dynamics, and applications. In addition, I have an active funded research program that involves undergraduate and graduate students.

12.   I am a Life Fellow of the Institute of Electrical and Electronic Engineers ("IEEE"), a Fellow of the Electrochemical Society, past Editor-in-Chief of the Proceedings of the IEEE, and I have served as Associate Editor of the IEEE Transactions on Electron Devices. I am a recipient of the IEEE Third Millennium

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