257	774
Class	Subclass
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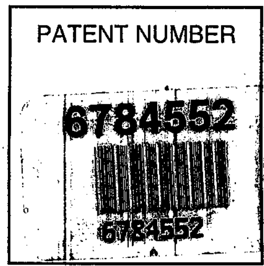


PATENT NUMBER

6784552

U.S. UTILITY Patent Application

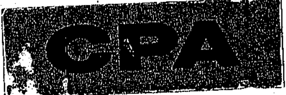
O.I.P.E.	PATENT DATE
SCANNED KW Q.A.	AUG 3 1 2004

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/540610		~~438~~ 257	~~707~~ 774	~~2812~~ 2815	Chu

APPLICANTS
James Nulty
Christopher Petti

TITLE
Method for eliminating lateral spacer erosion on enclosed contact topographies during RF sputter cleaning

PTO-2040
12/99



ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)						
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
257	774	257	774	775	776			
INTERNATIONAL CLASSIFICATION		438	634	637	639	257		
H01L	23/48							
H01L	23/52							
H01L	29/40							
			☐ Continued on Issue Slip Inside File Jacket					

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	7	18	4L	12	1
☐ The term of this patent subsequent to ____ (date) has been disclaimed.	(Assistant Examiner) 4/15/04 (Date)			NOTICE OF ALLOWANCE MAILED 04/20/04	
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. ____	BRADLEY BAUMEISTER PRIMARY EXAMINER (Primary Examiner) 4/17/04 (Date)			ISSUE FEE — Amount Due $1630	Date Paid 7/19/04
☐ The terminal ____ months of this patent have been disclaimed.	(Legal Instruments Examiner) 4/21/04 (Date)			ISSUE BATCH NUMBER	

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ISSUE FEE IN FILE

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APR 12 2004

INITIALS ______

PATENT APPLICATION

09540610

CONTENTS

		Date Received (Incl. C. of M.) or Date Mailed			Date Received (Incl. C. of M.) or Date Mailed
1.	Application 8 papers.		42.		
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3.	IDS	7-3-00	44.		
4.	Non-Final Rejection (3mths)	06.01.01	45.		
5.	Ex ① Cofm	10/4/01	46.		
6.	Amdt B	10/4/01	47.		
7.	Final Rejection (3mths)	1-9-02	48.		
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9.	Ext. of Time (1)	5.20.02	50.		
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12.	Ext. of Time (3) / CPA	6-5-02	53.		
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16.	Response req for recon	3/4/03	57.		
17.	Final Rejection (3mths)	5/20/03	58.		
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SEARCHED

Class	Sub.	Date	Exmr.
257	774	5/24/01	C.C.
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	776	5/24/01	
438	634	5/30/01	
	637	↓	
	639		
	257	5/30/01	C.C.
Searched class &	above subclass	1/4/01	C.C.
Searched class &	above subclass	8/14/02	C.C.
Searched class &	above subclass	5/13/03	C.C.
257	774	4/7/04	C.C.
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438	634		
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	257	4/7/04	C.C.

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
searched class &	above subclass	4/7/04	C.C.

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

Searched	Date	Exmr.
USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB;	5/24/01 ↓ 5/30/01	C.C. ↓ C.C.
Consulted with Gene M. Munson	1/4/02	C.C.
Allen Wilson	3/14/02	C.C.
Bill Baumeister	4/6/04	C.C.

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ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	[illegible]		4/7/00
O.I.P.E. CLASSIFIER		43	4/12/00
FORMALITY REVIEW	[illegible]	60125	6/3/00
RESPONSE FORMALITY REVIEW			

INDEX OF CLAIMS

✓	.... Rejected	N	.... Non-elected
=	.... Allowed	I	.... Interference
—	(Through numeral)... Canceled	A	.... Appeal
÷	.... Restricted	O	.... Objected

Claim Final	Claim Original	Date 5/30/01	Date 1/4/02	Date 8/14/02	Date 5/13/03	Date
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2	25	✓	✓	✓	✓	=
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If more than 150 claims or 10 actions
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PATENT APPLICATION SERIAL NO. ______________________

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PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

04/07/2000 JARTIS 00000006 09540610

01 FC:101 690.00 OP

PTO-1556
(5/87)

*U.S. GPO: 1999-459-082/19144

SAMSUNG-1002.005

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Bib Data Sheet

CONFIRMATION NO. 2171

SERIAL NUMBER 09/540,610	FILING DATE 03/31/2000 RULE	CLASS 257	GROUP ART UNIT 2815	ATTORNEY DOCKET NO. 16820.P097

APPLICANTS

James E. Nulty, San Jose, CA;

Christopher J. Petti, Mountain View, CA;

** CONTINUING DATA *************************

This application is a DIV of 08/577,751 12/22/1995 PAT 6,066,555

** FOREIGN APPLICATIONS ********************

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 06/02/2000

Foreign Priority claimed ❑ yes ❑ no 35 USC 119 (a-d) conditions met ❑ yes ❑ no ❑ Met after Allowance Verified and Acknowledged ______ Examiner's Signature ______ Initials	STATE OR COUNTRY CA	SHEETS DRAWING 8	TOTAL CLAIMS 13	INDEPENDENT CLAIMS 2

ADDRESS
43320
EVAN LAW GROUP LLC
566 WEST ADAMS, SUITE 350
CHICAGO , IL
60661

TITLE
STRUCTURE HAVING REDUCED LATERAL SPACER EROSION

FILING FEE RECEIVED 990	FEES: Authority has been given in Paper No. _________ to charge/credit DEPOSIT ACCOUNT No. _________ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other ____________

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ADDRESS
26263
SONNENSCHEIN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO , IL
60606-1080

TITLE
STRUCTURE HAVING REDUCED LATERAL SPACER EROSION

FILING FEE RECEIVED 690	FEES: Authority has been given in Paper No. ________ to charge/credit DEPOSIT ACCOUNT No. ________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other ________ ☐ Credit

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Washington, DC 20231
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Bib Data Sheet

CONFIRMATION NO. 2171

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/540,610	03/31/2000 RULE	257	2815	16820.P097

APPLICANTS

James E. Nulty, San Jose, CA;
Christopher J. Petti, Mountain View, CA;

** **CONTINUING DATA** ************************** Yes Application No. 08577751 (Dec. 22, 1995) C.C. (now Patent No. 6066555 issued May 23, 2002 C.C.

** **FOREIGN APPLICATIONS** ******************** none

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 06/02/2000

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☐ yes ☑ no	CA	8	~~13~~ 12	2
35 USC 119 (a-d) conditions met	☐ yes ☑ no ☐ Met after Allowance				
Verified and Acknowledged	[signature] Examiner's Signature — C.C. Initials				

ADDRESS

26263

TITLE

STRUCTURE HAVING REDUCED LATERAL SPACER EROSION

FILING FEE RECEIVED		
690	FEES: Authority has been given in Paper No. _________ to charge/credit DEPOSIT ACCOUNT No. _________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _______________ ☐ Credit

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Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/540,610	03/31/2000 RULE –	438	2812	16820.P097

APPLICANTS

James E. Nulty, San Jose, CA ;
Christopher J. Petti, Mountain View, CA ;

**** CONTINUING DATA** ************************* Yes Application No. 08 577751 (Dec. 22, 1995) C.C. (Now Patent No. 6066555 issued May 23, 2000) C.C.

**** FOREIGN APPLICATIONS** ********************* None C.C.

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 06/02/2000

Foreign Priority claimed ☐ yes ☑ no 35 USC 119 (a-d) conditions met ☐ yes ☑ no ☐ Met after Allowance Verified and Acknowledged [signature] Examiner's Signature C.C. Initials	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
	CA	8	13	2

ADDRESS

Blakely Sokoloff Taylor & Zafman
12400 Wilshire Boulevard
Seventh Floor
Los Angeles ,CA 90025

TITLE

STRUCTURE HAVING REDUCED LATERAL SPACER EROSION

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
690	No. _________ to charge/credit DEPOSIT ACCOUNT No. _________ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other ___________ ☐ Credit

04-03-00 A

"Express Mail" mailing label number EL3 4742US.
Date of Deposit MARCH 31, 2000

Case No. 10200/12

PATENT APPLICATION TRANSMITTAL LETTER

To the Assistant Commissioner for Patents:

Transmitted herewith for filing is the patent application of: NULTY, et al. for : METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING. Enclosed are:

☒ 8 sheet(s) of drawings, 34 pages of application (including title page), and the following Appendices : _____.

☐ Declaration.

☒ Power of Attorney.

☐ Verified statement to establish small entity status under 37 CFR §§ 1.9 and 1.27.

☐ Assignment transmittal letter and Assignment of the invention to : _____.

☒ COPY OF DECLARATION FROM PARENT APPLICATION (08/577,751); PRELIMINARY AMENDMENT.

Claims as Filed	Col. 1	Col. 2	Small Entity			Other Than Small Entity	
For	No. Filed	No. Extra	Rate	Fee	or	Rate	Fee
Basic Fee				$ 345	or		$ 690
Total Claims	14-20	0	x$9=	$	or	x$18=	$
Indep. Claims	2-3	0	x$39=	$	or	x$78=	$
Multiple Dependent Claims Present			+$130=	$	or	+$260=	$
*If the difference in col. 1 is less than zero, enter "0" in col. 2.			Total	$	or	Total	$690

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☒ The Assistant Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 23-1925. A duplicate copy of this sheet is enclosed.

- ☒ Any additional filing fees required under 37 CFR § 1.16.
- ☒ Any patent application processing fees under 37 CFR §1.17.

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- ☐ Any filing fees under 37 CFR § 1.16 for presentation of extra claims.
- ☐ Any patent application processing fees under 37 CFR § 1.17.
- ☐ The issue fee set in 37 CFR § 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR § 1.311(b).

3/31/00
Date

Paul E. Rauch, Ph.D.
BRINKS HOFER GILSON & LIONE
Registration No. 38,591

Rev. Nov-98
X:\PER\10200-12 Transmittal letter 000331.doc

Our Reference: 16820.P097

APPLICATION FOR UNITED STATES PATENT

FOR

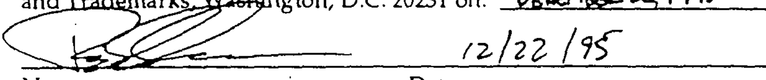
METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

Inventors: JAMES E. NULTY
CHRISTOPHER J. PETTI

Prepared by:

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025
(310) 207-3800

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail (Label No: TB756154652) in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on: December 22, 1995



12/22/95

Name Date

SAMSUNG-1002.011

BACKGROUND OF THE INVENTION

Field of the Invention:

The invention relates to semiconductor device processes, and more particularly, to improved methods for etching openings in insulating layers and a
5 semiconductor device with well defined contact openings.

Background of the Invention

In the fabrication of semiconductor devices, numerous conductive device regions and layers are formed in or on a semiconductor substrate. The conductive regions and layers of the device are isolated from one another by a dielectric.
10 Examples of dielectrics include silicon dioxide, SiO_2, tetraethyl orthosilicate glass ("TEOS"), silicon nitrides, Si_xN_y, silicon oxynitrides, $SiO_xN_y(H_z)$, and silicon dioxide/silicon nitride/silicon dioxide ("ONO"). The dielectrics may be grown, or may be deposited by physical deposition (e.g., sputtering) or by a variety of chemical deposition methods and chemistries (e.g., chemical vapor deposition ("CVD")).
15 Additionally, the dielectrics may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate glass ("BPTEOS").

At several stages of the fabrication of semiconductor devices, it is necessary to
20 make openings in the dielectric to allow for contact to underlying regions or layers. Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and the first metal layer is called a "contact opening", while an opening in other oxide layers such as an opening through an intermetal dielectric layer is referred to as a "via". For purposes

SAMSUNG-1002.012

of the claimed invention, henceforth "contact opening" or "contact region" will be used to refer to contact openings and/or via. The opening may expose a device region within the silicon substrate, such as a source or drain, or may expose some other layer or structure, for example, an underlying metallization layer, local
5 interconnect layer, or structure such as a gate. After the opening has been formed exposing a portion of the region or layer to be contacted, the opening is generally cleaned with a sputter etch, e.g., a Radio-Frequency ("RF") sputter etch, and then the opening is filled with a conductive material deposited in the opening and in electrical contact with the underlying region or layer.

10 To form the openings a patterning layer of photoresist is first formed over the dielectric layer having openings corresponding to the regions of the dielectric where the dielectric layer openings are to be formed. In most modern processes a dry etch is then performed wherein the wafer is exposed to a plasma, formed in a flow of one or more gases. Typically, one or more halocarbons and/or one or more other
15 halogenated compounds are used as the etchant gas. For example, CF_4, CHF_3 (Freon 23), SF_6, NF_3, and other gases may be used as the etchant gas. Additionally, gases such as O_2, Ar, N_2, and others may be added to the gas flow. The particular gas mixture used will depend on, for example, the characteristics of the dielectric being etched, the stage of processing, the etch tool being used, and the desired etch
20 characteristics, i.e., etch rate, sidewall slope, anisotropy, etc.

Many of the etch characteristics are generally believed to be affected by polymer residues that deposit during the etch. For this reason, the fluorine to carbon (F/C) ratio in the plasma is considered an important determinant in the etch. In general, a plasma with a high F/C ratio will have a faster etch rate than a plasma
25 with a low F/C ratio. At very low rates, i.e., high carbon content, polymer deposition occurs and etching ceases. The etch rate as a function of the F/C ratio is

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typically different for different materials. The difference is used to create a selective etch, by using a gas mixture that puts the F/C ratio in the plasma at a value that leads to etching at a reasonable rate for one material, and that leads to no etching or polymer deposition for another. For example, an etchant that has an etch rate ratio or a selectivity ratio of two to one for silicon nitride compared to silicon dioxide is an effective stripper of silicon nitride from the semiconductor substrate, because it will selectively strip silicon nitride over silicon dioxide on a substrate surface. An etchant that has an etch rate ratio or a selectivity ratio of 0.85 to one for silicon nitride compared to silicon dioxide is not considered an effective stripper of silicon nitride from the semiconductor substrate because the etchant will not effectively strip silicon nitride to the exclusion of silicon dioxide.

The selectivity of the etch process is a useful parameter for monitoring the process based on the etch rate characteristic of the particular etchant. As noted above, particular etchants or etchant chemistries attack different materials at different etch rates. With respect to dielectrics, for example, particular etchants attack silicon dioxide, BPTEOS, TEOS, and silicon nitride dielectrics at different rates. To make openings in a substrate comprising a contact region surrounded by different dielectric layers, e.g., a dielectric layer of TEOS surrounded by a dielectric layer of silicon nitride, a process will utilize different etchants to make openings through the different dielectrics. Thus, the different etch rates of particular dielectric layers for an etchant may be used to monitor the creation of an opening through a dielectric layer.

Further, by adjusting the feed gases, the taper of the sidewall in the etched opening of the dielectric can be varied. If a low sidewall angle is desired, the chemistry is adjusted to try to cause some polymer buildup on the sidewall. Conversely, if a steep sidewall angle is desired, the chemistry is adjusted to try to

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prevent polymer buildup on the sidewall. Varying the etch gas pressure, for example, has a significant effect on the shape of the opening. This is because the etchant ions generally arrive in a direction perpendicular to the substrate surface, and hence strike the bottom surfaces of the unmasked substrate. The sidewalls of etched openings, meanwhile, are subjected to little or no bombardment. By increasing the pressure of the etch gas, the bombardment directed toward the sidewalls is increased; by decreasing the pressure of the etch gas, the bombardment directed toward the sidewalls is decreased. The changing of the etch chemistry is also directly related to selectivity. Etchants that provide a near 90° sidewall angle are generally not highly selective while highly selective etches typically produce a sloped sidewall.

Following the dielectric etch(es) and prior to any conductive material deposition in a contact region, native oxide on top of the conducting layers in the contact region is removed or cleaned through a non-chemical sputter etch, e.g., an RF sputter etch. In addition to alleviating the contact region of native oxide, the sputter etch can erode any insulating dielectric layer or layers. Thus, the parameters of the sputter etch must be carefully monitored so as not to excessively erode the insulating dielectric layer(s) and expose other underlying conductive material. Exposing insulated conductive material adjacent to the conductive material in the contact region results in poor quality contacts or a short circuit through the underlying conductive material. For a thorough discussion of oxide etching, see S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Vol. 1, pp. 539-85 (1986).

The preceding discussion focused on the making of openings, e.g., contact openings, in dielectric material on a semiconductor substrate. The same principles are used in constructing device regions with a dielectric layer or layers. As geometries shrink, the forming of discreet devices on a semiconductor substrate

SAMSUNG-1002.015

becomes more specialized. Specialized deposition and etching techniques permit the density of semiconductor elements on a single chip to greatly increase, which translates into larger memory, faster operating speeds, and reduced production costs.

A typical metal oxide semiconductor (MOS) transistor, e.g., NMOS or PMOS
5 transistor, generally includes source/drain regions in a substrate, and a gate electrode formed above the substrate between the source/drain regions and separated from the substrate by a relatively thin dielectric. Contact structures can be inserted to the source/drain regions and interlays can overlie the contact structures and connect neighboring contact structures. These contact structures to the
10 diffusion region are isolated from the adjacent gate by dielectric spacer or shoulder portions. The dielectric spacer or shoulder portions also isolate the gate from the diffusion region.

Conventional contact structures limit the area of the diffusion region, because the contact hole is aligned to these regions with a separate masking step, and extra
15 area must be allocated for misalignment. Proper alignment is necessary to avoid shorting the contact structure to the gate or the diffusion well. The larger contact area means a smaller density of elements on a structure. The larger contact area is also responsible for increased diffusion-to-substrate junction capacitance, which limits device speed.

20 A self-aligned contact eliminates the alignment problems associated with conventional contact structures and increases the device density of a structure. A self-aligned contact is a contact to a source or drain diffusion region. A self-aligned contact is useful in compact geometries because it can overlap a conducting area to which it is not supposed to make electrical contact and can overlap the edge of a
25 diffusion region without shorting out to the well beneath. Consequently, less

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contact area is needed and gates or conductive material lines, e.g., polysilicon lines, can be moved closer together allowing more gates or lines on a given substrate than traditional contacts.

Figure 1 illustrates a self-aligned contact between two gate structures. Figure 1(A) is a planar top view of the contact. Figure 1(B) is a planar cross-sectional view of a self-aligned contact between a pair of gates taken through line 1(B) of Figure 1(A). Figure 1(C) is a planar cross-sectional view of a self-aligned contact between a pair of gates taken through line 1(C) of Figure 1(A).

The self-aligned contact is a contact to a source or drain diffusion region (n+ or p+ silicon) 140 that can overlap the edge of the diffusion region 140 without shorting out to the well beneath the diffusion region 140. This can be seen most illustratively through Figure 1(C). In Figure 1(C), the contact 130 does not lie directly in the diffusion region 140, but is misaligned and slightly overlaps the field oxide. In this illustration, the self-aligned contact is not directly over the diffusion region but extends over (i.e., overlaps) a well portion 170. The self-aligned contact does not short to the well portion 170 because the self-aligned contact is separated from the well 170 by the field oxide.

The self-aligned contact 130 is separated from a conducting polysilicon layer 110 by an encapsulating dielectric layer 120 such that the contact 130 can also overlap the polysilicon layer 110 without making electrical contact to the layer 110 or gate. The polysilicon layer 110 is separated from the source/drain diffusion region 140 by a dielectric spacer or shoulder 150 of the same or different dielectric material as the dielectric layer 120 directly above the conducting polysilicon.

A distinct dielectric etch stop layer 125 overlies the encapsulating dielectric layer 120. The etch stop layer 125 permits subsequent etching of the substrate

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without risk of exposing the device structures and layers because the device structuring and layers are protected from excessive etching by the etch stop layer. The diffusion contact is self-aligning because the structure can be etched to the substrate over the source/drain diffusion region 140 while the dielectric spacer 150 protects the polysilicon layer 110. Even if a photoresist that protects the polysilicon layer 110 from the etchant is misaligned with respect to the polysilicon layer 110, the dielectric spacer 150 prevents shorts to the polysilicon layer 110 when the contact 130 is provided for the diffusion region 140.

The current practice with respect to forming contact regions, particularly self-aligned contact regions, that are in electrical contact with gates, interconnect lines, or other structures in small feature size structures utilize etchants with high selectivity to protect underlying regions, like the etch stop layer and the first insulating layer. Figure 2 demonstrates a typical prior art process of forming a self-aligned contact region adjacent to a gate. In Figure 2(A), a gate oxide layer 210 is formed on a substrate 200 with a conducting layer, for example a polysilicon layer 220, overlying the gate oxide layer 210, and an insulating layer, for example a TEOS layer 230, overlying the polysilicon layer 220. Adjacent to the polysilicon layer is a contact opening region 270. The polysilicon layer 220 is separated from the contact region 270 by an insulating spacer portion, for example a TEOS spacer portion 235. A separate insulating or etch stop layer, for example a silicon nitride layer 240 overlies the TEOS layer 230 and the contact region 250. A blanket layer, for example a doped insulating layer like a BPTEOS layer 250, planarly overlies the etch stop layer 240.

A layer of photoresist material 280 overlies the planarized BPTEOS layer 250 to expose the contact opening 270. In Figure 2(A), a contact opening 270 has been opened through the BPTEOS layer 250. The etchant utilized to make the opening had a high selectivity toward BPTEOS relative to silicon nitride. When the contact

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opening was through the BPTEOS material, the etchant did not etch or did not effectively etch the silicon nitride layer 240 material. Hence the description of the silicon nitride layer 240 as an etch stop layer. The silicon nitride etch stop layer protected the underlying TEOS layer so that the polysilicon remains completely
5 encapsulated.

Figure 2(A) illustrates an etch 260 to remove the silicon nitride etch stop layer 240. In the etch illustrated in Figure 2(A), a high selectivity etch toward silicon nitride relative to the underlying TEOS layer 230 material is practiced to efficiently etch the silicon nitride layer and to protect the underlying TEOS layer 230 from the
10 etchant. An example of a high selectivity etch recipe to effectively strip silicon nitride as compared to the TEOS layer is 30 sccm CHF_3 and 30 sccm O_2 at 60 mtorr and 100 watts of power. The result of the high selectivity etch is illustrated in Figure 2(B).

Figure 2(B) shows that the silicon nitride selective etch effectively removed
15 silicon nitride 240 from the contact opening 270. The selective etch for silicon nitride compared to TEOS material, however, left the TEOS layer 230 with a spacer portion 235 wherein the spacer portion is sloping or tapered toward the contact opening. This result follows even where the spacer portion 235 is originally substantially rectangular as in Figure 2(A). The properties of the highly selective
20 etch of the overlying etch stop layer will transform a substantially rectangular spacer into a sloped spacer. Figure 2(B) presents a polysilicon layer 220 encapsulated in a TEOS layer 230 with a spacer portion 235 adjacent to the contact opening 270, the spacer portion 235 having an angle 290 that is less than 85°.

In addition to providing stopping points or selectivity between materials, the
25 use of high selectivity etches to form sloped spacer portions is the preferred practice

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because the sloped shape will result in good step coverage by the metal that is deposited into it. The filling of contact openings or gaps (i.e., gap fill) is an important consideration because it relates directly to the reliability of a device. If an opening is not completely filled with a insulative material, for example, and a gap is created, a subsequent conductive material deposit can fill the gap which can lead to shorting. Sloped contact openings are easier to completely fill than boxy structures because the transition between sloped structures and openings is smooth compared to the abrupt transitions between boxy structures and openings. Because of concerns for complete gap fill and good step coverage, industry preference is for sloped spacers and planar deposition layers similar to that shown in Figure 2(b).

Once the contact opening is made, the opening is cleaned with a sputter etch, e.g., an RF sputter etch, before conductive material is added to fill the opening or gap. The RF sputter etch that is used to clean the contact opening in the process described above will attack and erode a portion of the insulating spacer surrounding the conducting portion and adjacent to the contact region. Figure 3 presents a prior art substrate with a gate and a contact region undergoing an RF sputter etch. In Figure 3, a gate oxide 310 is formed on a substrate 300 with a polysilicon layer 320 overlying the gate oxide 310 and an insulating layer, for example a TEOS layer 330 overlying the polysilicon layer 320. A distinct insulating layer, for example a silicon nitride etch stop layer 340, overlies the TEOS layer 330 and this etch stop layer 340 is covered by a third insulating layer, for example a BPTEOS blanket layer 350. Adjacent to the gate is a contact region 360. An etch of the silicon nitride etch stop layer 340 with a high selectivity etch for silicon nitride relative to the underlying TEOS layer material produced a gate with a sloping or tapered spacer portion 370 of TEOS material, illustrated in ghost lines. A subsequent RF sputter etch is utilized to clean the contact region 360.

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Although brief and designed to clean the contact region, the RF sputter etch will erode a portion of the insulating TEOS spacer. The dynamics of the sputter etch are that it proceeds vertically, directing high-energy particles at the contact region. The sloping or tapered spacer portion adjacent the polysilicon and separating the polysilicon from the diffusion region is struck by the high-energy particles of the RF sputter etch 380. Because the spacer portion 370 is sloping or diagonal, a significant surface area portion of the spacer portion 370 is directly exposed to the high-energy particles from the RF sputter etch 380. Further, with sloping spacers, or spacers having an angle relative to the substrate surface of less than 85° the vertical portion of the dielectric layer ((i.e., that portion above the polysilicon gate) decreases much less than the diagonal portion of the spacer. In terms of measuring TEOS material removal during the RF sputter etch in Figure 3, the difference between d_1 and d_2 is greater than the difference between v_1 and v_2. Thus, in conventional prior art self-aligned contact structures, the diagonal thickness of the TEOS spacer, rather than the vertical thickness of the TEOS layer, determines the minimum insulating layer thickness for the gate.

For gate structures having minimum diagonal insulative spacer portions of 500 Å or less, the result of the sputter etch 380 is that the sputter etch 380 laterally erodes the diagonal portion of the TEOS layer 370 adjacent to the contact region to a point where the polysilicon 320 is no longer isolated from the contact region 360 by an insulating layer. In that case, there is a short circuit through the underlying conductive material when the contact opening is filled with conductive material. This result follows because the conventional RF sputter etch utilized for cleaning the contact region results in an approximately 200-500 Å loss of the spacer material. Further, process margins generally require that the device spacer have a final minimum thickness (after all etches, doping, and deposits) of at least 500 Å. Thus,

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to eliminate alignment sensitivity for conventional small feature size structures, including self-aligned contact structures, requires a final (i.e., at the time of contact deposition) minimum insulating spacer of more than 500 Å and preferably on the order of 1000-1500 Å or greater to fulfill requirements for an adequate process
5 margin, complete gap fill, and device reliability.

To construct structures having a minimum insulative spacer portion of more than 500 Å directly effects the number of structures that can be placed on a device, such as a chip. The construction of structures having a minimum insulative spacer portion of more than 500 Å requires that the pre-etch-stop-etch spacer be bigger or
10 thicker to yield an effective spacer after the etching processes. In such cases, the structures must be separated a distance such that the contact area opening is sufficient enough for an effective contact. This spacing requirement directly limits the number of structures that can be included on a device. In small feature size structures, particularly structures utilizing self-aligned contacts, the width of contact
15 openings is approximately 0.6 microns at the top of the planarized layer and 0.2 microns at the base of the contact opening. Figure 3 indicates the difference in contact opening widths for the same contact in prior art structures. w_1 represents the width at the top of the planarized layer and w_2 represents the width at the base of the contact opening. Further, an aspect ratio can be defined as the height of a
20 structure (field oxide plus conductive layer plus first insulative layer plus etch stop layer, if any) relative to the width of the base of a contact opening (i.e., the distance between adjacent spacers). Typical aspect ratios for self-aligned contact structures target ratios of 1.0-2.4. This prior art range is not achievable with any device reliability. To achieve aspect ratios of 1.0-2.4 requires minimum spacer portions of
25 less than 1000 Å and preferably on the order of 500 Å. As noted above, the minimum spacer portions required for aspect ratios of 1.0-2.4 cannot withstand the

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sputter etch and will result in the exposure of the underlying polysilicon gate and short circuiting with the contact.

There is a need for cost effective structures wherein the individual devices are as close together as possible while maintaining device reliability and an adequate process margin and assuring complete gap fill. There is a need for a device and for a process to manufacture such a device whereby there is provided a contact opening with no alignment sensitivity relative to a gate electrode or other structure and whereby the gate electrode does not fall within the contact opening but remains isolated from the contact opening by an insulating layer. The process must be compatible with gate electrode insulating spacers of less than 500 Å. The device resulting from the needed process should be capable of maintaining high quality contacts between the conductive material in the contact region and the adjacent conductive gate or other structure.

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SUMMARY OF THE INVENTION

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The invention relates to a process for minimizing lateral spacer erosion of an insulating layer on an enclosed contact region is disclosed and a device including a contact opening with a small alignment tolerance relative to a gate electrode or
5 other structure. The process provides high quality contacts between a conductive material in the contact region and a device region, such as a source or drain, or some other layer or structure. The process comprises the well known step of forming a conductive layer on the semiconductor body adjacent a contact region. This is followed by the forming of a first insulating layer adjacent said conductive layer and
10 the contact region. A selected area is masked with photoresist and the first insulating layer and the conductive layer are etched to form a device structure, such as a gate, adjacent the contact region. Next, insulating lateral spacers are added to the device structure to isolate the conductive portion of the device. The insulating spacers are etched so that the device comprises an insulating layer overlying a
15 conductive layer with a lateral spacer portion adjacent the contact region wherein the spacer portion has a substantially rectangular profile. A distinct insulating layer or etch stop layer is then formed adjacent to the first insulating layer and over the contact region. A third insulating layer or blanket layer is then optionally formed over the etch stop layer. The blanket layer may or may not be planarized.

20 If a blanket layer is included, an etchant is utilized to etch a contact opening through the exposed portion of the blanket layer to the etch stop layer. Next, a second etch or etch-stop etch is performed to remove the etch stop layer material from the contact region. The etch-stop etch is also almost completely anisotropic, meaning that the etchant etches in one direction–in this case, vertically (or
25 perpendicular relative to the substrate surface) rather than horizontally. The etch

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removes the etch stop insulating layer and retains the substantially rectangular lateral spacer portion of the first insulating layer. The anisotropic etch etches primarily the exposed etch stop material that lies normal to the direction of the etch. Thus, the etch removes the etch stop material covering the area of the contact
5 region but does not significantly etch the etch stop material adjacent to the spacer(s). The etch stop layer on the spacer adds dielectric thickness between the conductive layer and any contacting conductor. In general, the etching conditions utilized for the etch-stop etch have a low selectivity for etching the etch stop layer compared to the underlying insulating material.

10 The etch-stop etch may be followed by a sputter etch to clean the contact region. Unlike prior art processes whereby the sputter etch erodes the underlying sloping lateral spacer portion of the first insulating layer adjacent to the conducting layer, the sputter etch does not significantly erode the substantially rectangular lateral spacer of the first insulating layer, thus allowing the conductive layer of the
15 device structure to remain completely isolated or insulated by a spacer comprised of the first insulating layer and some etch stop layer material.

The structure contemplated by the invention is an effective device for small feature size structures, particularly self-aligned contacts. The structure consists of first and second conducting layers spaced apart by a region with an area defined in
20 the substrate; an insulating layer encapsulating each conductive layer, wherein the insulating layer includes lateral spacer portions; and an etch stop layer adjacent the insulating layer and over the first and second conducting layers. The invention contemplates that the structure region has a first width between the first and second conducting layers, and a second width between the lateral spacer portions of the
25 insulating layer adjacent to the first and second conducting layers, wherein the region has an aspect ratio of 1.0-2.4. The aspect ratio is defined as the height of the

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apparatus relative to the second width of the region. Thus, the invention contemplates larger contact openings for effective contacts, reduced device feature size, and increased device density, while maintaining aspect ratios similar to larger, less dense devices in the prior art. The invention further contemplates that the
5 structure has a minimum insulating layer thickness of 400 Å and that this minimum thickness is determined by the thickness of the insulating layer deposited vertically on the structure.

The device is capable of maintaining high quality, reliable contacts between the conductive material in the contact region and the underlying device region,
10 such as a source or drain, or some other layer or structure. The device contemplates minimum contact opening base widths of 0.2 microns and minimum contact opening widths of 0.5 microns when measured from the top of a planarized layer, and aspect ratios (i.e., height of structure including the etch stop layer relative to the width of the base of a contact opening between the spacers) on the order of 1.0-2.4.

15 Additional features and benefits of the invention will become apparent from the detailed description, figures, and claims set forth below.

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BRIEF DESCRIPTION OF THE DRAWINGS

The features, aspects, and advantages of the present invention will become more thoroughly apparent from the following detailed description, appended claims, and accompanying drawings in which:

5 Figure 1 is a planar view of a self-aligned contact to diffusion. Figure 1(A) is a planar top view of a self-aligned contact. Figure 1(B) is a cross-sectional planar side view of a self-aligned contact to diffusion through line 1(B) of Figure 1(A). Figure 1(C) is a cross-sectional planar side view of a self-aligned contact to diffusion through line 1(C) of Figure 1(A).

10 Figure 2 is a cross-sectional side view of the formation of a prior art contact opening formation. Figure 2(A) illustrates a high selectivity etch of an etch stop insulating layer, and Figure 2(B) illustrates the results of that etch.

Figure 3 is a cross-sectional side view of the formation of a prior art contact opening formation during a sputter cleaning etch.

15 Figure 3 is a cross-sectional view of an example of a semiconductor device during fabrication upon which the invention may be practiced.

Figure 4 presents a cross-sectional planar side view of the preparation of a series of gates on a semiconductor substrate surface.

Figure 4(A) illustrates a cross-sectional planar side view of an insulating layer
20 adjacent to a conducting layer, both layers overlying two diffusion regions.

Figure 4(B) illustrates a cross-sectional planar side view of a series of gates consisting of insulating material adjacent conducting material.

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Figure 4(C) illustrates a cross-sectional planar side view of the deposition of additional insulating material over the series of gates, the additional insulating material to be used for the formation of spacer portions adjacent the contact or diffusion regions.

5 Figure 4(D) illustrates a cross-sectional planar side view of a series of gates completely encapsulated in insulating material wherein the spacers of the insulating material adjacent the contact or diffusion regions have substantially rectangular profiles.

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10 encapsulated with insulating material and an insulating etch stop layer overlying the insulating material.

Figure 4(F) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material and an insulating etch stop layer overlying the insulating material, wherein the diffusion region is implanted to include a

15 silicide.

Figure 4(G) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, and a distinct planarized insulating layer overlying the etch stop layer.

Figure 4(H) illustrates a cross-sectional planar side view of a series of gates

20 encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the etch stop layer, and a photoresist patterning layer deposited over the blanket layer.

Figure 4(I) illustrates a cross-sectional planar side view of a series of gates

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material, a distinct planarized insulating blanket layer overlying the etch stop layer, and contact openings etch through the blanket layer above the diffusion region.

Figure 4(J) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating
5 material, a distinct planarized insulating blanket layer overlying the etch stop layer, and a contact opening to a diffusion region and a second contact opening through the blanket layer but separated from the diffusion region by an etch stop layer.

Figure 4(K) illustrates a close-up cross-sectional planar side view of a circled portion of Figure 4(J), the circled portion labeled 4(K) and illustrating the spacer
10 portion of a contact region following an etch of the etch stop layer from the contact region.

Figure 4(L) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the etch stop layer,
15 and a conductive contact in a contact region extending to a diffusion region in the semiconductor substrate.

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DETAILED DESCRIPTION OF THE INVENTION

The invention is a device and a process whereby there is provided a contact opening with a no alignment sensitivity relative to a gate electrode or other structure such that the gate electrode does not fall within the contact opening but
5 remains isolated from the contact opening by an insulating layer. The structure contemplated by the invention is an effective device for small feature size structures, particularly self-aligned contacts, because it is capable of maintaining high quality contacts between the conductive material in the contact region and the underlying device region, such as a source or drain, or some other layer or structure
10 with minimum contact opening base widths (i.e., at the base of the contact openings) of 0.2 microns and minimum contact opening widths of 0.5 microns when measured from the top of a planarized layer, minimum encapsulating layer thicknesses of 400 Å, and aspect ratios (i.e., height of structure including the etch stop layer relative to the width of the base of a contact opening between the spacers)
15 in the range of 1.0-2.4.

In the following description, numerous specific details are set forth such as specific materials, thicknesses, processing steps, process parameters, etc., in order to provide a thorough understanding of the invention. It will be obvious, however, to one skilled in the art that these specific details need not be employed to practice the
20 invention. In other instances, well known materials or methods have not been described in detail in order to avoid unnecessarily obscuring the invention. Furthermore, in the following discussion, several embodiments of the invention are illustrated with respect to specific structures, oxide layers, and oxide layer openings. It will be appreciated that each of the methods described herein can be
25 utilized on a variety of structures and oxide layers, to form any type of opening, and

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each of the insulating layer etching methods described herein is not necessarily restricted to the structure and/or insulating layer in conjunction with which it is described. Further, any of the methods described herein may be performed as part of a multistep etch comprising additional etch processes.

Figure 4 presents a cross-sectional view of the preparation of a series of gates or transistors on a semiconductor substrate surface. Referring to Figure 4(A), the semiconductor substrate 400 can be either p- or n-type, and includes diffusion regions 405, such as sources or drains, that are heavily doped with the opposite dopant type of the substrate. An n-type first conducting layer 415 of polysilicon doped by implantation with phosphorous to a resistivity of 50-200 ohms/square is deposited over the diffusion regions. The polysilicon layer 415 is deposited by low pressure CVD ("LPCVD") using an LPCVD tube and SiH_4 gas at 200-400 mtorr with a thickness of 2000-3000 Å. It should be appreciated by those skilled in the art that this conducting layer 415 could instead be a p-type conducting layer or a metallic conductor of, for example, W, Mo, Ta, and/or Ti, or that this conducting layer 320 could also be a silicide, consisting of WSi_2, $MoSi_2$, $TaSi_2$, PtSi, PdSi, or that this conducting layer 320 can further be a layered structure consisting of a silicide on top of doped polysilicon.

The polysilicon layer 415 overlays an insulating dielectric layer 410 such as doped or undoped silicon dioxide. The dielectric layer 410 may comprise a single oxide, or several layers formed by various methods. For example, one or more layers of oxide may be deposited by plasma enhanced chemical vapor deposition ("PECVD"), thermal CVD ("TCVD"), atmospheric pressure CVD ("APCVD"), subatmospheric pressure CVD ("SACVD"), for example utilizing, for example, TEOS and oxygen or TEOS and ozone chemistries. As used herein, reference to, for example, a PECVD TEOS oxide denotes an oxide layer deposited by PECVD utilizing

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TEOS chemistry. Additionally, one or more layers of dielectric layer 410 may be a spin-on-glass ("SOG") layer.

A TEOS dielectric layer 420 with a total thickness of approximately 3000 Å overlies the conducting layer 415. It should be appreciated by those of ordinary skill in the art that this TEOS layer 420 could instead be an insulating layer of, for example, silicon dioxide, SiO_2, ONO, silicon nitride (Si_xN_y), or silicon oxynitride (SiO_xN_y). Additionally, the insulating layer 420 may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate ("BPTEOS"). Further, the dielectric layer 420 may comprise a single layer oxide, like TEOS, or several layers formed by various methods.

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Referring further to Figure 4(A), a photoresist masking layer 425 is deposited over the TEOS dielectric layer 420. The photoresist masking layer 425 exposes diffusion regions 405 in the semiconductor substrate. Referring to Figure 4(B), a series of photolithographic etches are performed to remove the TEOS layer 420 material and the polysilicon layer 415 from the diffusion or contact regions. The etches are performed using a parallel plate plasma etcher with a power of 200-300 watts. First, a fluorocarbon photolithographic etch, CHF_3/C_2F_6 at 50 mtorr, is performed to remove the insulating TEOS material from areas adjacent to and including the diffusion or contact regions. This is followed by a single polysilicon photolithographic etch using a chlorine plasma (Cl_2/He) to define a polysilicon conducting layer 415 above the transistor or gate regions.

The process described thus far has been described in terms of multiple etching steps involving multiple passes through the etch chamber. It should be recognized

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by one of ordinary skill in the art that the etching steps can be combined into a multiple-step etch whereby the etch may be accomplished with one pass through the etch chamber, the etcher changing chemistries and executing the multiple etches sequentially.

5 Referring to Figure 4(C) and 4(D), spacers are formed between the polysilicon layer 415 of the gates and the contact regions by depositing an additional of conformal layer of TEOS material 430 over the structure and etching spacer portions extending into the contact opening and adjacent to the polysilicon layer 415 approximately 1500 Å in width. The spacer portions 435 of the TEOS layer 430 are 10 demarked by ghost lines in Figure 4(D). The spacers serve to insulate the polysilicon layers 415 from the conducting material that will fill the contact opening and prevent the gates from overlapping the diffusion regions. The spacers 435 serve to completely encapsulate the polysilicon layers 415 of the individual gates. As shown in Figure 4(C), care is taken to etch the spacers 435 such that the spacers 435 have a 15 substantially rectangular profile. This is accomplished using a low bias and high pressure etch (2.8 torr, 140 sccm He, 30 sccm CHF_3, 90 sccm CF_4, and 850 watts power), that results in low polymer formation. At this point, the preferred embodiment of the invention contemplates that the TEOS layer can have a minimum vertical width of approximately 3000 Å and spacers with a minimum 20 width of approximately 1000 Å.

Referring to Figure 4(E), the diffusion regions are next implanted with a suitable dopant utilizing conventional techniques. The dopant may be implants of arsenic, phosphorous, or boron. Subsequently, silicides, for example WSi_2 and $TiSi_2$, may also be formed. Figure 4(E) illustrates silicide formation 445 in the 25 diffusion regions.

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Referring to Figure 4(F), overlying the TEOS layer 420 is deposited a second distinct dielectric or etch stop layer 440, in this example, an silicon nitride (Si_xN_y) layer 440, with a total thickness of 700 angstroms. It should again be appreciated by those of ordinary skill in the art that this silicon nitride layer 440 could instead be an
5 insulating layer of, for example, silicon dioxide, SiO_2, ONO, or $SiO_xN_y(H_z)$. Additionally, the silicon nitride etch stop layer 340 may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate ("BPTEOS"). Further, the etch stop layer
10 440 may comprise a single silicon nitride layer or several layers formed by various methods. It is important that the etch stop layer be different or distinct from the underlying insulating layer.

The invention contemplates that at this point the structure has an aspect ratio of 1.0-2.4. As used herein, an aspect ratio is defined as the ratio of the height of a
15 contact opening to the top of the horizontal portion of the etch stop layer to the base width of the contact opening between the insulating spacers. For example, an embodiment of the invention contemplates contact opening heights of 5300 Å (0.53 μm) relative to widths of 0.32 μm to give aspect ratios of 1.6.

Referring to Figure 4(G), an optional dielectric blanket layer 450 is next
20 deposited adjacent to the etch stop layer 440. The blanket layer 450 may or may not be planarized. In Figure 4(G), the blanket layer 450 is planarized. The planarized blanket layer 450 facilitates the formation of an interconnect layer that might later be deposited over the contact regions. The blanket layer in Figure 4(G) is a doped silicate glass, for example BPTEOS. It should be appreciated by those of ordinary skill
25 in the art that this BPTEOS layer 450 could instead be another doped insulating layer of, for example, BPSG or PSG, or an undoped insulating layer of silicon dioxide,

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SiO_2, ONO, or SiO_xN_y. Further, the blanket layer 450 may comprise a single oxide, like BPTEOS, or several layers formed by various methods.

Next, as shown in Figure 4(H), a photoresist pattern or mask layer is deposited adjacent to the blanket layer such that the contact regions overlying the diffusion
5 regions are exposed. This is followed by a photolithographic etch of the BPTEOS blanket layer 450 in the contact regions. The etch is a fluorocarbon photolithographic etch (7 sccm CHF_3, 6 sccm Freon 134a) at 29 mtorr. The etch reveals a pair of contact regions 460 and 465 above the diffusion regions.

Referring to Figure 4(J), a photoresist material 470 is overlayed in contact
10 opening 465 adjacent to the etch stop layer to protect the etch stop material in contact opening 465 from a subsequent photolithographic etch to remove the etch stop layer. Next, a photolithographic etch, (900 mtorr, 100 sccm, He, 85 sccm C_2F_6, and 225 watts power using a Lam 4400 Series plasma etching system) is performed to remove the etch stop layer 440 from contact opening 460. The etch conditions for
15 this etch are low bombardment/high neutral flux conditions.

Figure 4(K) is a close-up view of the cross-sectional portion of contact opening 460 in Figure 4(J). The etch proceeds anisotropically, primarily removing etch stop material lying in a horizontal plane relative to the vertical direction of the etchant ions. The etchant removes material primarily from the base of the contact region
20 460, and does not remove all of the etch stop material adjacent to the spacer portion of the TEOS layer 420. Thus, the remaining etch stop material adjacent to the spacer portion of the TEOS layer serves as additional spacer material to insulate the polysilicon from a conductive contact that will subsequently be added to the contact region 460.

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The etchant utilized to remove silicon nitride from the contact region 460 has a low selectivity for etching the silicon nitride material compared to the underlying TEOS layer. The use of an etchant with a low selectivity for silicon nitride relative to TEOS does not significantly destroy the TEOS layer 420 spacer portion. The low
5 selectivity etch yields a TEOS layer 420 spacer portion that retains a rectangular or "boxy" profile. Figure 4(K) illustrates that only a small portion 475 (illustrated in ghost lines) of the TEOS layer 420 spacer portion is removed during the etch. Of primary significance, the spacer portion of the TEOS layer 420 retains its substantially rectangular profile.

10 It is to be appreciated that the described etch stop layer etch conditions (i.e., low selectivity, low bombardment/high neutral flax) are exemplary of etch conditions that result in the retention of a boxy spacer. The invention relates to these process conditions as well as others that result in the retention of a boxy spacer. Thus, the etch-stop etch conditions should be regarded in an illustrative
15 rather than restrictive sense.

The silicon nitride etch stop layer 440 etch is followed by a sputter etch to clean the contact opening 460. In a currently preferred embodiment, the sputter etch is carried out in an atmosphere of argon, a 8 mtorr pressure, with a 1000 volt bias. In a currently preferred embodiment, the sputter etch is carried out in a commercially
20 available system such as the Applied Materials Endura 5500 systems. Alternatively, any system having a sputter etch mode may be used to practice the invention. As will be appreciated by a person of ordinary skill in the art, the parameters can be varied considerably while still achieving the objects of the invention. In a currently preferred embodiment, the etch is designed to etch approximately 200 Å per minute
25 as measured on thermal oxide. Because of the retention of a substantially

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rectangular or "boxy" spacer portion, the sputter etch does not significantly erode the spacer portion of the TEOS layer.

At this point, the invention contemplates that the minimum encapsulating dielectric layer, i.e., TEOS, thickness will be approximately 400 Å and that this
5 minimum thickness will be at the corner most effected by the etch-stop layer etch and the sputter etch. In Figure 4(K) that minimum thickness is the diagonal denoted *d*.

Figure 4(L) presents a cross-sectional planar side view of the structure of the invention wherein a conductive contacts 480 have been deposited in the contact
10 openings 460.

The process described above yields a structure wherein first and second conductive layers (e.g., polysilicon layers) are separated by a contact region with an area defined in the semiconductor substrate. An insulating layer is adjacent to and encapsulates the first and second conductive layers. The invention contemplates
15 that the insulating layer has spacer portions between the conductive layers and the contact region. The invention contemplates that high quality contacts can be achieved wherein the spacer portions have a minimum insulative material thickness of 400 Å. In the preferred embodiment, the spacer portions of the insulating material further have substantially rectangular profiles. The invention
20 also contemplates that a portion of the etch stop layer material may remain adjacent to the spacer portion of the insulating layer following an anisotropic etch of the etch stop material with a low selectivity etch for the etch stop material relative to the insulating layer material. The result is a contact opening with spacer sidewalls comprised, at least potentially, of a portion of etch stop layer material.

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The invention contemplates that effective contact openings may have base widths as small as 0.2 μm (and as small as 0.5 μm when measured from the top of the optional planarized layer), and base areas as small as 0.1 μm^2. Thus, the invention contemplates aspect ratios for effective contact openings of 1.0-2.4,
5 wherein an aspect ratio is defined as the ratio of the height of a contact opening to the top of the horizontal portion of the etch stop layer to the base width of the contact opening between the spacers. Figure 4(L) illustrates a height, h, and a width, w, from which an aspect ratio may be calculated for a contact region, and a height h_1, and a width, w_1, from which an aspect ratio may be calculated for a contact region.

10 In the preceding detailed description, the invention is described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather
15 than a restrictive sense.

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CLAIMS

What is claimed is:

1 1. A process for minimizing lateral spacer erosion on a contact region,
2 said process comprising:

3 encapsulating a conducting layer in an insulating layer on said
4 semiconductor body adjacent said contact region, wherein said insulating layer
5 includes a substantially rectangular spacer portion adjacent said contact region;

6 depositing an etch stop layer adjacent said insulating layer and adjacent
7 said contact region; and

8 etching a portion of said etch stop layer adjacent said contact region
9 wherein said etching does not significantly erode said spacer portion of said
10 insulating layer.

1 2. The process of claim 1, wherein said etching step utilizes a plasma
2 etching system.

1 3. The process of claim 2, wherein an etching condition for said etching
2 step is a low bombardment/high neutral flux condition.

1 4. The process of claim 3, wherein said etching condition has a low
2 selectivity for said etch stop layer material relative to said first insulating layer
3 material.

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1 5. The process of claim 4, wherein said selectivity is less than or equal to
2 1:1.

1 6. The process of claim 2, wherein said plasma etching system is a Lam
2 4400 Series plasma etching system.

1 7. The process of claim 6, wherein said etch stop layer etch is performed
2 using a recipe of 900 mtorr, 100 sccm He, 85 sccm C_2F_6, and 225 watts power.

1 8. The process of claim 1, including cleaning said exposed portion of said
2 first insulating layer with a sputter etch after said etching of said etch stop layer
3 wherein said spacer portion of said first insulating layer retains its substantially
4 rectangular profile.

1 9. The process of claim 8, wherein said sputter etch is a radio-frequency
2 sputter etch.
1

1 10. The process of claim 1, including depositing a blanket insulating layer
2 adjacent said etch stop layer, forming a patterning layer on said blanket insulating
3 layer wherein said patterning layer exposes said contact region, and etching a
4 portion of said blanket insulating layer over said contact region with a suitable
5 etchant to expose a portion of said etch stop layer prior to said etching of said etch
6 stop layer.

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1 11. The process of Claim 10, wherein the blanket layer is planarized.

1 12. A process for minimizing lateral spacer erosion on a contact region,
2 said process comprising:

3 encapsulating a conducting layer in an insulating layer on said
4 semiconductor body adjacent said contact region, wherein said insulating layer
5 includes a substantially rectangular spacer portion adjacent said contact region;

6 depositing an etch stop layer adjacent said insulating layer and adjacent
7 said contact region; and

8 etching a portion of said etch stop layer adjacent said contact region
9 wherein said etching delivers a minimal diagonal erosion rate of said spacer portion
10 relative to the vertical erosion rate of said insulating layer.

1 13. The process of claim 12, wherein said etching step utilizes a plasma
2 etching system.

1 14. The process of claim 13, wherein an etching condition for said etching
2 step is a low bombardment/high neutral flux condition.

1 15. The process of claim 14, wherein said etching condition has a low
2 selectivity for said etch stop layer material relative to said first insulating layer
3 material.

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1 16. The process of claim 15, wherein said selectivity is less than or equal to
2 1:1.

1 17. The process of claim 13, wherein said plasma etching system is a Lam
2 4400 series plasma etching system.

1 18. The process of claim 17, wherein said etch stop layer etch is performed
2 using a recipe of 900 mtorr, 100 sccm He, 85 sccm C_2F_6, and 225 watts power.

1 19. The process of claim 12, including cleaning said exposed portion of said
2 first insulating layer with a sputter etch after said etching of said etch stop layer
3 wherein said spacer portion of said first insulating layer retains its substantially
4 rectangular profile.

1 20. The process of claim 19, wherein said sputter etch is a radio-frequency
2 sputter etch.
1

1 21. The process of claim 12, including depositing a blanket insulating layer
2 adjacent said etch stop layer, forming a patterning layer on said blanket insulating
3 layer wherein said patterning layer exposes said contact region, and etching a
4 portion of said blanket insulating layer over said contact region with a suitable
5 etchant to expose a portion of said etch stop layer prior to said etching of said etch
6 stop layer.

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1 22. The process of Claim 21, wherein the blanket layer is planarized.

1 23. A semiconductor apparatus comprising:

2 first and second conducting layers spaced apart by a region with an area
3 defined in the substrate;

4 an insulating layer adjacent said first and second conductive layers; and

5 an etch stop layer adjacent said insulating layer and over said first and second
6 conducting layers, and a second width between said insulating layer adjacent said
7 first and second conducting layers, and wherein said region has an aspect ratio of 1.0-
8 2.4 said aspect ratio defined as the height of said apparatus relative to the second
9 width of said region.

1

1 24. The semiconductor apparatus of claim 23, wherein said insulating layer
2 has a spacer portion adjacent said region wherein said spacer portion has a
3 substantially rectangular profile.

1

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1 25. The semiconductor apparatus of claim 23, wherein said etch stop layer
2 is silicon nitride.

1

1 26. The semiconductor apparatus of claim 23, wherein said etch stop layer
2 is silicon dioxide.

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ABSTRACT

A process for minimizing lateral spacer erosion of an insulating layer adjacent to a contact region and an apparatus whereby there is provided a contact opening with a small alignment tolerance relative to a gate electrode or other structure are disclosed. The process includes the steps of forming a conductive layer on said semiconductor body then depositing an insulating layer adjacent to the conductive layer. Next, substantially rectangular insulating spacers are formed adjacent to the gate. An etch stop layer is deposited adjacent said insulating layer followed by an etch to remove the etch stop layer material from the contact region. This etch is conducted under conditions wherein the etch removes the etch stop layer but retains the substantially rectangular lateral spacer profile of the first insulating layer. The apparatus is capable of maintaining high quality contacts between the conductive material in the contact region and the underlying device region, such as a source or drain, or some other layer or structure and is an effective structure for small feature size structures, particularly self-aligned contact structures.

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Our Ref.: 016820.P097

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

the specification of which

_____	is attached hereto.
XXXX	was filed on December 22, 1995 as
	Application Serial No. 08/577,751
	and was amended on ____________ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I do not know and do not believe that the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119, of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) — Priority Claimed

(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

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I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, a firm including: Keith G. Askoff, Reg. No. 33,828; Aloysius T.C. AuYeung, Reg. No. 35,432; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; William D. Davis, Reg. No. 38,428; Daniel M. De Vos, Reg. No. 37,813; Scot A. Griffin, Reg. No. 38,167; David R. Halvorson, Reg. No. 33,395; Brian D. Hickman, Reg. No. 35,894; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; Stephen L. King, Reg. No. 19,180; Daniel C. Mallery, Reg. No. 33,532; Michael J. Mallie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Edward W. Scott IV, Reg. No. 36,000; Maria E. Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; John C. Stattler, Reg. No. 36,285; David R. Stevens, Reg. No. 38,626; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Gary B. Goates, Reg. No. 35,159; Thomas X. Li, Reg. No. 37,079; and Edwin A. Sloane, Reg. No. 34,728; my patent agents, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor James E. Nulty

Inventor's Signature [signature] Date 4/26/96

Residence San Jose, California 95128 Citizenship U.S.A.
(City, State) (Country)

Post Office Address 1037 Lenor Way
San Jose, California 95128

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Full Name of Sole/First Inventor Christopher J. Petti

Inventor's Signature Date 4/26/96

Residence Mountain View, California 94041 Citizenship U.S.A.
(City, State) (Country)

Post Office Address 660 Sierra Avenue
Mountain View, California 94041

SAMSUNG-1002.047

Case No. 10200/12

Inventor(s): Nulty et al.

Title: METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING

POWER OF ATTORNEY

The specification of the above-identified patent application:

☒ is attached hereto
☐ was filed on _____ as application Serial No. ______

I hereby revoke all previously granted powers of attorney in the above-identified patent application and appoint the following attorneys to prosecute said patent application and to transact all business in the Patent and Trademark Office connected therewith:

Paul E. Rauch, Ph.D. – Reg. No. 38,591

Andrew D. Fortney, Ph.D. – Reg. No. 34,600

Please address all correspondence and telephone calls to Paul E. Rauch, Ph.D. in care of:

Brinks Hofer Gilson & Lione
P.O. Box 10395
Chicago, IL 60610
(312)321-4200

Cypress Semiconductor Corp., a Delaware corporation, certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

☒ An assignment from the inventor(s) of the patent application identified above, a copy of which is attached hereto.
OR

☐ An assignment from the inventor(s) of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Reel _____, frame _____.
OR

☐ A chain of title from the inventor(s), of the patent application identified above, to the current assignee as shown below:

1. From _____ To: _____
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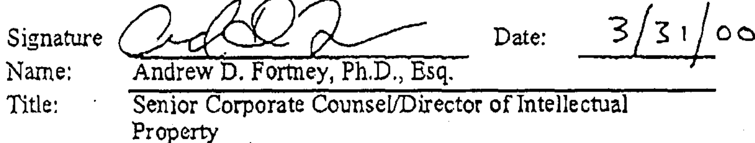
☐ Additional documents in the chain of title are listed on a supplemental sheet.

The undersigned has reviewed the assignment or all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.



Signature _______________ Date: 3/31/00
Name: Andrew D. Fortney, Ph.D., Esq.
Title: Senior Corporate Counsel/Director of Intellectual Property

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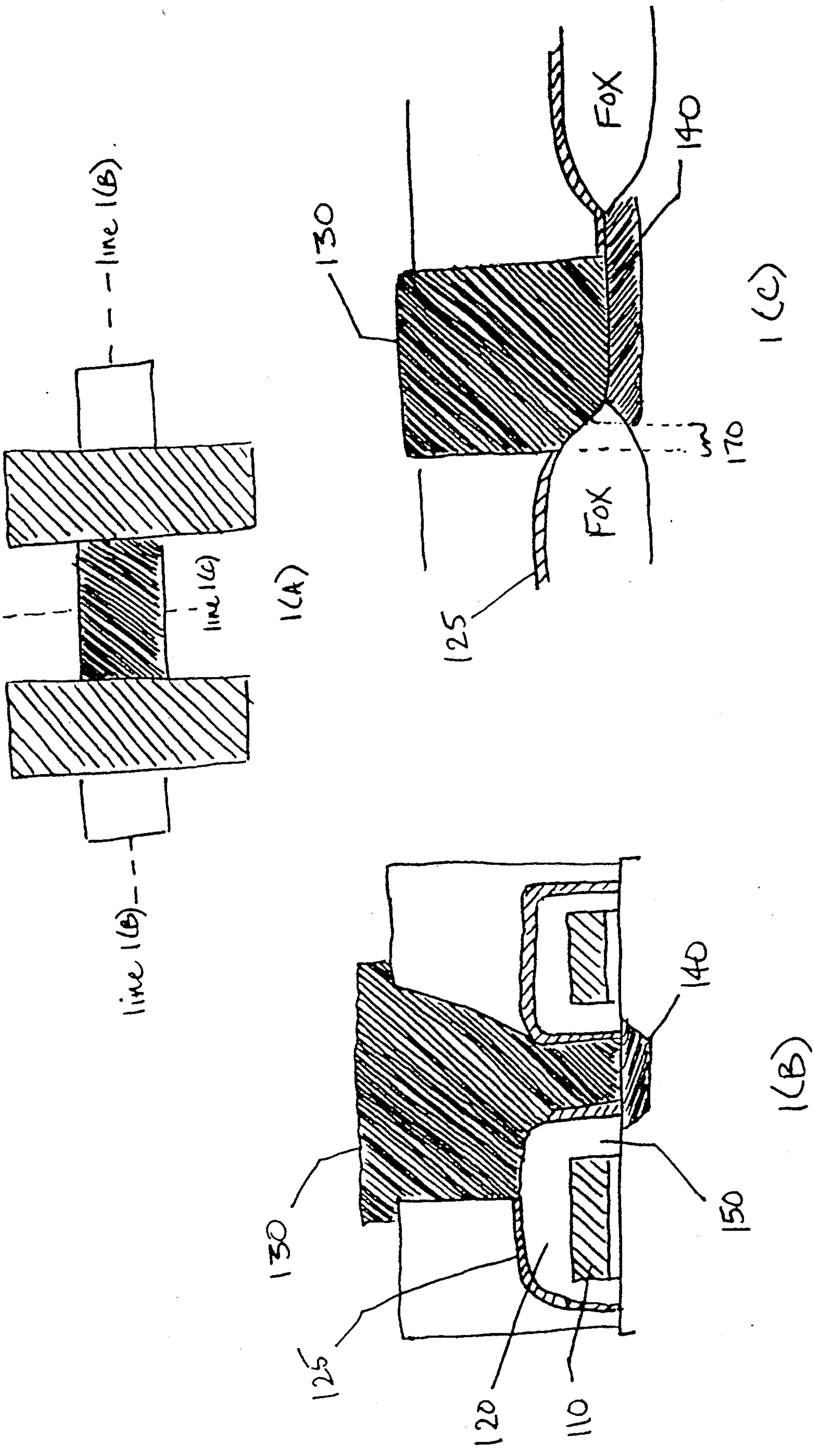


FIGURE 1

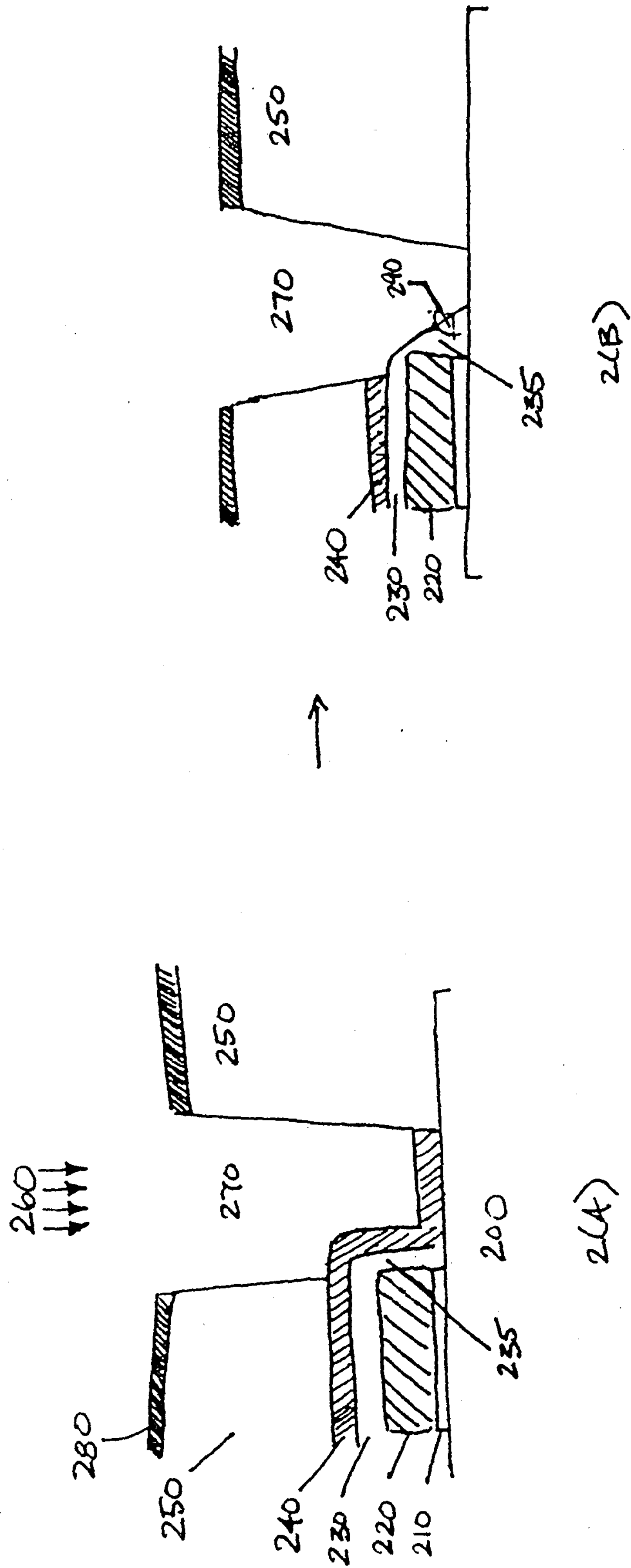


FIGURE 2

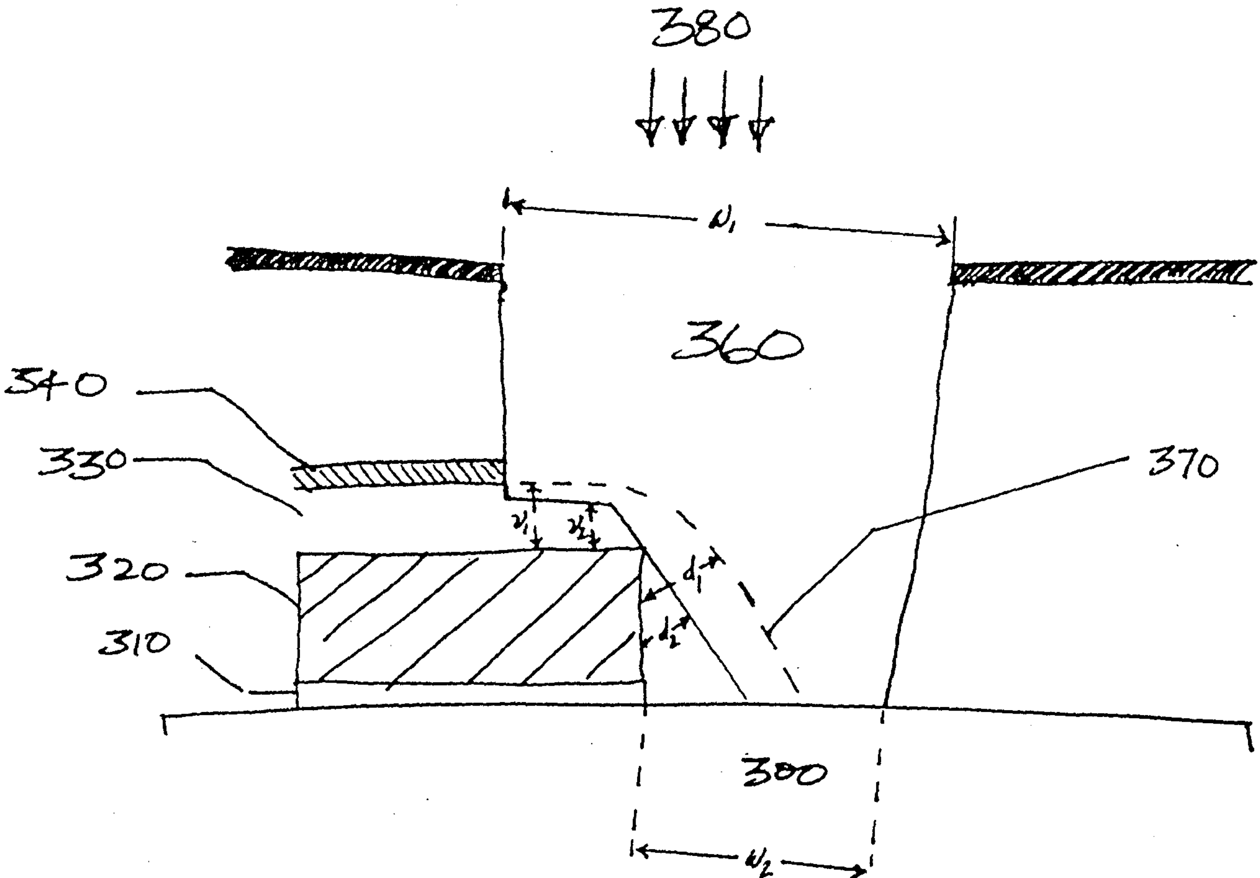
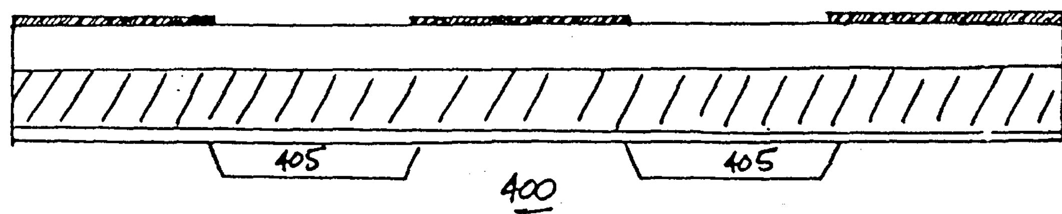
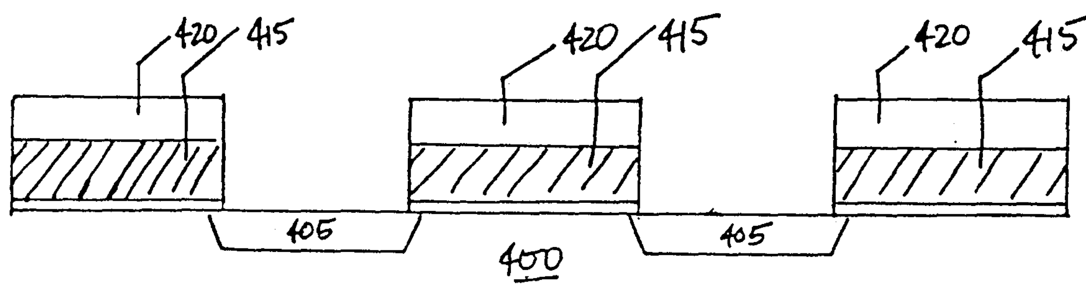
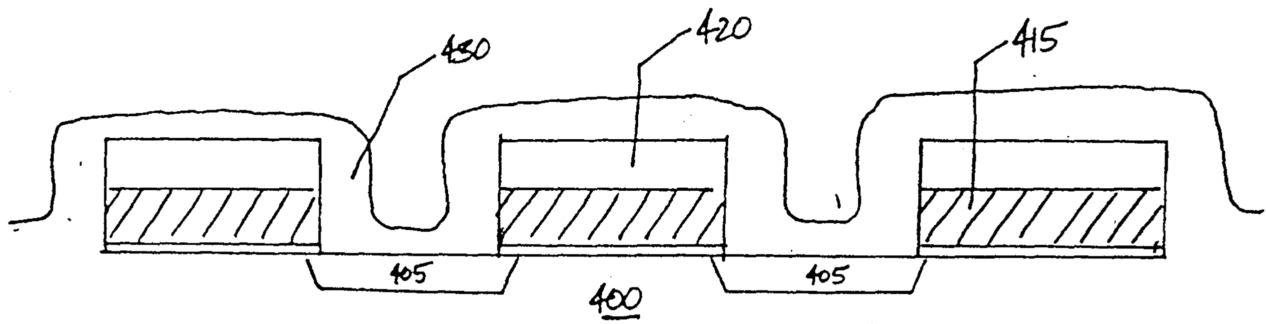
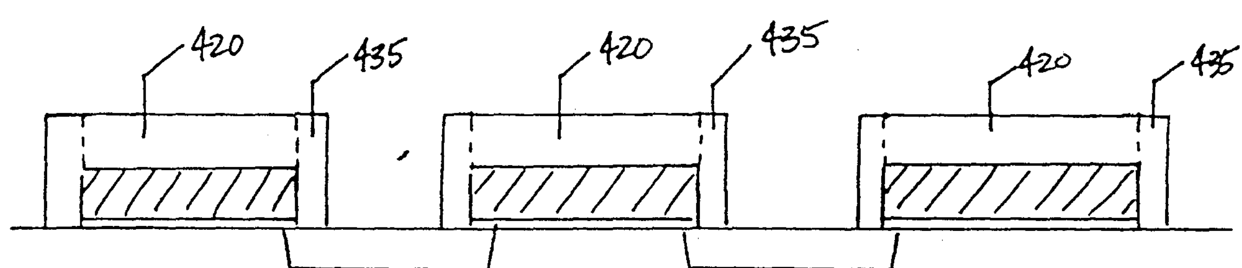


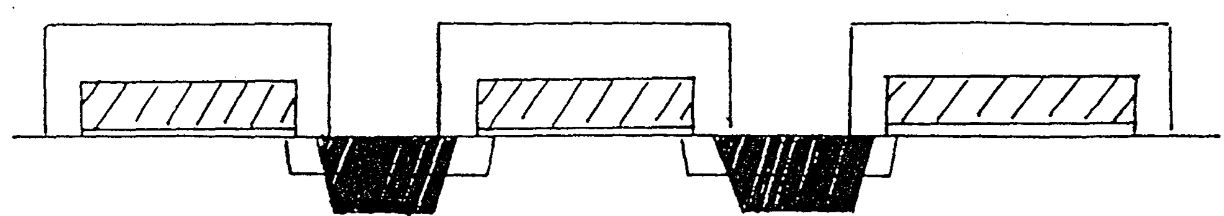
FIGURE 3











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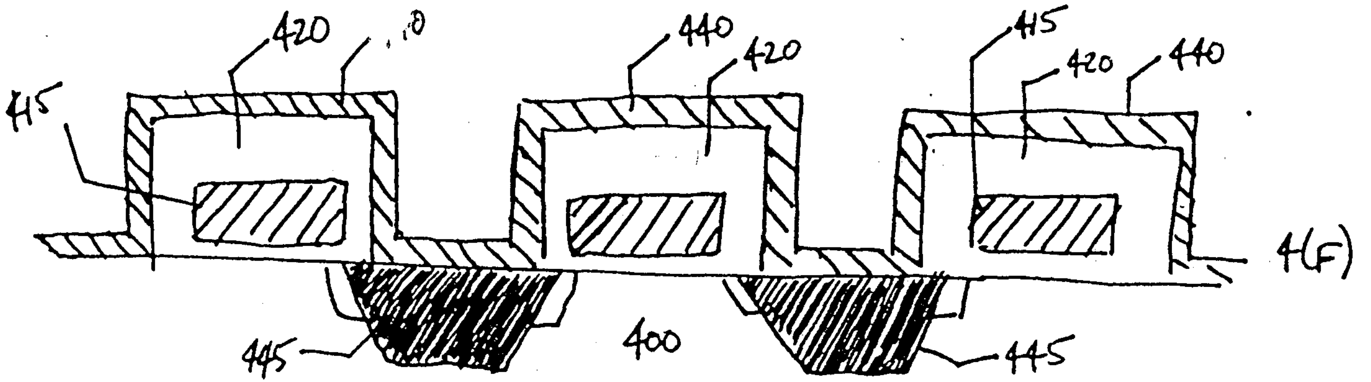

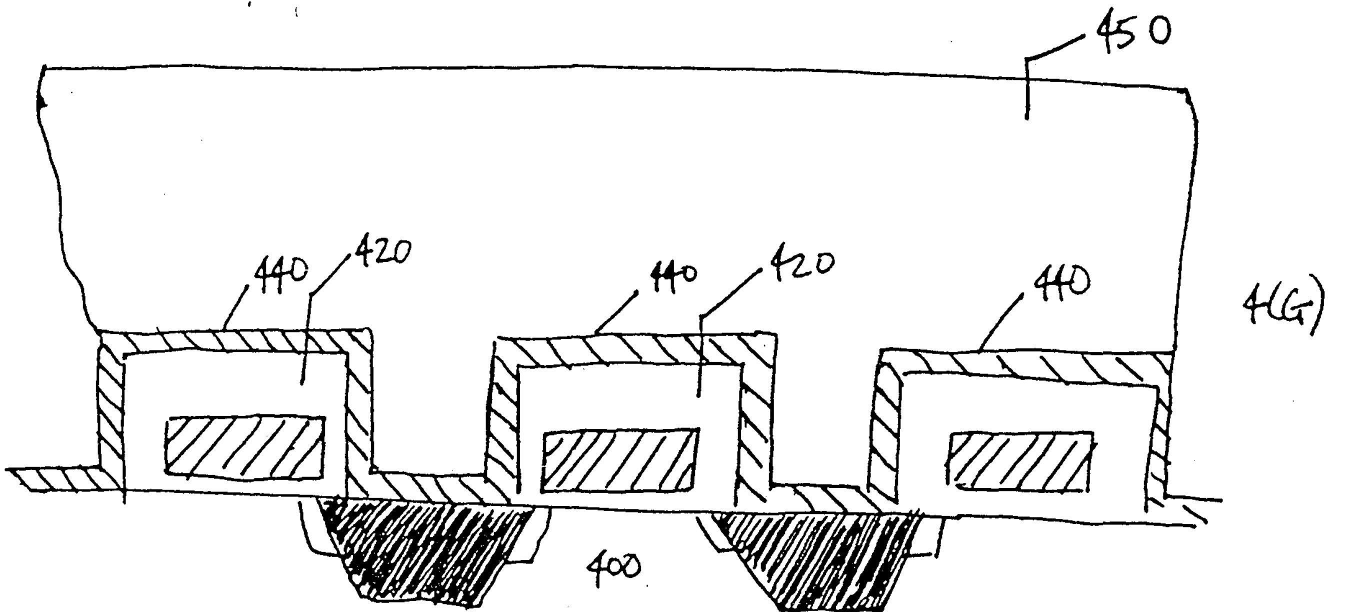

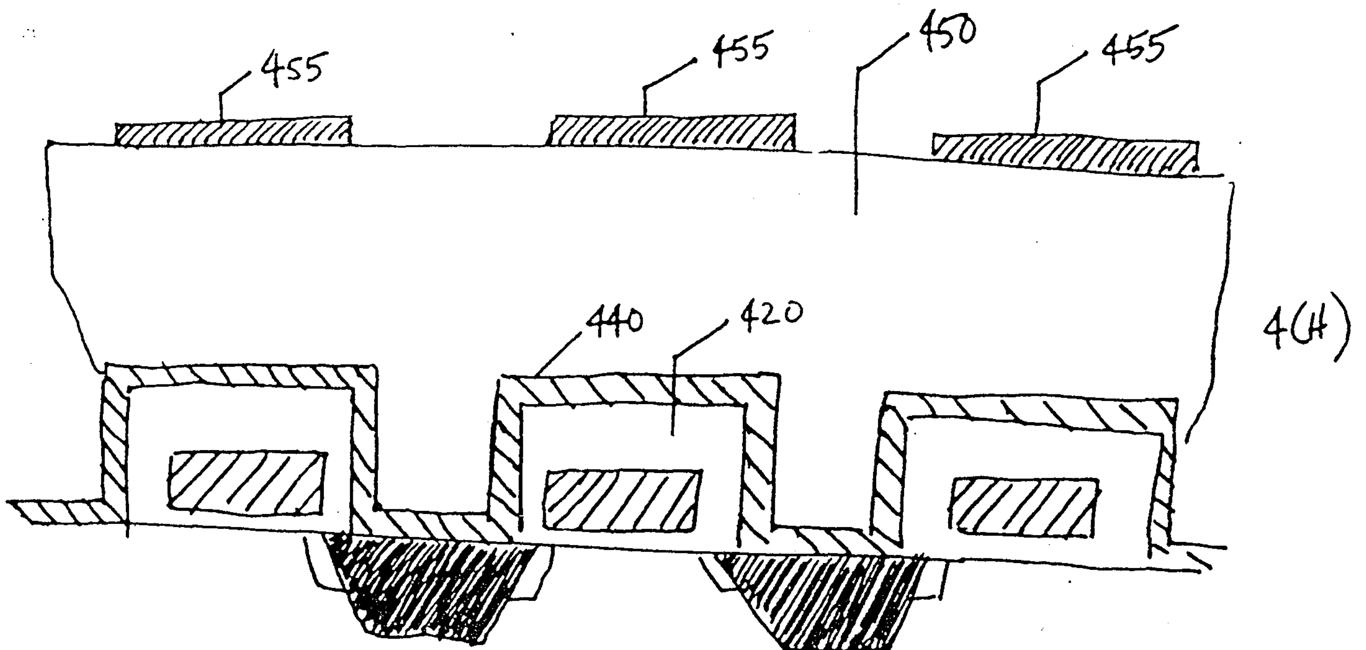

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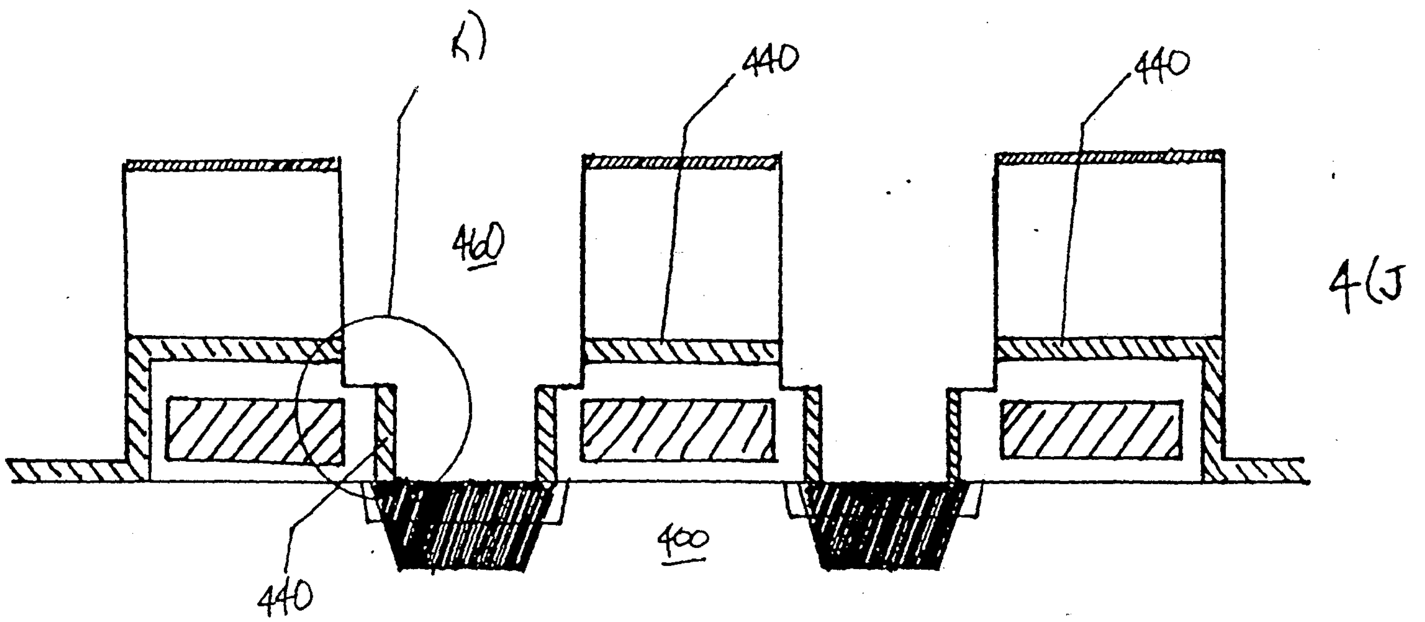
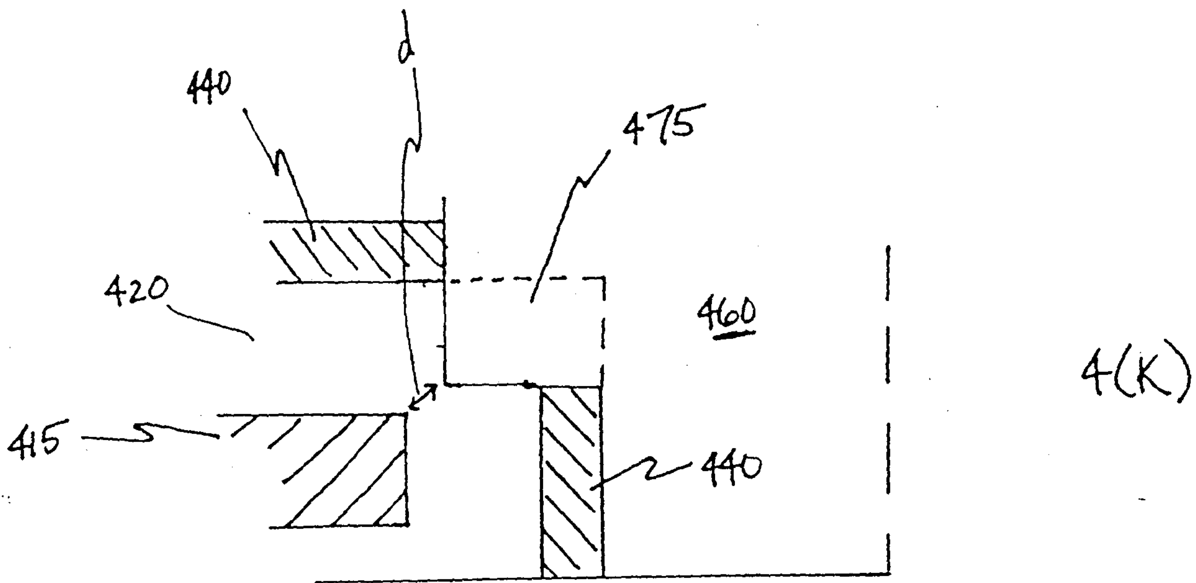
455 450 440 450

440 460 465 4(I)

420 415

FIGURE 4 (cont.)





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480

4C

440

420

415

h

400

w

w

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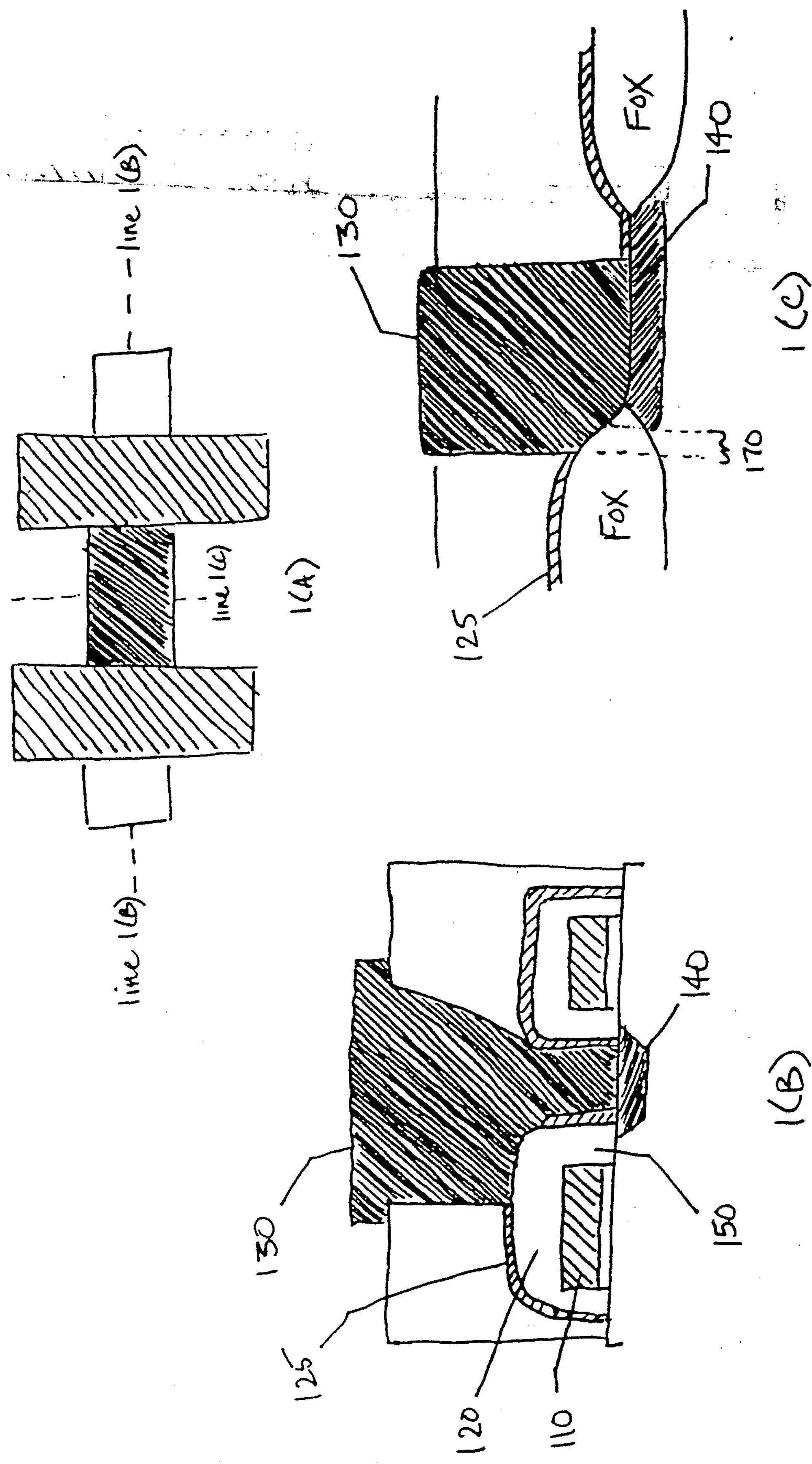

FIGURE 1

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250
270
240
235
2(B)
240
230
220

260
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200
235
2(A)
280
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230
220
210

FIGURE 2

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380

w_1

360

340

330

320

310

370

d_1

d_2

300

w_2

FIGURE 3

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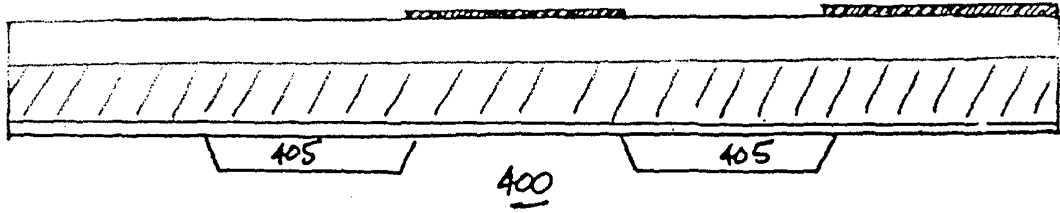

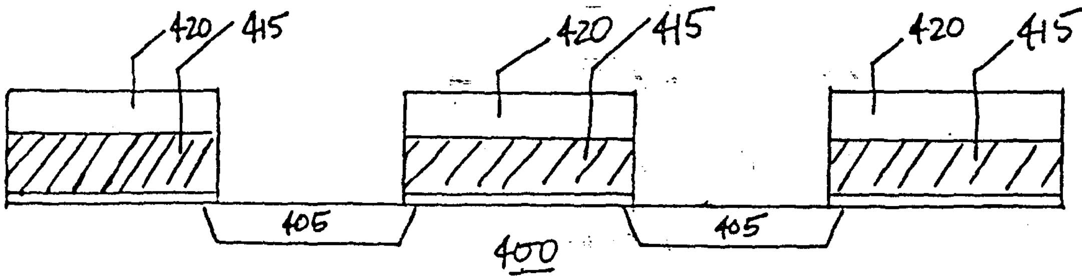

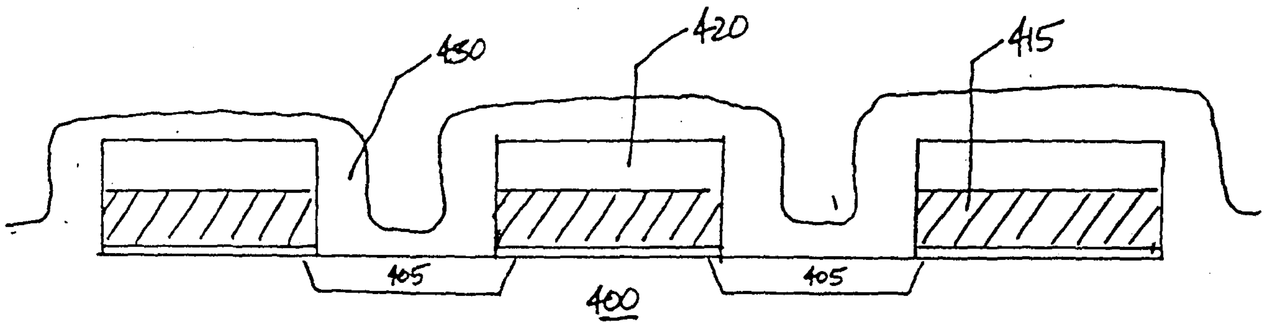

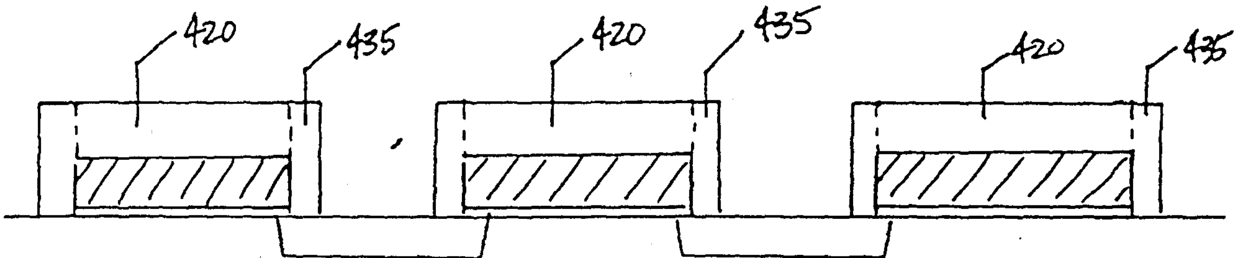

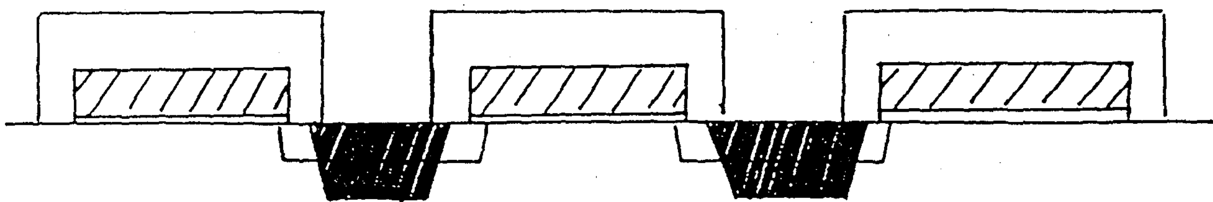

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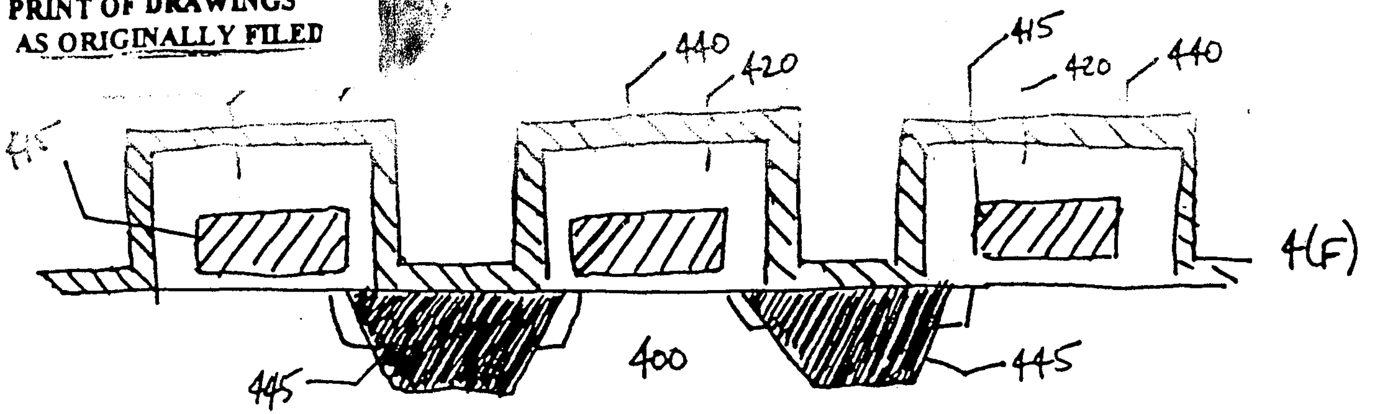

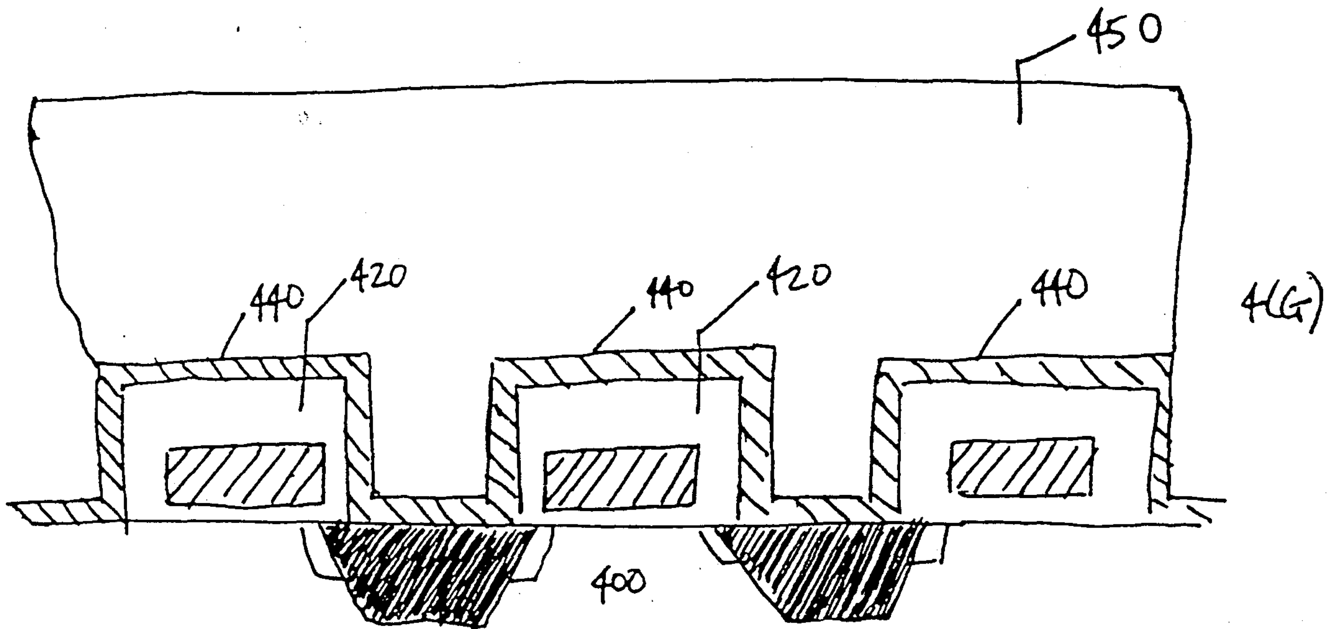

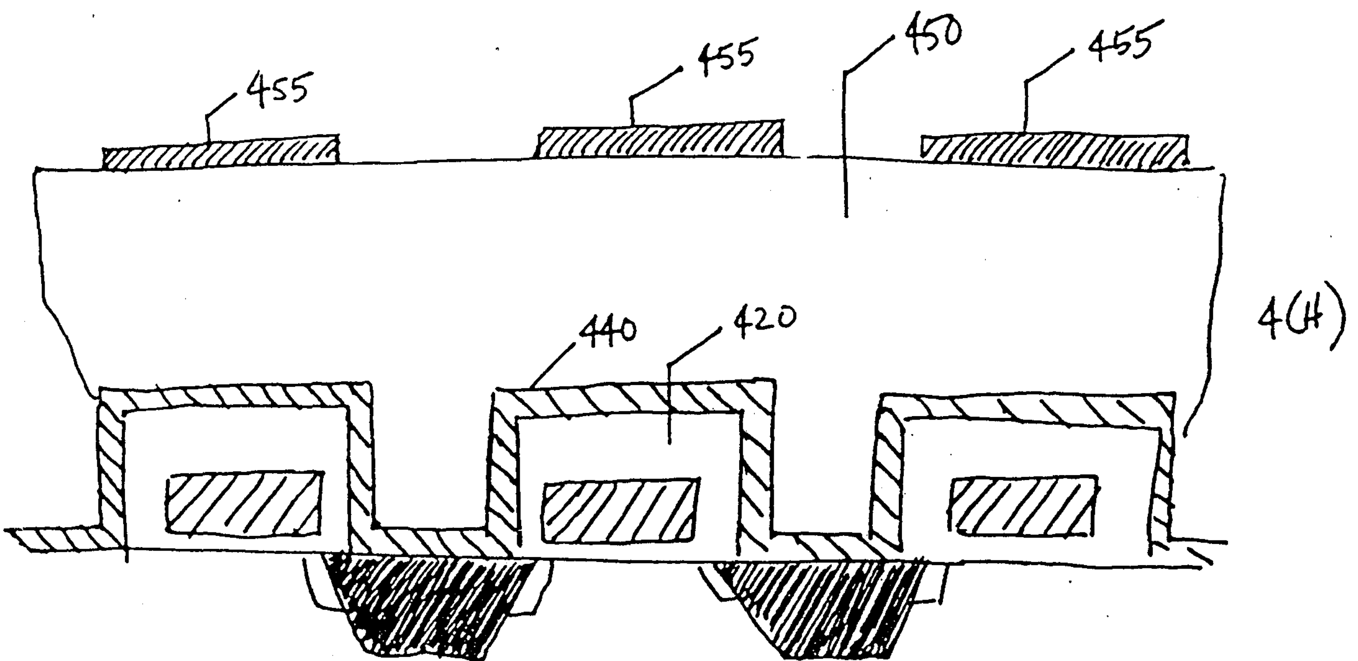

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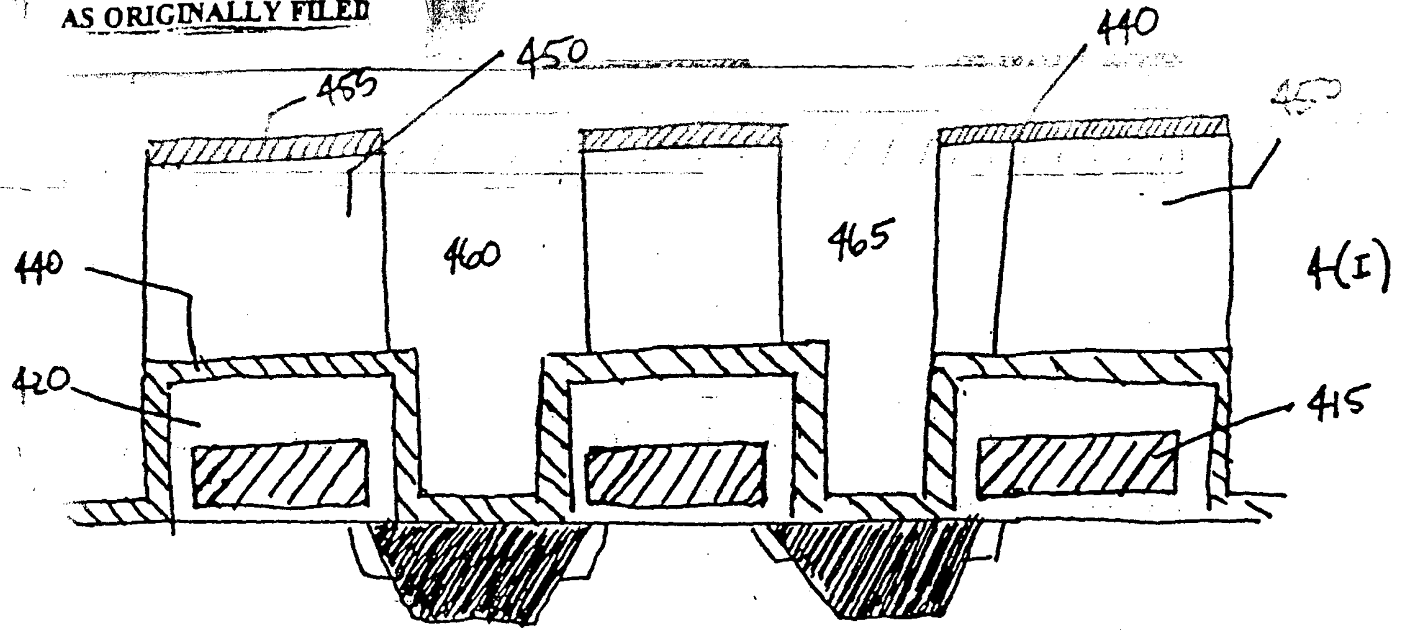

FIGURE 4 (cont.)

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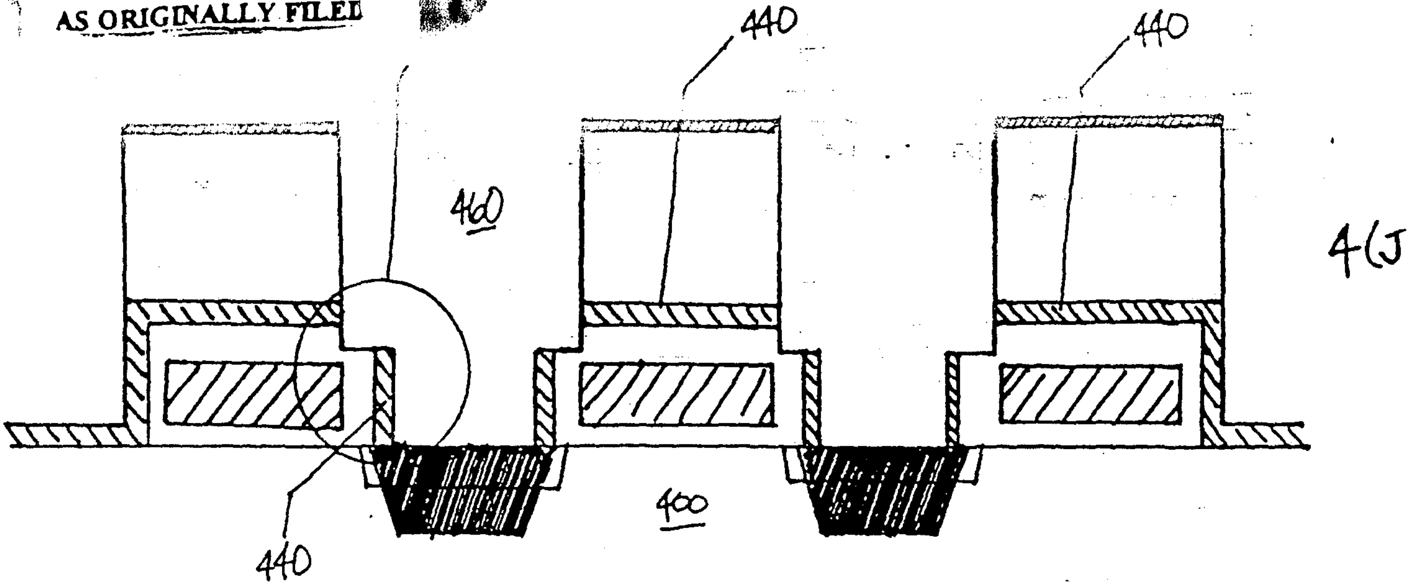

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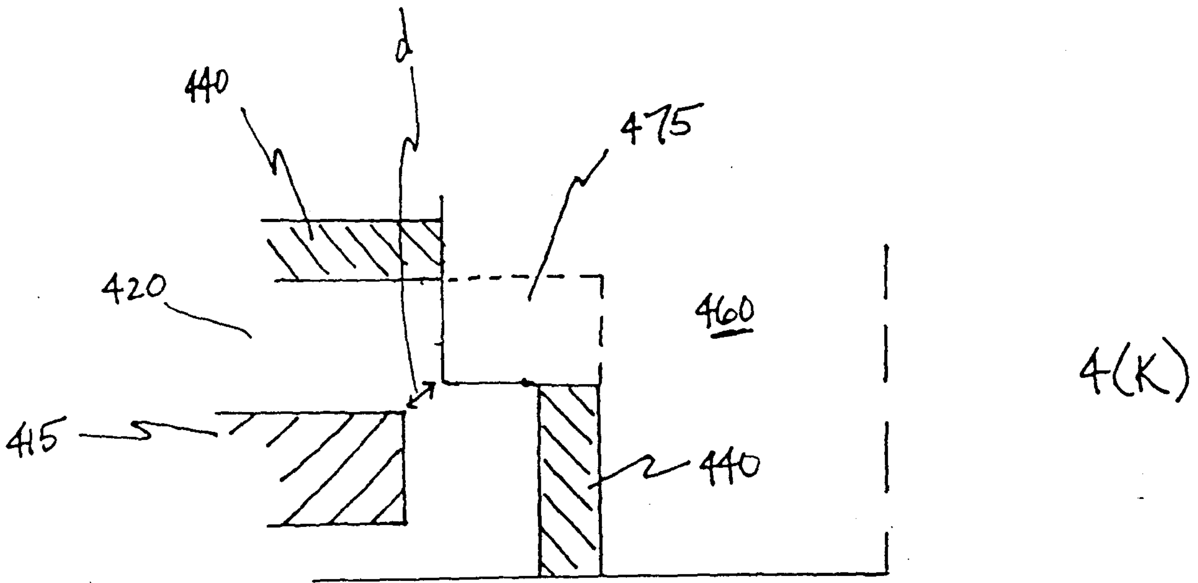

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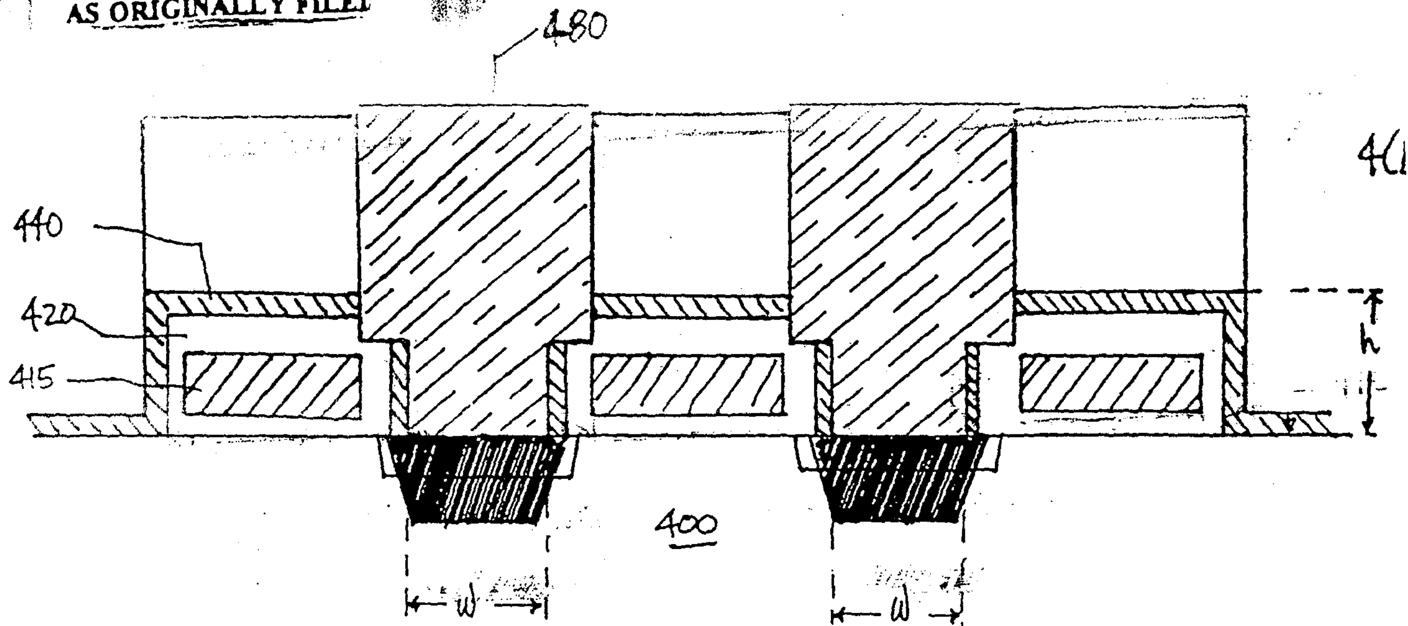

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#2 6-12-00 P.R. PRE. Amdt A

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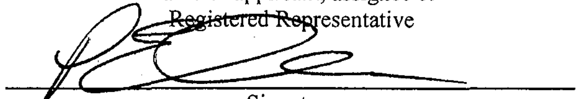
Date of Deposit

Paul E. Rauch, Ph.D.

Name of applicant, assignee or Registered Representative



Signature

March 31, 2000

Date of Signature

Our Case No. 10200/12

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)
Nulty et al.	)
	) Examiner
	) Group Art Unit No.
Filing Date: Filed herewith	)
For METHOD FOR ELIMINATING LATERAL SPACER EROSION ON ENCLOSED CONTACT TOPOGRAPHIES DURING RF SPUTTER CLEANING	)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to examination on the merits, please amend the above-identified application as follows:

IN THE TITLE

Please replace the title with the following: --STRUCTURE HAVING REDUCED LATERAL SPACER EROSION--.

IN THE CLAIMS

Please amend the claims as follows:

Please cancel Claims 1-24, without prejudice to their further prosecution in a Divisional and/or Continuation application.

Claims 25-26, line 2 of each, please change "is" to --comprises--.

Please add the following new claims:

27. A structure, comprising:

(a) a conductive layer disposed over a substrate;

(b) a first insulating layer on the conductive layer;

(c) a contact region in said first insulating layer;

(d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and

(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being distinct from the insulating spacer.

28. The structure of Claim 27, wherein the insulating spacer has a substantially rectangular profile in the contact region.

29. The structure of Claim 27, wherein the insulating spacer has a surface portion in the contact region without overlying etch stop material.

30. The structure of Claim 29, wherein the insulating spacer surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said substrate.

31. The structure of Claim 28, wherein the insulating spacer has a surface portion in the contact region without overlying etch stop material.

SAMSUNG-1002.066

Cont. A1

sub D2

32. The structure of Claim 27, further comprising a second insulating layer on the etch stop layer and over the conductive layer.

33. The structure of Claim 32, further comprising a second conductive material in the contact region.

sub E20

34. A structure, comprising the steps of:

(a) a first electrically conductive material formed in and/or on a surface of a substrate;

(b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate;

(c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material;

(d) an etch stop layer over the electrically insulative spacer and the first and second electrically conductive regions;

(e) a blanket layer over the etch stop layer; and

(f) an opening through a first part of the etch stop layer to the first electrically conductive region.

35. The structure of Claim 34, wherein the electrically insulative spacer has a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular ~~to the substrate surface.~~

sub D27

36. The structure of Claim 34, wherein the electrically insulating spacer has a surface portion without overlying etch stop material.

37. The structure of Claim 36, wherein the electrically insulating spacer surface portion without overlying etch stop material comprises a surface portion most distant from said substrate.

38. The structure of Claim 34, further comprising a second insulating layer on the etch stop layer and over the conductive layer.

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Cont'd A1

39. The structure of Claim 38, further comprising a second conductive material in the contact region.

REMARKS

Applicants submit the application is now in condition for examination on the merits. Early notice of such action is earnestly solicited.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicant

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200

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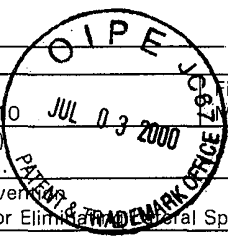


TRANSMITTAL LETTER			Case No. 10200/12
Serial No. 09/540,610	Filing Date March 31, 2000	Examiner	Group Art Unit
Inventor(s) Nulty et al.			
Title of Invention Method For Eliminating Lateral Spacer Erosion On Enclosed Contact Topographies RF Sputter			

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is Transmittal Letter (in duplicate); Information Disclosure Statement; PTO Form 1449; One Copy of References A1-A25.

☐ Small entity status of this application under 37 CFR § 1.27 has been established by verified statement previously submitted.

☐ A verified statement to establish small entity status under 37 CFR §§ 1.9 and 1.27 is enclosed.

☐ Petition for a ______month extension of time.

☒ No additional fee is required.

☐ The fee has been calculated as shown below:

	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra	Small Entity Rate	Small Entity Add'l Fee	or	Other Than Small Entity Rate	Other Than Small Entity Add'l Fee
Total		Minus			x $9 =			x $18 =	
Indep.		Minus			x 39 =			x $78 =	
First Presentation of Multiple Dep. Claim					+ $130 =			+ $260 =	
					Total add'l fee	$		total add'l fee	$

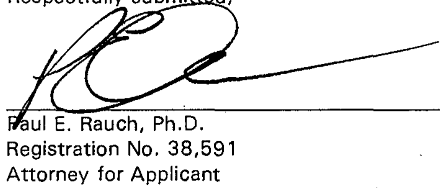
☐ Please charge Deposit Account No. 23-1925 (BRINKS HOFER GILSON & LIONE) in the amount of $_____. A duplicate copy of this sheet is enclosed.

☐ A check in the amount of $_____ to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge payment of any additional filing fees required under 37 CFR § 1.16 and any patent application processing fees under 37 CFR § 1.17 associated with this communication or credit any overpayment to Deposit Account No. 23-1925. A duplicate copy of this sheet is enclosed.

☒ I hereby petition under 37 CFR § 1.136(a) for any extension of time required to ensure that this paper is timely filed. Please charge any associated fees which have not otherwise been paid to Deposit Account No. 23-1925. A duplicate copy of this sheet is enclosed.

Respectfully submitted,



Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicant

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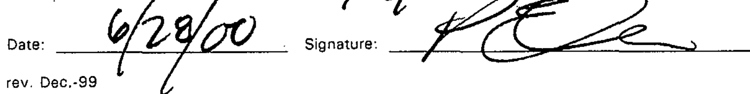
BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on 6/28/00



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Paul E. Rauch, Ph.D., Reg. No. 38,591
Name of Applicant, Assignee or Registered Representative

Signature

Our Case No. 10200/12

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Nulty et al.

Serial No. 09/540,610

Filing Date: March 31, 2000

For METHOD FOR ELIMINATING LATERAL SPACER EROSIION ON ENCLOSED CONTACT TOPOGRAPHIES RF SPUTTER CLEANING

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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Pursuant to the obligation under 37 C.F.R. 1.56 and in conformance with 37 C.F.R. 1.97-1.99, Applicants hereby submit references A1-A25 listed on the attached form PTO-1449 for consideration by the Examiner. Copies of the references are enclosed herewith.

The filing of this Information Disclosure Statement does not constitute an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. Section 1.56(b). Further, Applicants reserve the right to contest these references as prior art against the present application, and

Applicants do not believe that the disclosure of these references, even if finally determined to be prior art, anticipates Applicants' invention or that these references make Applicants' invention obvious.

Applicants respectfully request that the Examiner review the entire disclosure of these documents and make them of record.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicants

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200

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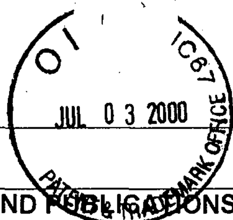

FORM PTO-1449	SERIAL NO. 09/540,610	CASE NO. 10200-12
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE March 31, 2000	GROUP ART UNIT
(use several sheets if necessary)	APPLICANT(S): Nulty et al.	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
C.C.	A1	Re.35,111	12/05/95	~~Lion et al.~~ Liou et al.	438/595	11/1992
C.C.	A2	4,660,276	04/28/87	Hsu	438/595	8/1985
C.C.	A3	4,806,201	02/21/89	Mitchell et al.	438/595	3/1988
C.C.	A4	4,956,312	09/1990	Van Laarhoven	437/180	5/1989
C.C.	A5	5,037,777	08/06/91	Mele et al.	43/639	7/1990
C.C.	A6	5,100,838	03/1992	Dennison	437/195	10/1990
C.C.	A7	5,166,096	11/24/92	Cote et al.	438/595	11/1992
C.C.	A8	5,264,341	11/23/93	~~Son et al.~~ Maciak et al.	435/7.21	8/1989
C.C.	A9	5,275,972	1/04/94	Ogawa et al.	43/639	8/1992
C.C.	A10	5,306,952	04/26/94	Matsuura et al.	257/165	10/1992
C.C.	A11	5,364,817	11/15/94	~~Lo et al.~~ Lur et al.	437/190	5/1994
C.C.	A12	5,366,929	11/22/94	Cleeves et al.	437/195	5/1993
C.C.	A13	5,378,646	01/03/95	Huang et al.	438/595	7/1994
C.C.	A14	5,382,483	01/17/95	Young	430/5	1/1992
C.C.	A15	5,384,281	01/25/95	Kenney et al.	437/189	Dec. 29, 1992
C.C.	A16	5,466,636	11/14/95	Cronin et al.	43/639	9/1992
C.C.	A17	5,482,894	01/1996	Havemann	437/195	1/1996
C.C.	A18	5,521,121	05/28/96	Tsai et al.	437/190	4/1995
C.C.	A19	5,562,801	10/08/96	Nulty	156/643.1	12/1994
C.C.	A20	5,569,628	10/29/96	Yano et al.	437/190	10/1996
C.C.	A21	5,587,331	12/24/96	Jun	437/190	12/1996
C.C.	A22	5,756,396	05/1998	Lee et al.	438/622	5/1998
C.C.	A23	5,759,867	04/21/95	Armacost et al.	438/634	6/1998

EXAMINER INITIAL		OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)
C.C.	A24	J. Givens et al., "Selective dry etching in a high density plasma for 0.5 µm complimentary metal-oxide-semiconductor technology," J. Vac. Sci. Technol. B 12(1), Jan/Feb 1994, pp. 427-432.
C.C.	A25	K.K. Shih et al., "Hafnium dioxide etch-stop layer for phase-shifting masks," J. Vac. Sci. Technol. B 11(6), Nov/Dec 1993, pp. 2130-2131.

EXAMINER [signature]	DATE CONSIDERED May 30, 2001

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/540,610	03/31/00	NULTY	J	16820.P097

MMC1/0601

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES CA 90025

EXAMINER	
CHU, C	
ART UNIT	**PAPER NUMBER**
2815	4

DATE MAILED: 06/01/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev.11/00)

1- File Copy

Office Action Summary	Application No. 09/540,610	Applicant(s) NULTY ET AL.	
	Examiner Chris C. Chu	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _25 - 39_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _25 - 39_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _31 March 2000_ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _3_ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

1. The preliminary amendment, which is filed on March 31, 2000, has been entered.

2. This application discloses and claims only subject matter disclosed in prior Application No. 08577751, filed Dec. 22, 1995, (now Patent No. 6066555, issued May 23, 2000) and names an inventor or inventors named in the prior application. Accordingly, this application may constitute a continuation or division. Should applicant desire to obtain the benefit of the filing date of the prior application, attention is directed to 35 U.S.C. 120 and 37 CFR 1.78.

Drawings

3. Figures 1 ~ 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the contact region in the first insulating layer must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: reference number "455" in Fig. 4H is not disclosed in the specification. Correction is required.

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

On page 20, line 15 and line 17 of the specification refers to conducting layer “320.”

On page 20, line 20 of the specification refers to the dielectric layer “410.”

On page 21, line 13 of the specification refers to a photoresist masking layer “425.”

On page 23, line 6 of the specification refers to the silicon nitride etch stop layer “340.”

On page 24, line 9 of the specification refers to a photoresist material “470.”

On page 27, line 8 of the specification refers to a height “h1.”

On page 27, line 9 of the specification refers to a width “w1.”

Above reference signs are not referenced in the figures.

Correction is required.

7. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the application is allowed by the examiner.

Specification

8. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 250 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

9. The abstract of the disclosure is objected to because it contains legal phraseology such as “said” and “means”. Correction is required. See MPEP § 608.01(b).

10. The disclosure is objected to because of the following informalities:

On page 16, lines 14 ~ 18, there are two brief descriptions for Figure 3. Which brief description is the brief description of Figure 3?

On pages 24, line 3, “Figure 4(H)” should be --Figure 4(I)--. This is because, the various reference characters they designate to Figure 4(H) on the page 24 of the specification appear to be inaccurate. Base on the description, i.e., reference characters 450, 460, etc., it appears that applicant is describing Figure 4(I). Therefore, the reference to Figure 4(H) should be changed to Figure 4(I).

The disclosure is missing a detailed description of Figure 4(H).

Appropriate correction is required.

Claim Objections

11. Claims 25 and 26 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Further, since claims 25 and 26 depend from canceled

SAMSUNG-1002.077

claim, for purposes of examination claims 25 and 26 will be treated as depending from claim 27. However, correction is required as mentioned in beginning of this paragraph.

12. Claim 34 is objected to because of the following informalities: spelling error on line 6 and on line 8, "insulative" should be --insulate-- or --insulating--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

13. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. Claims 25 ~ 39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it can not be determined what the applicant regards as "a contact region in the first insulating layer." The instant specification, specifically, the description of Fig. 4(I) discloses contact regions 460 and 465. However, these contact regions are not placed in the first insulating layer 420.

Regarding claim 34, this claim appears to be an apparatus claim; therefore, it is not understood why this claim recites the phrase "the steps of" in the preamble. Further, the claim recites the limitation "the first and second electrically conductive regions" in lines 8 and 9. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 25 and 27 ~ 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Dennison et al.

Regarding claim 25, Dennison et al. discloses the etch stop layer (20) is silicon nitride (column 3, line 35).

Regarding claim 27, note Fig. 2 of Dennison et al., where the reference shows a structure (10), comprising: a conductive layer (12 and column 3, lines 29 ~ 33) disposed over a substrate; a first insulating layer (18) on the conductive layer; a contact region (the area of 34) in the first insulating layer; at least one insulating spacer (18) in the contact region adjacent to the first insulating layer (see Fig. 2); and an etch stop material (20 and column 3, line 35) over the first insulating layer and adjacent to the insulating spacer (see Fig. 2), the etch stop material being distinct from the insulating spacer (see Fig. 2 and column 3, lines 32 ~ 38).

Regarding claim 28, Fig. 2 of Dennison et al., where the reference shows the insulating spacer (18) has a substantially rectangular profile in the contact region (see Fig. 2).

Regarding claims 29 and 36, Fig. 2 of Dennison et al., where the reference shows the insulating spacer (18) has a surface portion in the contact region without overlying etch stop material (see Fig. 2).

Regarding claims 30 and 37, Fig. 2 of Dennison et al., where the reference shows the insulating spacer (18) surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from the substrate (see Fig. 2).

Regarding claim 31, Fig. 2 of Dennison et al., where the reference shows the insulating spacer (18) has a surface portion in the contact region without overlying etch stop material (see Fig. 2).

Regarding claims 32 and 38, Fig. 2 of Dennison et al., where the reference shows a structure (10), further comprising a second insulating layer (28) on the etch stop layer and over the conductive layer (see Fig. 2).

Regarding claims 33 and 39, Fig. 2A of Dennison et al., where the reference shows a structure (10), further comprising a second conductive material (40) in the contact region (see Fig. 2A).

Regarding claim 34, Fig. 2 of Dennison et al., where the reference shows a structure, comprising the step of: a first electrically conductive material (24) formed in and/or on a surface of a substrate; a contact opening (the area of 34) in a region adjacent to a second electrically conductive material (the area of 40 in Fig. 2A) formed on the substrate; an electrically insulative spacer (18) in the contact opening adjacent to the second electrically conductive material; an etch stop layer (20) over the electrically insulative spacer and the first and second electrically conductive regions (see Fig. 2); a blanket layer (28) over the etch stop layer; and an opening through a first part of the etch stop layer to the first electrically conductive region (see Fig. 2).

Regarding claim 35, Fig. 2 of Dennison et al., where the reference shows the electrically insulative spacer (18) has a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface (see Fig. 2).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dennison et al. in view of Gonzalez.

Dennison et al. discloses the claimed invention except the etch stop layer is silicon dioxide. However, Gonzalez discloses the etch stop layer is silicon dioxide (31 in Fig. 18). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Dennison et al. by using the etch stop layer is silicon dioxide as taught by Gonzalez. The ordinary artisan would have been motivated to modify Dennison et al. in the manner described above for at least the purpose of preventing diffusion of element between layers.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Howard and Kimura disclose multi-layer and contact regions in a semiconductor device.

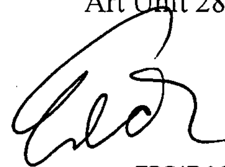
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
May 30, 2001



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

FORM PTO 948 (REV. 01-97) U.S. DEPARTMENT OF COMMERCE-Patent and Trademark Office Application No. 09/540,610

NOTICE OF DRAFTPERSON'S PATENT DRAWING REVIEW

The drawing filied (insert date) 3/31/00 are:

A. ______ not objected to by the Draftperson under 37 CFR 1.84 or 1.152.

B. X objected to by the Draftperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings whe necessary. Corrected drawings must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color.
   - ______ Color drawing are not acceptable until petition is granted. Fig.(s) ______
   - ______ Pencil and non black ink is not permitted. Fig(s) ______
2. PHOTOGRAPHS. 37 CFR 1.84(b)
   - ______ Photographs are not acceptable until petition is granted,
   - ______ 3 full-tone sets are required. Fig(s) ______
   - ______ Photographs not properly mounted (must brystol board or photographic double-weight paper). Fig(s) ______
   - ______ Poor quailty (half-tone). Fig(s) ______
3. TYPE OF PAPER. 37 CFR 1.84(e)
   - ______ Paper not flexible, strong, white and durable. Fig.(s) ______
   - ______ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not acceptable. (too thin)
   - ______ Mylar, vellum paper is not acceptable (too thin). Fig(s) ______
4. SIZE OF PAPER. 37 CFR 1.84(F): Acceptable sizes:
   - ______ 21.0 cm by 29.7 cm (DIN size A4)
   - ______ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   - ______ All drawings sheets not the same size. Sheet(s) ______
5. MARGINS. 37 CFR 18.4(g): Acceptable margins:
   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: A4 Size
   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: 8 1/2 x 11
   - X Margins not acceptable. Fig(s) 1A, 1B, 4A-4L
   - X Top (T) X Left (L)
   - X Right (R) X Bottom (B)
6. VIEWS. CFR 1.84(h)
   REMINDER: Specification may require revision to correspond to drawing changes.
   - ______ Views connected by projection lines or lead lines. Fig.(s) ______

   Partial views. 37 CFR 1.84(h)(2)
   - ______ Brackets needed to show figure as one entity. Fig.(s) ______
   - X Views not labeled separately or properly. Fig.(s) 1, 2, 4
   - ______ Enlarged view not labeled separately or properly. Fig.(s) ______
7. SECTIONAL VIEWS. 37 CFR 1.84(h)(3)
   - ______ Hatching not indicated for sectional portions of an object. Fig.(s) ______
   - ______ Sectional designation should be noted with Arabic or Roman numbers. Fig.(s) ______
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   - ______ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned, so that the top becomes the right side, except for graphs. Fig.(s) ______
   - ______ Views not on the same plane on drawing sheet. Fig.(s) ______
9. SCALE. 37 CFR 1.84(k)
   - ______ Scale not large enough to show mechansim with crowding when drawing is reduced in size to two-thirds in reproduction. Fig.(s) ______
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)
    - X Lines, numbers & letters not uniformly thick and well defined, clean, durable and black (poor line quality). Fig.(s) 1-4L
11. SHADING. 37 CFR 1.84(m)
    - ______ Solid black areas pale. Fig.(s) ______
    - ______ Solid black shading not permitted. Fig.(s) ______
    - ______ Shade lines, pale, rough and blurred. Fig.(s)
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.48(p)
    - X Numbers and reference characters not plain and legible. Fig.(s) 1-4L
    - X Figure legends are poor. Fig.(s) 1-4L
    - ______ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(3) Fig.(s) ______
    - ______ English alphabet not used. 37 CFR 1.84(p)(3) Fig.(s) ______
    - ______ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig.(s) ______
13. LEAD LINES. 37 CFR 1.84(q)
    - ______ Lead lines cross each other. Fig.(s) ______
    - ______ Lead lines missing. Fig.(s) ______
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.48(t)
    - ______ Sheets not numbered consecutively, and in Ababic numerals beginning with number 1. Fig.(s) ______
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    - ______ Views not numbered consecutively, and in Abrabic numerals, beginning with number 1. Fig.(s) ______
16. CORRECTIONS. 37 CFR 1.84(w)
    - ______ Corrections not made from PTO-948 dated ______
17. DESIGN DRAWINGS. 37 CFR 1.152
    - ______ Surface shading shown not appropriate. Fig.(s) ______
    - ______ Solid black shading not used for color contrast. Fig.(s) ______

COMMENTS

REVIEWER ______ DATE 5/30/01 TELEPHONE NO. 308-2011

ATTACHMENT TO PAPER NO. 4

PTO COPY

REMINDER

Drawing changes may also require changes in the specification, e.g., if Fig. I is changed to Fig. IA, Fig. IB, Fig. IC, etc., the specification, at the Brief Description of the Drawings, must likewise be changed. Please make such changes by 37 CFR 1.312 Amendment at the time of submitting drawing changes.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities--37 CFR 1.85

File new drawings with the changes incorporated therein. The application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application, should be placed on the back of each sheet of drawings in accordance with 37 CFR I .84(c). Applicant may delay filing of the new drawings until receipt of the Notice of Allowability (PTOL-37). Extensions of time may be obtained under the provisions of 37 CFR 1 .136. The drawing should be filed as a separate paper with a transmittal letter addressed to the Drawing Review Branch.

2. Timing of Corrections

Applicant is required to submit **acceptable** corrected drawings within the three-month shortened statutory period set in the Notice of Allowability (PTOL-37). If a correction is determined to be unacceptable by the Office, applicant must arrange to have acceptable correction resubmitted within the original three-month period to avoid the necessity of obtaining as extension of time and paying the extension fee. Therefore, applicant should file corrected drawings as soon as possible.

Failure to take corrective action within set (or extended) period will result in **ABANDONMENT** of the Application.

3. Corrections other than Informalities Noted by the Drawing Review Branch on the Form PTO 948

All changes to the drawings, other than informalities noted by the Drawing Review Branch, **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Notice of References Cited	Application/Control No. 09/540,610	Applicant(s)/Patent Under Reexamination NULTY ET AL.	
	Examiner Chris C. Chu	Art Unit 2815	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification	
	A	US-5338700-A	08-1994	Dennison et al.	438	253
	B	US-5234856-A	08-1993	Gonzales	438	244
	C	US-6046505-A	04-2000	Howard	257	776
	D	US- -				
	E	US- -				
	F	US- -				
	G	US- -				
	H	US- -				
	I	US- -				
	J	US- -				
	K	US- -				
	L	US- -				
	M	US- -				

FOREIGN PATENT DOCUMENTS

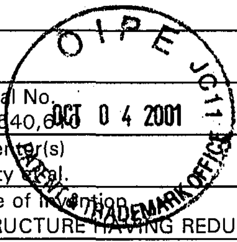
*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification	
	N	JP-11111691-A	04-1999	Japan	Kimura	---	---
	O	- -					
	P	- -					
	Q	- -					
	R	- -					
	S	- -					
	T	- -					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

$2815



Serial No. 09/540,640	Filing Date March 31, 2000	Examiner Chris C. Chu	Group Art Unit 2815

TRANSMITTAL LETTER — Case No. 10200/12, Client Ref. No. PM95012D

Inventor(s): Nulty et al.

Title of Invention: STRUCTURE HAVING REDUCED LATERAL SPACER EROSION

TO THE COMMISSIONER FOR PATENTS

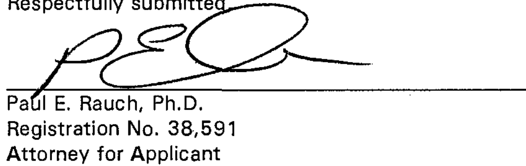
Transmitted herewith is Transmittal Letter (in duplicate), Amendment and Response, Petition for One (1) Month Extension of Time, Check for $110 and Return Postcard.

- [ ] Small entity status of this application under 37 CFR § 1.27 has been established by verified statement previously submitted.
- [ ] A verified statement to establish small entity status under 37 CFR §§ 1.9 and 1.27 is enclosed.
- [x] Petition for a one month extension of time.
- [x] No additional fee is required.
- [ ] The fee has been calculated as shown below:

	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra	Small Entity Rate	Small Entity Add'l Fee	or	Other Than Small Entity Rate	Other Than Small Entity Add'l Fee
Total		Minus			x $9=			x $18=	
Indep.		Minus			x 42=			x $84=	
First Presentation of Multiple Dep. Claim					+$140 =			+$280=	
					Total add'l fee	$		Total add'l fee	$

- [ ] Please charge Deposit Account No. 23-1925 (BRINKS HOFER GILSON & LIONE) in the amount of $_____. A duplicate copy of this sheet is enclosed.
- [x] A check in the amount of $110 to cover the filing fee is enclosed.
- [x] The Commissioner is hereby authorized to charge payment of any additional filing fees required under 37 CFR § 1.16 and any patent application processing fees under 37 CFR § 1.17 associated with this communication or credit any overpayment to Deposit Account No. 23-1925. A duplicate copy of this sheet is enclosed.
- [x] I hereby petition under 37 CFR § 1.136(a) for any extension of time required to ensure that this paper is timely filed. Please charge any associated fees which have not otherwise been paid to Deposit Account No. 23-1925. A duplicate copy of this sheet is enclosed.

Respectfully submitted,



Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicant

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on October 1, 2001.

Date: 10/1/01 Signature:

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Date of Deposit

Paul E. Rauch, Ph.D. – Reg. No. 38,591

Name of applicant, assignee or Registered Representative

Signature

10/1/01

Date of Signature

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BHGL Case No. 10200/12
Client Ref. No. PM95012D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Nulty et al.

Serial No: 09/540,610

Filed: March 31, 2000

For: STRUCTURE HAVING REDUCED LATERAL SPACER EROSION

Examiner: Chris C.Chu

Group Art Unit: 2815

PETITION AND FEE FOR EXTENSION OF TIME (37 CFR § 1.136(a))

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This is a petition for an extension of the time to respond to Office Action dated June 1, 2001 for a period of 1 month.

☒ Applicant is:
- ☐ a small entity, verified statement is:
  - ☐ attached
  - ☐ already filed

10/05/2001 HVUONG1 00000126 09540610

01 FC:115 110.00 OP

☒ other than small entity

	Extension Months	**Other Than Small Entity**	**Small Entity**
☒	One Month	$110.00	$55.00
☐	Two Months	$400.00	$200.00
☐	Three Months	$920.00	$460.00
☐	Four Months	$1,440.00	$720.00
☐	Five Months	$1,960.00	$980.00

Fee Payment

☒ Attached is a check for $110 for the Petition fee.
☐ Charge Petition fee to Deposit Account No. 23-1925. A duplicate copy of this Petition is attached.
☒ Charge any additional fee required or credit for any excess fee paid to Deposit Account No. 23-1925. A duplicate copy of this Petition is attached.

Respectfully submitted,

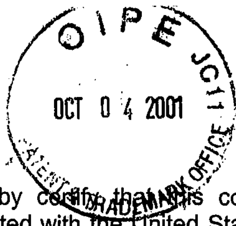
Dated: October 1, 2001

Paul E. Rauch
Registration No. 38,591
Attorney for Applicant

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, IL 60610
(312) 321-4200

Rev. Oct.-01

SAMSUNG-1002.088



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Commissioner for Patents
Washington, D.C. 20231
on October 1, 2001
Date of Deposit

Paul E. Rauch, Ph.D., Reg. No. 38,591
Name of applicant, assignee or Registered Representative

Signature
October 1, 2001
Date of Signature

#6/B 11/9/01

Our Case No. 10200/12
Client Ref. No. PM95012D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Nulty et al.

Serial No. 09/540,610

Filing Date: March 31, 2000

For STRUCTURE HAVING REDUCED LATERAL SPACER EROSION

Examiner Chris C. Chu

Group Art Unit No. 2815

AMENDMENT AND RESPONSE

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Responsive to the Office Action mailed June 1, 2001, Applicants respectfully request reconsideration in light of the following amendments and remarks.

IN THE SPECIFICATION

Please insert the following statement in the application on page 1, before line 1:

This application is a divisional of application Ser. No. 08/577,751, now U.S. Pat. No. 6,066,555, filed December 22, 1995.

Please replace the following paragraphs:

pg. 1, ln. 19-pg. 2, ln. 9

At several stages of the fabrication of semiconductor devices, it is necessary to make openings in the dielectric to allow for contact to underlying regions or layers. Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and a first metal layer is called a "contact opening", while an opening in other oxide layers such as an opening through an intermetal dielectric layer is referred to as a "via". For purposes of the claimed invention, henceforth "contact opening" or "contact region" will be used to refer to contact openings and/or via. The opening may expose a device region within the silicon substrate, such as a source or drain, or may expose some other layer or structure, for example, an underlying metallization layer, local interconnect layer, or structure such as a gate. After the opening has been formed exposing a portion of the region or layer to be contacted, the opening is generally cleaned with a sputter etch, e.g., a Radio-Frequency ("RF") sputter etch, and then the opening is filled with a conductive material deposited in the opening and in electrical contact with the underlying region or layer.

pg. 4, ln. 23-pg. 5, ln. 3

The preceding discussion focused on the making of openings, e.g., contact openings, in dielectric material on a semi-conductor substrate. The same principles are used in constructing device regions with a dielectric layer or layers. As geometries shrink, the forming of discrete devices on a semiconductor substrate becomes more specialized. Specialized deposition and etching techniques permit the density of semiconductor elements on a single chip to greatly increase, which translates into larger memory, faster operating speeds, and reduced production costs.

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pg. 6, ln. 4-8

B4

Figure 1 illustrates a self-aligned contact 130 between two gate structures. Figure 1(A) is a planar top view of the contact 130. Figure 1(B) is a planar cross-sectional view of the self-aligned contact 130 between a pair of gates taken through line 1(B) of Figure 1(A). Figure 1(C) is a planar cross-sectional view of the self-aligned contact 130 between a pair of gates taken through line 1(C) of Figure 1(A).

pg. 6, ln. 9-17

The self-aligned contact 130 is a contact to a source or drain diffusion region (n+ or p+ silicon) 140 that can overlap the edge of the diffusion region 140 without shorting out to a well beneath the diffusion region 140. This can be seen most illustratively through Figure 1(C). In Figure 1(C), the contact 130 does not lie directly in the diffusion region 140, but is misaligned and slightly overlaps the field oxide (designated by FOX in Fig. (1C). In this illustration, the self-aligned contact 130 is not directly over the diffusion region 140 but extends over (i.e., overlaps) a well portion 170. The self-aligned contact 130 does not short to the well portion 170 because the self-aligned contact 130 is separated from the well 170 by the field oxide.

pg. 6, ln.18-23

The self-aligned contact 130 is separated from a conducting polysilicon layer 110 by an encapsulating dielectric layer 120 such that the contact 130 can also overlap the polysilicon layer 110 without making electrical contact to the layer 110 or gate. The polysilicon layer 110 is separated from the source/drain diffusion region 140 by a dielectric spacer or shoulder 150 of the same or different dielectric material as the dielectric layer 120 directly above the conducting polysilicon layer 110.

pg. 6, ln. 24-pg. 7, ln. 8

A distinct dielectric etch stop layer 125 overlies the encapsulating dielectric layer 120. The etch stop layer 125 permits subsequent etching of the substrate without risk of exposing the device structures and layers because the device structuring and layers

are protected from excessive etching by the etch stop layer 125. The diffusion contact is self-aligning because the structure can be etched to the substrate over the source/drain diffusion region 140 while the dielectric spacer 150 protects the polysilicon layer 110. Even if a photoresist that protects the polysilicon layer 110 from the etchant is misaligned with respect to the polysilicon layer 110, the dielectric spacer 150 prevents shorts to the polysilicon layer 110 when the contact 130 is provided for the diffusion region 140.

B4

pg. 7, ln. 11-22

The current practice with respect to forming contact regions, particularly self-aligned contact regions, that are in electrical contact with gates, interconnect lines, or other structures in small feature size structures is to utilize etchants with high selectivity to protect underlying regions, like the etch stop layer and the first insulating layer. Figure 2 illustrates a typical prior art process of forming a self-aligned contact region adjacent to a gate. In Figure 2(A), a gate oxide layer 210 is formed on a substrate 200 with a conducting layer, for example a polysilicon layer 220, overlying the gate oxide layer 210, and an insulating layer, for example a TEOS layer 230, overlying the polysilicon layer 220. Adjacent to the polysilicon layer 220 is a contact opening region 270. The polysilicon layer 220 is separated from the contact region 270 by an insulating spacer portion, for example a TEOS spacer portion 235. A separate insulating or etch stop layer, for example a silicon nitride layer 240, overlies the TEOS layer 230 and the contact region 270. A blanket layer, for example a doped insulating layer like a BPTEOS layer 250, planarly overlies the etch stop layer 240.

B5

pg. 7, ln. 23-pg. 8, ln. 5

A layer of photoresist material 280 overlies the planarized BPTEOS layer 250 to expose the contact opening 270. In Figure 2(A), a contact opening 270 has been opened through the BPTEOS layer 250. The etchant utilized to make the opening had a high selectivity toward BPTEOS relative to silicon nitride. When the contact opening 270 was formed through the BPTEOS material, the etchant did not etch or did not effectively etch the silicon nitride layer 240 material. Hence, the description of the

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B5 silicon nitride layer 240 is described as an etch stop layer. The silicon nitride etch stop layer 240 protected the underlying TEOS layer 230 and spacer portion 235 so that the polysilicon layer 220 completely encapsulated.

pg. 8, ln. 6-13

B6 Figure 2(A) illustrates an etch 260 to remove the silicon nitride etch stop layer 240. In the etch 260 illustrated in Figure 2(A), a high selectivity etch toward silicon nitride relative to the underlying TEOS layer 230 material is practiced to efficiently etch the silicon nitride layer 240 and to protect the underlying TEOS layer 230 from the etchant. An example of a high selectivity etch recipe to effectively strip silicon nitride as compared to the TEOS layer is 30 sccm CHF_3 and 30 sccm O_2 at 60 mtorr and 100 watts of power. The result of the high selectivity etch is illustrated in Figure 2(B).

pg. 8, ln. 14-ln. 23

Figure 2(B) shows that the silicon nitride selective etch effectively removed silicon nitride layer 240 from the contact opening 270. The selective etch for silicon nitride compared to TEOS material, however, left the TEOS layer 230 with a spacer portion 235 wherein the spacer portion 235 is sloping or tapered toward the contact opening 270. This result follows even where the spacer portion 235 is originally substantially rectangular as in Figure 2(A). The properties of the highly selective etch of the overlying etch stop layer 240 will transform a substantially rectangular spacer into a sloped spacer. Figure 2(B) presents a polysilicon layer 220 encapsulated in a TEOS layer 230 with a spacer portion 235 adjacent to the contact opening 270, the spacer portion 235 having an angle 290 that is less than 85°.

pg. 8, ln. 24-pg. 9, ln. 10

In addition to providing stopping points or selectivity between materials, the use of high selectivity etches to form sloped spacer portions is the preferred practice because the sloped shape will result in good step coverage by the metal that is deposited into it. The filling of contact openings or gaps (i.e., gap fill) is an important consideration because it relates directly to the reliability of a device. If an opening is not

completely filled with an insulative material, for example, and a gap is created, a subsequent conductive material deposit can fill the gap which can lead to shorting. Sloped contact openings are easier to completely fill than boxy structures because the transition between sloped structures and openings is smooth compared to the abrupt transitions between boxy structures and openings. Because of concerns for complete gap fill and good step coverage, industry preference is for sloped spacers and planar deposition layers similar to that shown in Figure 2(B).

B6

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pg. 9, ln. 11-26

Once the contact opening is made, the opening is cleaned with a sputter etch, e.g., an RF sputter etch, before conductive material is added to fill the opening or gap. The RF sputter etch that is used to clean the contact opening in the process described above will attack and erode a portion of the insulating spacer surrounding the conducting portion and adjacent to the contact region. Figure 3 illustrates a prior art substrate with a gate and a contact region undergoing an RF sputter etch 380. In Figure 3, a gate oxide 310 is formed on a substrate 300 with a polysilicon layer 320 overlying the gate oxide 310 and an insulating layer, for example a TEOS layer 330 overlying the polysilicon layer 320. A distinct insulating layer, for example a silicon nitride etch stop layer 340, overlies the TEOS layer 330 and this etch stop layer 340 is covered by a third insulating layer, for example a BPTEOS blanket layer 350. Adjacent to the gate is a contact region 360. An etch of the silicon nitride etch stop layer 340 with a high selectivity etch for silicon nitride relative to the underlying TEOS layer material produced a gate with a sloping or tapered spacer portion 370 of TEOS material, illustrated in ghost lines. A subsequent RF sputter etch 380 is utilized to clean the contact region 360.

B7

pg. 10, ln. 1-16

Although brief and designed to clean the contact region, the RF sputter etch 380 will erode a portion of the insulating TEOS spacer portion 370. The dynamics of the sputter etch 380 are that it proceeds vertically, directing high-energy particles at the contact region. The sloping or tapered spacer portion 370 adjacent the polysilicon layer

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320 and separating the polysilicon layer 320 from the contact region 360 is struck by the high-energy particles of the RF sputter etch 380. Because the spacer portion 370 is sloping or diagonal, a significant surface area portion of the spacer portion 370 is directly exposed to the high-energy particles from the RF sputter etch 380. Further, with sloping spacers, or spacers having an angle relative to the substrate surface of less than 85° the vertical portion of the dielectric layer (i.e., that portion above the polysilicon layer 320) decreases much less than the diagonal portion of the spacer. In terms of measuring TEOS material removal during the RF sputter etch 380 in Figure 3, the difference between d_1 and d_2 is greater than the difference between v_1 and v_2. Thus, in conventional prior art self aligned contact structures, the diagonal thickness of the TEOS spacer portion 370, rather than the vertical thickness of the TEOS layer 330, determines the minimum insulating layer thickness for the gate.

B7

pg. 10, ln. 17-pg. 11, ln. 5

For gate structures having minimum diagonal insulative spacer portions of 500 Å or less, the result of the sputter etch 380 is that the sputter etch 380 laterally erodes the diagonal portion of the TEOS spacer portion 370 adjacent to the contact region to a point where the polysilicon layer 320 is no longer isolated from the contact region 360 by an insulating layer. In that case, there is a short circuit through the underlying conductive material when the contact region 360 is filled with conductive material. This result follows because the conventional RF sputter etch 380 utilized for cleaning the contact region 360 results in an approximately 200-500 Å loss of the spacer material. Further, process margins generally require that the device spacer have a final minimum thickness (after all etches, doping, and deposits) of at least 500 Å. Thus, eliminating alignment sensitivity for conventional small feature size structures, including self-aligned contact structures, requires a final (i.e., at the time of contact deposition) minimum insulating spacer of more than 500 Å and preferably on the order of 1000-1500 Å or greater to fulfill requirements for an adequate process margin, complete gap fill, and device reliability.

pg. 11, ln. 6-pg. 12, ln. 2

B7 To construct structures having a minimum insulative spacer portion of more than 500 Å directly effects the number of structures that can be placed on a device, such as a chip. The construction of structures having a minimum insulative spacer portion of more than 500 Å requires that the pre-etch-stop-etch spacer be bigger or thicker to yield an effective spacer after the etching processes. In such cases, the structures must be separated a distance such that the contact area opening is sufficient enough for an effective contact. This spacing requirement directly limits the number of structures that can be included on a device. In small feature size structures, particularly structures utilizing self-aligned contacts, the width of contact openings is approximately 0.6 microns at the top of the planarized layer and 0.2 microns at the base of the contact opening. Figure 3 indicates the difference in contact opening widths for the same contact in prior art structures. w_1 represents the width at the top of the planarized layer and w_2 represents the width at the base of the contact region 360. Further, an aspect ratio can be defined as the height of a structure (field oxide plus conductive layer plus first insulative layer plus etch stop layer, if any) relative to the width of the base of a contact opening (i.e., the distance between adjacent spacers). Typical aspect ratios for self-aligned contact structures target ratios of 1.0-2.4. This prior art range is not achievable with any device reliability. To achieve aspect ratios of 1.0-2.4 requires minimum spacer portions of less than 1000 Å and preferably on the order of 500 Å. As noted above, the minimum spacer portions required for aspect ratios of 1.0-2.4 cannot withstand the sputter etch and will result in the exposure of the underlying polysilicon gate and short circuiting with the contact.

pg. 13, ln. 2-19

B8 The invention relates to a process for minimizing lateral spacer erosion of an insulating layer on an enclosed contact region, and a device including a contact opening with a small alignment tolerance relative to a gate electrode or other structure. The process provides high quality contacts between a conductive material in the contact region and a device region, such as a source or drain, or some other layer or structure.

The process comprises the well known step of forming a conductive layer on the semiconductor body adjacent a contact region. This is followed by the forming of a first insulating layer adjacent said conductive layer and the contact region. A selected area is masked with photoresist and the first insulating layer and the conductive layer are etched to form a device structure, such as a gate, adjacent the contact region. Next, insulating lateral spacers are added to the device structure to isolate the conductive portion of the device. The insulating spacers are etched so that the device comprises an insulating layer overlying a conductive layer with a lateral spacer portion adjacent the contact region wherein the spacer portion has a substantially rectangular profile. A distinct insulating layer or etch stop layer is then formed adjacent to the first insulating layer and over the contact region. A third insulating layer or blanket layer is then optionally formed over the etch stop layer. The blanket layer may or may not be planarized.

B8

pg. 16, ln. 5-9

Figure 1 illustrates a self-aligned contact to a diffusion region. Figure 1(A) is a planar top view of the self-aligned contact. Figure 1(B) is a cross-sectional planar side view of the self-aligned contact taken through line 1(B) of Figure 1(A). Figure 1(C) is a cross-sectional planar side view of the self-aligned contact taken through line 1(C) of Figure 1(A).

B9

pg. 16, ln. 10-12

Figure 2 is a cross-sectional side view illustrating the formation of a prior art contact opening. Figure 2(A) illustrates a high selectivity etch of an etch stop insulating layer, and Figure 2(B) illustrates the results of that etch.

pg. 16, ln. 13-14

Figure 3 is a cross-sectional side view of a prior art contact opening formation during a sputter cleaning etch.

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pg. 17, ln. 9-11

Figure 4(E) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, wherein the diffusion regions are implanted with, for example, a silicide.

B10

pg. 17, ln. 12-15

Figure 4(F) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material and an insulating etch stop layer overlying the insulating material.

pg. 17, ln. 23-pg. 18, ln. 2

Figure 4(I) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the etch stop layer, and contact openings etched through the blanket layer above the diffusion regions, but separated from the diffusion regions by the etch stop layer.

B11

pg. 18, ln. 3-7

Figure 4(J) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the etch stop layer, and contact openings to the diffusion regions.

pg. 19, ln. 2-15

The invention is a device and a process whereby there is provided a contact opening with no alignment sensitivity relative to a gate electrode or other structure such that the gate electrode does not fall within the contact opening but remains isolated from the contact opening by an insulating layer. The structure contemplated by the invention is an effective device for small feature size structures, particularly self-aligned contacts,

B12

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because it is capable of maintaining high quality contacts between the conductive material in the contact region and the underlying device region, such as a source or drain, or some other layer or structure with minimum contact opening base widths (i.e., at the base of the contact openings) of 0.2 microns and minimum contact opening widths of 0.5 microns when measured from the top of a planarized layer, minimum encapsulating layer thicknesses of 400 Å, and aspect ratios (i.e., height of structure including the etch stop layer relative to the width of the base of a contact opening between the spacers) in the range of 1.0-2.4.

B12

pg. 20, ln. 5-18

Figure 4 presents a cross-sectional view of the preparation of a series of gates or transistors on a semiconductor substrate surface. Referring to Figure 4(A), the semiconductor substrate 400 can be either p- or n-type, and includes diffusion regions 405, such as sources or drains, that are heavily doped with the opposite dopant type of the substrate. An n-type first conducting layer 415 of polysilicon doped by implantation with phosphorous to a resistivity of 50-200 ohms/square is deposited over the diffusion regions 405. The polysilicon layer 415 is deposited by low pressure CVD ("LPCVD") using an LPCVD tube and SiH_4 gas at 200-400 mtorr with a thickness of 2000-3000 Å. It should be appreciated by those skilled in the art that this conducting layer 415 could instead be a p-type conducting layer or a metallic conductor of, for example, W, Mo, Ta, and/or Ti, or that this conducting layer 415 could also be a silicide, consisting of WSi_2, $MoSi_2$, $TaSi_2$, PtSi, PdSi, or that this conducting layer 415 can further be a layered structure consisting of a silicide on top of doped polysilicon.

B13

pg. 20, ln. 19-pg. 21, ln. 2

The polysilicon layer 415 overlays an insulating dielectric layer 410 such as doped or undoped silicon dioxide. The dielectric layer 410 may comprise a single oxide, or several layers formed by various methods. For example, one or more layers of oxide may be deposited by plasma enhanced chemical vapor deposition ("PECVD"), thermal CVD ("TCVD"), atmospheric pressure CVD ("APCVD"), subatmospheric pressure CVD

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("SACVD"), utilizing, for example, TEOS and oxygen, or TEOS and ozone chemistries. As used herein, reference to, for example, a PECVD TEOS oxide denotes an oxide layer deposited by PECVD utilizing TEOS chemistry. Additionally, one or more layers of dielectric layer 410 may be a spin-on-glass ("SOG") layer.

B13

pg. 21, ln. 13-23

Referring further to Figure 4(A), a photoresist masking layer 425 is deposited over the TEOS dielectric layer 420. The photoresist masking layer 425 is patterned to enable exposure of diffusion regions 405 in the semiconductor substrate. Referring to Figure 4(B), a series of photolithographic etches are performed to remove the TEOS layer 420 material and the polysilicon layer 415 from the diffusion regions 405 to form contact openings. The etches are performed using a parallel plate plasma etcher with a power of 200-300 watts. First, a fluorocarbon photolithographic etch, CHF_3/C_2F_6 at 50 mtorr, is performed to remove the insulating TEOS material from areas adjacent to and including the diffusion regions 405. This is followed by a single polysilicon photolithographic etch using a chlorine plasma (Cl_2/He) to define a polysilicon conducting layer 415 above the transistor or gate regions.

B14

pg. 22, ln. 5-20

Referring to Figures 4(C) and 4(D), spacers are formed between the polysilicon layer 415 of the gates and the contact openings by depositing an additional of conformal layer of TEOS material 430 over the structure and etching spacer portions extending into the contact openings and adjacent to the polysilicon layer 415 approximately 1500 Å in width. The spacer portions 435 of the TEOS layer 430 are demarked by ghost lines in Figure 4(D). The spacers 435 serve to insulate the polysilicon layers 415 from the conducting material that will fill the contact openings and prevent the gates from overlapping the diffusion regions 405. The spacers 435 serve to completely encapsulate the polysilicon layers 415 of the individual gates. As shown in Figure 4(C), care is taken to etch the spacers 435 such that the spacers 435 have a substantially rectangular profile. This is accomplished using a low bias and high pressure etch (2.8

B15

torr, 140 sccm He, 30 sccm CHF_3, 90 sccm CF_4, and 850 watts power), that results in low polymer formation. At this point, the preferred embodiment of the invention contemplates that the TEOS layer can have a minimum vertical width of approximately 3000 Å and spacers with a minimum width of approximately 1000 Å.

B16 [pg. 22, ln. 21-25]

Referring to Figure 4(E), the diffusion regions 405 are next implanted with a suitable dopant utilizing conventional techniques. The dopant may be implants of arsenic, phosphorous, or boron. Subsequently, silicides, for example WSi_2 and $TiSi_2$, may also be formed. Figure 4(E) illustrates silicide formation 445 in the diffusion regions 405.

[pg. 23, ln. 1-12]

Referring to Figure 4(F), overlying the TEOS layer 420 is deposited a second distinct dielectric or etch stop layer 440, in this example, a silicon nitride (Si_xN_y) layer 440, with a total thickness of 700 angstroms. It should again be appreciated by those of ordinary skill in the art that this silicon nitride layer 440 could instead be an insulating layer of, for example, silicon dioxide, SiO_2, ONO, or $SiO_xN_y(H_z)$. Additionally, the silicon nitride etch stop layer 440 may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate ("BPTEOS"). Further, the etch stop layer 440 may comprise a single silicon nitride layer or several layers formed by various methods. It is important that the etch stop layer 440 be different or distinct from the underlying insulating layer.

[pg. 23, ln. 13-18]

The invention contemplates that at this point the structure has an aspect ratio of 1.0-2.4. As used herein, an aspect ratio is defined as the ratio of the height of a contact opening measured to the top of the horizontal portion of the etch stop layer 440 to the base width of the contact opening between the insulating spacers 435. For example, an

embodiment of the invention contemplates contact opening heights of 5300 Å (0.53 μm) relative to widths of 0.32 μm to give aspect ratios of 1.6.

pg. 23, ln. 19-pg. 24, ln. 2

Referring to Figure 4(G), an optional dielectric blanket layer 450 is next deposited adjacent to the etch stop layer 440. The blanket layer 450 may or may not be planarized. In Figure 4(G), the blanket layer 450 is planarized. The planarized blanket layer 450 facilitates the formation of an interconnect layer that might later be deposited over the contact regions. The blanket layer 450 in Figure 4(G) is a doped silicate glass, for example BPTEOS. It should be appreciated by those of ordinary skill in the art that this BPTEOS layer 450 could instead be another doped insulating layer of, for example, BPSG or PSG, or an undoped insulating layer of silicon dioxide, SiO_2, ONO, or SiO_xN_y. Further, the blanket layer 450 may comprise a single oxide, like BPTEOS, or several layers formed by various methods.

3/15

pg. 24, ln. 3-8

Next, as shown in Figure 4(H), a photoresist pattern or mask layer 455 is deposited adjacent to the blanket layer 450 such that the diffusion regions 405 can be exposed. This is followed by a photolithographic etch of the BPTEOS blanket layer 450 in the contact openings. The etch is a fluorocarbon photolithographic etch (7 sccm CHF_3, 6 sccm Freon 134a) at 29 mtorr. The etch reveals a pair of contact openings 460 and 465 above the diffusion regions 405, as shown in Figure 4(I).

pg. 24, ln. 9-15

Referring to Figure 4(J), a photoresist material (not shown) is overlayed in contact opening 465 adjacent to the etch stop layer 440 to protect the etch stop material in contact opening 465 from a subsequent photolithographic etch to remove the etch stop layer 440. Next, a photolithographic etch, (900 mtorr, 100 sccm, He, 85 sccm C_2F_6, and 225 watts power using a Lam 4400 Series plasma etching system) is

performed to remove the etch stop layer 440 from contact opening 460. The etch conditions for this etch are low bombardment/high neutral flux conditions.

pg. 24, ln. 16-24

B15

Figure 4(K) is a close-up view of the cross-sectional portion of contact opening 460 in Figure 4(J). The etch proceeds anisotropically, primarily removing etch stop material lying in a horizontal plane relative to the vertical direction of the etchant ions. The etchant removes material primarily from the base of the contact opening 460, and does not remove all of the etch stop material adjacent to the spacer portion 435 of the TEOS layer 420. Thus, the remaining etch stop material adjacent to the spacer portion 435 of the TEOS layer 420 serves as additional spacer material to insulate the polysilicon layer 415 from a conductive contact that will subsequently be added to the contact opening 460.

pg. 25, ln. 1-9

B16

The etchant utilized to remove silicon nitride from the contact opening 460 has a low selectivity for etching the silicon nitride material compared to the underlying TEOS layer 420. The use of an etchant with a low selectivity for silicon nitride relative to TEOS does not significantly destroy the TEOS layer spacer portion 435. The low selectivity etch yields a TEOS layer spacer portion 435 that retains a rectangular or "boxy" profile. Figure 4(K) illustrates that only a small portion 475 (illustrated in ghost lines) of the TEOS layer spacer portion 435 is removed during the etch. Of primary significance, the spacer portion 435 of the TEOS layer 420 retains its substantially rectangular profile.

pg. 25, ln. 10-15

It is to be appreciated that the described etch stop layer etch conditions (i.e., low selectivity, low bombardment/high neutral flux) are exemplary of etch conditions that result in the retention of a boxy spacer. The invention relates to these process

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conditions as well as others that result in the retention of a boxy spacer. Thus, the etch-stop etch conditions should be regarded in an illustrative rather than restrictive sense.

pg. 25, ln. 16-pg. 26, ln. 2

The silicon nitride etch stop layer etch is followed by a sputter etch to clean the contact opening 460. In a currently preferred embodiment, the sputter etch is carried out in an atmosphere of argon, a 8 mtorr pressure, with a 1000 volt bias. In a currently preferred embodiment, the sputter etch is carried out in a commercially available system such as the Applied Materials Endura 5500 systems. Alternatively, any system having a sputter etch mode may be used to practice the invention. As will be appreciated by a person of ordinary skill in the art, the parameters can be varied considerably while still achieving the objects of the invention. In a currently preferred embodiment, the etch is designed to etch approximately 200 Å per minute as measured on thermal oxide. Because of the retention of a substantially rectangular or "boxy" spacer portion 435, the sputter etch does not significantly erode the spacer portion 435 of the TEOS layer 420.

pg. 26, ln. 8-10

Figure 4(L) presents a cross-sectional planar side view of the structure of the invention wherein conductive contacts 480 have been deposited in the contact openings 460.

pg. 26, ln. 11-24

The process described above yields a structure wherein first and second conductive layers (e.g., polysilicon layers) are separated by a contact opening with an area defined in the semiconductor substrate. An insulating layer is adjacent to and encapsulates the first and second conductive layers. The invention contemplates that the insulating layer has spacer portions between the conductive layers and the contact opening. The invention contemplates that high quality contacts can be achieved wherein the spacer portions have a minimum insulative material thickness of 400 Å. In the preferred embodiment, the spacer portions of the insulating material further have

substantially rectangular profiles. The invention also contemplates that a portion of the etch stop layer material may remain adjacent to the spacer portion of the insulating layer following an anisotropic etch of the etch stop material with a low selectivity etch for the etch stop material relative to the insulating layer material. The result is a contact opening with spacer sidewalls comprised, at least potentially, of a portion of etch stop layer material.

B17 pg. 27, ln. 1-9

The invention contemplates that effective contact openings may have base widths as small as 0.2 µm (and as small as 0.5 µm when measured from the top of the optional planarized layer), and base areas as small as 0.1 μm^2. Thus, the invention contemplates aspect ratios for effective contact openings of 1.0-2.4, wherein an aspect ratio is defined as the ratio of the height of a contact opening measured to the top of the horizontal portion of the etch stop layer 440 to the base width of the contact opening between the spacers. Figure 4(L) illustrates a height, *h*, and a width, *w*, from which an aspect ratio may be calculated for a contact region.

Please delete the text on pg. 16, ln. 15-16.

Please replace the Abstract on page 33 with the following new Abstract:

B18

A process for minimizing lateral spacer erosion of an insulating layer adjacent to a contact region and an apparatus whereby there is provided a contact opening with a small alignment tolerance relative to a gate electrode or other structure are disclosed. The process includes the steps of forming a conductive layer on a semiconductor body, then depositing an insulating layer adjacent to the conductive layer. Next, substantially rectangular insulating spacers are formed adjacent to the gate electrode. An etch stop layer is deposited adjacent the insulating layer, followed by an etch to remove the etch stop layer material from the contact region. This etch is conducted under conditions wherein the etch removes the etch stop layer, but retains the substantially rectangular lateral spacer profile of the first insulating layer. The apparatus is capable of maintaining high quality contacts between the conductive material in the contact region and an

underlying device region such as a source or drain, or some other layer or structure, and is an effective structure for small feature size structures, particularly self-aligned contact structures.

IN THE CLAIMS

Please amend the claims as follows:

25. (Twice Amended) The semiconductor apparatus of claim 27 wherein said etch stop layer comprises silicon nitride.

26. (Twice Amended) The semiconductor apparatus of claim 27 wherein said etch stop layer comprises silicon dioxide.

34. (Once Amended) A structure, comprising:

(a) a first electrically conductive material formed in and/or on a surface of a substrate;

(b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate;

(c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material;

(d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being distinct from the insulative spacer;

(e) a blanket layer over the etch stop material; and

(f) an opening through a first part of the etch stop material to the first electrically conductive material.

SUPPORT FOR AMENDMENT

The specification has been amended to correct inadvertent typographical and grammatical errors and to add appropriate reference numerals at various places in the

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specification in conformance with the parent application. Appendix A attached herewith is a marked-up version of the changes made in the replacement paragraphs. The Abstract has been amended for proper language format. A marked-up version of the Abstract is attached herewith as Appendix B. Claims 25-26 have been amended to depend from claim 27. The preamble of claim 34 has been amended to correct a typographical error. The amendment of part (d) of claim 34 is supported by claim 27. Appendix C, attached herewith, is a marked-up version of the changes made to the claims. No new matter has been added. Claims 25-39 are pending.

REMARKS

The present invention relates to a semiconductor device with well defined contact openings. At several stages of the fabrication of semiconductor devices, it is necessary to make openings in the dielectric to allow for contact to underlying regions or layers. The current practice with respect to forming contact openings, particularly self aligned contact openings, is to utilize etchants with high selectivity to protect underlying regions. However, the properties of a highly selective etch of the overlying etch stop layer will transform a substantially rectangular spacer adjacent to the contact region into a sloped spacer, such that the spacer is sloping or tapered toward the contact opening. Before the conductive material is added to the contact opening, the opening is cleaned with a sputter etch. The sputter etch will erode a portion of the sloped insulating spacer.

Therefore, in conventional self-aligned contact structures, the diagonal thickness of the spacer, rather than the vertical thickness of the insulating layer, determines the minimum insulating layer thickness for the gate. The sloping spacers limit the number of structures that can be included on a device.

The present invention avoids this problem by retaining the substantially rectangular profile of the insulating spacers. The present invention includes at least one insulating spacer in the contact region and an etch stop material over the first insulating layer and adjacent to the insulating spacer, the etch stop material being distinct from the insulating spacer.

Rejections under 35 U.S.C. § 102 and 103

The rejection of the claims under 35 U.S.C. § 102 and 103 over Dennison et al. (U.S. Pat. No. 5,338,700), either alone or in combination with Gonzalez (U.S. Pat. No. 5,234,856), is respectfully traversed. Dennison et al. describes a barrier layer rather than an etch stop material, and does not suggest that it is a distinct material from the insulating spacer.

Dennison et al. describes a method of forming a bit line over a capacitor array of memory cells. The semiconductor wafer of Dennison et al. has an array of electrically isolated word lines **12**, **14** and **16** having insulating spacers and caps **18** (Figure 1). The spacers and caps **18** preferably comprise an insulative nitride, such as Si_3N_4 (col. 3, ln. 33-34). The reference further states "a thin layer **20** of Si_3N_4 is provided atop the wafer to function as a diffusion barrier" (col. 3, ln. 34-36). Dennison et al. does not teach or suggest that the spacers and caps **18** and diffusion barrier **20** are distinct materials, but rather that **18** and **20** are the same material. Furthermore, since **20** is described as a diffusion barrier, not an etch stop, there would be no reason to use a material distinct from the spacer **18**.

Gonzalez describes a dynamic random access memory cell having a stacked-trench capacitor that is resistant to alpha particle generated soft errors. Gonzalez only describes silicon dioxide in spacers **31** (col. 5, ln. 10-12).

The claimed invention includes an etch stop material that is distinct from the insulating spacer. The barrier layer of Dennison et al. is described as Si_3N_4, the same material as the spacers. Furthermore, there is no suggestion that they be formed from distinct materials since the barrier layer is not intended to function as an etch stop layer. Gonzalez does not correct this deficiency.

Therefore, Applicants submit that Dennison et al., alone or in combination with Gonzalez, does not anticipate nor make obvious the claimed invention. Withdrawal of the rejection of the claims on these grounds is respectfully requested.

Rejections under 35 U.S.C. § 112

The rejections of claims 25-33 under 35 U.S.C. § 112 second paragraph is respectfully traversed. Applicants submit that the contact regions 460 and 465 are in the first insulating layer 420 as illustrated in Figures 4(I)-4(K). Withdrawal of this rejection is respectfully requested.

The rejection of claims 34-39 under 35 U.S.C. § 112 second paragraph has been obviated by appropriate amendment.

Claim objections

Claims 25-26 were objected to for failing to further limit the subject matter of claim 27. Applicants respectfully traverse this objection since claims 25-26 specify the material comprising the etch stop layer, which is not specified in the claim from which they depend. Withdrawal of the objection on these grounds is respectfully requested.

The objection to claims 25-26 for depending from cancelled claim 23 has been obviated by appropriate amendment.

Applicants submit that the word "insulative" in claim 34 is not misspelled as evidenced by the definition of "insulative" from the Oxford English Dictionary, attached herewith. Withdrawal of the objection to claim 34 is respectfully requested.

Objections to the drawings

The drawings were objected to for several informalities, and these objections are addressed by the corrected drawings filed herewith and appropriate amendment to the specification, except as noted below.

Applicants submit that the contact region 460 and 465 are in the first insulating layer 420, shown in Figures 4(I)-4(K). Withdrawal of this objection to the drawings is respectfully requested.

Applicants request permission to amend the figures as shown in red on copies of Figures 3 and 4(A)-4(L) attached herewith.

Therefore, withdrawal of the objections to the drawings is respectfully requested.

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Objections to the specification

The objection to the abstract has been obviated by appropriate amendment.

The specification has been amended to delete the second description of Figure 3 in the brief description of the drawings on pg. 16, ln. 15-16.

Applicants note that the detailed description of Figure 4(H) is found on pg. 24, ln. 3-6. The detailed description of Figure 4(I) is found on pg. 24, ln. 6-8. Reference to Figure 4(I) has been added. Withdrawal of the objection to the specification on these grounds is respectfully requested.

In light of the amendments and remarks, Applicants respectfully submit that the present application is in condition for allowance. Early notice of such action is earnestly solicited.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicant

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200

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APPENDIX A

pg. 1, ln. 19-pg. 2, ln. 9

At several stages of the fabrication of semiconductor devices, it is necessary to make openings in the dielectric to allow for contact to underlying regions or layers. Generally, an opening through a dielectric exposing a diffusion region or an opening through a dielectric layer between polysilicon and a [the] first metal layer is called a "contact opening", while an opening in other oxide layers such as an opening through an intermetal dielectric layer is referred to as a "via". For purposes of the claimed invention, henceforth "contact opening" or "contact region" will be used to refer to contact openings and/or via. The opening may expose a device region within the silicon substrate, such as a source or drain, or may expose some other layer or structure, for example, an underlying metallization layer, local interconnect layer, or structure such as a gate. After the opening has been formed exposing a portion of the region or layer to be contacted, the opening is generally cleaned with a sputter etch, e.g., a Radio-Frequency ("RF") sputter etch, and then the opening is filled with a conductive material deposited in the opening and in electrical contact with the underlying region or layer.

pg. 4, ln. 23-pg. 5, ln. 3

The preceding discussion focused on the making of openings, e.g., contact openings, in dielectric material on a semi-conductor substrate. The same principles are used in constructing device regions with a dielectric layer or layers. As geometries shrink, the forming of discrete [discreet] devices on a semiconductor substrate becomes more specialized. Specialized deposition and etching techniques permit the density of semiconductor elements on a single chip to greatly increase, which translates into larger memory, faster operating speeds, and reduced production costs.

pg. 6, ln. 4-8

Figure 1 illustrates a self-aligned contact 130 between two gate structures. Figure 1(A) is a planar top view of the contact 130. Figure 1(B) is a planar cross-sectional view of the [a] self-aligned contact 130 between a pair of gates taken through

line 1(B) of Figure 1(A). Figure 1(C) is a planar cross-sectional view of the [a] self-aligned contact 130 between a pair of gates taken through line 1(C) of Figure 1(A).

pg. 6, ln. 9-17

The self-aligned contact 130 is a contact to a source or drain diffusion region (n+ or p+ silicon) 140 that can overlap the edge of the diffusion region 140 without shorting out to a [the] well beneath the diffusion region 140. This can be seen most illustratively through Figure 1(C). In Figure 1(C), the contact 130 does not lie directly in the diffusion region 140, but is misaligned and slightly overlaps the field oxide (designated by FOX in Fig. (1C). In this illustration, the self-aligned contact 130 is not directly over the diffusion region 140 but extends over (i.e., overlaps) a well portion 170. The self-aligned contact 130 does not short to the well portion 170 because the self-aligned contact 130 is separated from the well 170 by the field oxide.

pg. 6, ln. 18-23

The self-aligned contact 130 is separated from a conducting polysilicon layer 110 by an encapsulating dielectric layer 120 such that the contact 130 can also overlap the polysilicon layer 110 without making electrical contact to the layer 110 or gate. The polysilicon layer 110 is separated from the source/drain diffusion region 140 by a dielectric spacer or shoulder 150 of the same or different dielectric material as the dielectric layer 120 directly above the conducting polysilicon layer 110.

pg. 6, ln. 24-pg. 7, ln.8

A distinct dielectric etch stop layer 125 overlies the encapsulating dielectric layer 120. The etch stop layer 125 permits subsequent etching of the substrate without risk of exposing the device structures and layers because the device structuring and layers are protected from excessive etching by the etch stop layer 125. The diffusion contact is self-aligning because the structure can be etched to the substrate over the source/drain diffusion region 140 while the dielectric spacer 150 protects the polysilicon layer 110. Even if a photoresist that protects the polysilicon layer 110 from the etchant is misaligned with respect to the polysilicon layer 110, the dielectric spacer 150 prevents

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shorts to the polysilicon layer 110 when the contact 130 is provided for the diffusion region 140.

pg. 7, ln. 11-22

The current practice with respect to forming contact regions, particularly self-aligned contact regions, that are in electrical contact with gates, interconnect lines, or other structures in small feature size structures is to utilize etchants with high selectivity to protect underlying regions, like the etch stop layer and the first insulating layer. Figure 2 illustrates [demonstrates] a typical prior art process of forming a self-aligned contact region adjacent to a gate. In Figure 2(A), a gate oxide layer 210 is formed on a substrate 200 with a conducting layer, for example a polysilicon layer 220, overlying the gate oxide layer 210, and an insulating layer, for example a TEOS layer 230, overlying the polysilicon layer 220. Adjacent to the polysilicon layer 220 is a contact opening region 270. The polysilicon layer 220 is separated from the contact region 270 by an insulating spacer portion, for example a TEOS spacer portion 235. A separate insulating or etch stop layer, for example a silicon nitride layer 240, overlies the TEOS layer 230 and the contact region 270 [250]. A blanket layer, for example a doped insulating layer like a BPTEOS layer 250, planarly overlies the etch stop layer 240.

pg. 7, ln. 23-pg. 8, ln. 5

A layer of photoresist material 280 overlies the planarized BPTEOS layer 250 to expose the contact opening 270. In Figure 2(A), a contact opening 270 has been opened through the BPTEOS layer 250. The etchant utilized to make the opening had a high selectivity toward BPTEOS relative to silicon nitride. When the contact opening 270 was formed through the BPTEOS material, the etchant did not etch or did not effectively etch the silicon nitride layer 240 material. Hence, the description of the silicon nitride layer 240 is described as an etch stop layer. The silicon nitride etch stop layer 240 protected the underlying TEOS layer 230 and spacer portion 235 so that the polysilicon layer 220 [remains] completely encapsulated.

pg. 8, ln. 6-13

Figure 2(A) illustrates an etch 260 to remove the silicon nitride etch stop layer 240. In the etch 260 illustrated in Figure 2(A), a high selectivity etch toward silicon nitride relative to the underlying TEOS layer 230 material is practiced to efficiently etch the silicon nitride layer 240 and to protect the underlying TEOS layer 230 from the etchant. An example of a high selectivity etch recipe to effectively strip silicon nitride as compared to the TEOS layer is 30 sccm CHF_3 and 30 sccm O_2 at 60 mtorr and 100 watts of power. The result of the high selectivity etch is illustrated in Figure 2(B).

pg. 8, ln. 14-ln. 23

Figure 2(B) shows that the silicon nitride selective etch effectively removed silicon nitride layer 240 from the contact opening 270. The selective etch for silicon nitride compared to TEOS material, however, left the TEOS layer 230 with a spacer portion 235 wherein the spacer portion 235 is sloping or tapered toward the contact opening 270. This result follows even where the spacer portion 235 is originally substantially rectangular as in Figure 2(A). The properties of the highly selective etch of the overlying etch stop layer 240 will transform a substantially rectangular spacer into a sloped spacer. Figure 2(B) presents a polysilicon layer 220 encapsulated in a TEOS layer 230 with a spacer portion 235 adjacent to the contact opening 270, the spacer portion 235 having an angle 290 that is less than 85°.

pg. 8, ln. 24-pg. 9, ln. 10

In addition to providing stopping points or selectivity between materials, the use of high selectivity etches to form sloped spacer portions is the preferred practice because the sloped shape will result in good step coverage by the metal that is deposited into it. The filling of contact openings or gaps (i.e., gap fill) is an important consideration because it relates directly to the reliability of a device. If an opening is not completely filled with an insulative material, for example, and a gap is created, a subsequent conductive material deposit can fill the gap which can lead to shorting. Sloped contact openings are easier to completely fill than boxy structures because the

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transition between sloped structures and openings is smooth compared to the abrupt transitions between boxy structures and openings. Because of concerns for complete gap fill and good step coverage, industry preference is for sloped spacers and planar deposition layers similar to that shown in Figure 2(B [b]).

pg. 9, ln. 11-26

Once the contact opening is made, the opening is cleaned with a sputter etch, e.g., an RF sputter etch, before conductive material is added to fill the opening or gap. The RF sputter etch that is used to clean the contact opening in the process described above will attack and erode a portion of the insulating spacer surrounding the conducting portion and adjacent to the contact region. Figure 3 illustrates [presents] a prior art substrate with a gate and a contact region undergoing an RF sputter etch 380. In Figure 3, a gate oxide 310 is formed on a substrate 300 with a polysilicon layer 320 overlying the gate oxide 310 and an insulating layer, for example a TEOS layer 330 overlying the polysilicon layer 320. A distinct insulating layer, for example a silicon nitride etch stop layer 340, overlies the TEOS layer 330 and this etch stop layer 340 is covered by a third insulating layer, for example a BPTEOS blanket layer 350. Adjacent to the gate is a contact region 360. An etch of the silicon nitride etch stop layer 340 with a high selectivity etch for silicon nitride relative to the underlying TEOS layer material produced a gate with a sloping or tapered spacer portion 370 of TEOS material, illustrated in ghost lines. A subsequent RF sputter etch 380 is utilized to clean the contact region 360.

pg. 10, ln. 1-16

Although brief and designed to clean the contact region, the RF sputter etch 380 will erode a portion of the insulating TEOS spacer portion 370. The dynamics of the sputter etch 380 are that it proceeds vertically, directing high-energy particles at the contact region. The sloping or tapered spacer portion 370 adjacent the polysilicon layer 320 and separating the polysilicon layer 320 from the contact [diffusion] region 360 is struck by the high-energy particles of the RF sputter etch 380. Because the spacer portion 370 is sloping or diagonal, a significant surface area portion of the spacer

portion 370 is directly exposed to the high-energy particles from the RF sputter etch 380. Further, with sloping spacers, or spacers having an angle relative to the substrate surface of less than 85° the vertical portion of the dielectric layer [(](i.e., that portion above the polysilicon layer 320 [gate]) decreases much less than the diagonal portion of the spacer. In terms of measuring TEOS material removal during the RF sputter etch 380 in Figure 3, the difference between d_1 and d_2 is greater than the difference between v_1 and v_2. Thus, in conventional prior art self aligned contact structures, the diagonal thickness of the TEOS spacer portion 370, rather than the vertical thickness of the TEOS layer 330, determines the minimum insulating layer thickness for the gate.

pg. 10, ln. 17-pg. 11, ln. 5

For gate structures having minimum diagonal insulative spacer portions of 500 Å or less, the result of the sputter etch 380 is that the sputter etch 380 laterally erodes the diagonal portion of the TEOS spacer portion [layer] 370 adjacent to the contact region to a point where the polysilicon layer 320 is no longer isolated from the contact region 360 by an insulating layer. In that case, there is a short circuit through the underlying conductive material when the contact region 360 [opening] is filled with conductive material. This result follows because the conventional RF sputter etch 380 utilized for cleaning the contact region 360 results in an approximately 200-500 Å loss of the spacer material. Further, process margins generally require that the device spacer have a final minimum thickness (after all etches, doping, and deposits) of at least 500 Å. Thus, eliminating [to eliminate] alignment sensitivity for conventional small feature size structures, including self-aligned contact structures, requires a final (i.e., at the time of contact deposition) minimum insulating spacer of more than 500 Å and preferably on the order of 1000-1500 Å or greater to fulfill requirements for an adequate process margin, complete gap fill, and device reliability.

pg. 11, ln. 6-pg. 12, ln. 2

To construct structures having a minimum insulative spacer portion of more than 500 Å directly effects the number of structures that can be placed on a device, such as a chip. The construction of structures having a minimum insulative spacer portion of

more than 500 Å requires that the pre-etch-stop-etch spacer be bigger or thicker to yield an effective spacer after the etching processes. In such cases, the structures must be separated a distance such that the contact area opening is sufficient enough for an effective contact. This spacing requirement directly limits the number of structures that can be included on a device. In small feature size structures, particularly structures utilizing self-aligned contacts, the width of contact openings is approximately 0.6 microns at the top of the planarized layer and 0.2 microns at the base of the contact opening. Figure 3 indicates the difference in contact opening widths for the same contact in prior art structures. w_1 represents the width at the top of the planarized layer and w_2 represents the width at the base of the contact region 360 [opening]. Further, an aspect ratio can be defined as the height of a structure (field oxide plus conductive layer plus first insulative layer plus etch stop layer, if any) relative to the width of the base of a contact opening (i.e., the distance between adjacent spacers). Typical aspect ratios for self-aligned contact structures target ratios of 1.0-2.4. This prior art range is not achievable with any device reliability. To achieve aspect ratios of 1.0-2.4 requires minimum spacer portions of less than 1000 Å and preferably on the order of 500 Å. As noted above, the minimum spacer portions required for aspect ratios of 1.0-2.4 cannot withstand the sputter etch and will result in the exposure of the underlying polysilicon gate and short circuiting with the contact.

pg. 13, ln. 2-19

The invention relates to a process for minimizing lateral spacer erosion of an insulating layer on an enclosed contact region, [is disclosed] and a device including a contact opening with a small alignment tolerance relative to a gate electrode or other structure. The process provides high quality contacts between a conductive material in the contact region and a device region, such as a source or drain, or some other layer or structure. The process comprises the well known step of forming a conductive layer on the semiconductor body adjacent a contact region. This is followed by the forming of a first insulating layer adjacent said conductive layer and the contact region. A selected area is masked with photoresist and the first insulating layer and the conductive layer are etched to form a device structure, such as a gate, adjacent the contact region.

Next, insulating lateral spacers are added to the device structure to isolate the conductive portion of the device. The insulating spacers are etched so that the device comprises an insulating layer overlying a conductive layer with a lateral spacer portion adjacent the contact region wherein the spacer portion has a substantially rectangular profile. A distinct insulating layer or etch stop layer is then formed adjacent to the first insulating layer and over the contact region. A third insulating layer or blanket layer is then optionally formed over the etch stop layer. The blanket layer may or may not be planarized.

pg. 16, ln. 5-9

Figure 1 illustrates [is a planar view of] a self-aligned contact to a diffusion region. Figure 1(A) is a planar top view of the [a] self-aligned contact. Figure 1(B) is a cross-sectional planar side view of the [a] self-aligned contact taken [to diffusion] through line 1(B) of Figure 1(A). Figure 1(C) is a cross-sectional planar side view of the [a] self-aligned contact taken [to diffusion] through line 1(C) of Figure 1(A).

pg. 16, ln. 10-12

Figure 2 is a cross-sectional side view illustrating [of] the formation of a prior art contact opening [formation]. Figure 2(A) illustrates a high selectivity etch of an etch stop insulating layer, and Figure 2(B) illustrates the results of that etch.

pg. 16, ln. 13-14

Figure 3 is a cross-sectional side view [of the formation] of a prior art contact opening formation during a sputter cleaning etch.

pg. 17, ln. 9-11

Figure 4(E) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, wherein the diffusion regions are implanted with, for example, a silicide [and an insulating etch stop layer overlying the insulating material].

pg. 17, ln. 12-15

Figure 4(F) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material and an insulating etch stop layer overlying the insulating material[, wherein the diffusion region is implanted to include a silicide].

pg. 17, ln. 23-pg. 18, ln. 2

Figure 4(I) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the etch stop layer, and contact openings etched through the blanket layer above the diffusion regions, but separated from the diffusion regions by the etch stop layer.

pg. 18, ln. 3-7

Figure 4(J) illustrates a cross-sectional planar side view of a series of gates encapsulated with insulating material, an etch stop layer overlying the insulating material, a distinct planarized insulating blanket layer overlying the etch stop layer, and [a] contact openings to the [a] diffusion regions [and a second contact opening through the blanket layer but separated from the diffusion region by an etch stop layer].

pg. 19, ln. 2-15

The invention is a device and a process whereby there is provided a contact opening with [a] no alignment sensitivity relative to a gate electrode or other structure such that the gate electrode does not fall within the contact opening but remains isolated from the contact opening by an insulating layer. The structure contemplated by the invention is an effective device for small feature size structures, particularly self-aligned contacts, because it is capable of maintaining high quality contacts between the conductive material in the contact region and the underlying device region, such as a source or drain, or some other layer or structure with minimum contact opening base widths (i.e., at the base of the contact openings) of 0.2 microns and minimum contact

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opening widths of 0.5 microns when measured from the top of a planarized layer, minimum encapsulating layer thicknesses of 400 Å, and aspect ratios (i.e., height of structure including the etch stop layer relative to the width of the base of a contact opening between the spacers) in the range of 1.0-2.4.

pg. 20, ln. 5-18

Figure 4 presents a cross-sectional view of the preparation of a series of gates or transistors on a semiconductor substrate surface. Referring to Figure 4(A), the semiconductor substrate 400 can be either p- or n-type, and includes diffusion regions 405, such as sources or drains, that are heavily doped with the opposite dopant type of the substrate. An n-type first conducting layer 415 of polysilicon doped by implantation with phosphorous to a resistivity of 50-200 ohms/square is deposited over the diffusion regions 405. The polysilicon layer 415 is deposited by low pressure CVD ("LPCVD") using an LPCVD tube and SiH_4 gas at 200-400 mtorr with a thickness of 2000-3000 Å. It should be appreciated by those skilled in the art that this conducting layer 415 could instead be a p-type conducting layer or a metallic conductor of, for example, W, Mo, Ta, and/or Ti, or that this conducting layer 415 [320] could also be a silicide, consisting of WSi_2, $MoSi_2$, $TaSi_2$, PtSi, PdSi, or that this conducting layer 415 [320] can further be a layered structure consisting of a silicide on top of doped polysilicon.

pg. 20, ln. 19-pg. 21, ln. 2

The polysilicon layer 415 overlays an insulating dielectric layer 410 such as doped or undoped silicon dioxide. The dielectric layer 410 may comprise a single oxide, or several layers formed by various methods. For example, one or more layers of oxide may be deposited by plasma enhanced chemical vapor deposition ("PECVD"), thermal CVD ("TCVD"), atmospheric pressure CVD ("APCVD"), subatmospheric pressure CVD ("SACVD"), [for example] utilizing, for example, TEOS and oxygen, or TEOS and ozone chemistries. As used herein, reference to, for example, a PECVD TEOS oxide denotes an oxide layer deposited by PECVD utilizing TEOS chemistry. Additionally, one or more layers of dielectric layer 410 may be a spin-on-glass ("SOG") layer.

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pg. 21, ln. 13-23

Referring further to Figure 4(A), a photoresist masking layer 425 is deposited over the TEOS dielectric layer 420. The photoresist masking layer 425 is patterned to enable exposure of [exposes] diffusion regions 405 in the semiconductor substrate. Referring to Figure 4(B), a series of photolithographic etches are performed to remove the TEOS layer 420 material and the polysilicon layer 415 from the diffusion regions 405 to form [or] contact openings [regions]. The etches are performed using a parallel plate plasma etcher with a power of 200-300 watts. First, a fluorocarbon photolithographic etch, CHF_3/C_2F_6 at 50 mtorr, is performed to remove the insulating TEOS material from areas adjacent to and including the diffusion [or contact] regions 405. This is followed by a single polysilicon photolithographic etch using a chlorine plasma (Cl_2/He) to define a polysilicon conducting layer 415 above the transistor or gate regions.

pg. 22, ln. 5-20

Referring to Figures 4(C) and 4(D), spacers are formed between the polysilicon layer 415 of the gates and the contact openings [regions] by depositing an additional of conformal layer of TEOS material 430 over the structure and etching spacer portions extending into the contact openings and adjacent to the polysilicon layer 415 approximately 1500 Å in width. The spacer portions 435 of the TEOS layer 430 are demarked by ghost lines in Figure 4(D). The spacers 435 serve to insulate the polysilicon layers 415 from the conducting material that will fill the contact openings and prevent the gates from overlapping the diffusion regions 405. The spacers 435 serve to completely encapsulate the polysilicon layers 415 of the individual gates. As shown in Figure 4(C), care is taken to etch the spacers 435 such that the spacers 435 have a substantially rectangular profile. This is accomplished using a low bias and high pressure etch (2.8 torr, 140 sccm He, 30 sccm CHF_3, 90 sccm CF_4, and 850 watts power), that results in low polymer formation. At this point, the preferred embodiment of the invention contemplates that the TEOS layer can have a minimum vertical width of approximately 3000 Å and spacers with a minimum width of approximately 1000 Å.

pg. 22, ln. 21-25

Referring to Figure 4(E), the diffusion regions 405 are next implanted with a suitable dopant utilizing conventional techniques. The dopant may be implants of arsenic, phosphorous, or boron. Subsequently, silicides, for example WSi_2 and $TiSi_2$, may also be formed. Figure 4(E) illustrates silicide formation 445 in the diffusion regions 405.

pg. 23, ln. 1-12

Referring to Figure 4(F), overlying the TEOS layer 420 is deposited a second distinct dielectric or etch stop layer 440, in this example, a[n] silicon nitride (Si_xN_y) layer 440, with a total thickness of 700 angstroms. It should again be appreciated by those of ordinary skill in the art that this silicon nitride layer 440 could instead be an insulating layer of, for example, silicon dioxide, SiO_2, ONO, or $SiO_xN_y(H_z)$. Additionally, the silicon nitride etch stop layer 440 [340] may be undoped or may be doped, for example with boron, phosphorous, or both, to form, for example, borophosphosilicate glass ("BPSG"), phosphosilicated glass ("PSG"), and borophosphosilicate tetraethyl orthosilicate ("BPTEOS"). Further, the etch stop layer 440 may comprise a single silicon nitride layer or several layers formed by various methods. It is important that the etch stop layer 440 be different or distinct from the underlying insulating layer.

pg. 23, ln. 13-18

The invention contemplates that at this point the structure has an aspect ratio of 1.0-2.4. As used herein, an aspect ratio is defined as the ratio of the height of a contact opening measured to the top of the horizontal portion of the etch stop layer 440 to the base width of the contact opening between the insulating spacers 435. For example, an embodiment of the invention contemplates contact opening heights of 5300 Å (0.53 μm) relative to widths of 0.32 μm to give aspect ratios of 1.6.

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pg. 23, ln. 19-pg. 24, ln. 2

Referring to Figure 4(G), an optional dielectric blanket layer 450 is next deposited adjacent to the etch stop layer 440. The blanket layer 450 may or may not be planarized. In Figure 4(G), the blanket layer 450 is planarized. The planarized blanket layer 450 facilitates the formation of an interconnect layer that might later be deposited over the contact regions. The blanket layer 450 in Figure 4(G) is a doped silicate glass, for example BPTEOS. It should be appreciated by those of ordinary skill in the art that this BPTEOS layer 450 could instead be another doped insulating layer of, for example, BPSG or PSG, or an undoped insulating layer of silicon dioxide, SiO_2, ONO, or SiO_xN_y. Further, the blanket layer 450 may comprise a single oxide, like BPTEOS, or several layers formed by various methods.

pg. 24, ln. 3-8

Next, as shown in Figure 4(H), a photoresist pattern or mask layer 455 is deposited adjacent to the blanket layer 450 such that [the contact regions overlying] the diffusion regions 405 can be [are] exposed. This is followed by a photolithographic etch of the BPTEOS blanket layer 450 in the contact openings [regions]. The etch is a fluorocarbon photolithographic etch (7 sccm CHF_3, 6 sccm Freon 134a) at 29 mtorr. The etch reveals a pair of contact openings [regions] 460 and 465 above the diffusion regions 405, as shown in Figure 4(I).

pg. 24, ln. 9-15

Referring to Figure 4(J), a photoresist material (not shown) [470] is overlayed in contact opening 465 adjacent to the etch stop layer 440 to protect the etch stop material in contact opening 465 from a subsequent photolithographic etch to remove the etch stop layer 440. Next, a photolithographic etch, (900 mtorr, 100 sccm, He, 85 sccm C_2F_6, and 225 watts power using a Lam 4400 Series plasma etching system) is performed to remove the etch stop layer 440 from contact opening 460. The etch conditions for this etch are low bombardment/high neutral flux conditions.

pg. 24, ln. 16-24

Figure 4(K) is a close-up view of the cross-sectional portion of contact opening 460 in Figure 4(J). The etch proceeds anisotropically, primarily removing etch stop material lying in a horizontal plane relative to the vertical direction of the etchant ions. The etchant removes material primarily from the base of the contact opening [region] 460, and does not remove all of the etch stop material adjacent to the spacer portion 435 of the TEOS layer 420. Thus, the remaining etch stop material adjacent to the spacer portion 435 of the TEOS layer 420 serves as additional spacer material to insulate the polysilicon layer 415 from a conductive contact that will subsequently be added to the contact opening [region] 460.

pg. 25, ln. 1-9

The etchant utilized to remove silicon nitride from the contact opening [region] 460 has a low selectivity for etching the silicon nitride material compared to the underlying TEOS layer 420. The use of an etchant with a low selectivity for silicon nitride relative to TEOS does not significantly destroy the TEOS layer [420] spacer portion 435. The low selectivity etch yields a TEOS layer [420] spacer portion 435 that retains a rectangular or "boxy" profile. Figure 4(K) illustrates that only a small portion 475 (illustrated in ghost lines) of the TEOS layer [420] spacer portion 435 is removed during the etch. Of primary significance, the spacer portion 435 of the TEOS layer 420 retains its substantially rectangular profile.

pg. 25, ln. 10-15

It is to be appreciated that the described etch stop layer etch conditions (i.e., low selectivity, low bombardment/high neutral flux [flax]) are exemplary of etch conditions that result in the retention of a boxy spacer. The invention relates to these process conditions as well as others that result in the retention of a boxy spacer. Thus, the etch-stop etch conditions should be regarded in an illustrative rather than restrictive sense.

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pg. 25, ln. 16-pg. 26, ln. 2

The silicon nitride etch stop layer [440] etch is followed by a sputter etch to clean the contact opening 460. In a currently preferred embodiment, the sputter etch is carried out in an atmosphere of argon, a 8 mtorr pressure, with a 1000 volt bias. In a currently preferred embodiment, the sputter etch is carried out in a commercially available system such as the Applied Materials Endura 5500 systems. Alternatively, any system having a sputter etch mode may be used to practice the invention. As will be appreciated by a person of ordinary skill in the art, the parameters can be varied considerably while still achieving the objects of the invention. In a currently preferred embodiment, the etch is designed to etch approximately 200 Å per minute as measured on thermal oxide. Because of the retention of a substantially rectangular or "boxy" spacer portion 435, the sputter etch does not significantly erode the spacer portion 435 of the TEOS layer 420.

pg. 26, ln. 8-10

Figure 4(L) presents a cross-sectional planar side view of the structure of the invention wherein [a] conductive contacts 480 have been deposited in the contact openings 460.

pg. 26, ln. 11-24

The process described above yields a structure wherein first and second conductive layers (e.g., polysilicon layers) are separated by a contact opening [region] with an area defined in the semiconductor substrate. An insulating layer is adjacent to and encapsulates the first and second conductive layers. The invention contemplates that the insulating layer has spacer portions between the conductive layers and the contact opening [region]. The invention contemplates that high quality contacts can be achieved wherein the spacer portions have a minimum insulative material thickness of 400 Å. In the preferred embodiment, the spacer portions of the insulating material further have substantially rectangular profiles. The invention also contemplates that a

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portion of the etch stop layer material may remain adjacent to the spacer portion of the insulating layer following an anisotropic etch of the etch stop material with a low selectivity etch for the etch stop material relative to the insulating layer material. The result is a contact opening with spacer sidewalls comprised, at least potentially, of a portion of etch stop layer material.

pg. 27, ln. 1-9

The invention contemplates that effective contact openings may have base widths as small as 0.2 μm (and as small as 0.5 μm when measured from the top of the optional planarized layer), and base areas as small as 0.1 μm^2. Thus, the invention contemplates aspect ratios for effective contact openings of 1.0-2.4, wherein an aspect ratio is defined as the ratio of the height of a contact opening measured to the top of the horizontal portion of the etch stop layer 440 to the base width of the contact opening between the spacers. Figure 4(L) illustrates a height, *h*, and a width, *w*, from which an aspect ratio may be calculated for a contact region[, and a height h_1, and a width, w_1, from which an aspect ratio may be calculated for a contact region].

APPENDIX B

ABSTRACT

A process for minimizing lateral spacer erosion of an insulating layer adjacent to a contact region and an apparatus whereby there is provided a contact opening with a small alignment tolerance relative to a gate electrode or other structure are disclosed. The process includes the steps of forming a conductive layer on a [said] semiconductor body, then depositing an insulating layer adjacent to the conductive layer. Next, substantially rectangular insulating spacers are formed adjacent to the gate electrode. An etch stop layer is deposited adjacent the [said] insulating layer, followed by an etch to remove the etch stop layer material from the contact region. This etch is conducted under conditions wherein the etch removes the etch stop layer, but retains the substantially rectangular lateral spacer profile of the first insulating layer. The apparatus is capable of maintaining high quality contacts between the conductive material in the contact region and an [the] underlying device region such as a source or drain, or some other layer or structure, and is an effective structure for small feature size structures, particularly self-aligned contact structures.

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APPENDIX C

25. (Once Amended) The semiconductor apparatus of claim 27 [23] wherein said etch stop layer comprises silicon nitride.

26. (Once Amended) The semiconductor apparatus of claim 27 [23] wherein said etch stop layer comprises silicon dioxide.

34. (Amended) A structure, comprising [the steps of]:

(a) a first electrically conductive material formed in and/or on a surface of a substrate;

(b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate;

(c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material;

(d) an etch stop [layer] material over the electrically insulative spacer and the first and second electrically conductive [regions] materials, the etch stop material being distinct from the insulative spacer;

(e) a blanket layer over the etch stop [layer] material; and

(f) an opening through a first part of the etch stop [layer] material to the first electrically conductive [region] material.

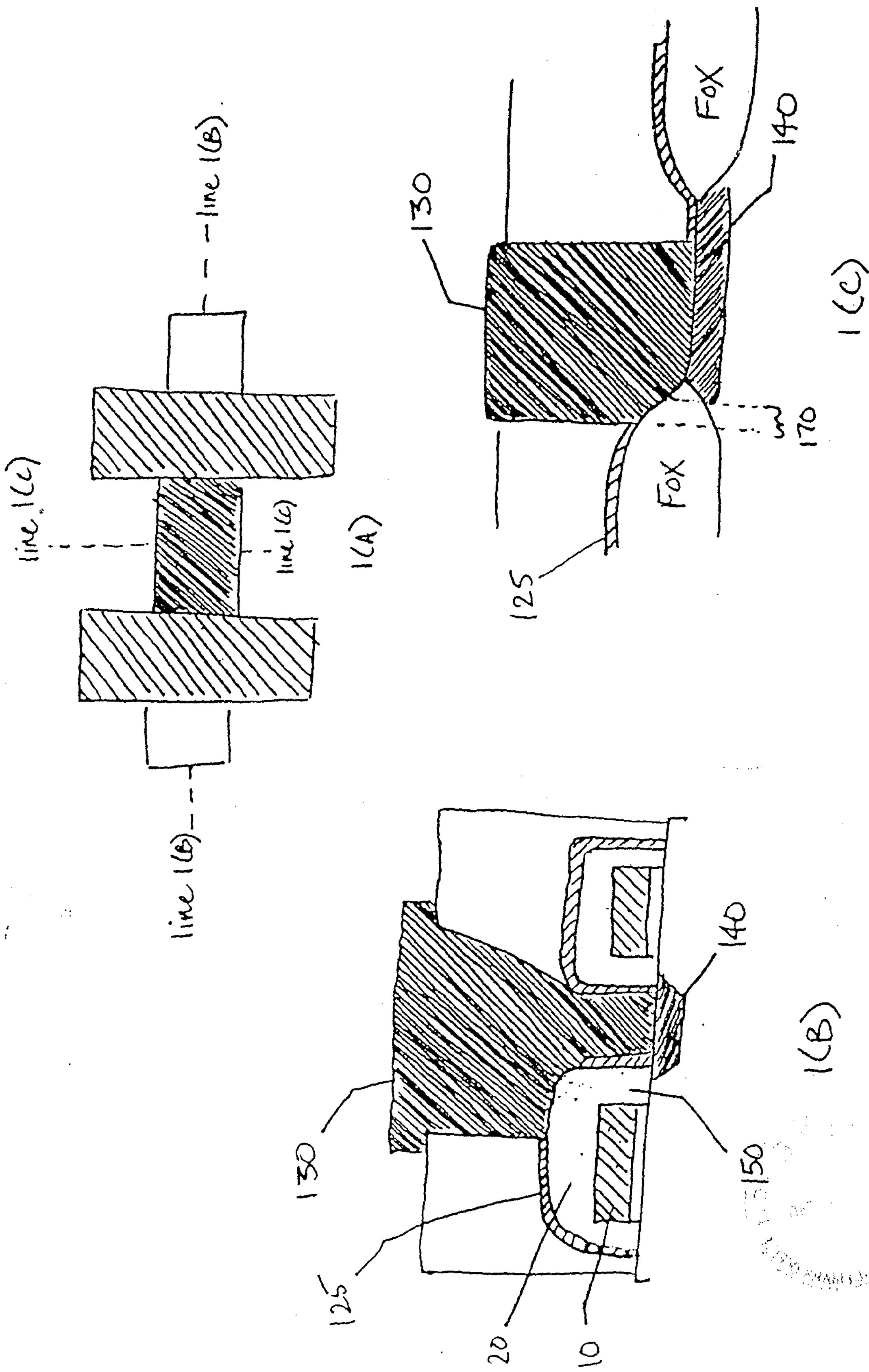


Figure 1
(Prior Art)

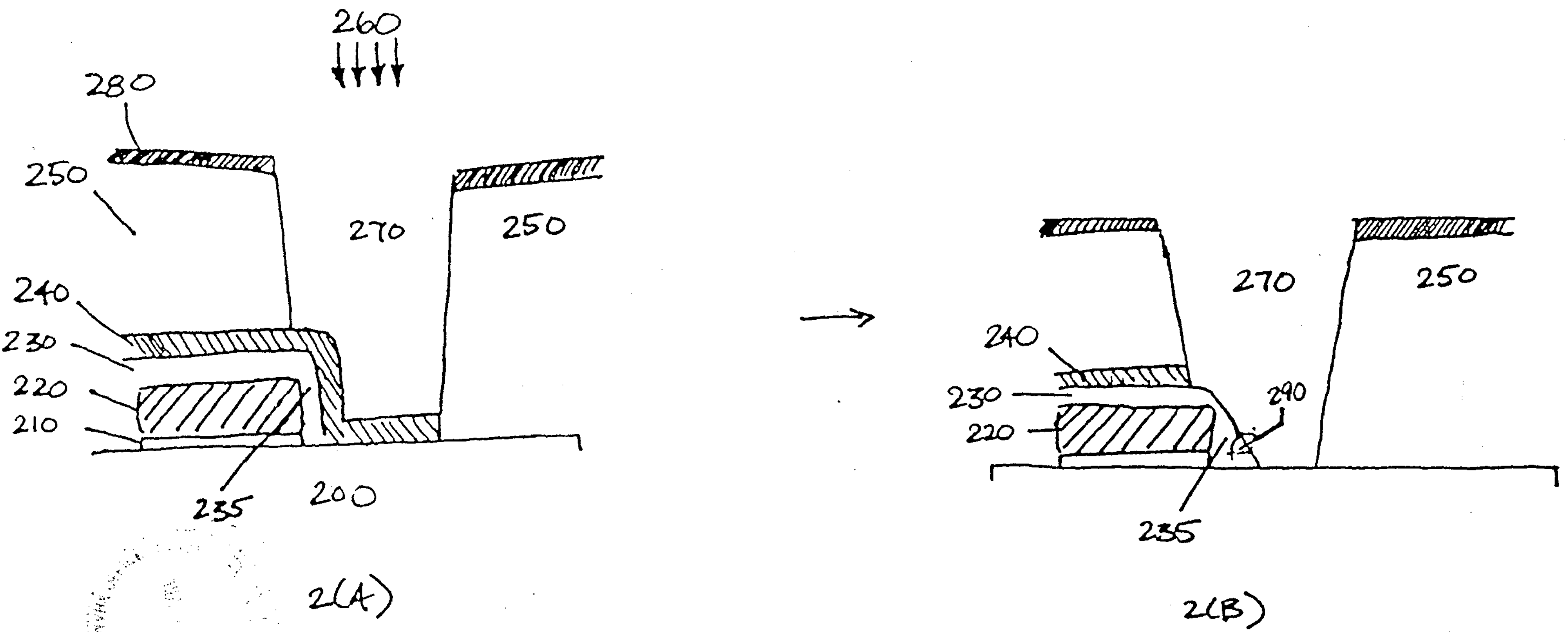


FIGURE 2
(Prior Art)

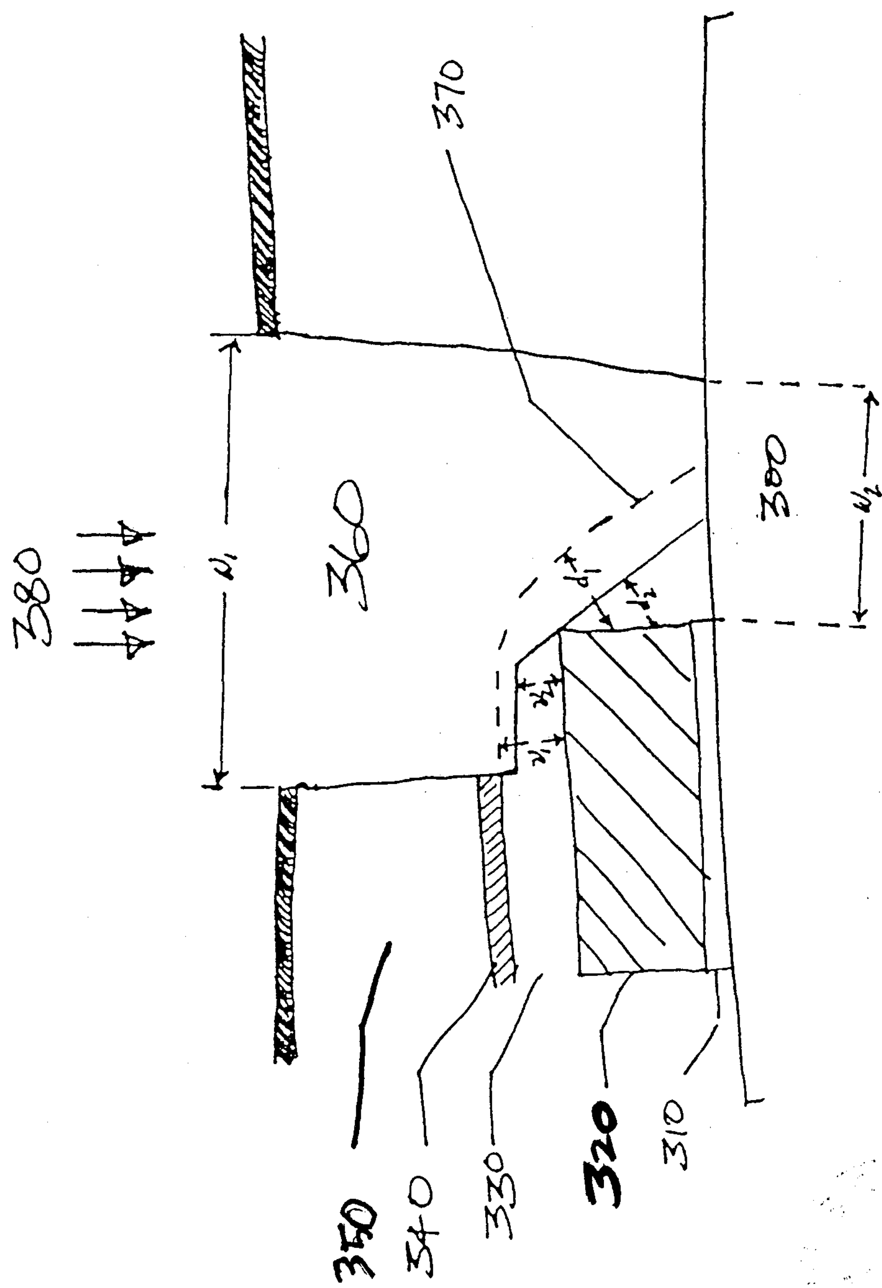
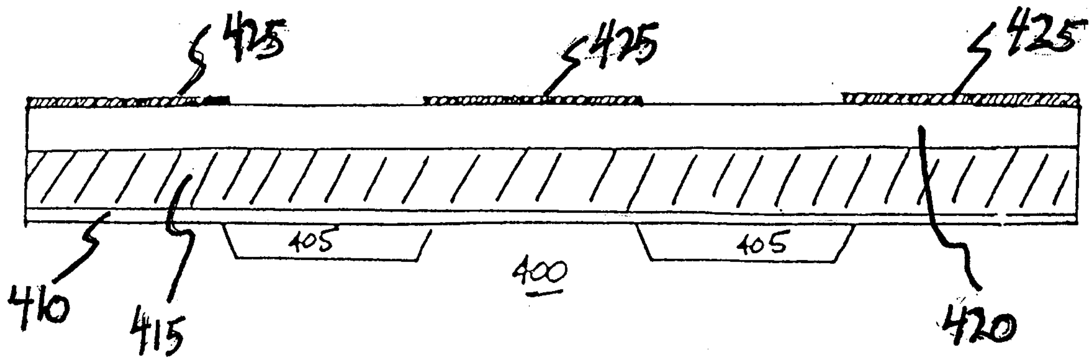


FIGURE 3
(Prior Art)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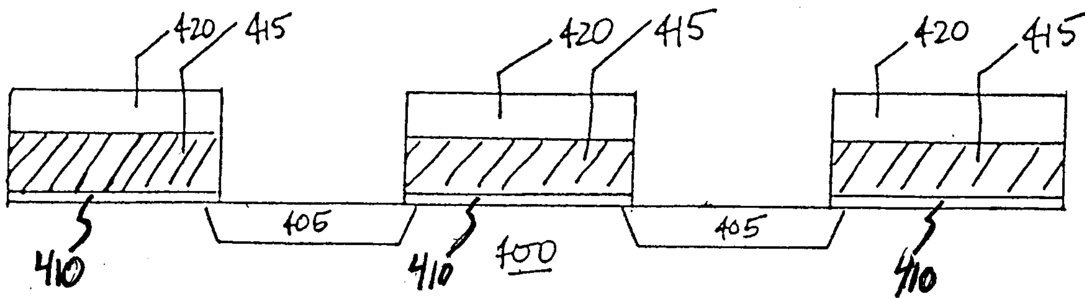
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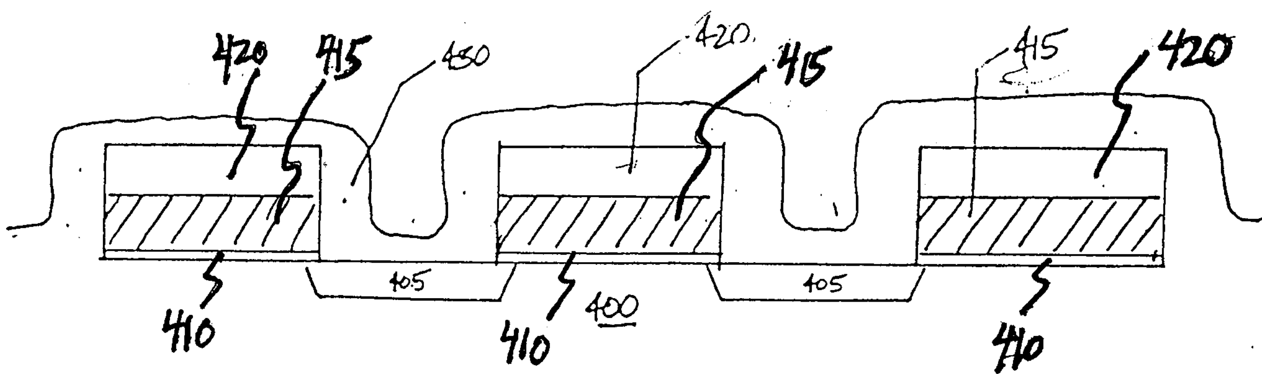
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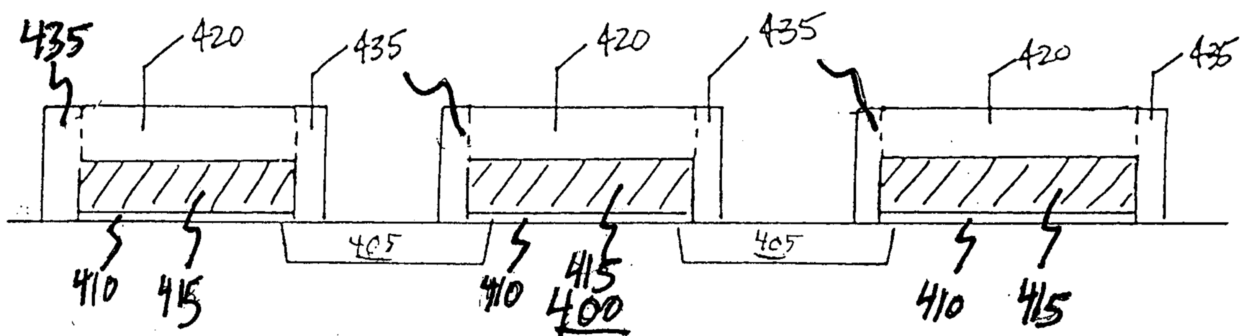
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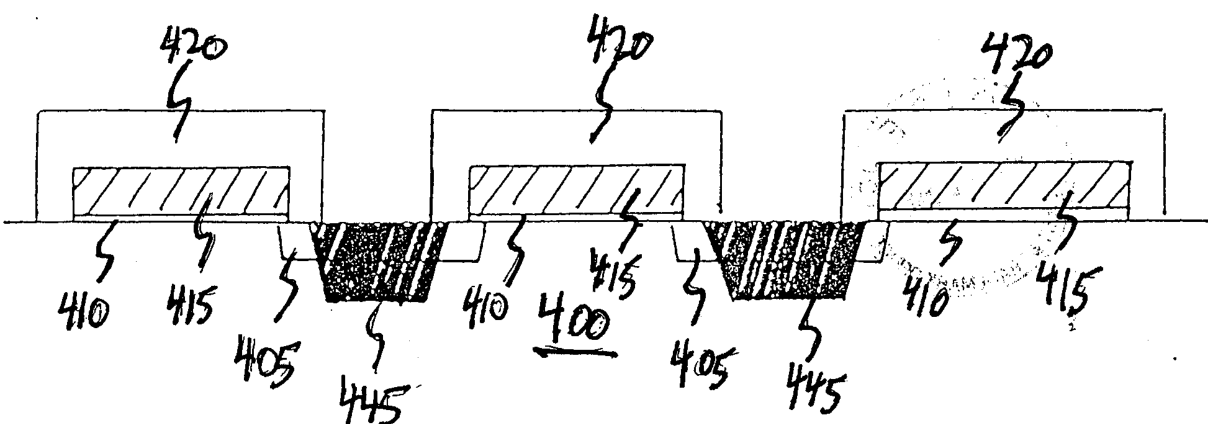
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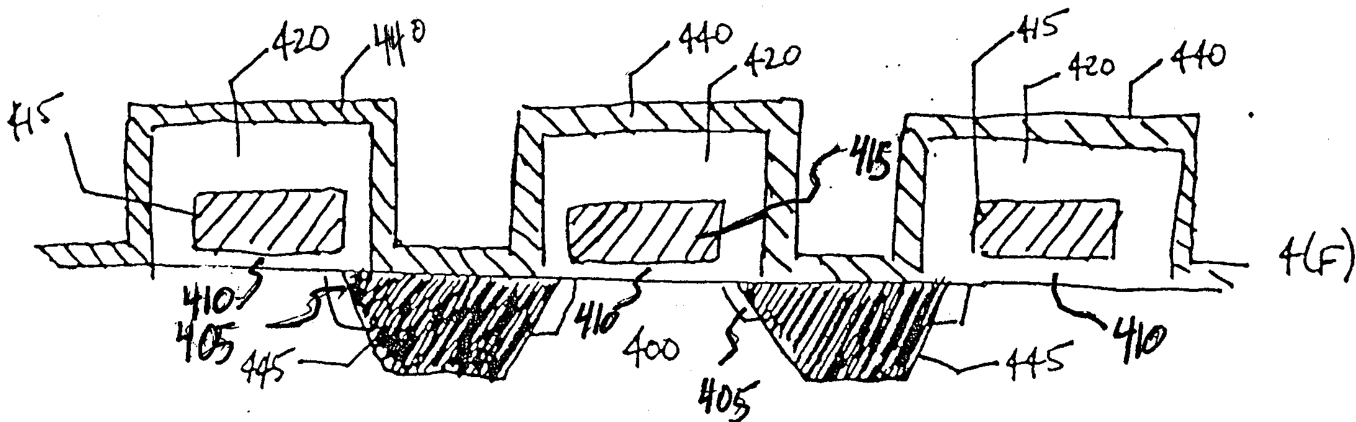
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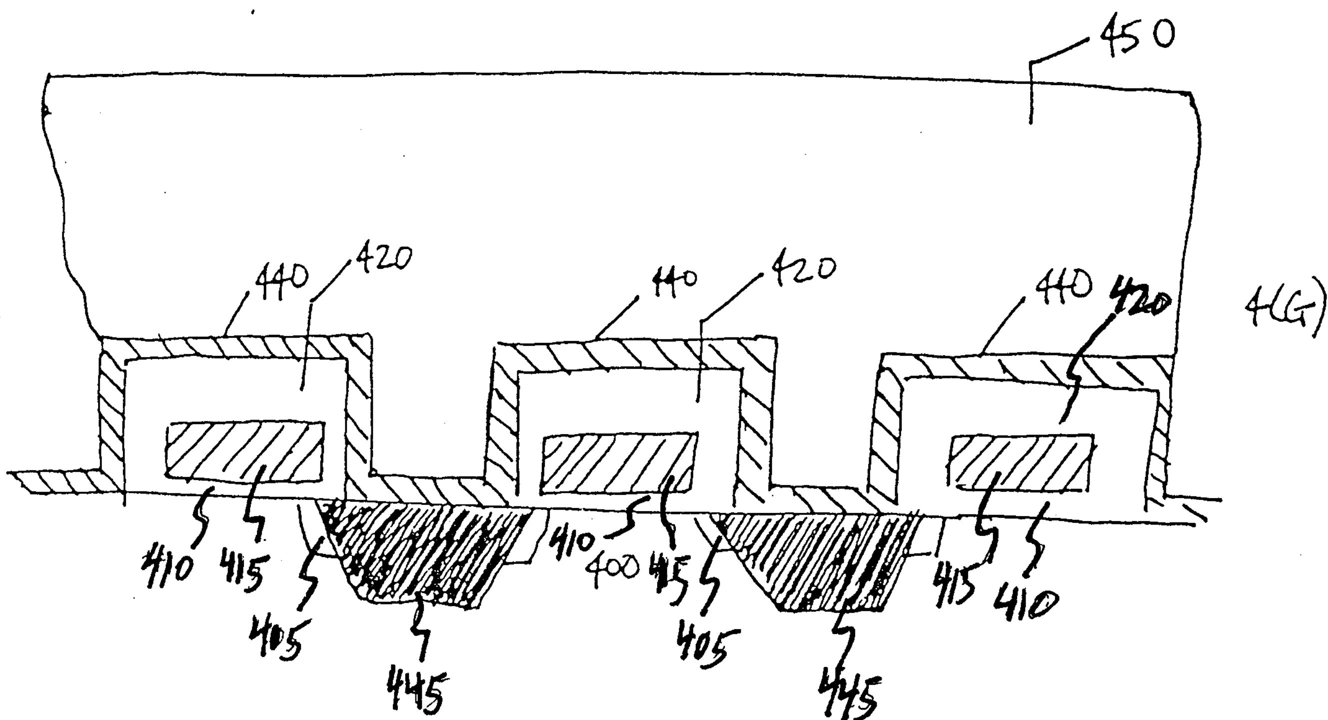
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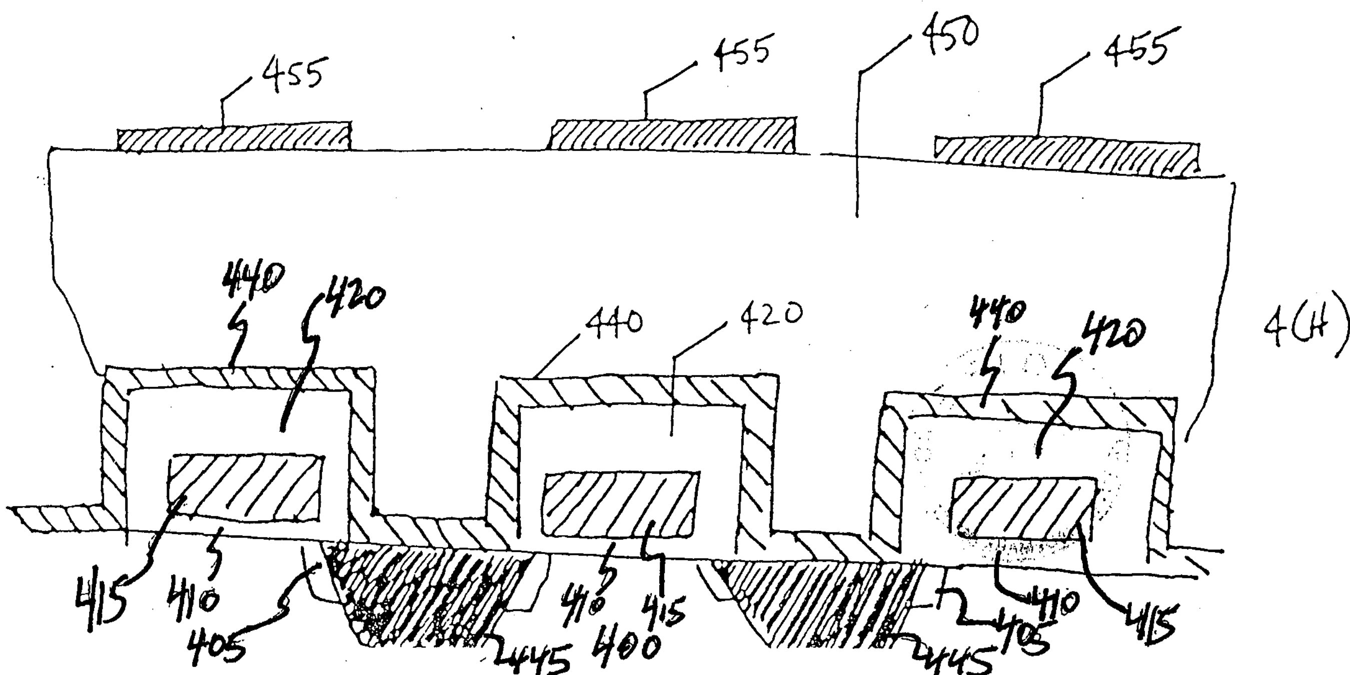
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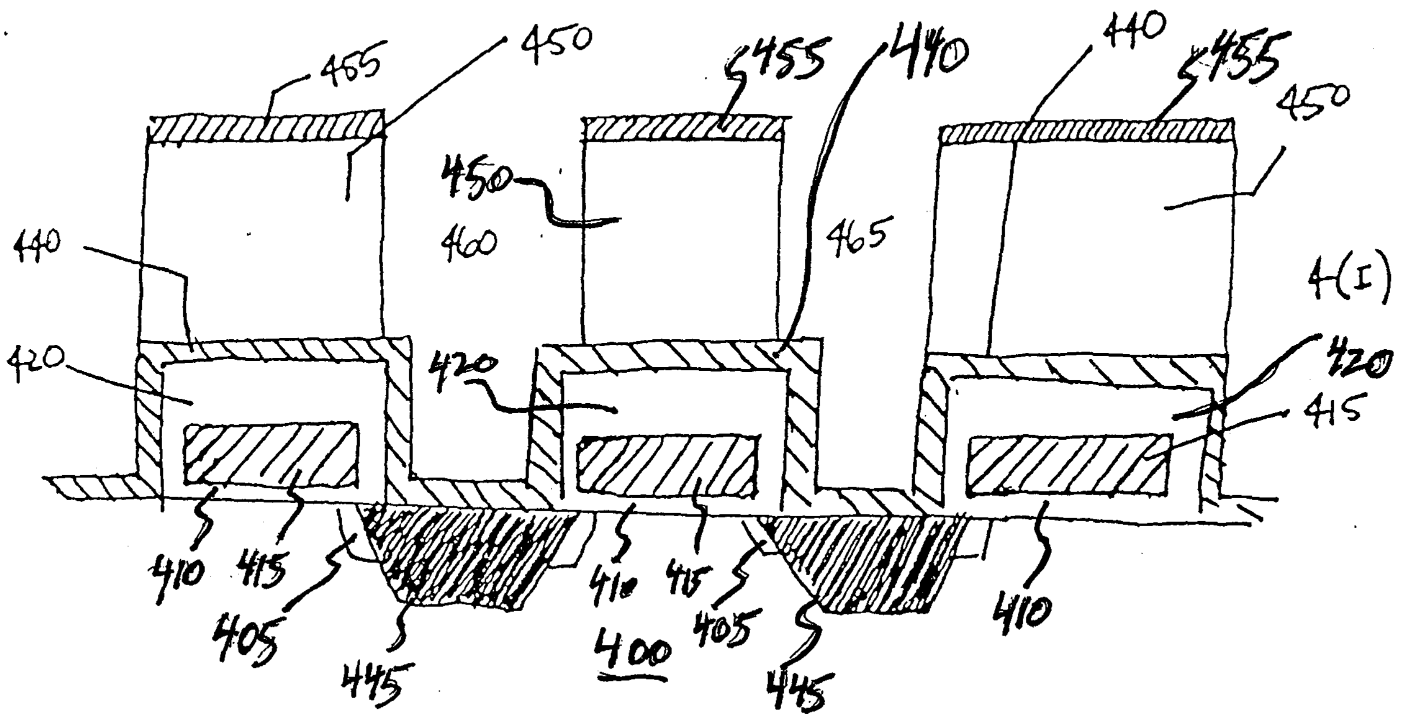
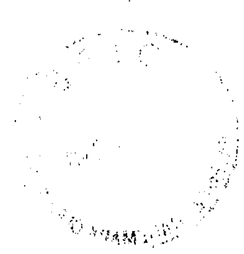
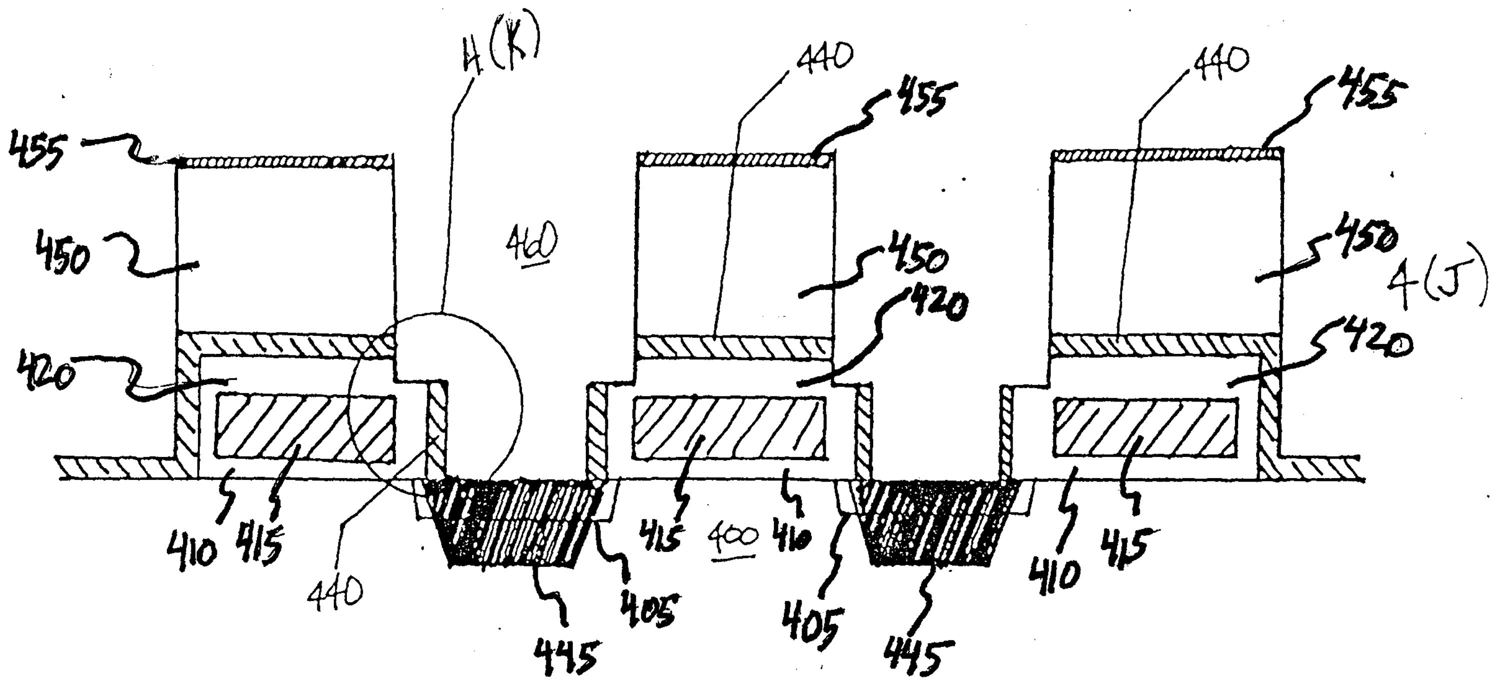


FIGURE 4 (cont.)

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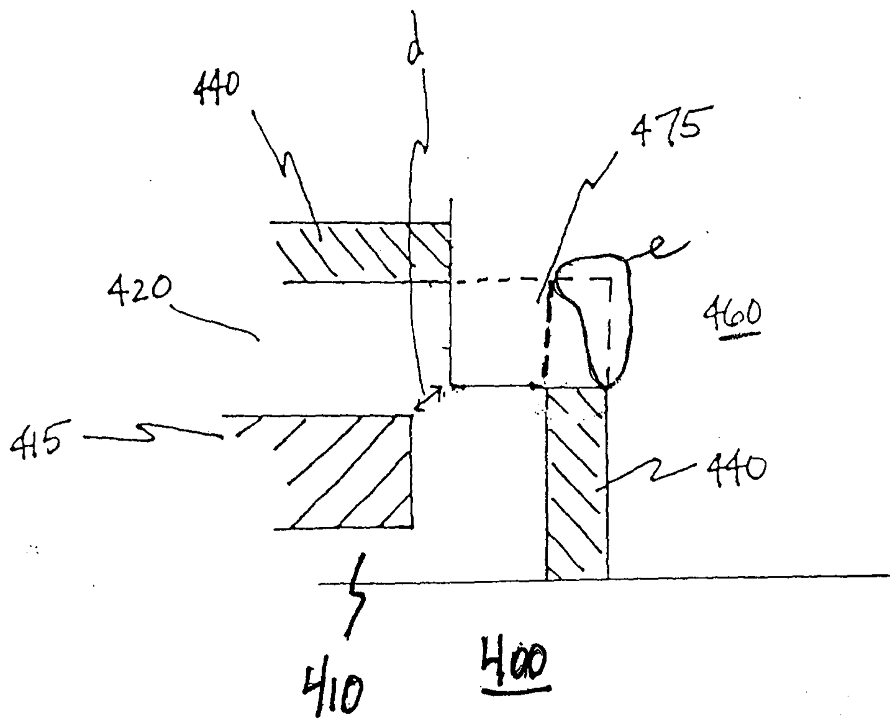
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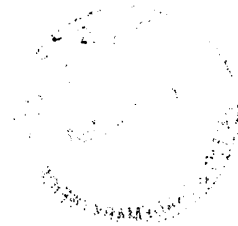

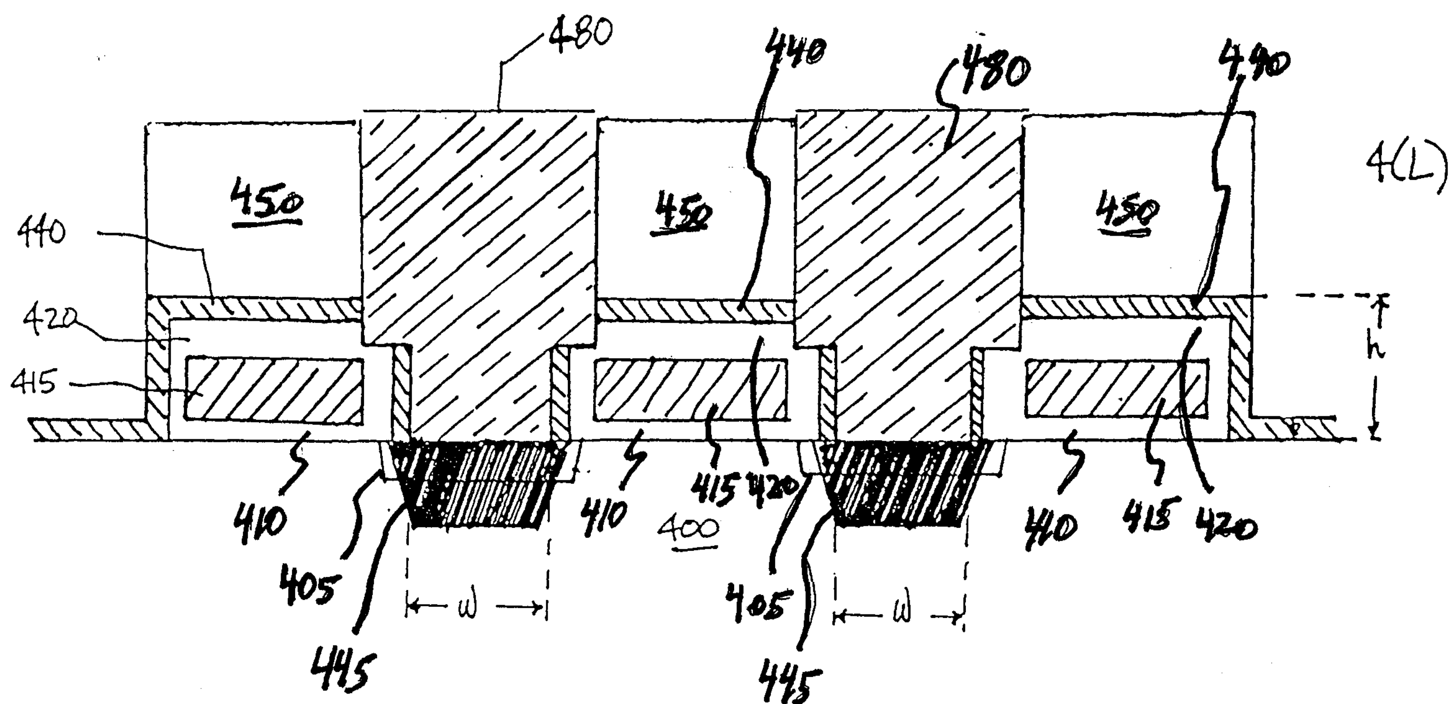
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Blakely Sokoloff Taylor & Zafman
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025

EXAMINER	
CHU, CHRIS C	
ART UNIT	**PAPER NUMBER**
2815	7

DATE MAILED: 01/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No.	Applicant(s)
	09/540,610	NULTY ET AL.
	Examiner	Art Unit
	Chris C. Chu	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *October 4, 2001*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25 - 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25 - 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. The amendment filed on October 4, 2001 has been received and entered in this office action.

Amend claims: 25, 26, and 34.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 25 and 27 ~ 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Dennison et al.

Regarding claim 25, Dennison et al. discloses the etch stop layer (20) is silicon nitride (column 3, line 35).

Regarding claim 27, note Fig. 2 of Dennison et al., where the reference shows a structure (10), comprising: a conductive layer (12 and column 3, lines 29 ~ 33) disposed over a substrate; a first insulating layer (18) on the conductive layer; a contact region (the area of 34) in the first insulating layer; at least one insulating spacer (18) in the contact region adjacent to the first insulating layer (see Fig. 2); and an etch stop material (20 and

column 3, line 35) over the first insulating layer and adjacent to the insulating spacer (see Fig. 2), the etch stop material being distinct from the insulating spacer (see Fig. 2 and column 3, lines 32 ~ 38).

Regarding claim 28, Fig. 2 of Dennison et al., where the reference shows the insulating spacer (18) has a substantially rectangular profile in the contact region (see Fig. 2).

Regarding claims 29 and 36, Fig. 2 of Dennison et al., where the reference shows the insulating spacer (18) has a surface portion in the contact region without overlying etch stop material (see Fig. 2).

Regarding claims 30 and 37, Fig. 2 of Dennison et al., where the reference shows the insulating spacer (18) surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from the substrate (see Fig. 2).

Regarding claim 31, Fig. 2 of Dennison et al., where the reference shows the insulating spacer (18) has a surface portion in the contact region without overlying etch stop material (see Fig. 2).

Regarding claims 32 and 38, Fig. 2 of Dennison et al., where the reference shows a structure (10), further comprising a second insulating layer (28) on the etch stop layer and over the conductive layer (see Fig. 2).

Regarding claims 33 and 39, Fig. 2A of Dennison et al., where the reference shows a structure (10), further comprising a second conductive material (40) in the contact region (see Fig. 2A).

Regarding claim 34, Fig. 2 of Dennison et al., where the reference shows a structure, comprising the step of: a first electrically conductive material (24) formed in

and/or on a surface of a substrate; a contact opening (the area of 34) in a region adjacent to a second electrically conductive material (the area of 40 in Fig. 2A) formed on the substrate; an electrically insulative spacer (18) in the contact opening adjacent to the second electrically conductive material (see Fig. 2); an etch stop material (20) over the electrically insulative spacer and the first and second electrically conductive materials (see Fig. 2), the etch stop material being distinct from the insulative spacer (see Fig. 2); a blanket layer (28) over the etch stop material; and an opening through a first part of the etch stop material to the first electrically conductive material (see Fig. 2).

Regarding claim 35, Fig. 2 of Dennison et al., where the reference shows the electrically insulative spacer (18) has a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface (see Fig. 2).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dennison et al. in view of Gonzalez.

Dennison et al. discloses the claimed invention except the etch stop layer is silicon dioxide. However, Gonzalez discloses the etch stop layer is silicon dioxide (31 in Fig. 18). Thus, it would have been obvious to one of ordinary skill in the art at the time

when the invention was made to modify Dennison et al. by using the etch stop layer is silicon dioxide as taught by Gonzalez. The ordinary artisan would have been motivated to modify Dennison et al. in the manner described above for at least the purpose of preventing diffusion of element between layers.

Response to Arguments

6. Applicant's arguments filed on October 4, 2001 have been fully considered but they are not persuasive.

In page 20, paragraph 1, applicant argues "Dennison et al. describes a barrier layer rather than an etch stop material, and does not suggest that it is a distinct material from the insulating spacer." The argument is not persuasive. Note that the material of layer 20, Si_3N_4, is well known in the art to use as an etch stop material (read page 23, line 2 of instant invention).

Further, the recitation "an etch stop material [] is a distinct material from the insulating spacer" is not recited in the rejected claim(s). It is noted that the features upon which applicant relies (i.e., an etch stop material [] is a distinct material from the insulating spacer) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

For the above reasons, the rejections are maintained.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

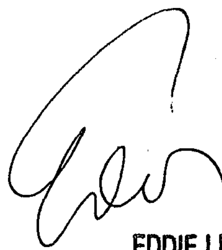
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
January 4, 2002



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Interview Summary	**Application No.**	**Applicant(s)**	
	09/540,610	NULTY ET AL.	
	Examiner	**Art Unit**	
	Chris C. Chu	2815	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Chris C. Chu*. (3) *Eddie Lee*.

(2) *Paul E. Rauch*. (4)_____.

Date of Interview: *14 March 2002* .

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____ .

Claim(s) discussed: *claim 27* .

Identification of prior art discussed: *Dennison et al.* .

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

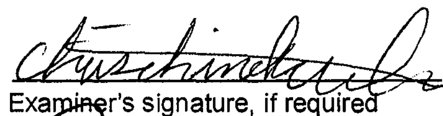
Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *Applicant argued that the claims define the material of the etch stop material as being distinct or different material from the material of the insulating spacer. However, no limitations regarding distinct material can be found in the claims.* .

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

i)☐ It is not necessary for applicant to provide a separate record of the substance of the interview(if box is checked).

Unless the paragraph above has been checked, THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.



Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case unless both applicant and examiner agree that the examiner will record same. Where the examiner agrees to record the substance of the interview, or when it is adequately recorded on the Form or in an attachment to the Form, the examiner should check the appropriate box at the bottom of the Form which informs the applicant that the submission of a separate record of the substance of the interview as a supplement to the Form is not required.

It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

BRINKS
HOFER
GILSON
&LIONE

A Professional Corporation
Intellectual Property Attorneys

NBC Tower - Suite 3600
455 N. Cityfront Plaza Drive
Chicago, Illinois 60611-5599
Facsimile 312-321-4299
Telephone 312-321-4200

Indianapolis, IN
Ann Arbor, MI
San Jose, CA
Arlington, VA

FACSIMILE COVER SHEET

Date: May 20, 2002

To: Examiner Chris C. Chu
Fax No: 703-746-3865
Group Art: 2815

From: Paul E. Rauch, Ph.D.
Tel. No: 312-321-4780

Serial No.: 09/540,610
Client No: 10200/12

No. of Pages
(inc. this page): 13

Confirmation Copy To Follow: Yes ___ No ✓

IF YOU HAVE ANY PROBLEMS RECEIVING THIS MESSAGE,
PLEASE CALL 312-321-4200 AND ASK FOR: Michelle Hoffman X4380

THIS MESSAGE IS INTENDED ONLY FOR THE INDIVIDUAL OR ENTITY TO WHICH IT IS ADDRESSED. IT MAY CONTAIN PRIVILEGED, CONFIDENTIAL, ATTORNEY WORK PRODUCT, OR TRADE SECRET INFORMATION WHICH IS EXEMPT FROM DISCLOSURE UNDER APPLICABLE LAWS. IF YOU ARE NOT THE INTENDED RECIPIENT, OR AN EMPLOYEE OR AGENT RESPONSIBLE FOR DELIVERING THE MESSAGE TO THE INTENDED RECIPENT, YOU ARE HEREBY NOTIFIED THAT ANY DISSEMINATION, DISTRIBUTION, OR COPYING OF THIS MESSAGE IS STRICTLY PROHIBITED. IF YOU HAVE RECEIVED THIS MESSAGE IN ERROR, PLEASE NOTIFY US IMMEDIATELY BY TELEPHONE AND RETURN THE ORIGINAL MESSAGE (AND ALL COPIES) TO US BY MAIL AT THE ABOVE ADDRESS. WE WILL REIMBURSE YOU FOR POSTAGE.

COVER MESSAGE:

Courtesy copy for Examiner: This is a copy of what was originally faxed to the Group Art Unit on April 29, 2002. Included at the end is a copy of our facsimile confirmation page.

TECHNOLOGY CENTER 2800
MAY 20 2002
FAX COPY RECEIVED

Received from < 312 321 4299 > at 5/20/02 3:26:23 PM [Eastern Daylight Time]

..ANSMITTAL LETTER			Case No. 10200/12 Client Ref. No. PM95012D
Serial No. 09/540,610	Filing Date March 31, 2000	Examiner Chris C. Chu	Group Art Unit 2815
Inventor(s) Nulty et al.			
Title of Invention STRUCTURE HAVING REDUCED LATERAL SPACER EROSION			

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is Transmittal Letter (in duplicate), Petition and Fee for One (1) Month Extension of Time (in duplicate), and Amendment and Response After Final.

☐ Small entity status of this application under 37 CFR § 1.27 has been established by verified statement previously submitted.

☐ A verified statement to establish small entity status under 37 CFR §§ 1.9 and 1.27 is enclosed.

☒ Petition for a 1 month extension of time.

☒ No additional fee is required.

☐ The fee has been calculated as shown below:

	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra	Small Entity Rate	Small Entity Add'l Fee	or	Other Than Small Entity Rate	Other Than Small Entity Add'l Fee
Total		Minus			x $9 =			x $18 =	
Indep.		Minus			x 42 =			x $84 =	
First Presentation of Multiple Dep. Claim					+ $140 =			+ $280 =	
					Total add'l fee	$		Total add'l fee	$

☒ Please charge Deposit Account No. 23-1925 (BRINKS HOFER GILSON & LIONE) in the amount of $110. A duplicate copy of this sheet is enclosed.

☐ A check in the amount of $_____ to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge payment of any additional filing fees required under 37 CFR § 1.16 and any patent application processing fees under 37 CFR § 1.17 associated with this communication or credit any overpayment to Deposit Account No. 23-1925. A duplicate copy of this sheet is enclosed.

☒ I hereby petition under 37 CFR § 1.136(a) for any extension of time required to ensure that this paper is timely filed. Please charge any associated fees which have not otherwise been paid to Deposit Account No. 23-1925. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicants

00757
PATENT TRADEMARK OFFICE

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200

I hereby certify that this correspondence is being sent via facsimile 703-308-7722 to Examiner Chris C. Chu, Group Art Unit 2815, at the United States Patent and Trademark Office on: 5/20/02

Date: 5/20/02 Signature:

MAY 20 2002
TECHNOLOGY CENTER 2800

Received from < 312 321 4299 > at 5/20/02 3:26:23 PM [Eastern Daylight Time]

TRANSMITTAL LETTER			Case No. 10200/12 Client Ref. No. PM95012D
Serial No. 09/540,610	Filing Date March 31, 2000	Examiner Chris C. Chu	Group Art Unit 2815
Inventor(s) Nulty et al.			
Title of Invention STRUCTURE HAVING REDUCED LATERAL SPACER EROSION			

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is Transmittal Letter (in duplicate), Petition and Fee for One (1) Month Extension of Time (in duplicate), and Amendment and Response After Final.

☐ Small entity status of this application under 37 CFR § 1.27 has been established by verified statement previously submitted.

☐ A verified statement to establish small entity status under 37 CFR §§ 1.9 and 1.27 is enclosed.

☒ Petition for a 1 month extension of time.

☒ No additional fee is required.

☐ The fee has been calculated as shown below:

	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra	Small Entity Rate	Small Entity Add'l Fee	or	Other Than Small Entity Rate	Other Than Small Entity Add'l Fee
Total		Minus			x $9=			x $18=	
Indep.		Minus			x 42=			x $84=	
First Presentation of Multiple Dep. Claim					+$140 =			+$280=	
					Total add'l fee	$		Total add'l fee	$

☒ Please charge Deposit Account No. 23-1925 (BRINKS HOFER GILSON & LIONE) in the amount of $110. A duplicate copy of this sheet is enclosed.

☐ A check in the amount of $_____ to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge payment of any additional filing fees required under 37 CFR § 1.16 and any patent application processing fees under 37 CFR § 1.17 associated with this communication or credit any overpayment to Deposit Account No. 23-1925. A duplicate copy of this sheet is enclosed.

☒ I hereby petition under 37 CFR § 1.136(a) for any extension of time required to ensure that this paper is timely filed. Please charge any associated fees which have not otherwise been paid to Deposit Account No. 23-1925. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicants

00757
PATENT TRADEMARK OFFICE

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200

I hereby certify that this correspondence is being sent via facsimile 703-308-7722 to Examiner Chris C. Chu, Group Art Unit 2815, at the United States Patent and Trademark Office on: 5/21/02

Date: 5/21/02 Signature:

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MAY 20 2002
TECHNOLOGY CENTER 2800

Received from < 312 321 4299 > at 5/20/02 3:26:23 PM [Eastern Daylight Time]

I hereby certify that this correspondence is being sent via facsimile 703-308-7722 to Examiner Chris C. Chu, Group Art Unit 2815, at the United States Patent and Trademark Office on:

4/29/02
Date of Facsimile

Paul E. Rauch, Ph.D. – Reg. No. 38,591
Name of applicant, assignee or Registered Representative

Signature

4/29/02
Date of Signature

Our Case No. 10200/12
Cypress Ref. No. PM95012D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

James E. Nulty et al.

Serial No. 09/540,610

Filing Date: March 31, 2000

For Structure Having Reduced Lateral Spacer Erosion

Examiner Chu, Chris C.

Group Art Unit No.2815

AMENDMENT AND RESPONSE AFTER FINAL

Commissioner for Patents
Washington, D.C. 20231

Dear Madam:

Responsive to the Final Office Action mailed January 9, 2002, Applicants respectfully request reconsideration in light of the following amendments and remarks.

IN THE CLAIMS

Please amend claims 25-27 and 34 as follows.

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MAY 20 2002
TECHNOLOGY CENTER 2800

Received from < 312 321 4299 > at 5/20/02 3:26:23 PM [Eastern Daylight Time]

25. (Twice Amended) The semiconductor apparatus of claim 27 wherein said etch stop material comprises silicon nitride.

26. (Twice Amended) The semiconductor apparatus of claim 27 wherein said etch stop material comprises silicon dioxide.

27. (Amended) A structure, comprising:

(a) a conductive layer disposed over a substrate;

(b) a first insulating layer on the conductive layer;

(c) a contact region in said first insulating layer;

(d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and

(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer.

34. (Twice amended) A structure, comprising:

(a) a first electrically conductive material formed in and/or on a surface of a substrate;

(b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate;

(c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material;

(d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer;

(e) a blanket layer over the etch stop material; and

(f) an opening through a first part of the etch stop material to the first electrically conductive material.

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TECHNOLOGY CENTER 2800

Received from < 312 321 4299 > at 5/20/02 3:26:23 PM [Eastern Daylight Time]

SUPPORT FOR AMENDMENT

The amendments of claims 27 and 34 are supported on page 23, ln. 11-12. Claims 25-26 have been amended for clarity. Appendix A, attached herewith, is a marked-up version of the changes made to the claims. No new matter has been added. Claims 25-39 are pending.

REMARKS

Applicants thank the Examiner for the helpful telephone discussion on March 14, 2002. During this discussion, Applicants noted that the claimed invention specifies that the etch stop material is a different material than the insulating spacer.

The present invention relates to a semiconductor device with well defined contact openings. The current practice with respect to forming contact openings during the fabrication of semiconductor devices, particularly self aligned contact openings, is to use etchants with high selectivity to protect underlying regions. However, the properties of a highly selective etch of the overlying etch stop layer can transform a substantially rectangular spacer adjacent to the contact region into a sloped spacer. Before the conductive material is added to the contact opening, the opening is cleaned with a sputter etch whichcan erode a portion of the sloped insulating spacer. Thus, in conventional self-aligned contact structures, the diagonal thickness of the spacer, rather than the vertical thickness of the insulating layer, determines the minimum insulating layer thickness for the gate. Sloping spacers limit the number of structures that can be included on a device.

The present invention avoids this problem by retaining the substantially rectangular profile of the insulating spacers. The present invention includes at least one insulating spacer in the contact region and an etch stop material over the first insulating layer and adjacent to the insulating spacer, the etch stop material being different from the insulating spacer.

Rejections under 35 U.S.C. § 102 and 103

The rejection of the claims under 35 U.S.C. § 102 and 103 over Dennison et al. (U.S. Pat. No. 5,338,700), either alone or in combination with Gonzalez (U.S. Pat. No. 5,234,856), is respectfully traversed. Dennison et al. describes a barrier layer rather

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SAMSUNG-1002.152

than an etch stop material, and does not suggest that it is a different material from the insulating spacer.

Dennison et al. describes a method of forming a bit line over a capacitor array of memory cells. The semiconductor wafer of Dennison et al. has an array of electrically isolated word lines **12**, **14** and **16** having insulating spacers and caps **18** (Figure 1). The spacers and caps **18** preferably comprise an insulative nitride, such as Si_3N_4 (col. 3, ln. 33-34). The reference further states "a thin layer **20** of Si_3N_4 is provided atop the wafer to function as a diffusion barrier" (col. 3, ln. 34-36). Dennison et al. does not teach or suggest that the spacers and caps **18** and diffusion barrier **20** are different materials. On the contrary, the reference specifically teaches that **18** and **20** are the same material. Furthermore, since **20** is a diffusion barrier, not an etch stop, there would be no reason to use a material distinct from the spacer **18**.

Gonzalez describes a dynamic random access memory cell having a stacked-trench capacitor that is resistant to alpha particle generated soft errors. Gonzalez only describes silicon dioxide in spacers **31** (col. 5, ln. 10-12).

The claimed invention includes an etch stop material that is different from the insulating spacer. The barrier layer of Dennison et al. is described as Si_3N_4, the same material as the spacers. Furthermore, there is no suggestion that they be formed from different materials since the barrier layer is not intended to function as an etch stop layer. The combination with Gonzalez does not correct this deficiency.

Therefore, Applicants submit that Dennison et al., either alone or in combination with Gonzalez, does not anticipate nor make obvious the claimed invention. Withdrawal of the rejection of the claims on these grounds is respectfully requested.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicants

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200

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APPENDIX A

25. (Twice Amended) The semiconductor apparatus of claim 27 wherein said etch stop [layer] material comprises silicon nitride.

26. (Twice Amended) The semiconductor apparatus of claim 27 wherein said etch stop [layer] material comprises silicon dioxide.

27. (Amended) A structure, comprising:

(a) a conductive layer disposed over a substrate;

(b) a first insulating layer on the conductive layer;

(c) a contact region in said first insulating layer;

(d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and

(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a [distinct] different material from the insulating spacer.

34. (Twice amended) A structure, comprising:

(a) a first electrically conductive material formed in and/or on a surface of a substrate;

(b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate;

(c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material;

(d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a [distinct] different material from the insulative spacer;

(e) a blanket layer over the etch stop material; and

(f) an opening through a first part of the etch stop material to the first electrically conductive material.

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I hereby certify that this correspondence is being sent via facsimile 703-308-7722 to Examiner Chris C. Chu, Group Art Unit 2815, at the United States Patent and Trademark Office on: 4/29/02

Date of Facsimile

Paul E. Rauch, Ph.D. – Reg. No. 38,591

Name of applicant, assignee or Registered Representative

Signature

4/29/02

Date of Signature

BHGL Case No. 10200/12
Client Ref. No. PM95012D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
James E. Nulty et al.	
Serial No: 09/540,610	Examiner: Chris C.Chu
Filed: March 31, 2000	Group Art Unit: 2815
For: Structure Having Reduced Lateral Spacer Erosion	

PETITION AND FEE FOR EXTENSION OF TIME (37 CFR § 1.136(a))

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This is a petition for an extension of time to respond to the Office Action dated January 9, 2002 for a period of 1 month.

☒ Applicant is:

☐ a small entity

☒ other than small entity

Received from < 312 321 4299 > at 5/20/02 3:26:23 PM [Eastern Daylight Time]

BHGL Case No. 10200/12
Client Ref. No. PM95012D

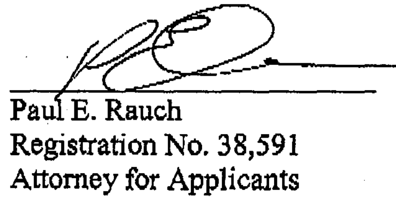
	Extension Months	Other Than Small Entity	Small Entity
☒	One Month	$110.00	$55.00
☐	Two Months	$400.00	$200.00
☐	Three Months	$920.00	$460.00
☐	Four Months	$1,440.00	$720.00
☐	Five Months	$1,960.00	$980.00

Fee Payment

☐ Attached is a check for $_____ for the Petition fee.
☒ Charge Petition fee to Deposit Account No. 23-1925. A duplicate copy of this Petition is attached.
☒ Charge any additional fee required or credit for any excess fee paid to Deposit Account No. 23-1925. A duplicate copy of this Petition is attached.

Respectfully submitted,

Dated: 4/19/02



Paul E. Rauch
Registration No. 38,591
Attorney for Applicants

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, IL 60610
(312) 321-4200

Received from < 312 321 4299 > at 5/20/02 3:26:23 PM [Eastern Daylight Time]

SAMSUNG-1002.156

#9/Ext. of Time (1)
6.6.02
C. Will

I hereby certify that this correspondence is being sent via facsimile 703-308-7722 to Examiner Chris C. Chu, Group Art Unit 2815, at the United States Patent and Trademark Office on: 4/29/02

Date of Facsimile

Paul E. Rauch, Ph.D. – Reg. No. 38,591

Name of applicant, assignee or Registered Representative

Signature

4/29/02

Date of Signature

BHGL Case No. 10200/12
Client Ref. No. PM95012D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
James E. Nulty et al.	
Serial No: 09/540,610	Examiner: Chris C.Chu
Filed: March 31, 2000	Group Art Unit: 2815
For: Structure Having Reduced Lateral Spacer Erosion	

PETITION AND FEE FOR EXTENSION OF TIME (37 CFR § 1.136(a))

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This is a petition for an extension of time to respond to the Office Action dated January 9, 2002 for a period of 1 month.

☒ Applicant is:

- ☐ a small entity
- ☒ other than small entity

Received from < 312 321 4299 > at 5/20/02 3:26:23 PM [Eastern Daylight Time]

BHGL Case No. 10200/12
Client Ref. No. PM95012D

	Extension Months	Other Than Small Entity	Small Entity
☒	One Month	$110.00	$55.00
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☐	Three Months	$920.00	$460.00
☐	Four Months	$1,440.00	$720.00
☐	Five Months	$1,960.00	$980.00

Fee Payment

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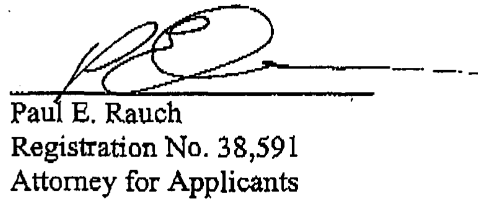
☒ Charge Petition fee to Deposit Account No. 23-1925. A duplicate copy of this Petition is attached.

☒ Charge any additional fee required or credit for any excess fee paid to Deposit Account No. 23-1925. A duplicate copy of this Petition is attached.

Respectfully submitted,

Dated: 4/29/02



Paul E. Rauch
Registration No. 38,591
Attorney for Applicants

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, IL 60610
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****************** -COMM. JP~ NHL- ****************

MODE = MEMORY TRANSMISSION START=APR-29 18:33 END=APR-29 18:37

FILE NO.=205

STN NO.	COMM.	ONE-TOUCH/ ABBR NO.	STATION NAME/TEL NO.	PAGES	DURATION
001	OK	≡	*#571020091703308772 2	012/012	00:02:46

-BHG & L

** -BGH & L - ***** - 312 321 4299- **********

BRINKS
HOFER
GILSON
&LIONE

A Professional Corporation
Intellectual Property Attorneys

NBC Tower • Suite 3600
455 N. Cityfront Plaza Drive
Chicago, Illinois 60611-5599
Facsimile 312-321-4299
Telephone 312-321-4200

San Jose, CA
Indianapolis, IN
Ann Arbor, MI
Arlington, VA

FACSIMILE COVER SHEET

Date: April 29, 2002

To: Examiner Chris C. Chu
Fax No: (703) 308-7722

From: Paul E. Rauch, Ph.D.

Tel. No: (312) 321-4780

Client No: 10200/12
Cypress Ref. No. PM95012D

No. of Pages
(inc. this page): 12

Confirmation Copy To Follow: Yes ☐ No ☒

IF YOU HAVE ANY PROBLEMS RECEIVING THIS MESSAGE,
PLEASE CALL 312-321-4200 AND ASK FOR: Erika Mitchell @ ext. 4668

THIS MESSAGE IS INTENDED ONLY FOR THE INDIVIDUAL OR ENTITY TO WHICH IT IS ADDRESSED. IT MAY CONTAIN PRIVILEGED, CONFIDENTIAL, ATTORNEY WORK PRODUCT, OR TRADE SECRET INFORMATION WHICH IS EXEMPT FROM DISCLOSURE UNDER APPLICABLE LAWS. IF YOU ARE NOT THE INTENDED RECIPIENT, OR AN EMPLOYEE OR AGENT RESPONSIBLE FOR DELIVERING THE MESSAGE TO THE INTENDED RECIPIENT, YOU ARE HEREBY NOTIFIED THAT ANY DISSEMINATION, DISTRIBUTION, OR COPYING OF THIS MESSAGE IS STRICTLY PROHIBITED. IF YOU HAVE RECEIVED THIS MESSAGE IN ERROR, PLEASE NOTIFY US IMMEDIATELY BY TELEPHONE AND RETURN THE ORIGINAL MESSAGE (AND ALL COPIES) TO US BY MAIL AT THE ABOVE ADDRESS. WE WILL REIMBURSE YOU FOR POSTAGE.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,610	03/31/2000	James E. Nulty	16820.P097	2171

7590 06/13/2002

Blakely Sokoloff Taylor & Zafman
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025

EXAMINER
CHU, CHRIS C

ART UNIT	PAPER NUMBER
2815	11

DATE MAILED: 06/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Advisory Action	Application No.	Applicant(s)	
	09/540,610	NULTY ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 20 May 2002 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 4 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1.☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2.☒ The proposed amendment(s) will not be entered because:

(a) ☒ they raise new issues that would require further consideration and/or search (see NOTE below);

(b) ☐ they raise the issue of new matter (see Note below);

(c) ☒ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: *See Continuation Sheet*.

3.☐ Applicant's reply has overcome the following rejection(s): _____.

4.☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5.☐ The a)☐ affidavit, b)☐ exhibit, or c)☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

6.☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7.☒ For purposes of Appeal, the proposed amendment(s) a)☒ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____.

Claim(s) objected to: _____.

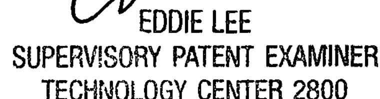
Claim(s) rejected: 25 - 39.

Claim(s) withdrawn from consideration: _____.

8.☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9.☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10.☐ Other: _____



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Continuation of 2. NOTE: The proposed amendment to claims 25 - 27and 34 raise new issues which require further consideration and/or search.

SAMSUNG-1002.162

6-7-02

Date of Deposit: June 5, 2002

"Express Mail" mailing label number EL 669 271 865 US

CPA 2815 #12 6-28-02

CONTINUED PROSECUTION APPLICATION (CPA) REQUEST TRANSMITTAL

Submit an original, and a duplicate for fee processing.

(Only for Continuation or Divisional applications under 37 C.F.R. § 1.53(d))

CHECK BOX, if applicable: ☐ **DUPLICATE**

Address to: Commissioner for Patents Box CPA Washington, DC 20231		
	Attorney Docket No. of Prior Application	10200/12
	First Named Inventor	J. Nulty
	Examiner Name	C. Chu
	Group/Art Unit.	2815
	Express Mail Label No.	EL 669 271 865 US

This is a request for a ☒ continuation or ☐ divisional application under 37 C.F.R. § 1.53(d), (continued prosecution application (CPA)) of prior application number 09/540,610, filed March 31, 2000, entitled Structure Having Reduced Lateral Spacer Erosion.

NOTES

FILING QUALIFICATIONS: *The prior application identified above must be a nonprovisional application that is either: (1) complete as defined by 37 C.F.R. § 1.51(b), or (2) the national stage of an international application in compliance with 35 U.S.C. § 371.*

C-I-P NOT PERMITTED: *A continuation-in-part application cannot be filed as a CPA under 37 C.F.R. § 1.53(d), but must be filed under 37 C.F.R. § 1.53(b).*

EXPRESS ABANDONMENT OF PRIOR APPLICATION: *The filing of this CPA is a request to expressly abandon the prior application as of the filing date of the request for a CPA. 37 C.F.R. § 1.53(b) must be used to file a continuation, divisional, or continuation-in-part of an application that is not to be abandoned.*

ACCESS TO PRIOR APPLICATION: *In a CPA, no reference to the prior application is needed in the first sentence of the specification and none should be submitted. If a sentence referencing the prior application is submitted, it will not be entered. A request for a CPA is the specific request required by 35 U.S.C. § 120 and to every application assigned the application number identified in such request, 37 C.F.R. § 1.78(a).*

1. ☒ Enter the unentered amendment previously filed on April 29, 2002 under 37 C.F.R. § 1.116 in the prior nonprovisional application.
2. ☐ A preliminary amendment is enclosed.
3. This application is filed by fewer than all the inventors named in the prior application, 37 C.F.R. § 1.53(d)(4).
   a. ☐ ***DELETE*** the following inventor(s) named in the prior nonprovisional application:
   ______.
   b. ☐ The inventor(s) to be deleted are set forth on a separate sheet attached hereto.
4. ☐ A new power of attorney or authorization of agent is enclosed.
5. Information Disclosure Statement (IDS) is enclosed:
   a. ☐ PTO-1449
   b. ☐ Copies of IDS Citations

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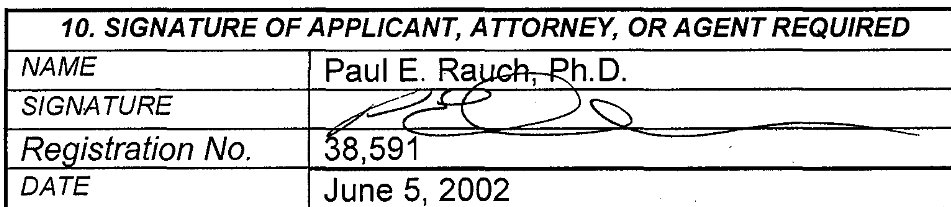
Rev. Oct.-01

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 C.F.R. § 1.16(c))	15 - 20 =	0	x $ 18.00	$
	INDEPENDENT CLAIMS (37 C.F.R. § 1.16(b))	2 - 3 =	0	x $ 84.00	
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 C.F.R. § 1.16(d))			+ $ 280.00	
				BASIC FEE (37 C.F.R. § 1.16(a)	740.00
			Total of above Calculations =		
	Reduction by 50% for filing by small entity (Note 37 C.F.R. §§ 1.9, 1.27, 1.28).				
				TOTAL =	$740.00

6. Small entity status:
   a. ☐ A small entity statement is enclosed.
   b. ☐ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
   c. ☐ Is no longer claimed.
7. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 23-1925:
   a. ☒ Fees required under 37 C.F.R. § 1.16.
   b. ☐ Fees required under 37 C.F.R. § 1.17.
   c. ☐ Fees required under 37 C.F.R. § 1.18.
8. ☒ A check in the amount of $ 740 is enclosed.
9. ☐ Other:______.

NOTE: ***The prior application's correspondence address will carry over to this CPA UNLESS a new correspondence address is provided.***



10. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED	
NAME	Paul E. Rauch, Ph.D.
SIGNATURE	
Registration No.	38,591
DATE	June 5, 2002

Brinks Hofer Gilson & Lione
P.O. Box 10395
Chicago, IL 60610

Application or Docket Number

09/540610

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2001

CPA

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	15 minus 20=	* —
INDEPENDENT CLAIMS	2 minus 3 =	* —
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ RATE	FEE	OR	OTHER THAN SMALL ENTITY RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	740. pd.

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 8/01) Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/540,610	03/31/2000	2815	690	16820.P097	8	13	2

CONFIRMATION NO. 2171

Blakely Sokoloff Taylor & Zafman
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025

CORRECTED FILING RECEIPT

OC000000008372391

Date Mailed: 06/28/2002

Receipt is acknowledged of a CPA in this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

James E. Nulty, San Jose, CA;
Christopher J. Petti, Mountain View, CA;

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted 06/02/2000

CPA filed on: 06/05/2002

Projected Publication Date: 10/10/2002

Non-Publication Request: No

Early Publication Request: No

Title

STRUCTURE HAVING REDUCED LATERAL SPACER EROSION

Preliminary Class

257

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,610	03/31/2000	James E. Nulty	16820.P097	2171

7590 09/11/2002

Blakely Sokoloff Taylor & Zafman
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025

EXAMINER	
CHU, CHRIS C	
ART UNIT	PAPER NUMBER
2815	13

DATE MAILED: 09/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No.	Applicant(s)
	09/540,610	NULTY ET AL.
	Examiner	Art Unit
	Chris C. Chu	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 20 May 2002.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 25 - 39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 25 - 39 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on May 20, 2002 has been received and entered in this office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 25 and 27 ~ 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dennison et al. in view of Figura et al.

Regarding claim 25, Dennison et al. discloses in column 3, line 35 the etch stop material (20) being silicon nitride.

Regarding claim 27, Dennison et al. discloses in Fig. 2 a structure (10), comprising:

- a conductive layer (12 and column 3, lines 29 ~ 33) disposed over a substrate;
- a first insulating layer (18) on the conductive layer;
- a contact region (the area of 34) in the first insulating layer;

- at least one insulating spacer (18) in the contact region adjacent to the first insulating layer (see Fig. 2); and
- an etch stop material (20 and column 3, line 35) over the first insulating layer and adjacent to the insulating spacer (see Fig. 2).

Dennison et al. does not disclose the etch stop material being a different material from the insulating spacer. However, Figura et al. discloses in Fig. 1 an etch stop material (column 4, lines 51 and 52) being a different material from the insulating spacer (column 4, lines 11 and 12). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Dennison et al. by using different materials for the etch stop material and the insulating spacer as taught by Figura et al. The ordinary artisan would have been motivated to modify Dennison et al. in the manner described above for at least the purpose of minimizing current leakage and short circuits (column 2, lines 36 ~ 38).

Regarding claim 28, Dennison et al. discloses in Fig. 2 the insulating spacer (18) having a substantially rectangular profile in the contact region (see Fig. 2).

Regarding claims 29 and 36, Dennison et al. discloses in Fig. 2 the insulating spacer (18) having a surface portion in the contact region without overlying etch stop material (see Fig. 2).

Regarding claims 30 and 37, Dennison et al. discloses in Fig. 2 the insulating spacer (18) surface portion without overlying etch stop material comprising an insulating spacer surface portion most distant from the substrate (see Fig. 2).

Regarding claim 31, Dennison et al. discloses in Fig. 2 the insulating spacer (18) having a surface portion in the contact region without overlying etch stop material (see Fig. 2).

Regarding claims 32 and 38, Dennison et al. discloses in Fig. 2 a structure (10), further comprising a second insulating layer (28) on the etch stop layer and over the conductive layer (see Fig. 2).

Regarding claims 33 and 39, Dennison et al. discloses in Fig. 2A a structure (10), further comprising a second conductive material (40) in the contact region (see Fig. 2A).

Regarding claim 34, Dennison et al. discloses in Fig. 2 a structure, comprising the step of:

- a first electrically conductive material (24) formed in and/or on a surface of a substrate;
- a contact opening (the area of 34) in a region adjacent to a second electrically conductive material (the area of 40 in Fig. 2A) formed on the substrate;
- an electrically insulative spacer (18) in the contact opening adjacent to the second electrically conductive material (see Fig. 2);
- an etch stop material (20) over the electrically insulative spacer and the first and second electrically conductive materials (see Fig. 2);
- a blanket layer (28) over the etch stop material; and
- an opening through a first part of the etch stop material to the first electrically conductive material (see Fig. 2).

Dennison et al. does not disclose the etch stop material being a different material from the insulating spacer. However, Figura et al. discloses in Fig. 1 an etch stop material (column 4, lines 51 and 52) being a different material from the insulating spacer (column 4, lines 11 and 12). Thus, it would have been obvious to one of ordinary skill in the art at the time when the

invention was made to modify Dennison et al. by using different materials for the etch stop material and the insulating spacer as taught by Figura et al. The ordinary artisan would have been motivated to modify Dennison et al. in the manner described above for at least the purpose of minimizing current leakage and short circuits (column 2, lines 36 ~ 38).

Regarding claim 35, Dennison et al. discloses in Fig. 2 the electrically insulative spacer (18) having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface (see Fig. 2).

4. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dennison et al. and Figura et al. as applied to claim 27 above, and further in view of Gonzalez.

Dennison et al. and Figura et al. disclose the claimed invention except the etch stop material being silicon dioxide. However, Gonzalez discloses an etch stop material being silicon dioxide (31 in Fig. 18). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Dennison et al. by using silicon dioxide for the etch stop material as taught by Gonzalez. The ordinary artisan would have been motivated to further modify Dennison et al. in the manner described above for at least the purpose of preventing diffusion of element between layers.

Response to Arguments

5. Applicant's arguments with respect to claims 25 ~ 27 and 34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

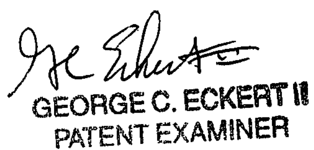
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
August 14, 2002



GEORGE C. ECKERT II
PATENT EXAMINER

Notice of References Cited	Application/Control No. 09/540,610	Applicant(s)/Patent Under Reexamination NULTY ET AL.	
	Examiner Chris C. Chu	Art Unit 2815	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5488011 - A	01-1996	Figura et al.	438/253
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

#14

I hereby certify that this correspondence is being sent via facsimile 703-308-7382 to Examiner Chris C. Chu at the United States Patent and Trademark Office on

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Date of Facsimile

Paul E. Rauch, Ph.D.
Name of Applicant, assignee or Registered Representative

Signature

Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
James E. Nulty, et al.	
Serial No. 09/540,610	Examiner Chris C. Chu
Filing Date: March 31, 2000	Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning	

PETITION AND FEE FOR EXTENSION OF TIME (37 CFR § 1.136(a))

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This is a petition for an extension of the time to respond to the Office Action dated September 11, 2002 for a period of three months.

Please charge the $930.00 filing fee to American Express Account No. 3785-716974-01002. A Credit Card Payment Form is attached. A duplicate copy of this Petition is attached.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicant

SONNENSCHEIN NATH & ROSENTHAL
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
(312) 876-8000

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Name of Applicant, assignee or Registered Representative

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J. mcmilla
3/11/03

Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

James E. Nulty, et al.

Serial No. 09/540,610 — Examiner Chris C. Chu

Filing Date: March 31, 2000 — Group Art Unit No. 2815

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Registration No. 38,591
Attorney for Applicant

03/12/2003 JMCMILLA 00000006 09540610
01 FC:1253 930.00 OP

SONNENSCHEIN NATH & ROSENTHAL
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
(312) 876-8000

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This file wrapper was thoroughly reviewed by our technical staff. The Facsimile Cover Sheet is missing from the original USPTO file history.

This has been brought to your attention so that you will know it has not been overlooked.

PTO/SB/122 (10-01)
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#15 CAD J. McWilliams 3/11/03

CHANGE OF CORRESPONDENCE ADDRESS *Application*	Application Number	09/540,610
Address to:	Filing Date	March 31, 2000
Assistant Commissioner for Patents	First Named Inventor	James E. Nulty
Washington, D.C. 20231	Art Unit	2815
	Examiner Name	Chris C. Chu
	Attorney Docket Number	09799940-0011

Please change the Correspondence Address for the above-identified application to:

[X] Customer Number 26263 → *Place Customer Number Bar Code Label here*
Type Customer Number here

OR

[X] Firm *or* Individual Name	Sonnenschein Nath & Rosenthal				
Address	P.O. Box 061080				
Address	Wacker Drive Station				
City	Chicago	State	IL	ZIP	60606
Country	United States of America				
Telephone	312-876-8000	Fax	312-876-7934		

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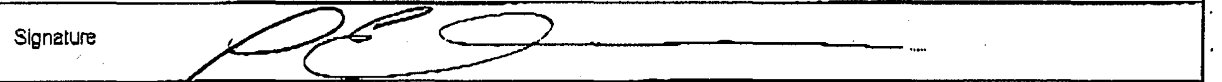
I am the :

[ ] Applicant/Inventor.

[ ] Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

[X] Attorney or Agent of record.

[ ] Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number ___________

Typed or Printed Name	Paul E. Rauch, Ph.D., Registration No. 38,591
Signature	
Date	3/4/03

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[X] *Total of 1 forms are submitted.

Burden Hour Statement: This form is estimated to take 3 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

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Date of Facsimile

Paul E. Rauch, Ph.D.
Name of Applicant, assignee or Registered Representative

Signature

Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
James E. Nulty, et al.)
Serial No. 09/540,610) Examiner Chris C. Chu
Filing Date: March 31, 2000) Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning)

TRANSMITTAL

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Transmitted herewith is:

- ☒ Credit Card Payment Form
- ☒ Three Month Extension of Time
- ☒ Amendment and Request for Reconsideration
- ☒ No additional fee is required for additional Independent, Dependent or Multiple Dependent Claims.
- ☒ The Commissioner is hereby authorized to charge any fees associated with this communication or credit any overpayment to Deposit Account No. 19-3140. A duplicate copy of this sheet is attached.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicants

SONNENSCHEIN NATH & ROSENTHAL
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
(312) 876-8000

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Paul E. Rauch, Ph.D.
Name of Applicant, assignee or Registered Representative

Signature

Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)
James E. Nulty, et al.	)
Serial No. 09/540,610	) Examiner Chris C. Chu
Filing Date: March 31, 2000	) Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning	)

TRANSMITTAL

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Transmitted herewith is:

☒ Credit Card Payment Form

☒ Three Month Extension of Time

☒ Amendment and Request for Reconsideration

☒ No additional fee is required for additional Independent, Dependent or Multiple Dependent Claims.

☒ The Commissioner is hereby authorized to charge any fees associated with this communication or credit any overpayment to Deposit Account No. 19-3140. A duplicate copy of this sheet is attached.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicants

SONNENSCHEIN NATH & ROSENTHAL
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
(312) 876-8000

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Date of Facsimile

Paul E. Rauch, Ph.D.
Name of Applicant, assignee or Registered Representative

Signature

#16 Response Req for Recon Jmcaniello 3/11/03

Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

James E. Nulty, et al.

Serial No. 09/540,610 — Examiner Chris C. Chu

Filing Date: March 31, 2000 — Group Art Unit No. 2815

For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning

AMENDMENT AND REQUEST FOR RECONSIDERATION

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Responsive to the Official Action of September 11, 2002 Applicants respectfully request reconsideration in light of the following remarks.

REMARKS

Applicants would like to thank the Examiner for indicating withdrawal of the previous grounds of rejection.

The present invention relates to a semiconductor device with well defined contact openings. In the past, the practice with respect to forming contact openings during the fabrication of semiconductor devices, particularly self-aligned contact openings, was to

use etchants with high selectivity to protect underlying regions. However, the properties of a highly selective etch of the overlying etch layer can transform a substantially rectangular spacer adjacent to the contact region into a sloped spacer. Before the conductor materials are added to the contact opening, the opening was cleaned with a sputter etchant which can erode a portion of the sloped insulating spacer. Thus in conventional self-aligned contact structures, the diagonal thickness of the spacer, rather than the vertical thickness of the insulating layer, determined the minimum insulating layer thickness for the gate. Sloping spacers limit the number of structures that can be included on a device.

The present invention avoids this problem by retaining the substantially rectangular profile of the insulating spacers. The present invention includes at least one insulating spacer in the contact region and an etch-stop material over a first insulating layer and adjacent to the insulating spacer, the etch-stop material being a different material from the insulating spacer.

The rejection of the claims under 35 U.S.C. § 103 over Dennison, et al., in view of Figura, et al., and optionally further in view of Gonzalez, is respectfully traversed. Dennison, et al. includes spacers and caps which act as an etch-stop material with respect to the overlying BPSG layer and therefore must be made of silicon nitride in order to function. The thin overlying layer **20** is described by Dennison, et al. as a barrier layer which prevents diffusion from the BPSG layer. Figura, et al. describes oxide spacers, a silicon nitride etch-stop layer, and does not describe any barrier layers.

Dennison, et al. describes a method of forming a bit line over a capacitor array of memory cells. The semiconductor wafer of Dennison, et al. has an array of electrically isolated word lines **12, 14,** and **16** having insulating spacers and caps **18**; the spacers and caps preferably comprise an insulative nitride, such as Si_3N_4 (Figure 1; column 3, lines 25-36). A thin layer **20** of Si_3N_4 is provided atop the wafer to function as a diffusion barrier (column 3, lines 34-36). Dennison, et al. is clear about the function of all of these structures:

> The principal purpose of barrier layer **20** is to prevent diffusion of boron or phosphorous atoms from BPSG layer **28** into active areas **24** and **26**. Caps [and spacers] **18** are preferably comprised of nitride (Si_3N_4) where

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layer **28** is comprised of oxide, such that the contact etch to produce first contacts **32** will stop relative to word lines spacers and caps **18.**

Accordingly, Dennison, et al., indicates that the caps and spacers act as an etch-stop material with respect to the overlying BPSG layer, and therefore need to be formed of a material such as silicon nitride. Dennison, et al. also indicates that barrier layer **20** functions to prevent diffusion from the overlying BPSG layer **28.**

Figura et al. describes a method of forming contact areas between vertical conductors. A structure is described which includes transistor gate electrodes **22** which include gate insulating protective layer **28**, and an insulating spacers **30** formed on either side of the gate electrodes (column 4, lines 6-10; Figure 1). The gate insulating protective layer **28** and insulating spacers **30** are preferably made of silicon dioxide; the lower insulating layer **36** on top of these structures is made of BPSG (column 4, lines 10-14; Figure 2). It is also noted that silicon nitride may be used instead of silicon dioxide for insulating protective layer **28** and spacers **30** (column 4, lines 22-24). Shown in Figure 3a, an etch-stop layer **43**, made of silicon nitride or other suitable material, is deposited *over* lower insulating layer **36** (column 4, lines 50-53).

Gonzalez has only been cited for a description of silicon dioxide spacers.

The spacers and caps of Dennison, et al. are required to act as an etch-stop material (see Dennison, et al., column 4, lines 6-10); the only etch-stop material described in any of the references is silicon nitride. Layer **20** in Dennison, et al. is described as a barrier layer for preventing diffusion; of all the references only Dennison, et al. describes a barrier layer, and the only material described is silicon nitride. If one were to substitute silicon oxide for the caps and spacers in Dennison, et al., then they would not act as an etch-stop material with respect to the overlying BPSG layer, and therefore such a substitution would destroy their function. Accordingly, although Figura, et al. does describe a specific embodiment where an etch-stop layer is silicon nitride and caps and spacers are formed from silicon oxide, changing the composition of the caps and spacers in Dennison, et al. would defeat their function. Furthermore, there is no suggestion to replace the barrier layer **20** of Dennison, et al. with a different material--nothing else is suggested in any of the references which would provide a barrier function other than silicon nitride. Gonzalez does not provide any additional

teaching to cure this deficiency. Accordingly, Applicants submit that combining the references defeats the purpose of Dennison, et al., and therefore the claimed invention is not obvious over the applied references. Withdrawal of this ground of rejection is respectfully requested.

Applicants respectfully request that the Examiner contact the undersigned upon the indication of any allowable subject matter. Applicants submit the application is now in condition for allowance. Early notice of such action is earnestly solicited.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicants

SONNENSCHEIN NATH & ROSENTHAL
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
(312) 876-8000

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,610	03/31/2000	James E. Nulty	16820.P097	2171

26263 7590 05/20/2003

SONNENSCHEIN NATH & ROSENTHAL
P.O. BOX 061080
WACKER DRIVE STATION
CHICAGO, IL 60606-1080

EXAMINER	
CHU, CHRIS C	
ART UNIT	**PAPER NUMBER**
2815	17

DATE MAILED: 05/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No.	Applicant(s)
	09/540,610	NULTY ET AL.
	Examiner	Art Unit
	Chris C. Chu	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 11 March 2003.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 25 - 39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 25 - 39 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on March 11, 2003 has been received and entered in the case.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 25 and 27 ~ 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dennison et al. in view of Figura et al.

Regarding claim 25, Dennison et al. discloses in column 3, line 35 the etch stop material (20) being silicon nitride.

Regarding claim 27, Dennison et al. discloses in Fig. 2 a structure (10), comprising:

- a conductive layer (12 and column 3, lines 29 ~ 33) disposed over a substrate;
- a first insulating layer (18) on the conductive layer;

- a contact region (the area of 34) in the first insulating layer;
- at least one insulating spacer (18) in the contact region adjacent to the first insulating layer (see Fig. 2); and
- an etch stop material (20 and column 3, line 35) over the first insulating layer and adjacent to the insulating spacer (see Fig. 2).

Dennison et al. does not disclose the etch stop material being a different material from the insulating spacer. However, Figura et al. discloses in Fig. 1 an etch stop material (column 4, lines 51 and 52) being a different material from the insulating spacer (column 4, lines 11 and 12). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Dennison et al. by using different materials for the etch stop material and the insulating spacer as taught by Figura et al. The ordinary artisan would have been motivated to modify Dennison et al. in the manner described above for at least the purpose of minimizing current leakage and short circuits (column 2, lines 36 ~ 38).

Regarding claim 28, Dennison et al. discloses in Fig. 2 the insulating spacer (18) having a substantially rectangular profile in the contact region (see Fig. 2).

Regarding claims 29 and 36, Dennison et al. discloses in Fig. 2 the insulating spacer (18) having a surface portion in the contact region without overlying etch stop material (see Fig. 2).

Regarding claims 30 and 37, Dennison et al. discloses in Fig. 2 the insulating spacer (18) surface portion without overlying etch stop material comprising an insulating spacer surface portion most distant from the substrate (see Fig. 2).

Regarding claim 31, Dennison et al. discloses in Fig. 2 the insulating spacer (18) having a surface portion in the contact region without overlying etch stop material (see Fig. 2).

Regarding claims 32 and 38, Dennison et al. discloses in Fig. 2 a structure (10), further comprising a second insulating layer (28) on the etch stop layer and over the conductive layer (see Fig. 2).

Regarding claims 33 and 39, Dennison et al. discloses in Fig. 2A a structure (10), further comprising a second conductive material (40) in the contact region (see Fig. 2A).

Regarding claim 34, Dennison et al. discloses in Fig. 2 a structure, comprising the step of:

- a first electrically conductive material (24) formed in and/or on a surface of a substrate;
- a contact opening (the area of 34) in a region adjacent to a second electrically conductive material (the area of 40 in Fig. 2A) formed on the substrate;
- an electrically insulative spacer (18) in the contact opening adjacent to the second electrically conductive material (see Fig. 2);
- an etch stop material (20) over the electrically insulative spacer and the first and second electrically conductive materials (see Fig. 2);
- a blanket layer (28) over the etch stop material; and
- an opening through a first part of the etch stop material to the first electrically conductive material (see Fig. 2).

Dennison et al. does not disclose the etch stop material being a different material from the insulating spacer. However, Figura et al. discloses in Fig. 1 an etch stop material (column 4, lines 51 and 52) being a different material from the insulating spacer (column 4, lines 11 and 12). Thus, it would have been obvious to one of ordinary skill in the art at the time when the

invention was made to modify Dennison et al. by using different materials for the etch stop material and the insulating spacer as taught by Figura et al. The ordinary artisan would have been motivated to modify Dennison et al. in the manner described above for at least the purpose of minimizing current leakage and short circuits (column 2, lines 36 ~ 38).

Regarding claim 35, Dennison et al. discloses in Fig. 2 the electrically insulative spacer (18) having a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface (see Fig. 2).

4. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dennison et al. and Figura et al. as applied to claim 27 above, and further in view of Gonzalez.

Dennison et al. and Figura et al. disclose the claimed invention except the etch stop material being silicon dioxide. However, Gonzalez discloses an etch stop material being silicon dioxide (31 in Fig. 18). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Dennison et al. by using silicon dioxide for the etch stop material as taught by Gonzalez. The ordinary artisan would have been motivated to further modify Dennison et al. in the manner described above for at least the purpose of preventing diffusion of element between layers.

Response to Arguments

5. Applicant's arguments filed on March 11, 2003 have been fully considered but they are not persuasive.

On page 3, applicant argues "the spacers and caps of Dennison et al. are required to act as an etch-stop material; the only etch-stop material described in any of the references is silicon nitride ... If one were to substitute silicon oxide for the caps and spacers in Dennison et al., then they would not act as an etch-stop material with respect to the overlying BPSG layer, and therefore such a substitution would destroy their function." This argument is not persuasive. Yang, cited herein for evidence purpose, clearly discloses in Fig. 5 and column 6, lines 9 ~ 11 the silicon oxide layer in Figura et al. does in fact act as an etch-stop material. Thus, the substitution does not destroy the function of the spacers in Dennison et al. Further, since examiner replaced the material of the caps (20) of Dennison et al. with silicon nitride which is an etch-stop material, the substitution does not destroy the functions of the caps in Dennison et al. Thus, changing the composition of the caps and spacers in Dennison et al. does not defeat their function.

Further, applicant argues "there is no suggestion to replace the barrier layer 20 of Dennison et al. with a different material--nothing else is suggested in any of the references which would provide a barrier function other than silicon nitride." This argument is not persuasive. As explained in the paragraph three of this Office action, since examiner replaced the material of the barrier layer 20 of Dennison et al. with silicon nitride of Figura et al. as same material as the barrier layer 20 of Dennison et al., the substitution would not destroy the barrier functions of the layer 20. Therefore, the combining the references does not defeat the purpose of Dennison et al.

For the above reasons, the rejection is maintained.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
May 14, 2003

ALLAN R. WILSON
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 09/540,610	Applicant(s)/Patent Under Reexamination NULTY ET AL.	
	Examiner Chris C. Chu	Art Unit 2815	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5306657 - A	04-1994	Yang	438/278
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
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	K	US-			
	L	US-			
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FOREIGN PATENT DOCUMENTS

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	N					
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NON-PATENT DOCUMENTS

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Sonnenschein
SONNENSCHEIN NATH & ROSENTHAL LLP

8000 Sears Tower
Chicago, IL 60606
312.876.8000
312.876.7934 fax
www.sonnenschein.com

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CLIENT / MATTER•	09799940-0011
FROM•	Paul E. Rauch

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Paul E. Rauch, Ph.D.
Name of Applicant, assignee or Registered Representative

Signature

Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
James E. Nulty, et al.	)	
Serial No. 09/540,610	)	Examiner Chris C. Chu
Filing Date: March 31, 2000	)	Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning	)	

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- ☒ Two Month Extension of Time (in duplicate)
- ☒ Notice of Appeal (in duplicate)
- ☒ Amendment and Request for Reconsideration
- ☒ No additional fee is required.
- ☒ The Commissioner is hereby authorized to charge any fees associated with this communication not covered by check or credit card payment or credit any overpayment to Deposit Account No. 19-3140. A duplicate copy of this sheet is attached.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591

SONNENSCHEIN NATH & ROSENTHAL LLP
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
(312) 876-8000

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In re Application of:

James E. Nulty, et al.

Serial No. 09/540,610

Filing Date: March 31, 2000

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Examiner Chris C. Chu

Group Art Unit No. 2815

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Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

James E. Nulty, et al.

Serial No. 09/540,610 — Examiner Chris C. Chu

Filing Date: March 31, 2000 — Group Art Unit No. 2815

For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning

PETITION AND FEE FOR EXTENSION OF TIME (37 CFR § 1.136(a))

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Dear Sir:

This is a petition for an extension of the time to respond to the Office Action dated May 20, 2003 for a period of two months.

Please charge the $420.00 fee to American Express Account No. 3785-716974-01002. A Credit Card Payment Form is attached. A duplicate copy of this Petition is attached.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicant

SONNENSCHEIN NATH & ROSENTHAL LLP
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
James E. Nulty, et al.	
Serial No. 09/540,610	Examiner Chris C. Chu
Filing Date: March 31, 2000	Group Art Unit No. 2815
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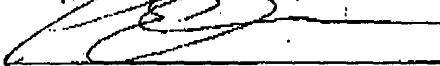

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicant

SONNENSCHEIN NATH & ROSENTHAL LLP
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#19 10-29/03

In re Application of:

James E. Nulty, et al.

Serial No. 09/540,610 — Examiner Chris C. Chu

Filing Date: March 31, 2000 — Group Art Unit No. 2815

For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning

NOTICE OF APPEAL

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P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant hereby appeals to the Board of Patent Appeals and Interferences from the decision of the Examiner dated May 20, 2003, finally rejecting Claims 25-39. Pursuant to 37 C.F.R. § 1.17(b), the fee for this Notice of Appeal is $330.00. PTO Form 2038 is enclosed to cover the required fees.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-3140. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicants

SONNENSCHEIN NATH & ROSENTHAL
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
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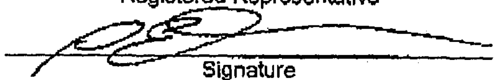
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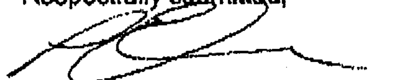
The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-3140. A duplicate copy of this sheet is enclosed.

Respectfully submitted,



Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicants

SONNENSCHEIN NATH & ROSENTHAL
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606

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CLIENT / MATTER• 09799940-0011
FROM• Paul E. Rauch
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Re U.S. Application Serial No. 09/540,610

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312.876.8000
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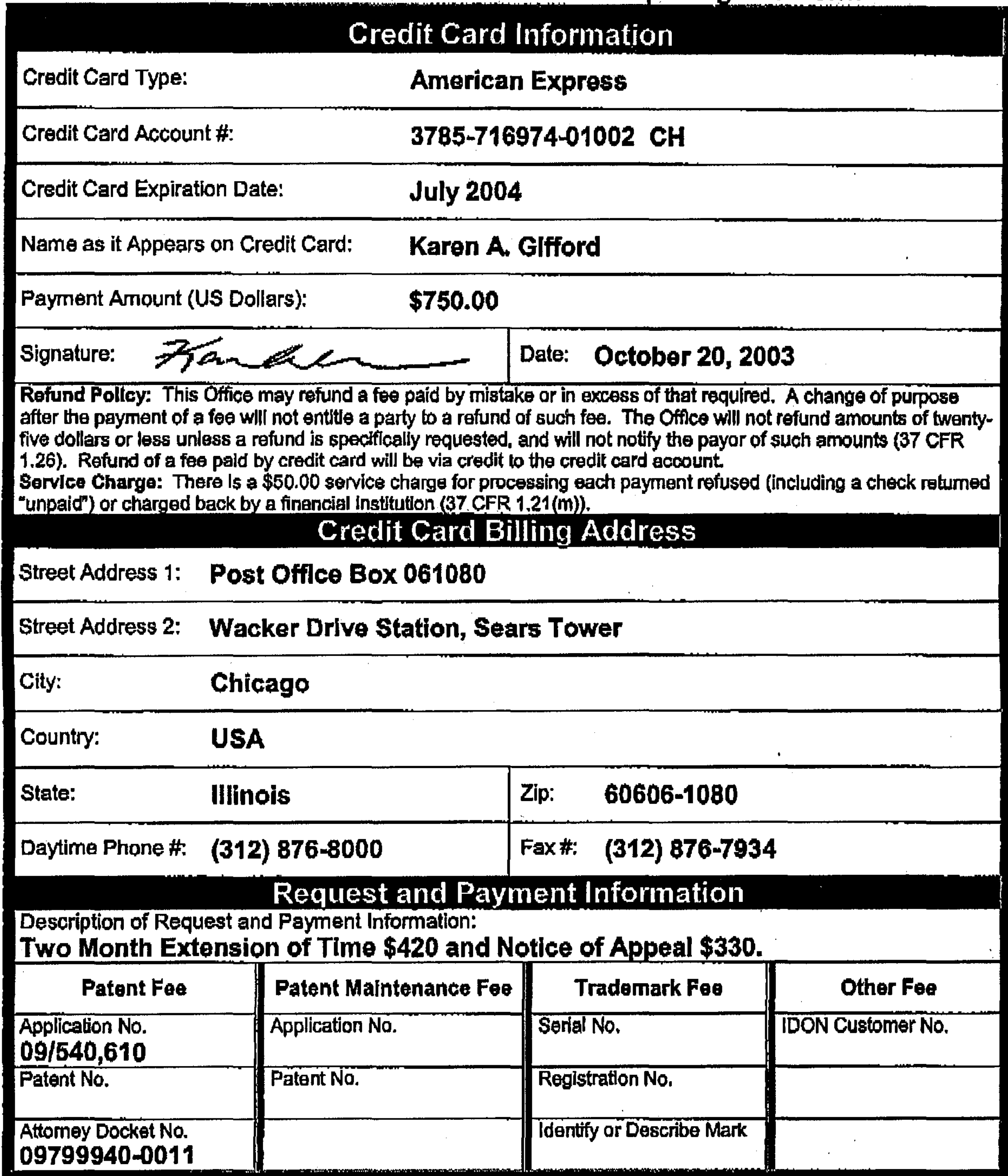

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Patent No.	Patent No.	Registration No.	
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Name of Applicant, assignee or Registered Representative

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Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
James E. Nulty, et al.	
Serial No. 09/540,610	Examiner Chris C. Chu
Filing Date: March 31, 2000	Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning	

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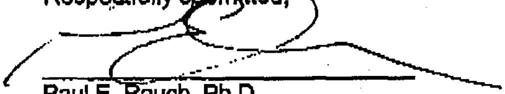

Paul E. Rauch, Ph.D.
Registration No. 38,591

SONNENSCHEIN NATH & ROSENTHAL LLP
P. O. BOX 061080
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In re Application of:

James E. Nulty, et al.

Serial No. 09/540,610

Filing Date: March 31, 2000

For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning

Examiner Chris C. Chu

Group Art Unit No. 2815

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WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
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PAGE 7/17 * RCVD AT 2/6/2004 12:40:08 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/1 * DNIS:7463865 * CSID: * DURATION (mm-ss):03-36

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Serial No. 09/540,610	)	Examiner Chris C. Chu
Filing Date: March 31, 2000	)	Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning	)	

PETITION AND FEE FOR EXTENSION OF TIME (37 CFR § 1.136(a))

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Dear Sir:

This is a petition for an extension of the time to respond to the Office Action dated May 20, 2003 for a period of two months.

Please charge the $420.00 fee to American Express Account No. 3785-716974-01002. A Credit Card Payment Form is attached. A duplicate copy of this Petition is attached.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicant

SONNENSCHEIN NATH & ROSENTHAL LLP
P. O. BOX 061080
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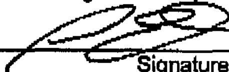
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In re Application of:

James E. Nulty, et al.

Serial No. 09/540,610

Filing Date: March 31, 2000

For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning

Examiner Chris C. Chu

Group Art Unit No. 2815

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In re Application of:	
James E. Nulty, et al.	
Serial No. 09/540,610	Examiner Chris C. Chu
Filing Date: March 31, 2000	Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning	

NOTICE OF APPEAL

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P.O. Box 1450
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Examiner Chris C. Chu

Group Art Unit No. 2815

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Filing Date: March 31, 2000	)	Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning	)	

AMENDMENT AND REQUEST FOR RECONSIDERATION

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Dear Sir:

Responsive to the Official Action of May 5, 2003 Applicants respectfully request reconsideration in light of the following amendments and remarks.

IN THE CLAIMS

25. (Previously presented) The semiconductor apparatus of claim 27 wherein said etch stop material comprises silicon nitride.

26. (Previously presented) The semiconductor apparatus of claim 27 wherein said etch stop material comprises silicon dioxide.

27. (Currently Amended) A structure, comprising:

(a) a conductive layer disposed over a substrate;

(b) a first insulating layer on the conductive layer;

(c) a contact region in said first insulating layer;

(d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and

(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,

wherein the insulating spacer has a substantially rectangular profile in the contact region. wherein the insulating spacer has an angle relative to the substrate surface of more than 85°

28. (Cancelled)

29. (Previously presented) The structure of Claim 27, wherein the insulating spacer has a surface portion in the contact region without overlying etch stop material.

30. (Previously presented) The structure of Claim 29, wherein the insulating spacer surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said substrate.

31. (Cancelled) .

32. (Previously presented) The structure of Claim 27, further comprising a second insulating layer on the etch stop layer and over the conductive layer.

PAGE 13/17 * RCVD AT 2/6/2004 12:40:08 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/1 * DNIS:7463865 * CSID: * DURATION (mm-ss):03-36

SAMSUNG-1002.216

33. (Previously presented) The structure of Claim 32, further comprising a second conductive material in the contact region.

34. (Currently amended) A structure, comprising:

(a) a first electrically conductive material formed in and/or on a surface of a substrate;

(b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate;

(c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material;

(d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer;

(e) a blanket layer over the etch stop material; and

(f) an opening through a first part of the etch stop material to the first electrically conductive material,

wherein the electrically insulative spacer has a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular to the substrate surface.

35. (Cancelled).

36. (Currently amended) The structure of Claim 34, wherein the electrically insulatingve spacer has a surface portion without overlying etch stop material.

37. (Currently amended) The structure of Claim 36, wherein the electrically insulatingve spacer surface portion without overlying etch stop material comprises a surface portion most distant from the substrate.

38. (Previously presented) The structure of Claim 34, further comprising a second insulating layer on the etch stop layer and over the conductive layer.

39. (Previously presented) The structure of Claim 38, further comprising a second conductive material in the contact region.

PAGE 14/17 * RCVD AT 2/6/2004 12:40:08 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/1 * DNIS:7463865 * CSID: * DURATION (mm-ss):03-36

SAMSUNG-1002.217

REMARKS

Claims 27 and 34 have been amended by incorporating the claims 28 and 35, respectively. Claims 36 and 37 have been amended to correct a typographical error. No new matter has been added.

Applicants respectfully requests entry of this amendment, since no new limitations have been presented.

The present invention relates to a semiconductor device with well defined contact openings. In the past, the practice with respect to forming contact openings during the fabrication of semiconductor devices, particularly self-aligned contact openings, was to use etchants with high selectivity to protect underlying regions. However, the properties of a highly selective etch of the overlying etch layer can transform a substantially rectangular spacer adjacent to the contact region into a sloped spacer. Before the conductor materials are added to the contact opening, the opening was cleaned with a sputter etchant which can erode a portion of the sloped insulating spacer. Thus in conventional self-aligned contact structures, the diagonal thickness of the spacer, rather than the vertical thickness of the insulating layer, determined the minimum insulating layer thickness for the gate. Sloping spacers limit the number of structures that can be included on a device.

The present invention avoids this problem by retaining the substantially rectangular profile of the insulating spacers. As illustrated in Figure 4K of the present specification, the spacer retains a substantially rectangular or "boxy" profile, i.e. the sides of the spacer are not sloping.

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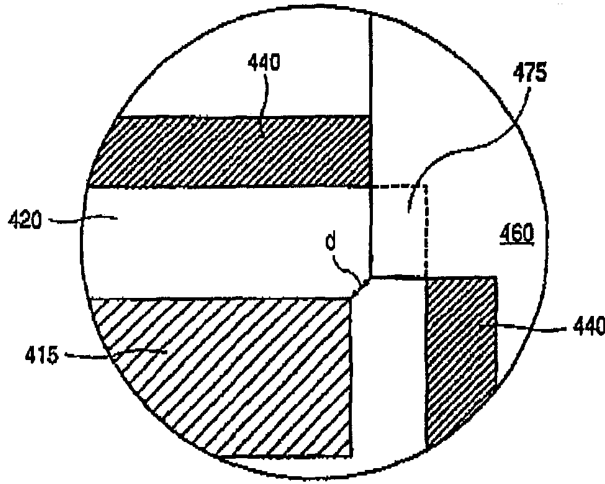
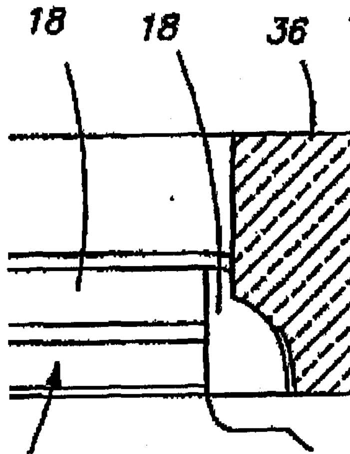


Figure 4K

The rejection of the claims under 35 U.S.C. § 103 over Dennison, et al., in view of Figura, et al., and optionally further in view of Gonzalez, is respectfully traversed. Dennison, et al. does not show a substantially rectangular insulating spacer.

Dennison, et al. describes a method of forming a bit line over a capacitor array of memory cells. Element 18 in Figure 2 shows a spacer. This portion of the figure is reproduced below. As illustrated, the spacer has a sloping portion, and is not substantially rectangular.



A portion of Figure 2 from Dennison, et al.

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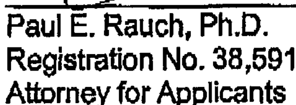
SAMSUNG-1002.219

Figura et al. has been cited for an etch stop material being different from the insulating spacer. Gonzalez has only been cited for a description of silicon dioxide spacers. Neither reference describes a substantially rectangular insulating spacer.

The present invention, as claimed, includes a substantially rectangular insulating spacer. As used in the present specification, this means that the spacer does not have sloping sides, and retains a "boxy" profile; this is illustrated in Figure 4K, shown above. In contrast, the spacers of Dennison, et al. has sloping sides, and is therefore not substantially rectangular, as shown in Figure 2 of this reference, also shown above. Figura et al. and Gonzalez also fail to show or suggest a substantially rectangular insulating spacer. Applicants respectfully submit that the claimed invention is not obvious over the applied references. Withdrawal of this ground of rejection is respectfully requested.

Applicants respectfully request that the Examiner contact the undersigned upon the indication of any allowable subject matter. Applicants submit the application is now in condition for allowance. Early notice of such action is earnestly solicited.

Respectfully submitted,



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PAGE 17/17 * RCVD AT 2/6/2004 12:40:08 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/1 * DNIS:7463865 * CSID: * DURATION (mm-ss):03-36

SAMSUNG-1002.220

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SONNENSCHEIN NATH & ROSENTHAL LLP

8000 Sears Tower
Chicago, IL 60606
312.876.8000
312.876.7934 fax
www.sonnenschein.com

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Facsimile Transmittal Sheet

DATE: February 20, 2004

PLEASE DELIVER THE FOLLOWING PAGES TO:

NAME: Examiner Chris C. Chu
FIRM: USPTO, Group Art Unit 2815
PHONE: 571-272-1724
FAX: 571-273-1724
CLIENT / MATTER: 09799940-0011
FROM: Paul E. Rauch
TOTAL NUMBER OF PAGES TRANSMITTED, INCLUDING THIS SHEET: 11

MESSAGE:

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Please deliver to Examiner Chris C. Chu
Group Art Unit 2815
Serial No. 09/540,610

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Feb. 20, 2004
Date of Facsimile

Paul E. Rauch, Ph.D.
Name of Applicant, assignee or Registered Representative

Signature

Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

James E. Nulty, et al.

Serial No. 09/540,610

Filing Date: March 31, 2000

For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning

Examiner Chris C. Chu

Group Art Unit No. 2815

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TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is:

- ☒ Two Month Extension of Time (in duplicate)
- ☒ Amendment
- ☒ The Commissioner is hereby authorized to charge any fees associated with this communication to Deposit Account No. 19-3140. A duplicate copy of this sheet is attached.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
SONNENSCHEIN NATH & ROSENTHAL LLP
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
(312) 876-8000

PAGE 2/11 * RCVD AT 2/20/2004 2:17:01 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/24 * DNIS:2731724 * CSID: * DURATION (mm-ss):02-02

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Feb. 20, 2004
Date of Facsimile

Paul E. Rauch, Ph.D.
Name of Applicant, assignee or Registered Representative

Signature

Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
James E. Nulty, et al.)
Serial No. 09/540,610) Examiner Chris C. Chu
Filing Date: March 31, 2000) Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning)

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

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- ☒ Two Month Extension of Time (in duplicate)
- ☒ Amendment
- ☒ The Commissioner is hereby authorized to charge any fees associated with this communication to Deposit Account No. 19-3140. A duplicate copy of this sheet is attached.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591

SONNENSCHEIN NATH & ROSENTHAL LLP
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
(312) 876-8000

This file wrapper was thoroughly reviewed by our technical staff. Fax pages 4, 8, 9 and 10 are missing from the original USPTO file history.

This has been brought to your attention so that you will know it has not been overlooked.

#20/ex
4/6/4
[handwritten initials]

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Date of Facsimile

Paul E. Rauch, Ph.D.
Name of Applicant, assignee or Registered Representative

[signature]
Signature

Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
James E. Nulty, et al.	)	
Serial No. 09/540,610	)	Examiner Chris C. Chu
Filing Date: March 31, 2000	)	Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning	)	

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PETITION AND FEE FOR EXTENSION OF TIME (37 CFR § 1.136(a))

Mail Stop - AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is a petition for a two month extension of time for the filing of an Appeal Brief.

The Commissioner is hereby authorized to charge any fees associated with this communication to Deposit Account No. 19-3140. A duplicate copy of this sheet is attached.

Respectfully submitted,

[signature]

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicant

SONNENSCHEIN NATH & ROSENTHAL LLP
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
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PAGE 5/11 * RCVD AT 2/20/2004 2:17:01 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/24 * DNIS:2731724 * CSID: * DURATION (mm-ss):02-02

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Paul E. Rauch, Ph.D.
Name of Applicant, assignee or Registered Representative

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Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

James E. Nulty, et al.

Serial No. 09/540,610

Filing Date: March 31, 2000

For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning

Examiner Chris C. Chu

Group Art Unit No. 2815

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AMENDMENT

Mail Stop - AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants respectfully request reconsideration in light of the following amendments and remarks.

IN THE SPECIFICATION

Please add the following paragraph to the specification, page 15, after line 16:

D1

The phrase "substantially rectangular" means that a side of the spacer has an angle relative to the substrate surface of more than 85°.

PAGE 7/11 * RCVD AT 2/20/2004 2:17:01 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/24 * DNIS:2731724 * CSID: * DURATION (mm-ss):02-02

SAMSUNG-1002.227

IN THE CLAIMS

1-24. (Cancelled)

2 25. (Previously presented) The semiconductor apparatus of claim 1 27 wherein said etch stop material comprises silicon nitride.

3 26. (Previously presented) The semiconductor apparatus of claim 1 27 wherein said etch stop material comprises silicon dioxide.

1 27. (Currently Amended) A structure, comprising:

(a) a conductive layer disposed over a substrate;

(b) a first insulating layer on the conductive layer;

(c) a contact region in said first insulating layer;

(d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and

(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,

wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85° ~~a substantially rectangular profile in the contact region~~.

28. (Cancelled).

4 29. (Previously presented) The structure of Claim 1 27, wherein the insulating spacer has a surface portion in the contact region without overlying etch stop material.

5 30. (Previously presented) The structure of Claim 4 29, wherein the insulating spacer surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said substrate.

31. (Cancelled).

PAGE 4/7 * RCVD AT 3/31/2004 1:34:54 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/25 * DNIS:2731724 * CSID: * DURATION (mm-ss):01-36

SAMSUNG-1002.228

6
~~32.~~ (Previously presented) The structure of Claim ~~27,~~ 1 further comprising a second insulating layer on the etch stop layer and over the conductive layer.

7
~~33.~~ (Previously presented) The structure of Claim ~~32;~~ 6 further comprising a second conductive material in the contact region.

8
~~34.~~ (Currently amended) A structure, comprising:

(a) a first electrically conductive material formed in and/or on a surface of a substrate;

(b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate;

D2

(c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material;

(d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer;

(e) a blanket layer over the etch stop material; and

(f) an opening through a first part of the etch stop material to the first electrically conductive material,

wherein a side of the electrically insulative spacer has ~~a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular~~ an angle relative to the substrate surface that is either a right angle or an acute angle ~~of more than 85°~~.

35. (Cancelled).

9
~~36.~~ (Previously presented) The structure of Claim ~~34~~ 8, wherein the electrically insulative spacer has a surface portion without overlying etch stop material.

10
~~37.~~ (Previously presented) The structure of Claim ~~36~~ 9, wherein the electrically insulative spacer surface portion without overlying etch stop material comprises a surface portion most distant from the substrate.

PAGE 5/7 * RCVD AT 3/31/2004 1:34:54 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/25 * DNIS:2731724 * CSID: * DURATION (mm-ss):01-36

SAMSUNG-1002.229

11
~~38.~~ (Previously presented) The structure of Claim ~~34~~ 8, further comprising a second insulating layer on the etch stop layer and over the conductive layer.

D2

12
~~39.~~ (Previously presented) The structure of Claim ~~38~~ 11, further comprising a second conductive material in the contact region.

PAGE 6/7 * RCVD AT 3/31/2004 1:34:54 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/25 * DNIS:2731724 * CSID: * DURATION (mm-ss):01-36

SAMSUNG-1002.230

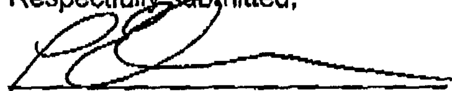
REMARKS

The amendment to claims 27 and 34, and the specification, are supported by the specification, page 8, lines 19-23, and page 10, lines 8-11. No new matter has been added.

Applicants would like to thank Examiner Chu for the courteous and helpful discussion held with applicants representative on February 19, 2004. During that discussion, it was indicated that the above amendments would clarify the claims.

Applicants submit that the application is now in condition for allowance. Early notice of such action is earnestly solicited.

Respectfully submitted,



Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicants

SONNENSCHEIN NATH & ROSENTHAL
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
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SONNENSCHEIN NATH & ROSENTHAL LLP

8000 Sears Tower
Chicago, IL 60606
312.876.8000
312.876.7934 fax
www.sonnenschein.com

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FAX•	571-273-1724
CLIENT / MATTER•	09799940-0011
FROM•	Paul E. Rauch

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MESSAGE •

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Group Art Unit 2815
Serial No. 09/540,610

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March 31, 2004
Date of Facsimile

Paul E. Rauch, Ph.D.
Name of Applicant, assignee or Registered Representative

/Reg. No. 43,853
Signature

Our File No. 09799940-0011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
James E. Nulty, et al.	
Serial No. 09/540,610	Examiner Chris C. Chu
Filing Date: March 31, 2000	Group Art Unit No. 2815
For Method for Eliminating Lateral Spacer Erosion on Enclosed Contact Topographies During RF Sputter Cleaning	

CORRECTED AMENDMENT

Mail Stop - AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Amendment is identical to the last amendment filed but it corrects the format of the presented claim set. Applicants thank Examiner Chu for pointing out this omission.

IN THE SPECIFICATION

Please add the following paragraph to the specification, page 15, after line 16:

The phrase "substantially rectangular" means that a side of the spacer has an angle relative to the substrate surface of more than 85°.

PAGE 3/7 * RCVD AT 3/31/2004 1:34:54 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/25 * DNIS:2731724 * CSID: * DURATION (mm-ss):01-36

SAMSUNG-1002.234

IN THE CLAIMS

1-24. (Cancelled)

25. (Previously presented) The semiconductor apparatus of claim 27 wherein said etch stop material comprises silicon nitride.

26. (Previously presented) The semiconductor apparatus of claim 27 wherein said etch stop material comprises silicon dioxide.

27. (Currently Amended) A structure, comprising:

(a) a conductive layer disposed over a substrate;

(b) a first insulating layer on the conductive layer;

(c) a contact region in said first insulating layer;

(d) at least one insulating spacer in the contact region adjacent to the first insulating layer; and

(e) an etch stop material over said first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer,

wherein a side of the insulating spacer has an angle relative to the substrate surface of more than 85° ~~a substantially rectangular profile in the contact region~~.

28. (Cancelled).

29. (Previously presented) The structure of Claim 27, wherein the insulating spacer has a surface portion in the contact region without overlying etch stop material.

30. (Previously presented) The structure of Claim 29, wherein the insulating spacer surface portion without overlying etch stop material comprises an insulating spacer surface portion most distant from said substrate.

31. (Cancelled).

PAGE 4/7 * RCVD AT 3/31/2004 1:34:54 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/25 * DNIS:2731724 * CSID: * DURATION (mm-ss):01-36

32. (Previously presented) The structure of Claim 27, further comprising a second insulating layer on the etch stop layer and over the conductive layer.

33. (Previously presented) The structure of Claim 32, further comprising a second conductive material in the contact region.

34. (Currently amended) A structure, comprising:

(a) a first electrically conductive material formed in and/or on a surface of a substrate;

(b) a contact opening in a region adjacent to a second electrically conductive material formed on the substrate;

(c) an electrically insulative spacer in the contact opening adjacent to the second electrically conductive material;

(d) an etch stop material over the electrically insulative spacer and the first and second electrically conductive materials, the etch stop material being a different material from the insulative spacer;

(e) a blanket layer over the etch stop material; and

(f) an opening through a first part of the etch stop material to the first electrically conductive material,

wherein a side of the electrically insulative spacer has ~~a substantially rectangular cross-sectional shape in a plane that is substantially perpendicular~~ an angle relative to the substrate surface of more than 85°.

35. (Cancelled).

36. (Previously presented) The structure of Claim 34, wherein the electrically insulative spacer has a surface portion without overlying etch stop material.

37. (Previously presented) The structure of Claim 36, wherein the electrically insulative spacer surface portion without overlying etch stop material comprises a surface portion most distant from the substrate.

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SAMSUNG-1002.236

38. (Previously presented) The structure of Claim 34, further comprising a second insulating layer on the etch stop layer and over the conductive layer.

39. (Previously presented) The structure of Claim 38, further comprising a second conductive material in the contact region.

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SAMSUNG-1002.237

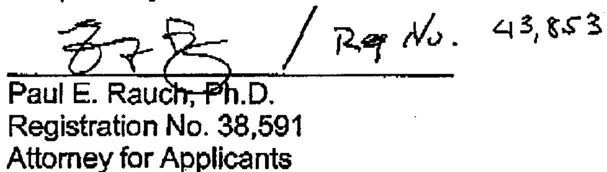
REMARKS

The amendment to claims 27 and 34, and the specification, are supported by the specification, page 8, lines 19-23, and page 10, lines 8-11. No new matter has been added.

Applicants would like to thank Examiner Chu for the courteous and helpful discussion held with applicants representative on February 19, 2004. During that discussion, it was indicated that the above amendments would clarify the claims.

Applicants submit that the application is now in condition for allowance. Early notice of such action is earnestly solicited.

Respectfully submitted,



Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicants

SONNENSCHEIN NATH & ROSENTHAL
P. O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606
(312) 876-8000

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SAMSUNG-1002.238

Notice of Allowability	Application No. 09/540,610	Applicant(s) NULTY ET AL.	
	Examiner Chris C. Chu	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 2/20/04.
2. ☒ The allowed claim(s) is/are 25 - 27, 29, 30, 32-34 and 36-39.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☒ to Paper No./Mail Date 4.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 22.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Drawings

1. The proposed drawings mailed on October 4, 2001 are approved by Examiner. However, applicant should submit formal replacement sheets with labeled as such in the header according to 37 CFR 1.121(d) and formal drawings for the figures. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The replacement drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for replacement drawings will not be held in abeyance.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interview with Paul E. Rauch on April 15, 2004.

The application has been amended as follows:

In claim 27, line 11, after "substrate surface," insert: -- that is either a right angle or an acute angle--.

In claim 34, at the last line, after "substrate surface," insert: -- that is either a right angle or an acute angle--.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

4. The prior art of record does not teach or reasonably suggest, either singularly or in combination, at least one insulating spacer in a contact region adjacent to a first insulating layer; an etch stop material over the first insulating layer and adjacent to the insulating spacer, the etch stop material being a different material from the insulating spacer; and wherein a side of the insulating spacer has an angle relative to the substrate surface that is either a right angle or an acute angle of more than 85°.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
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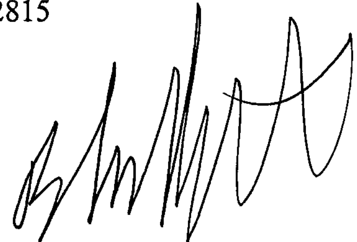

BRADLEY BAUMEISTER
PRIMARY EXAMINER

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26263 7590 04/20/2004

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P.O. BOX 061080
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CHICAGO, IL 60606-1080

EXAMINER	
CHU, CHRIS C	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/20/2004

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,610	03/31/2000	James E. Nulty	16820.P097	2171

TITLE OF INVENTION: STRUCTURE HAVING REDUCED LATERAL SPACER EROSION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$300	$1630	07/20/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

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If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

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If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 11/03) Approved for use through 04/30/2004.

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Complete and send this form, together with applicable fee(s), to: Mail
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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000

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CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

26263 7590 04/20/2004

SONNENSCHEIN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,610	03/31/2000	James E. Nulty	16820.P097	2171

TITLE OF INVENTION: STRUCTURE HAVING REDUCED LATERAL SPACER EROSION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$300	$1630	07/20/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHU, CHRIS C	2815	257-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 ____________
2 ____________
3 ____________

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent); ❑ individual ❑ corporation or other private group entity ❑ government

4a. The following fee(s) are enclosed:

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❑ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number ____________ (enclose an extra copy of this form).

Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) (Date)

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This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,610	03/31/2000	James E. Nulty	16820.P097	2171

26263 7590 04/20/2004

SONNENSCHEIN NATH & ROSENTHAL LLP
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WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

EXAMINER	
CHU, CHRIS C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/20/2004

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (Rev. 11/03) Approved for use through 04/30/2004.

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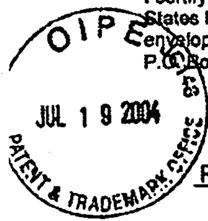

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July 15, 2004
Date of Deposit

Paul E. Rauch, Ph.D., Registration No. 38,591
Name

Signature

Our File No. CYP01-007-DIV-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
James E. Nulty, et al.	)	
Serial No. 09/540,610	)	Examiner Chris C. Chu
Filing Date: March 31, 2000	)	Group Art Unit No. 2815
For Structure Having Reduced Lateral Spacer Erosion	)	

TRANSMITTAL

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Commissioner for Patents
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Alexandria, VA 22313-1450

Dear Sir:

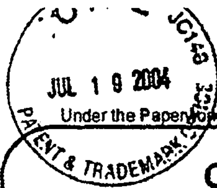
Transmitted herewith is:

- ☒ Credit Card Payment Form
- ☒ Part B Fee Transmittal Form PTOL-85 (in duplicate)
- ☒ Change of Correspondence Address
- ☒ Letter to Official Draftsman
- ☒ 7 Sheets of Formal Drawings (Figures 1-4)
- ☒ No additional fee is required.
- ☒ The Commissioner is hereby authorized to charge any fees associated with this communication not covered by check or credit card payment or credit any overpayment to Deposit Account No. (50-3123). A duplicate copy of this sheet is attached.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591

Evan Law Group LLC
566 West Adams
Suite 350
Chicago, Illinois 60661
(312) 876-1400



PTO/SB/122 (09-03)
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Application

Address to:
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Application Number	09/540,610
Filing Date	March 31, 2000
First Named Inventor	James E. Nulty, et al.
Art Unit	2815
Examiner Name	Chris C. Chu
Attorney Docket Number	CYP01-007-DIV-US

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I am the:

☐ Applicant/Inventor

☐ Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☑ Attorney or Agent of record. Registration Number 38,591

☐ Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number________.

Typed or Printed Name	Paul E. Rauch, Ph.D.
Signature	[signature]
Date	July 15, 2004
Telephone	312-876-1400

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

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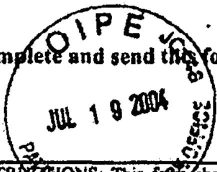

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26263 7590 04/20/2004

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~~P.O. BOX 061080~~
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~~CHICAGO, IL 606~~

Evan Law Group LLC
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Paul E. Rauch, Ph.D., Registration No. 38,591 (Depositor's name)
[signature] (Signature)
July 15, 2004 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,610	03/31/2000	James E. Nulty	16820.P097	2171

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nonprovisional	NO	$1330	$300	$1630	07/20/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHU, CHRIS C	2815	257-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
   - [X] Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
   - [ ] "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
   1. EVAN LAW GROUP LLC
   2.
   3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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(A) NAME OF ASSIGNEE: CYPRESS SEMICONDUCTOR CORPORATION
(B) RESIDENCE: (CITY and STATE OR COUNTRY): SAN JOSE, CALIFORNIA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ individual ☒ corporation or other private group entity ☐ government

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- [X] Publication Fee
- [X] Advance Order - # of Copies 10

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- [X] Payment by credit card. Form PTO-2038 is attached.
- [X] The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-3123 (enclose an extra copy of this form).

Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) [signature] (Date) July 15, 2004

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

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02 FC:1504 300.00 OP
03 FC:8001 30.00 OP

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July 15, 2004
Date of Deposit

Paul E. Rauch, Ph.D., Registration No. 38,591
Name

Signature

#24MC

Our File No. CYP01-007-DIV-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

James E. Nulty, et al.

Serial No. 09/540,610 — Examiner Chris C. Chu

Filing Date: March 31, 2000 — Group Art Unit No. 2815

For Structure Having Reduced Lateral Spacer Erosion

SUBMISSION OF FORMAL DRAWINGS

M.S. Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In response to the Notice of Allowability dated April 20, 2004, Applicants have enclosed 7 sheets of formal drawings (Figures 1-4) including changes required by the Notice of Draftsperson's Patent Drawing Review, PTO-948 attached to Paper No. 4 and 22.

Respectfully submitted,

Paul E. Rauch, Ph.D.
Registration No. 38,591
Attorney for Applicant

Evan Law Group LLC
566 West Adams
Suite 350
Chicago, Illinois 60661
(312) 876-1400

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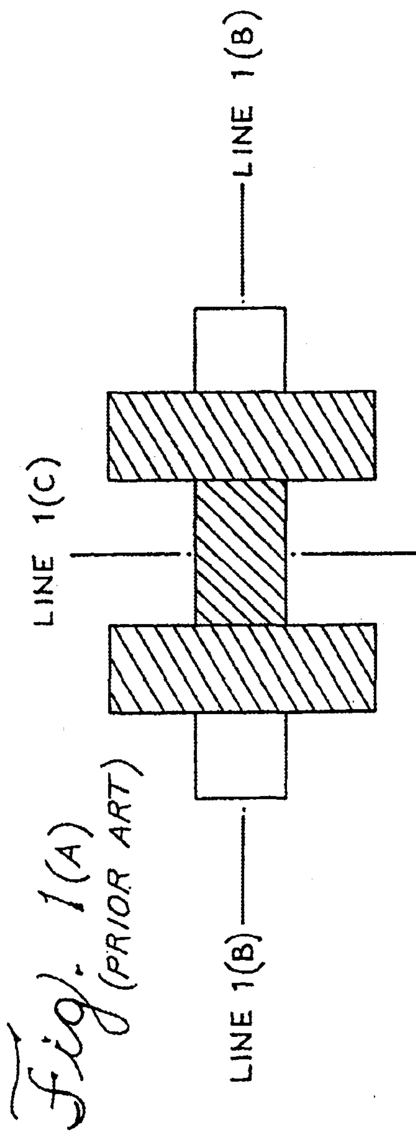

Fig. 1(A) (PRIOR ART)

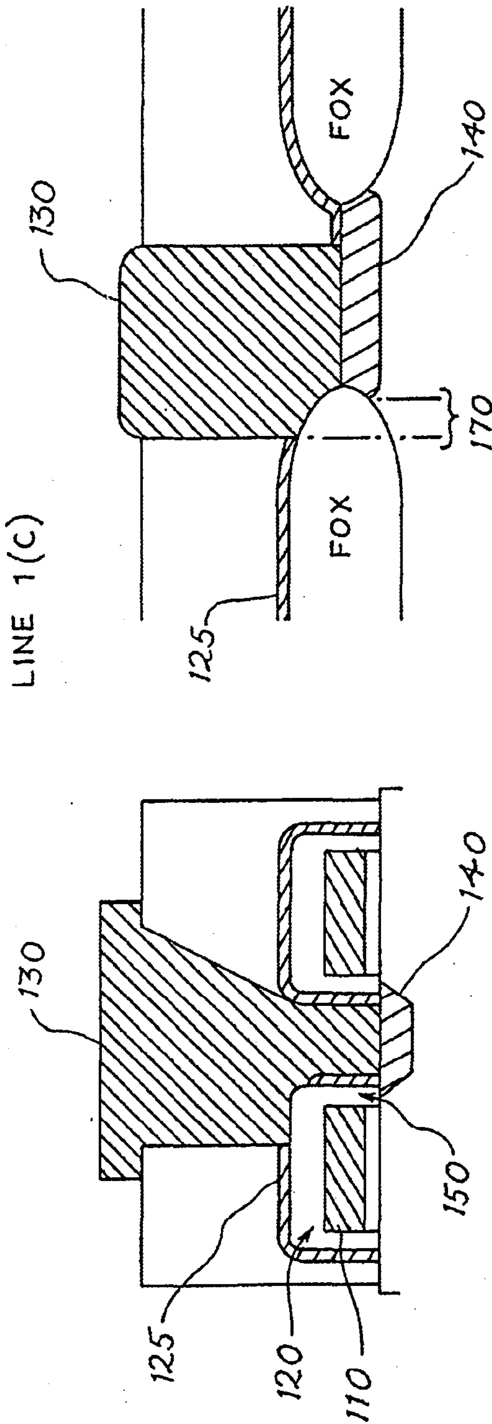

Fig. 1(B) (PRIOR ART)

Fig. 1(C) (PRIOR ART)

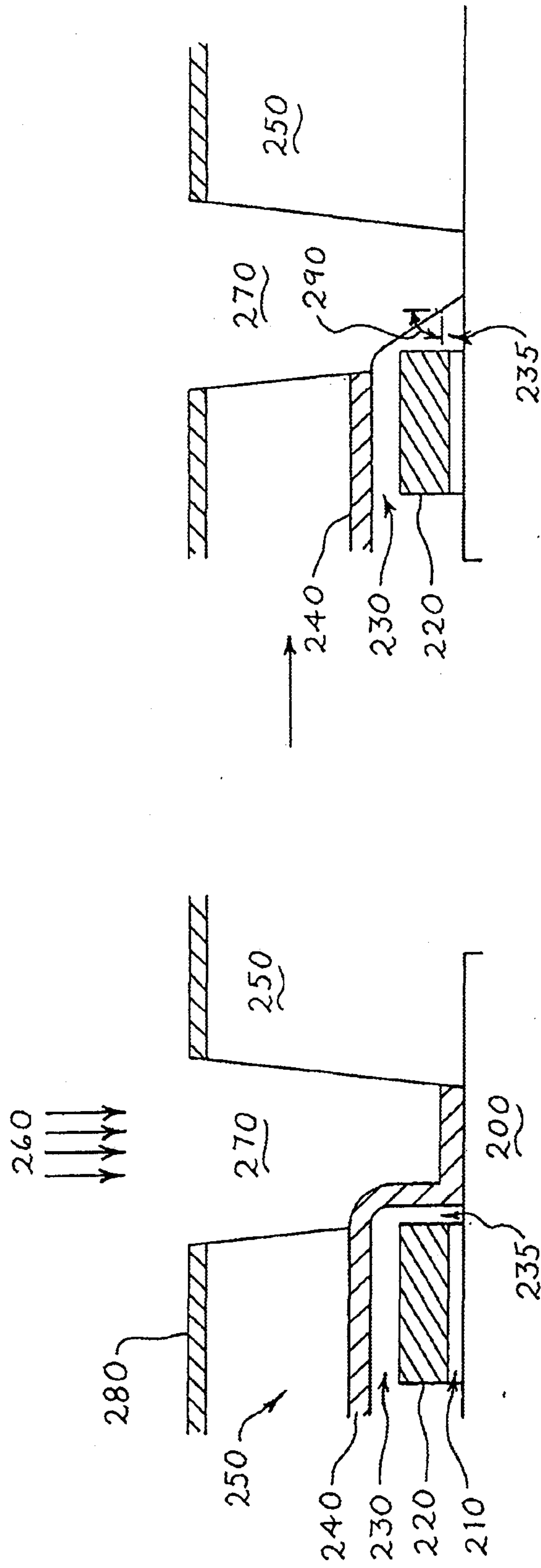

Fig. 2(B) (PRIOR ART)

Fig. 2(A) (PRIOR ART)

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Fig. 3 (PRIOR ART)

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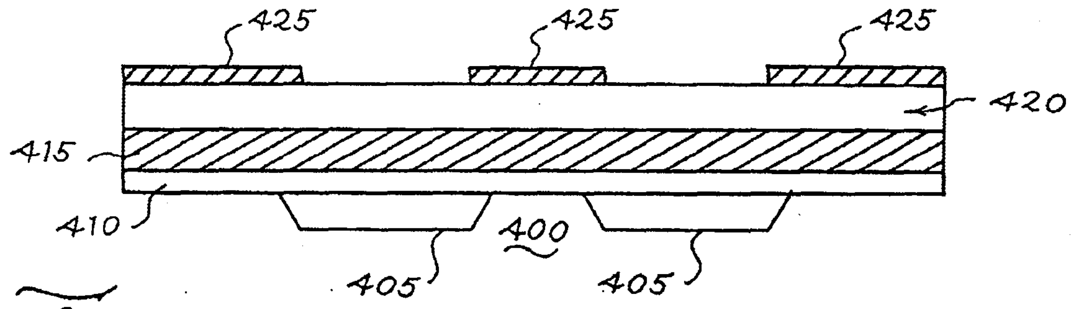


Fig. 4(A)

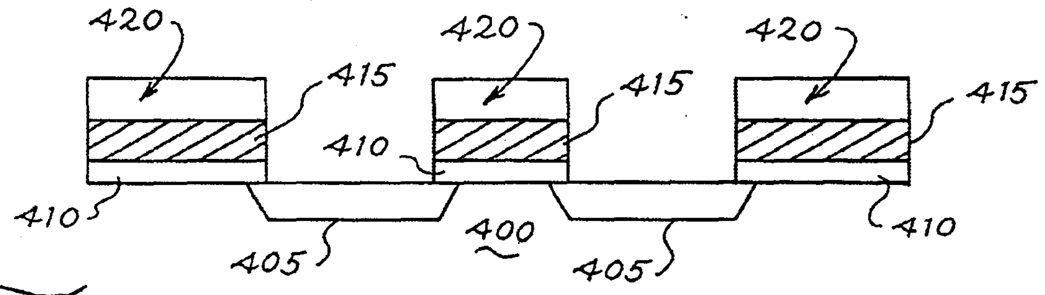


Fig. 4(B)

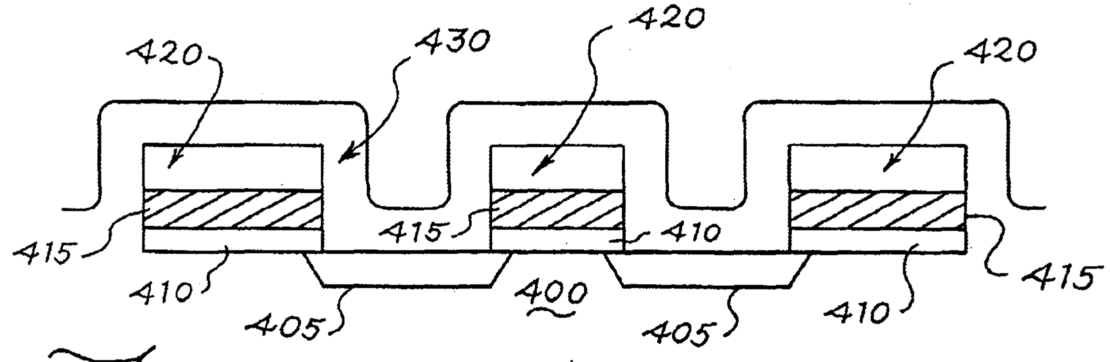


Fig. 4(C)

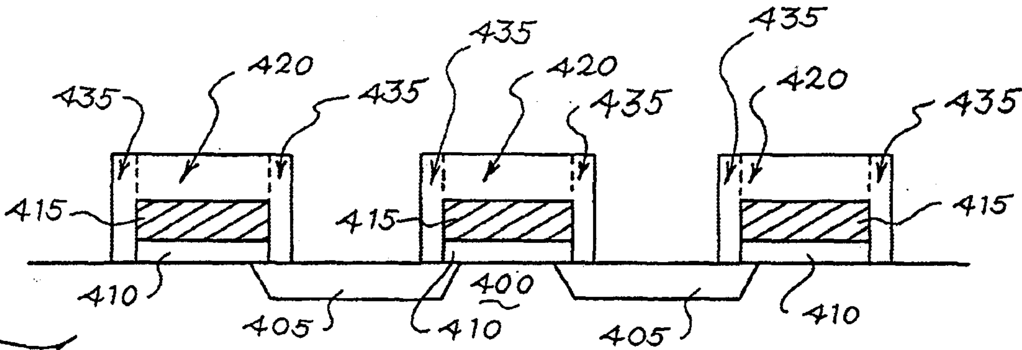


Fig. 4(D)

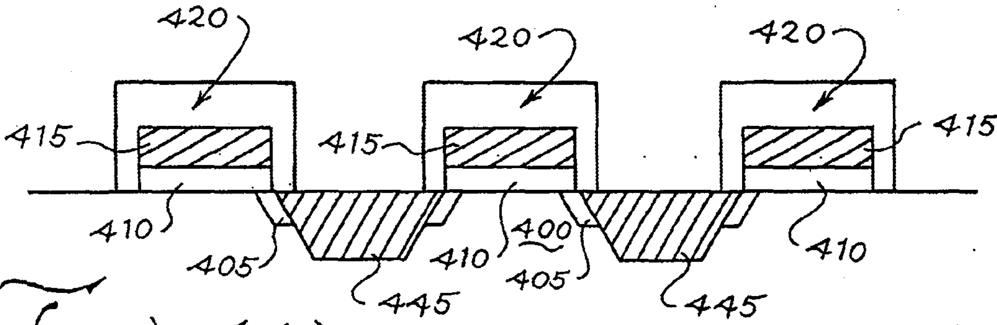


Fig. 4(E)

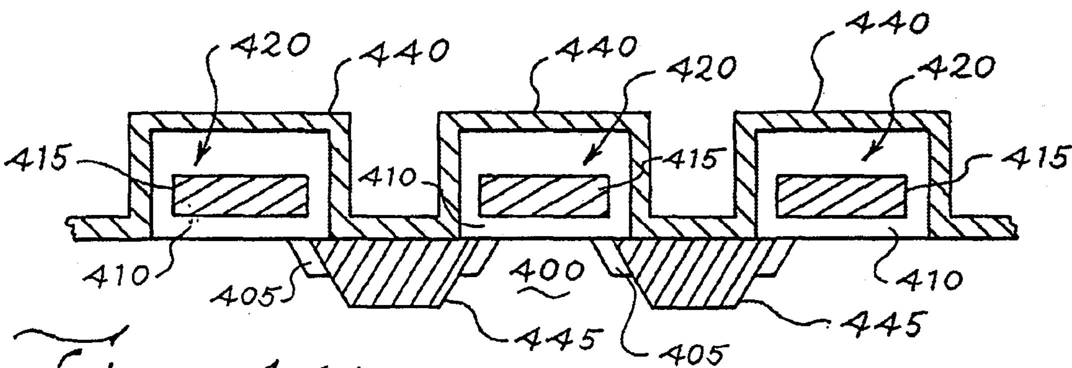
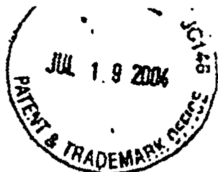


Fig. 4(F)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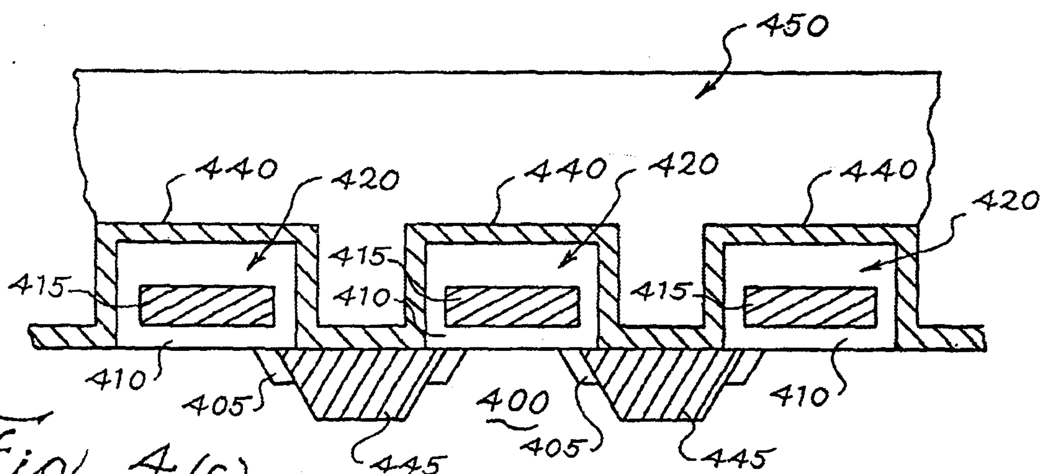
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Fig. 4(G)

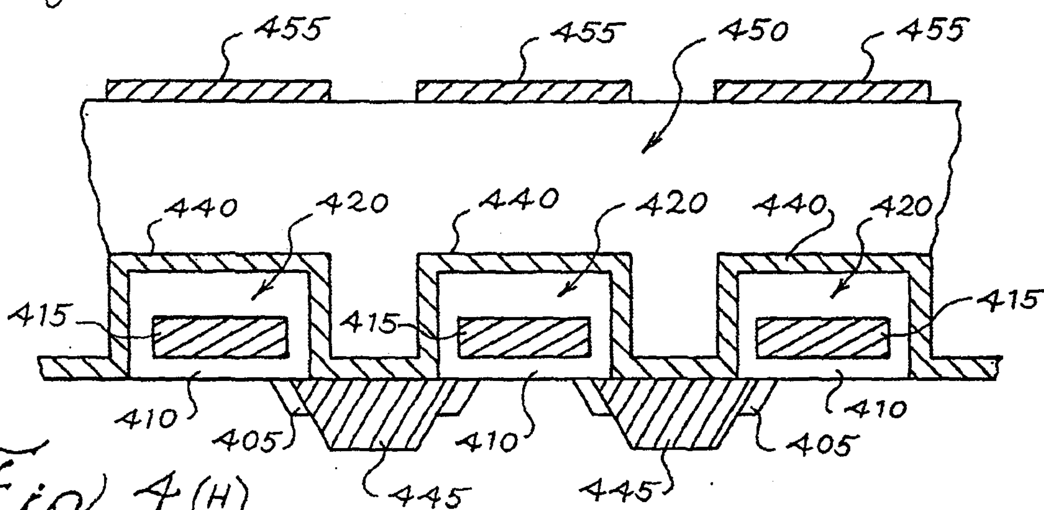
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Fig. 4(H)

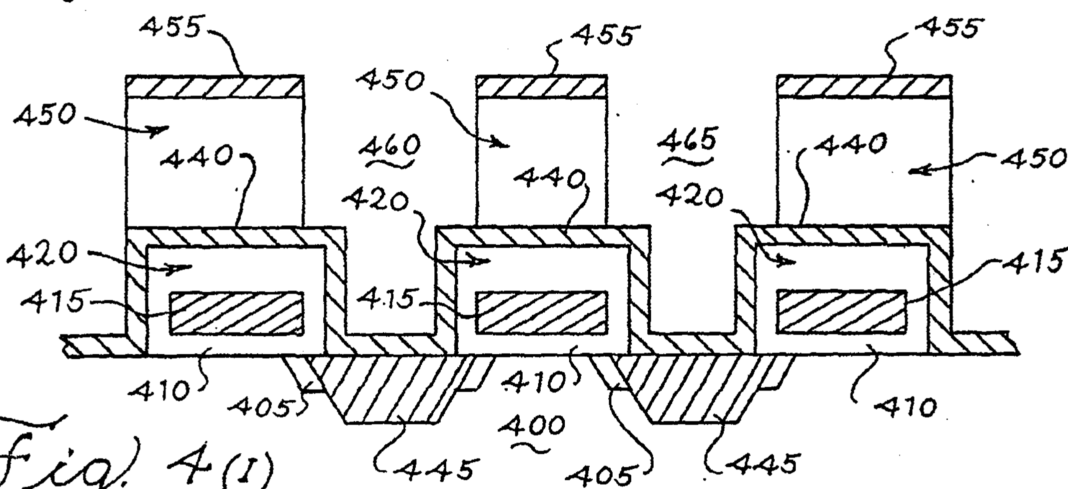
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Fig. 4(I)

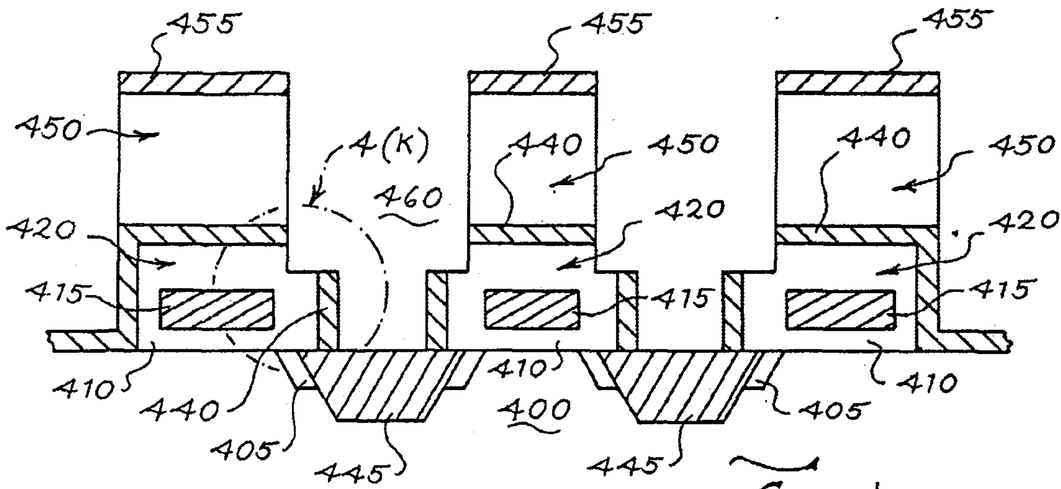

Fig. 4(J)

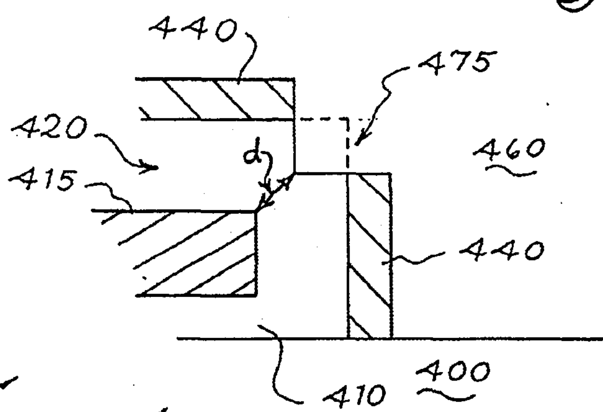

Fig. 4(K)

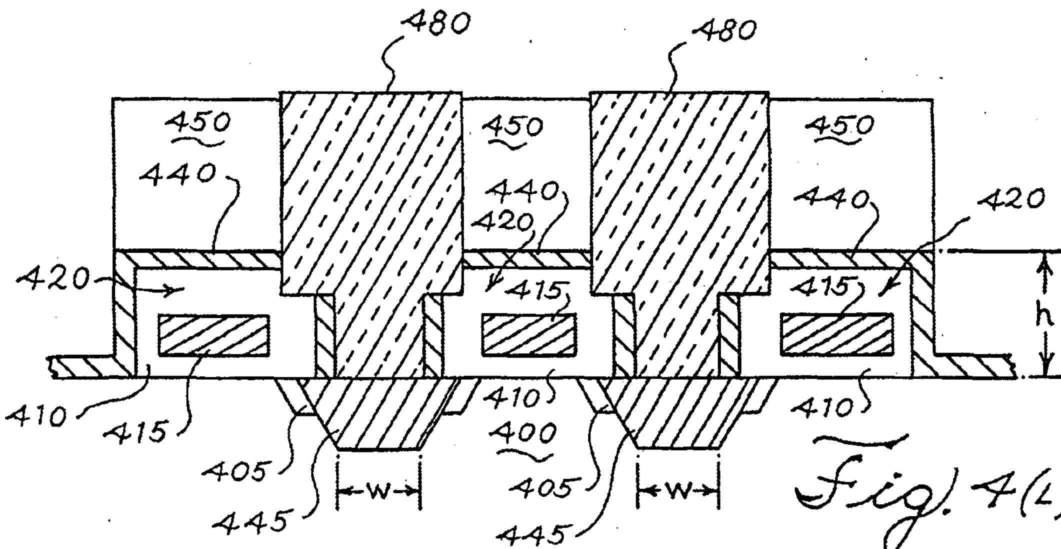

Fig. 4(L)

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PATENT NUMBER	FEE AMT	MAINT. SURCHG	U.S. APPL NUMBER	PATENT ISSUE DATE	APPL. FILING DATE	PAY-MENT YEAR	SMALL ENTITY?	TOTAL PYMT DUE	ATTORNEY DOCKET NUMBER
6784552	930	130	09540610	08/31/04	03/31/00	4	NO	1060	16820.P097

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MF4401 (7/2007)

PATENT APPLICATION FEE DETERMINATION RECORD Effective October 1, 2003	Application or Docket Number 09/540610

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ RATE	FEE	OR	OTHER THAN SMALL ENTITY RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A D

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 12	Minus	** 20	=
Independent	* 2	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
XS 9=		OR	XS18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

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FORM PTO-875 (Rev 10/03) Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ OR OTHER THAN SMALL ENTITY

RATE	FEE	OR	RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

B

SMALL ENTITY OR OTHER THAN SMALL ENTITY

AMENDMENT A

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
	Total	* 15	Minus	** 20	= —
	Independent	* 2	Minus	*** 3	= —
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

C (NE)

AMENDMENT B

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	Total	* 15	Minus	** 20	= —
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RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

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	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
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TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

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PATENT APPLICATION FEE DETERMINATION RECORD Effective December 29, 1999	Application or Docket Number

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)	SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE		RATE	FEE
BASIC FEE				345.00	OR		690.00
TOTAL CLAIMS	13 minus 20=	*	X$ 9=		OR	X$18=	
INDEPENDENT CLAIMS	2 minus 3 =	*	X39=		OR	X78=	
MULTIPLE DEPENDENT CLAIM PRESENT			+130=		OR	+260=	
			TOTAL		OR	TOTAL	690

* If the difference in column 1 is less than zero, enter "0" in column 2

Cancel 1-24

CLAIMS AS AMENDED - PART II

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	Independent	* 2	Minus	***	=	X39=		OR	X78=	
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						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

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	Independent	*	Minus	***	=	X39=		OR	X78=	
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						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
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						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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(Rev. 12/99)
Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
*U.S. GPO: 2000-463-433/29044

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1	BRS	1638	257/774	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
2	BRS	137	257/774 and etch adj stop and (conductive or metal or wiring) and (insulating or dielectric)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
3	BRS	3872	etch adj stop and (conductive or metal or wiring) and (insulating or dielectric)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
4	BRS	3735	etch adj stop and (conductive or metal or wiring) and (insulating or dielectric) not (257/774 and etch adj stop and (conductive or metal or wiring) and (insulating or dielectric))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
5	BRS	996	etch adj stop and (conductive or metal or wiring) and (insulating or dielectric) and spacer not (257/774 and etch adj stop and (conductive or metal or wiring) and (insulating or dielectric))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
6	BRS	25	6146997.pn. or 6165880.pn. or 6172411.pn. or 6097090.pn. or 5879986.pn. or 5292677.pn. or 5538922.pn. or 5362666.pn. or 5338700.pn. or 5275972.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB

	Type	Hits	Search Text	DBs
1	BRS	53	(257/775 or 257/776)and etch adj stop and (conductive or metal or wiring) and (insulating or dielectric)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
2	BRS	0	(257/775 or 257/776)and etch adj stop and (conductive or metal or wiring) and (insulating or dielectric)	JPO
3	BRS	9	etch adj stop and (conductive or metal or wiring) and (insulating or dielectric)	JPO
4	BRS	40	(257/775 or 257/776)and etch adj stop and silicon adj dioxide	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
5	BRS	6	(257/775 or 257/776)and etch adj stop and silicon adj dioxide and multi adj layer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
6	BRS	0	(257/775 or 257/776)and ((etch adj stop) near (silicon adj dioxide)) and multi adj layer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB

	Type	Hits	Search Text	DBs
7	BRS	1	(257/775 or 257/776)and ((etch adj stop) near (silicon adj dioxide))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
8	BRS	1	257/774 and ((etch adj stop) near (silicon adj dioxide))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
9	BRS	53	((etch adj stop) near (silicon adj dioxide))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB
10	BRS	46	((etch adj stop) near (silicon adj dioxide))	USPAT
11	BRS	3	6133598.pn. or 6046505.pn. or 5234856.pn.	USPAT
12	BRS	4	6133598.pn. or 6046505.pn. or 5234856.pn. or 5338700.pn.	USPAT
13	BRS	426	(438/634 or 438/637 or 438/639 or 438/257)and etch adj stop and (conductive or metal or wiring) and (insulating or dielectric)	USPAT
14	BRS	392	(438/634 or 438/637 or 438/639 or 438/257)and etch adj stop and (conductive or metal or wiring) and (insulating or dielectric)adj layer	USPAT

	Type	Hits	Search Text	DBs
15	BRS	117	(438/634 or 438/637 or 438/639 or 438/257)and etch adj stop and (conductive or metal or wiring) and (insulating or dielectric)adj layer and spacer	USPAT

SAMSUNG-1002.264

	Type	Hits	Search Text	DBs	Time Stamp
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2	BRS	659	257/776 and spac$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 20:34
3	BRS	839	(438/634 or 438/637) and spacer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 20:48
4	BRS	1541	(438/639 or 438/257) and spacer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 21:13

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	Type	Hits	Search Text	DBs	Time Stamp
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6	BRS	312	(257/759 or 257/760 or 257/762) and spacer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 21:28
7	BRS	276	(257/763 or 257/765) and spacer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 21:29

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2	BRS	2591	257/774	USPAT	2004/04/07 17:58
3	BRS	1531	257/774 and spac$3	USPAT	2004/04/07 18:57
4	BRS	8	"6066555"	USPAT	2004/04/07 18:00
5	BRS	204	257/774 and spac$3	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 20:24

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-	2591	257/774	USPAT	2004/04/07 17:58
-	1531	257/774 and spac$3	USPAT	2004/04/07 18:57
-	8	"6066555"	USPAT	2004/04/07 18:00
-	204	257/774 and spac$3	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 20:24
-	517	257/775 and spac$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 20:29
-	659	257/776 and spac$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 20:34
-	839	(438/634 or 438/637) and spacer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 20:48
-	1541	(438/639 or 438/257) and spacer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 21:13
-	836	(257/756 or 257/757 or 257/758) and spacer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 21:14
-	312	(257/759 or 257/760 or 257/762) and spacer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 21:28
-	276	(257/763 or 257/765) and spacer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/07 21:29

Selective dry etching in a high density plasma for 0.5 μm complementary metal–oxide–semiconductor technology

J. Givens, S. Geissler, J. Lee, and O. Cain
IBM Corporation, Technology Products, Essex Junction, Vermont 05452

J. Marks, P. Keswick, and C. Cunningham
Applied Materials, ACET New Products Group, Santa Clara, California 95054

(Received 6 August 1993; accepted 7 October 1993)

0.5 μm complementary metal–oxide–semiconductor structures were utilized to investigate the selective nature of a high density plasma reactor. The formation of borderless contacts and local interconnects by the selective etch stop film approach was discussed and shown to be affected by topography, planarization, and nonuniformities. A factorial design of experiments determined the optimum conditions of the selective oxide etch chemistry. The resulting etch chemistry was characterized by measurable quantities such as an oxide etch rate of 1200 nm/min, a patterned (0.5 μm image) etch-rate ratio for oxide:nitride >100:1 and 5%-3σ uniformity. And, finally, an integrated *in situ* oxide etch/resist strip/nitride etch was presented.

I. INTRODUCTION

The reduced cell size of static random access memory (SRAM) and desired enhancements in logic performance necessitate the use of borderless contacts and local interconnects in very high performance 0.5 μm complementary metal–oxide–semiconductor (CMOS) technologies. After device fabrication, local interconnects and borderless contacts can be formed simultaneously using a tungsten damascene stud process.[1] One such approach utilizes a silicon nitride film (as an etch stop) coupled with a highly selective oxide:nitride etch chemistry. Using a plasma enhanced chemical vapor deposition (PECVD) for the nitride film provides a low temperature ($T_{max} \approx 600$ °C) metallization scheme with its inherent advantages.[2]

The key to the etch stop approach is the use of a selective oxide:nitride etch process. This selective etch is difficult to achieve since both materials behave similarly. Oxide selectivities have been obtained by combining polymer deposition and high ion bombardment.[3,4] However, in conventional reactive ion etch (RIE) and magnetically enhanced RIE (MERIE) reactors, the control of polymer deposition and ion bombardment energy is limited. Thus, the etch process is marginal for both maintaining selectivity to nitride and sustaining the oxide etch rate.

This article presents the etch process window for a selective oxide: nitride etch chemistry which could be used for the above application. Experiments were performed using realistic semiconductor structures (0.5 μm feature sizes) utilizing a PECVD nitride film as the etch stop layer. All experiments were done in a high density plasma (HDP) etch system and correlations between the HDP conditions and etching characteristics are presented.

II. EXPERIMENT

The experiments for this study were processed in a HDP chamber schematically shown in Fig. 1. The plasma source region of the process chamber is a nonresonant, multiple turn antenna wound around a quartz cylinder. The antenna is capable of delivering up to 3000 W of rf power to the chamber to generate a very high plasma density. The biased electrode is used to extract ions from the plasma. A rf bias voltage, coupled through a solid state matching network, as is the source voltage, is capacitively coupled to the wafer to control ion energy. In addition to being operated "off resonance," this configuration improves upon established helical resonator technology with the inclusion of a top electrode in the source region. This electrode provides a large area dc grounded reference for the plasma which minimizes the likelihood of chamber wall sputtering and provides for a stable discharge over a wide range of operating conditions. The chamber is pumped using a 600 ℓ/s turbomolecular pump allowing the process to operate at <10 mTorr. Ion densities in excess of 1E12 have been recorded using Langmuir probe techniques to measure an argon plasma discharge at a pressure of 10 mTorr with a source power of 2500 W.[5]

III. RESULTS AND DISCUSSION

A. Borderless contact process window

The implementation of borderless contacts/local interconnects requires a determination of the process window. The silicon nitride etch stop approach has been evaluated with the basis of the analysis being the selectivity calculation, i.e., etch-rate ratio (ERR). The feasibility of this approach relies on the following two ERRs:

(1) selectively etching oxide insulator layer to nitride film;
(2) selectively etching nitride film to silicon and oxide.

These two etches are performed in succession, respectively. Intuitively, the selectivity required for etching oxide to nitride is inversely proportional to the nitride thickness, whereas, the selectivity needed for etching nitride to silicon and oxide is proportional to the nitride thickness. As one can infer, the silicon nitride etch stop thickness must be optimized based on the empirical results of the selective etch chemistries. For this article, we shall concentrate on the selective etching of oxide to nitride in our calculations.

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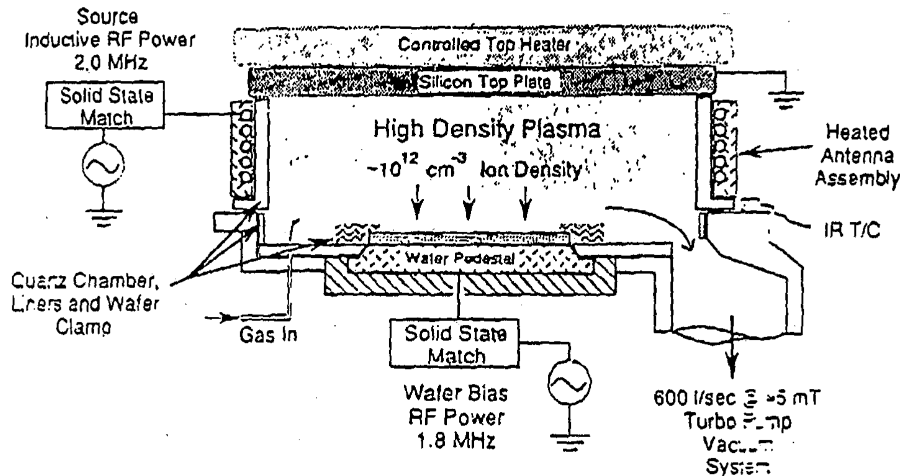

FIG. 1. Schematic of the high density plasma reactor used for this study.

When analyzing the etch stop process, the first factor to be considered is the degree of functionality offered to the technology. In other words, what type of contact or interconnect is to be made? Will the contact be bordered (protective spacing added) or borderless (eliminates critical lithographic alignment) to the gate and/or device isolation? The most difficult application is the source/drain contact which is borderless to the gate. This particular contact is permitted to land on the gate structure, but remain electrically isolated from the gate, while making electrical connection to the source and drain. A contact that is borderless to the gate contact demands the largest ERR. Figure 2 depicts the borderless to gate (a) and borderless to diffusion (b) contacts.

After examining the process functionality, one must evaluate the process steps and their relationship to the ERR calculation. The important parameters to consider are the device topography and tolerance, nitride thickness and tolerance, insulator thickness and tolerance, percent planarization, and percent overetch and etch tolerance. A statistical analysis of the 3-σ process window is depicted in Figs. 3, 5, and 6.

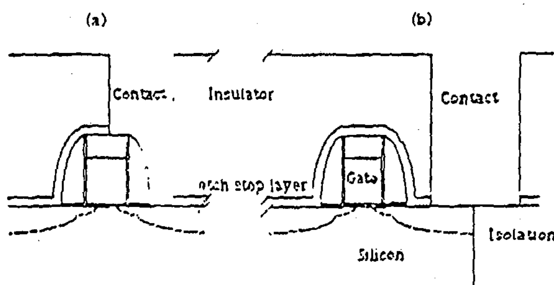

FIG. 2. Schematic of the physical cross sections for a borderless to gate (a) contact and a borderless to diffusion (b) contact.

Figure 3 shows the effect of etch stop thickness on the selectivity required for the borderless contact. This calculation has assumed a gate stack of 5500 and 8250 Å of insulator. The significance of the graph is the inverse relationship of the ERR to nitride film thickness and the dramatic effect of planarization on the required selectivity. The inverse ERR relationship is a critical parameter for integration concerns. When removing the nitride etch stop, minimizing the removal of device isolation oxide is the main objective. One obvious technique is to thin the etch stop thickness for a given nitride etch process thus moving the oxide loss distribution to lower values. However, the generation of large, controllable oxide:nitride selectivities is very difficult in conventional RIE and MERIE systems.[5] Therefore, a realistic

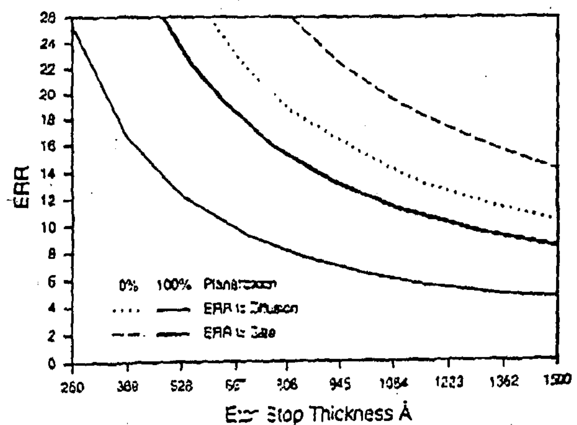

FIG. 3. Graph of the ERR as a function of the etch-stop layer thickness. Depicted in this figure is the inverse relationship of the ERR to nitride film thickness and the dramatic effect of planarization on the required selectivity. The calculation has assumed a stack height of 5500 and 8250 Å of insulator.

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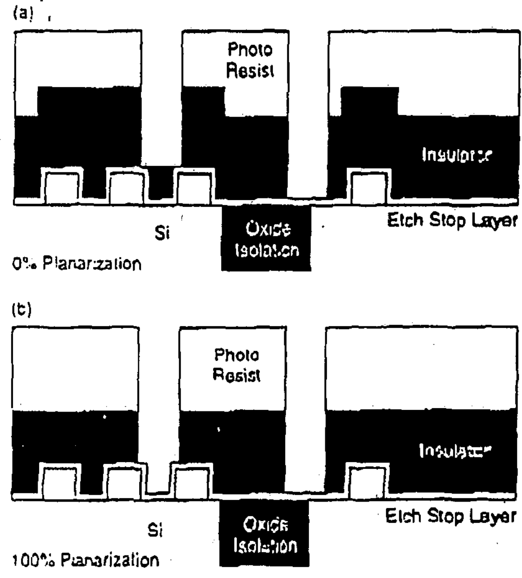

FIG. 4. Illustration of the effect of planarization. Planarization removes the insulator thickness differences between dense and isolated structures.

evaluation of the overall process window must account for both oxide:nitride selectivity and subsequent device isolation loss. (The process must minimize nitride remaining after the oxide etch and minimize nitride overetch in the nitride etch.)

Also shown in Fig. 3 is the dramatic effect of planarization on the required selectivity. Planarization produces a significant reduction in the ERR requirement and opens the process window to allow for a decrease in the etch stop thickness. This improvement is accomplished by reducing the oxide thickness differences between highly dense semiconductor devices and isolated structures which in turn reduces the amount of overetch on the nitride film in the isolated areas thus decreasing the necessary selectivity. Figure 4 illustrates the effect of planarization.

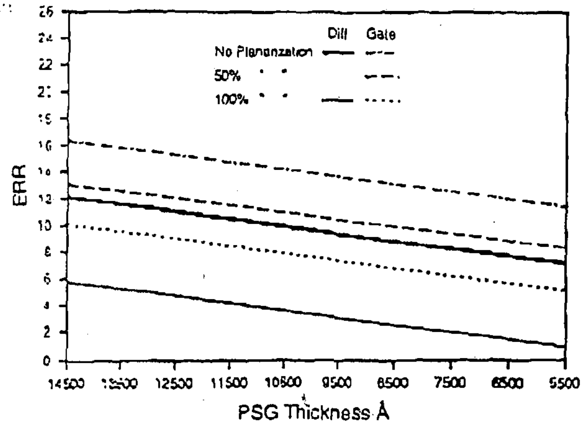

FIG. 5. This graph of the ERR vs the PSG (insulator) thickness shows a linear dependence as calculated. This is a direct result of selectivity being proportional to the tolerances (nonuniformities) of the process. A 1500 Å etch stop film and 5500 Å stack height are assumed.

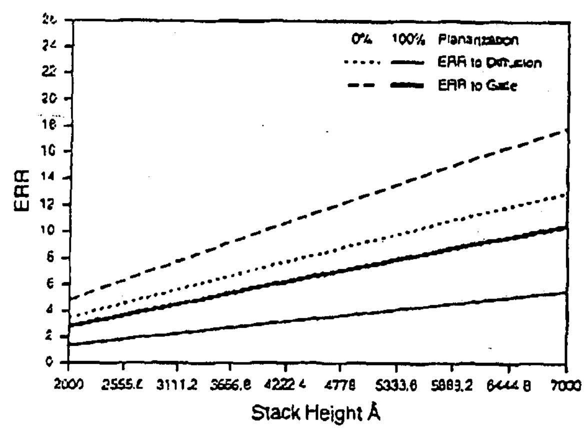

FIG. 6. The ERR as a function of the underlying stack height (gate topography). The selectivity necessary to fabricate borderless contacts is proportional to the gate topography. The analysis assumed a 1500 Å nitride film and PSG thickness given by 1.5× the stack height.

Figure 5 shows the ERR as a function of insulator thickness. IBM uses phosphosilicate glass (PSG) as the insulator. A 1500 Å etch stop film and 5500 Å gate stack are assumed. The graph presents the linear dependence of the selectivity on the PSG thickness. (The ERR is also proportional to the tolerances of the overall process.) From this graph, one can see the need to optimize the PSG thickness for a reduction in the selectivity requirement. Also shown again is the improvement in process margin afforded by planarization.

The relationship of selectivity and gate stack topography is shown in Fig. 6. The analysis assumed a 1500 Å nitride film and PSG thickness given by 1.5× the stack height. The significance of the graph is that the selectivity necessary to fabricate the borderless contacts is proportional to the gate topography. Also, with increasing topography, planarization provides a large reduction in the ERR requirements of the process.

From the preceding analysis, the relationships between insulator thickness, etch stop thickness, and gate stack height and the required ERR were revealed. Optimization of these parameters, coupled with planarization, provides an enlargement of the process window for the selective etch chemistry and reduction in the ERR. Conversely, utilization of a highly

TABLE I. Oxide etch process trend summary. A dash means parameter is not function of change in process variable.

Parameters	Oxide ER	Nitride ER	Profile	μ loading
C_2F_6 flow	↗	↑	—	↘
Pressure	↗	↗	More taper	↗
Source power	↘	↓	More vertical	↘
Bias power	↑	↗	More vertical	↗
Si top plate temperature	↗	↓	—	—

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TABLE II. Oxide and nitride etch comparison.

	Conventional RIE	HDP etch
Oxide etch rate (4 wt % PSG)	4000 Å/min	12 000 Å/min
Selectivity (PSG: nitride) (Meas. 0.5 μm hole)	8.1	100:1
Uniformity	9%-3sigma	5%-3sigma
Critical dimension slope	86–88 deg	88–90 deg
Nitride etch rate (PECVD nitride)	500 Å/min	2500 Å/min
Selectivity (Blanket) (Nitride: TEOS)	3:1	7:1[a]
Uniformity	6%-1sigma	15%-1sigma[a]

[a]Preliminary results.

selective oxide etch would increase the processing latitude for each of these parameters.

B. HDP oxide etch

The key to generating a highly selective oxide:nitride etch is the reduction of fluorine in the polymer by-product generated during the etch process. This has been accomplished by using a heated Si top plate and a high C:F ratio fluorocarbon in the HDP reactor.[5]

A computer aided design of experiments was performed to characterize the HDP process parameters. The experiments consisted of two matrices comprising a two level fractional factorial with four factors and one center point each. The five variables studied were: C_2F_6 flow, pressure, source power, bias power, and Si top-plate temperature. The measured responses were: oxide etch rate, nitride etch rate, profile angle, and microloading. Oxide and nitride wafers patterned with a deep ultraviolet (UV) resist at 0.5 μm dimensions were used as monitors. Etch rates were determined by scanning electron microscopy (SEM) cross-sectional measurements in 0.5 μm structures on 200 mm wafers.

Table I provides a summary of the trends generated by the factorial experiments. The C_2F_6 flow, and source power are shown to have a strong effect on the nitride etch rate, while

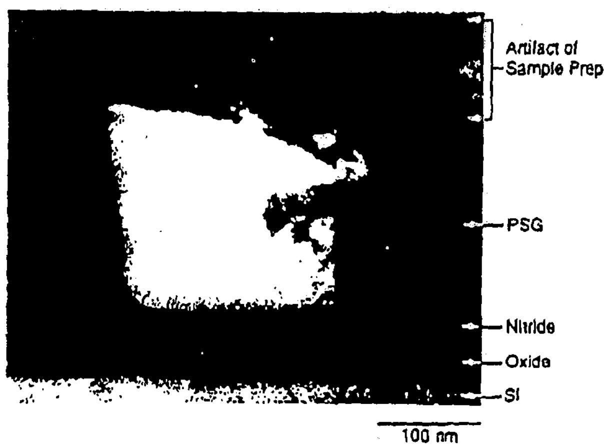

FIG. 7. Cross-sectional TEM micrograph depicting the selectivity of the HDP oxide etch process. The empirical selectivity of PSG (4 wt %) to PECVD nitride was determined to be greater than 100:1.

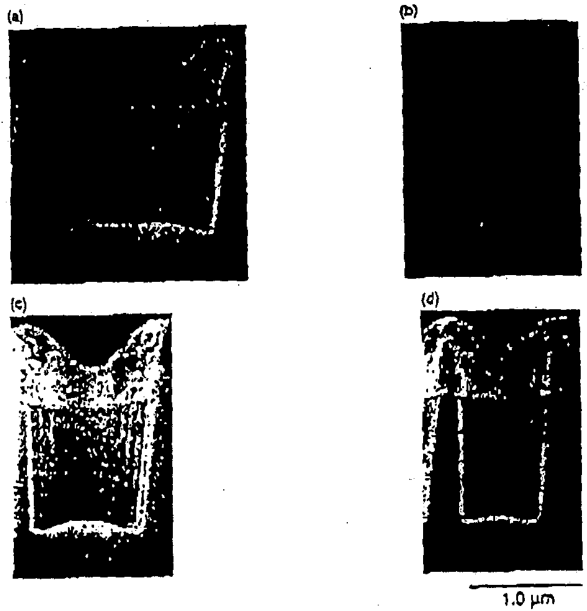

FIG. 8. SEM micrographs depicting the HDP oxide etch rate as a function of contact image size. The etch rate is constant for all image sizes (smallest feature=0.5 μm).

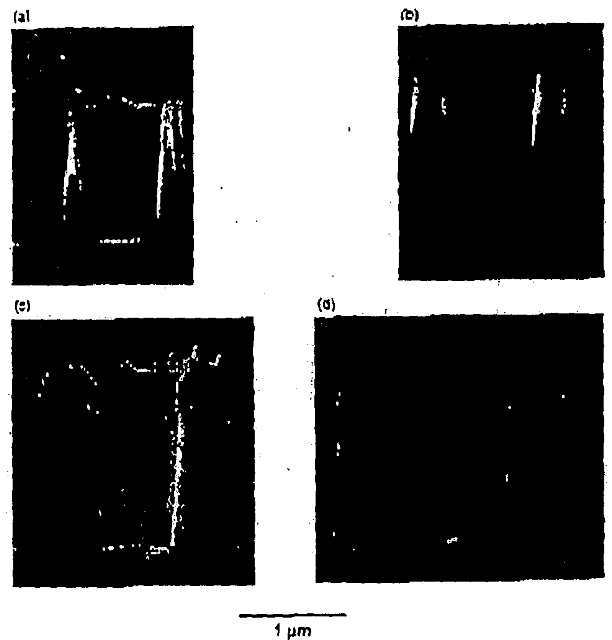

FIG. 9. The oxide etch rate is shown to be constant with variable spacing between contacts. The SEM micrographs also show that enhanced resist sputtering can occur with minimal image spacing.

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the oxide etch rate is very sensitive to changes in the bias power. Using the results of the matrices, the process was optimized for the measured responses. The resultant conditions were

35 sccm C_2F_6, 4 mTorr, 2700 W source,

1400 W bias, 250 °C.

Table II presents the measured properties of the optimized HDP oxide etch process as compared to conventional RIE/MERIE. Readily seen from this data are the improvements in oxide etch rate, selectivity, uniformity, and anisotropy.

Figure 7 is a transmission electron microscopy (TEM) cross section of a patterned structure which has been etched with the optimized conditions. The PSG (4 wt % phosphorus) has been etched down to the PECVD (480 °C deposition process) silicon nitride. The nitride was subjected to 100% overetch and exhibited ≈125 Å loss. A conservative estimate of the selectivity (PSG etch divided by nitride etch rate) yields 100:1. The selectivity is conservative because it is independent of the overetch. An initial material loss no etch rate is observed on the nitride film. After the etch clears the PSG and exposes the nitride, the nitride initially etches but this process is rapidly terminated as deposition of the carbon rich polymer begins on the nitride.

The effect of pattern factor on microloading is shown in the scanning electron microscopy (SEM) cross sections of Figs. 8 and 9. This experiment also used the optimized etch process. Figure 8 presents microloading as a function of variable contact size. No degradation in the etch rate is observed with the decreasing contact diameter (smallest feature=0.5 μm). Figure 9 shows that the HDP etch rate does not change with variable spacing between images. However, at very small spacing, the resist experiences enhanced sputtering. This is a geometric phenomenon stemming from the resist having a triangular profile rather than the expected rectangular shape. The scalloping depicted in the micrographs is currently being investigated. The microloading results are in agreement with earlier work.

TABLE III. Nitride process trend summary. A dash means nitride ER≠f(CO_2 pressure).

Parameters	Nitride ER	Oxide ER	Profile
CH_3F	↘	↗	More taper
CO_2	↘	↓	
Pressure	—	↘	More taper
Source	↗	↘	
Bias	↘	↗	

C. HDP nitride etch

In order to examine the feasibility of etching nitride selectively to oxide, a two level fractional factorial with five factors and one center point was performed. The five variables studied were: CH_3F flow, CO_2 flow, pressure, source power, and bias power. The measured responses were nitride etch rate, oxide etch rate, and profile angle. Unpatterned oxide and nitride wafers were used as planar etch rate monitors. The oxide film was an undensified low-pressure chemical vapor deposition (LPCVD) tetraethylorthosilicate (TEOS) and the nitride was deposited by PECVD (480 °C process). Nitride wafers patterned with a deep-UV resist at 0.5 μm dimensions were used as profile monitors. Etch rates were determined by spectral reflectivity measurements on the 200 mm wafer surfaces.

Table III provides a summary of the trends generated by the factorial experiment. The CO_2 flow is shown to have a strong effect on the oxide etch rate, while the oxide etch rate is very sensitive to changes in the bias power. The results of the matrix revealed a process which selectively etched nitride to oxide with a ratio of 7:1. The resultant conditions were

34 sccm CH_3F, 92 sccm CO_2, 25 mTorr,

2700 W source, 150 W bias.

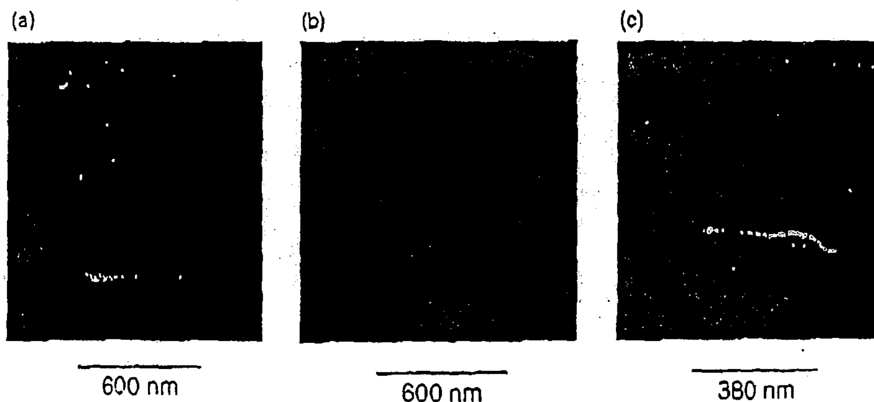

FIG. 10. SEM micrographs showing the HDP *in situ* process flow. (a) The oxide etch removes the insulator and selectively stops on the nitride layer. (b) The polymer generated at the bottom of the contact and the remaining resist are removed by an O_2 plasma. (c) The nitride etch stop is etched selectively to the underlying silicide and oxide isolation.

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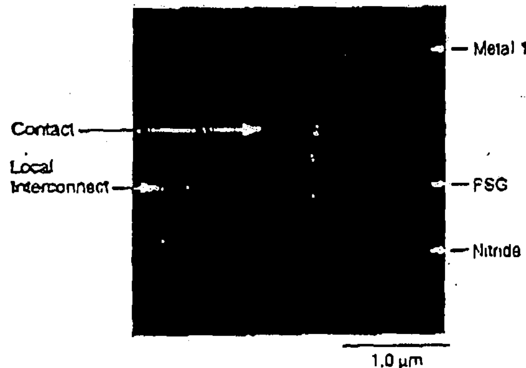

FIG. 11. SEM cross section of a local interconnect borderless to the device isolation. The interconnect is wired to the metal 1 layer thru a contact stud.

More experiments examining the process and patterned selectivity are in progress. The preliminary results for this process are shown in Table II.

The significance of the cursory nitride evaluation is that an integrated, highly selective, *in situ* etch solution was now possible. Figure 10 is a sequence of SEM micrographs showing the HDP *in situ* process flow. The sequence of processes within the HDP reactor are shown to be the following.

(a) The oxide etch removes the insulator and selectively stops on the nitride etch stop layer.

(b) The polymer generated at the bottom of the contact and the remaining resist are removed by an O_2 plasma.

(c) The nitride layer is etched selectively to the underlying silicide and oxide isolation. The dip shown in the bottom right corner of the micrograph is the materials interface between the device silicon and the planarized oxide isolation.

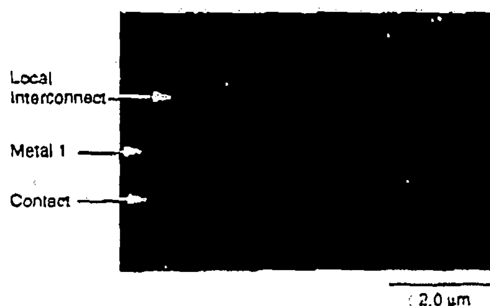

FIG. 12. SRAM wiring is shown in this SEM micrograph. Extensive local interconnect usage is apparent. The passivating and insulating layers have been removed by sample preparation.

TABLE IV. Electrical improvements for HDP over conventional RIE.

Parameter	Improvement	Physical correlation
Junction leakage	10X[a]	Silicide damage isolation loss
R_s[b]	33%[a]	CD control
Contact resistance	25%[a]	Silicide damage CD control

[a]Distribution tails reduced.
[b]Sheet resistance.

The discontinuity is due to device processing and not the result of plasma etch trenching.

D. Electrical characterization

The HDP selective oxide etch was utilized as part of the tungsten damascene stud process for contact and interconnect formation. Figures 11 and 12 are SEM micrographs depicting typical W interconnect structures. The electrical data for the HDP oxide etch is compared to conventional RIE results in Table IV. The highly selective nature of the HDP process caused less silicide damage and isolation loss which translated into a 10X improvement in diffusion junction leakage for the borderless contacts. Improvements in etch uniformity and contact profile were electrically characterized by reductions in sheet resistance and contact resistance. The full benefit of the HDP process cannot be realized until both the oxide and nitride are removed in this reactor.

IV. SUMMARY

0.5 μm CMOS structures were utilized to investigate the selective nature of a high density plasma (HDP) reactor. The formation of borderless contacts and local interconnects by the selective etch stop film approach was discussed and shown to be affected by topography, planarization, and nonuniformities. A factorial design of experiments determined the optimum conditions of the selective oxide etch chemistry. The resulting etch chemistry was characterized by measurable quantities such as an oxide etch rate of 1200 nm/min, an ERR for oxide:nitride>100:1, and 5%-3σ uniformity. And finally, an integrated *in situ* oxide etch/resist strip nitride etch was presented.

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Hafnium dioxide etch-stop layer for phase-shifting masks

K. K. Shih, T. C. Chieu, and D. B. Dove
IBM Research Division, Thomas J. Watson Research Center, Yorktown Heights, New York 10598

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Phase-shift masks were prepared using sputter deposited films for the phase-shift layer and etch stop layer on fused quartz silica substrates. It has been found that the combination of SiO_2 for the phase-shift layer and HfO_2 for the etch-stop layer offers a unique combination of properties advantageous for the preparation of phase-shift masks. The optical transmission properties of HfO_2 layers with or without a SiO_2 phase-shifting layer on quartz substrates are presented.

The use of the phase shift approach to increase the resolution of lithography has been reported.[1-4] Several methods have been reported for obtaining the 180° optical phase-shift pattern. Etching into the surface of the quartz plate has a number of advantages but requires great care in etching uniformly to the correct depth. Spin-on-glass layers have also been reported. These require special thermal processing to achieve the desired properties. We have investigated the use of sputtered films of SiO_2. In order to etch the phase-shift layer without etching the quartz substrates, an etch-stop layer is necessary. Al_2O_3 (Ref. 5) has been recommended as an etch-stop layer because it has good optical transmission at *i* line and in the deep UV, and it also has good etch selectively for the SiO_2 phase-shift layer. We have found that it is difficult to produce Al_2O_3 films that are resistant to typical chemical cleaning process (e.g., 4:1 H_2SO_4: H_2O_2 at 90 °C). Also the films are typically highly stressed, which is very undesirable for the phase-shift mask (PSM) application due to the high level of flatness required of the substrates. Although methods can be found to produce high-quality films,[6] alternative materials were sought for this application. We have reviewed the literature and found that HfO_2 films have good UV transmission properties and are difficult to etch. Since the other properties of HfO_2 films are not well known, it is of interest to study them and to determine whether HfO_2 films are good etch-stop layers for PSMs.

We then discovered that HfO_2 films not only have good optical transmission at *i* line and deep UV, good etch selectivity with the SiO_2 phase-shifting layer, low film stress on quartz substrates, but are also not attacked by the chemical cleaning solution at 90 °C. The HfO_2 films were deposited by a rf sputtering process. The sputtering system was evacuated to less than 10^{-7} Torr by a turbomolecular pump prior to the introduction of the argon–oxygen gas mixture. 5 in.^{2} fused silica plates were used as substrates and were mounted on a water-cooled 8 in. diam plate. During the deposition input power was between 200 and 400 W. Argon–oxygen gas mixture was used, and the total pressure was 5 mTorr. The oxygen content in the sputtering gas was ~10%; oxygen contents as high as 40% have been used with no significant effects on deposited films. After deposition, thicknesses were determined by a Tencor Alpha-step Profilometer. Films were grown with thicknesses varying from ~50 to 105 nm. For some of the samples, SiO_2 phase-shifting layers were deposited on top of some HfO_2 films for the study of their optical properties. Optical transmission was measured using a Varian DMS-

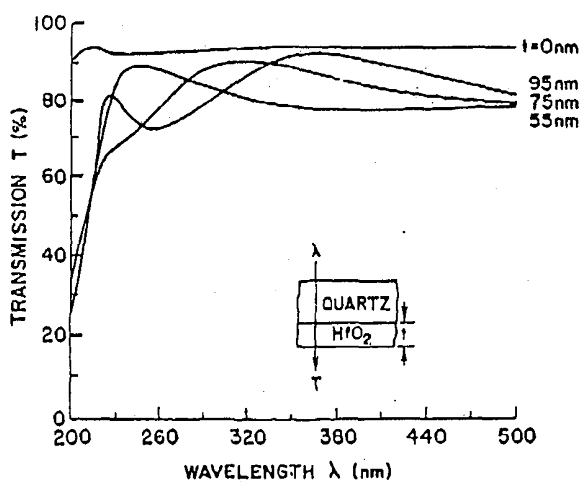

FIG. 1. Optical transmission of HfO_2 films with different thickness on fused quartz substrates.

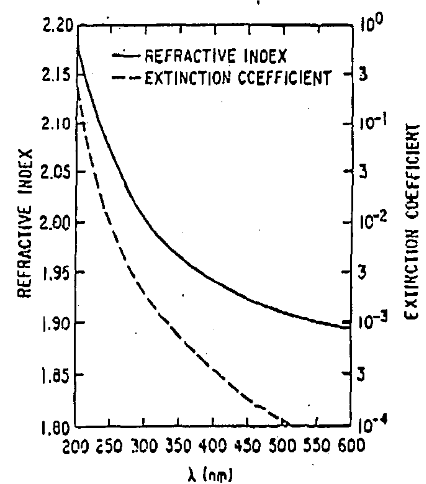

FIG. 2. Refractive index of HfO_2 on quartz substrates between 200 and 600 nm.

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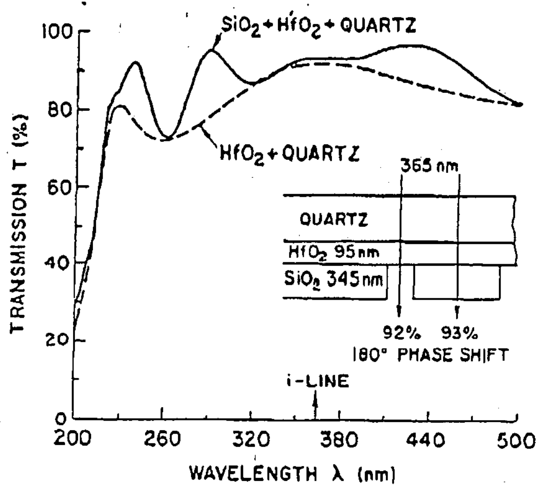

FIG. 3. Optical transmission spectra of a PSM designed for an *i*-line (365 nm) stepper.

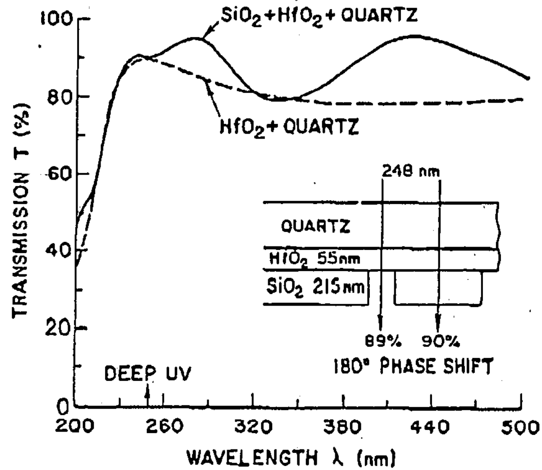

FIG. 4. Optical transmission spectra of a PSM designed for a deep-UV (248 nm) stepper.

200 UV visible spectrophotometer. The film stress was measured by observing interference fringes between the surface of the silica plate and an optical flat plate before and after film deposition.

The stress of HfO_2 films is sufficiently low that no more than two fringes between the coated substrates and the optical flat plate was observed. The HfO_2 film etch rate was evaluated using reactive ion etching (RIE) employed for patterning the SiO_2 layer. We tested the etch rate on a Plasma-Therm RIE system using CHF_3 gas at 100 W power and 50–100 mTorr pressure. A series of runs was carried out to determine the optimum SiO_2 etching conditions. It was found that the ratio of etch rate for HfO_2 to SiO_2 is better than 1 to 16. These results of etch studies will be reported in detail in another article.[7]

The transparency of HfO_2 films deposited on quartz substrates was measured from 200 to 500 nm as a function of film thickness, and the results are shown in Fig. 1. As shown in Fig. 1, for *i*-line application, a film with a thickness of ~ 95 nm had an optical transmission of $\sim 92\%$ at 365 nm. With decreasing thickness, the peak shifts to lower wavelength. The optical transmission is $\sim 89\%$ at 248 nm at a film thickness of ~ 55 nm.

The refractive index and extinction coefficient of films on quartz between 200 and 600 nm were calculated using a computer fit to the optical transmission curves for the given thickness of the films. The results are shown in Fig. 2.

Figure 3 shows the measured optical transmission spectra of a PSM designed for an *i*-line stepper. The thickness of the etch-stop layer was ~ 95 nm and that of the phase-shifting layer was ~ 345 nm. A small transparency difference of $\sim 1\%$ was observed. Figure 4 shows the measured optical transmission spectra of a PSM designed for deep UV at 248 nm. In this case, the thickness of the etch-stop layer is ~ 55 nm and the phase-shifting layer ~ 215 nm. Also, there is a small difference between the transmission with and without the SiO_2 layer at 248 nm. We have made a series of PSMs using these materials with etched patterns on 5 and 6 in.[2] quartz substrates. Details of design and fabrication of these masks will be published later.[7]

In summary, we have found that HfO_2 films can be used as etch-stop layers for PSMs. The films have good optical transmission at 365 and 248 nm and high etching selectively compared to SiO_2 film. This material also is chemically stable and not attacked by chemical cleaning solutions. In general, the sputtered HfO_2 films have been found to be very reproducible and are easily prepared in the chemically resistant, low stress condition.

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insulative, *a.*

Of, pertaining to, or as insulation.

1945 *Sci. News Let.* 23 June 397/3 The insulative concretes vary in weight from one-third to one-half that of ordinary gravel concrete. **1971** *Nature* 4 June 331/1 The fur was very spiny with virtually no soft underfur and thus probably offers little insulative protection. This may be an adaptation to the tropical environment. **1973** *Ibid.* 26 Jan. 240/1 Their fur is less than half as long..and has a correspondingly lower insulative quality.