

Timothy D. Dorney

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SUMMARY

An organized, creative professional offering extensive electrical engineering, VLSI design, testing, and patent prosecution experience. Strengths include full custom IC design, critical path optimization and switching noise reduction, layout, verification, parasitic back annotation, and debug. Managed several activities to improve device performance and project schedule. Technical lead for literal and equivalent patent claim infringement opinions. Developed and taught DRAM design and project specific material to joint ventures and in-house. A dependable, thorough, results-oriented team player who strives to find creative solutions.

SKILLS & ADVANCED COURSES

Languages: C, Windows C, FORTRAN, Pascal, Assembly, BASIC, PWS tslang

Programs: TISpice, Cadence Analog Artist, Mentor Graphics Design Architect and IC Station, ADCAP, ICE, LSIM, Siganal, MATLAB, AWK, HTML, Windows, UNIX, Interleaf, MS Office

Hardware: PC, Macintosh, DEC, HP, Apollo, Sun, Flex and Colt IIIA device testers

- Six Sigma Design for Manufacturability
- Advanced DSP
- Filter Theory
- Digital Image Processing
- Image Feature Extraction
- Spectral Estimation
- Computer Architecture
- VLSI
- Communication Theory
- Wavelets
- Random Processes
- Digital Control
- Artificial Neural Networks
- Fuzzy Logic
- Speech Processing
- Leading Effective Meetings
- Presentation Skills
- PC board design and manufacture

PROFESSIONAL EXPERIENCE

Rosenthal & Osha L.L.P., Houston, TX

2001 - 2003

Patent Agent

Applied broad area of experience to originate over 50 utility patent applications per year. Technical fields include analog and digital circuits, microprocessor architecture, computer system design, and digital signal processing (DSP). Responded to both national and international Office Actions, and filed RCEs in response to Advisory Actions. Managed 5 person team focused on protecting microprocessor core IP. Mentored patent engineers and reviewed draft applications.

Rice University, Houston, TX

1994 - 2001

Research Associate - Department of Electrical and Computer Engineering

Utilized a wide variety of DSP techniques for terahertz (THz) time-domain spectroscopy. Solved inverse problems, improved resolution, and facilitated imaging and classification for real-time THz systems. Authored 9 journal articles, and presented and/or authored papers for 16 conferences or lecture series. Other areas of investigation include wavelets, speech processing, biomedical imaging, and computer architecture.

Texas Instruments Incorporated, Houston, TX

1988 - 1998

MOS Memory Design

Circuits Center of Expertise Engineer - Memory Products Design

1997 - 1998

Originated comparisons of internal and competitor designs through simulation, characterization, deprocessing, and internal probe. Identified and evaluated key aspects of DRAM designs by interacting with design teams, product engineering, competitor analysis group, and external resources to gather and disseminate information. Built web

pages to report the analysis to a broad audience. Integrated information and made sound conclusions from which future designs could draw.

- Promoted and helped implement the formation of the Circuits COE that resulted in being the only individual contributor chosen from the Houston design center.
- Achieved an 8% speed improvement in access time through a redesign of the critical path and output buffers.
- Identified and correlated device processing characteristics which degraded signal transmission and device performance.
- Simulated and summarized the work on competing access versus hold time specifications which demonstrated that additional regulation circuitry was not needed.

IC Design Engineer - Application Specific DRAM Design

1990 - 1997

Demonstrated engineering breadth and depth through the design, simulation, probe, debug, and test support of various major sections on at least five devices, two of which had 95M units shipped with \$525M in sales. These included row and row redundancy, column and column redundancy, design-for-test, I/O buffers, internal refresh, and data I/O. Performed full-chip schematic verification, design rule verification, and probe versus simulation comparison. Supported the leadframe design, ESD implementation, parasitic back annotation, laser repair, and layout.

- Originated six patents and two pending patents that focused on reduced silicon usage and improved DRAM performance.
- Traveled to Japan (KTI), and Singapore (TECH) for Design support and training. Traveled to TI-Singapore for T3/batch testing support.
- Spearheaded new hire activities and on-campus recruiting which resulted in at least ten new employees.
- Mentored and supervised engineers and layout support to achieve on-time schematic verification.
- Selected point person by V.P. to assemble a team, create, and help instruct "DRAM Design for Non-DRAM Designers". Implemented the course both in Europe and Asia Pacific region.
- Investigated and audited TI's first commercial 64 megabit Synchronous DRAM column, internal refresh, voltage regulators, and power-up circuitry.
- Provided weekly training of DRAM design basics to Houston PDE/CQE engineers.

Product Development Engineer - Video RAM Development

1988 - 1990

Programmed a PWS Colt IIIA device tester for gross functional tests and test time reduction. Drafted specification sheets. Created and updated device comparison tables. Resolved customer issues including returned device evaluation and device specification comparison.

EDUCATION

Ph.D., Electrical and Computer Engineering, Rice University, Houston, TX - 2002. (4.0/4.0)

M.S., Electrical Eng. and Applied Physics, Case Western Reserve University, Cleveland, OH - 1992. (3.8/4.0)

B.S., Electrical Engineering, Texas A&M University, College Station, TX - 1990. (3.6/4.0)

HONORS & CERTIFICATIONS

- Honors Program Diploma, Texas A&M
- Cum Laude, Texas A&M University
- Eta Kappa Nu Honor Society
- Tau Beta Pi Honor Society
- Registered Patent Agent - USPTO
- Engineer in Training - Texas
- Phi Kappa Phi Honor Society
- Boy Scout Eagle Palms Award