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during a three-channel transmission above that which is observed in a two-channel receiver during a two-channel transmission.

In the above analysis, the output peak S/N ratio was defined as the ratio of the peak output signal power in the absence of noise to the mean output noise power in the presence of an unmodulated carrier [8].

Acknowledgment

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The Vertical Interval: A General-Purpose Transmission Path

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***Abstract*—Equipment is now available to utilize the vertical interval of the television signal to transmit digital information. A vertical interval (VI) encoder selects any line, 13 through 20, onto which is clocked the data originating from a character generator, computer or other digital device. At the receiving point, data are decoded for display in "real time" using a character generator, printed out in hard copy, or used to initiate electromechanical operations through proper interfaces.**

Numerous applications exist for VI transmission: transmitting information to network affiliates, newswire distribution, remote computer access, centralized clock system control, remote control of VTR's and video switchers, and test signal transmission.

Introduction

HISTORICALLY the vertical blanking interval has been utilized by television networks and common carriers to transmit video test signals. Equipment is now available that further permits the addition of digital information from character generators, computers, and other sources onto the vertical interval.

Fig. 1 shows a picture of the vertical interval with data encoded on line 16. Note the equalizing pulses, vertical serration, and the beginning of the horizontal lines that occur during vertical blanking. As you know, each television line is equal to 63.5 μs. About 50 μs of each line is used to handle the data. To determine the theoretical maximum amount of time or space available during the vertical interval, subtract line 13 from line 20, equalling 7 lines: 7×50 gives us 350 μs, the total time available.

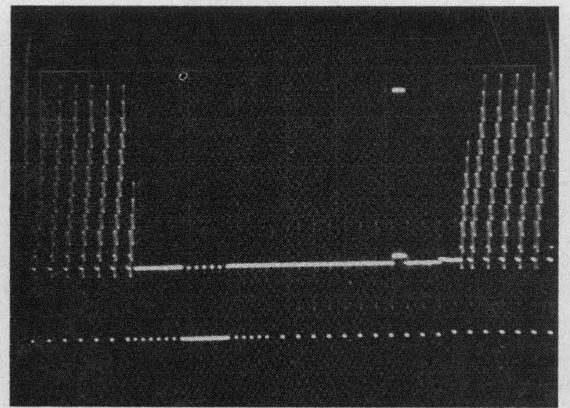

Fig. 1. Vertical interval with data encoded on line 16.

The practical limit in handling raw data is about 40 bits per horizontal line; however, by means of modulation techniques, we can easily have 160 bits per hori-

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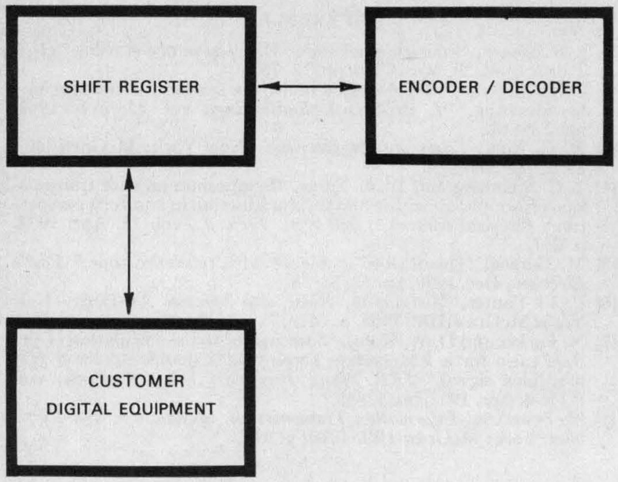

Fig. 2. Vertical interval encoder/decoder system.

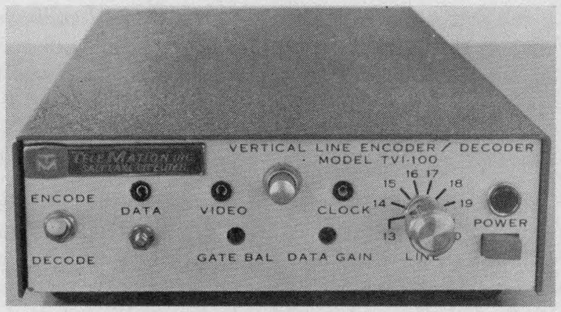

Fig. 3. TVI-100 Vertical Interval Encoder/Decoder.

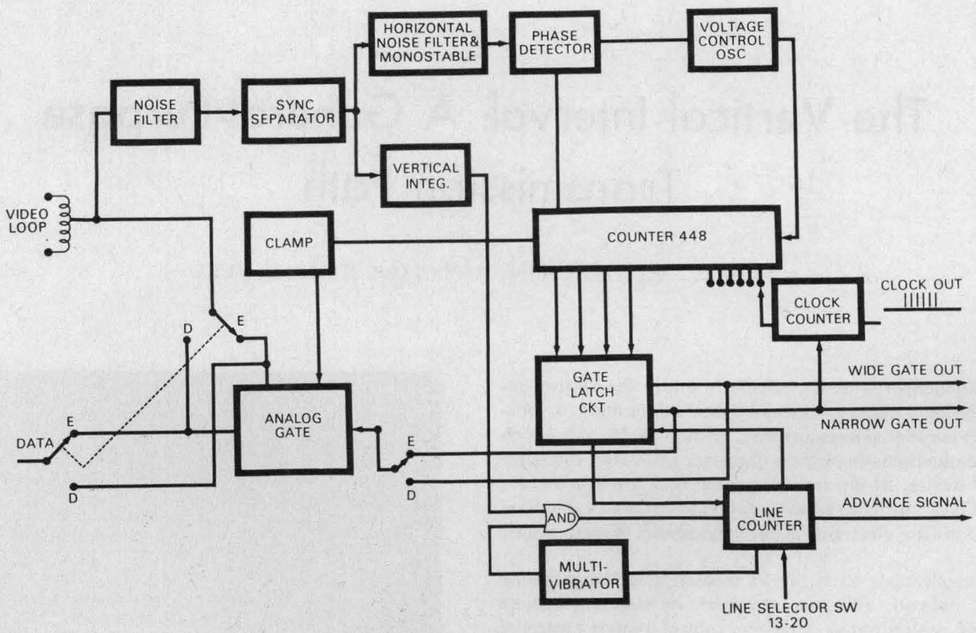

Fig. 4. TVI-100 circuit diagram.

zontal line. The limitation is fixed by the bandwidth of the system which is just slightly greater than 4 MHz.

It is possible to add data to more than one line at a time, making use of any line that has not been assigned or is not in use for test signals.

Adding Data to the Vertical Interval

If we consider that we have access to one horizontal line (50 μs) each 1/60 of a second in which to send information, this means we must wait approximately 16 000 μs before sending any other information. Storage is not necessary when adding test signals to the vertical interval since they are keyed directly into the selected line. However, to insert data, some means is needed to store the information generated at a fixed rate until it can be added to the video signal, such as the shift register in Fig. 2. Fig. 2 is a simple block diagram of the vertical interval encoder or decoder system. It shows the TVI-100 Vertical Interval Encoder, a shift register, and the consumer's digital equipment. (The TVI-100 can be either an encoder or a decoder, depending on the position of the encode/decode switch shown in Fig. 3.)

Starting with the video loopthrough (Fig. 4) we can follow the signal up to the noise filter, which is used to improve the signal-to-noise ratio of the system. The cutoff frequency is selected to roll off a peak white signal that precedes the front porch as much as possible without doing away with it altogether. The sync separator, a rather sophisticated device, is fed by a constant current source to prevent the average picture level from changing the clipping point.

The stripped sync is then fed to a vertical integrater and to a low-pass filter, which improves the signal-to-noise ratio even further. At this point, we actually invert the sync to trigger the monostable multivibrator. The output of this monostable is fed into a phase detector that controls the frequency of a voltage-controlled oscillator.

In an earlier unit, the oscillator was shock-excited and the starting of the oscillator was determined by one horizontal sync pulse. If noise was present, a phase shift would result, which caused problems in getting the encoder and the decoder correctly phased together.

In this later design, the voltage-controlled oscillator runs continuously. The horizontal sync pulses are integrated for a complete frame, so if noise is present, it will average out and cancel. By feedback, we control the frequency and phase of the oscillator, causing it to run at about 7 MHz.

The counter is TTL logic. You will notice it is marked for a count of 448. The monostables are a basic divide-by-512 with the NAND gate detecting the 449th count and resetting the counter to zero. The counter is necessary to lock the 7-MHz oscillator to the incoming sync for system timing.

The TVI-100 provides for a wide and a narrow gate output. The narrow gate out is used for encoding, the wide gate out for decoding. These gate pulses are derived from the counter: the divider is decoded to provide start and stop pulses to determine width of each of the pulses.

Taps on the counter permit changing the clock frequency, depending on the amount of data to be encoded in the vertical interval. Notice the lines from the gate circuit to the line counter. The line selector selects a line, 13 through 20. The monostables keep any incoming signal from triggering the line counter until the vertical interval approaches. When the vertical signal arrives, we start the line counter and let it run until it selects the desired line. To alert the character generator or computer that information will be sent on the next line, an advance signal pulse is generated one line ahead of the line selected for transmission.

The real key to the whole encoder is the analog gate circuit (Fig. 5). Starting from the video loopthrough, we see the input to the noise filter and sync separator. Notice the data input; we are in the encode mode. The data come into an emitter–follower that offers a high impedance to the video loopthrough and a low impedance to the diode gate. When the narrow gate arrives, we forward-bias the diode bridge, closing the gate. The TVI-100 clocks the data out of the shift register only when the diode gate is closed.

The current adder, made of $Q1$ and $Q2$, is designed so the collector junction is at ground potential. When

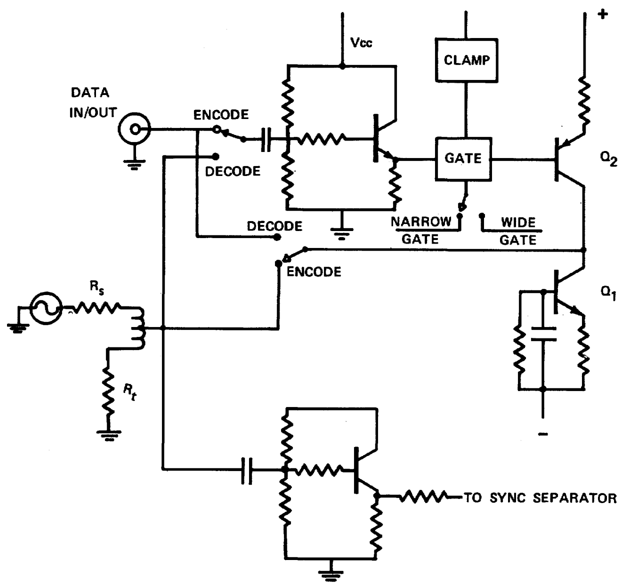

Fig. 5. Analog gate circuit.

the diode gate is closed, the digital information appearing at the base of $Q2$ causes $Q2$ to require more current. This is supplied through the terminating resistor (R_t) adding the digital information to the horizontal line that has been selected. The clamp is keyed from the counter circuit, so clamping is done on the back porch of the horizontal blanking.

The Decoding Process

If we put the encoder/decoder switch in the decode mode, the video signal now comes into the emitter–follower. The gate circuit is controlled by the wide gate; data are encoded from the horizontal line in the vertical interval and coupled into the data output jack. The remaining circuitry is controlled to allow operation of this gate either to add data to the vertical interval or to remove them.

What could happen to the video in the loopthrough path if the encoder malfunctions? You will notice that the system is capacitatively coupled. If $C1$ or $C2$ were to short, a high impedance remains parallel with the low impedance of the loopthrough.

The current adder maintains a high impedance even when the diode bridge is forward-biased (gate closed). R_t, the terminating resistor, is the load resistor and the current through it is determined by the unbalance in $Q1$ and $Q2$ when the digital signal is coupled to the base of $Q2$.

We should say more about how the digital information is actually added to this horizontal line. The generator source resistance, shown in the figure, should be as close to 75 Ω as possible to reduce reflection since the added signal energy tends to go both toward R_s and R_t. Tektronix has made us all aware of the importance of a return loss measurement; it is desirable that the return

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