

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Bendik, et al.
U.S. Patent No.: 5,591,678
Issue Date: January 7, 1997
Appl. Serial No.: 482,172
Filing Date: June 7, 1995
Title: PROCESS OF MANUFACTURING A MICROELECTRIC
DEVICE USING A REMOVABLE SUPPORT SUBSTRATE
AND ETCH-STOP

DECLARATION OF LEONARD W. SCHAPER

I, Leonard W. Schaper, of Naples, Florida, declare that:

1. I have been retained by counsel for Petitioner Samsung Electronics, Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (collectively, “Samsung” or “Petitioner”) to provide my independent analysis of the issues raised in the Petition for *inter partes* review of U.S. Patent No. 5,591,678 (“the ’678 Patent”).

2. I am not currently and have not at any time in the past been an employee of Samsung Electronics, Co., Ltd., Samsung Electronics America, Inc., or Samsung Semiconductor, Inc.

3. I am being compensated for my time expended in connection with this matter at the rate of \$500.00 per hour, plus reimbursement of any expenses I incur. I have no financial stake in this matter, and my compensation is not contingent upon the outcome of this *inter partes* review of the ’678 Patent.

I. QUALIFICATIONS AND PROFESSIONAL EXPERIENCE

4. I am an expert in the fields of semiconductor design, semiconductor fabrication, electronic packaging, and interconnect, among other fields.

5. I have 36 years of experience in the field of electronic packaging, including 12 years at AT&T Bell Laboratories from 1978-1990, where I was co-inventor of the silicon substrate multichip module technology known as Advanced VLSI Packaging (“AVP”). During the 1980s I served in various technology planning functions that required me to have extensive knowledge of the electronic packaging and interconnect fields.

6. I am Professor Emeritus of Electrical Engineering at the University of Arkansas where I also served as Director of the High Density Electronics Center. In that capacity, I have been responsible for over \$30 million in research grants and contracts covering many aspects of electronic packaging, including thermomechanical reliability of chip packaging.

7. I have taught graduate courses in electronic packaging, and I am a chapter author in Advanced Packaging with Emphasis on Multichip Modules (William D. Brown ed., Wiley-IEEE Press 1999), and Advanced Packaging, R.K. Ulrich and W.D. Brown, Eds., Wiley-IEEE Press, 2006.

8. I am a Fellow of the Institute of Electrical and Electronic Engineers (“IEEE”). I am the winner of the IEEE-CPMT (“Components, Packaging, and

Manufacturing Technology”) Society “Outstanding Sustained Technical Contributions” Award, as well as an ECTC (“Electronic Components and Technology Conference”) Outstanding Paper Award.

9. I am a Fellow and Life Member of the International Microelectronics and Packaging Society (“IMAPS”), and a past president of the International Electronics Packaging Society (“IEPS”), one of the societies that merged to form IMAPS. I am the 2002 winner of the IMAPS William D. Ashman Memorial Award “for outstanding contributions to the field of electronic packaging, particularly advanced in broad, module, and chip package power distribution and decoupling capacitor design, leading to higher performance system designs.”

10. I am an inventor of co-inventor of 21 U.S. patents and several foreign patents, all in the field of electronic packaging or optical communications.

11. Additional details regarding my qualifications and a listing of my publications are provided in my curriculum vitae, which is attached as Exhibit SAM1015 to this Petition. (“Schaper Curriculum Vitae”).

II. MATERIALS CONSIDERED

12. In writing this Declaration I have considered the following: my own knowledge and experience, including my work experience in the field of semiconductor design and fabrication, my industry experience in semiconductor

design and fabrication, and my experience in working with others involved in the field. In addition, I have analyzed the following publications and materials:

- U.S. Patent No. 5,591,678 and its accompanying prosecution file history (Ex. SAM1001 and Ex. SAM1011);
- U.S. Patent No. 5,347,154 (“Takahashi”) (Ex. SAM1005);
- U.S. Patent No. 4,599,792 (“Cade”) (Ex. SAM1006);
- U.S. Patent No. 5,002,818 (“Licari”) (Ex. SAM1008);
- U.S. Patent No. 4,601,779 (“Abernathey”) (Ex. SAM1007);
- U.S. Patent No. 4,975,126 (“Margail”) (Ex. SAM1014);
- R.B. Soper (*Mechanical Damage – Its Role in Silicon Surface Preparation*, Silicon Device Processing, Vol. 13 (Nov. 1970) (“Soper”) (Ex. SAM1009);
- Kurt E. Petersen (*Silicon as a Mechanical Material*, Proceedings of the IEEE, Vol. 70, No. 5 (May 1982) (“Petersen”) (Ex. SAM1010);
- H. Seidel, *Anisotropic Etching of Crystalline Silicon in Alkaline Solutions - I. Orientation Dependence and Behavior of Passivation Layers*, J. Electrochem. Soc., Vol. 137, No. 11 (1990) (“Seidel”) (Ex. SAM1012); and
- Ruzyllo, *Semiconductor Glossary*, (2004) (“Ruzyllo”) (Ex. SAM1013).

13. Although for the sake of brevity this Declaration refers to selected portions of the cited references, it should be understood that one of ordinary skill in the art would view the references cited herein in their entirety, and in combination

with other references cited herein or cited within the references themselves. The references used in this Declaration, therefore, should be viewed as being incorporated herein in their entirety.

III. PERSON OF ORDINARY SKILL IN THE ART

14. I am familiar with the content of the '678 Patent, which, I have been informed by counsel, has an earliest possible filing date of January 19, 1993 (hereinafter "the Priority Date").

15. Additionally, I have reviewed the other references cited above in this Declaration. Counsel has informed me that I should consider these materials through the lens of one of ordinary skill in the art related to the '678 Patent at the time of the invention. I believe one of ordinary skill around January 19, 1993 would have had either a (i) Bachelor of Science in Electrical Engineering with 5 years of experience in semiconductor design and manufacture, (ii) or a masters or Ph.D. degree in Electrical Engineering with equivalent experience in semiconductor design and manufacture.

A. *Grounds for Invalidating Patent Claims in an Inter Partes Review: 35 U.S.C. § 102 and/or 35 U.S.C. § 103*

16. I understand that the following restriction—which is set forth in 35 U.S.C. § 311(b)—limits an IPR petition to anticipation and obviousness grounds, using only prior art consisting of patents or printed publications. In other words, an IPR petitioner can only discuss whether another published prior art reference

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