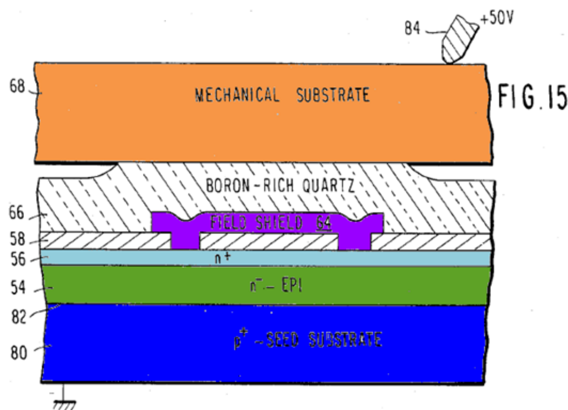
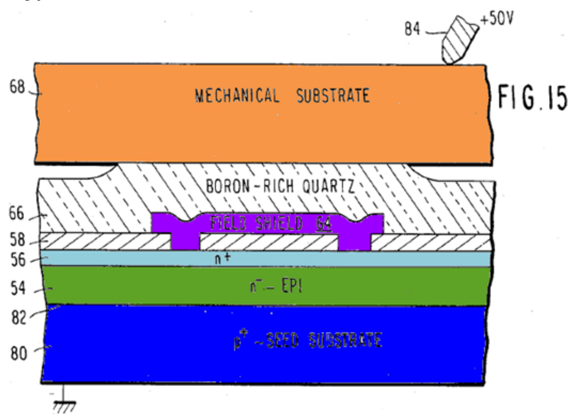
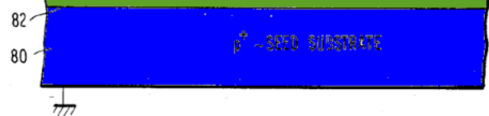
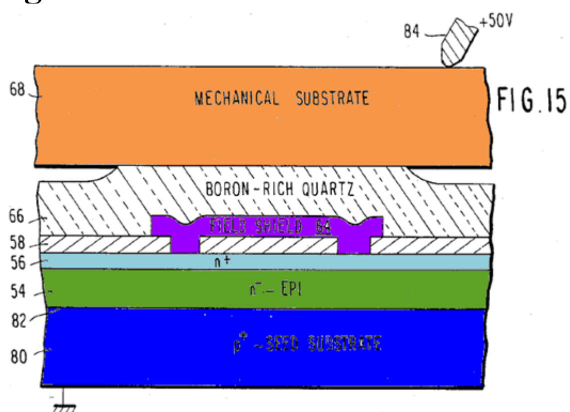
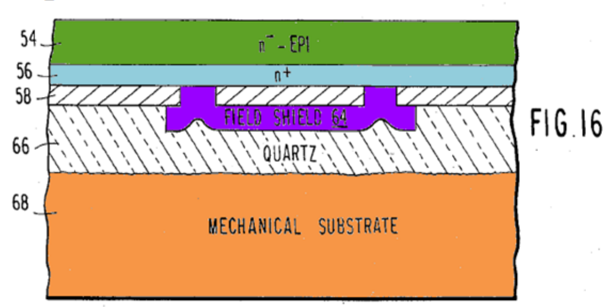
Claim 5	
The method of claim 1, wherein the etchable layer is silicon, the etch-stop layer is silicon dioxide, and the wafer is single-crystal silicon.	“A seed wafer 20, illustrated in FIG. 1, is prepared from a (100) silicon wafer 22.” **Cade, 2:55-56**. “Fabrication in the second embodiment begins with a heavily doped p+ seed substrate 80, shown in FIG. 15, on which is grown the n- epitaxial layer 54.” **7:4-6.** “Then the n+ emitter layer 56 and the thin dielectric layer 58 are grown just as in the first embodiment.” **7:10-12**. **Figure 15 of Cade**  “As shown in FIG. 1, an n- epitaxial layer 12 is formed on a p+ or N+0.008 ohm/cm silicon wafer 10.” **Abernathey, 3:40-41**. “A buried etch-stop layer 14 is then formed within epitaxial layer 12, separating epitaxial layer 12 into a first portion 12A overlaying the etch-stop 14 and a second portion 12B laying beneath the etch-stop 14.” **Abernathey, 3:59-62**. “In a preferred bonding technique as shown in FIG. 2, a layer of silicon dioxide 16A is grown on epitaxial portion 12A.” **Abernathey, 4:29-31**. “Any one of a number of known bonding techniques can be used to bond substrate 10 to a "mechanical" (i.e. physical support) wafer 100.” **Abernathey, 4:27-29**. **Figure 2 of Abernathey**

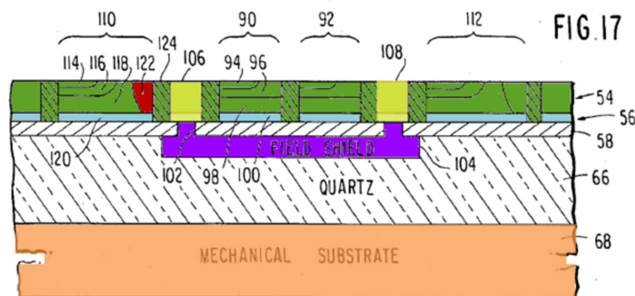
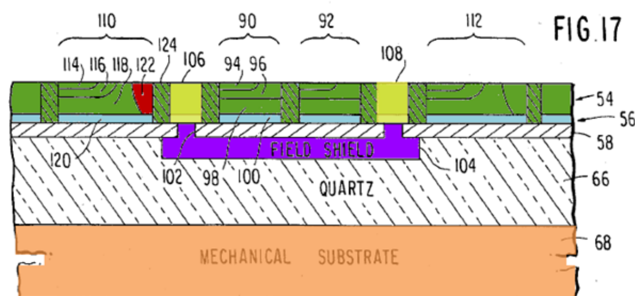
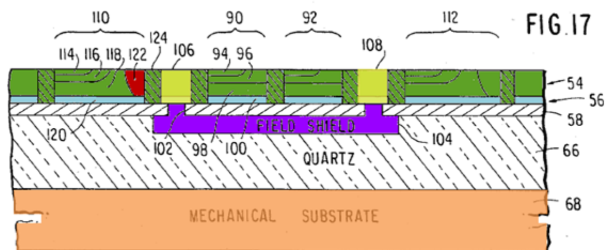
DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

Claim 13	
A method of fabricating a microelectronic device, comprising the steps of:	"The invention pertains generally to integrated circuits. In particular, it pertains to the fabrication of a buried field shield beneath other semiconductor devices on an integrated circuit chip." **Cade, 1:8-11**.
furnishing a first substrate having a silicon etchable layer, a silicon dioxide etch-stop layer overlying the silicon layer, and a single-crystal silicon wafer overlying the etch-stop layer, the wafer having a front surface not contacting the silicon dioxide layer;	"Fabrication in the second embodiment begins with a heavily doped p+ seed substrate 80, shown in FIG. 15, on which is grown the n- epitaxial layer 54." **7:4-6.** "Then the n+ emitter layer 56 and the thin dielectric layer 58 are grown just as in the first embodiment." **7:10-12**. **Figure 15 of Cade** 
forming a microelectronic circuit element in the front surface of the single-crystal silicon wafer;	"The field shield 64 and the boron-rich quartz 66 are likewise formed by similar procedures using the laser-scribed alignment marks for any required definition including possible definition of the emitter layer 56." **Cade, 7:24-27**. "It is anticipated that the n+ region 56 is delineated on top of the dielectric layer 58 so that devices, such as capacitors, can be fabricated using both the insulating layer 58 and the field shield 64 as constituent elements." **Cade, 7:64-68**. **Figure 15 of Cade**

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

	
attaching the front surface of the single-crystal silicon wafer to a first side of a second substrate; and	"The mechanical substrate 68 of silicon is then anodically bonded to the quartz 66 by applying voltage to a voltage probe 84 with the seed substrate 80 grounded." **Cade, 7:27-30**. **Figure 15 of Cade** 
etching away the silicon etchable layer down to the silicon dioxide etch-stop layer using an etchant that attacks the silicon layer but not the silicon dioxide layer.	"The etch-back of the seed substrate 80 is performed with hydrofluoric-nitric-acetic acid (HNA) in the proportions of 1:3:8. The etchant HNA is an isotropic etch and attacks heavily doped p+ or n+ silicon. However, it does not appreciably attack silicon doped below the level of 10^{18} /cm^3. The etch stopping characteristics are improved by the p+ /n junction at the interface 82." **Cade, 7:31-37**. **Figure 16 of Cade** 
Claim 14	
The method of claim 13, further including an additional-step, after the step of etching, of	**Figure 16 of Cade**

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

	Figure 17 of Cade 
Claim 15	
The method of claim 14, further including an additional step, after the step of patterning, of forming an electrical connection to the microelectronic circuit element through the patterned etch-stop layer and through the wafer.	"The field shield 104 is connected to the surface by field shield reach-throughs or contacts 106 and 108." **Cade, 8:15-17**. **Figure 17 of Cade** 
Claim 16	
The method of claim 14, further including an additional step, after the step of patterning, of forming an electrical connection to the wafer through the patterned etch-stop layer.	"A planar contact is made to the n epitaxial layer 18[sic][1] with an n+ layer 120 connected to the surface with a diffused n+ reach-through 122." **Cade, 8:20-22**. **Figure 17of Cade** 

[1] The reference number 18 to the n^- epitaxial layer is a typographical error. The n^- epitaxial layer should correspond to reference number 118, as seen in Figure 17.

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.