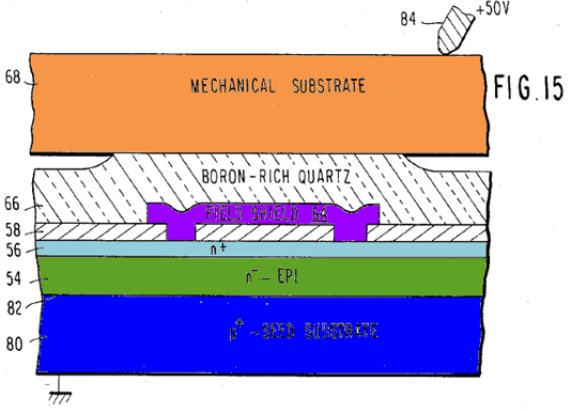
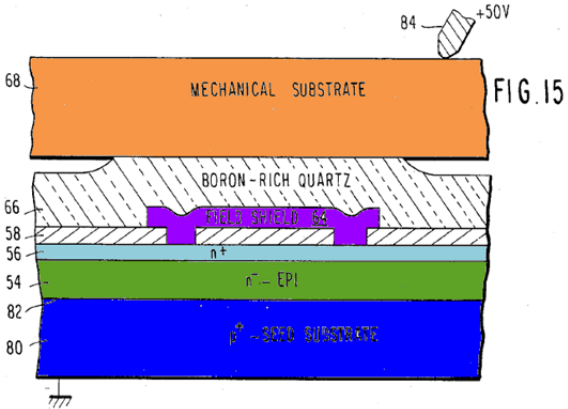


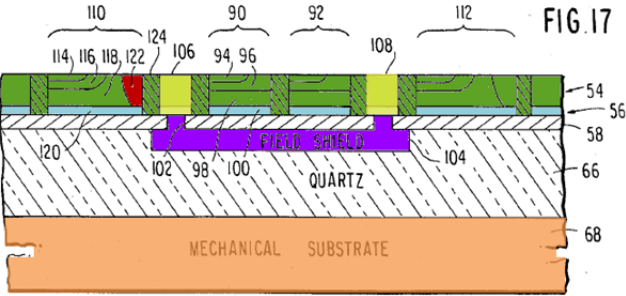
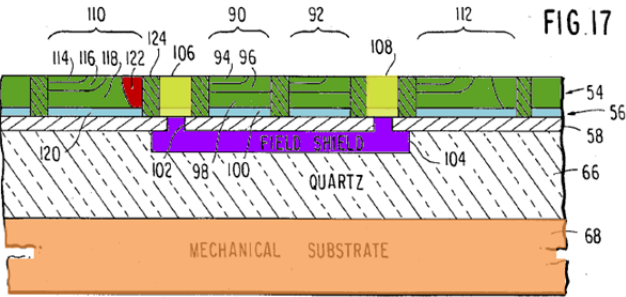
Cade anticipates claims 1-4 and 10 of U.S. Patent No. 5,591,678 to Bendik et al. (“the ’678 Patent”) under 35 U.S.C. § 102

Prior Art Cited in this Chart:

U.S. Patent No. 4,599,792 to Cade et al. (“Cade”)

Claim Language	Cade
Claim 1	
A method of fabricating a microelectronic device, comprising the steps of:	“The invention pertains generally to integrated circuits. In particular, it pertains to the fabrication of a buried field shield beneath other semiconductor devices on an integrated circuit chip.” 1:8-11.
furnishing a first substrate having an etchable layer, an etch-stop layer overlying the etchable layer, and a wafer overlying the etch-stop layer;	<p>“Fabrication in the second embodiment begins with a heavily doped p+ seed substrate 80, shown in FIG. 15, on which is grown the n- epitaxial layer 54.” 7:4-6.</p> <p>“Then the n+ emitter layer 56 and the thin dielectric layer 58 are grown just as in the first embodiment.” 7:10-12.</p> <p>Figure 15</p>
forming a microelectronic circuit element in the exposed side of the wafer of the first substrate opposite to the side overlying the etch-stop layer;	<p>“The field shield 64 and the boron-rich quartz 66 are likewise formed by similar procedures using the laser-scribed alignment marks for any required definition including possible definition of the emitter layer 56.” 7:24-27.</p> <p>“It is anticipated that the n+ region 56 is delineated on top of the dielectric layer 58 so that devices, such as</p>

Claim Language	Cade
	<p>capacitors, can be fabricated using both the insulating layer 58 and the field shield 64 as constituent elements.” 7:64-68.</p> <p>Figure 15</p> 
<p>attaching the wafer of the first substrate to a second substrate; and</p>	<p>“The mechanical substrate 68 of silicon is then anodically bonded to the quartz 66 by applying voltage to a voltage probe 84 with the seed substrate 80 grounded.” 7:27-30.</p> <p>Figure 15</p> 
<p>etching away the etchable layer of the first substrate down to the etch-stop layer.</p>	<p>“The etch-back of the seed substrate 80 is performed with hydrofluoric-nitric-acetic acid (HNA) in the proportions of 1:3:8. The etchant HNA is an isotropic etch and attacks heavily doped p+ or n+ silicon. However, it does not appreciably attack silicon doped below the level of 10^{18} /cm³. The etch stopping</p>

Claim Language	Cade
<p>further including an additional step, after the step of patterning, of forming an electrical connection to the microelectronic circuit element through the patterned etch-stop layer and through the wafer.</p>	<p>field shield reach-throughs or contacts 106 and 108.” 8:15-17.</p> <p>Figure 17</p> 
<p>Claim 4</p>	
<p>The method of claim 2, further including an additional step, after the step of patterning, of forming an electrical connection to the wafer through the patterned etch-stop layer.</p>	<p>“A planar contact is made to the n epitaxial layer 18[sic]¹ with an n+ layer 120 connected to the surface with a diffused n+ reach-through 122.” 8:20-22.</p> <p>Figure 17</p> 
<p>Claim 10</p>	
<p>The method of claim 1, wherein the step of etching includes the step of contacting the etchable layer to a liquid etchant that attacks the</p>	<p>“The etch-back of the seed substrate 80 is performed with hydrofluoric-nitric-acetic acid (HNA) in the proportions of 1:3:8. The etchant HNA is an isotropic etch and attacks heavily doped p+ or n+ silicon. However, it does not appreciably attack silicon doped below the level of 10¹⁸/cm³. The etch stopping</p>

¹ The reference number 18 to the n⁻ epitaxial layer is a typographical error. The n⁻ epitaxial layer should correspond to reference number 118, as seen in Figure 17.

Claim Language	Cade
etchable layer rapidly and the etch-stop layer slowly.	characteristics are improved by the p+ /n junction at the interface 82.” 7:31-37.