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Margail et al.

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[45] **Date of Patent: Dec. 4, 1990**

[54] **PROCESS FOR THE PRODUCTION OF AN INSULATING LAYER EMBEDDED IN A SEMICONDUCTOR SUBSTRATE BY IONIC IMPLANTATION AND SEMICONDUCTOR STRUCTURE COMPRISING SUCH LAYER**

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[21] Appl. No.: **207,379**

[22] Filed: **Jun. 15, 1988**

[30] **Foreign Application Priority Data**

Jun. 15, 1987 [FR] France 87 08272

[51] **Int. Cl.**[5] **H01L 21/265**

[52] **U.S. Cl.** **145/33.2**; 437/24; 437/25; 437/26; 437/84; 437/248

[58] **Field of Search** 437/24, 26, 82, 84, 437/247, 248, 25; 148/33, 33.2, 33.3

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[57] **ABSTRACT**

A process for the production of an insulator buried in a semiconductor substrate by ionic implantation, and semiconductor structure comprising such layer.

According to the invention the semiconductor structure comprises a silicon dioxide layer (**104**) interposed between a silicon substrate (**102**) and a silicon film (**106**) obtained by successive implantations of oxygen ions in the substrate, with doses less than $1.5 \cdot 10^{18}$ ions/cm^2, each implantation being followed by an annealing at a temperature higher than 1100° C. The semi-conductor film (**106**) has a level of dislocations lower than 10^5 per cm^2, and the oxide layer (**104**) is completely homogeneous.

12 Claims, 3 Drawing Sheets

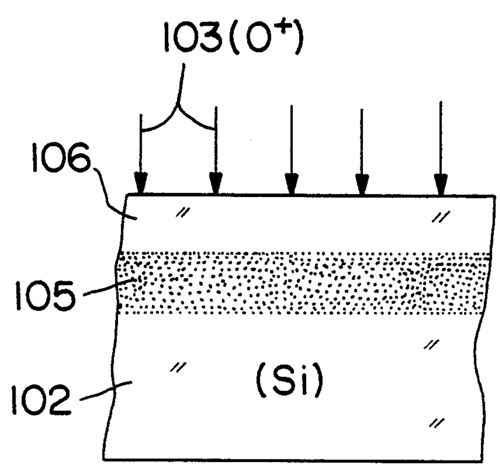


FIG. 1

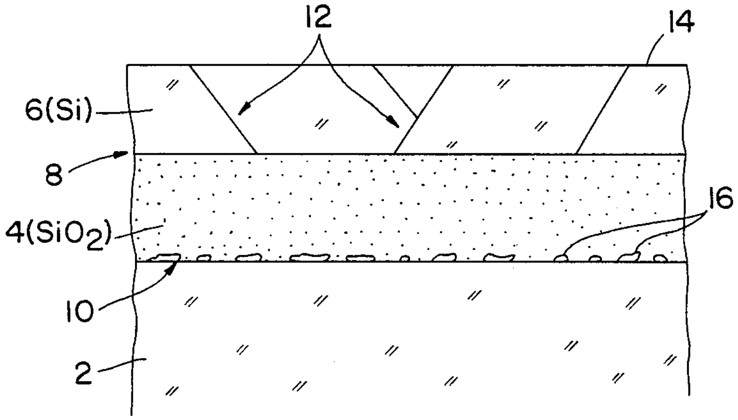


FIG. 3

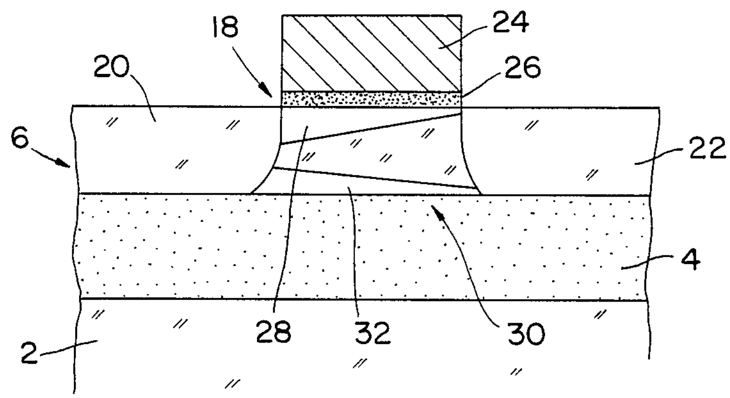


FIG. 2

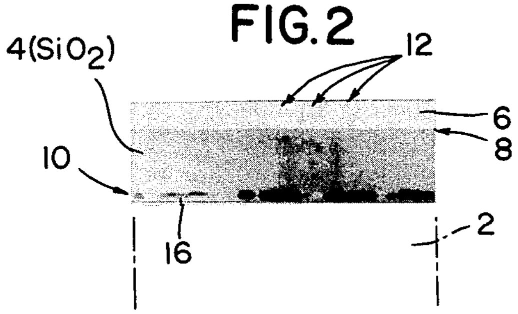
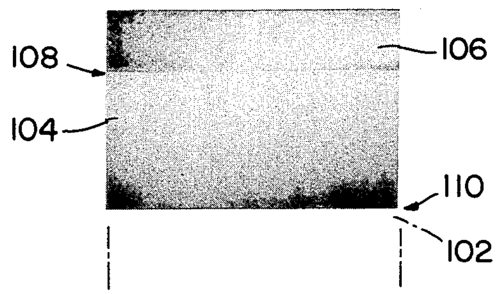


FIG. 5



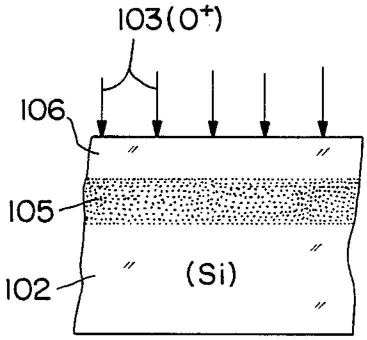


FIG.4a

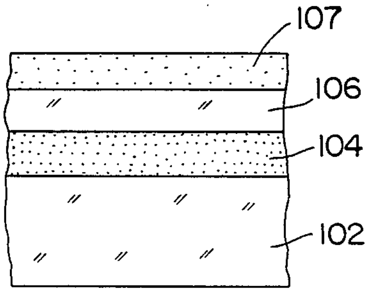


FIG.4b

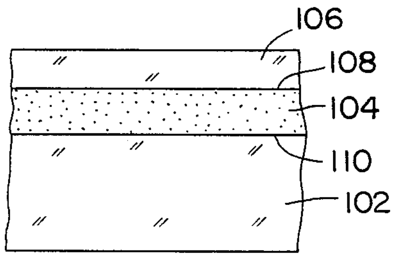


FIG.4c

PROCESS FOR THE PRODUCTION OF AN INSULATING LAYER EMBEDDED IN A SEMICONDUCTOR SUBSTRATE BY IONIC IMPLANTATION AND SEMICONDUCTOR STRUCTURE COMPRISING SUCH LAYER

DESCRIPTION

The invention relates to a process for the production of a continuous layer of oxide or nitride buried in a semiconductor substrate, by implantation of oxygen or nitrogen ions in the substrate, and also to semiconductor structures comprising such buried layer of oxide or nitride.

The invention relates more particularly to the production of MIS (metal/insulator/semiconductor) integrated circuits, CMOS (compatible metal/oxide/semiconductor) integrated circuits or bipolar circuits of the silicon-on-insulator type, which operate very quickly and are possibly highly resistant to ionizing radiations and must dissipate high powers. The invention also applies to the field of guided, possibly integrated optics, for the production of flat or stripe-type light guides.

Silicon-on-insulator technology represents a substantial improvement in the field of microelectronics in comparison with the standard techniques in which the active components of the integrated circuits are produced directly on a solid silicon monocrystalline substrate, since the use of an insulating support results in a considerable reduction in the stray capacity as between the source and the substrate on the one hand, and the drain and the substrate on the other, and reduces considerably the active components of the circuits, the result being an increase in the operating speed of such circuits.

Silicon-on-insulator technology also leads to an appreciable simplification of manufacturing processes, an increase in integration density, improved behaviour under high voltages, and low sensitivity to radiations, since the volume of monocrystalline silicon is low.

One of the silicon-on-insulator technologies at present known consists of implanting oxygen O^+ ions or nitrogen N^+ ions in heavy doses in solid monocrystalline silicon, so as to form, after high temperature annealing of the substrate, a buried insulating layer of silicon dioxide or silicon nitride. This process, known as the SIMOX process (separation by implanted oxygen) has formed the subject of a large number of publications.

In this respect the following may be cited: the article by P. L. F. Hemment "Silicon-on-insulator formed by O^+ or N^+ ion implantation", published in Mat. Res. Soc. Symp., vol. 53, 1986; the article by J. Stoemenos et al. "New conditions for synthesizing SOI structures by high dose oxygen implantation", published in the Journal of Crystal Growth 73 (1985) 546–550; the article by M. Bruel et al. "High temperature annealing of SIMOX layers", published in E. MRS. Strasbourg, June 1986, pp. 105–119; the article by J. Stoemenos et al., published in Appl. Phys. Lett. 48 (21), 26 May 1986, pp. **1470–1472**, entitled "SiO_2 buried layer formation by subcritical dose oxygen ion implantation" or the article by G. K. Celler et al. "High quality Si-ON-SiO_2 films by large dose oxygen implantation and lamp annealing", published in Appl. Phys. Lett. 48 (8), of 24 Feb. 1986, pp. 532–534.

FIG. **1** shows a semiconductor structure obtained by the SIMOX process in diagrammatical longitudinal section. The structure comprises a solid monocrystalline silicon substrate **2** surmounted by a silicon dioxide layer **4** coated with a monocrystalline silicon film **6**.

The Si/SiO_2 interface **8** is the monocrystalline film **6**, the dioxide layer **4** being referred to as the "front interface", the Si/SiO_2 **10** interface between the solid substrate **2** and the dioxide layer **4** being referred to as the "rear interface".

The standard conditions of the SIMOX technology for the formation of an oxide layer are: oxygen implantation doses of 1.6 to $2.5\cdot10^{18}O^+/cm^2$ ions, an implantation energy of 200 keV, a substrate heating during implantation to a temperature of between 500° and 700° C., then a high temperature annealing to complete the formation of the buried silica layer at temperatures of between 1150° to 1405° C. More particularly, annealing is performed at 1300° C. for 6 hours (cf. the above articles by Stoemenos and Bruel) or at 1405° C. for 30 minutes, as disclosed in the Celler article.

High temperature annealing induces a segregation of all the implanted oxygen towards the inside of the buried silicon dioxide layer. More particularly, the silicon film **6** surmounting the dioxide layer **4** no longer contains any oxide precipitate, as indicated in Bruel's article.

The widely used SIMOX process has some disadvantages. More particularly, the movement of oxygen or nitrogen ions into the silicon to a varying extent damages the monocrystalline silicon film **6**, creating often irreparable defects **12** (FIG. **1**). The defects are more particularly traversing dislocations anchored to the Si/SiO_2 interface **8**, passing through the silicon film **6** and coming out on the surface **14** thereof. Their density varies between 10^6 and $10^{10}/cm^2$.

FIG. **2**, which is a photograph of a semiconductor structure obtained by implanting oxygen ions with a dose of $1.6\cdot10^{18}$ ions/cm^2 in a silicon substrate heated to 600° C., the substrate then being annealed at 1300° C. for 6 hours, clearly shows the dislocations traversing the monocrystalline silicon film. This photograph is a microscopy by electronic transmission on edge.

These defects or dislocations of the silicon film cause a reduction in the preformances of the electric components subsequently produced in the semiconductor layer **6**, and can form, for example, the source of junction leaks, thus producing considerable leakage currents.

In the field of guided optics such dislocations disturb the light vehicled by the buried silica layer, causing light losses.

Moreover, the quality of the buried silicon dioxide layer is not perfect. More particularly, it has silicon islets **16** which are very troublesome, more particularly in microelectronics, since they reduce the voltage behaviour of the dioxide layer **4** and may be priviledged centres of charge trapping. Such silicon islets are clearly shown in FIG. **2**.

The presence of silicon islets or precipitates in the oxide layer is particularly troublesome in the case of MIS transistors produced in the semiconductor film **6**.

In this respect FIG. **3** shows a front transistor **18** comprising source **20** and a drain **22** respectively defined by implantation of n-type or p-type ions in the monocrystalline film **6**, and a grid **24**, generally consisting of polycrystalline silicon, surmounting the silicon film **6** and isolated therefrom by the grid oxide **26**. The channel **28** of the front transistor **18** is defined beneath

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