



CONTENTS

<u>Paper No.</u>		<u>Page No.</u>
1.	Welcoming Remarks Dr. Lewis M. Branscomb, Director, National Bureau of Standards	1
2.	Some Thoughts on How We Might Improve Our Materials and Process Work Dr. D. G. Thomas, Executive Director, Bell Telephone Laboratories	3
SESSION I - GENERAL, CHAIRMAN - D. E. KOONTZ		
3.	Crystallographic Imperfections as Related to Silicon Crystal Growth J. A. Lenard, IBM, Components Division	11
4.	A Review of Silicon Substrates Surface Preparation and Evaluation K. E. Lemons, Signetics Corporation Paper Withdrawn from Publication	-
5.	Epitaxial Growth of Silicon B. A. Joyce, Mullard Research Laboratories	19
6.	Diffusion in Silicon: Properties and Techniques C. F. Gibbon, Bell Telephone Laboratories, Inc.	21
7.	Measurement and Control of Dielectric Film Properties During Semiconductor Device Processing B. E. Deal, Fairchild Camera and Instrument	36
SESSION II-A - EPITAXY-TECHNIQUES AND FACILITIES, CHAIRMAN - J. W. CARLSON		
8.	Equipment Considerations for Silicon Epitaxy Reactors M. L. Hammond and W. P. Cox, Hugel Industries, Inc.	51
9.	A Comparison of a Resistance Heated Reactor for Silicon Epitaxial Growth With Other Epitaxial Systems W. A. Kohler, Fairchild Camera and Instrument Corp.	60
10.	Techniques for Depositing Highly Uniform and Defect-Free Epitaxial Silicon D. C. Gupta, The Waltham Research Center of the General Telephone and Electronics Laboratories, Inc. and J. L. Porter, Sylvania Electric Products, Inc.	66
11.	Control of Thin Silicon Films Grown From Silane D. J. Dumin, RCA Laboratories	79
12.	The Growth of Submicron Single and Multilayer Silicon Epitaxy J. Simpson, A. C. Adams and M. H. Hanes, Bell Telephone Laboratories, Inc.	87
SESSION II-B - DIFFUSION-PROPERTIES CHARACTERISTICS, CHAIRMAN - E. E. GARDNER		
13.	Techniques for Determining Surface Concentration of Diffusants J. C. Irvin, Bell Telephone Laboratories	99
14.	Current Status of the Spreading Resistance Probe and Its Application T. H. Yeh, IBM Components Division	111
15.	Incremental Sheet Resistivity Technique for Determining Diffusion Profiles R. P. Donovan and R. A. Evans, Research Triangle Institute	123
16.	Nuclear Methods for the Determination of Diffusion Profiles B. J. Masters, IBM Components Division	132
17.	Use of High-Energy Ion Beams for Analysis of Doped Surface Layers S. L. Chou, L. A. Davidson and J. F. Gibbons, Stanford Electronics Laboratories	141

<u>Paper No.</u>		<u>Page No.</u>
18.	Determination of Diffusion Coefficients in Silicon and Accepted Values M. F. Millea, Aerospace Corporation	156
	SESSION III-A - DIFFUSION-TECHNIQUES AND FACILITIES, CHAIRMAN - F. L. GITTLER	
19.	Diffusion Technology For Advanced Microelectronic Processing W. Greig, K. Cunniff, H. Hyman and S. Muller, RCA Solid State Division	168
20.	Diffusion From Doped-Oxide Sources M. L. Barry, Fairchild Camera and Instrument Corporation	175
21.	Capacitance-A Device Parameter and Tool for Measuring Doping Profiles B. R. Chawla, Bell Telephone Laboratories, Inc.	182
22.	Concentration Dependent Diffusion Phenomena P. E. Bakeman, Jr., Rensselaer Research Corporation and J. M. Borrego, Rensselaer Polytechnic Institute	184
23.	Orientation Dependent Diffusion Phenomena L. E. Katz, Bell Telephone Laboratories, Inc.	192
24.	Diffusion Inducted Defects and Diffusion Kinetics in Silicon M. L. Joshi, IBM, Components Division and S. Dash, Fairchild Semiconductor	202
	SESSION III-B - EPITAXY-PROPERTIES AND CHARACTERISTICS, CHAIRMAN - D. C. GUPTA	
25.	Limitations of Current Epitaxial Evaluations (Abstract Only) R. N. Tucker, Fairchild Semiconductor. Paper Withdrawn from Publication	223
26.	On the Interpretation of Some Measurement Methods for Epitaxially Grown Layers P. J. Severin, Philips Research Laboratories	224
27.	Thickness Measurement of Very Thin Epitaxial Layers by Infrared Reflectance P. A. Schumann, Jr., IBM Components Division	234
28.	Spreading Resistance Measurements on Buried Layers in Silicon Structures R. G. Mazur, Westinghouse Research Laboratories	244
29.	Variations of a Basic Capacitance-Voltage Technique for Determination of Impurity Profiles in Semiconductors W. C. Niehaus, W. vanGelder, T. D. Jones and P. Langer, Bell Telephone Laboratories	256
31.	Structural Faults in Epitaxial and Buried Layers in Silicon in Device Fabrication P. Wang, F. X. Pink and D. C. Gupta, General Telephone and Electronics Laboratories	285
32.	An Instrument for Automatic Measurement of Epitaxial Layer Thickness A. C. Roddan, Beckman Instruments, Inc. and V. Vizir, Fairchild Semiconductor	302
30.	A New Impurity Profile Plotter for Epitaxy and Devices B. J. Gordon and H. L. Stover, University of Southern California and R. S. Harp, California Institute of Technology	273
	SESSION IV-A - INTERDEPENDENCE OF UNIT PROCESSING OPERATIONS, CHAIRMAN - J. OROSHNIK	
33.	A Statistical Approach to the Design and Fabrication of Diffused Junction Transistors D. P. Kennedy, IBM, Components Division Previously published in IBM J. of R and D <u>8</u> , 482 (1964)	-
34.	Defects Induced in Silicon Through Device-Processing M. L. Joshi and J. K. Howard, IBM, Components Division	313
35.	A Study Relating MOS Processes to a Model of the Al-SiO <sub>2</sub> -Si System M. H. White, F. C. Blaha and D. S. Herman, Westinghouse Corporation	365

<u>Paper No.</u>		<u>Page No.</u>
36.	Activation Analysis in Silicon Device Processing G. B. Larrabee and H. G. Carlson, Texas Instruments, Inc.	375
37.	The Use of the Scanning Electron Microscope as a Semiconductor Device Production Line Quality Control Tool J. W. Adolphsen and R. J. Anstead, NASA Goddard Space Flight Center.	384
38.	Metallization Deposition Parameters and Their Effect on Device Performance J. R. Black, Motorola, Inc.	398
39.	Methods for Determination of the Characteristics of Hyper-pure Semiconductor Silicon and Their Information Content for Device Production Fritz G. Vieweg-Gutberlet, Wacker Chemitronic GMBH	409
SESSION IV-B - SURFACE PREPARATION, CHAIRMAN - E. MENDEL		
40.	Mechanical Damage-Its Role in Silicon Surface Preparation R. B. Soper, Semiconductor Processing Co., Inc.	412
41.	Crystallographic Damage to Silicon By Typical Slicing, Lapping, and Polishing Operations T. M. Buck and R. L. Meek, Bell Telephone Laboratories	419
42.	The Preparation of Practical, Stabilized Surfaces for Silicon Device Fabrication A. Mayer and D. A. Puotinen, RCA Corporation	431
43.	Surface Contamination J. W. Faust, Jr., University of South Carolina	436
44.	The Precipitation of Oxygen in Silicon and Its Effect on Surface Perfection W. J. Patrick, IBM, Components Division	442
45.	Auger Spectroscopy and Silicon Surfaces J. H. Affleck, General Electric Company	450
46.	Characterization of Semiconductor Surfaces and Interfaces by Ellipsometry N. M. Bashara, University of Nebraska	457

## Mechanical Damage - Its Role in Silicon Surface Preparation

R. B. Soper

Semiconductor Processing Co., Inc.  
Hingham, Mass. 02043

Silicon is mechanically damaged during the centerless grinding, slicing, lapping and mechanical polishing operations used to shape the ingot into wafers. Surface damage, removed by chemical processes and peripheral defects such as conchoidal fractures, indents, and microcracks are discussed. A comparison of various polishing methods and how they relate to mechanical damage is given.

**Key Words:** Centerless grinding, etching, lapping, mechanical damage, peripheral damage, polishing, silicon, slicing, surface damage, surface preparation.

### 1. Introduction

The silicon surface quality sufficient for the manufacture of different devices varies widely; for instance, a simple diode may require only a surface obtained from the free etching of a sawn slice, whereas the slice used for the vidicon image tube should be of precise diameter, polished on both sides, free of any peripheral or surface damage, thin (four to six mils), flat and parallel.

To prepare the high quality silicon surface required for today's sophisticated devices, consideration must be given to the damage created by the necessary abrasive operations such as centerless grinding, orientation flat generation, slicing and lapping. Operations such as polarity probing, resistivity measurements, thickness measurement and handling with tweezers can also cause thermal or impact damage to the silicon surface. Abrasive, thermal and impact damage is best removed by chemical processes. The final polishing operation should leave the surface as damage-free as possible.

In the last decade mechanical damage induced in semiconductor materials has been investigated by many workers. (1-10)<sup>1</sup> There has been a difference in the depths of damage reported by different workers because of the variables involved in the abrasive operations and in the techniques used to determine the depth of the damaged layer. These points will be further discussed by others at this meeting.

The primary concern of this paper will be the damage created at the periphery of the wafer and how it can be controlled.

### 2. Peripheral Damage

Below is a description of the different types of mechanical damage which is located or is generated at the periphery of the wafer.

**Conchoidal Fracture** - A conchoidal fracture is a spalled flake of silicon. It may be shallow or deep, and multiple fractures may be on both sides of the wafer. In some cases partial spalling results due to incomplete fracturing.

**Indent** - An indent fracture is any irregularity from the normal profile of the wafer. It may be bounded by crystallographic planes or be random in shape.

**Microcrack** - A microcrack is a minor break which does not involve any appreciable separation of silicon. The depth usually penetrates the entire thickness of the wafer. The break normally follows a crystallographic plane, but the initiating force can be directed so as to yield a multi-directional break.

<sup>1</sup> Figures in brackets indicate the literature references at the end of this paper.

# Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

## Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

## Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

## Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

## API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

## LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

## FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

## E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.