# United States Patent [19]

**Abernathey et al.**

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[54] **METHOD OF PRODUCING A THIN SILICON-ON-INSULATOR LAYER**


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[51] **Int. Cl.**[4] ..... **H01L 21/306**; B44C 1/22; C03C 15/00; C03C 25/06

[52] **U.S. Cl.** ..... **156/628**; 29/576 B; 29/576 E; 148/1.5; 148/175; 156/630; 156/633; 156/643; 156/646; 156/645; 156/657; 156/662; 204/192 E; 204/192 N; 252/79.1; 252/79.3; 252/79.5; 427/85; 427/86

[58] **Field of Search** ..... 29/571, 576 E, 576 B, 29/576 R; 148/1.5, 175; 204/192 EC, 192 E, 192 N; 427/85, 86, 93, 94, 95; 156/628, 630, 633, 643, 646, 645, 657, 662; 252/79.1, 79.3, 79.5



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[57] **ABSTRACT**

A method of forming a thin silicon layer upon which semiconductor devices may be constructed. An epitaxial layer is grown on a silicon substrate, and oxygen or nitrogen ions are implanted into the epitaxial layer in order to form a buried etch-stop layer therein. An oxide layer is grown on the epitaxial layer, and is used to form a bond to a mechanical support wafer. The silicon substrate is removed using grinding and/or HNA, the upper portions of the epitaxy are removed using EDP, EPP or KOH, and the etch-stop is removed using a non-selective etch. The remaining portions of the epitaxy forms the thin silicon layer. Due to the uniformity of the implanted ions, the thin silicon layer has a very uniform thickness.


**27 Claims, 6 Drawing Figures**

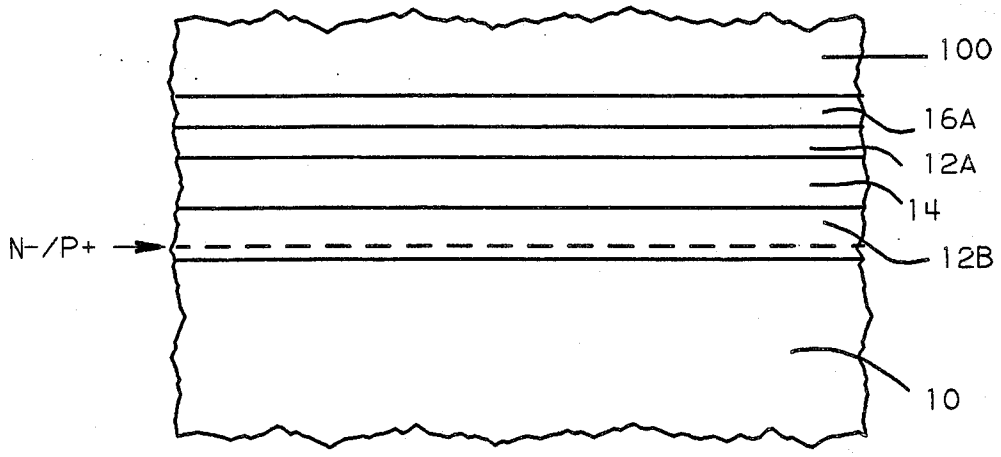


FIG. 1

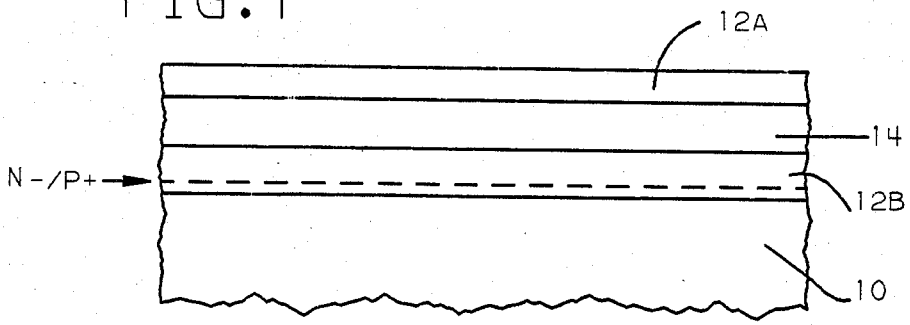



FIG. 2

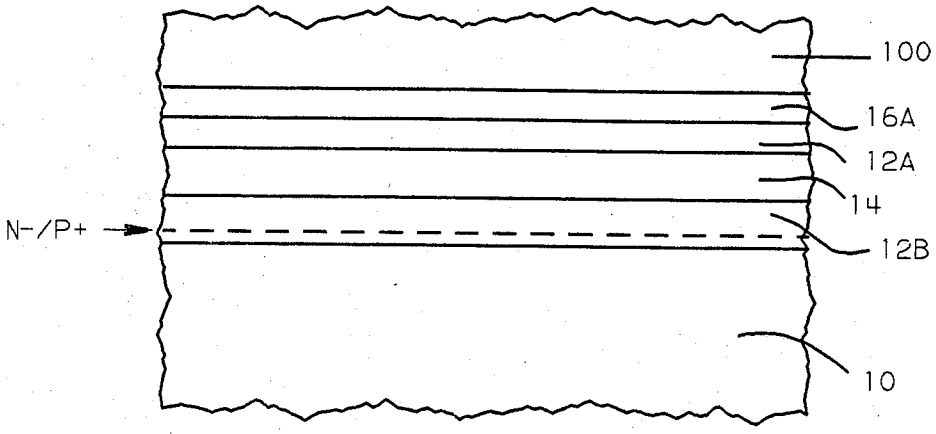



FIG. 3

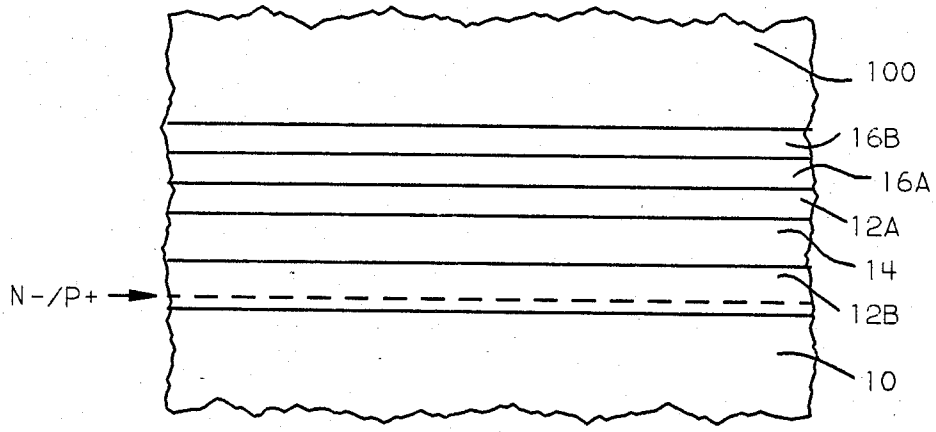


FIG. 4

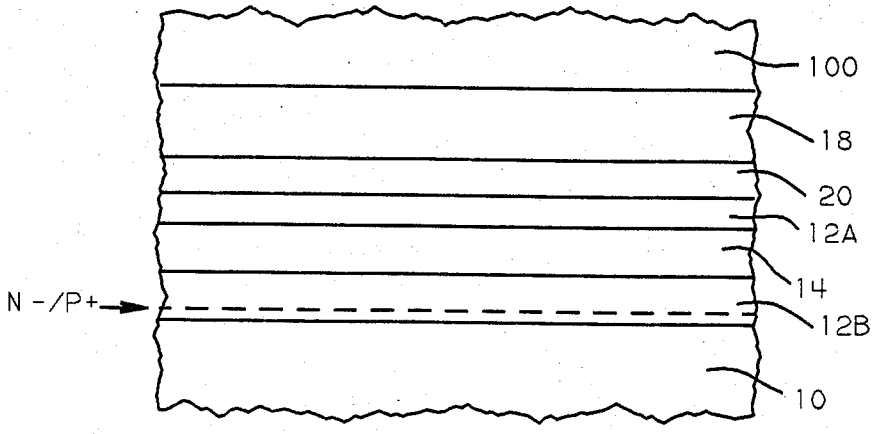



FIG. 5

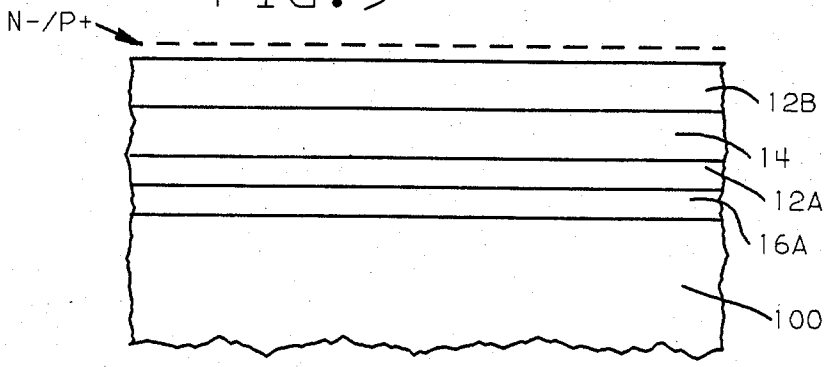
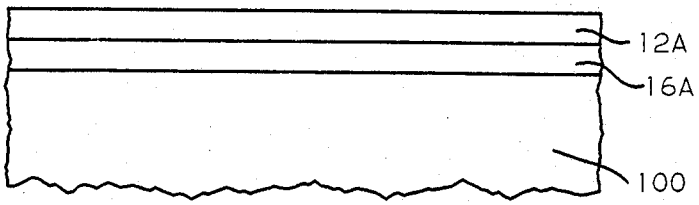



FIG. 6



# METHOD OF PRODUCING A THIN SILICON-ON-INSULATOR LAYER

## CROSS-REFERENCE TO RELATED APPLICATIONS

Reference is made to co-pending U.S. patent application, Ser. No. 625,758, filed June 28, 1984, entitled "Silicon-on-Insulator Transistors With a Shared Element", by Abernathey et al and assigned to the assignee of the present invention. This application discloses and claims a method of forming devices upon a silicon-on-insulator structure.

## TECHNICAL FIELD

The present invention relates to a method of forming a silicon-on-insulator structure.

## BACKGROUND ART

In the present era of very large scale integration (VLSI), in which the dimensions of transistors and other semiconductor structures are shrinking below one micrometer, a host of new problems must be addressed. In general, greater isolation is required between devices. For CMOS applications, this isolation must prevent latch-up. At the same time, this increased isolation must not be provided at the expense of available chip space.

Silicon-on-insulator technology appears to be a particularly promising method of addressing this problem. A general example of this technology is shown in the article by R. J. Lineback, "Buried Oxide Marks Route to SOI Chips", *Electronics Week,* Oct. 1, 1984, pp. 11–12. As shown in this article, oxygen ions are implanted into a bulk silicon to form a buried oxide layer therein. The implant is then annealled for two hours so that the portion of the silicon lying above the buried oxide is single-crystal silicon. The various semiconductor devices are then formed on the single-crystal layer. The underlying buried oxide provides isolation between adjacent devices.

More recently, a specific method of forming silicon-on-insulator structures has evolved, in which two silicon substrates are bonded together and one of the substrates is at least partially removed. An example of this method is disclosed in an article by M. Kimura et al, "Epitaxial Film Transfer Technique for Producing Single Crystal Si Film on an Insulating Substrate", *Applied Physics Letters,* Vol. 43, No. 3, Aug. 1, 1983. As described in this article, a first p+ substrate has a P− epitaxial layer grown thereon. A second substrate has a layer of oxide grown thereon. Both substrates are then coated with a glass, and the two substrates are bonded together using these glass layers. More specifically, the glass layers of the two substrates are pressed together and are heated to about 930° C. After the substrates are bonded together, the substrate having the epitaxial layer is removed, leaving behind the epitaxial layer on the bonded glass layers. The glass layers provide insulation. See also the article by Brock et al, "Fusing of Silicon Wafers", *IBM Technical Disclosure Bulletin,* Vol. 19, No. 9, February 1977, pp. 3405–3406, in which it is stated that "wafers may be fused together conveniently by forming a layer of silicon dioxide on each wafer, then placing the layers of silicon dioxide abutting each other, and heating, preferably in a steam atmosphere at a temperature in the order of 1050° C. for about one-half hour."

U.S. Pat. No. 4,142,925 (issued 3/3/79 to King et al) discloses a method of making a structure which includes an epitaxial layer, an insulator layer and a polished silicon layer. As shown in the front figure of the patent, an epitaxial layer is grown on an n+ silicon substrate. An insulator layer of $SiO_2$ is grown on the epitaxial layer, and the insulator is covered with a polysilicon support layer. The n+ silicon substrate is then removed, leaving the epitaxial layer atop the $SiO_2$ layer.

It has been found that the step of removing the silicon substrate without removing the underlaying epitaxial layer is facilitated if these two layers have different doping concentrations or are of different conductivity types. For example, if the substrate is p+ and the epitaxial layer is p− or n type, the substrate may be removed by etching in a 1:3:8 solution of hydroflouric, nitric and acetic ("HNA") acid.

A problem with the above process is that the HNA acid will etch to the p+/p− or p+/n junction, which does not occur at the actual physical interface of these two layers. For example, in order to form a final n epitaxial layer of 200 nm (nanometers) on a p+ substrate, an epitaxial layer of 1000–1200 nm must be deposited. This is because boron will out-diffuse from the substrate into the epitaxial layer, such that the p+/n junction actually occurs at a point approximately 800–1000 nm, respectively, above the physical interface between the substrate and the epitaxial layer.

Forming a 1000–1200 nm layer of epitaxy leads to another problem. Typically, when working in the nm range, the deposition tools used in the industry can deposit a layer with approximately plus or minus 5 percent error. Thus, if the original epitaxial layer is 1000 nm thick, the final epitaxial layer (i.e. after removal of the p+ substrate) will be approximately 250±50 nm thick. When the dopant concentration of the epitaxial layer is sufficiently low, the depletion regions of the channels of FETs subsequently formed on the epitaxial layer will extend to the bottom of the layer. Hence, the threshold voltages of these FETs are at least partially determined by the thickness of the epitaxial layer, such that the above variation in thickness would lead to an unacceptable variation in the threshold voltages of the FETs. Obviously, as the thickness of the epitaxial layer as initially deposited is increased, the resultant thickness variation increases. For example, if the initial epitaxial thickness is 2500 nm, its final thickness would be approximately 250±150 nm.

## SUMMARY OF THE INVENTION

It is thus an object of the present invention to provide an improved silicon-on-insulator fabrication process.

It is another object of the invention to provide a silicon-on-insulator process by which the thickness of the final silicon layer is substantially uniform.

It is yet another object of the invention to provide an improved silicon-on-insulator fabrication process in which the etching of the final silicon layer may be more precisely controlled.

These and other objects of the invention are realized in a process of forming a relatively thin silicon-on-insulator structure having a uniform thickness. After a thin epitaxial layer is formed on a silicon substrate, ions are implanted into the epitaxial layer in order to form a thin buried etch-stop layer therein. The buried layer has etching characteristics which differ from those of the

epitaxial layer. After bonding the epitaxial layer to a mechanical substrate, the silicon substrate and portions of the epitaxial layer overlaying the buried layer are removed. Subsequently, the remainder of the epi layer above the buried layer is removed in an etchant which does not appreciably attack the buried layer. The buried layer is then removed.

The remaining epitaxial layer has a substantially uniform thickness. This is due to the uniformity of the buried layer, which is in turn due to the uniform concentration of ions achieved during ion implantation.

## BRIEF DESCRIPTION OF THE DRAWING

The foregoing and other structures and teachings of the present invention will become more apparent upon a detailed description of the best mode for carrying out the invention as rendered below. In the description to follow, reference will be made to the accompanying drawing, in which:

FIG. **1** is a cross-sectional view of a silicon substrate having an epitaxial layer and a buried etch stop layer;

FIG. **2** is a cross-sectional view of the substrate of FIG. **1** bonded to a mechanical support utilizing a first bonding technique substrate;

FIG. **3** is a cross-sectional view of the substrate of FIG. **1** bonded to a mechanical support substrate utilizing a second bonding technique;

FIG. **4** is a cross-sectional view of the substrate of FIG. **1** bonded to a mechanical support substrate utilizing a third bonding technique;

FIG. **5** is a cross-sectional view of the mechanical support substrate with the first substrate removed; and

FIG. **6** is a cross-sectional view of the second substrate as shown in FIG. **5** with the overlaying portions of the epitaxial layer and the buried etch stop layer removed.

## BEST MODE FOR CARRYING OUT THE INVENTION

As shown in FIG. **1**, an n− epitaxial layer **12** is formed on a p+ or N+0.008 ohm/cm silicon wafer **10**. The epitaxial layer **12** is grown using conventional deposition gases such as $SiH_2Cl_2$, $SiH_4$, $SiCl_4$ or $SiHCl_3$. Preferably, $SiH_2Cl_2$ is used at 1050°–1080° C. The resulting epitaxial layer can be relatively thick (e.g. 2500 nm). This is because the initial thickness of the epitaxial layer has minimal bearing upon the final thickness of the silicon-on-insulator structure, as will be described in more detail below. Note that the dopant concentration of substrate **10** should be $6\times10^{18}$ ions/cm$^3$ or greater, $1\times10^{19}$ being a typical choice. Such a concentration is necessary for this substrate to be etched in HNA. When the epitaxial layer **12** is formed on substrate **10**, boron will outdiffuse from the substrate such that a p+/n− junction will be established within epitaxial layer **12**. The boron atoms penetrate into the epitaxy to form the junction at approximately 400–800 nm above the physical epitaxy-substrate interface.

A buried etch-stop layer **14** is then formed within epitaxial layer **12**, separating epitaxial layer **12** into a first portion **12A** overlaying the etch-stop **14** and a second portion **12B** laying beneath the etch-stop **14**. In general, buried layer **14** can be comprised of any element which has etch characteristics that are appreciably different from those of the epitaxial layer **12**. For example, buried layer **14** can be formed implanting oxygen ions at a dose of $1\times10^{16}$–$1\times10^{18}$ O+ ions/cm$^2$ at 160 kev into the substrate, with the substrate being heated to approximately 500° C. The substrate is heated during implantation in order to minimize damage in the portion **12A** of epitaxial layer **12** overlaying the buried ions. If oxygen ions are implanted, a buried layer of silicon oxide is formed. Note that nitrogen ions could also be used to form a buried layer of silicon nitride. In addition, carbon ions could be implanted to form a buried layer of silicon carbide. The dosage is one factor determining the "effectiveness" of the etch-stop. Specifically, the higher the dosage, the more effective the etch stop and hence the more planar the resulting epitaxial layer upon subsequent etching. This property will be discussed in more detail later. As the dosage increases, a thinner portion of region **12A** is left free of defects. Doses of $4\times10^{16}$ ions/cm$^2$ and $1\times10^{17}$ ions/cm$^2$ have produced good results, with the latter being preferred. Finally, the implantation energy also affects the position of the ions within epitaxial layer **12**. In general, implantation energies of 80 kev and up (160 kev being preferred) can be used.

Since buried layer **14** is formed by implantation, it has a thickness which is substantially uniform due to the minimal deviation of the implant energy. In addition, layer **14** is relatively planar (i.e. the upper surface of layer **14** is buried below the exposed surface of the epi layer at the same depth across the entire wafer).

Any one of a number of known bonding techniques can be used to bond substrate **10** to a "mechanical" (i.e. physical support) wafer **100**. In a preferred bonding technique as shown in FIG. **2**, a layer of silicon dioxide **16A** is grown on epitaxial portion **12A**. The thickness of this oxide layer **16A** can vary in the range of approximately 10–2000 Å, with the upper limit being the amount of epitaxial portion **12A** consumed during oxide growth. Preferably, $SiO_2$ **16A** is 450 Å in thickness, and is grown in an oxygen ambient at approximately 800° C. Alternatively, $SiO_2$ may be pyrolytically deposited upon epitaxial portion **12A**, eliminating silicon consumption. In either case, the oxide layer **16A** is then bonded to the mechanical wafer **100** by contact in a steam ambient and heating to a temperature within the range of 700°–1200° C. (preferably 900° C.) for approximately 50 minutes.

In another bonding technique as shown in FIG. **3**, an oxide layer **16B** of any thickness (e.g. up to 20,000 Å) is grown on mechanical substrate **100** prior to bonding. Thus, the oxide layers **16A** and **16B** bond together, forming a very thick oxide layer. Such a thick oxide may be advantageous in high voltage applications.

In yet another technique as shown in FIG. **4**, a reflowable glass such as borosilicate glass (BSG) or borophosphosilicate glass (BPSG) layer **18** is used instead of silicon dioxide. When the glass is deposited on epitaxial portion **12A**, it is advisable to first deposit a 50–1000 Å (typically 200 Å) thick layer of silicon nitride **20**. The nitride will prevent outdiffusion of impurities from the glass into epitaxial portion **12A** during subsequent high temperature processing. Note that when bonding takes place, the bonding temperature must be above the glass transition temperature. For example, using a 4:4:92 BPSG layer of 0.4 $\mu$m thickness, bonding is carried out in a steam atmosphere at approximately 900° C. Alternatively, a layer of reflowable glass could also be formed on the mechanical substrate **100**.

After any of the above bonding operations, p+ substrate **10** is removed to expose epitaxial portion **12B**. The resulting structure is shown in FIG. **5**. One removal method is to grind or lap (or otherwise mechani-

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