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Bendik et al.

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[45] **Date of Patent: Jan. 7, 1997**

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[54] PROCESS OF MANUFACTURING A MICROELECTRIC DEVICE USING A REMOVABLE SUPPORT SUBSTRATE AND ETCH-STOP

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[21] Appl. No.: **482,172**

[22] Filed: **Jun. 7, 1995**

Related U.S. Application Data

[63] Continuation of Ser. No. 6,120, Jan. 19, 1993, abandoned.

[51] **Int. Cl.**^{6} **H01L 21/283**; H01L 21/56; H01L 21/58; H01L 21/60

[52] **U.S. Cl.** **437/208**; 437/974; 437/915; 148/DIG. 135; 148/DIG. 150; 156/662.1; 156/630.1

[58] **Field of Search** .... 437/208, 974, 437/915; 148/DIG. 135, DIG. 150; 156/630, 662, 901

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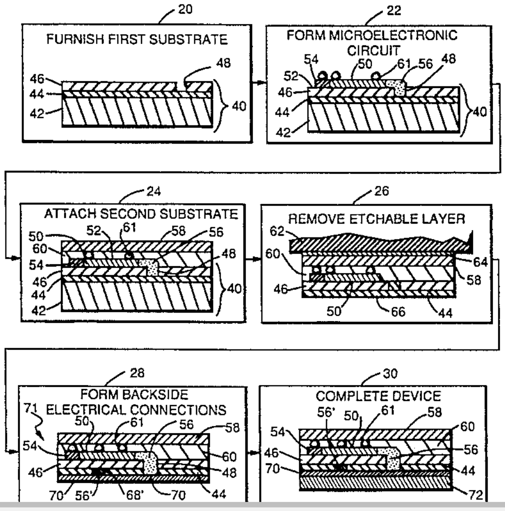
[57] ABSTRACT

A microelectronic device is fabricated by furnishing a first substrate (**40**) having a silicon etchable layer (**42**), a silicon dioxide etch-stop layer (**44**) overlying the silicon layer (**42**), and a single-crystal silicon wafer (**46**) overlying the etch-stop layer (**44**), the wafer (**46**) having a front surface (**52**) not contacting the etch stop layer (**44**). A microelectronic circuit element (**50**) is formed in the single-crystal silicon wafer (**46**). The method further includes attaching the front surface (**52**) of the single-crystal silicon wafer (**46**) to a second substrate (**58**), and etching away the silicon layer (**42**) of the first substrate (**40**) down to the etch-stop layer (**44**). The second substrate (**58**) may also have a microelectronic circuit element (**58'**) therein that can be electrically interconnected to the microelectronic circuit element (**50**).

18 Claims, 2 Drawing Sheets



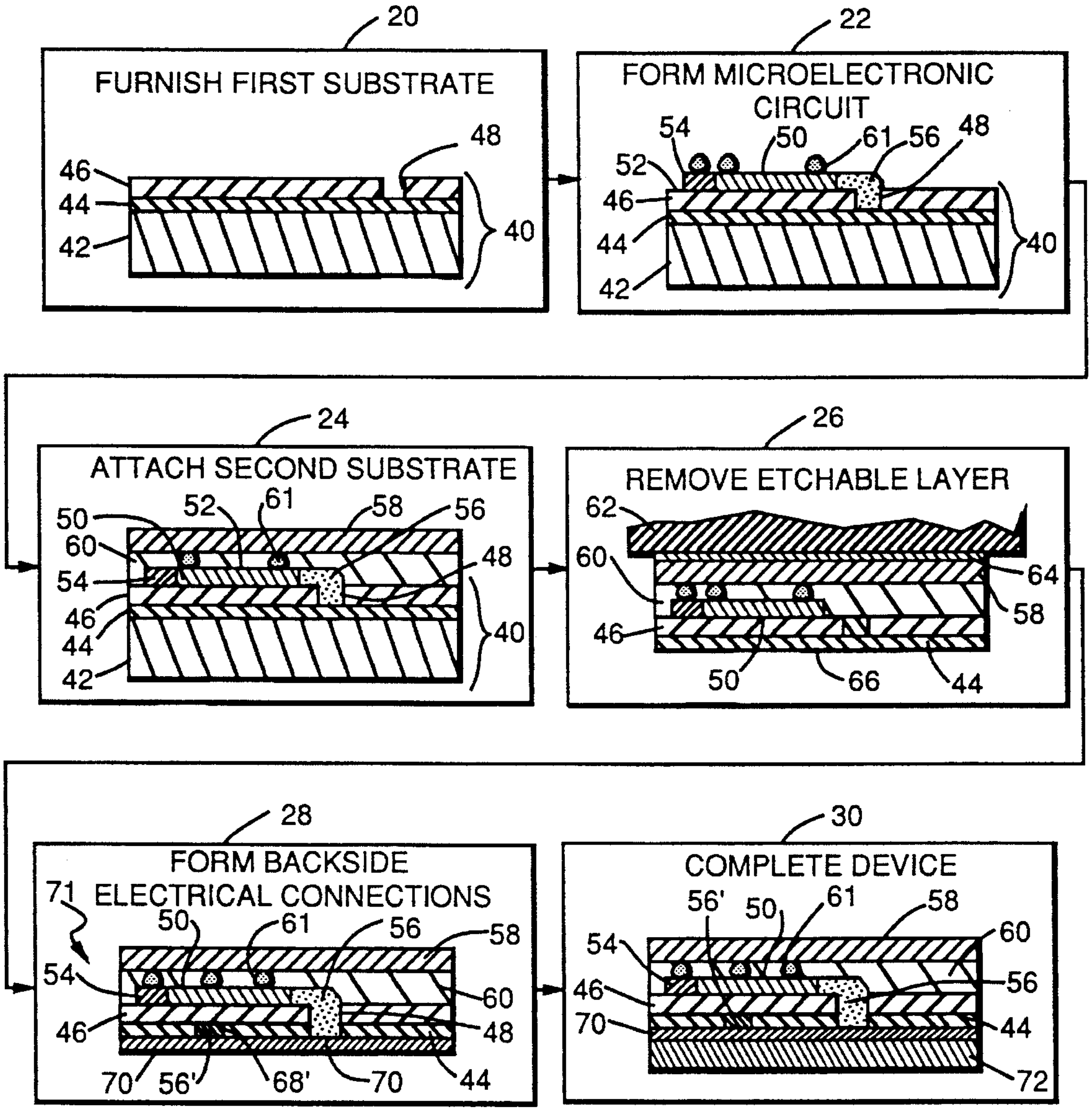

20
FURNISH FIRST SUBSTRATE
48
46
44
42
40
22
FORM MICROELECTRONIC CIRCUIT
54
50
61
56
48
52
46
44
42
40
24
ATTACH SECOND SUBSTRATE
50
52
61
58
56
60
54
48
46
44
42
40
26
REMOVE ETCHABLE LAYER
62
60
64
58
46
50
66
44
28
FORM BACKSIDE ELECTRICAL CONNECTIONS
71
50
61
56
58
54
60
48
46
70
56'
68'
70
44
30
COMPLETE DEVICE
56'
50
61
58
54
60
46
56
70
44
72

FIG. 1.

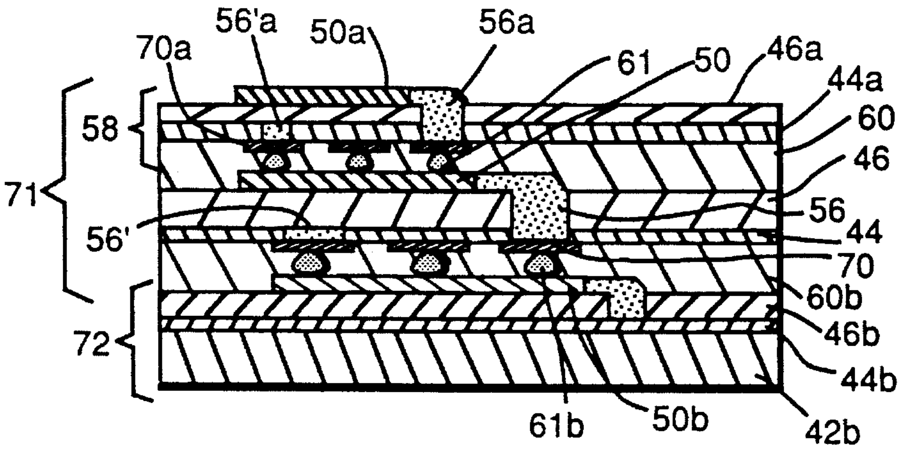


FIG. 2.

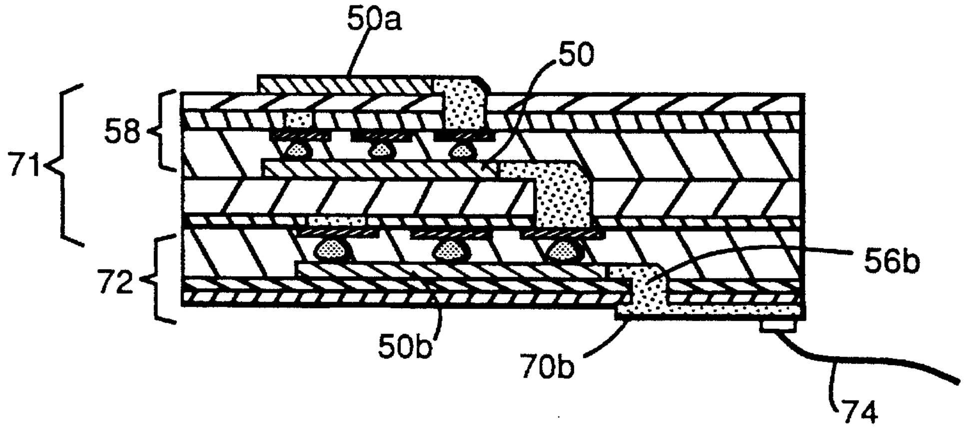


FIG. 3.

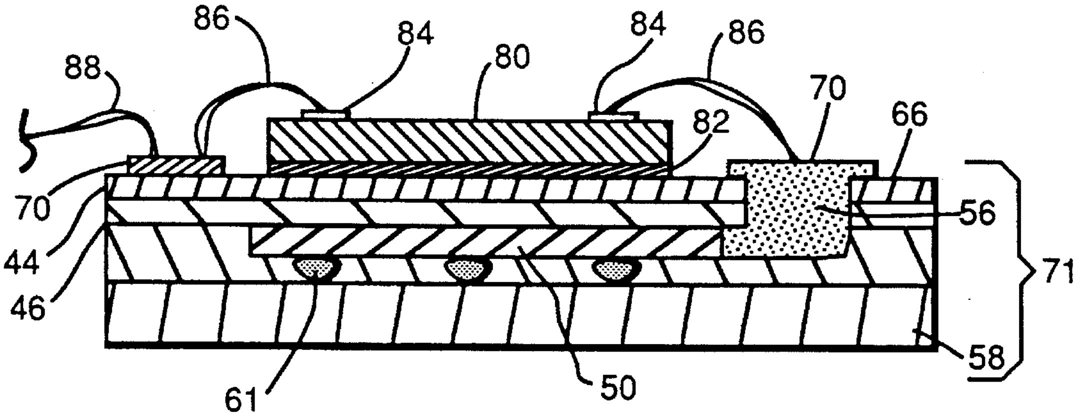


FIG. 4.

PROCESS OF MANUFACTURING A MICROELECTRIC DEVICE USING A REMOVABLE SUPPORT SUBSTRATE AND ETCH-STOP

This is a continuation of application Ser. No. 006,120 filed Jan. 19, 1993, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to microelectronic devices, and, more particularly, to a microelectronic device that is moved from one support to another support during fabrication.

Microelectronic devices are normally prepared by a series of steps such as patterning, deposition, implantation, growth, and etching that build up an electronic circuit on or near the top surface of a thin substrate wafer. Interconnection pads are placed on the surface of the wafer to provide connections to external leads or to other microelectronic devices. Such a microelectronic device is considered a two-dimensional structure in the plane of the substrate wafer. There are usually multiple layers of deposited conductors and insulators, but each layer is quite thin. Any height of the device in the third dimension perpendicular to the substrate surface is much less than the dimensions in the plane of the substrate wafer, and is often no more than a few thousand Angstroms.

The microelectronic devices or arrays of such devices are usually placed inside a protective housing called a package, with leads or connection pads extending out of the package. When the microelectronic devices are used, a number of the packages with their contained microelectronic devices are normally affixed to a base such as a phenolic plastic board. Wires are run between the various devices to interconnect them. There may be metallic traces imprinted onto the base to provide common power, ground, and bus connections, and the base itself has external connections. Such boards with a number of interconnected devices are commonly found inside both consumer and military electronics equipment. For example, an entire microcomputer may be assembled as a number of microelectronic devices such as a processor, memory, and peripheral device controllers mounted onto a single board.

The present inventors have determined that for some applications it would be desirable to stack and interconnect a number of such two-dimensional microelectronic devices, fabricated on a substrate wafer, one on top of the other to form a three-dimensional device. The stack might also include other circuit elements such as interconnect layers and thin film sensors as well. To interconnect the stacked wafers using leads that extend from the pads on the top of one wafer to the pads on the top of another wafer, around the sides of the wafers, or using plug interconnects or the like, would be clumsy, space consuming, and impossible to do for the case of highly complex circuitry requiring many interconnects.

In considering fabrication techniques to produce such three-dimensional, stacked devices, the fragility of the devices is a concern. The individual substrate wafers and their microelectronic circuitry are usually made of fragile semiconductor materials, chosen for their electronic characteristics rather than their strength or fracture resistance. The selected fabrication technique cannot damage the circuitry that has already been placed onto the substrate wafer.

Thus, there is a need for a method to fabricate three-

wafers with circuitry already on them. The present invention fulfills this need, and further provides related advantages.

SUMMARY OF THE INVENTION

The present invention provides an approach for fabricating microelectronic devices that permits three-dimensional manipulations and fabrication steps with two-dimensional devices already deposited upon a wafer substrate. The invention permits microelectronic devices to be prepared using well-established, inexpensive thin-film deposition, etching, and patterning techniques, and then to be further processed singly or in combination with other such devices, into more complex devices.

In accordance with the invention, a method of fabricating a microelectronic device comprises the steps of furnishing a first substrate having an etchable layer, an etch-stop layer overlying the etchable layer, and a wafer overlying the etch-stop layer, and forming a microelectronic circuit element in the wafer of the first substrate. The method further includes attaching the wafer portion of the first substrate to a second substrate, and etching away the etchable layer of the first substrate down to the etch-stop layer. The second substrate may include a microelectronic device, and the procedure may include the further step of interconnecting the microelectronic device on the first substrate with the microelectronic device on the second substrate.

In a typical application, the "back side" etch-stop layer is patterned, and an electrical connection to the microelectronic circuit element on the wafer is formed through the etch-stop layer. This technique permits access to the microelectronic circuit element from the back side. Electronic connections can therefore be made directly to the back side of the wafer layer, and indirectly to the front side microelectronic circuit element by opening access to front-side interconnects from the back side. Such an ability to achieve electronic access can be valuable for some two-dimensional devices, and also permits multiple two-dimensional devices to be stacked one above the other to form three-dimensional devices by using techniques such as indium bumps to form interconnections between the stacked devices.

In a preferred approach to practicing the invention, a method of fabricating a microelectronic device comprises the steps of furnishing a first substrate having a silicon etchable layer, a silicon dioxide etch-stop layer overlying the silicon layer, and a single-crystal silicon wafer overlying the etch-stop layer. The wafer has a front surface not contacting the silicon dioxide layer. A microelectronic circuit element is formed in the single-crystal silicon wafer on or through the front surface. The method further includes attaching the front surface of the single-crystal silicon wafer to a first side of a second substrate, and etching away the silicon etchable layer of the first substrate down to the silicon dioxide etch-stop layer using an etchant that attacks the silicon layer but not the silicon dioxide layer. As discussed previously, the silicon dioxide layer may then be patterned and connections formed therethrough.

The present approach is based upon the ability to transfer a thin film microelectronic circuit element or device from one substrate structure to another substrate structure. The circuit element usually is fabricated with a relatively thick first substrate that provides support during initial fabrication and handling. However, it is difficult to achieve electrical connections through such a thick substrate, because of the difficulty in locating deep, through-support vias precisely at deep vias, and the difficulty in filling a deep via with conducting material. The first substrate cannot simply be removed to permit access to the bottom side of the electrical circuit element, as the assembly could not be handled in that very thin form.

In the present approach, after initial circuit element fabrication on a first substrate structure, the electrical circuit element is transferred to a second substrate structure. (If the second substrate itself contains another microelectronic circuit element, interconnections between the two microelectronic circuit elements are made at this point, as by using an indium-bump technique/epoxy technique.) With the circuit element thus supported, the etchable portion of the first substrate is removed by etching, down to the etch-stop layer. The terms "etchable" and "etch-stop" are used herein relative to a specific selected etchant. There is chosen an etchant that readily etches the etchable layer but has a much lower etching rate for the etch-stop layer. It is understood, however, that the etch-stop layer may be generally or selectively etched by yet other techniques, after the etchable layer is removed.

Once the etchable layer is removed, the relatively thin etch-stop layer may be patterned and through-etched to provide access to the microelectronic circuit element, including its connection pads, through the etch-stop layer. Many alternative approaches are possible. For example, the two-dimensional structure may be used with direct back connections and indirect front connections. The additional surface area on the bottom of the etch-stop layer provides space for deposition of interconnection metallization traces. The two-dimensional structure may be stacked with other two-dimensional structures to form a three-dimensional structure. Further circuitry could be deposited upon the back side of the etch-stop layer, as needed and permitted by constraints imposed by the front-side circuit element structure.

Thus, the present approach provides a highly flexible approach to the fabrication of complex microelectronic devices using a building-block approach. Other features and advantages of the present invention will be apparent from the following more detailed description of the preferred embodiment, taken in conjunction with the accompanying drawings, which illustrate, by way of example, the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagrammatic process flow diagram for the approach of the invention, with the structure at each stage of fabrication indicated schematically;

FIG. **2** is a schematic side sectional view of a microelectronic device structure prepared according to the procedure of FIG. **1**;

FIG. **3** is a schematic side elevational view of a three-dimensional microelectronic device built from two-dimensional devices using the present approach; and

FIG. **4** is a schematic side elevational view of a "smart board" configuration.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. **1**, the present invention is practiced by first providing a first substrate **40**, numeral **20**. The first substrate **40** includes an etchable layer **42**, an etch-stop layer **44** grown upon and overlying the etchable layer **42**, and a wafer layer **46** bonded to and overlying the etch-stop layer **44**. Such substrates can be purchased commercially.

In the preferred practice, the etchable layer **42** is a layer of bulk silicon about 500 micrometers thick and the etch-stop layer **44** is a layer of silicon dioxide about 1 micrometer thick. The wafer layer **46** is normally thicker than required when it is bonded to the etch stop layer **44**, and is thinned to the required final thickness. A typical thinning process involves lapping followed by a chem-mechanical polish. Preferably, the wafer layer **46** is a layer of single crystal silicon initially about 500 micrometers thick which becomes, after thinning, about 30 nanometers to 50 micrometers thick. These dimensions are not critical, and may be varied as necessary for particular applications. (The structure depictions In FIGS. **1–4** are not drawn to scale.) The wafer layer **45** may also be or include an interconnect material such as a metal or other structure as may be appropriate for a particular application. In the present case, an optional via opening **48** is provided through the wafer layer **46**. The use of this via **48** will become apparent from subsequent discussions.

The first substrate **40** is prepared by applying well-known microelectronic techniques. The silicon dioxide etch-stop layer **44** is produced on a bulk silicon piece **42** by heating it in an oxygen-hydrogen atmosphere at a temperature of about 1100° C. for a time sufficient to achieve the desired thickness, typically about 2 hours. The wafer layer **46** is either deposited directly upon the etch-stop layer **44** or fabricated separately and bonded to the etch-stop layer **46** by direct interdiffusion, preferably the latter, and thinned. The via **48** is produced by standard patterning and etching techniques. (All references herein to "standard" or "well known" techniques, or the like, mean that individual process steps are known generally, not that they are known in the present context or combination, or to produce the present type of structure.)

A microelectronic circuit element **50** is formed in the wafer layer **46**, numeral **22**, working from a front exposed side **52**. The microelectronic circuit element **50** may be of any type, and may itself include multiple layers of metals, semiconductors, insulators, etc. Any combination of steps can be used, including, for example, deposition, implantation, film growth, etching, and patterning steps. As used herein, the term "microelectronic circuit element" is to be interpreted broadly, and can include active devices and passive structure. For example, the microelectronic circuit element **50** can include many active devices such as transistors. Alternatively, it may be simply a patterned electrical conductor layer that is used as an interconnect between other layers of structure in a stacked three-dimensional device, or may be a sensor element.

An important virtue of the present invention is that it is operable with a wide range of microelectronic circuit elements **50**, and therefore the present invention is not limited to any particular circuit element **50**. In the presently preferred case, the first substrate **40** is silicon based, and therefore the microelectronic circuit element **50** is preferably a silicon-based device. Where the microelectronic circuit element **50** is based upon other material systems, it may be preferred for the first substrate to be made of a material compatible to that material system. In this usage, "compatible" means that the first substrate permits fabrication of the microelectronic circuit element **50** therein.

As it is illustrated in FIG. **1**, the microelectronic circuit element **50** includes two types of electrical interconnects. A front-side electrical interconnect **54** permits direct electrical

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