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# United States Patent [19]

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Frey, Jr. et al.

[45] Date of Patent: **Jan. 19, 1993**

- [54] **ADAPTIVE ROUTING IN A PARALLEL COMPUTING SYSTEM**
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- [73] Assignee: **IBM Corporation**, Armonk, N.Y.
- [21] Appl. No.: **386,521**
- [22] Filed: **Jul. 27, 1989**
- [51] Int. Cl.<sup>5</sup> ..... **H04L 12/00; H04L 12/46**
- [52] U.S. Cl. .... **340/825.02; 395/200; 340/826; 340/827**
- [58] Field of Search ... **364/200 MS File, 900 MS File; 370/58; 379/826; 340/825.02, 827; 395/200**

E. Chow et al., 1988, pp. 90-99, California Institute of Technology, Pasadena, Calif. 91109.  
 "The Torus Routing Chip", W. Dally et al., 1986, pp. 187-196, Department of Computer Science, California Institute of Technology, Pasadena, Calif., USA.

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*Attorney, Agent, or Firm*—L. Keith Stephens; Marc Block; David Koffsky

### [57] ABSTRACT

A multi-dimensional, multi-nodal routing mechanism is described for relaying information from node to node using a header consisting of route descriptor bits. Each node's receiver/transmitter pair changes states as the information is guided to the destination node. The message is propagated over several nodes simultaneously to traverse the nodes and reach the destination node quickly. When the final node is reached, all alternate communication routes are freed.

### [56] References Cited

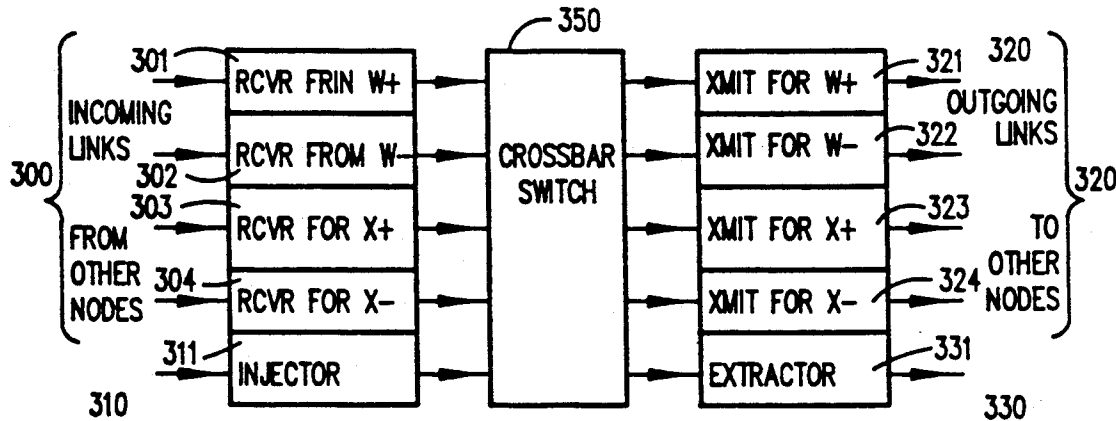
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- 4,825,206 4/1989 Brice, Jr. et al. .... 340/825.02
- 4,872,197 10/1989 Pemmaraju ..... 379/93

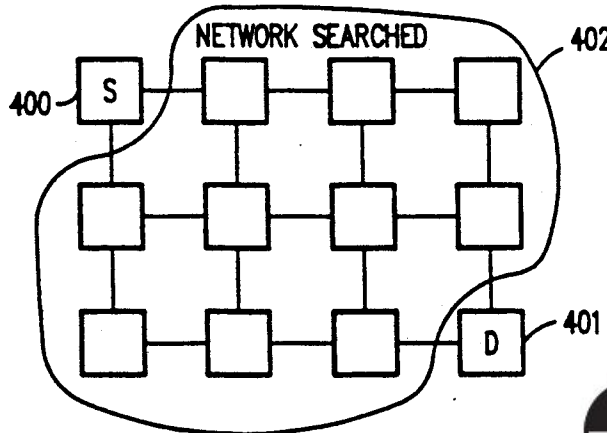
#### OTHER PUBLICATIONS

"Hyperswitch Network for the Hypercube Computer",

15 Claims, 8 Drawing Sheets



HEADER  
 0000 0101  
 0000 0101  
 0000 0001  
 0000 0000



**EXHIBIT**  
**Ex. 1030**

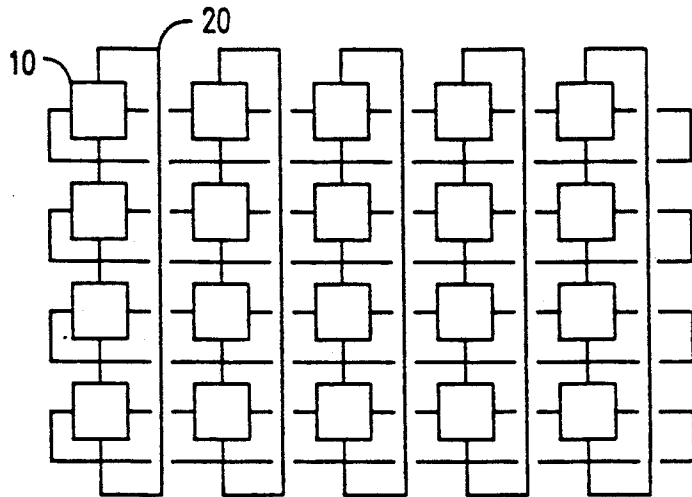


FIG. 1

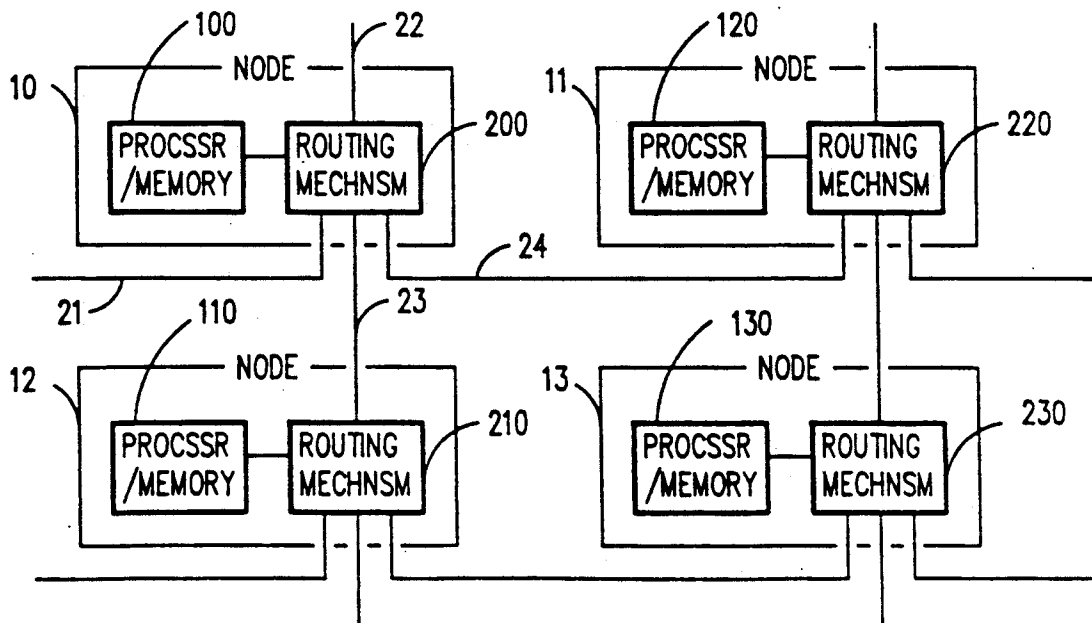


FIG. 2

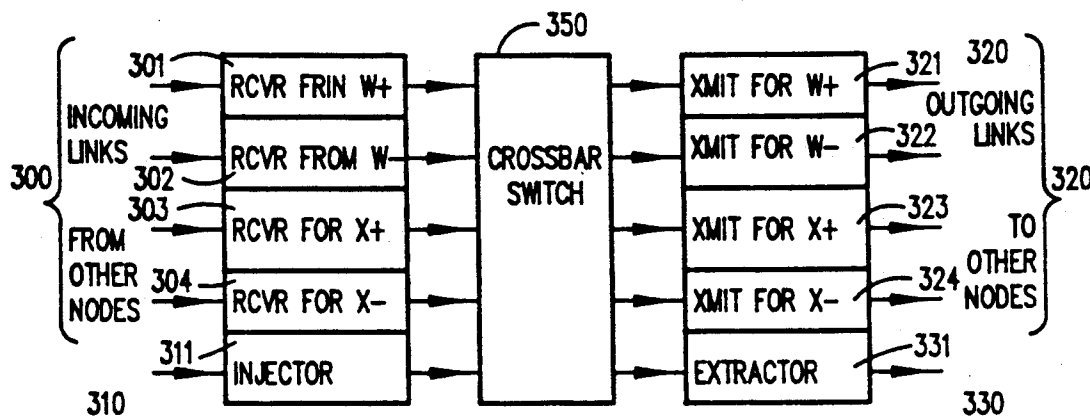


FIG. 3

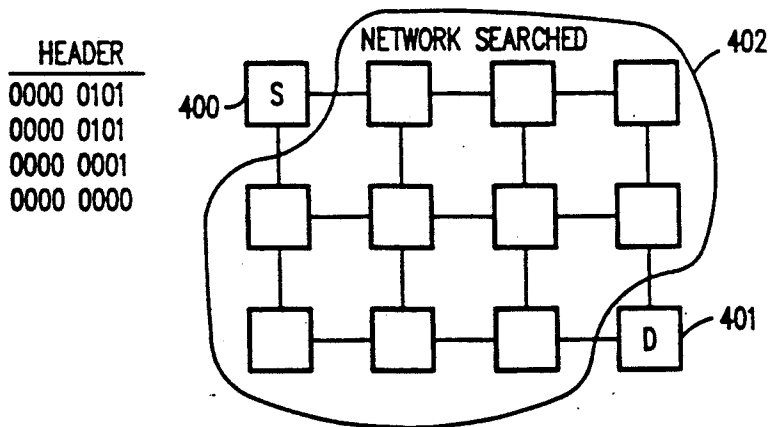


FIG. 4

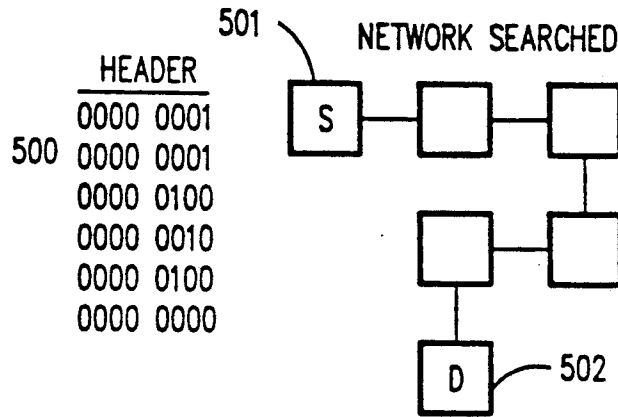


FIG. 5

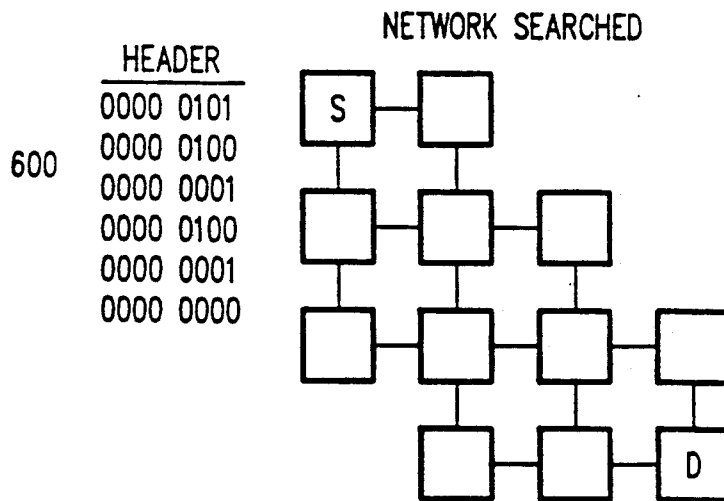


FIG. 6

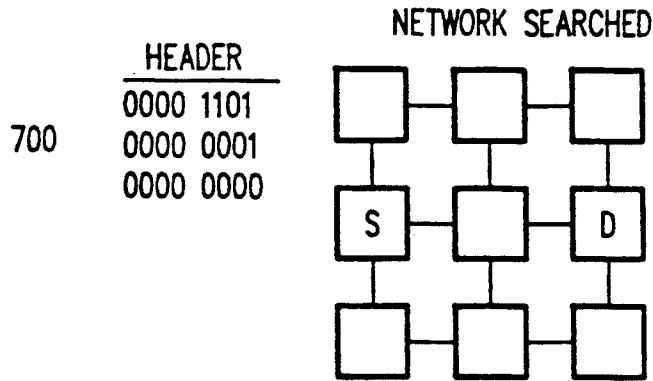


FIG. 7

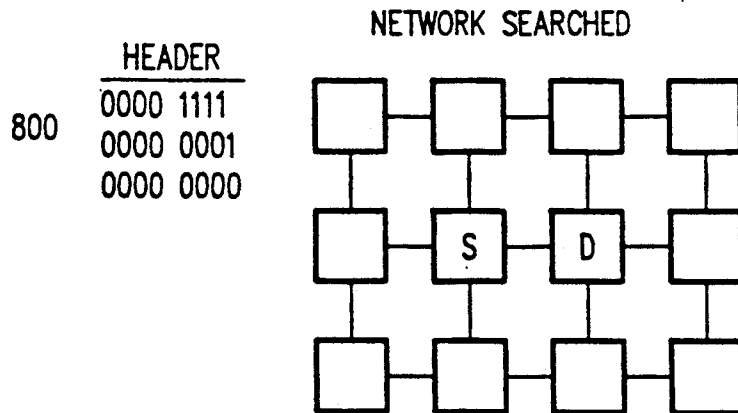


FIG. 8

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