(Draft)

Video Electronics Standards Association

2150 North First Street, Suite 440	Phone: (408) 435-0333
San Jose, CA 95131-2029	FAX: (408) 435-8225

VESA Unified Memory Architecture
Hardware Specifications Proposal
Version: 1.0p
Document Revision: 0.4p
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Purpose

To enable core logic chipset and VUMA device designers to design VUMA devices supporting the Unified Memory Architecture.

Summary

This document contains a specification for VUMA devices' hardware interface. It includes logical and electrical interface specifications. The BIOS protocol is described in VESA document VUMA VESA BIOS Extensions (VUMA-SBE) rev. 1.0.

Scope

Because this is a draft document, it cannot be considered complete or accurate in all respects although every effort has been made to minimize errors.

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Support For This Specification

If you have a product that incorporates VUMA^{TM}, you should ask the company that manufactured your product for assistance. If you are a manufacturer of the product, VESA can assist you with any clarification that you may require. All questions must be sent in writing to VESA via:

(The following list is the preferred order for contacting VESA.)

VESA World Wide Web Page:	*www.vesa.org*
Fax:	(408) 435-8225
Mail:	VESA
	2150 North First Street
	Suite 440
	San Jose, California 95131-2029

Acknowledgments

This document would not have been possible without the efforts of the members of the 1995 VESA Unified Memory Architecture Committee and the professional support of the VESA staff.

Work Group Members

Any industry standard requires information from many sources. The following list recognizes members of the VUMA Committee, which was responsible for combining all of the industry input into this proposal.

Chairperson

Rajesh Shakkarwar	OPTi

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Jonathan Claman	S3
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Revision History

Initial Revision 0.1p   Sept. 21 '95

Revision 0.2p   Oct 5 '95
      Added sync DRAM support
      Electrical Section
      Boot Protocol
      Reformatted document

Revision 0.3p   Oct 19 '95
      Graphics controller replaced with VUMA device
      MD[n:0] changed to t/s
      Modified Aux Memory description
      Added third solution to Memory Expansion Problem
      Synch DRAM burst length changed to 2/4
      Modified all the bus hand off diagrams
      Added DRAM Driver Characteristics section

Revision 0.4p   Oct 19 '95
      Sync DRAM Burst Length changed to 1/2/4
      DRAM controller pin multiplexing added
      Changed AC timing parameters

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