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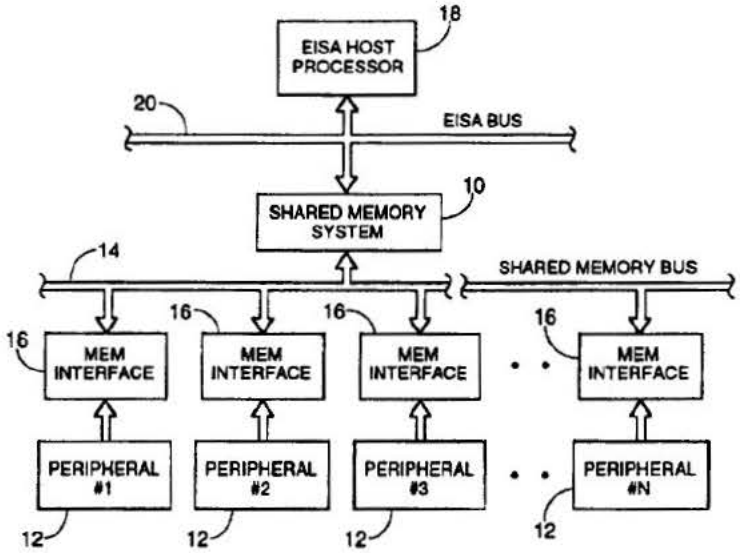

(57) Abstract

A shared memory system (10) interfaces a shared memory bus (14) and EISA processor bus (20). The shared memory system (10) has an associated arbitration logic circuit (78) that services bus requests from each of the memory interfaces (16). In one of 2 arbitration modes, the shared memory system (10) allows a bus request from one of the memory interfaces (16) to transfer one byte of data, after which its priority is lowered and it relinquishes the bus to another one of the memory interfaces (16). This allows a byte-by-byte transfer without allowing any memory interface (16) to seize the bus. In another mode, each of the memory interfaces (16) is allowed to seize the bus to continuously transfer data with a priority system implemented to allow a higher priority one to seize the bus away from a lower

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SHARED MEMORY SYSTEM

In large integrated computer networks, large storage systems are typically disposed in a server-based system with multiple peripheral systems allowed to operate independently and access the server main memory. One typical way for integrating such a network is that utilized in Local Area Networks (LANs). In these type of networks, a single broadband communication bus or media is provided through which all signals are passed. These LANs provide some type of protocol to prevent bus conflicts. In this manner, they provide an orderly method to allow the peripheral systems to "seize" the bus and access the server main memory. However, during the time that one of the peripheral systems has seized the bus, the other peripheral systems are denied access to the server main memory.

In the early days of computers, this was a significant problem in computer centers in that a computer operator determined which program was loaded on the computer, which in turn determined how the computer resources were utilized. However, the computer operator would assign priority to certain programs such as those from a well-known professor in a university system. In such an environment, it was quite common for priority to be assigned such that the computer could be tied up for an entire evening working on a problem for an individual with such a high priority. Students in the university-based system, of course, had the lowest priority and, therefore, their programs were run only when the system resources were available. The problem with this type of system was that an extremely small program that took virtually no time to run was required to sit on the shelf for anywhere from five to twenty hours waiting for the larger, higher priority program to run. Although it would have been desirable to have the system operator instruct it to interrupt the higher priority program for a relatively short time to run a number of the fairly short programs, this was not an available option. Even if this interruption may have extended the higher priority program for a fairly short time, it would clearly provide a significantly higher level of service to the low priority small program users.

Present networks are seldom comprised of a single LAN system due to the fact that these networks are now distributed. For example, a single system at a given site utilizing a local network that operates over, for example, an Ethernet® cable, would have a relatively high data transfer rate on the local cable. The Ethernet® cables in those systems provide a means to access remote sites via the telephone lines or other communication links. However, these communication links tend to have significantly slower access time. Even though they can be routed through a relatively high speed Ethernet® bus, they still must access and transmit instructions through the lower speed communication link. With the advent of multimedia, the need for much larger memories that operate in a shared memory environment has increased. In the multimedia world, the primary purpose of the system is for data exchange. As such, the rate of data transfer from the server memory to multiple systems is important. However, regardless of the type of memory system or the type of data transfer performed, the system still must transfer the data stored in the server memory in a serial manner; that is, only one word of data can be accessed and transferred out of the memory (or written thereto) on any given instruction cycle associated with the memory. When multiple systems are attempting to access the given server memory, it is necessary to control the access to the server memory by the peripheral system in an orderly manner to ensure all peripheral systems are adequately served.

In typical systems that serve various communication links to allow those communication links to access the server memory, separate coprocessors are typically provided to handle the communication link.

This will therefor requires the server processor to control access to the server main memory. By requiring the server processor to serve access control limits the amount of data that can be transferred between the server and the communication coprocessor, thus to the peripheral.

SUMMARY OF THE INVENTION

The present invention, disclosed and claimed herein, comprises a shared memory system that includes a centrally located memory. The shared memory has a plurality of storage locations, each for storing data of a finite data size as a block of data. The block of data is accessible by an address associated with the storage location of the block of data for storage of data therein or retrieval of data therefrom. The centrally located memory is controlled by a memory access control device. A plurality of peripheral devices are disposed remote to the shared memory system, each operable to access the centrally located memory and generate addresses for transmittal thereto to address a desired memory location in the central locating memory system. The peripheral device is then allowed to transfer data thereto or retrieve data therefrom. A memory interface device is disposed between each of the peripheral devices and the centrally located memory system and is operable to control the transmittal of addresses from the associated peripheral device to the centrally located memory and transfer of data therebetween. The memory interface device has a unique ID which is transmitted to the centrally located memory. Associated with the centrally located memory is an arbitration device that is operable to determine which of the peripheral devices is allowed to access the centrally located memory. The arbitration device operates in a block-by-block basis to allow each peripheral unit to only access the centrally located memory for a block of data before relinquishing access, wherein all requesting ones of the peripheral devices will have access to at least one block of data prior to any of the peripheral devices having access to the next block of data requested thereby.

In an alternate embodiment of the present invention, each block of data comprises a byte of data. Further, each memory interface device is given a priority bas upon its unique ID. The arbitration device operates in a second mode to allow the highest priority one of the requesting peripheral devices to seize the bus away from any of the other peripheral devices to access all of the data requested thereby.

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