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United States Patent [19]

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Bowes et al.

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[54] **MEMORY BUS ARBITER FOR A COMPUTER SYSTEM HAVING A DSP CO-PROCESSOR**

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5,353,417 10/1994 Fuoco et al. 395/325

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[57] **ABSTRACT**

[21] Appl. No.: **189,138**

An arbitration scheme for a computer system in which a digital signal processor resides on the computer system's memory bus without requiring a block of dedicated static random access memory. An arbitration cycle is divided into 10 slices of which 5 slices are provided in each arbitration loop to the digital signal processor. Two slices are provided each to the system's I/O interface and to the peripheral bus controller. A final slice is provided to the system's CPU. A default state when no memory bus resource is requesting the system memory bus parks the memory bus on the CPU. The arbitration scheme provides sufficient bandwidth for real-time signal processing by the digital signal processor operating from the system's dynamic random access memory while also providing sufficient bandwidth for a local area network interface through the system's I/O interface.

[22] Filed: **Jan. 28, 1994**

[51] Int. Cl.⁶ **G06F 13/00**

[52] U.S. Cl. **395/294; 395/293**

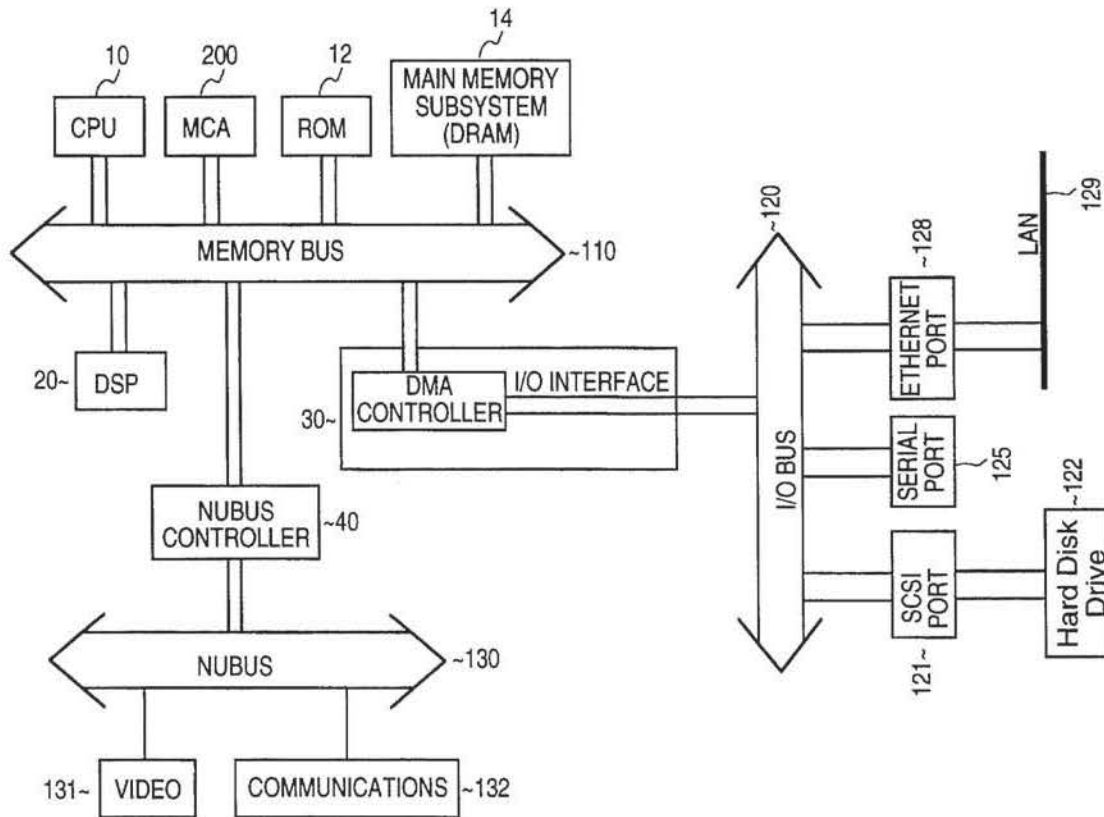
[58] Field of Search **395/325, 425**

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8 Claims, 5 Drawing Sheets



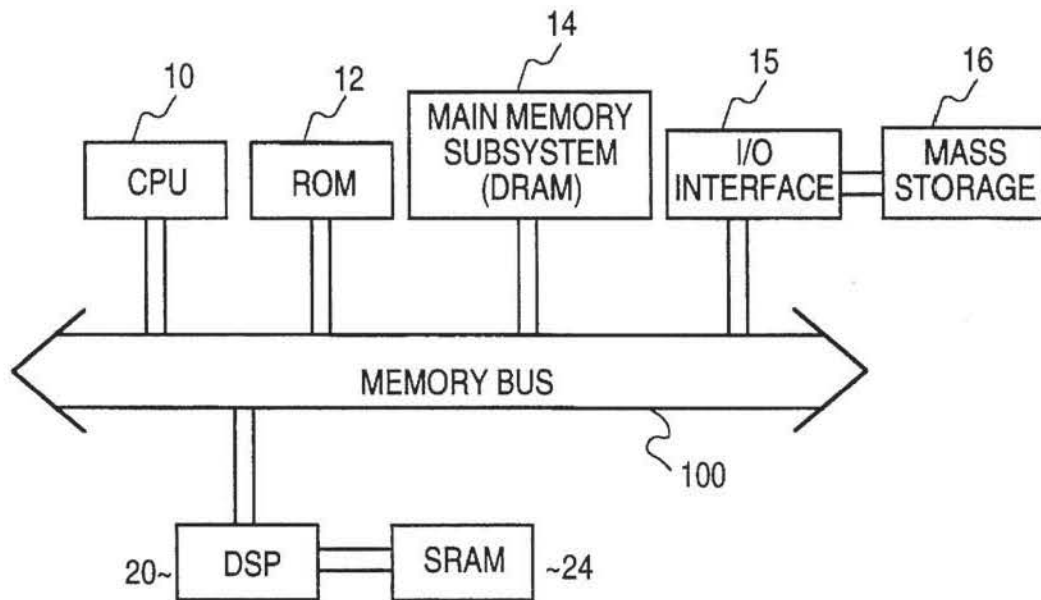


Figure 1 (Prior Art)

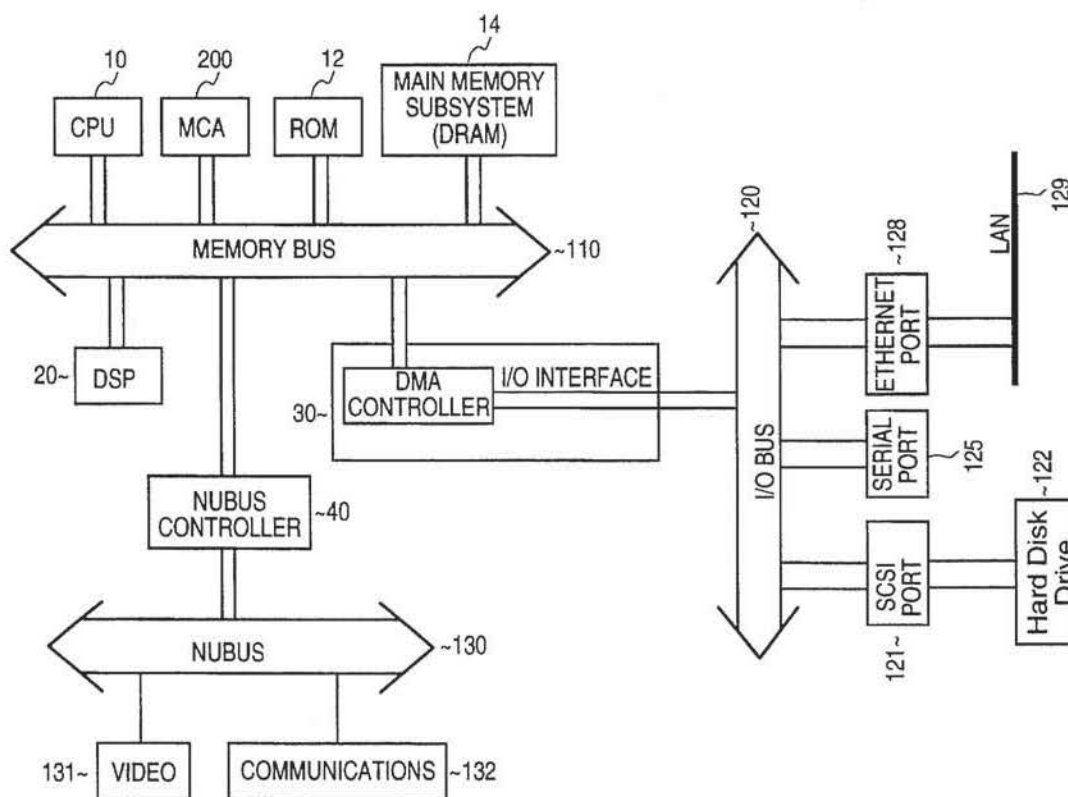


Figure 2

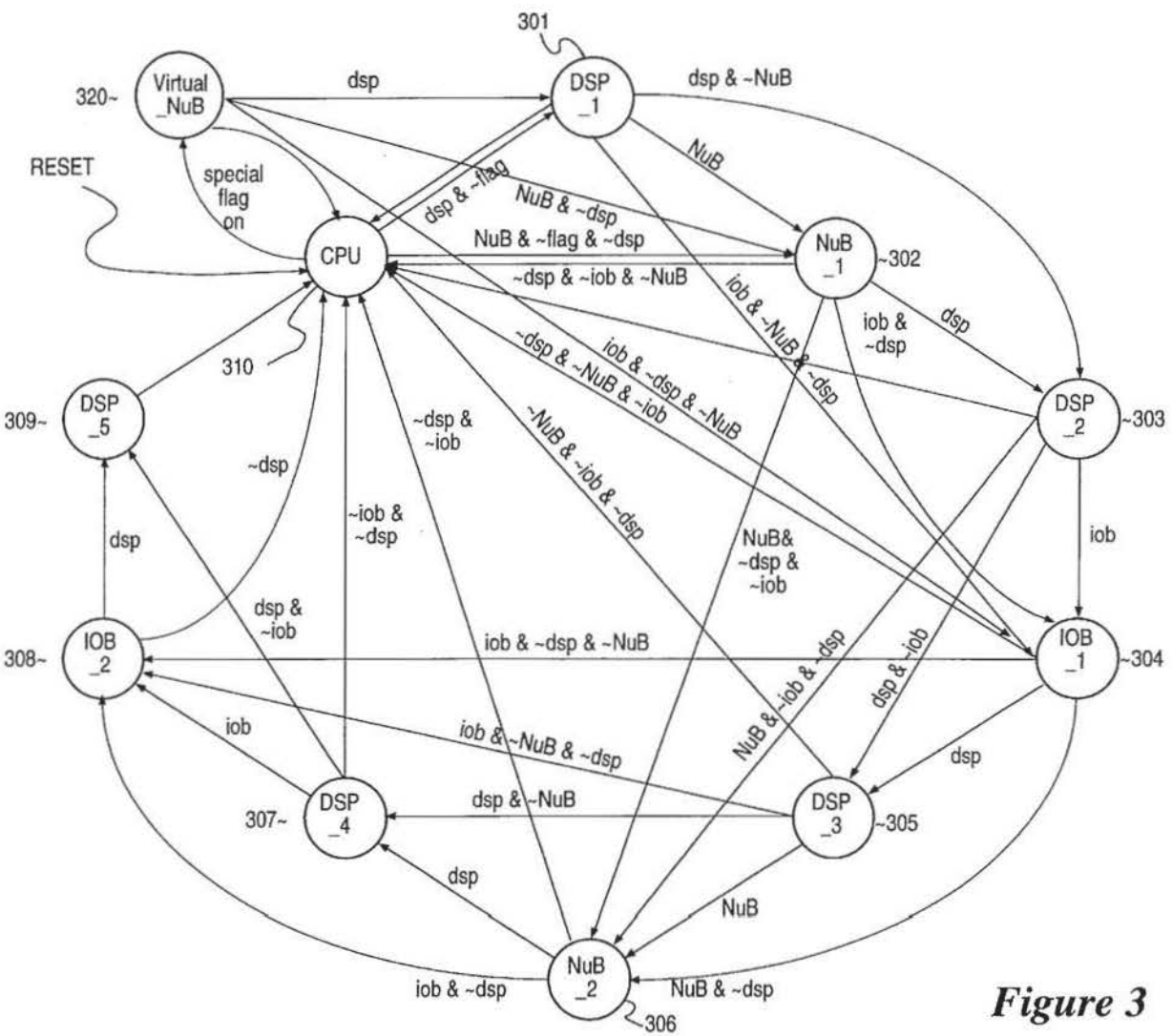


Figure 3

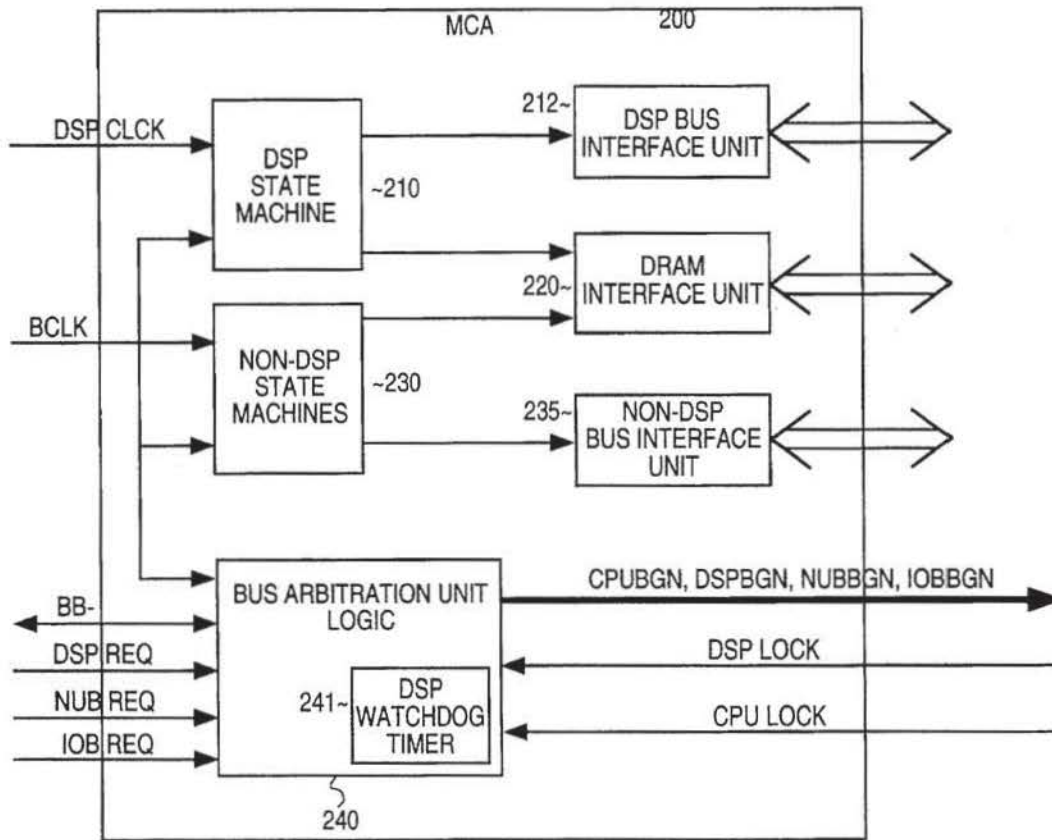


Figure 4

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