

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ASUSTEK COMPUTER, INC. and
ASUS COMPUTER INTERNATIONAL,
Petitioner,

v.

AVAGO TECHNOLOGIES GENERAL IP (SINGAPORE) PTE. LTD.,
Patent Owner.

Case IPR2016-00646
Patent 5,870,087

Before GLENN J. PERRY, PATRICK R. SCANLON, and
J. JOHN LEE, *Administrative Patent Judges*.

SCANLON, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

ASUSTeK Computer, Inc. and ASUS Computer International (collectively, “Petitioner”) filed a Petition (Paper 3, “Pet.”) requesting an *inter partes* review of claims 1, 5, 7–11, and 16 of U.S. Patent No. 5,870,087 (Ex. 1001, “the ’087 patent”) pursuant to 35 U.S.C. §§ 311–319. Avago Technologies General IP (Singapore) Pte. Ltd., (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”).

We have jurisdiction under 35 U.S.C. § 314, which provides that *inter partes* review may not be instituted unless “the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

Upon consideration of the Petition and the Preliminary Response, and for the reasons discussed below, we determine that Petitioner has established a reasonable likelihood of prevailing in showing the unpatentability of the challenged claims. Accordingly, we institute *inter partes* review of claims 1, 5, 7–11, and 16.

II. BACKGROUND

A. Related Matters

Petitioner indicates that the ’087 patent is at issue in the following United States District Court proceedings: *Avago Technologies General IP (Singapore) PTE Ltd. v. ASUSTeK Computer, Inc.*, Case No. 3:15-cv-04525 (N.D. Cal.) and *Avago Technologies General IP (Singapore) PTE Ltd. v. ASUSTeK Computer Inc.*, Case No. 3:16-cv-00451 (N.D. Cal.). Pet. 1. The ’087 patent is also asserted against entities unrelated to Petitioner in *Avago Technologies General IP (Singapore) PTE Ltd. v. Acer Inc.*, Case No. 3:15-cv-05427 (N.D. Cal.). *Id.*

B. The '087 patent

The '087 patent describes “an MPEG decoder system and method for video decoding or decompression which includes a unified memory for multiple functions.” Ex. 1001, 4:65–5:1. Figure 3, reproduced below, shows an embodiment of an MPEG decoder system.

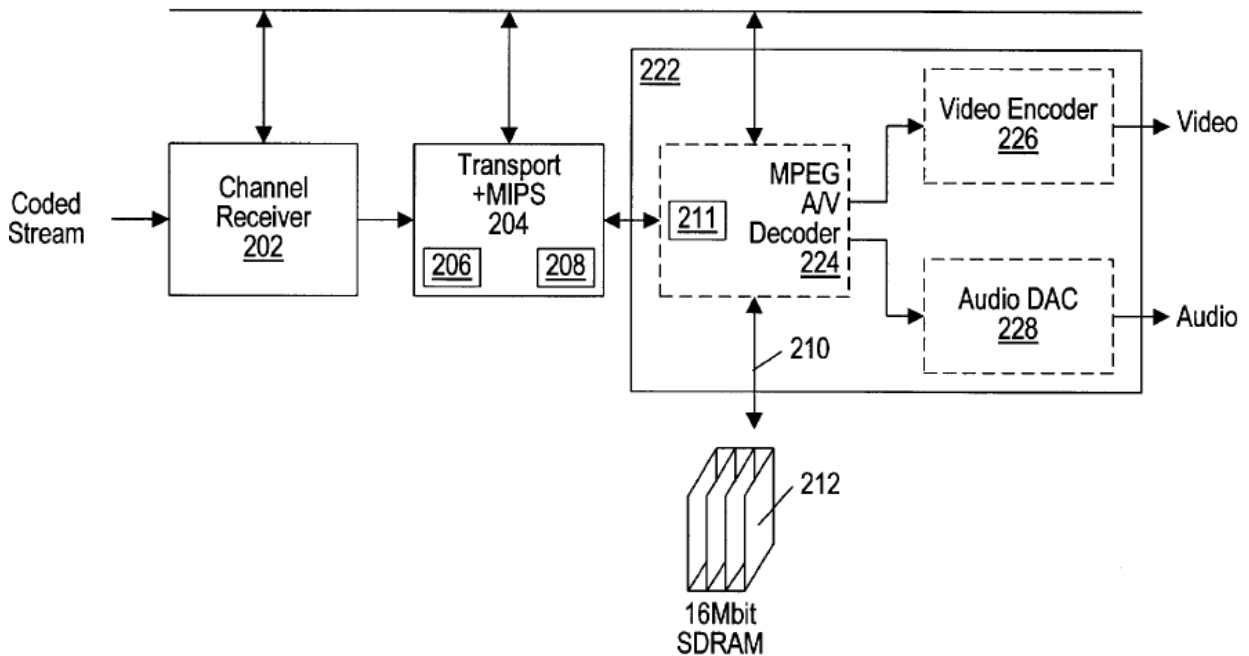


FIG. 3

Figure 3 is a block diagram illustrating an MPEG decoder system including a unified memory. Ex. 1001, 5:55–56.

The system includes channel receiver 202 that receives a coded stream and provides the coded stream to transport and system controller block 204. *Id.* at 8:7–9. Transport and system controller block 204 includes transport logic 206, which demultiplexes the received MPEG encoded stream into a plurality of multimedia data streams, and system controller 208, which monitors and preferably controls the MPEG system. *Id.* at 8:10–13, 29–35. The system also includes MPEG

decoder 224 that “receives data from the transport and system controller block 204 and operates to perform MPEG decoding to produce a decoded or decompressed signal.” *Id.* at 8:50–53. Transport and system controller block 204 couples to external memory 212 via memory controller 211 in MPEG decoder 224. *Id.* at 8:38–40. The system “includes a single unified memory which stores code and data for the transport logic, system controller and MPEG decoder functions.” *Id.* at 5:3–6.

C. Illustrative Claim

Of the challenged claims in the '087 patent, claims 1, 10, and 16 are independent. Claim 1 is illustrative of the claims at issue:

1. An MPEG decoder system which includes a single memory for use by transport, decode and system controller functions, comprising:

a channel receiver for receiving and MPEG encoded stream;

transport logic coupled to the channel receiver which demultiplexes one or more multimedia data streams from the encoded stream;

a system controller coupled to the transport logic which controls operations within the MPEG decoder system;

an MPEG decoder coupled to receive one or more multimedia data streams output from the transport logic, wherein the MPEG decoder operates to perform MPEG decoding on the multimedia data streams; and

a memory coupled to the MPEG decoder, wherein the memory is used by the MPEG decoder during MPEG decoding operations, wherein the memory stores code and data useable by the system controller which enables the system controller to perform control functions within the MPEG decoder system, wherein the memory is used by the transport logic for demultiplexing operations;

wherein the MPEG decoder is operable to access the memory during MPEG decoding operations;

wherein the transport logic is operable to access the memory to store and retrieve data during demultiplexing operations; and

wherein the system controller is operable to access the memory to retrieve code and data during system control functions.

Ex. 1001, 17:15–45.

D. The Prior Art

Petitioner relies on the following prior art:

1. U.S. Patent No. 5,960,464, issued Sept. 28, 1999 (“Lam”) (Ex. 1004);
2. U.S. Patent No. 5,898,695, issued Apr. 27, 1999 (“Fujii”) (Ex. 1005); and
3. U.S. Patent No. 5,847,771, issued Dec. 8, 1998 (“Cloutier”) (Ex. 1006).

E. The Asserted Grounds

Petitioner challenges claims 1, 5, 7–11, and 16 of the ’087 patent on the following grounds:¹

References	Basis	Claims Challenged
Lam	§ 102(e)	1, 5, 10, 11, and 16
Fujii	§ 102(e)	1, 7, 10, 11, and 16
Fujii and Lam	§ 103	1, 5, 7–11, and 16
Lam and Cloutier	§ 103	7–9
Fujii and Cloutier	§ 103	7–9
Fujii, Lam, and Cloutier	§ 103	7–9

¹ Sections 3(b) and 3(c) of the Leahy-Smith America Invents Act (“AIA”) amended 35 U.S.C. § 102 and § 103, respectively. Pub. L. No. 112-29, 125 Stat. 284, 285–287 (2011). Because the ’087 patent has a filing date before March 16, 2013 (effective date of § 3), the pre-AIA versions of §§ 102, 103 apply in this proceeding. *See id.* § 3(n)(1), 125 Stat. at 293.

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