512K x 16Bit x 2 Bank Synchronous DRAM

FEATURES

- JEDEC standard 3.3V Power Supply.
- LVTTL compatible with multiplexed address.
- Dual Bank.
- MRS cycle with address key programs.
  - -. CAS Latency (1, 2, 3)
  - -. Burst Length (1, 2, 4, 8 & Full page)
  - -. Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst Read Single Bit Write Operation.
- L(U)DQM for byte masking.
- Auto & Self Refresh.
- 32ms Refresh Period. (2K cycle)

GENERAL DESCRIPTION

The KM416S1120A is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 524,288 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology.

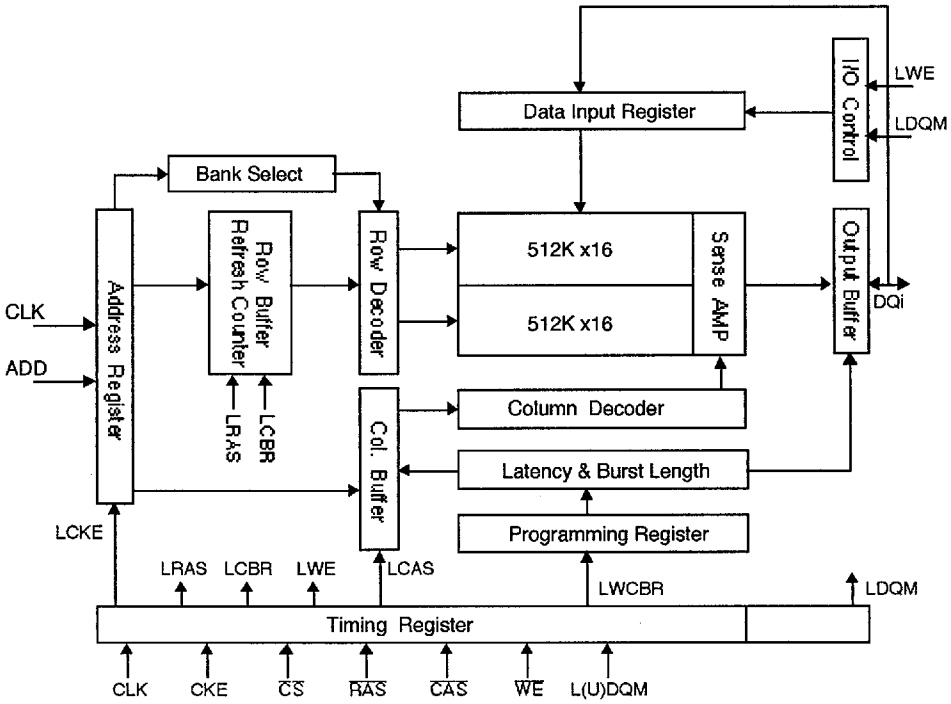
Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle.

Range of operating frequencies, programmable burst length, and programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

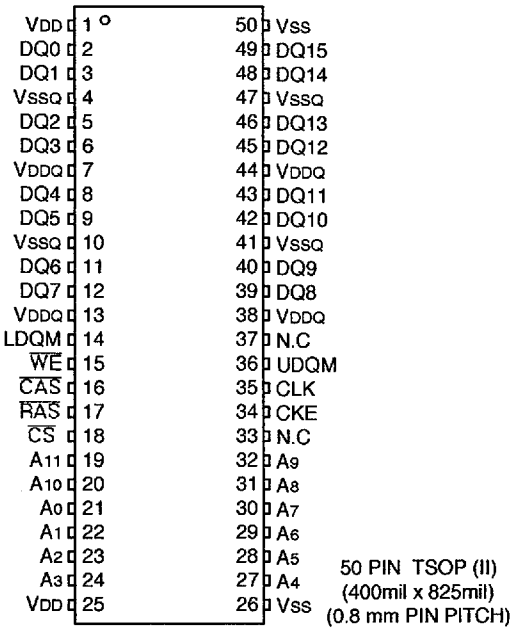
ORDERING INFORMATION

Part NO.	Max Freq.	Package
KM416S1120AT-G/F10	100 MHz	TSOP (II)
KM416S1120AT-G/F12	83 MHz	TSOP (II)

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



50 PIN TSOP (II)
(400mil x 825mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE, and L(U)DQM
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down in standby. CKE should be enabled t_{PDE} prior to valid command.
$A_0 \sim A_{10}$	*Address*	Row / column addresses are multiplexed on the same pins. Row address : $RA_0 \sim RA_{10}$, Column address : $CA_0 \sim CA_7$
A_{11}	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge.
L(U)DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
$DQ_{0 \sim 15}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power Supply/Ground*	
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltages referenced to Vss = 0V, T_A=0°C to 70°C)

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Supply voltage	V_{DD},V_{DDQ}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.3	0	0.8	V	Note 1
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH}=-2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	uA	Note 2
Output leakage current	I_{OL}	-5	-	5	uA	Note 3

Note : 1. V_{IL}(min.) = -1.5V AC (pulse width ≤ 5 ns)
2. Any input 0≤V_{IN}≤V_{DD} + 0.3V, all other pins are not under test = 0V.
3. Dout is disabled, 0V≤V_{OUT}≤V_{DD}.

CAPACITANCE (V_{DD}= 3.3V, T_A= 25°C, f= 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{11})	C_{IN1}	-	5	pF
Input capacitance (CLK,CKE,$\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$ & L(U)DQM)	C_{IN2}	-	5	pF
Data input/output capacitance (DQ_0 ~ DQ_{15})	C_{OUT}	-	6	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitors are added to power line on PCB.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and Vss	C_{DC1}	0.1 * 3	uF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	0.1 * 3	uF

Note : 1. V_{DD} and V_{DDQ} pins are separated each other.
All V_{DD} pins are connected inside the chip. All V_{DDQ} pins are connected inside the chip.
2. Vss and V_{SSQ} pins are separated each other.
All Vss pins are connected inside the chip.

DC CHARACTERISTICS

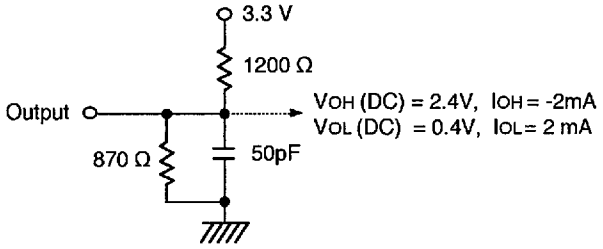
(Recommended Operating Conditions Unless Otherwise Noted, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Version -12	Unit	Note
Operating Current	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA	3	105	100	mA	1
			2	95	90		
			1	90	85		
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE≤V_{IL}(max), t_{CC}=15ns		3		mA	
	I_{CC2PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		2			
Precharge Standby Current in Non power-down mode	I_{CC2N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		25		mA	
	I_{CC2NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		8			
Active Standby Current in power-down mode	I_{CC3P}	CKE≤V_{IL}(max), t_{CC}=15ns		3		mA	
	I_{CC3PS}	CKE & CLK≤V_{IL}(max), t_{CC}= ∞		2			
Active Standby Current in Non power-down mode (One Bank Active)	I_{CC3N}	CKE≥V_{IH}(min), $\overline{CS}$≥V_{IH}(min), t_{CC}=15ns Input signals are changed one time during 30ns		30		mA	
	I_{CC3NS}	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		15			
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA Page Burst All Banks activated t_{CCD}=t_{CCD}(min)	3	145	125	mA	1, 2
			2	105	90		
			1	65	60		
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3	95	90	mA	3
			2	90	85		
			1	85	80		
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V		2		mA	4
				250		uA	5

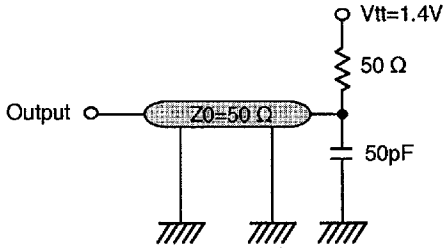
Note : 1. Measured with outputs open.
2. Assumes minimum column address update cycle t_{CCD}(min)
3. Refresh period is 32ms.
4. KM416S1120AT-G**
5. KM416S1120AT-F**

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, T_A = 0 to 70 °C)

Parameter	Value
AC input levels	V_{IH}/ V_{IL}= 2.4V / 0.4V
Input timing measurement reference level	1.4V
Input rise and fall time	tr / tf = 1ns / 1ns
Output measurement reference level	1.4V
Output load condition	See Fig. 2



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version -10	Version -12	Unit	Note
Row active to Row active delay		tRRD(min)	20	24	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	26	30	ns	1
Row precharge time		tRP(min)	26	30	ns	1
Row active time		tRAS(min)	60	66	ns	1
		tRAS(max)	200	200	us	
Row cycle time		tRC(min)	96	100	ns	1
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to Row precharge		tRDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	0		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS Latency= 3		2		ea	4
	CAS Latency= 2		1			
	CAS Latency= 1		0			

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of Row precharge interrupt, Auto precharge and Read burst stop.

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