

Am79C971
PCnet™-FAST
Hardware User's Manual



1 INTRODUCTION

1.1 INTRODUCTION

The PCnet™-FAST board is an advanced PC network interface adapter card targeted for the Ethernet-PCI adapter card market. It is based on the Am79C971 PCnet-FAST device, a single-chip 32-bit full-duplex, 10/100-Mbps highly integrated Ethernet system solution. Designed to address high performance system applications, the flexible bus master architecture provides high data throughput in the system and low CPU and system bus utilization. The PCnet-FAST board supports the PCI Specification (Rev. 2.1), jumperless bus and media configuration, and driver software compatible with the existing PCnet family of drivers.

This manual provides a complete description of the PCnet-FAST board, with sections covering the functional description of each building block, the setup and installation of the board, and the hardware specification.

It is assumed that the user of this manual has access to the information listed below, since references to these documents are made throughout this manual:

- *AMD Ethernet/IEEE 802.3 Family, 1994 World Network Data Book/Handbook (PID# 14287).*
- *Am79C971 PCnet-FAST Single-Chip Full-Duplex 10/100 Mbps Ethernet Controller for PCI Local Bus Preliminary Data Sheet (PID# 20550B)*
- *PCnet Family Network Family Driver Installation Guide (PID# 18233D)*
- *PCI Specification, Revision 2.1*

2 FUNCTIONAL DESCRIPTION

2.1 BOARD DESCRIPTION

The PCnet-FAST board is a 10/100-Mbps PCI network interface card. The Ethernet connection is implemented through the single RJ-45 jack which is connected to an external 10/100 TX transceiver. The transceiver is connected to the PCnet-FAST controller through the integrated Media Independent Interface (MII). Due to the high integration of the PCnet-FAST device, very few external parts are needed. The PCnet-FAST evaluation board provides the remote boot capability via an EPROM on the FLASH device. In addition, SRAMs may be added to optimize performance. In most applications, two 15-ns 32x8 SRAMs are sufficient to satisfy the buffer requirement.

The following diagram illustrates the implementation of the PCnet-FAST board.

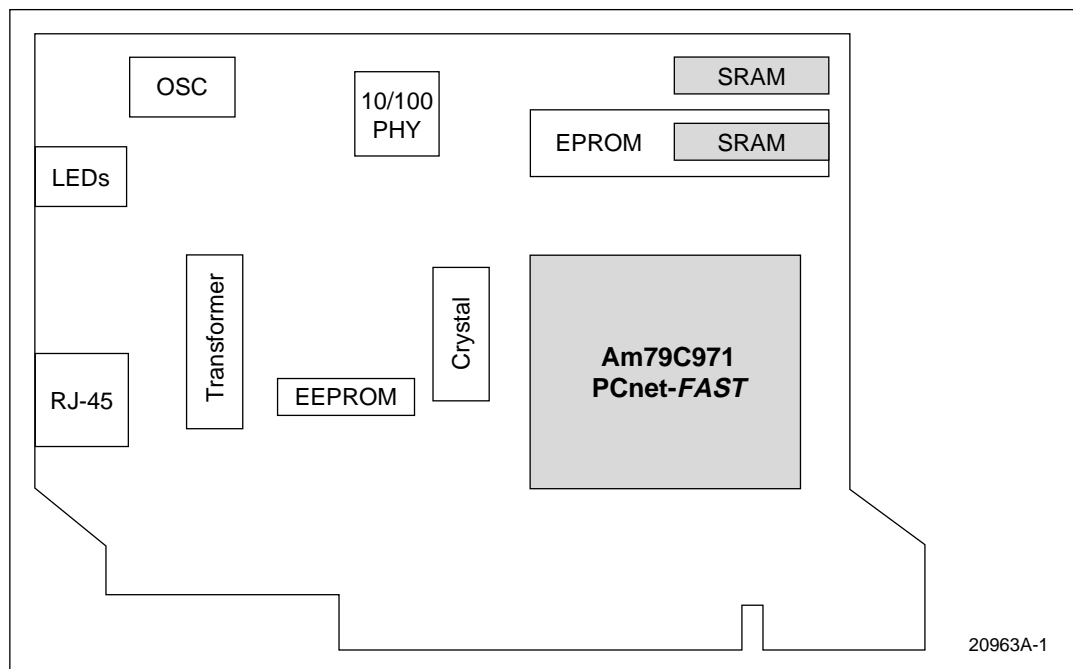


Figure 2-1 Board Diagram

2.2 ETHERNET NODE CONTROLLER

The single-chip Am79C971 PCnet-FAST Ethernet solution is a highly integrated solution that contains a Bus Interface Unit (BIU), a DMA buffer management unit, an ISO/IEC 8802-3 and ANSI/IEEE 802.3-compliant Media Access Control (MAC) function, a flexible buffer architecture with an SRAM-based FIFO extension for support up to 128 Kbytes of external frame buffering, optional remote boot PROM/FLASH, integrated 10BASE-T and 10BASE-2/5 (AUI) physical layer interface, and an ANSI/IEEE 802.3-compliant Media Independent Interface (MII).

2.3 LOCAL BUS INTERFACE

The PCnet-FAST board implements the local bus interface to the Peripheral Components Interconnect (PCI) revision 2.1 specification through the Am79C971 chip. The BIU in the chip is designed to operate as a PCI bus master during normal operations, and some slave I/O accesses to the controller are required in normal operation as well. Initialization of the Ethernet controller is achieved through a combination of PCI Configuration Space accesses, bus slave accesses, bus master accesses, and an optional read of a serial EEPROM that is performed by the controller.

2.4 ETHERNET INTERFACE

The Ethernet interface for the PCnet-FAST board is achieved through the single RJ-45 jack. The RJ-45 jack is connected to an external 10/100-Mbps transceiver connected to the PCnet-FAST controller through the integrated MII.

2.5 EXPANSION BOOT ROM/FLASH

The PCnet-FAST board can accommodate up to 256K bits of Boot ROM Code. An external latch is used to allow Boot ROM Address and Data Latching when $\overline{AS_EBOE}$ is asserted. The PCnet-FAST board supports EPROM or Flash as an Expansion boot ROM device. Both are configured using the same methods and operate the same way.

2.6 SRAM INTERFACE

When using the controller in a 100-Mbps environment, additional frame buffering capability is provided by a 16-bit wide SRAM interface which provides high performance and high latency tolerance on the system bus and network. The controller can use up to 128 Kbytes of SRAM as an extension of its dual transmit and receive FIFOs. When no SRAM is used, the Am79C971 controller's FIFOs are programmed to bypass the SRAM interface.

2.7 SERIAL EEPROM INTERFACE

The PCnet-FAST board stores the unique IEEE physical address and bus configuration of each node in the serial EEPROM. Once powered up, the Am79C971 chip automatically detects the presence of the EEPROM and reads the 32 words stored in it through the MicroWire interface protocol. For details of the MicroWire interface, refer to the Am79C971 data sheet. The interface also supports the WRITE operation to the EEPROM.

2.8 AUTO-NEGOTIATION CONTROL

The PCnet-FAST board implements the Auto-Negotiation standard per the IEEE 802.3 specification for the 10BASE-T Media Attachment Unit (MAU) and the MII port. Auto-Negotiation automatically configures the link between two link partners through the Fast Link Pulse. The Fast Link Pulse is made up of a train of 17 clocks alternating with the 16 data fields for a total of 33 pulses. The two link partners send information in the 16 data positions between themselves. Both sides look to see what is possible and then connect at the greatest speed and capability (without any software support) as shown in the table below. The Auto-Negotiation capabilities for the PCnet-FAST board are as follows:

Table 2-1 Auto-Negotiation Capabilities

Network Speed	Physical Network Type
200 Mbps	100BASE-TX, Full Duplex
100 Mbps	100BASE-TX, Half Duplex
20 Mbps	10BASE-T, Full Duplex
10 Mbps	10BASE-T, Half Duplex

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