National Semiconductor

DP83840
10/100 Mb/s Ethernet Physical Layer

General Description

The DP83840 is a Physical Layer device for Ethernet 10BASE-T and 100BASE-X using category 5 Unshielded, Type 1 Shielded and Fiber Optic cables.

This VLSI device is designed for easy implementation of 10/100 Mb/s Ethernet LANs. It interfaces to the PMD sub-layer through National Semiconductor's DP83223 Twisted Pair Transceiver, and to the MAC layer through a Media Independent Interface (MII), ensuring interoperability between products from different vendors.

The DP83840 is designed with National Semiconductor's BiCMOS process. Its system architecture is based on the integration of several of National Semiconductor's industry proven core technologies as listed below:

— 10BASE-T ENDEC/Transceiver module to provide the 10 Mb/s IEEE 802.3 functions

— Clock Recovery/Generator Modules from National Semiconductor's leading FDDI product

— FDDI Stream Cipher (Cyclone)

— 100BASE-X physical coding sub-layer (PCS) and control logic that integrate the core modules into a dual speed Ethernet physical layer controller

Features

■ IEEE 802.3 10BASE-T compatible—ENDEC and UTP/STP transceivers and filters built-in

■ IEEE 802.3u 100BASE-X compatible—support for 2 pair Category 5 UTP (100m), Type 1 STP and Fiber Optic Transceivers—Connects directly to the DP83223 Twisted Pair Transceiver

■ ANSI X3T12 TP-PMD compatible

■ IEEE 802.3u Auto-Negotiation for automatic speed selection

■ IEEE 802.3u compatible Media Independent Interface (MII) with Serial Management Interface

■ Integrated high performance 100 Mb/s clock recovery circuitry requiring no external filters

■ Full Duplex support for 10 and 100 Mb/s

■ MII Serial 10 Mb/s output mode

■ Fully configurable node and repeater modes—allows operation in either application

■ Programmable loopback modes for easy system diagnostics

■ Flexible LED support

■ IEEE 1149.1 Standard Test Access Port and Boundary-Scan compatible
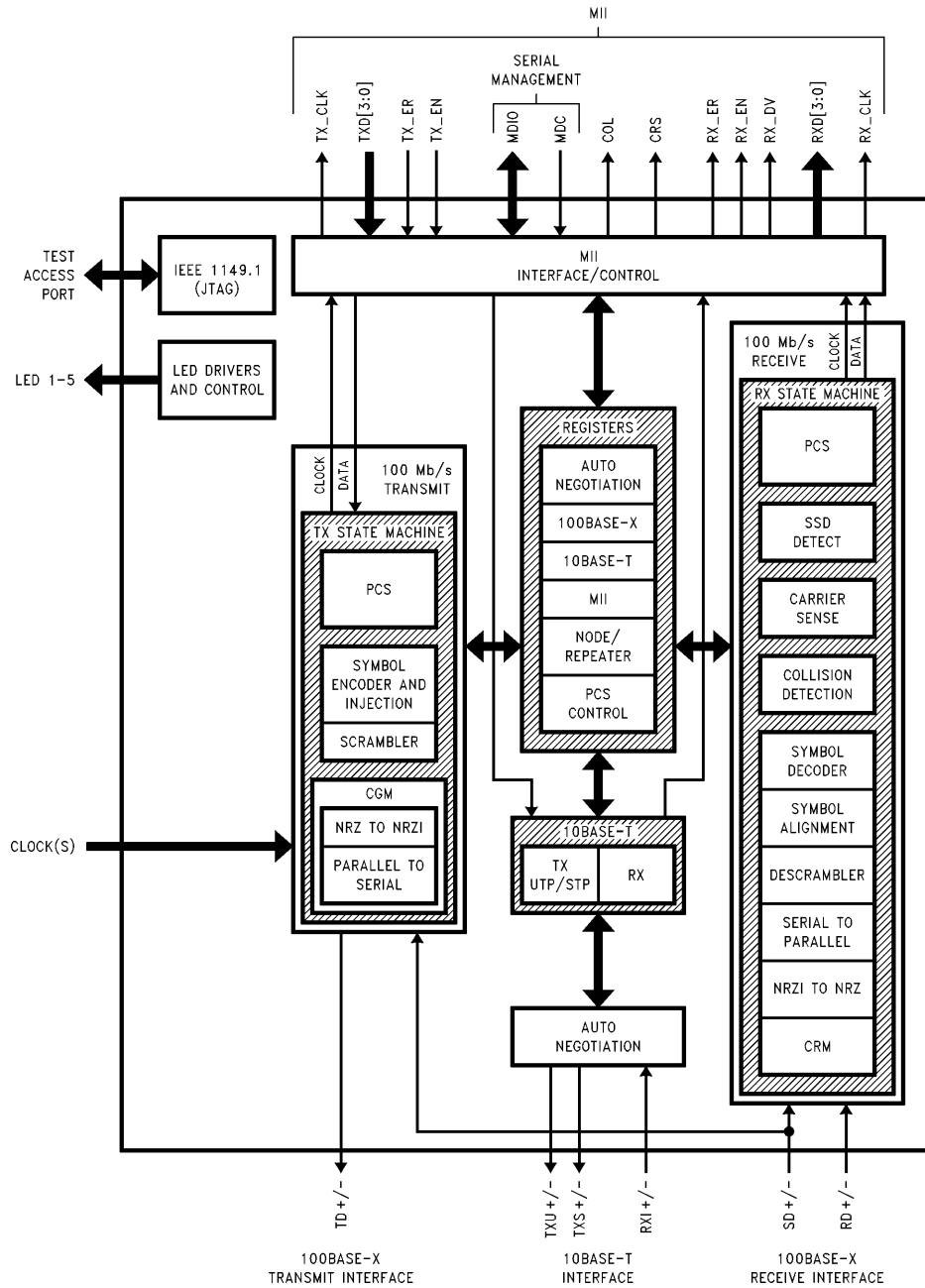
■ Small footprint 100-pin PQFP package

System Diagram
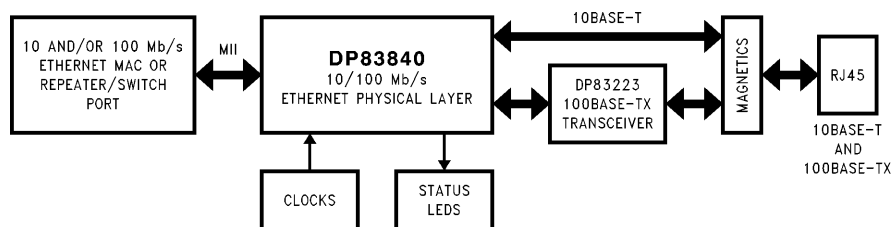
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U.S. Patents Pending

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Block Diagram

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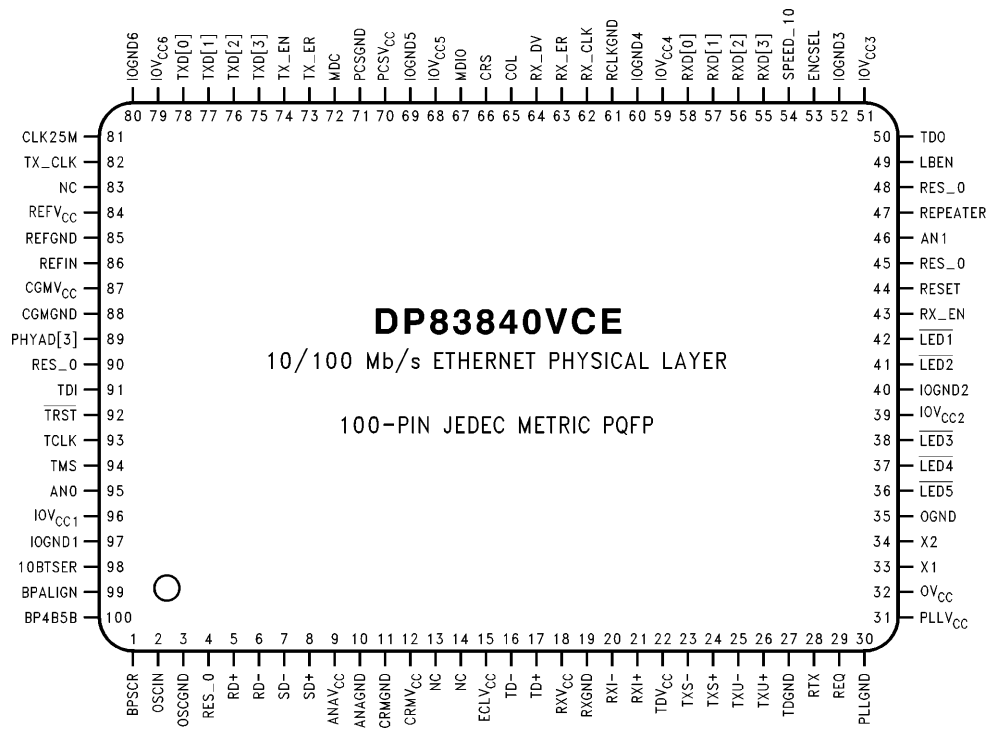
1.0 Pin Connection Diagram

FIGURE 1. DP83840 Pin Connection Diagram

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2.0 Pin Description

The DP83840 pins are classified into the following interface categories (each interface is described in the sections that follow):

MII INTERFACE

100 Mb/s SERIAL PMD INTERFACE

10 Mb/s INTERFACE

CLOCK INTERFACE

DEVICE CONFIGURATION INTERFACE

LED INTERFACE

IEEE 1149.1 INTERFACE

PHY ADDRESS INTERFACE

MISCELLANEOUS PINS

POWER AND GROUND PINS

SPECIAL CONNECT PINS

2.1 MII INTERFACE

Signal Name	Type	Pin #	Description
TX_CLK	O, Z	82	**TRANSMIT CLOCK:** Transmit clock output from the DP83840: — 25 MHz nibble transmit clock derived from Clock Generator Module's (CGM) PLL in 100BASE-TX mode — 2.5 MHz transmit clock in 10BASE-T nibble mode — 10 MHz transmit clock in 10BASE-T serial mode
TXD[3] TXD[2] TXD[1] TXD[0]	I, J	75 76 77 78	**TRANSMIT DATA:** Transmit data input pins for nibble data from the MII in 100 Mb/s or 10 Mb/s nibble mode (25 MHz for 100 Mb/s mode, 2.5 MHz for 10 Mb/s nibble mode). In 10 Mb/s serial mode, the TXD[0] pin is used as the serial data input pin. TXD[3:1] are ignored.
TX_EN	I, J	74	**TRANSMIT ENABLE:** Active high input indicates the presence of valid nibble data on TXD[3:0] for both 100 Mb/s or 10 Mb/s nibble mode. In 10 Mb/s serial mode, active high indicates the presence of valid 10 Mb/s data on TXD[0].
TX_ER	I, J	73	**TRANSMIT ERROR:** In 100 Mb/s mode, when this signal is high and TX_EN is active the HALT symbol is substituted for the actual data nibble. In 10 Mb/s mode, this input is ignored. In encoder bypass mode (BP_4B5B or BP_ALIGN) TX_ER becomes the TXD[4] pin, the fifth TXD data bit.
MDC	I, J	72	**MANAGEMENT DATA CLOCK:** Synchronous clock to the MDIO management data input/output serial interface which may be asynchronous to transmit and receive clocks. The maximum clock rate is 2.5 MHz.
MDIO	I/O, J	67	**MANAGEMENT DATA I/O:** Bi-directional management instruction/data signal that may be sourced by the station management entity or the PHY. This pin requires a 4.7 kΩ pullup resistor.
CRS (PHYAD[2])	I/O, Z, J	66	**CARRIER SENSE:** This pin is asserted high to indicate the presence of carrier due to receive or transmit activities in 10BASE-T or 100BASE-X Half Duplex modes. In Repeater, Full Duplex, or Loopback mode a logic 1 indicates presence of carrier due only to receive activity. This is also the PHY address sensing (PHYAD[2]) pin for multiple PHY applications—see Section 2.8 for more details.
COL	O, Z, J	65	**COLLISION DETECT:** Asserted high to indicate detection of collision conditions in 10 Mb/s and 100 Mb/s Half Duplex modes. In 10BASE-T Half Duplex mode with Heartbeat asserted (bit 4, register 1Ch), it is also asserted for a duration of approximately 1 μs at the end of transmission to indicate CD heartbeat. In Full Duplex mode this signal is always logic 0. There is no heartbeat function in this mode.
RX_CLK	O, Z	62	**RECEIVE CLOCK:** Provides the recovered receive clock for different modes of operation: — 25 MHz nibble clock in 100 Mb/s mode — 2.5 MHz nibble clock in 10 Mb/s nibble mode — 10 MHz receive clock in 10 Mb/s serial mode

I = TTL/CMOS input   O = TTL/CMOS output   Z = TRI-STATE® output   J = IEEE 1149.1 pin

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