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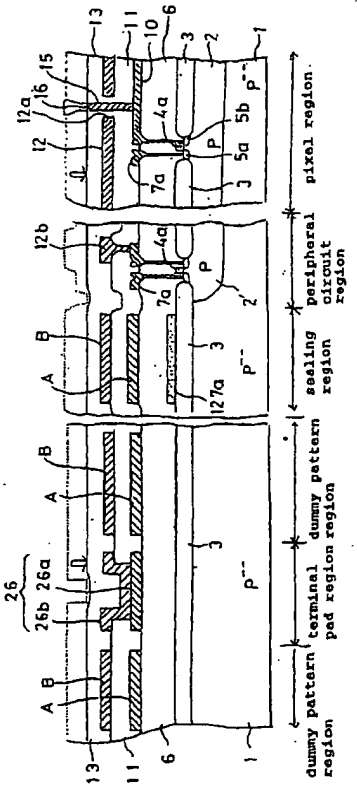
(54) Electro-optical device substrate and electro-optical device comprising such a substrate

(57) [Object] In a liquid crystal panel substrate having a layered film structure of interlayer insulation films and metal layers alternately formed on a semiconductor substrate provided with a transistor region for pixel selection thereon, to provide a configuration for achieving a uniform polishing rate without thickening of the interlayer insulation film to be polished.

[Solving Means] A liquid crystal panel substrate is provided with a shading film 12 composed of a second metal layer in a pixel region, a second interlayer insulation film 11 under the shading film, a wiring film 10 composed of a first metal layer under the second interlayer insulation film, a pixel electrode composed of a third metal layer on a third interlayer insulation film 13 on the shading film, and a connecting plug 15 connecting the wiring film 10 and the pixel electrode through an opening provided in the shading film 12. An lower dummy pattern A composed of the first metal layer and an upper dummy pattern B composed of the second metal layer are formed on the periphery of input terminal pads 26 in the non-pixel region. Since the surface level of the third interlayer insulation film 13 formed on the dummy patterns A and B is raised, excessive polishing is prevented at the position. As a result, a uniform polishing rate is achieved in CMP treatment.

[Fig. 2]



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Description

The present invention relates to substrates for electro-optical devices such as a reflective liquid crystal panel substrate, and particularly relates to an electro-optical device substrate comprising a pixel region formed on an element region for selecting a pixel.

The present applicant disclosed configurations of a liquid crystal panel substrate, a liquid crystal panel and a projection display device in Japanese Patent Application No. 8-279388 filed on October 22, 1996, as described below. The projection display device (liquid crystal projector) using a reflective liquid crystal panel as a light valve includes, as shown in Fig. 17, a light source 110 arranged along the system optical axis L_0, a polarized light illumination unit 100 including an integrator lens 120 and a polarized light converter 130; a polarized light beam splitter 200 for reflecting the S-polarized light beam emitted from the polarized light illumination unit 100 by an S-polarized light reflecting face 201; a dichroic mirror 412 for separating the blue light component (B) from the light reflected by the S-polarized light reflecting face 201 of the polarized light beam splitter 200; a reflective liquid crystal light valve 300B for modulating the separated blue light component (B); a dichroic mirror 413 for separating by reflection the red light component (R) from the light beams after separation of the blue light by a dichroic mirror 412; a reflective liquid crystal light valve 300R for modulating the separated red light component (R); a reflective liquid crystal light valve 300G for modulating the residual green light component (G) passing through the dichroic mirror 413; a projection optical system 500 including a projection lens for projecting synthesized light onto a screen 600, in which the light components modulated in the three reflective liquid crystal light valves 300R, 300G and 300B are synthesized by the dichroic mirrors 413 and 412 and the polarized light beam splitter 200 in their reverse paths. Reflective liquid crystal panels 30 shown in Fig. 18 as a cross-sectional view are used as the reflective liquid crystal light valves 300R, 300G and 300B.

The reflective liquid crystal panel 30 includes a reflective liquid crystal panel substrate 31 fixed with an adhesive on a supporting substrate 32 composed of glass or ceramic; a glass substrate 35 which is provided with a counter electrode (common electrode) 33 composed of a transparent conductive (ITO) film, and which lies at the incident light side, and is opposed with a gap to the reflective liquid crystal panel substrate 31 enclosed by a frame composed of a sealing agent 36; and a known twisted nematic (TN) liquid crystal or a super homeotropic (SH) liquid crystal 37 in which liquid crystal molecules are vertically aligned in a no-applied voltage state, the liquid crystal being sealed in the space enclosed by the sealing agent 36 between the reflective liquid crystal panel substrate 31 and the glass substrate 35.

Fig. 19 is a plan view of an enlarged layout of a reflective liquid crystal panel substrate 31 used in the reflective liquid crystal panel 30. The reflective liquid crystal panel substrate 31 includes a rectangular pixel region (display region) 20 provided with pixel electrodes disposed in matrix 14 shown in Fig. 18; gate line driver circuits (Y drivers) 22R and 22L lying at the exteriors of the right and left sides of the pixel region 20 for scanning gate lines (scanning electrodes or line electrodes); a precharging/testing circuit 23 lying at the exteriors of the upper side of the pixel electrode 14 for data lines (signal electrodes or column electrodes); an image signal sampling circuit 24 lying at the exterior of the bottom side of the pixel electrode 14 for supplying image signals to the data lines in response to the image data; a sealing region 27 with a frame shape lying at the exterior of the gate line drivers 22R and 22L, the precharging/testing circuit 23 and the image signal sampling circuit 24, for placing a sealing agent 36; a plurality of terminal pads 26 arranged along the bottom end and connected to a flexible tape wiring 39 with an anisotropic conductive film (ACF) 38 therebetween; a data line driver circuit(X driver) 21 lying between the terminal pad array 26 and the sealing region 27 for supplying image signals to data lines in response to the image data; and relay terminal pads (so-called silver points) 29R and 29L lying beside both ends of the data line driver circuit 21 for energizing the counter electrode 33 on the glass substrate 35.

The peripheral circuits (the gate line driver circuits 22R and 22L, the precharging/testing circuit 23 and the image signal sampling circuit 24) lying at the interior of the sealing region 27 have a shading film 25 (refer to Fig. 18) to shield from the incident light, which is the same as the pixel electrode 14 of the topmost layer.

Fig. 20 is an enlarged partial plan view of the pixel region 20 of the reflective liquid crystal panel substrate 31, and Fig. 21 is a cross-sectional view taken along the line A-A' of Fig. 20. In Fig. 21, numeral 1 represents a single-crystal silicon P^- semiconductor substrate (an N^- semiconductor substrate is also available) having a side of 20 mm. Numeral 2 represents a P-type well region formed on the top surface (main face) in the device-forming region (MOSFET etc.) of the semiconductor substrate 1, and numeral 3 represents a field oxide film (so-called LOCOS) which is formed for separating devices in the non-element-forming region of the semiconductor substrate 1. The p-type well region 2 shown in Fig. 21 is formed as a common well region for the pixel region 20 provided with a matrix of pixels having dimensions of, for example, 768x1024, and it is separated from a P-type well region 2' (refer to Fig. 22) for fabricating the devices of the peripheral circuits (the gate line driver circuits 22R and 22L, the precharging/testing circuit 23, the image signal sampling circuit 24 and the data line driver 21).

The field oxide film 3 is provided with two openings in the divided region of each pixel. A gate electrode 4a composed of polycrystalline silicon or a metal silicide is formed via a gate insulating film 4b in the center of one

opening; an N^+ source region 5a, and an N^+ drain region 5b formed on the P-type well region 2 at the both sides of the gate electrode 4a form a N-channel MOSFET (insulated-gate field effect transistor) for pixel selection together with the gate electrode 4a. Gate electrodes 4a in a plurality of pixels arrayed in a line extend in the scanning line direction (the line direction of the pixels) to form gate lines 4.

A P-type capacitor electrode region 8, which is common to the line direction, is formed on the P-type well region 2 in the other opening; a capacitor electrode 9a composed of polycrystalline silicon or a metal silicide formed on the P-type capacitor electrode region 8 with an insulating film (dielectric film) 9b therebetween forms a retention capacitor C for retaining a signal selected by the MOSFET for pixel selection together with the P-type capacitor electrode region 8.

A first interlayer insulation film 6 is formed on the gate electrode 4a and the capacitor electrode 9a, and a first metal layer composed mainly of aluminum is formed on the insulating film 6.

The first metal layer includes a data line 7 (refer to Fig.20) extending in the column direction, a source electrode wiring 7a, which protrudes from the data line 7 in a comb shape and is brought into conductive contact with a source region 4b through a contact hole 6a, and a relay wiring 10 which is brought into conductive contact with the drain region 5b through a contact hole 6b and with the capacitor electrode 9a through a contact hole 6c.

A second interlayer insulation film 11 is formed on the first metal layer which forms the data line 7, the source electrode wiring 7a, and the relay wiring 10, and a second metal layer essentially consisted of aluminum is formed on the second interlayer insulation film 11. The second metal layer includes a shading film 12 to cover the entire pixel region 20. The second metal layer as the shading film 12 forms a wiring 12b (refer to Fig. 22) for connecting the devices in the peripheral circuits (the gate line driver circuits 22R and 22L, the precharging/testing circuit 23, the image signal sampling circuit 24 and the data line driver circuit 21) formed on the periphery of the pixel region 20.

A plug hole 12a is provided at a position of the shading film 12 corresponding to the relay wiring 10. A third interlayer insulation film 13 is formed on the shading film 12, and a rectangular pixel electrode 14 which substantially corresponds to one pixel is formed as a reflective electrode on the interlayer insulation film 13. A contact hole 16 is formed through the third and second interlayer insulation films 13 and 11 so that it is located inside the opening 12a. After the contact hole 16 is filled with a high-melting-point metal such as tungsten by a CVD process, the high-melting-point metal layer formed on the third interlayer insulation film 13 and the front face of the interlayer insulation film 13 are flattened to form a mirror surface by a chemomechanical polishing (CMP) process. Next, an aluminum layer is formed by a low temperature sputtering process and a rectangular pixel electrode 14 with a side of 15 μm to 20 μm is formed by a patterning process. The relay wiring 10 and the pixel electrode 14 are electrically connected by a pillar connecting plug (interlayer conductive section) 15. A passivating film 17 is formed on the entire pixel electrode 14.

Alternatively, the connecting plug 15 may be formed by planarizing the third interlayer insulation film 13 by a CMP process, providing a contact hole and burying a high-melting-point metal such as tungsten.

The planarization of the third interlayer insulation film 13 by the CMP process is essential for depositing a pixel electrode 14 with a mirror surface as a reflective electrode on each pixel. The process is also essential for the formation of a dielectric mirror film on the pixel electrode 14 with a protective film therebetween. The CMP process uses a slurry (polishing liquid) composed of components which simultaneously prompt chemical etching and mechanical polishing of a wafer before scribing.

In the pixel region 20, however, the MOSFET for pixel selection, the electrode wirings 7a and 10 of the retention capacitor C and the shading film 12 are formed as underlying layers. Also, as shown in Fig. 22, in the peripheral circuit region (the gate line driver circuits 22R and 22L, the precharging/testing circuit 23, the image signal sampling circuit 24 and the data line driver circuit 21), the electrode wirings 7a and the wiring 12b between the devices are formed as underlying layers. Further, in the region of the terminal pad 26, an lower layer film 26a composed of the first metal layer and an upper layer film 26b composed of the second metal layer are formed. As a result, immediately after the deposition of the third interlayer insulation film 13, the surface level 13a represented by a broken line in Fig. 22 rises up at the pixel region, the peripheral circuit region and the terminal pad region. When polishing the surface of the third interlayer insulation film 13 having such large unevenness by the CMP process, the finished level 13b after polishing represented by the solid line in Fig. 22 reflects the original surface level 13a represented by the broken line. According to intensive investigations by the present inventor, it is clarified that the surface planarization of the third interlayer insulation film 13 on the pixel region is particularly important in the liquid crystal panel substrate 31 subjected to such polishing treatment.

Japanese Unexamined Patent Publication No. 9-68718 discloses a technology for planarization of the third interlayer insulation film 13 on the pixel region 20, in which discrete dummy patterns of the metal layer for individual pixels are provided between the first metal layer, such as the relay wiring 10, and the second metal layer (shading layer) to raise the level in order to suppress the entire surface unevenness of the shading film 12. When the intermediate metal layer is formed only for raising the level for each pixel, an additional step for depositing an interlayer insulation film should be incorporated. When the surface unevenness of the interlayer

insulation film is reduced before polishing, the initial polishing rate in the CMP treatment unintentionally decreases, and thus planarization of the interlayer insulation film 13 to form a mirror surface requires a long polishing time and a large amount of polishing liquid. The deposition of dummy patterns on individual pixels in the pixel region 20 therefore has a disadvantage in the production process, resulting in increased production costs.

[Problems to be Solved by the Invention]

Fig. 23 is a contour plot of film illustrating the thickness distribution of the third interlayer insulation film 13 after polishing of the liquid crystal panel substrate 31, in which the third interlayer insulation film 13 with a thickness of approximately 24,000 Å is formed and then subjected to the CMP treatment until the residual thickness of the third interlayer insulation film 13 reaches approximately 12,000 Å in the center of the pixel region 20. In Fig. 24, a graph depicted by marks × shows the residual thickness distribution of the left seal in the vertical direction taken along line a-a' of Fig. 23. In Fig. 25, a graph depicted by marks × shows the residual thickness distribution of the central pixel in the vertical direction taken along line b-b' of Fig. 23. In Fig. 26, a graph depicted by marks × shows the residual thickness distribution of the upper seal in the transverse direction taken along line c-c' of Fig. 23. In Fig. 27, a graph depicted by marks x shows the residual thickness distribution of the central pixel in the transverse direction taken along line d-d' of Fig. 23. In Fig. 28, a graph depicted by marks × shows the residual thickness distribution of the lower sealing region in the transverse direction taken along line e-e' of Fig. 23.

As shown in Figs. 23 to 28, the maximum difference in the thickness is approximately 6,120 Å in the pixel region 20 and the sealing region 27, hence the substrate including the pixel region 20 and sealing region 27 as a whole is not sufficiently flattened. The periphery of the terminal pad 26 and the upper and lower centers of the sealing regions 27 are excessively polished, whereas the right and left centers of the sealing region 27 are insufficiently polished.

As shown in Fig. 22, since the protruding terminal pads 26 in spot shape are discretely arranged as an array in the terminal pad region, the protruding sections 13c covered with the third interlayer insulation film 13 will be rapidly polished. The region of the terminal pad 26 therefore has a higher initial polishing rate than that of the pixel region 20. Accordingly, the region of the terminal pad 26 may be excessively polished to expose the underlying layer (upper layer film 26b) before the pixel region 20 is sufficiently flattened.

A means for compensating for the excessive polishing of the terminal pad 26 includes thick deposition of the third interlayer insulation film 13. According to this method, even if the region of the terminal pad 26 is rapidly polished, planarization of the third interlayer insulation film 13 is almost completed in this region before the underlying layer is exposed, hence the polishing rate significantly decreases compared with the initial polishing rate. As a result, the pixel region 20 can be flattened by spending an increased polishing time without exposing the underlying layer.

The formation of the thick third interlayer insulation film 13 causes an increased depth of the contact hole for the connecting plug 15, and it is difficult to embed the contact hole 16 with the high-melting-point metal which constitutes the connecting plug 15 as a result of such a high aspect ratio. The contact hole 16 originally has a large depth because the connecting plug 15 is a conductive section skipping an interlayer, which is formed through the second interlayer insulation film 11, the shading layer 12 and the third interlayer insulation film 13, and reaches the pixel electrode 14. Further, the opening 12a and thus the diameter of the contact hole 16 must be reduced in order to prevent leakage of the light entering from the gap between the pixel electrodes 14 to the devices such as MOSFET and the like through the opening 12a. The contact hole 16 inevitably has a high aspect ratio. Thinning of the interlayer insulation film 13 to be polished is therefore required. As described above, however, the CMP process excessively polishes the third interlayer insulation film 13 in the region of the terminal pad 26.

Since the thickness of the upper and lower centers of the sealing region 27 is smaller than that of the pixel region because of excessive polishing in the region of the terminal pad 26, the upper and lower edges of the pixel region 20 and the upper and lower center of the sealing region 27 are excessively polished, as shown in Fig. 26 and 28. The four corners of the sealing region 27 at the right and left sides will have also small thicknesses because of the excessive polishing of the region of the terminal pad 26, whereas the right and left centers of the sealing region 27 are hardly polished because of a low initial polishing rate caused by the flatness of the sealing region 27 before polishing. As a result, the right and left sides of the sealing region 27 and the right and left edges of the pixel region 20 are insufficiently polished in their central portions. When the peripheral edges of the pixel region 20 and the sealing region 27 have such tilted faces, the reflectance of the pixel electrode 14 formed on the third interlayer insulation film 13 after polishing decreases, the cell gap is adjusted with difficulty in the liquid crystal assembly, and the sealing agent has unsatisfactory adhesiveness. When the contact hole 16 for the connecting plug 15 is provided after the CMP treatment, it is difficult to optimize the etching time for the contact hole because of the uneven thickness.

In view of the incompatible problems regarding the interlayer insulation film formed between the shading film and the pixel electrode and requiring the polishing treatment in the reflective liquid crystal panel substrate, a first object of the present invention is to provide an

electro-optical device substrate, such as a liquid crystal panel substrate, comprising a layered film structure of a plurality of interlayer insulation films and a plurality of conductive layers alternately formed in a pixel region formed on a substrate, wherein the electro-optical substrate has a structure requiring no additional deposition step and having a uniform polishing rate for the interlayer insulation film without thickening of the interlayer insulation film.

A second object of the present invention is to provide an electro-optical device substrate, such as a liquid crystal panel substrate, which has a flattened polished surface of the interlayer insulation film in the sealing region as well as in the pixel region, an improved reflectance of the pixel electrode, and which permits ready adjustment of the cell gap, improved adhesiveness of the sealing agent, and an optimized etching time of the contact hole.

Embodiments of the present invention will now be described by way of example only and with reference to the accompanying drawings, in which:

Fig. 1 is a plan view of a layout of a reflective liquid crystal panel substrate for a reflective liquid crystal panel in accordance with Embodiment 1 of the present invention.

Fig. 2 is a cross-sectional view taken along the line B-B' in Fig. 1.

Fig. 3 is a cross-sectional view of another configuration of the input terminal pad corresponding to the sectional structure in Fig.1.

Fig. 4 is a partial plan view near the pixel region and the sealing region in the reflective liquid crystal panel substrate in Embodiment 1.

Fig. 5 is a partial plan view near the data line driver circuit in the reflective liquid crystal panel substrate in Embodiment 1.

Fig. 6 is a partial plan view near the terminal pads in the reflective liquid crystal panel substrate in Embodiment 1.

Fig. 7 is a partial plan view illustrating connection between the terminal pads and flexible tape wiring in the reflective liquid crystal panel substrate in Embodiment 1.

Fig. 8 is a cross-sectional view taken along the line A-A' in Fig. 7.

Fig. 9 is a partial plan view of the periphery of the relay terminal pad in the reflective liquid crystal panel substrate in accordance with Embodiment 1.

Fig. 10 is a contour plot of film illustrating the thickness distribution of the third interlayer insulation film after polishing of the liquid crystal panel substrate in accordance with Embodiment 1, in which the third interlayer insulation film with a thickness of approximately 24,000 Å is formed and then subjected to the CMP treatment until the residual thickness of the third interlayer insulation film reaches approximately 12,000 Å in the center of the pixel region.

Fig. 11 is a partial plan view of the four-corner portion of the sealing region in a reflective liquid crystal panel substrate in accordance with Embodiment 2 of the present invention.

Fig. 12 is a cross-sectional view taken along the line C-C' in Fig. 11.

Fig. 13 is a contour plot of film illustrating the thickness distribution of the third interlayer insulation film after polishing of the liquid crystal panel substrate in accordance with Embodiment 2, in which the third interlayer insulation film with a thickness of approximately 24,000 Å is formed and then subjected to the CMP treatment until the residual thickness of the third interlayer insulation film reaches approximately 12,000 Å in the center of the pixel region.

Fig. 14 is a partial plan view of the four-corner portion of the sealing region in a reflective liquid crystal panel substrate in accordance with Embodiment 3 of the present invention.

Fig. 15 is a cross-sectional view taken along the line C-C' in Fig. 14.

Fig. 16 is a contour plot of film illustrating the thickness distribution of the third interlayer insulation film after polishing of the liquid crystal panel substrate in accordance with Embodiment 3, in which the third interlayer insulation film with a thickness of approximately 24,000 Å is formed and then subjected to the CMP treatment until the residual thickness of the third interlayer insulation film reaches approximately 12,000 Å in the center of the pixel region.

Fig. 17 is a schematic diagram of a video projector as an example of a projection display device using a reflective liquid crystal panel as a light valve.

Fig. 18 is a cross-sectional view of a reflective liquid crystal panel.

Fig. 19 is a plan view of a reflective liquid crystal panel substrate used in a conventional reflective liquid crystal panel.

Fig. 20 is a partial plan view of the pixel region of the reflective liquid crystal panel substrate in Fig. 19.

Fig. 21 is a cross-sectional view taken along the line A-A' of Fig. 13.

Fig. 22 is a cross-sectional view taken along the line B-B' of Fig. 12.

Fig. 23 is a contour plot of film illustrating the thickness distribution of the third interlayer insulation film after polishing of the conventional reflective liquid crystal panel substrate shown in Fig.19, in which the third interlayer insulation film with a thickness of approximately 24,000 Å is formed and then subjected to the CMP treatment until the residual thickness of the third interlayer insulation film reaches approximately 12,000 Å in the center of the pixel region.

Fig. 24 is a graph of residual film thickness distributions in the vertical direction of the left side of the seal taken along the line a-a' in the conventional embodiment in Fig. 23, Embodiment 1 in Fig. 10, Embodiment 2 in Fig. 13 and Embodiment 3 in Fig. 16.

Fig. 25 is a graph of residual film thickness distribu-

tions in the vertical direction of the pixel center taken along the line b-b' in the conventional embodiment in Fig. 23, Embodiment 1 in Fig. 10, Embodiment 2 in Fig. 13 and Embodiment 3 in Fig. 16.

Fig. 26 is a graph of residual film thickness distributions in the transverse direction of the upper side of the seal taken along the line c-c' in the conventional embodiment in Fig. 23, Embodiment 1 in Fig. 10, Embodiment 2 in Fig. 13 and Embodiment 3 in Fig. 16.

Fig. 27 is a graph of residual film thickness distributions in the transverse direction of the pixel center taken along the line d-d' in the conventional embodiment in Fig. 23, Embodiment 1 in Fig. 10, Embodiment 2 in Fig. 13 and Embodiment 3 in Fig. 16.

Fig. 28 is a graph of residual film thickness distributions in the transverse direction of the pixel center taken along the line e-e' in the conventional embodiment in Fig. 23, Embodiment 1 in Fig. 10, Embodiment 2 in Fig. 13 and Embodiment 3 in Fig. 16. In a first means in the present invention for achieving the first object, in order to flatten the surface level of the unpolished interlayer insulation film as uniformly as possible, a dummy pattern for raising the level of an interlayer insulation film to be polished is formed on the entire exterior of the pixel region by using the previously formed wiring layer, instead of on the space in the pixel region. That is, the arrangement is characterized by an electro-optical device substrate comprising a layered film structure of a plurality of interlayer insulation films and a plurality of conductive layers alternately formed in a pixel region, in which a switching element is arranged on the substrate in response to each pixel, at least one interlayer insulation film below the top conductive layer among the plurality of conductive layers being flattened by polishing; the substrate being characterized in that a dummy pattern with a single or a plurality of layers comprising the conductive layers below said interlayer insulation film subjected to the polishing is provided near at least a terminal pad formed at a non-pixel region on the substrate. The terminal pad includes an input terminal pad arranged near the edge of the substrate and a relay terminal pad provided at the inner position of the substrate.

Since the surface level of the formed interlayer insulation film to be polished is raised near the terminal pad in such a configuration of the dummy pattern provided near the terminal pad, the surface level is substantially the same as the surface level of the interlayer insulation film to be polished in the pixel region, and thus the surface level is made uniform over the entire surface. The uniform surface has a uniform polishing rate in chemomechanical polishing (CMP) or the like without prompted polishing near and outside the terminal pad region and the polished surface of the interlayer insulation film is more flattened than conventional surfaces. As a result, the pixel region is more satisfactorily flattened, control of the cell gap is improved in cell assembly using a counter substrate, and the etching time for the contact holes of the interlayer conductive portion etc., in the pixel region after polishing is easily determined.

Such a uniform polished surface prevents exposition of the underlying terminal pad layer due to excessive polishing at the terminal pad portion, and can achieve thinning of the unpolished interlayer insulation film. Since the aspect ratio of the contact hole at the interlayer conductive portion in the pixel electrode is improved by the thinning, an opening portion with a small diameter is achieved by a contact hole with a small diameter. As a result, shading characteristics are improved.

The interlayer conductive portion electrically connects the first conductive layer connecting to the switching element and the upper conductive layer formed on the interlayer insulation film to be polished, and the dummy pattern may be any one of a first dummy pattern composed of the first conductive layer, a second dummy pattern composed of the second conductive layer which is formed between the first conductive layer and the upper conductive layer such as the shielding film, and a composite thereof.

When a conductive dummy pattern lies near the terminal pads outside the pixel region, the dummy pattern functions as a shading film, hence it prevents the invasion of stray light from the exterior of the pixel region into the pixel region on the substrate, resulting in a suppressed photocurrent flow and an improved switching element.

Since the input terminal pad is connected to the external wiring by thermocompression bonding using an anisotropic conductive film, conductive particles damage the thinned interlayer insulation film after polishing over the dummy pattern region, and short-circuiting to the input terminal pad will occur. When a dummy pattern is formed over the almost entire range other than extract wiring region near the input terminal pads, two adjacent input terminal pads will cause short-circuiting through the dummy pattern.

In the present invention, the dummy pattern arranged on the periphery of the input terminal pads is composed of a plurality of divisional dummy pattern, hence the surface level of the formed interlayer insulation film to be polished is made uniform without short-circuiting between the adjacent terminal pads. The probability of the short-circuiting decreases as the number of divisional dummy patterns increases.

It is preferable that a non-dummy pattern region be provided between two adjacent input terminal pads. The non-dummy pattern region adjoins the wire of the flexible tape wiring which is compressed during the thermocompression bonding. If the dummy patterns are continuously formed, conductive particles in the anisotropic conductive film will raise the probability of short-circuiting between a terminal pad and dummy pattern, causing short-cutting between two terminal pads through the dummy pattern. The formation of the non-dummy pattern can securely prevent such undesirable

short-circuiting.

The distance between the input terminal pad and the divisional dummy pattern on its periphery is set to be larger than the distance between the wiring and the dummy pattern near the wiring in order to prevent as much as possible bridging and thus short-circuiting between the input terminal pad and the divisional dummy pattern through the conductive particles in the anisotropic conductive film.

The distance between the relay terminal pad and the dummy pattern on its periphery is set to be larger than the distance between the wiring and the dummy pattern near the wiring . Generally silver paste causes conduction on the relay terminal pad. Silver paste on the relay terminal pad will not cause short-circuiting to the dummy pattern near the relay terminal pad even if the silver paste slightly spreads out of the relay terminal pad.

In order to achieve the second object, a second means of the present invention is characterized in that dummy patterns composed of a single or plural conductive layers lying under the interlayer insulation film to be polished are provided on the sealing region surrounding the pixel region as well as near the terminal pad. When no dummy pattern is provided in the sealing region, the interlayer insulation film tends to have a slanted surface at the periphery of the pixel region before polishing. Such a slanted surface causes a low reflectance of the shading film of the upper conductive layer and a difficulty in optimization of the etching time for the formation of the hole due to an uneven thickness of the interlayer insulation film after polishing. The provision of the dummy pattern can solve such problems. The surface level of the unpolished interlayer insulation film is substantially uniform over the entire region, including the sealing region, near the pixel region, hence the polished interlayer insulation film barely has a slanted surface and an uneven thickness in the pixel region.

If no dummy pattern is provided at the exterior of the sealing region provided with a dummy pattern, the interlayer insulation film on the sealing region has a slanted surface after polishing. The slanted surface will disturb the control of the gap between two substrates (referred to as a cell gap) when adhering to the counter substrate in fabrication of an electro-optical device and cause a drawback to adhesiveness of the sealing agent.

It is preferable that a dummy pattern be provided at the peripheral region of the sealing region in order to solve these problems.

The dummy pattern may be the first dummy pattern composed of the first conductive layer electrically connected to the switching element, the second dummy pattern composed of the second conductive layer lying between the first conductive layer and the upper conductive layer such as the shading film, or a composite dummy pattern of the first and second dummy patterns.

Preferably, the dummy pattern provided at the sealing region and the peripheral region of the sealing region is formed on an isolated pattern which is the same layer as the control wiring layer of the switching element. Also, if required, the dummy pattern near the terminal pad region is preferably formed on an isolated pattern which is the same layer as the control wiring layer of the switching element. By using the pattern as a base plate for raising the bottom, planarization of the surface level of the polished interlayer insulation film can be more precisely controlled.

Further, the arrangement is characterized in that a single or plural dummy patterns composed of conductive layer underlying the interlayer insulation film to be polished are provided at the neighboring region of the driver circuit which is provided at the periphery of the pixel region and supplies signals to the switching element. The provision of the dummy pattern at the medial region between the sealing region and the pixel region helps planarization of the interlayer insulation film by polishing. The dummy pattern may be the first dummy pattern composed of the first conductive layer, the second dummy pattern composed of the second conductive layer, or a composite dummy pattern of the first and second dummy patterns.

Further, the arrangement is characterized in that a single or plural dummy patterns are provided at the corner region of the sealing region which is provided at the periphery of the pixel region , and the dummy patterns are composed of conductive layer underlying the interlayer insulation film to be polished and have a lower density than that of the periphery of a side region of the sealing region and the periphery of the corner region of the sealing region formed on the periphery of the pixel region. In the corner region of the sealing region, a plurality of divisional dummy patterns are distributed as groups, and the dummy patterns are different from wide continuous dummy patterns at the sealing side and on the periphery of the corner region. The surface roughness of the unpolished interlayer insulation film at the four-corner sealing portion is therefore reflected by the unevenness due to the divisional dummy patterns, and the four-corner portion has a higher initial polishing rate compared to the four-corner portion having a continuous wide dummy pattern. As a result, the polishing rate at the four-corner portion is equalized to that in the sealing region, and a change in residual thickness can be reduced in the pixel region and the sealing region.

The corner portion is indented and the boundary portion is cornered in the sealing region formed on the periphery of the pixel region, even when a single or plural dummy patterns composed of conductive layer underlying the interlayer insulation film to be polished are formed at the sealing region excluding the corner region, that is, even when no dummy pattern is formed at the four-corner portion. The boundary portion is therefore easily polished at the initial stage and a slanted surface is formed. The slanted surface gradually extends to the inner pixel region and the sealing region. Accordingly, the pixel region and the sealing region can be flattened

or planarized as a whole.

Such dummy patterns may be the first dummy pattern composed of the first conductive layer, the second dummy pattern composed of the second conductive layer, or a composite dummy pattern of the first and second dummy patterns.

Also, the arrangement is characterized in that a plurality of uneven pseudo pixel patterns including the conductive layer lying under the interlayer insulation film to be polished are formed at the non-pixel region on the substrate instead of the forming a continuous wide dummy pattern in the non-pixel region. In the substrate having uneven pseudo dummy patterns, since the unpolished interlayer insulation film at the non-pixel region and the pixel region have very similar uneven surface patterns, the initial polishing rate is almost equalized over the entire substrate and a highly precise surface flatness can be achieved at least in the pixel and sealing regions.

It is preferable that a plurality of uneven pseudo pixel patterns are formed repeatedly in the direction of two dimensions on the substrate such that the arrangement has spatial regularity. The regularity corresponds to the spatial regularity of the uneven pixel pattern such as matrix in the pixel region. The surface over the pixel region and the sealing region is further significantly flattened or planarized.

The uneven pseudo pixel pattern may be the first dummy pattern composed of the first conductive layer, the second dummy pattern composed of the second conductive layer, or a composite dummy pattern of the first and second dummy patterns. A pseudo pixel pattern including the pattern of the interlayer insulation film will more closely imitate the pixel pattern.

Preferably, the uneven pseudo pixel pattern is formed of at least a pseudo gate line and a pseudo data line. These form typical unevenness in the pixel and are concerned with regularity of unevenness in the pixel region.

An electro-optical device is fabricated using the electro-optical device substrate, and is suitable for use in display portions of various electronic devices, for example, a light valve of a projection display device.

The embodiments in accordance with the present invention will now be described with reference to the attached drawings.

[0050]

[Embodiment 1]

Fig. 1 is a plan view of a layout of a reflective liquid crystal panel substrate for a reflective liquid crystal panel in accordance with Embodiment 1 of the present invention, and Fig. 2 is a cross-sectional view taken along the line B-B' in Fig. 1.

The reflective liquid crystal panel substrate 131 in accordance with this embodiment shown in Fig. 1 includes, as in the conventional liquid crystal panel substrate 31 shown in Figs. 18 and 19, a rectangular pixel region (display region) 20 provided with a matrix of pixel electrodes 14 shown in Fig. 18; gate line driver circuits (Y drivers) 22R and 22L lying at the exteriors of the right and left sides of the pixel region 20 for scanning gate lines (scanning electrodes or line electrodes); a precharging/testing circuit 23 for data lines (signal electrodes or column electrodes); an image signal sampling circuit 24 lying at the exterior of the bottom side of the pixel electrodes 14 for supplying image signals to the data lines in response to the image data; a sealing region 127 lying at the exterior of the gate line driver circuits 22R and 22L, the precharging/testing circuit 23 and the image signal sampling circuit 24, for placing a sealing agent 36 (refer to Fig. 18); a plurality of terminal pads 26 arranged along the bottom end and adhesively connected to a flexible tape wiring with an anisotropic conductive film therebetween; a data line driver circuit(X driver) 21 lying between the terminal pad array 26 and the bottom side of the sealing region 127 for supplying sampling signals to the image signal sampling circuit 24; and relay terminal pads (so-called silver points) 29R and 29L lying beside both ends of the data line driver 21 for energizing the counter electrode 33 on the glass substrate 35. Each of the gate line driver circuits 22R and 22L and the data line driver circuit 21 has a shift register to supply scanning signals to the gate lines and sampling signals to the image signal sampling circuit 24, respectively, in response to transmission of shift data in the shift register. The signal sampling circuit 24 supplies image signals to the data lines in response to sampling signals.

In this embodiment, the sealing region 127 having a frame shape and surrounding the pixel region 20 forms an isolated wide-continuous dummy pattern region as shown by hatching. The input terminal pads 26, the relay terminal pads 29R and 29L and the data line driver circuit 21 are surrounded by the wide continuous dummy pattern region as shown by the hatching.

The plan and sectional configurations of the pixel region 20 of the panel substrate 131 are the same as those shown in Figs. 20 and 21, respectively. As shown in Fig. 2, a P-type well region 2 is formed on the top surface of a P^- semiconductor substrate 1 (a N^- semiconductor substrate is also available) composed of single-crystal silicon having a large size (a side of approximately 20 mm), and a field oxide film (so-called LOCOS film) 3 is formed thereon. The p-type well region 2 is formed as a common well region for the pixel region 20 provided with a matrix of pixels having dimensions of, for example, 768x1024, and it is separated from a P-type well region 2' for fabricating the devices of the peripheral circuits (the gate line driver circuits 22R and 22L, the precharging/testing circuit 23, the image signal sampling circuit 24 and the data line driver circuit 21).

The field oxide film 3 is provided with two openings at the divided region of each pixel. A gate electrode 4a

composed of polycrystalline silicon or a metal silicide is formed via a gate insulating film 4b in the center of one opening; an N^+ source region 5a, and an N^+ drain region 5b formed on the P-type well region 2 at the both sides of the gate electrode 4a form a switching element, that is, a N-channel MOSFET (insulated-gate field effect transistor) for pixel selection together with the gate electrode 4a. As shown in Fig. 20, the gate electrodes 4a in a plurality of pixels arrayed in a line extend in the scanning line direction (the line direction of the pixels) to form gate lines 4.

Although not shown in Fig. 2, a P-type capacitor electrode region 8, which is common to the line, is formed on the P-type well region 2 in the other opening. A capacitor electrode 9a composed of polycrystalline silicon or a metal silicide formed on the P-type capacitor electrode region 8 with an insulating film (dielectric film) 9b therebetween forms a retention capacitor (accumulating capacitor) C for retaining a signal selected by the MOSFET for pixel selection together with the P-type capacitor electrode region 8.

The retention capacitor 9a can be formed by a film deposition process for a polycrystalline silicon or metal silicide layer which functions as the gate electrode 4a in the MOSFET for pixel selection. The insulating film (dielectric film) 9b under the retention capacitor 9a can also be formed by an insulating film deposition process for the gate insulating film 4b. The insulating films 9b and 4b are formed by a thermal oxidation process and have thicknesses of approximately 400 Å to 800 Å. The capacitor electrode 9a and gate electrode 4a have a composite structure of a polycrystalline silicon layer with a thickness of 1,000 Å to 2,000Å and a silicide layer of a high melting point metal such as Mo or W having a thickness of 1,000 Å to 3,000 Å. The source and drain regions 5a and 5b are formed by a self-alignment ion implantation process of an N-type impurity on the surface of the substrate at both sides of the gate electrode 4a acting as a mask.

The P-type capacitor electrode region 8 is formed by a doping process including ion implantation and heat treatment(drive-in). Ion implantation may be performed before the gate electrode is formed. After the formation of the insulating film 9b, the same impurity as in the P-type well 2 is doped such that the surface of the P-type well 2 has a higher impurity content than its interior and forms a low resistance layer. The impurity content in the P-type well 2 is preferably 1×10^{17} cm^{-3} or less and more preferably ranges from 1×10^{16} cm^{-3} to 5×10^{16} cm^{-3}. The preferable impurity content in the source and drain regions 5a and 5b ranges from 1×10^{20} cm^{-3} to 3×10^{30} cm^{-3}. The preferable impurity content in the P-type capacitor electrode region 8 ranges from 1×10^{18} cm^{-3} to 5×10^{19} cm^{-3}, and more preferably from 1×10^{18} cm^{-3} to 1×10^{19} cm^{-3} in view of reliability and pressure resistance of the insulating film 9b as a constituent of the retention capacitor C.

A first interlayer insulation film 6 is formed on the gate electrode 4a and the capacitor electrode 9a, and a first conductive layer (hereinafter referred to as a first metal layer) essentially consisting of aluminum is formed on the insulating film 6. The first metal layer includes data lines 7 extending in the column direction (refer to Fig. 20), source electrode wirings 7a, which extend from the data line 7 like a comb and come into conductive contact with the source region 4a through a contact hole 6a, a relay wiring 10 coming into conductive contact with the drain region 5b through the contact hole 6b and with the capacitor electrode 9a through a contact hole 6c.

The first interlayer insulation film 6 is formed by, for example, depositing an HTO film (a silicon oxide film formed by a high-temperature CVD process) with a thickness of approximately 1,000 Å and depositing a BSPG film (a silicate glass film containing boron and phosphorus) with a thickness of approximately 8,000 Å to 10,000 Å. The first metal layer forming the source electrode wiring 7a and the relay wiring 10 has, for example, a quadrilayer structure composed of Ti/TiN/Al/TiN in that order from the bottom.

The bottom Ti layer has a thickness of approximately 100 Å to 600 Å, the second TiN layer has a thickness of approximately 1,000 Å, the third Al layer has a thickness of approximately 4,000 Å to 10,000 Å, and the top TiN layer has a thickness of approximately 300 Å to 600 Å.

A second interlayer insulation film 11 is formed on the first metal layer, and a second conductive layer (hereinafter referred to as a second metal layer) composed of aluminum is formed on the second interlayer insulation film 11. The second metal layer covers most of the pixel region 20 and includes a shading film 12 for shielding the spacing portion between two adjacent pixel electrodes 14. The second metal layer forming the shading film 12 is used as a connecting wiring 12b (refer to Fig. 2) in the peripheral circuits (the gate line driver circuits 22R and 22L, the precharging/testing circuit 23, the image signal sampling circuit 24 and the data line driver circuit 21).

The second interlayer insulation film 11 is formed by, for example, depositing a silicon oxide film (hereinafter referred to as TEOS film) with a thickness of approximately 3,000 Å to 6,000 Å from tetraethyl ortho-silicate (TEOS) by a plasma CVD process, depositing a spin-on-glass (SOG) film thereon, etching it by an etch-back process, and depositing a second TEOS film with a thickness of approximately 2,000 Å to 5,000 Å thereon.

The second metal layer forming the shading film 12 and the like may have the same configuration as the first metal layer, for example, a quadrilayer structure of Ti/TiN/Al/TiN formed from the bottom.

The bottom Ti layer has a thickness of approximately 100 Å to 600 Å, the second TiN layer has a thickness of approximately 1,000 Å, the third Al layer has a thickness of approximately 4,000 Å to 10,000 Å, and the top TiN layer has a thickness of approximately 300 Å to 600

Å.

A plug hole 12a is provided at a position of the shading film 12 corresponding to the relay wiring 10. A third interlayer insulation film 13 is formed on the shading film 12, and a rectangular pixel electrode 14 which substantially corresponds to one pixel is formed as a reflective electrode on the interlayer insulation film 13. The third interlayer insulation film may be formed as in the second interlayer insulation film 11, that is, by depositing a TEOS film with a thickness of approximately 3,000 Å to 6,000 Å, depositing a SOG film thereon, etching it by an etch-back process, ana depositing a second TEOS film with a thickness of approximately 16,000 Å to 24,000 Å. Alternatively, the third interlayer insulation film may be formed of only the TEOS film instead of the SOG film interposed between two TEOS films. The thickness in this case preferably ranges from 16,000 Å to 24,000 Å. A silicon nitride film may be formed under or on the TEOS film in order to improve humidity resistance. When the silicon nitride film is the upper layer, the TEOS film is flattened by a CMP process before depositing the silicon nitride film or the silicon nitride film is flattened by a CMP process.

A contact hole 16 is formed through the third and second interlayer insulation films 13 and 11 so that it is located inside the opening 12a of the shielding film 12. After the contact hole 16 is filled with a high-melting-point metal such as tungsten by a CVD process, the high-melting-point metal layer formed on the third interlayer insulation film 13 and the front face of the interlayer insulation film 13 are flattened to form a mirror surface by a chemomechanical polishing (CMP) process. The residual thickness of the interlayer insulation film 13 after polishing is adjusted to be approximately 4,000 Å to 10,000 Å at the thinnest portion.

Next, an aluminum layer with a thickness of approximately 300 Å to 5,000 Å is formed by a low temperature sputtering process and a rectangular pixel electrode 14 with a side of 15 μm to 20 μm is formed by a patterning process. A connecting plug (interlayer conductive portion) 15 composed of a high-melting-point metal electrically connects the relay wiring 10 and the pixel electrode 14, skipping one metal layer of the shading layer 12. The connecting plug 15 may be formed by planarizing the third interlayer insulation film 13 by a CMP process, providing a contact hole, and embedding a high-melting-point metal such as tungsten therein. Alternatively, the opening 12a in the second metal layer 12 may be enlarged, a second relay wiring composed of a second metal layer 12 and having, for example, a rectangular shape may be formed in the opening 12a, the first relay wiring 10 and the second relay wiring may be connected to each other, and the second relay wiring may be the connected to the pixel electrode 14 by the connecting plug 15. A passivating film 17 with a thickness of approximately 500 Å to 2,000 Å composed of silicon oxide or the like is formed on the entire pixel electrode 14. An alignment film is formed on the entire passivating film 17 and subjected to rubbing treatment in the fabrication of the liquid crystal panel. In this embodiment, although the pixel electrode 14 is formed of a third conductive layer (hereinafter referred to as a third metal layer), it may be formed in the upper layer when the substrate is formed by a process for depositing a plurality of metal layers. The pixel electrode 15 is formed of the uppermost metal layer in all the cases.

A silicon oxide film is used as the passivating film 17 which covers the pixel region 20 as described above, whereas a silicon nitride film with a thickness of approximately 2,000 Å to 10,000 Å is used in the peripheral circuit region, sealing region and the scribe portion. A dielectric mirror film may be formed on the passivating film 17.

As shown in Fig. 1, the pixel region 20, which occupies most of the rectangular semiconductor device 1, is surrounded by the sealing region 127 having a frame shape. The sealing region 127 forms a border region between the pixel region 20 and a non-pixel region not containing the liquid crystal (the peripheral circuit region, the terminal pad region, and the scribe region). In this embodiment, the sealing region 127 includes parts of the peripheral circuits (the gate line driver circuits 22R and 22L, the precharging/testing circuit 23, and the image signal sampling circuit 24), and thus only the data line driver circuit 21 lies at the exterior of the sealing region 127.

Of course, the data line driver circuit 21 may also lie at the interior of the sealing region 127.

The cross-sectional configuration of the sealing region 127 in this embodiment includes, as shown in Fig. 2, a wide continuous pattern 127a composed of polycrystalline silicon or a metal silicide, which is formed on the field oxide film 3 and separated from the gate electrode 4a, a wide continuous lower dummy pattern A composed of the first metal layer, and an isolated wide-continuous upper dummy pattern B composed of the second metal layer. The pattern 127a may be formed by the process for the gate electrode 4a. The dummy patterns A and B may be formed by the process for the first and second metal layers, respectively. The surface level of the third interlayer insulation film 13 is uniformly raised by the thickness corresponding to the thicknesses of the pattern 127a and the dummy patterns A and B, and is substantially equal to the surface level of the pixel region and the peripheral circuit region.

The periphery of the data line driver circuit 21 lying at the exterior of the sealing region 127 and the peripheries of the relay terminal pads 29R and 29L and the input terminal pad 26 as shown by hatching in Figs. 4 to 6 and Fig. 9, other than the wiring region, form a dummy pattern region which is electrically floating or clamped by the power source voltage. The input terminal pad 26 in this embodiment has a structure piled with the lower layer 26a as the first metal layer and the upper layer 26b as the second metal layer, and the cross-sectional configuration of the dummy pattern region includes the wide

continuous lower dummy pattern A as the first metal layer which is formed on the first interlayer insulation film 6 on the field oxide film 3, and the wide continuous upper dummy pattern B as the second metal layer which is formed on the second interlayer insulation film 11. The dummy patterns A and B may be formed by the process for the metal layer. The surface level of the third interlayer insulation film 13 is uniformly raised by the thickness corresponding to the thicknesses of the dummy patterns A and B immediately after the formation of the film, and the level just above the input terminal pad 26 is substantially equal to the surface level of the pixel region and the peripheral circuit region by the raising effect at the neighboring regions.

As shown in Figs. 4 and 5, isolated rectangular interwiring dummy patterns M lie between a plurality of wirings L_{OUT} extending from the data line driver circuit 21 in the border region X between the lower side of the sealing region 127 and the data line driver circuit 21. The interwiring dummy patterns M are also formed by the process for the metal layers.

In the formation of the input terminal pad 26, the upper layer 26b is embedded into a large opening provided in the second interlayer insulation film 11 on the lower layer 26a, hence a large indent is formed on the upper layer 26, and the third interlayer insulation film 13 just above the upper layer 26 also inevitably has an indent. When the deposition process of the third interlayer insulation film 13 includes the formation of the SOG film, the indent on the upper layer 26 can be moderated to some extent.

Since the area of the input terminal pad 26 is significantly larger than that of the contact hole of the wiring electrode, the indent on the third interlayer insulation film 13 just above the input terminal pad 26 cannot be compensated for only by the additional formation of the SOG film.

Fig. 3 is a cross-sectional view of another configuration of the input terminal pad. In Fig. 3, after a plurality of small contact holes are formed on the lower layer 26a, a terminal pad 26' is formed by embedding the upper layer 26b'. In such a configuration, the dropping of the material for the upper layer 26b' into the contact hole is suppressed and fine indents independently form; hence the surface of the upper layer 26b' is flattened. As a result, the surface of the formed third interlayer insulation film 13 is easily flattened without reflecting the fine indents.

In this embodiment as described above, wide continuous dummy pattern regions (dummy patterns A and B) are vertically formed such that the pattern density reaches almost 100% in the entire region at the exterior of the pixel region and the peripheral circuit region, hence the surface level of the third interlayer insulation film 13 after deposition is substantially uniform over the entire substrate. The solid lines in Figs. 2 and 3 show the polished surface level of the third interlayer insulation film 13 after the CMP polishing treatment. Since the surface of the interlayer insulation film 13 before polishing is not significantly high in the regions of the input terminal pads 26 and 26', a uniform and moderate polishing rate is achieved without exposure of the input terminal pads 26 and 26'. The time for the CMP polishing, and thus the polished depth can be increased compared with the conventional depth (approximately 4,000 Å). Such an advantage of a uniform polishing rate results in a thickness reduction of the third interlayer insulation film 13 after polishing. The aspect ratio of the contact hole 16 provided on the opening 12a of the shading film 12 in the pixel region 20, and the diameter of the connecting plug 15 is reduced to reduce opening area of the opening 12a, resulting in enhanced shielding characteristics. An increased polishing depth can moderate the deep step at the opening 12a, which is formed when the third interlayer insulation film 13 is composed of only the TEOS film, in the CMP polishing process without forming the SOG film. Accordingly, the deposition process for the third interlayer insulation film 13 can be simplified, resulting in improved productivity.

As shown by hatching in the planar layout of Fig. 1, the dummy pattern region in this embodiment lies over almost the entire exterior of the sealing region 127 excluding the data line driver circuit 21, the signal wiring, the electric power source wiring, input terminal pads 26, and the relay terminal pads 29R and 29L. As shown in Figs. 4 and 5, the rectangular interwiring dummy pattern M formed between wirings L_{OUT} and the dummy patterns N_R and N_L at the right and left sides of the substrate are arranged in the interposed region X between the data line driver circuit 21 (including a shift register and a logic circuit forming sampling signals based on the output from the shift register) and the sealing region 127. The distance between a wiring L_{OUT} and the interwiring dummy pattern M is approximately 5 μm. The output wirings L_{OUT} for output of the sample signals extend from the data line driver circuit 21 (the shift register and the logic circuit) to the image signal sampling circuit 24, hence the interwiring dummy pattern has a regular shape. As shown in Fig. 6, there are two types of wirings extending from the region of the input terminal pads 26 to the interior of the substrate, that is, wirings L_{IN} for inputting signals (DXIN (data signals), power source V_{ddx} and V_{ssx}, clock signals and inverted clock signals) to the data line driver circuit 21, and wirings for inputting signals (DYIN (data signals), power source V_{ddy} and V_{ssy}, clock signals and inverted clock signals) to the gate line driver circuits 22R and 22L and the precharging/testing circuit 23. Hence the wirings L extracted from the input terminal pads 26 towards the column direction (vertical direction in the drawing) are divided into the wirings L_{IN} directed to the data line driver circuit 21 and the other wirings in the wiring region in the line direction (transverse direction in the drawing). Thus, the input terminal pads 26, a plurality of isolated rectangular divisional dummy patterns S_1 to S_3 formed between the input wirings, and isolated rectangular interwiring dummy pat-

terns T, formed between the wirings L_{IN} for input to the data line driver circuit 21, lie in the interposed region Y between the region of the input terminal pads 26 and the data line driver circuit 21. In Fig. 6, the number of the shown input terminal pads 26 is reduced.

The planar shape of each input terminal pad 26 includes a rectangular conductive contact portion 261 as a main portion and a wiring extracting portion 262 with a small width extending from the right or left side of the conductive contact portion 261 to the interior of the substrate (in the column direction). The wiring extracting portion 262 of each input terminal pad 26 lying at the right side of the centerline of the substrate is located at the left side of the conductive contact portion 261, whereas the wiring extracting portion 262 of each input terminal pad 26 lying at the left side of the centerline of the substrate is located at the right side of the conductive contact portion 261. The isolated rectangular divisional dummy patterns S_2 in the transverse direction are arranged between the wiring extracting portions 262. Further, isolated rectangular divisional dummy patterns S_3 are formed between the ends of the wiring extracting portions 262 with wirings L extracted from the wiring extracting portions 262. Also, isolated rectangular divisional dummy patterns S_1 are formed beside the edges of the input terminal pads 26 at the side of the substrate.

The dummy patterns N_R and N_L at the right and left sides of the substrate extend to the position of the input terminal pads 26, and isolated divisional dummy patterns S_2' are formed in the spaces beside the wiring extracting portions 262 of the rightmost and leftmost input terminal pads 26. The tips of the dummy patterns N_R and N_L have the same level as the tips of the input terminal pads 26, and isolated divisional dummy patterns S_0 are provided beside the tips of the dummy patterns N_R and N_L at the corners of the substrate. The planar shapes of these divisional dummy patterns are not limited to rectangular shapes (including square shapes), and a variety of shapes (triangular, polygonal, and curved) can be selected. For example, hexagonal divisional dummy patterns may be arranged to form a honeycomb shape.

These input terminal pads 26 are connected to a flexible tape wiring 39 with an anisotropic conductive film (ACF) 38 therebetween by thermocompression bonding as shown in Fig. 18. The broken lines in Fig. 6 represent the edge of the region occupied by the anisotropic conductive film 38. The flexible tape wiring 39 includes, as shown in Figs. 7 and 8, an insulating flexible tape 39a and a plurality of stripe lead wires 39b bonded thereon. The anisotropic conductive film 38 is interposed between the edge of the flexible tape 39a and the array of the input terminal pads 26.

The anisotropic conductive film 38 is composed of conductive particles 38a with a particle size of approximately 5 μm to 10 μm and an insulating adhesive resin 38b. The flexible tape 39a is compressed so that the thickness is reduced to approximately 2 μm to 10 μm. Since each terminal pad 26 and the corresponding lead wire 39b of the flexible tape wiring 39 are conduct-connected with compressed conductive particles 38a which are discretely distributed, the anisotropic conductive film 38 has conductivity only in the vertical direction. Also in Figs. 7 and 8, the number of the shown input terminal pads 26 is reduced.

By depositing dummy pattern regions (dummy patterns A and B) on the periphery of the input terminal pads 26, the surface level of the third interlayer insulation film 13 formed on the input terminal pads 26 is not raised alone but substantially equal to that of the pixel region 20; hence the initial polishing rate is reduced in the region of the input terminal pads 26 in the polishing process, the input terminal pads 26 are prevented from polishing, and thinning of the third interlayer insulation film 13 can be achieved. If a dummy pattern region is continuously formed around the input terminal pads 26, short-circuiting between input terminal pads 26 will occur through the conductive particles 38a and the dummy pattern after thermocompression bonding of the anisotropic conductive film 38.

In contrast, in this embodiment, no dummy pattern is provided between the input terminal pads 26, hence a non-dummy pattern E is provided, and the input terminal pads 26 are surrounded by divisional dummy patters S_1 to S_2 to prevent short-circuiting between the input terminal pads 26. The distances between the input terminal pads 26 and the divisional dummy patterns S_0 to S_2 and between the individual divisional dummy patterns S_0 to S_2 are wider than the distance (approximately 5 μm) between the wiring L and the dummy pattern S_3 in order to prevent short-circuiting through the anisotropic conductive film 38.

In order to further suppress the prominence of the third interlayer insulation film 13 in the region of the input terminal pads 26 immediately after the film deposition, a dummy pattern may be formed between the input terminal pads 26, and the dummy pattern between the input terminal pads 26 is also divided into divisional dummy patterns to prevent short-circuiting between the input terminal pads 26. As the number of the divisional dummy patterns increases, the possibility of short-circuiting decreases; however, as the number increases, the surface prominence of the third interlayer insulation film 13 in the dummy pattern region is significant immediately after the film deposition.

Accordingly, a moderate number is preferably selected. The planar shapes of these divisional dummy patterns are not limited to rectangular shapes (including square shapes), and a variety of shapes (triangular, polygonal, and curved) can be selected. For example, hexagonal divisional dummy patterns may be arranged to form a honeycomb shape.

Fig. 9 is a partial plan view of the periphery of the relay terminal pad 29R. The relay terminal pad 29R (29L) is a rectangular pad connected to the wiring L (for supplying a standard voltage for reversion of the polarity

of the input voltage for alternate current drive of the liquid crystal) from the outermost terminal pad 26 beside the data line driver circuit 21, and is connected to the counter electrode 33 of the glass substrate 35 with a silver paste. The relay terminal pad 29R (29L) is surrounded by the dummy patterns N_R and N_L. As a result, the surface level of the third interlayer insulation film 13 is uniform immediately after the film deposition as in the terminal pads 26.

In this embodiment, the distance between the relay terminal pad 29R and the dummy pattern N_R is set to, for example, 70 μ in order to prevent short-circuiting even when the applied silver paste slightly protrudes. That is, the distance between the relay terminal pad 29R and the dummy pattern N_R is wider than that between the wiring and the nearest dummy pattern. The dummy pattern surrounding the relay terminal pad 29R may be a divisional dummy pattern.

Fig. 10 is a contour plot of film illustrating the thickness distribution of the third interlayer insulation film 13 after polishing of the liquid crystal panel substrate 131 in accordance with Embodiment 1, in which the third interlayer insulation film 13 with a thickness of approximately 24,000 Å is formed and then subjected to the CMP treatment until the residual thickness of the third interlayer insulation film 13 reaches approximately 12,000 Å in the center of the pixel region 20. In Fig. 24, a graph depicted by marks Δ shows the residual thickness distribution of the left seal in the vertical direction taken along line a-a' of Fig. 10. In Fig. 25, a graph depicted by marks Δ shows the residual thickness distribution of the central pixel in the vertical direction taken along line b-b' of Fig. 10. In Fig. 26, a graph depicted by marks Δ shows the residual thickness distribution of the upper seal in the transverse direction taken along line c-c' of Fig. 10. In Fig. 27, a graph depicted by marks Δ shows the residual thickness distribution of the central pixel in the transverse direction taken along line d-d' of Fig10. In Fig. 28, a graph depicted by marks Δ shows the residual thickness distribution of the lower sealing region in the transverse direction taken along line e-e' of Fig. 10.

These graphs demonstrate that the maximum difference in the thickness between the pixel region 20 and the sealing region 127 is 2,720 Å, and the distance between the contour lines (corresponding to a difference of 1,000 Å in the thickness) is considerably larger than that in Fig. 23. The flatness of the pixel region 20 is improved by a factor of two or more.

The maximum difference in the thickness is reduced to approximately 2,910 Å over the entire substrate (chip). The slope of the indented central portion of the top side of the sealing region 127 is reduced to approximately one-half or less, and the slope of the indented central portion of the bottom side of the sealing region 127 is reduced to approximately one quarter or less. The right and left sides of the sealing region 127 have minimum thicknesses at the top corners, hence the central protrusion is prevented, and the slope is reduced to one quarter or less. Wide continuous dummy pattern regions (dummy patterns A and B) cause such significant improvement in almost the entire exterior of the pixel region 20 and the peripheral circuit region.

It is preferable that the maximum difference in the thickness be reduced to 1,000 Å or less in the pixel region 20. In the thickness distribution of the pixel region 20, the vertical line in the pixel center corresponds to the trough line of the thickness, and the central region of the input terminal pads 26 corresponds to the maximum thickness (approximately 14,500Å). This suggests insufficient polishing in the region of the input terminal pads 26 in contrast to the conventional one in Fig. 23.

[Embodiment 2]

Fig. 11 is a partial plan view of the four-corner portion of the sealing region in a reflective liquid crystal panel substrate in accordance with Embodiment 2 of the present invention. Fig. 12 is a cross-sectional view taken along the line C-C' in Fig. 11. In Fig. 11, regions with dotted patterns represent the first metal layer and regions with hatching represent the second metal layer, whereas the third metal layer is not shown. The configurations other than that described below are the same as those of the reflective liquid crystal panel substrate in accordance with Embodiment 1.

The reflective liquid crystal panel substrate 231 has substantially the same configuration as that of the reflective liquid crystal panel substrate 131 in accordance with Embodiment 1. The pixel region 20 is surrounded by the sealing region 127 of isolated wide continuous dummy pattern regions (the dummy pattern A of the first metal layer and the dummy pattern B of the second metal layer). The input terminal pads 26, the relay terminal pads 29R and 29L and the data line driver circuit 21 are also surrounded by wide continuous dummy pattern regions (the dummy pattern A of the first metal layer and the dummy pattern B of the second metal layer). Differing from the wide continuous dummy patterns, such as the dummy patterns A lying between the wirings L_{OUT} at the sealing side in Embodiment 1, in a rectangular region at the four-corner sealing portion 127C of the sealing region 127, the dummy pattern of the first metal layer forms a group including a plurality of independent divisional patterns. In detail, a plurality of rectangular divisional patterns a each having a different area are separately arranged in the vertical and transverse directions, and have a pattern density of 50% or less. The divisional patterns a have different areas from each other which are smaller than that of the input terminal pads 26. The dummy pattern B' of the second metal layer at the four-corner sealing portion 127C has a rectangular wide continuous surface. As a result, as shown by the dotted line in Fig. 12 the unpolished surface of the third interlayer insulation film 13 at the four-corner sealing portion 127C has roughness which reflects the uneven-

ness of the divisional dummy patterns a.

In CMP treatment of the surface of the third interlayer insulation film 13 on the substrate provided with divisional dummy patterns a with a low density distribution at the four-corner sealing portion 127C, the four-corner sealing portion 127C has a higher initial polishing rate than that at the gentle bump side of the sealing region 127. Hence the polishing rate of the sealing region 127 surrounded by four units at the four-corner sealing portion 127c are equalized to that of the interior region during polishing, and the difference in the residual thickness between the pixel region 20 and the sealing region 127 is suppressed. In particular, it is important to impart in advance roughness to the right and left corners of the bottom side of the sealing region 127 among the corner portion 127a of the four units.

When the divisional dummy patterns a have substantially the same area and are distributed uniformly or randomly at the four-corner sealing portion 127C, a decreased pattern density (a decreased ratio of the total dummy pattern area per unit area) causes larger distances between the dummy patterns a and thus the dummy patterns a have a small distribution density. As a result, the initial polishing rate of the third interlayer insulation film 13 is higher than that of the periphery of the four-corner sealing portion 127C, a slanted surface is first formed at the periphery of the four-corner sealing portion 127C, and the slanted surface gradually spreads towards the inside during polishing. When the pattern density is the same, when the number of the divisional dummy patterns a is reduced and when the area of the divisional dummy patterns a is increased, these are prominent and have larger initial polishing rates. The boundary of the four-corner sealing portion 127C rapidly forms a slanted surface, and the slanted surface gradually spreads towards the inside during polishing as in the above case. Since a dummy pattern distribution for causing the initial polishing rate or the four-corner sealing portions 127C to increase compared with its periphery is provided in this embodiment, the residual thickness is affected by the residual thickness of the four-corner sealing portion 127C as a standard thickness, and thus can be easily equalized at the periphery of the sealing region 127 surrounded by the four-corner sealing portion 127C of the four units and the pixel region 20. Accordingly, the sealing region 127 and the pixel region 20 are flattened or planarized.

As shown in Fig. 11, in the four-corner sealing portion 127C, a plurality of rectangular divisional dummy patterns a are arranged in the vertical direction at the right and left sides of the sealing region, and a plurality of rectangular divisional dummy patterns a are arranged in the transverse direction at the top and bottom sides of the sealing region. It is considered that each vertical rectangular divisional dummy pattern a having the highest initial polishing rate at the longitudinal (vertical) sides contributes to the planarization of the vertical direction of the sealing region, whereas each transverse rectangular divisional dummy pattern a having the highest initial polishing rate at the longitudinal (transverse) sides contributes to the planarization of the transverse direction of the sealing region. In this embodiment, the vertical rectangular divisional dummy patterns a are not arranged near the top and bottom sides of the sealing portion and the transverse rectangular divisional dummy patterns a are not arranged near the right and left sides of the sealing portion. Instead, the vertical rectangular divisional dummy patterns a are arranged near the right and left sides of the sealing portion, and the transverse rectangular divisional dummy patterns a are arranged near the top and bottom sides of the sealing portion. As a result, a high initial polishing rate at the four-corner sealing portion 127C is achieved by the high initial polishing rates of these dummy patterns in the vertical and transverse directions.

Modification of the shapes, array and pattern density of the divisional dummy patterns a will further improve planarization of the sealing region 127 and the inner region.

When the four-corner sealing portion 127C has no dummy pattern (a pattern density of zero), the boundary is easily polished to form a slanted surface at the initial stage of the polishing, since the corner is indented from its periphery and the boundary portion protrudes. The slanted surface gradually spreads towards the inner region. As a result, the pixel region 20 and the sealing region are totally flattened or planarized.

Fig. 13 is a contour plot of film illustrating the thickness distribution of the third interlayer insulation film 13 after polishing of the liquid crystal panel substrate 231 in accordance with Embodiment 2, in which the third interlayer insulation film 13 with a thickness of approximately 24,000 Å is formed and then subjected to the CMP treatment until the residual thickness of the third interlayer insulation film 13 reaches approximately 12,000 Å in the center of the pixel region 20. In Fig. 24, a graph depicted by marks □ shows the residual thickness distribution of the left seal in the vertical direction taken along line a-a' of Fig. 13. In Fig. 25, a graph depicted by marks □ shows the residual thickness distribution of the central pixel in the vertical direction taken along line b-b' of Fig. 13. In Fig. 26, a graph depicted by marks □ shows the residual thickness distribution of the upper seal in the transverse direction taken along line c-c' of Fig. 13. In Fig. 27, a graph depicted by marks □ shows the residual thickness distribution of the central pixel in the transverse direction taken along line d-d' of Fig. 13. In Fig. 28, a graph depicted by marks □ shows the residual thickness distribution of the lower sealing region in the transverse direction taken along line e-e' of Fig. 13.

These graphs demonstrate that the maximum difference in thickness between the pixel region 20 and the sealing region 127 is 1,380 Å, and the distance between the contour lines (corresponding to a difference of 1,000 Å in thickness) is larger than that in Fig. 10. The flatness

of the pixel region 20 is improved by a factor of two or more compared with Embodiment 1. The maximum difference in the thickness is approximately 2,500 Å over the entire substrate (chip), since the region of the input terminal pads 26 including wide continuous dummy patterns is insufficiently polished and still has large thickness. The slope of the indented central portion of the top side of the sealing region 127 is reduced to approximately one-half or less compared with that in Embodiment 1. The right and left sides of the sealing region 127 are substantially flattened because dummy patterns with a low pattern density at the bottom right and left corners of the sealing region 127 prompt polishing.

As shown in Fig. 13, however, the sealing region still has a large thickness on the periphery of the bottom right and left corners, hence the maximum difference in the thickness in the pixel region 20 and the sealing region 127 is not smaller than 100 Å. When the four-corner sealing portion 127C has no dummy pattern a (a pattern density of zero), the inner pixel region 20 is further flattened or planarized, but the boundary of the four-corner sealing portion 127C could have a steep slope. Dummy patterns a may be formed such that the pattern density decreases from the bottom right and left corners 127C to the upper positions of the right and left sides, or to the central portion of the bottom side. In such a case, the pixel region 20 and the sealing region 127 can be further flattened or planarized.

[Embodiment 3]

Fig. 14 is a partial plan view of the four-corner portion of the sealing region in a reflective liquid crystal panel substrate in accordance with Embodiment 3 of the present invention. Fig. 15 is a cross-sectional view taken along the line C-C' in Fig. 14. In Fig. 14, regions with dotted patterns represent the first metal layer and regions with hatching represent the second metal layer, whereas the third metal layer is not shown. The configurations other than that described below are the same as those of the reflective liquid crystal panel substrate in accordance with Embodiment 1.

The reflective liquid crystal panel substrate 331 in this embodiment has uneven pseudo pixel patterns P as a matrix of dummy patterns (two-dimensionally repeated pattern) lying over the sealing region 227 surrounding the pixel region 20 and its outer region. The uneven pseudo pixel patterns P vertically and horizontally extend to the peripheries of the data line driver circuit 21, the relay terminal pads 29R and 29L, and the input terminal pads 26. Each uneven pseudo pixel pattern P produces a uneven pattern, which resembles the pixel pattern and has a volume similar to that of each pixel in the pixel region 20, on the third interlayer insulation film 13.

In this embodiment, each uneven pseudo pixel pattern includes pseudo gate lines 4_p of the first metal layer having substantially the same width as that of the gate lines 4 lying on the bottommost layer of the pixel; data lines 7 of the first metal layer of the pixel; pseudo data lines 7_p of the first metal layer having substantially the same width as that of the source electrode wirings 7a and the relay wirings 10; pseudo source electrode wirings $7a_p$; pseudo relay wiring 10_p; and wide pseudo shading films 12_p of the second metal layer imitating the shading film 12 of the second metal layer in the pixel portion. The pattern density of the bottom layer wirings and the first metal layer is approximately 25% in each pixel, hence the pattern density of the uneven pseudo pixel patterns P composed of the first metal and second metal layers is set to substantially the same value.

At the periphery of the upper and lower sealing regions (sides) 227 and the boundary region X', the signal wiring L_{OUT} of the first metal layer from the data line driver circuit 21 to the pixel signal sampling circuit 24 is used as the pseudo data line 7_p. The pseudo gate line 4_p' of the first metal layer and the pseudo source electrode wiring $7a_p$' are not connected to the pseudo data line 7_p.

The uneven pseudo pixel patterns P are vertically and horizontally repeated on the substrate, but the matrix of the uneven pseudo pixel patterns P is slightly different from the matrix of the pixel region 20 in this embodiment. The matrices of the uneven pseudo pixel patterns P and the pixel region 20 can be unified by changing the layout of the devices in the peripheral circuit region, such as the data line driver circuit 21, pixel signal sampling circuit 24, and the gate line driver circuits 22R and 22L, and the layout of the signal wirings L_{OUT}.

On the substrate 331 provided with the uneven pseudo pixel patterns P, uneven surface patterns like the uneven pixel patterns are periodically arranged over the surface of a region of the third interlayer insulation film 13 before CMP treatment other than the pixel region 20. Accordingly, the polishing rate is made uniform over the entire substrate 331 from the initial polishing stage and at least the pixel region 20 and the sealing region 227 can be flattened or planarized with high accuracy.

Fig. 16 is a contour plot of film illustrating the thickness distribution of the third interlayer insulation film 13 after polishing of the liquid crystal panel substrate 331 in accordance with Embodiment 3, in which the third interlayer insulation film 13 with a thickness of approximately 24,000 Å is formed and then subjected to the CMP treatment until the residual thickness of the third interlayer insulation film 13 reaches approximately 12,000 Å in the center of the pixel region 20. In Fig. 24, a graph depicted by marks O shows the residual thickness distribution of the left seal in the vertical direction taken along line a-a' of Fig. 16. In Fig. 25, a graph depicted by marks O shows the residual thickness distribution of the central pixel in the vertical direction taken along line b-b' of Fig. 16. In Fig. 26, a graph depicted by marks O shows the residual thickness distribution of the upper seal in the transverse direction taken along line c-c' of Fig. 16. In Fig. 27, a graph depicted by marks O shows the residual thickness distribution of the central

pixel in the transverse direction taken along line d-d' of Fig. 16. In Fig. 28, a graph depicted by marks O shows the residual thickness distribution of the lower sealing region in the transverse direction taken along line e-e' of Fig. 16.

These graphs demonstrate that the maximum difference in the thickness between the pixel region 20 and the sealing region 127 (including the four-corner sealing portion 227C) is approximately 850 Å, and the maximum difference in the thickness over the entire substrate is approximately 950 Å. The pixel region 20 and the sealing region 227 are satisfactorily flattened. Although the peripheral region of the input terminal pads 26 shows slightly insufficient polishing, the region will be further flattened by reducing the pattern density of the uneven pseudo pixel patterns P.

The elements forming the uneven surface pattern on the pixel region include the two openings provided in the field oxide film, the gate lines 4 of the bottom layer, the data lines 7 of the first metal layer, the source electrode wirings 7a, the relay electrodes 10, the shading film 12 of the second metal layer, and the plug hole 12a. In this embodiment, although the pseudo gate line 4_p of the first metal layer imitates the gate line 4 of the bottom layer, the pseudo gate line 4_p may be formed of the bottom wiring layer. Further, each segment of the uneven pseudo pixel pattern P may include pseudo openings imitating the two openings provided in the field oxide film 3 and a pseudo plug hole imitating the plug hole 12a. Uneven pseudo pixel patterns significantly resembling the pixel pattern can be formed on the periphery of the pixel region 20 by the same process without additional steps, and the pixel region 20 and the sealing region 227 can be further flattened.

At the initial stage in the CMP treatment, a dense protruded portion of the surface is polished with difficulty, while a sparsely protruded portion is polished with ease, since isolated protrusions are rapidly polished. When there are two regions, that is, a dense region in which dense protrusions are distributed at random, and a sparse region in which sparse protrusions are distributed at random, both protrusions having substantially the same size, the sparse region has a higher initial polishing rate, hence a slanted surface will be formed over these regions after polishing. The sparse region has a low pattern density as a result. On the other hand, the protrusion (islands) with a small surface area has a higher initial polishing rate, whenever the surface to be polished has a uniform pattern density, because the perimeter of the island is long relative to the area of the island. A region in which protrusions with a large area are densely distributed at random is polished with most difficulty at the initial polishing stage. A representative example is a wide continuous pattern covering the entire range. In contrast, a region in which protrusions with small areas are sparsely distributed at random can be easily polished at the initial polishing stage. A representative example is a region having no protrusions (no dummy pattern). It is presumed that a region in which protrusions with large areas are sparsely distributed at random and a region in which protrusions with small areas are densely distributed at random have mediate polishing rates between the maximum rate and the minimum rate at the initial polishing stage; however, it is not known which has a higher initial polishing rate because the polishing rate depends on the polishing solution and other parameters including the regularity of distribution, and the shape, arrangement, and position of the protrusions. The polishing solution probably has a regular flow distribution due to a regular bump distribution in the pixel region 20 during the CMP treatment; hence a means for achieving the similar flow distribution is required for the non-pixel regions.

Within the chip size of the reflective liquid crystal panel substrate, since the input terminal pads 26 are considered to be the largest protrusions and to be sparsely distributed in view of its one-dimensional array extension, the region including the input terminal pads 26 has the maximum polishing rate. The pixel region 20, however, has spatial periodicity in configuration of a matrix of uneven pixel patterns. As a result, the pixel region 20 has a hierarchic regularity including two different levels of regularity, that is, higher-order regularity of spatial periodicity in the uneven pixel patterns and lower-order regularity within a uneven pixel pattern. The uneven pixel pattern has a hierarchic structure comprising a distribution of various basic (primary), microscopic uneven sections represented by fine lines with a width of 1,000 Å to 10,000 Å (two openings in the field oxide film 3, the gate line 4 of the bottom wiring layer, the data line 7 of the first metal layer, the source electrode wiring 7a, the relay electrode wiring 10, and the shading film 12 and plug hole 12a of the second metal layer) and condensed uneven portions (second uneven portions) caused by the irregularity of the basic uneven portions in the pixel. The uneven pseudo pixel pattern P in this embodiment imitates a macroscopic condensed uneven portion including only the pseudo gate line 4_p, the pseudo data line 7_p, the pseudo source electrode $7a_p$, and the pseudo relay wiring 10_p, instead of the basic uneven portion. The condensed uneven portion in this embodiment is considered to be an overlap portion of the gate line 4 and the data line 7 and an overlap portion of the capacitor electrode 9a and the relay wiring 10. Accordingly, the uneven pseudo pixel pattern P preferably includes the pseudo gate line 4_p, the pseudo data line 7_p and the pseudo relay wiring 10_p. A typical uneven portion may be used as an element of uneven pseudo pixel pattern P. It is not necessary that the position of a typical uneven portion in the uneven pseudo pixel pattern P exactly corresponds to the position of a typical uneven portion in the actual pixel.

Supposing that the uneven pixel pattern has a third or more hierarchic configuration, it is necessary that the basic uneven portion is exactly replicated and thus imitation of the second or third order uneven portion is suf-

ficiently useful. When the hierarchic configuration in the uneven pixel pattern is not clarified, an uneven pseudo pixel pattern P being the exact replica of the basic uneven portion has an advantage, that is, a simplified mask design. For high accuracy planarization with a maximum difference in the thickness of less than 1,000 Å, it is preferable that the uneven pseudo pixel pattern P be the exact replica of the basic uneven portion.

The liquid crystal panel substrate in this embodiment is suitable for use in reflective liquid crystal panel, and is also applicable to light valves for liquid crystal projectors; portable information processing machines including wrist watch-type electronic devices, word processors, and personal computers; and displays for portable telephones and other electronic devices.

In the liquid crystal panel substrate in this embodiment, switching elements are fabricated on the main surface of a semiconductor substrate. Insulating substrates, such as glass substrates and quartz substrates, can also be used instead of semiconductor substrates. The present invention is also applicable to formation of thin film transistors (TFTs) on an insulating substrate as a switching device.

Further the present invention is applicable to flat display panel substrates other than liquid crystal panel substrates.

As described above, in the present invention no dummy pattern is formed in the unused space of the pixel region, and a dummy pattern for raising the level of the upper interlayer insulation film, which is subjected to polishing, is formed by using the conductive layer preformed in the entire non-pixel region. If a dummy pattern is formed in the pixel region, additional deposition steps for depositing a medial conductive layer and an interlayer insulation film are required for raising the level. When the surface bump of the interlayer insulation film before polishing is suppressed, the initial polishing rate undesirably decreases, mirror planarization of the interlayer insulation film requires a long polishing time and a large amount of polishing solution. The present invention can solve such problems and has the following advantages.

(1) When a dummy pattern of a single or plural layers is provided near the terminal pad, the surface level of the upper interlayer insulation film near the terminal pad is substantially equal to the surface level in the pixel region. Since the surface level is smoothed as a whole, a uniform polishing rate is achieved over the entire surface. Accordingly the present invention improves excessive polishing at the terminal pad portion, which has not been solved in conventional formed surfaces with nonuniform surface levels, and thus the underlying layer at the terminal pad portion is not exposed by polishing. Such an advantage is useful for mirror planarization of the surface in the pixel region, and thinning of the interlayer insulation film before polishing will be achieved. The thinning improves the aspect ratio of the contact hole of the conductive interlayer in the pixel region and thus can form an opening having a smaller diameter accompanied by the contact hole having a smaller diameter. The shading effect is therefore improved, resulting in an improvement in switching elements. Of course, no additional film deposition step is required.

When a conductive dummy pattern lies near the terminal pads outside the pixel region, the dummy pattern functions as a shading film, hence it prevents the invasion of stray light from the exterior of the pixel region into the pixel region on the substrate, resulting in a suppressed photocurrent flow and an improved switching element.

(2) When a dummy pattern arranged near the input terminal pads is divided into a plurality of divisional dummy patterns, a uniform surface level of the interlayer insulation film immediately after deposition is achieved and short-circuiting between the two adjacent input terminal pads can be prevented.

(3) When a non-dummy pattern region is provided between two adjacent input terminal pads, short-circuiting between the two adjacent input terminal pads can be securely prevented.

(4) When the distance between an input terminal pad and a divisional dummy pattern provided near the input terminal pad is larger than the distance between a wiring and a dummy pattern near the wiring, bridging by conductive particles in an anisotropic conductive film between the input terminal pad and the divisional dummy pattern will barely occur and thus short-circuiting can be more effectively prevented.

(5) When the distance between a relay terminal pad and a divisional dummy pattern provided near the relay terminal pad is larger than the distance between a wiring and a dummy pattern near the wiring, silver paste on the relay terminal pad will not cause short-circuiting to the dummy pattern near the relay terminal pad even if the silver paste slightly spreads, although conduction is intended to occur generally by the silver paste on the relay terminal pad.

(6) When dummy patterns are provided on the sealing region surrounding the pixel region including that near the terminal pad, the surface level of the interlayer insulation film before polishing in this region is substantially equal to the surface level of the pixel region. The pixel region and its peripheral region are polished at a uniform polishing rate in the planarization process. Thus, the pixel region is more satisfactorily flattened or planarized compared with conventional configurations, resulting in

improved reflectance and easy determination of the etching time of the contact hole after polishing.

(7) A dummy pattern, provided at the peripheral portion of the sealing region, has the same surface level as that of the interlayer insulation film lying on the sealing region. The surface of the interlayer insulation film in the sealing region has therefore no slope after polishing, and adhesiveness of the sealing material is improved.

(8) When a dummy pattern in the sealing region is formed on isolated patterns lying on the same layer as the control wiring layer of the switching element, the surface of the interlayer insulation film can be more accurately flattened or planarized by polishing.

(9) When a dummy pattern is formed on a region near the driver circuit which is provided at the periphery of the pixel region and which supplies signals to the switching element, the dummy pattern helps planarization of the interlayer insulation film by polishing.

(10) In one arrangement a dummy pattern is formed at the corner portion of the sealing region surrounding the pixel region and has a lower density than those in the side portion of the sealing region and the peripheral region of the corner portion. As a result, the surface of the unpolished interlayer insulation film has roughness, which reflects a plurality of uneven discrete dummy patterns, at the four-corner sealing portion. Since the four-corner sealing portion has a larger initial polishing rate compared with the gentle bump side in the sealing region in polishing process, the polishing rate is substantially equalized in the inner-sealing region surrounded by the four-corner sealing portion. Accordingly, a variation in residual thickness is suppressed in the pixel region and the sealing region.

(11) Even when the four-corner sealing portion has no dummy pattern (a pattern density of zero), the boundary portion having a higher level than the corner region forms a slanted surface at an initial polishing stage, and the slanted surface spreads towards the inner position.

Consequently, the pixel region and the sealing region can be flattened or planarized as a whole.

(12) In one arrangement a plurality of uneven pseudo pixel patterns imitating the uneven pixels can be formed instead of a wide continuous flat dummy pattern in the non-pixel region. Since the regions other than the pixel region have substantially the same uneven pattern as that of the pixel region, the substrate has a uniform polishing rate from the initial stage, and the surfaces of the pixel region and the sealing region can be flattened or planarized with high accuracy.

(13) When a plurality of uneven pseudo pixel patterns are arranged in the two-dimensional directions on the non-pixel region, the non-pixel region has spatial regularity corresponding to the matrix in the pixel region and thus the flatness over the pixel region and the sealing region is further improved.

(14) When each pseudo pixel pattern includes at least a pseudo gate line and a pseudo data line, the pseudo pixel pattern is very similar to the uneven regularity in the typical uneven pixel portion and the pixel region, and the interlayer insulation film can be flattened or planarized with high accuracy in the pixel region and the sealing region.

Claims

1. An electro-optical device substrate comprising a layered film structure of a plurality of interlayer insulation films and a plurality of conductive layers alternately formed in a pixel region, in which a switching element is arranged on the substrate in response to each pixel, at least one interlayer insulation film below the top conductive layer among said plurality of conductive layers being flattened or planarized by polishing;

   said substrate being characterized in that a dummy pattern with a single or a plurality of layers comprising said conductive layer below said interlayer insulation film subjected to said polishing is provided near at least a terminal pad formed at a non-pixel region on said substrate.

2. The electro-optical device substrate according to claim 1, wherein said terminal pad is an input terminal pad arranged near the edge of the substrate, and said dummy pattern arranged on the periphery of said input terminal pad comprises a plurality of divisional dummy patterns which are divided in the plane of the substrate.

3. The electro-optical device substrate according to claim 2, wherein a non-dummy pattern region is provided between two adjacent input terminal pads.

4. The electro-optical device substrate according to claim 3, wherein the distance between said input terminal pad and said divisional dummy patterns arranged around said input terminal pad is larger than the distance between a wiring and said dummy pattern near the wiring.

5. The electro-optical device substrate according to

claim 1, wherein said terminal pad is a relay terminal pad arranged at the interior of the substrate, and the distance between said relay terminal pad and said dummy pattern arranged around said relay terminal pad is larger than the distance between a wiring and said dummy pattern near the wiring.

6. An electro-optical device substrate comprising a layered film structure of a plurality of interlayer insulation films and a plurality of conductive layers alternately formed in a pixel region, in which a switching element is arranged on the substrate in response to each pixel, at least one interlayer insulation film below the top conductive layer among said plurality of conductive layers being flattened or planarized by polishing;

said substrate being characterized in that a dummy pattern with a single or a plurality of layers comprising said conductive layer below said interlayer insulation film subjected to said polishing is provided in a sealing region formed on the periphery of said pixel region.

7. An electro-optical device substrate comprising a layered film structure of a plurality of interlayer insulation films and a plurality of conductive layers alternately formed in a pixel region, in which a switching element is arranged on the substrate in response to each pixel, at least one interlayer insulation film below the top conductive layer among said plurality of conductive layers being flattened or planarized by polishing;

said substrate being characterized in that a dummy pattern with a single or a plurality of layers comprising said conductive layer below said interlayer insulation film subjected to said polishing is provided in a peripheral region outside a sealing region formed on the periphery of said pixel region.

8. The electro-optical device substrate according to either claim 6 or 7, wherein said dummy pattern is formed on an isolated pattern formed in the same layer as a control wiring layer of said switching element.

9. An electro-optical device substrate comprising a layered film structure of a plurality of interlayer insulation films and a plurality of conductive layers alternately formed in a pixel region, in which a switching element is arranged on the substrate in response to each pixel, at least one interlayer insulation film below the top conductive layer among said plurality of conductive layers being flattened or planarized by polishing;

said substrate being characterized in that a dummy pattern with a single or a plurality of layers comprising said conductive layer below said interlayer insulation film subjected to said polishing is provided in a peripheral region of a driver circuit arranged on the periphery of said pixel region and supplying signals to said switching element.

10. An electro-optical device substrate comprising a layered film structure of a plurality of interlayer insulation films and a plurality of conductive layers alternately formed in a pixel region, in which a switching element is arranged on the substrate in response to each pixel, at least one interlayer insulation film below the top conductive layer among said plurality of conductive layers being flattened or planarized by polishing;

said substrate being characterized in that a dummy pattern with a single or a plurality of layers patterns comprising said conductive layer below said interlayer insulation film subjected to said polishing is provided in a corner region of a sealing region formed on the periphery of said pixel region, said dummy pattern having a lower density of distribution than the peripheral region of a side region of said sealing region or of said corner region.

11. An electro-optical device substrate comprising a layered film structure of a plurality of interlayer insulation films and a plurality of conductive layers alternately formed in a pixel region, in which a switching element is arranged on the substrate in response to each pixel, at least one interlayer insulation film below the top conductive layer among said plurality of conductive layers being flattened or planarized by polishing;

said substrate being characterized in that a dummy pattern with a single or a plurality of layers comprising said conductive layer below said interlayer insulation film subjected to said polishing is provided in a sealing region, excluding the corner region, formed on the periphery of said pixel region.

12. An electro-optical device substrate comprising a layered film structure of a plurality of interlayer insulation films and a plurality of conductive layers alternately formed in a pixel region, in which a switching element is arranged on the substrate in response to each pixel, at least one interlayer insulation film below the top conductive layer among said plurality of conductive layers being flattened or planarized by polishing;

said substrate being characterized in that a plurality of uneven pseudo pixel patterns including said conductive layer below said interlayer insulation film subjected to said polishing treatment are provided in a non-pixel region on said substrate.

13. The electro-optical device substrate according to claim 12, wherein said uneven pseudo pixel patterns are formed by being repeatedly formed in the two-dimensional directions on the substrate.

14. The electro-optical device substrate according to either claim 12 or 13, wherein a first conductive layer among said conductive layers electrically connected to said switching element is electrically connected to an upper conductive layer formed on the interlayer insulation film subjected to said polishing, a second conductive layer is provided between said first conductive layer and said upper conductive layer; and

said uneven pseudo pixel pattern comprises either a first dummy pattern comprising said first conductive layer or a second dummy pattern comprising said second conductive layer or comprises a pile of said first dummy pattern and the second dummy pattern.

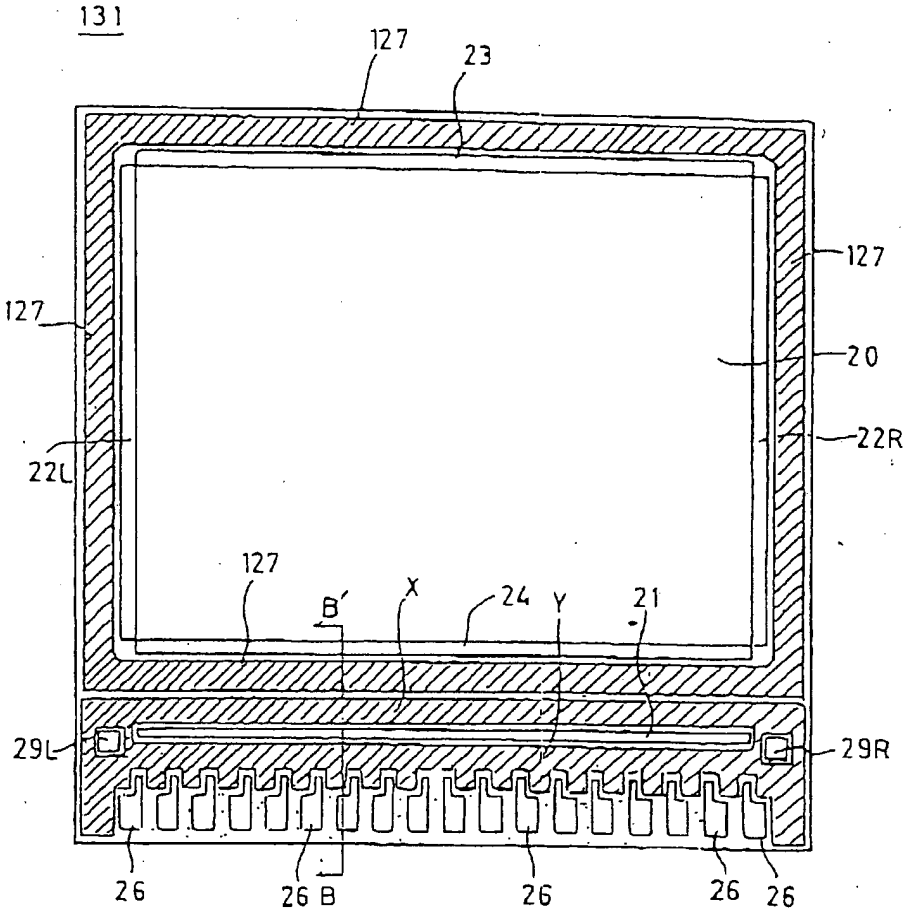
15. The electro-optical device substrate according to claim 12, wherein said uneven pseudo pixel pattern comprises at least a pseudo gate line and a pseudo data line.

16. The electro-optical device comprising an electro-optical device substrate described any one of claims 1 to 15, wherein an electro-optical material interposed between said substrate and a transparent substrate opposed to said substrate.

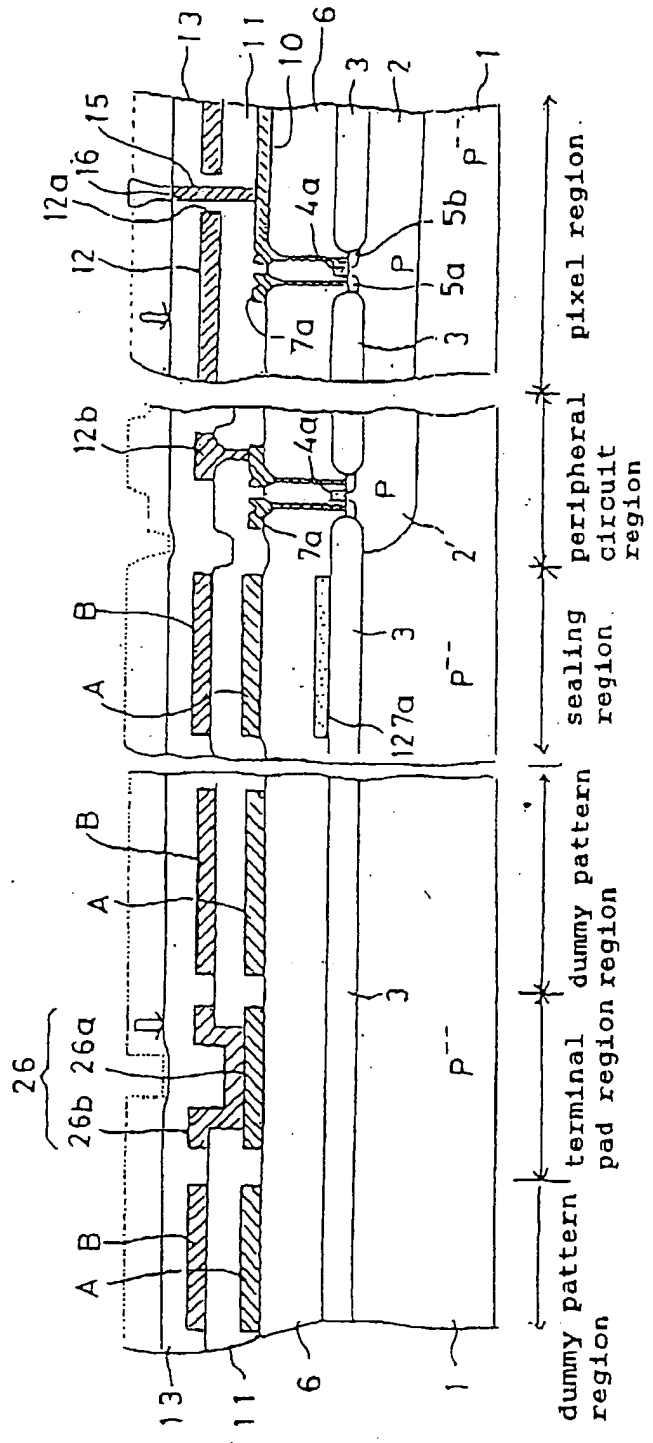
17. An electronic device comprising a display device using an electro-optical device described in claim 16.

18. A projection display device comprising a light valve using an electro-optical device described in claim 16.

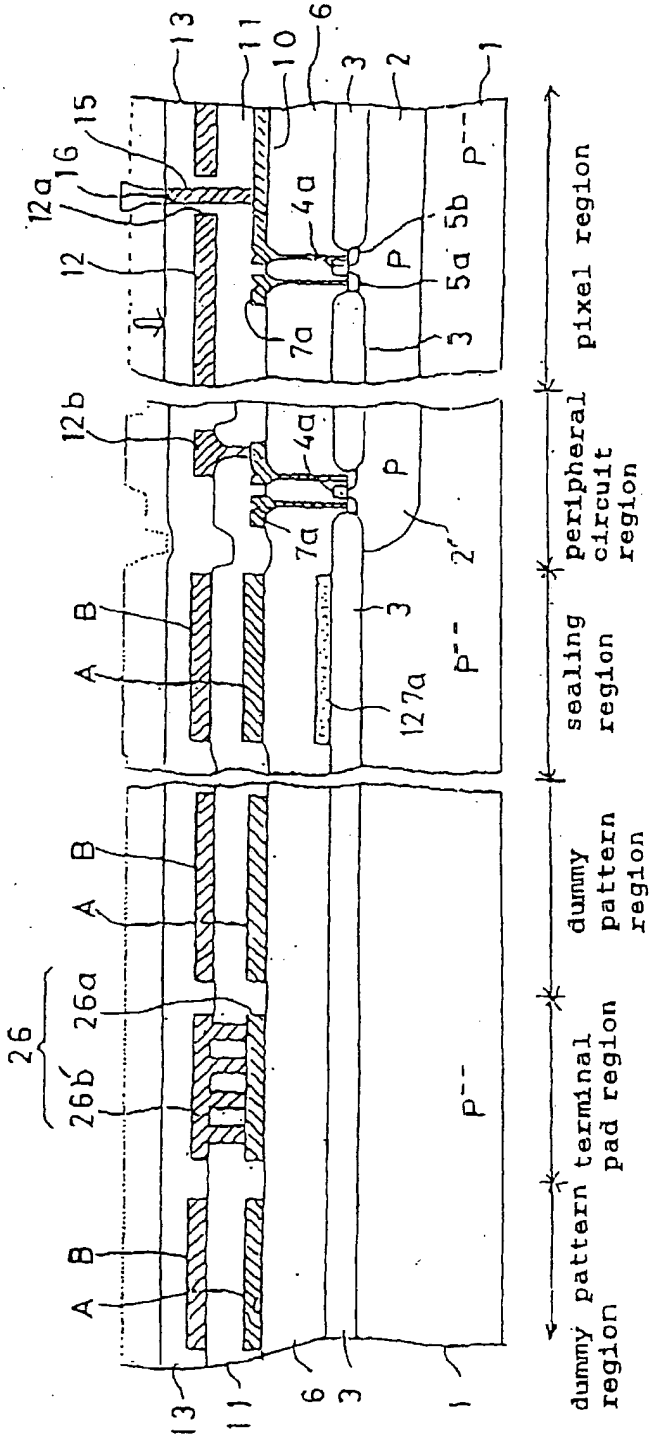
[Fig. 1]



[Fig. 2]


dummy pattern region
terminal pad region
dummy pattern region
sealing region
peripheral circuit region
pixel region
P--
P
A
B
26
26a
26b
12a
12b
12
15
16
13
11
10
6
4a
7a
5a
5b
3
2
1

[Fig. 3]


dummy pattern region
terminal pad region
dummy pattern region
sealing region
peripheral circuit region
pixel region
P--
P
A
B
26
26a
26b
12a
12b
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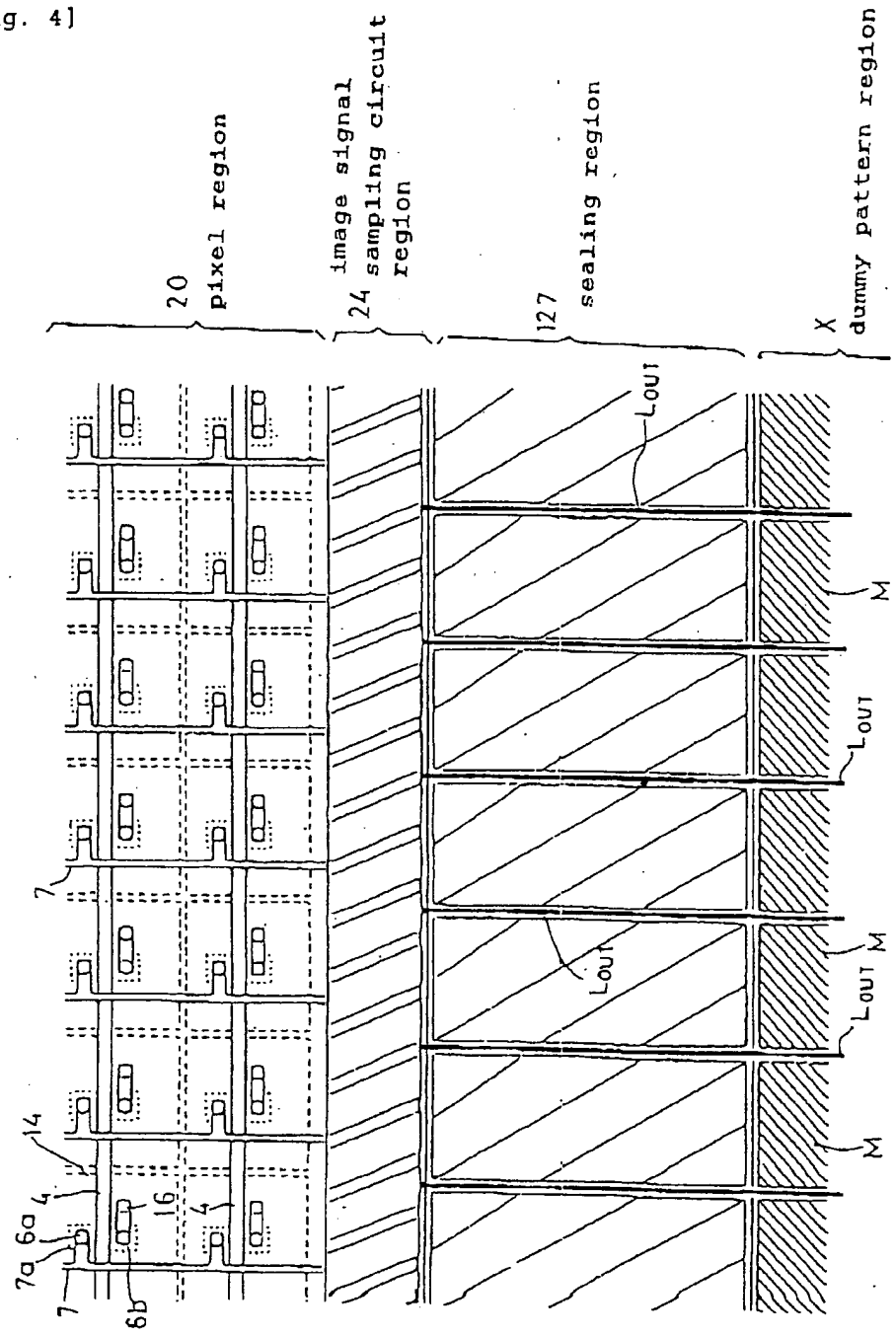
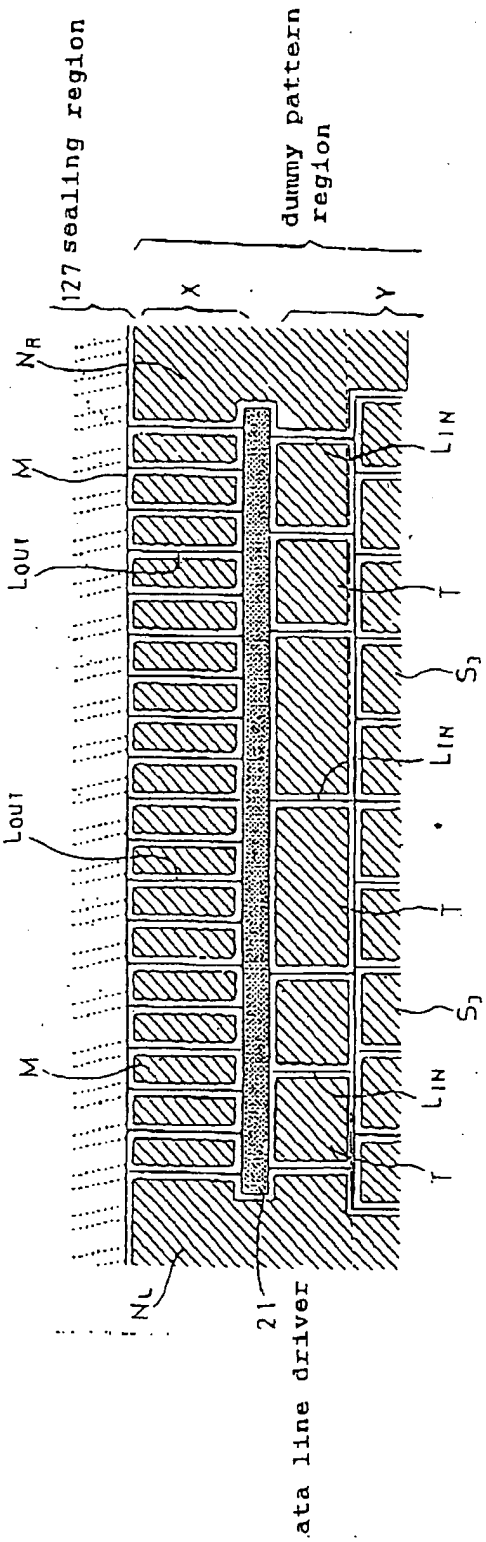
5a
5b
7a
2'
127a

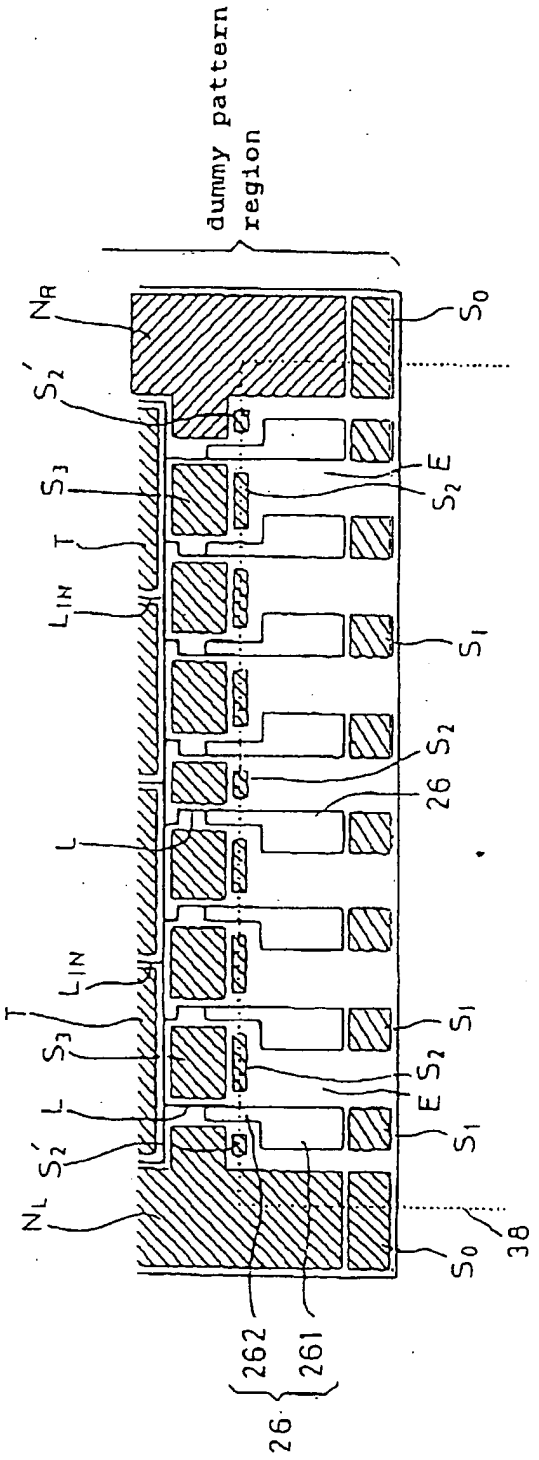
[Fig. 4]


20
pixel region
24
image signal sampling circuit region
127
sealing region
X
dummy pattern region
LOUT
M
7
14
4
6a
7a
16
6b

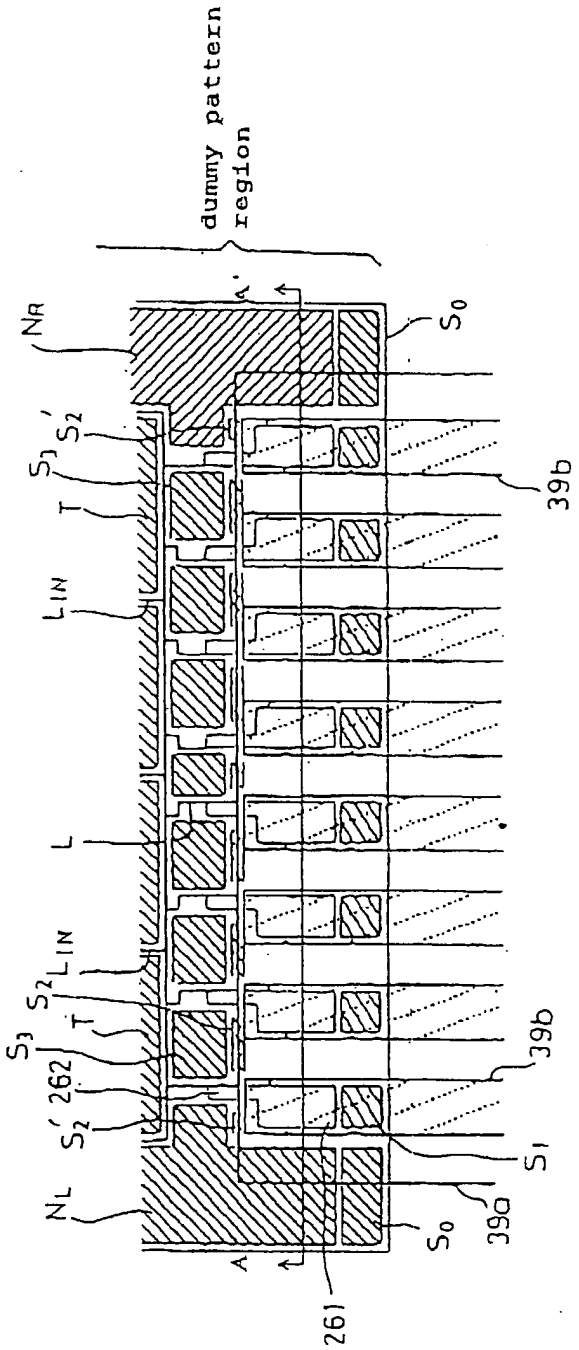
[Fig. 5]


127 sealing region
dummy pattern region
X
Y
N_R
M
L_{OUT}
L_{OUT}
M
N_L
21
ata line driver
L_{IN}
T
S_J
L_{IN}
T
S_J
L_{IN}
T

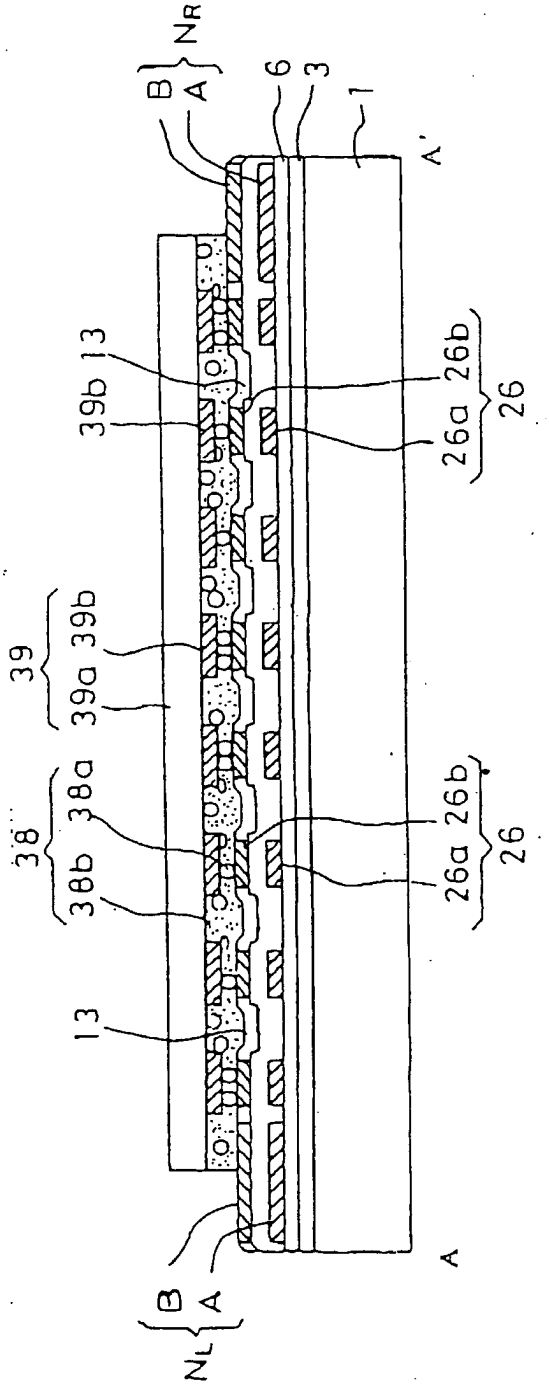
[Fig. 6]


dummy pattern region
N_R
S_0
S_2'
S_3
S_2 E
T
L_{IN}
S_1
S_2
26
L
L_{IN}
T
S_3
S_1
S_2
E
L
S_1
S_2'
N_L
S_0
38
262
261
26

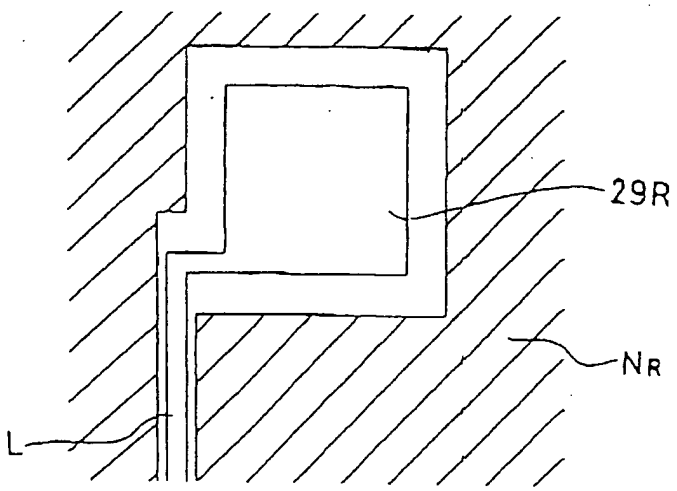
[Fig. 7]


dummy pattern region
A'
A
N_R
S_0
S_3
S_2'
T
L_{IN}
L
S_2
262
S_1
N_L
39b
39a
261

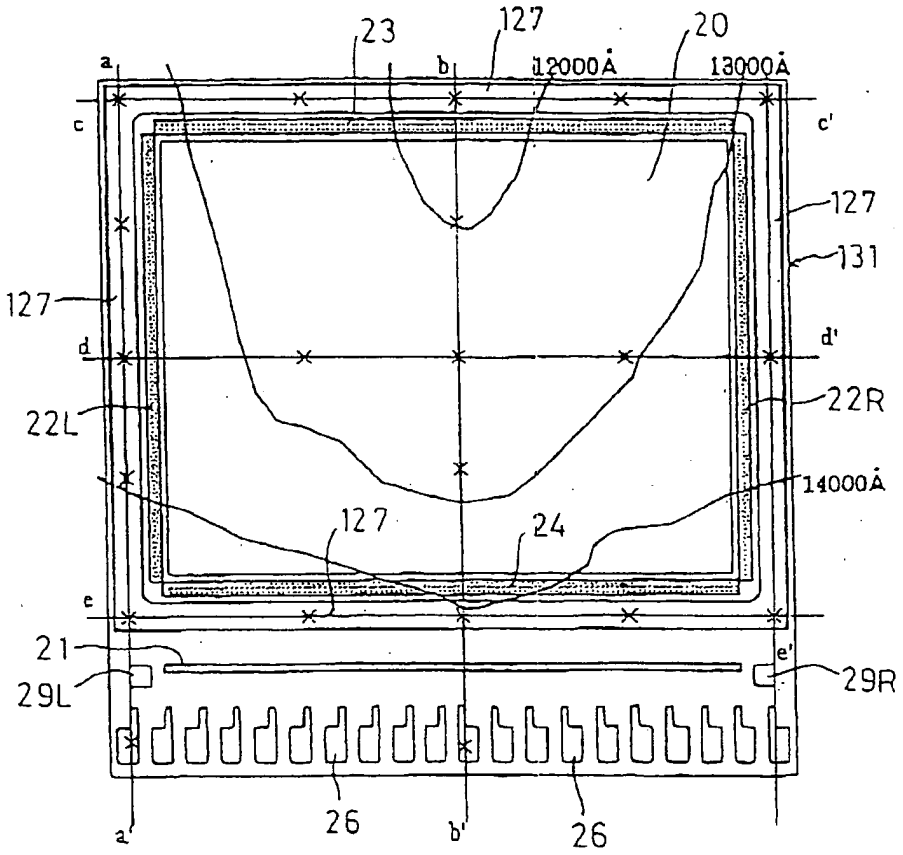
[Fig. 8]



[Fig. 9]



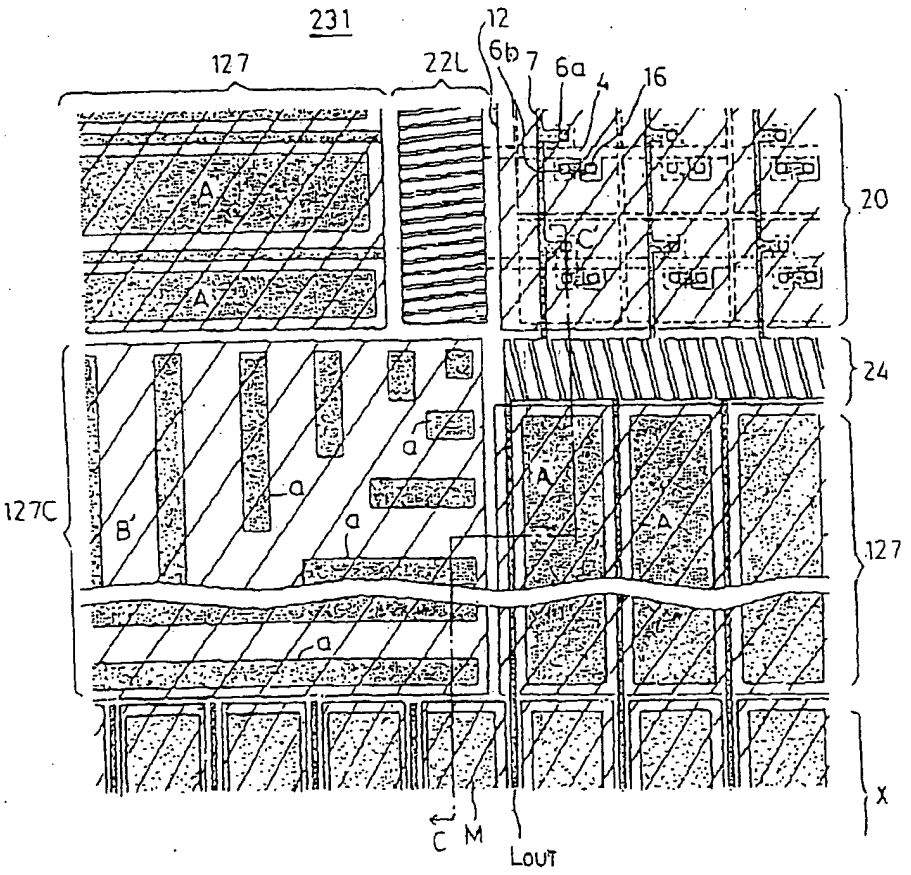
[Fig. 10]



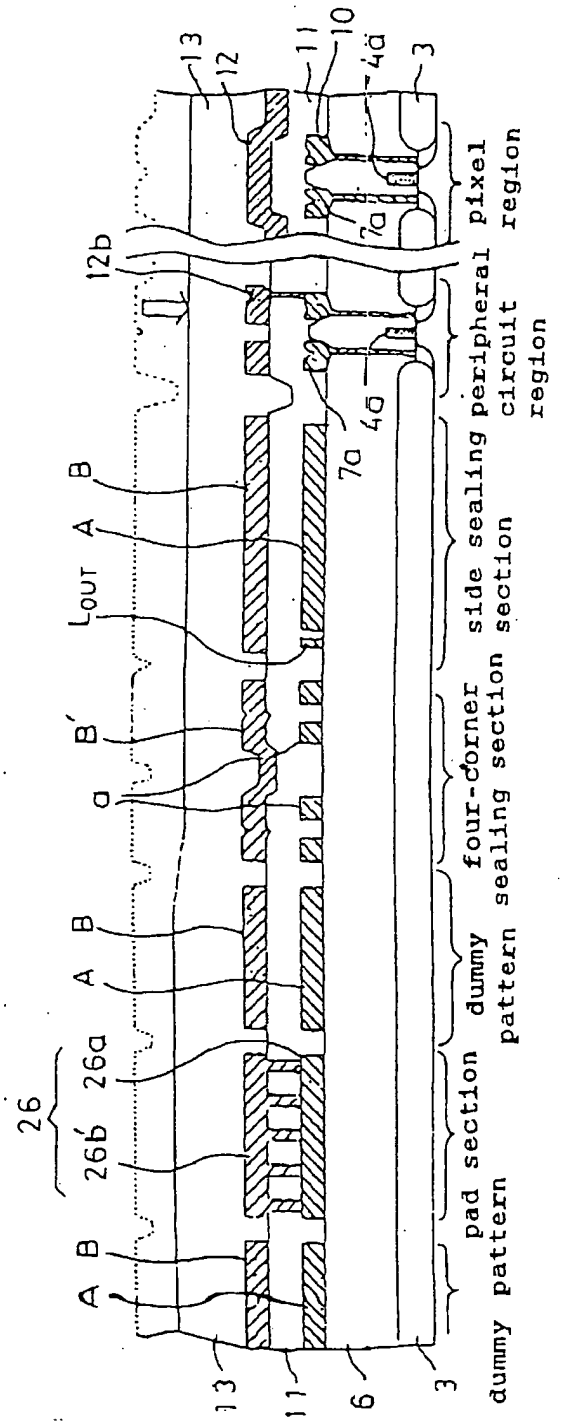
× point for measuring interlayer film thickness

provided with a dummy pattern

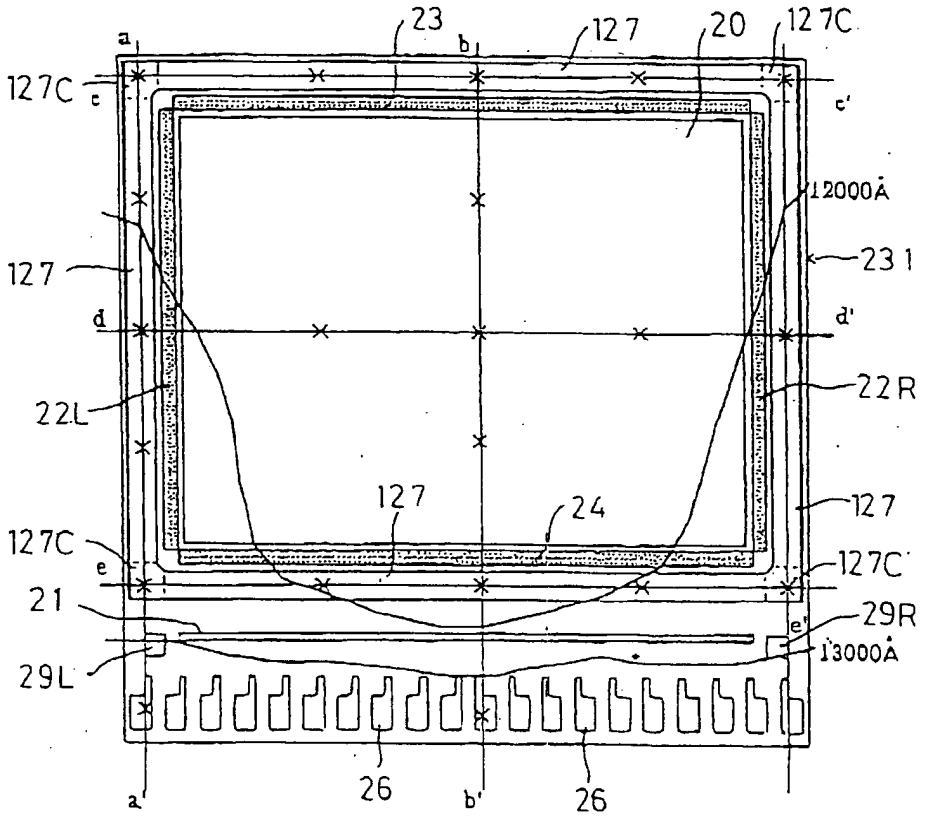
[Fig. 11]



[Fig. 12]

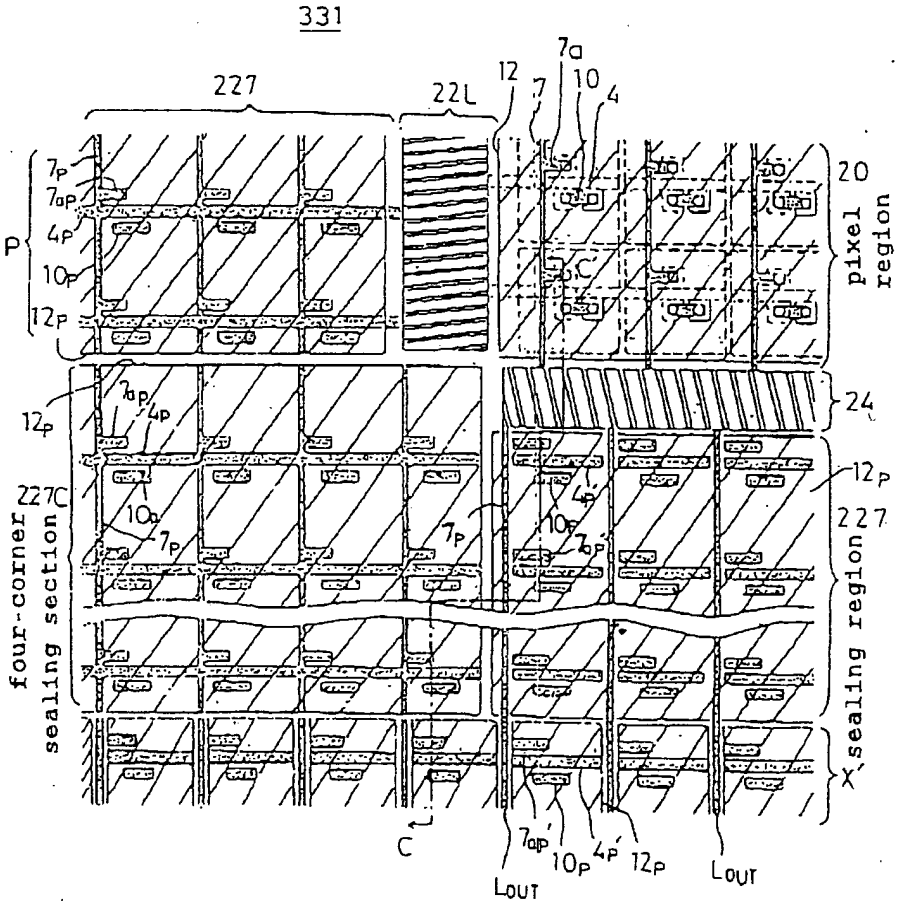

13
12
11
10
4a
3
12b
7a
pixel region
peripheral circuit region
side sealing section
four-corner sealing section
dummy pattern
pad section
dummy pattern
A
B
26
26a
26b
a
B'
Lout
13
11
6
3

[Fig. 13]

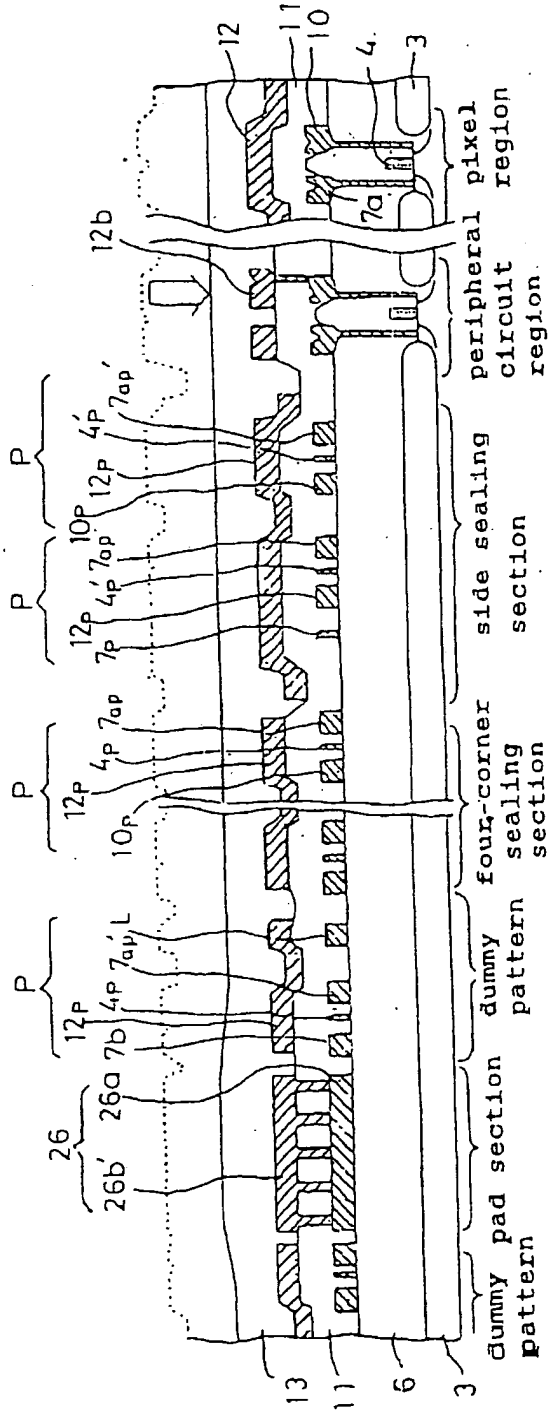


× point for measuring interlayer film thickness

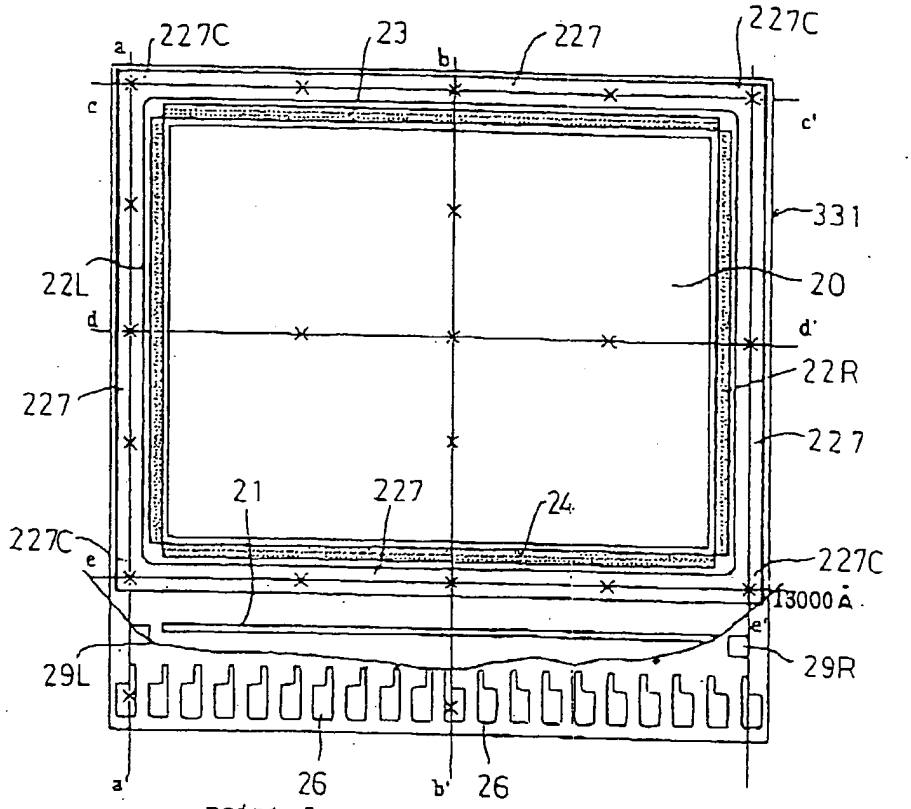
[Fig. 14]


331
227
22L
12
7
7a
10
4
20
pixel region
24
12P
227
sealing region
four-corner sealing section
227C
P
7P
7aP
4P
10P
12P
C
LOUT
7aP'
10P
4P'
12P
LOUT

[Fig. 15]

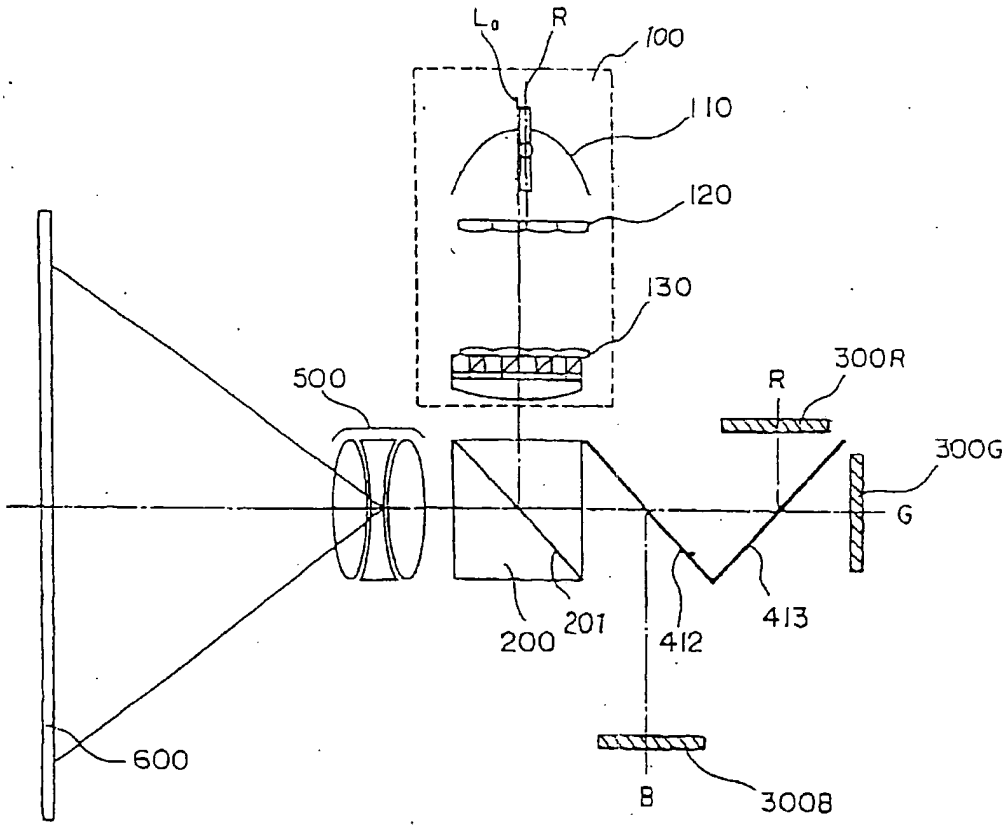

12
11
10
4
3
12b
7a
pixel region
peripheral circuit region
side sealing section
four-corner sealing section
dummy pattern
dummy pad section pattern
P
4'P
7ap'
12P
10P
4P
7ap
7P
7a'L
7b
26a
26b'
26
13
11
6
3

[Fig. 16]

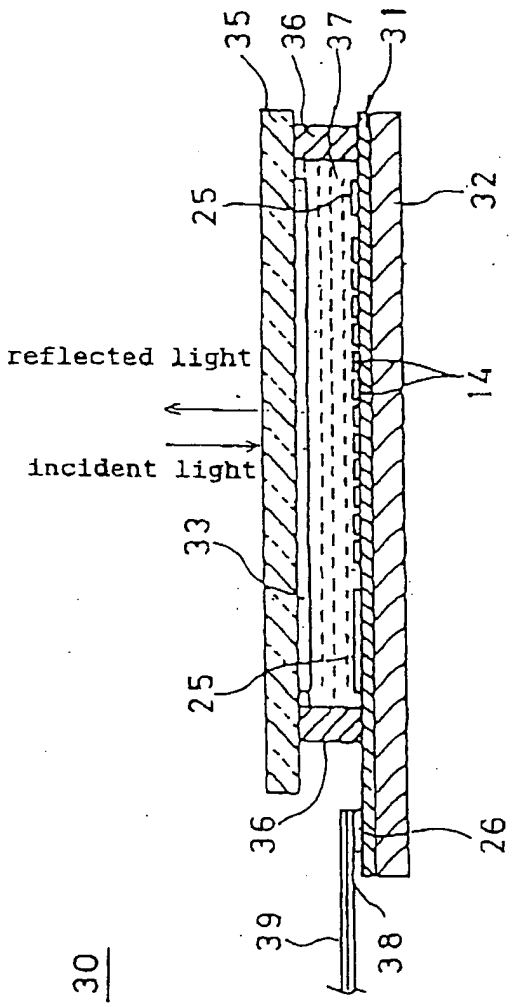


× point for measuring interlayer film thickness

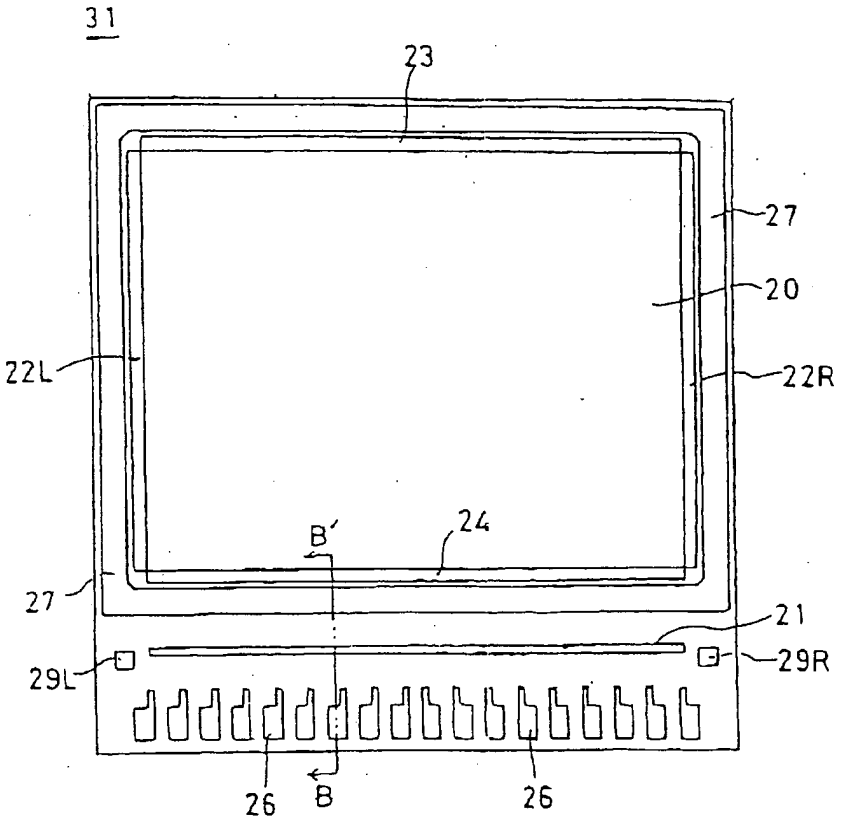
[Fig. 17]



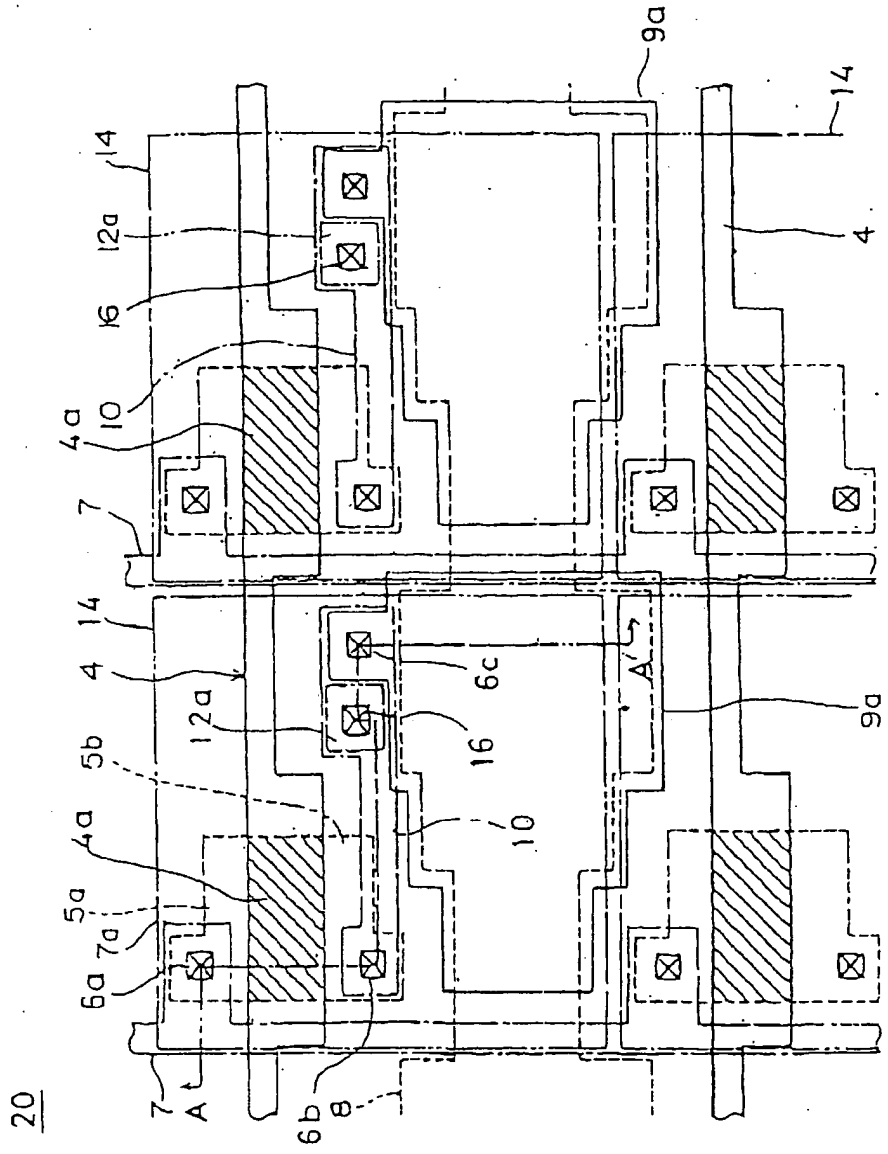
[Fig. 18]


35
36
37
31
25
32
reflected light
14
incident light
33
25
36
26
39
38
30

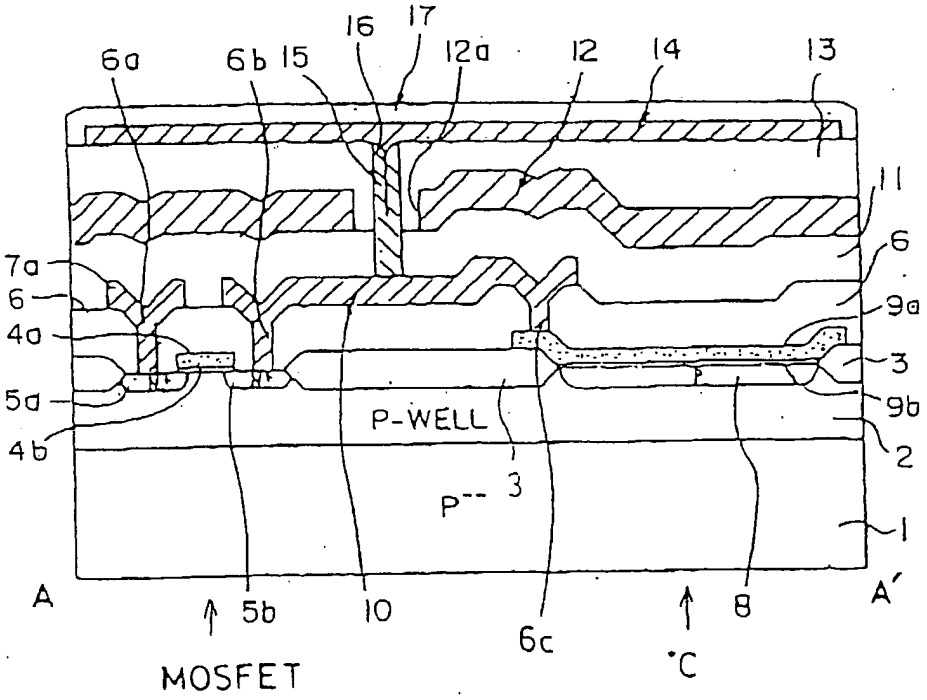
[Fig. 19]



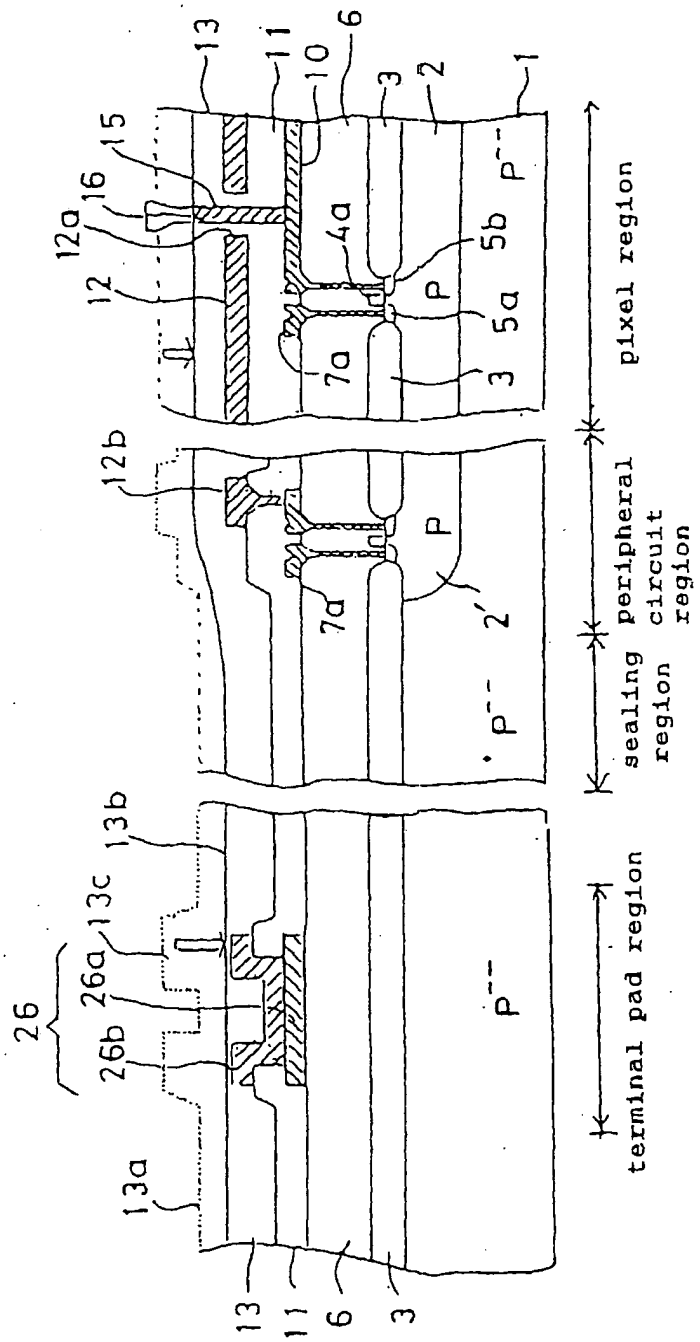
[Fig. 20]



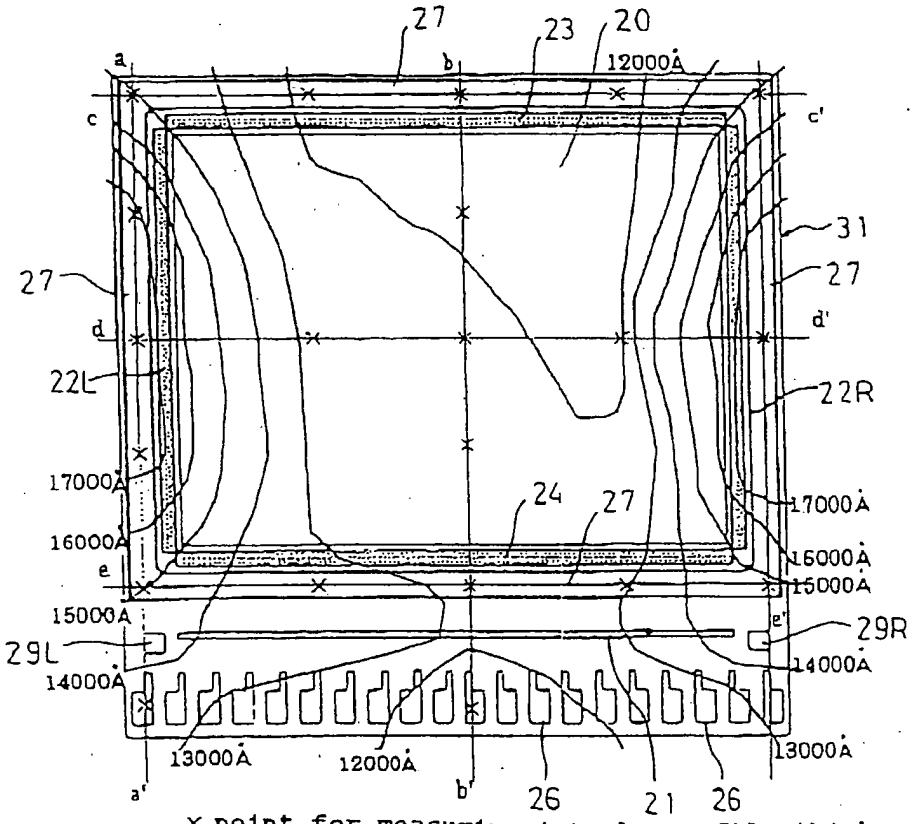
[Fig. 21]


16
17
6a
6b
15
12a
12
14
13
11
6
7a
6
9a
4a
3
5a
9b
P-WELL
4b
2
P-- 3
1
A
5b
10
6c
8
A'
MOSFET
C

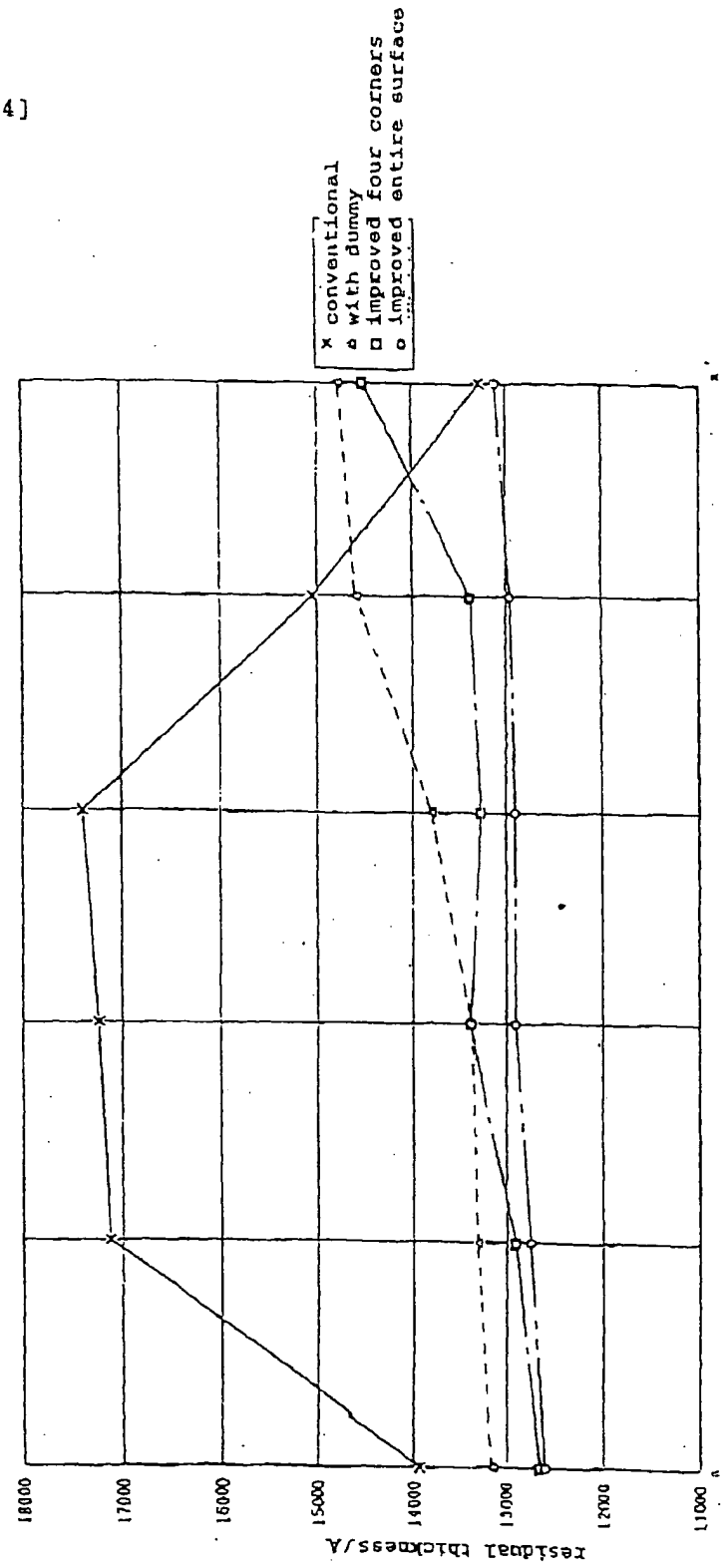
[Fig. 22]


13
11
10
6
3
2
1
15
16
12a
12
4a
5b
5a
7a
P
P--
12b
7a
P
2'
P--
13b
13c
26a
26
26b
13a
P--
13
11
6
3
pixel region
peripheral circuit region
sealing region
terminal pad region

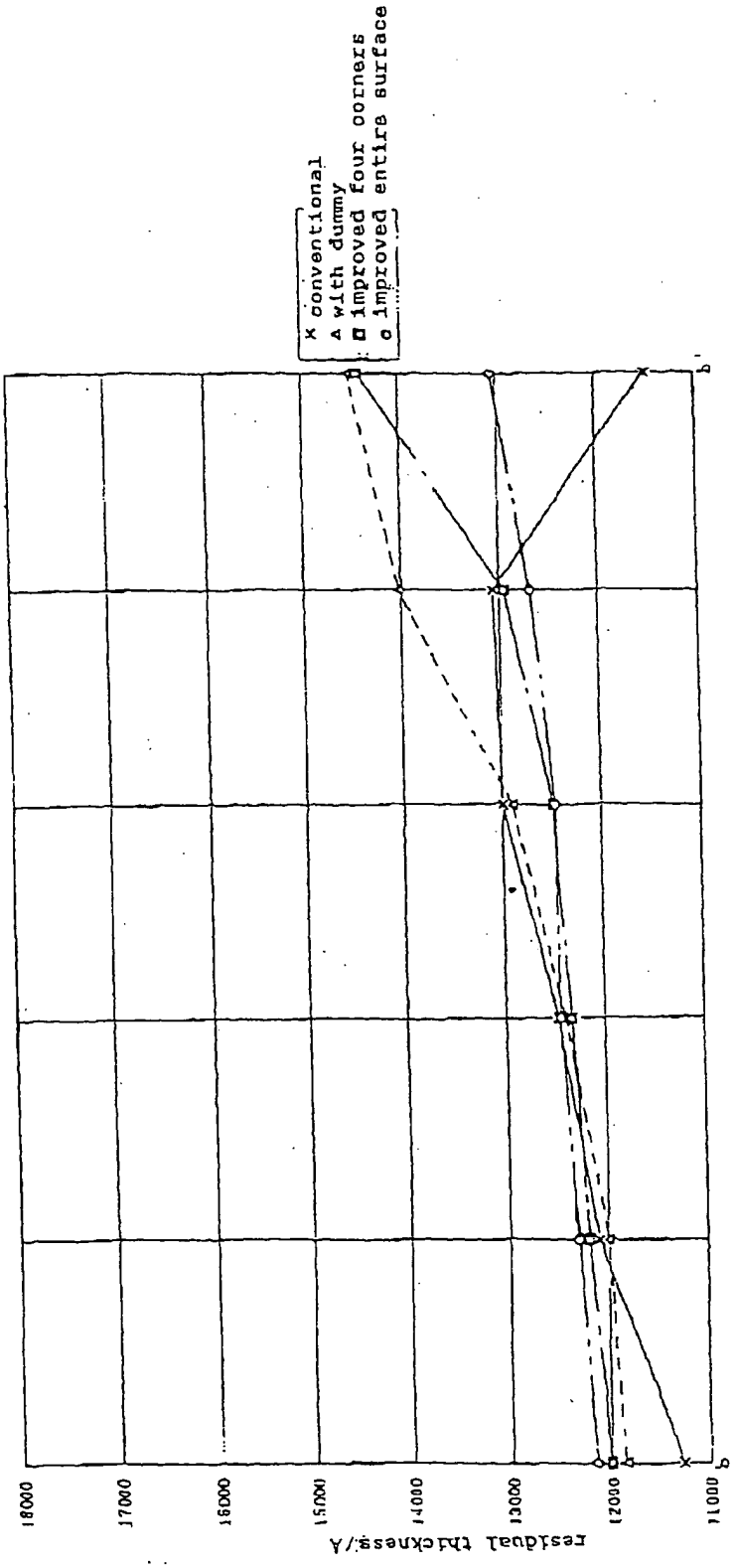
[Fig. 23]


27
23
20
12000Å
a
b
c
c'
31
27
27
d
d'
22L
22R
17000Å
16000Å
e
15000Å
24
27
17000Å
16000Å
15000Å
e'
29L
29R
14000Å
14000Å
13000Å
12000Å
13000Å
a'
b'
26
21
26
× point for measuring interlayer film thickness

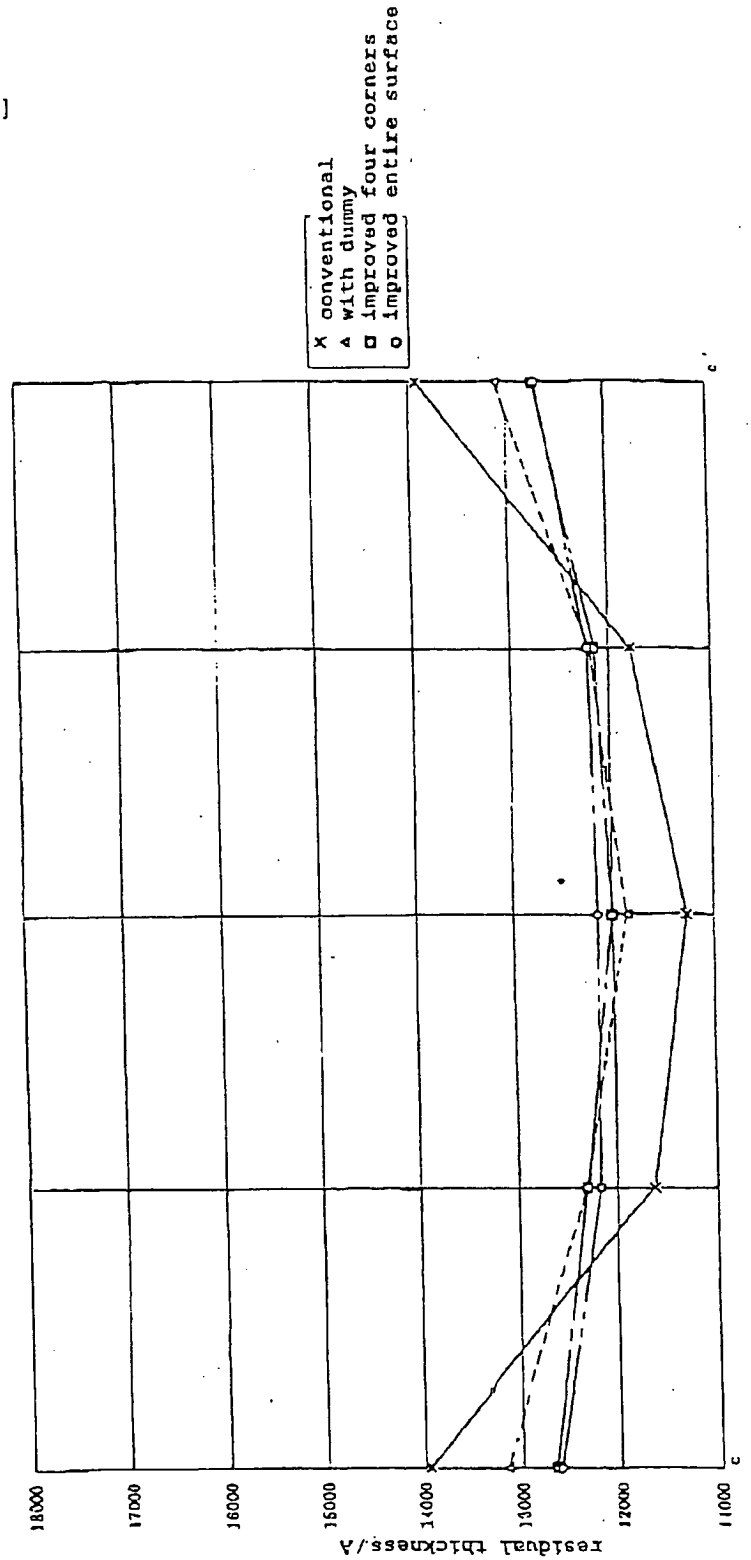
[Fig. 24]


× conventional
▵ with dummy
□ improved four corners
○ improved entire surface
residual thickness/Å
18000
17000
16000
15000
14000
13000
12000
11000

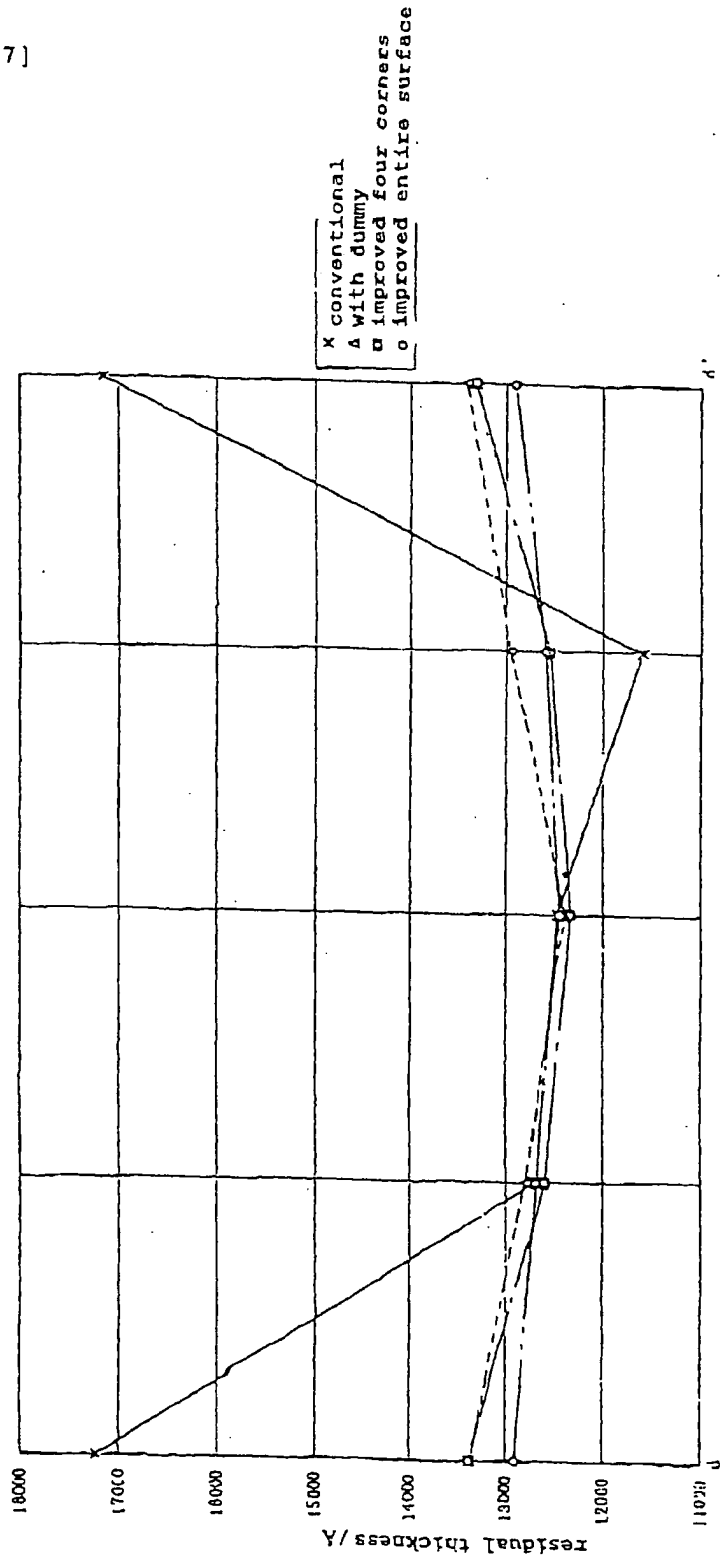
[Fig. 25]


× conventional
▲ with dummy
□ improved four corners
○ improved entire surface
residual thickness/Å
18000
17000
16000
15000
14000
13000
12000
11000

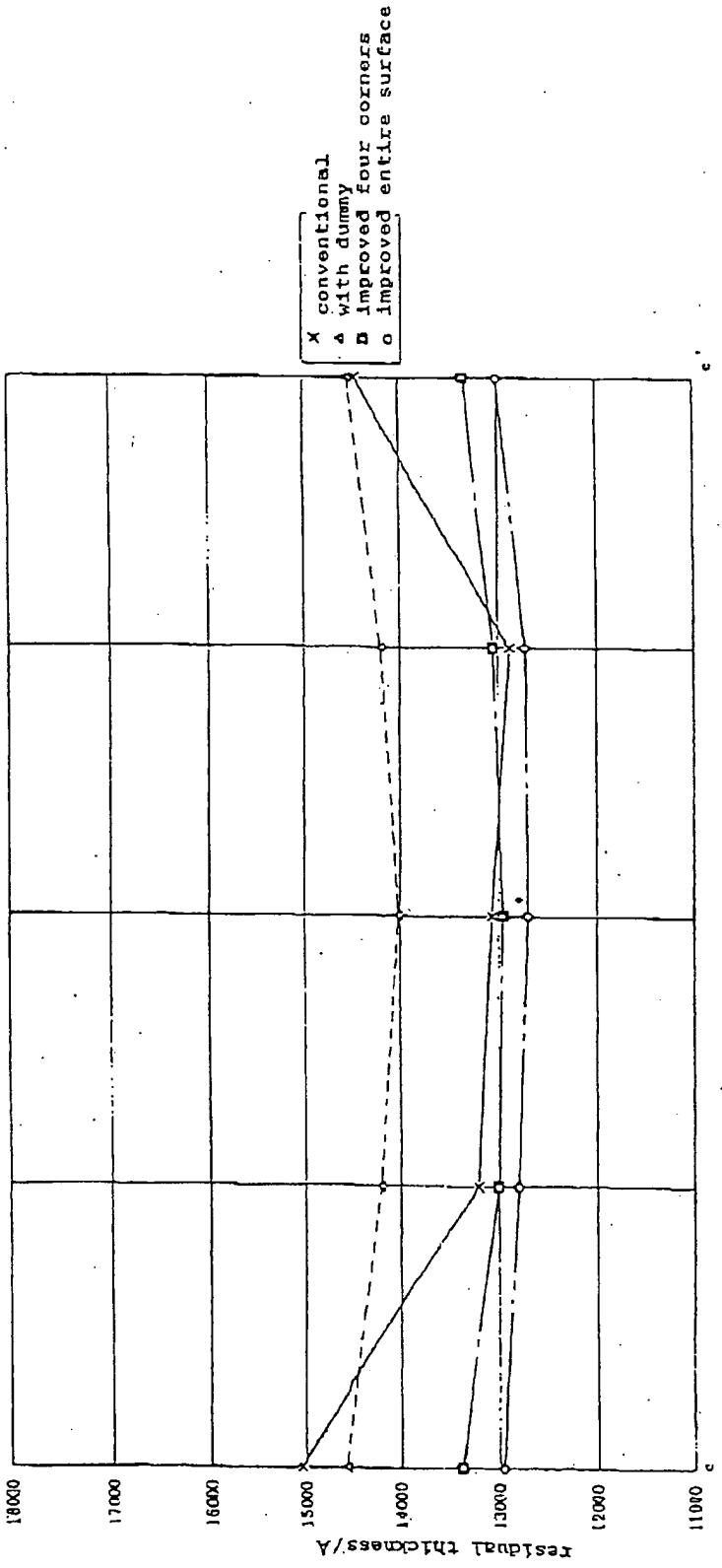
[Fig. 26]


X conventional
▲ with dummy
□ improved four corners
○ improved entire surface
residual thickness/Å
18000
17000
16000
15000
14000
13000
12000
11000

[Fig. 27]


× conventional
Δ with dummy
□ improved four corners
○ improved entire surface
residual thickness /Å
18000
17000
16000
15000
14000
13000
12000
11000
P
P'

[Fig. 28]


x conventional
▲ with dummy
■ improved four corners
○ improved entire surface
residual thickness/Å
18000
17000
16000
15000
14000
13000
12000
11000

JAPANESE PATENT OFFICE
PATENT JOURNAL (A)
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Filing Date:	May 28, 1997
Publication Date:	December 18, 1998
No. of Claims:	3 (Total of 7 pages; FD)
Examination Request:	Not filed

MANUFACTURING METHOD OF ACTIVE MATRIX TYPE LIQUID CRYSTAL DISPLAY ELEMENT

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[There are no amendments in this invention]

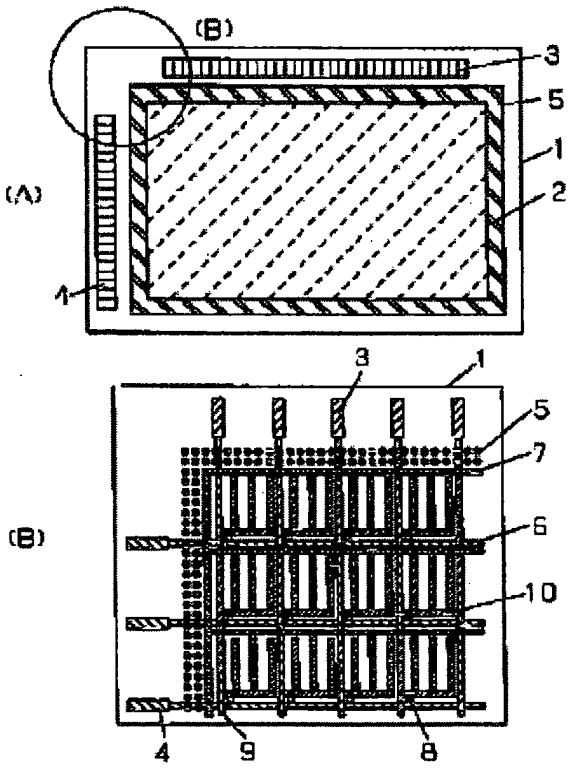
Abstract

Problem

To offer a manufacturing method for a high-quality active matrix type liquid crystal display element by improving the uniformity for rubbing a comb-shaped electrode substrate.

Means to solve

To manufacture an active matrix type liquid crystal display element, which is an active matrix type liquid crystal display element that changes the array of liquid crystal molecules by generating an electric field that is parallel to both substrates between a pixel electrode (10) and a common electrode (7), by forming a projection step (5) in the outer circumference of the display region (2) of the array substrate (1) at an equal interval at the same interval as the comb-shaped electrode or below that and rubbing the oriented layer that is formed over the array substrate (1) with a resin fiber cloth for stipulating the orientation direction of the liquid crystal.



Legend:

	1	Array substrate
	2	Display region
	3	Pull-out part of the signal line
	4	Pull-out part of the scanning line

5	Projection step
6	Scanning electrode
7	Common electrode
8	Switching element
9	Signal electrode
10	Pixel electrode

Claims

1. A manufacturing method of an active matrix type liquid crystal display element, which is an active matrix type liquid crystal display element that has an array substrate with several signal wirings and scanning wirings that are arranged in a matrix form, switching elements that are provided while corresponding to their respective cross points a, comb-shaped pixel electrode connected to the aforementioned switching element, and a comb-shaped common electrode that is formed engaging together with the aforementioned pixel electrode, an opposing substrate that is arranged facing the aforementioned array substrate, a liquid crystal that is held by the aforementioned array substrate and the aforementioned opposing substrate, and two polarization plates that are arranged outside of the aforementioned array substrate and the aforementioned opposing substrate, and the array of the liquid crystal molecules is changed by generating an electric field that is parallel to the aforementioned array substrate and opposing substrate between the aforementioned pixel electrode and the aforementioned common electrode, characterized in that a projection step at an equal interval is formed in the outer circumference outside of the display region of the aforementioned array substrate at the same interval as the aforementioned comb-shaped electrode or below that, and the oriented layer that is formed over the aforementioned array substrate is rubbed with a resin fiber cloth for regulating the direction of the orientation of the liquid crystal.

2. A manufacturing method of an active matrix type liquid crystal display element, which is an active matrix type liquid crystal display element that has an array substrate with several signal wirings and scanning wirings that are arranged in a matrix form, switching elements that are provided while corresponding to their respective cross points, a comb-shaped pixel electrode connected to the aforementioned switching element, and a comb-shaped common electrode that is formed engaging together with the aforementioned pixel electrode, an opposing substrate that is arranged facing the aforementioned array substrate, a liquid crystal that is held by the aforementioned array substrate and the aforementioned opposing substrate, and two polarization plates that are arranged outside of the aforementioned array substrate and the aforementioned opposing substrate, and the array of the liquid crystal molecules is changed by generating an electric field that is parallel to the aforementioned array substrate and opposing substrate between the aforementioned pixel electrode and the aforementioned common electrode,

characterized in that a frame that has a projection step formed at an equal interval is arranged as the outer circumference of the aforementioned array substrate at the same interval of the aforementioned comb-shaped electrode or at an interval below that, and the aforementioned array substrate is rubbed.

3. A manufacturing method of an active matrix type liquid crystal display element, which is an active matrix type liquid crystal display element that has an array substrate with several signal wirings and scanning wirings that are arranged in a matrix form, switching elements that are provided while corresponding to their respective cross points, a comb-shaped pixel electrode connected to the aforementioned switching element, and a comb-shaped common electrode that is formed engaging together with the aforementioned pixel electrode, an opposing substrate that is arranged facing the aforementioned array substrate, a liquid crystal that is held by the aforementioned array substrate and the aforementioned opposing substrate, and two polarization plates that are arranged outside of the aforementioned array substrate and the aforementioned opposing substrate, and the array of the liquid crystal molecules is changed by generating an electric field that is parallel to the aforementioned array substrate and opposing substrate between the aforementioned pixel electrode and the aforementioned common electrode, characterized in that the substrate that has a projection step formed at an equal interval at the same interval as the aforementioned comb-shaped electrode or at an interval below that is rubbed, and the aforementioned array substrate is then rubbed.

Detailed explanation of the invention

[0001]

Technical field of the invention

This invention concerns a manufacturing method for a liquid crystal display element that is used in flat displays for AV appliances, computers, and word processors, etc., a horizontal electric field mode active matrix type liquid crystal element that has less dependency on the angle of visibility as the display characteristic in particular.

[0002]

Prior art

Liquid crystal elements are applied to liquid crystal TVs, computers, and word processors, etc. They have been widely used in OA displays and projection TVs in recent years, and their display qualities have improved each year.

[0003]

An active matrix type method twisted nematic liquid crystal display that uses a thin film transistor (will be referred to as TFT below) as the switching element in particular has a significant characteristic of maintaining a high contrast in large-capacity displays, and it has been actively developed and commercialized primarily in large size and capacity full color displays for laptop computers, notebook computers, and engineering workstations that are very highly in demand in the market in recent years in particular.

[0004]

The twisted nematic (will be referred to as TN below) method is a liquid crystal displaying mode that is widely used in said active matrix method liquid crystal display element. In the TN method, a panel that has the structure where liquid crystal molecules are twisted at 90° between the electrode substrates that hold a liquid crystal layer is sandwiched by two polarization plates. When a voltage is applied between the electrode substrates, the liquid crystal molecules attempt to orient in the direction of the electric field while untying the twisted structure, the polarization of the light that passes through the panel is changed by the state of the array of these molecules, and the transmission rate of the light is modulated. However, the polarization of the transmitted light is also changed by the incident direction of the light that enters the liquid crystal panel although in the same molecular array state, and the transmission rate of the light will be different while corresponding to the incident direction. More precisely, the liquid crystal panel is characterized in that it is dependent on the visual angle. This characteristic of the visual angle causes a reversing phenomenon of the brightness when the visual point is inclined diagonally in the direction of the main visual angle, which is in the direction of the major axis of the liquid crystal molecule in the intermediate layer of the liquid crystal layer. More precisely, it refers to the phenomenon where the display intensity at a certain voltage at this display mode becomes brighter than the intensity at a voltage lower than that. The intensity reversing phenomenon where a high voltage is applied for a black display in particular has become a serious problem in the picture quality of the liquid crystal panel.

[0005]

To solve this problem, there is a horizontal electric field method with its application direction to the liquid crystal in the direction almost parallel to the substrate instead of applying the electric field in a vertical direction of the substrate as in the TN type liquid crystal display method, and it is disclosed in the Japanese Kokoku Patent No. Sho 63[1988]-21907 and Japanese Kokai Patent Application No. Hei 6[1994]-160878, for example. A common horizontal electric field method liquid crystal display element has a structure where a panel that has a liquid crystal

held by an electrode substrate that has a comb-shaped pixel electrode engaged together with a common electrode and an opposing substrate is sandwiched by two polarization plates. A voltage is applied between the pixel electrode and the common electrode here, and the molecular sequence of the liquid crystal between the electrodes will be changed in a planar manner. The transmission rate of the light will be modulated, and a picture image will be displayed. In this horizontal electric field method, the change in the array of the liquid crystal molecules changes parallel to the electrode substrate, and the dependency of the light modulation on the angle of visibility will be less.

[0006]

With both the TN type and horizontal electric field type, the rubbing method that rubs the surface of an oriented layer, such as a polyimide, for example, that is formed over an electrode substrate using a resin fiber cloth is generally used. In a general rubbing method, a roll that has a rayon and nylon cloth with a fiber length at about 1-5 mm wrapped is rotated, the substrate or the roll is moved in a state where the tip of the fiber touches at about 0.1-0.5 mm, and the entire surface of the substrate is treated. The orientation direction of the liquid crystal will be determined in the direction that the fiber tips rub the substrate by this rubbing method.

[0007]

For rubbing the substrate, when a rubbing cloth (42) that is wrapped around a rubbing roll (41) is rotated, and the substrate (43) is provided with a rubbing treatment in the direction of arrow (44), as indicated in Figure 4, the hair tips are separated when they rub the substrate end surfaces and areas with level differences, and the polarized area (45) is formed in the hair of the rubbing cloth (42) by the effect of the substrate end surfaces and the effect of an irregular level difference of about 0.1-1 μm by the pixel electrode that is formed over an actual active matrix type liquid crystal display element TFT array substrate, electrode pull-out electrode for receiving electric signals from an external driving circuit, and signal wiring electrode for transmitting signals to the inside of the substrate.

[0008]

Figure 5(A) also shows an abbreviated diagram of the rubbing process, and Figure 5(B) shows an enlarged diagram of its major part. An electrode substrate (53) is moved toward a rubbing cloth (52), which is wrapped around a rubbing roll (51) and rotated, in the direction of arrow (54), and rubbing treatment is obtained. The diameter of 1 hair (55) during this is 10-30 μm in general. When the hair tips rub the electrode substrate (53) in the direction of arrow (56), a region that the cloth does not rub, which is a non-orientation region (58) where the

orientation direction of the liquid crystal cannot be stipulated, is formed before and after the projecting part (57) of a pixel, for example, that is formed over the electrode substrate (53). With this non-orientation region (58) in a general TN mode liquid crystal display element as indicated in Figure 6, the light shielding layer (62) that is provided at the opposing substrate (61) is laminated in a manner such that the non-oriented region (65) that is formed by the projecting parts (64) by the electrodes and wiring parts that are formed in the array substrate (63) will be hidden, and the non-oriented region (65) does not affect the display quality. Here, (66) indicates an opposing common electrode, (67) is a liquid crystal layer, (68) is an oriented layer, (69) is a color filter layer, and (610) is a pixel electrode. However, in a general horizontal electric field type liquid crystal display element indicated in Figure 7, for obtaining a larger light transmission amount, the light shielding layer (72) that is formed in the opposing substrate (71) is arranged in a manner such that it hides only the wiring step area (73) and laminated. Accordingly, the non-oriented region (76) that is formed in the step area (75) of the comb-shaped electrode, which is a pixel electrode that is formed in the array substrate (74), is not completely hidden by the light shielding layer (72) of the opposing substrate (71), and the non-oriented region (76) has a direct effect on the display quality. More precisely, a display defect occurs when there is a partial difference in the size of the non-oriented region (76). Here, (77) indicates an oriented layer, (78) is a color filter layer, and (79) is a liquid crystal layer.

[0009]

In the rubbing process as described above, the unevenness in the rubbing cloth occurs by the effect of the irregularity on the substrate end surfaces and the substrate surfaces through the rubbing treatment. When a horizontal electric field mode liquid crystal display element is rubbed in this state, there is a difference in the size of the non-oriented region between the polarized area and the regular area of the rubbing cloth, and that affects the direction of the advancement of the roll or the substrate. As a result, a streak-shaped irregularity (46) is formed over the display region, as indicated in Figure 4. The unevenness in the cloth by such irregularity (46) becomes more prominent as the number of substrates that are treated for rubbing increases, and the condition for the formation of the streak irregularity also continues to deteriorate.

[0010]

For this streak-shaped irregularity, a reduction of the non-oriented region, which is a reduction of the level difference area, will be considered. As its measurement method, a method for forming a flat layer over a comb-shaped electrode is considered. However, it results in an increase in the cost and a decline in the yield by an increase of the processes and the effective voltage phenomenon that is applied to the liquid crystal by the flat layer. As an orientation

method that replaces the aforementioned rubbing method, the formation of an oriented film by a diagonal deposition of silicon oxide, Langmuir-Blodgett's film, and a chemical adsorption method also has been attempted, but it is significantly inferior to the rubbing method from the viewpoint of mass productivity.

[0011]

Problems to be solved by the invention

The purpose of this invention for a rubbing method with an excellent mass productivity at a horizontal electric field mode that has a comb-shaped electrode on a substrate is to obtain a high-quality display element without the display irregularity that is observed in the aforementioned conventional example.

[0012]

Means to solve the problems

For the aforementioned purpose, this invention concerns a manufacturing method, which is a manufacturing method of an active matrix type liquid crystal display element that has an array substrate with several signal wirings and scanning wirings that are arranged in a matrix form, switching elements that are provided while corresponding to their respective cross points, a comb-shaped pixel electrode connected to the aforementioned switching element, and a comb-shaped common electrode that is formed engaging together with the aforementioned pixel electrode, an opposing substrate that is arranged facing the aforementioned array substrate, a liquid crystal that is held by the aforementioned array substrate and the aforementioned opposing substrate, and two polarization plates that are arranged outside of the aforementioned array substrate and opposing substrate, and the array of the liquid crystal molecules is changed by generating an electric field that is parallel to the aforementioned array substrate and the opposing substrate between the aforementioned pixel electrode and the aforementioned common electrode, in that a projection step at an equal interval is formed in the outer circumference outside of the display region of the aforementioned array substrate at the same interval as the aforementioned comb-shaped electrode or below that, and the oriented layer that is formed over the aforementioned array substrate is rubbed with a resin fiber cloth for stipulating the direction of the orientation of the liquid crystal.

[0013]

The purpose of this invention for the projection step is also attained by

arranging and forming a frame that has a projection step formed at an equal interval in the outer circumference of the array substrate at the same interval as the aforementioned comb-shaped electrode or below that, and rubbing it.

[0014]

The purpose of this invention is also attained by first rubbing the substrate that has a projection step formed at an equal interval at the same interval as the aforementioned comb-shaped electrode or below that, and then rubbing the array substrate.

[0015]

Embodiments of the invention

This invention can be implemented in the forms described in the respective claims. As described in Claim 1, in an active matrix type liquid crystal display element that has an array substrate with several signal wirings and scanning wirings that are arranged in a matrix form, switching elements that are provided while corresponding to their respective cross points, a comb-shaped pixel electrode connected to the aforementioned switching element, and a comb-shaped common electrode that is formed engaging together with the aforementioned pixel electrode, an opposing substrate that is arranged facing the aforementioned array substrate, a liquid crystal that is held by the aforementioned array substrate and the aforementioned opposing substrate, and two polarization plates that are arranged outside of the aforementioned array substrate and opposing substrate, and the array of the liquid crystal molecules is changed by generating an electric field that is parallel to the aforementioned array substrate and opposing substrate between the aforementioned pixel electrode and the aforementioned common electrode, a projection step at an equal interval is formed in the outer circumference outside of the display region of the aforementioned array substrate at the same interval as the aforementioned comb-shaped electrode or below that, and the orientation direction of the liquid crystal is stipulated by rub-treating the array substrate.

[0016]

As described in Claim 2, a frame that has a projection step formed at an equal interval is also arranged in the outer circumference outside of the array substrate that has the comb-shaped electrode formed at the same interval as the aforementioned comb-shaped electrode or below that, and it is rubbed for stipulating the orientation direction of the liquid crystal.

[0017]

As described in Claim 3, the substrate that has a projection step formed at an equal interval is formed at the same interval as the aforementioned comb-shaped electrode of the array substrate that has the comb-shaped electrode formed or below that, and the array substrate that has the comb-shaped electrode formed is afterwards rubbed for stipulating the orientation direction of the liquid crystal.

[0018]

Application examples

Concrete application examples of this invention will be explained in detail while referring to the figures below.

[0019]

Application Example 1

Figure 1(A) is an abbreviated front view diagram of a horizontal electric field mode TFT array substrate that is used in the manufacturing method for a liquid crystal display element in Application Example 1 in this invention. Figure 1(B) shows an enlarged diagram of area (B) in Figure 1(A).

[0020]

Over an array substrate (1), a projection step (5) at an equal pitch is formed in the circumference of the display region that has a display region (2) that has switching elements and pixel electrodes arranged in a matrix shape, pull-out area (3) of its signal line, and pull-out area (4) of its scanning line. Figure 1(B) is an enlarged diagram of the boundary area of the array substrate (1) inside and outside of the display region. Over the array substrate (1), scanning electrodes (6) are pattern-formed in the shape in the figure using chromium. At the same time, common electrodes (7) are also formed in the shape in the figure along the direction of the long side of the pixel. The width of the common electrode (7) is 5 μm. The material is not limited only to chromium, and aluminum and metals that have aluminum as the main component, for example, in a conductive single layered film or multilayered film may also be used. As the gate insulating film of TFT, silicon nitride (SiN_x) is laminated on top of it. Next, a switching element (8) that controls the switching function of TFT is laminated by amorphous silicon (α-Si) by a plasma CVD method, an insulating layer of silicon nitride (SiN_x) is formed again and patterned. Titanium/aluminum (Ti/Al) accumulated in two layers are afterwards accumulated by a sputtering method, and the signal electrode (9) and the pixel electrode (10) are pattern formed together with the switching element by dry etching. The width of the pixel electrode (10) is

5 μm. The material is not limited to titanium/aluminum (Ti/Al) only, and conductive metals in a single layered film or multilayered film may also be used. The distance between the common electrode (7) and the pixel electrode (10) during this is 10 μm, and a projecting structure of 3000 Å from the substrate surface is used. A projection step (5) in a round shape with a diameter of 5 μm and a level difference of 3000 Å is formed at an interval of 5 μm at the outside of the display region at the formation of the aforementioned insulating film. The material of the projection step (5) is not limited only to an insulating material, and conductive metals in a single layered film or multilayered film may also be used.

[0021]

A polyimide film is flexographically printed on a thin-film transistor array substrate that is completed in this manner and an opposite color filter substrate that has a light shielding band is formed, dried and hardened as an oriented layer, and provided to the rubbing treatment. In the rubbing treatment, a rayon cloth with a fiber diameter of one fiber of 20 μm and a density of 20000/cm^2 is wrapped around a roll with a diameter of 100 mm, the roll is rotated at 800 rpm in a state where the hair is pushed to the substrate for 0.2 mm, and the aforementioned array substrate and the opposing substrate are treated in a specified direction. The rubbing cloth rubs the projection step at an equal pitch that is formed outside of the display region before rub-treating the display region (2) in the array substrate (1) that has a comb-shaped electrode formed here, and the unevenness in the rubbing cloth will be corrected, and the non-oriented region that is formed in the level difference area of the comb-shaped electrode in the display region can be made even. The array substrate (1) and the opposing substrate after the rubbing treatment will be laminated together, a liquid crystal is poured in by a vacuum pouring method, and a liquid crystal display element is prepared. As a result, irregularity in a streak shape is not formed. Liquid crystal display elements were prepared by providing 1 roll to rub-treating 2000 substrates, but the deterioration in the display quality was not observed.

[0022]

The projection step was formed in the region adjacent to the display region in this application example; however, an array in the same structure is also prepared by forming the projection step in the peripheral area of the base substrate, as indicated in Figure 2, and a horizontal electric field type liquid crystal display element is prepared by the same method. As a result, the unevenness in the rubbing cloth was corrected by the effect of the projection step, and the formation of the rubbing streak was not observed. Here, (21) indicates a horizontal electric field type array substrate, (22) is a display region, (23) is a pull-out part of the signal line, (24) is a pull-out part of the scanning line, (25) is a projection step, (26) is a scanning electrode, (27) is a

common electrode, (28) is a switching element, (29) is a signal electrode, and (30) is a pixel electrode.

[0023]

The projection step (25) in this application example is in a round shape. However, the change in the correcting effect by the rubbing cloth by the level difference is not observed if it is at the same equal pitch at the same interval as the comb-shaped electrode or below that. A similar result was also obtained if the size of the level difference was about the same as the level difference of the array substrate (21) or more.

[0024]

Comparative example

A conventional horizontal electric field TFT array substrate by the same method and the electrode structure as in the aforementioned Application Example 1 without the formation of the projection step at an equal interval in the peripheral area of the substrate is prepared, subjected to the rubbing treatment, and a liquid crystal display element is prepared. As a result, a thin streak-shaped irregularity was observed in the progressing direction of the substrate during rubbing. The streak became vivid after providing 1 rubbing roller to 100 rubbing treatments, and the formation of the streak became more prominent gradually as the rubbing number increased.

[0025]

Application Example 2

Figure 3(A) shows an abbreviated diagram of a horizontal electric field mode TFT array substrate that is used in the liquid crystal display element in Application Example 2 of this invention, and Figure 3(B) is an enlarged diagram of Figure 3(A).

[0026]

In the conventional horizontal electric field type liquid crystal display array substrate (31) that is prepared in the aforementioned comparative example (conventional horizontal electric field type structure), a frame that has a round projection step with a diameter of 5 μm and a level difference of 1 μm formed is arranged in the outer circumference of the substrate of a rubbing system, and subjected to the rubbing treatment. The unevenness in the rubbing cloth is corrected by rubbing the projection step that is formed over the substrate at an equal interval arranged in the substrate periphery by the rubbing cloth, and a uniform rubbing treatment is obtained, and the formation of the rubbing streak is not observed. Here, (31) indicates a conventional horizontal electric field type array substrate, (32) is a display region, (33) is a pull-out part of the signal

line, (34) is a pull-out part of the scanning electrode, (35) is a projection step formation frame, (36) is a scanning electrode, (37) is a common electrode, (38) is a switching element, (39) is a signal electrode, and (40) is a pixel electrode.

[0027]

The shape of the projection step in this application example is round, but no change in the correcting effect by the rubbing cloth by the level difference is observed if it is at the same interval as the comb-shaped electrode or below and at an equal pitch, and the same result was also obtained if the size of the level difference was about the same as the level difference of the array substrate or more.

[0028]

Application Example 3

A 3000 Å SiN_x film is formed over a glass substrate, and a substrate that has an irregular stripe pattern with a level difference of 3000 Å at a width of 5 μm and a pitch of 5 μm formed by a photolithographic method is prepared. This is rubbed prior to the rubbing treatment of the conventional horizontal electric field comb-shaped array substrate, and the formation of the rubbing streak that is polarized by the pattern in the array substrate was not observed.

[0029]

In this application example, the irregular pattern at an equal pitch is in a stripe pattern; however, no change in the correcting effect by the rubbing cloth by the pattern of the level difference is observed if it is at the same interval as the comb-shaped electrode or below and at an equal pitch. The same effect was also obtained if the size of the level difference was about the same as the level difference of the array substrate or more.

[0030]

Effect of the invention

As explained above, the effect as a liquid crystal display that will be described below will be obtained in this invention.

[0031]

Through the invention described in Claim 1, the projection step at an equal interval that is formed in the outer circumference outside of the display region of the substrate corrects the unevenness in the rubbing cloth that occurs during rubbing. Accordingly, the display region will be evenly rubbed, and a high-quality liquid crystal display element can be manufactured.

[0032]

Through the invention described in Claim 2, a frame that has a level difference at an equal pitch formed is arranged in the periphery of the substrate during rubbing for correcting the unevenness of the rubbing cloth that occurs during rubbing. Accordingly, the display region will be evenly rubbed, and a high-quality liquid crystal display element can be manufactured.

[0033]

Through the invention described in Claim 3, the substrate as a manufacturing product is rubbed after rubbing the level difference dummy substrate at an equal pitch. As a result, the unevenness in the rubbing cloth will be corrected, the display region will be evenly rubbed, and a high-quality liquid crystal display element can be manufactured.

[0034]

This invention concerns a technique that has many significant benefits in the preparation of a liquid crystal panel, and a liquid crystal display with a high display performance can be manufactured.

Brief description of the figures

Figure 1(A) is an abbreviated top view diagram of the liquid crystal display element in Application Example 1 in this invention.

Figure 1(B) is an enlarged diagram of the area indicated by a circle in (A).

Figure 2(A) is an abbreviated top view diagram of another liquid crystal display element in Application Example 1 in this invention.

Figure 2(B) is an enlarged diagram of the area indicated by a circle in (A).

Figure 3(A) is an abbreviated top view diagram of the liquid crystal display element in Application Example 2 in this invention.

Figure 3(B) is an enlarged diagram of the area indicated by a circle in (A).

Figure 4 is a diagram that explains the concept of the unevenness in the rubbing cloth.

Figure 5 is a diagram that explains the concept of the unevenness of the rubbing process.

Figure 6 is an abbreviated cross-sectional diagram of the TN mode panel.

Figure 7 is an abbreviated cross-sectional diagram of the horizontal electric field mode by the comb-shaped electrode.

Explanation of symbols

1, 21, 31 Array substrates

2, 22, 32	Display regions
3, 23, 33	Pull-out parts of signal lines
4, 24, 34	Pull-out parts of scanning lines
5, 25	Projection steps
6, 26, 36	Scanning electrodes
7, 27, 37	Common electrodes
8, 28, 38	Switching elements
9, 29, 39	Signal electrodes
10, 30, 40	Pixel electrodes
35	Projection step formation frame

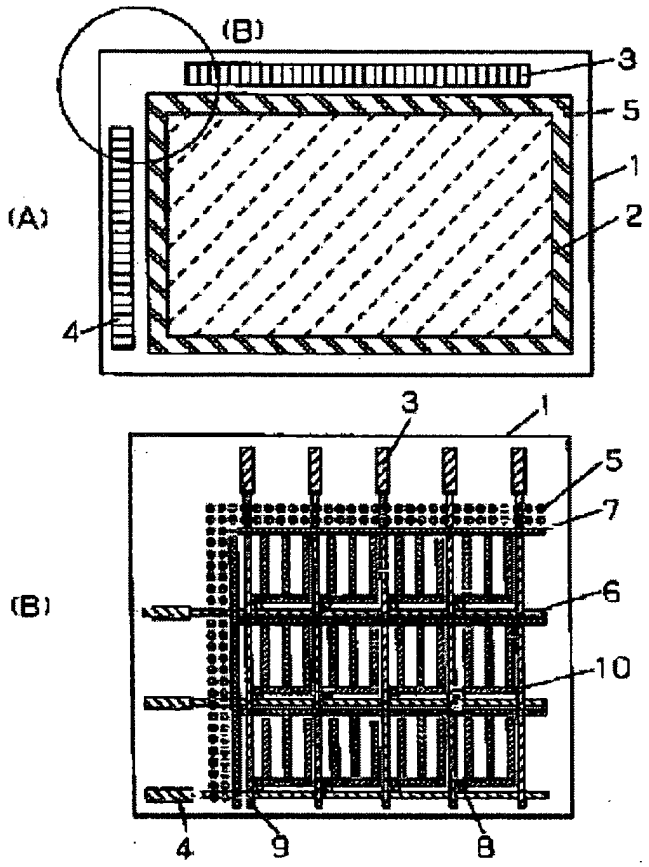


Figure 1

Legend:		
	1	Array substrate
	2	Display region
	3	Pull-out part of the signal line
	4	Pull-out part of the scanning line
	5	Projection step
	6	Scanning electrode

7	Common electrode
8	Switching element
9	Signal electrode
10	Pixel electrode

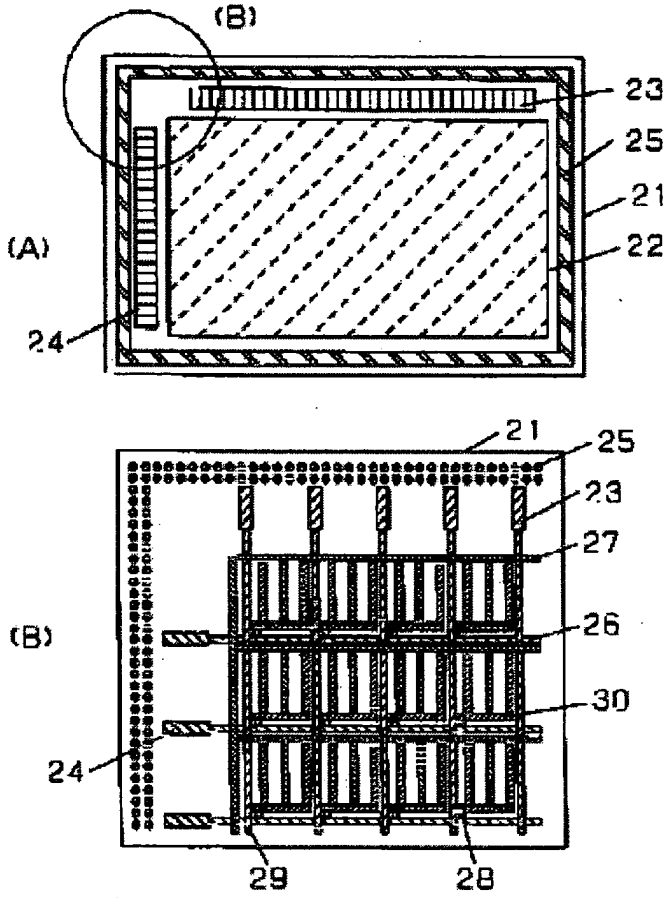


Figure 2

Legend:		
	21	Array substrate
	22	Display region
	23	Pull-out part of the signal line
	24	Pull-out part of the scanning line
	25	Projection step
	26	Scanning electrode
	27	Common electrode
	28	Switching element
	29	Signal electrode
	30	Pixel electrode

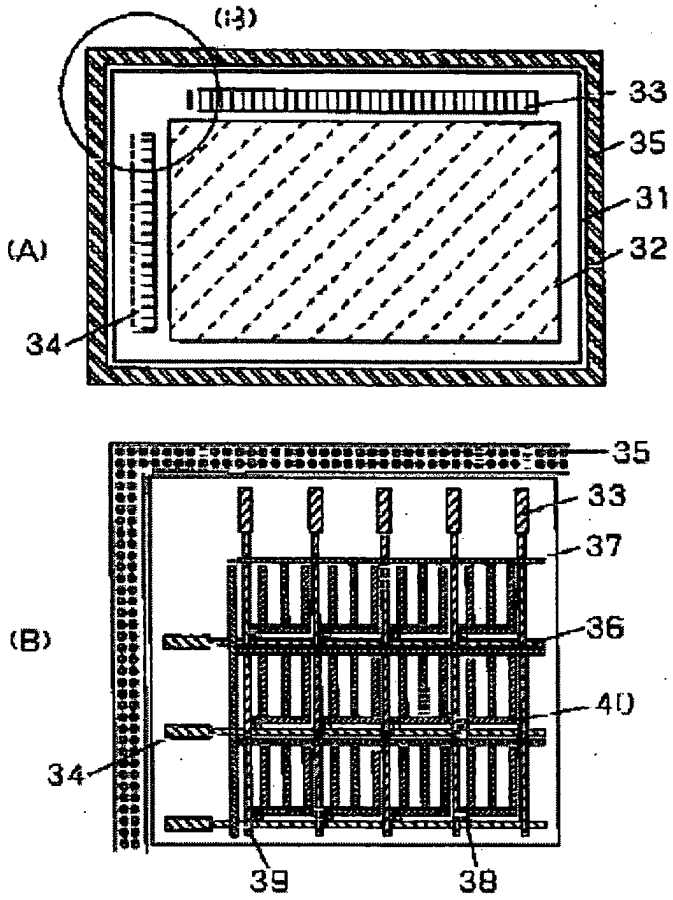


Figure 3

Legend:		
	31	Array substrate
	32	Display region
	33	Pull-out part of the signal line
	34	Pull-out part of the scanning line
	35	Projection step
	36	Scanning electrode
	37	Common electrode
	38	Switching element
	39	Signal electrode
	40	Pixel electrode

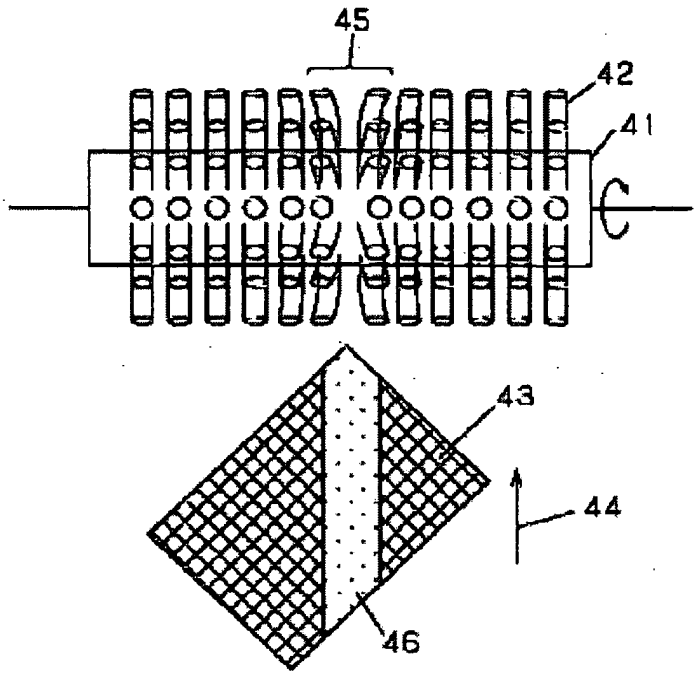


Figure 4

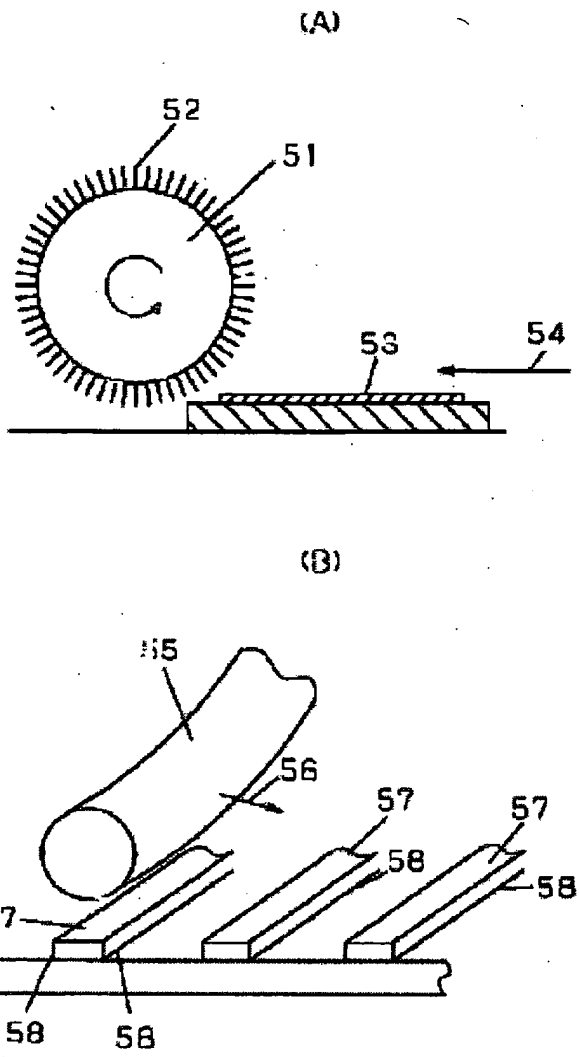


Figure 5

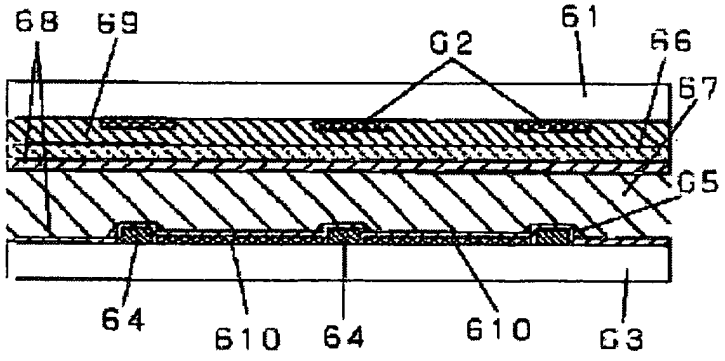


Figure 6

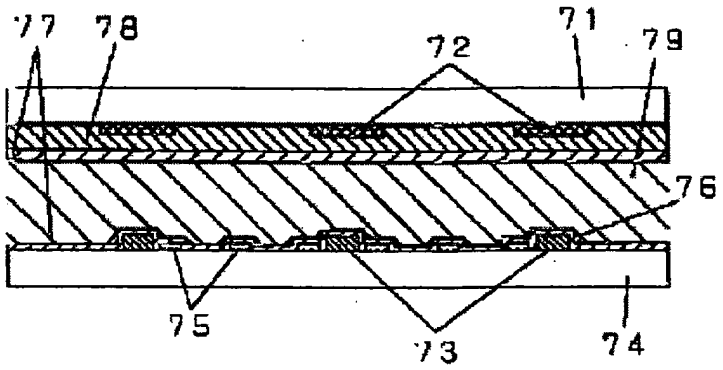


Figure 7

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Kim Vitray
Operations Manager

Subscribed and sworn to before me this 17th day of February, 2009..

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Notary Public, State of Texas
My Commission Expires
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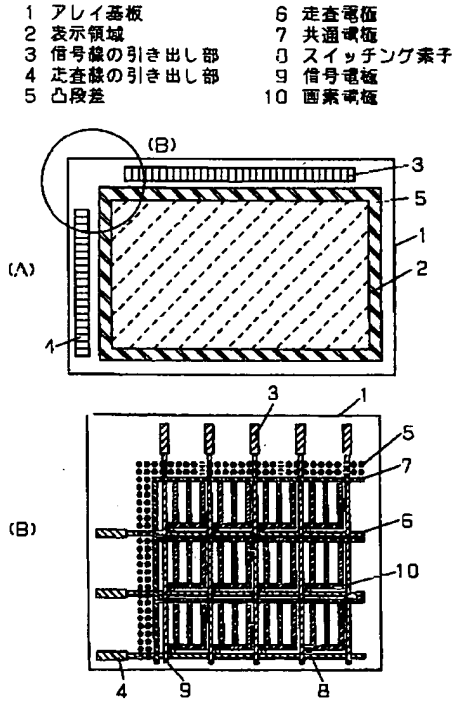
(54)【発明の名称】　アクティブマトリクス型液晶表示素子の製造方法

(57)【要約】

【課題】　櫛形電極基板におけるラビング均一性を向上させ、高品位なアクティブマトリクス型液晶表示素子の製造方法を提供する。

【解決手段】　画素電極１０と共通電極７間に、両基板に対して平行な電界を発生させることにより液晶分子の配列を変化させるアクティブマトリクス型液晶表示素子において、アレイ基板１の表示領域２の外周に櫛形状の電極間隔と同じかあるいはそれ以下の間隔で等間隔の凸段差５を形成し、アレイ基板１上に形成した配向層を樹脂繊維布でラビングすることによって液晶の配向方位を規定してアクティブマトリクス型液晶表示素子を製造する。



【特許請求の範囲】

【請求項１】　マトリクス状に配置された複数の信号配線と走査配線およびその各交差点に対応して設けたスイッチング素子と、前記スイッチング素子に接続された櫛形状の画素電極と、前記画素電極と咬合して形成された櫛形状の共通電極とを有するアレイ基板と、前記アレイ基板に対向して配置された対向基板と、前記アレイ基板と前記対向基板に挟持された液晶層と、前記アレイ基板と対向基板の外部に配置された２枚の偏光板を有し、前記画素電極と前記共通電極間に、前記アレイ基板と対向基板に対して平行な電界を発生させることにより液晶分子の配列を変化させるアクティブマトリクス型液晶表示素子において、前記アレイ基板の表示領域外の外周に前記櫛形状の電極間隔と同じかあるいはそれ以下の間隔で等間隔の凸段差を形成し、前記アレイ基板上に形成した配向層を樹脂繊維布でラビングすることによって液晶の配向方位を規定することを特徴とするアクティブマトリクス型液晶表示素子の製造方法。

【請求項２】　マトリクス状に配置された複数の信号配線と走査配線およびその各交差点に対応して設けたスイッチング素子と、前記スイッチング素子に接続された櫛形状の画素電極と、前記画素電極と咬合して形成された櫛形状の共通電極とを有するアレイ基板と、前記アレイ基板に対向して配置された対向基板と、前記アレイ基板と前記対向基板に挟持された液晶層と、前記アレイ基板と対向基板の外部に配置された２枚の偏光板を有し、前記画素電極と前記共通電極間に、前記アレイ基板と対向基板に対して平行な電界を発生させることにより液晶分子の配列を変化させるアクティブマトリクス型液晶表示素子において、前記アレイ基板の外周に前記櫛形状の電極間隔と同じかあるいはそれ以下の間隔で等間隔の凸段差を形成した枠を配置し、前記アレイ基板をラビングすることを特徴とするアクティブマトリクス型液晶表示素子の製造方法。

【請求項３】　マトリクス状に配置された複数の信号配線と走査配線およびその各交差点に対応して設けたスイッチング素子と、前記スイッチング素子に接続された櫛形状の画素電極と、前記画素電極と咬合して形成された櫛形状の共通電極とを有するアレイ基板と、前記アレイ基板に対向して配置された対向基板と、前記アレイ基板と前記対向基板に挟持された液晶層と、前記アレイ基板と対向基板の外部に配置された２枚の偏光板を有し、前記画素電極と前記共通電極間に、前記アレイ基板と対向基板に対して平行な電界を発生させることにより液晶分子の配列を変化させるアクティブマトリクス型液晶表示素子において、前記櫛形状の電極間隔と同じかあるいはそれ以下の間隔で等間隔の凸段差を形成した基板をラビングした後、前記アレイ基板をラビングすることを特徴とするアクティブマトリクス型液晶表示素子の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はＡＶ機器およびパソコンやワープロ等の平面ディスプレイに使用される液晶表示素子、特に表示特性に視野角依存性の少ない横電界モードのアクティブマトリクス型液晶表示素子の製造方法に関するものである。

【０００２】

【従来の技術】液晶表示素子は、液晶テレビ，パソコン，ワープロ等に応用されており、最近ではＯＡ用ディスプレイやプロジェクションＴＶとしても広く使用され、その表示品位は年々向上している。

【０００３】特にスイッチング素子として薄膜トランジスタ（以下、ＴＦＴという）を用いたアクティブマトリクス型方式のＴｗｉｓｔｅｄ　Ｎｅｍａｔｉｃ液晶表示装置は大容量の表示を行っても高いコントラストが保たれるという大きな特徴を持ち、特に近年市場要望の極めて高い、ラップトップパソコンやノートパソコン、さらには、エンジニアリングワークステーション用の大型，大容量フルカラーディスプレイの中心として開発，商品化が盛んである。

【０００４】このようなアクティブマトリクス方式の液晶表示素子において、広く用いられている液晶表示モードに、Ｔｗｉｓｔｅｄ　Ｎｅｍａｔｉｃ（以下、ＴＮという）方式がある。ＴＮ方式は液晶層を挟持する電極基板間で液晶分子が９０°捻れた構造をとるパネルを２枚の偏光板により挟んだものである。電極基板間に電圧を印加すると液晶分子は捻れ構造をほどきながら電界の向きに配列しようとし、この分子の配列状態により、パネルを透過してくる光の偏光状態が変わり、光の透過率が変調されるからである。しかし、同じ分子配列状態でも、液晶パネルに入射してくる光の入射方向によって透過光の偏光状態は変化するので、入射方向に対応して光の透過率は異なってくる。すなわち、液晶パネルの特性は視角依存性を持つ。この視角特性は主視角方向すなわち液晶層の中間層における液晶分子の長軸方向に対し視点を斜めに傾けると輝度の逆転現象を引き起こす。すなわち、この表示モードの場合、ある電圧の時の表示輝度が、それより低い電圧時の輝度より明るくなる現象をいい、特に黒表示のため高電圧を印加した時の輝度逆転現象は、液晶パネルの画質上、重要な課題となっている。

【０００５】この課題を解決するために、ＴＮ型液晶表示方式のように基板垂直方向に電界を印加するのではなく、液晶に印加する方向を基板に対してほぼ平行な方向とする横電界方式があり、例えば特公昭６３－２１９０７号や特開平６－１６０８７８号により開示されている。一般的な横電界方式の液晶表示素子は、櫛形状の画素電極と共通電極が咬合された電極基板と対向基板に液晶が挟持されたパネルを２枚の偏光板で挟んだ構造である。ここで、画素電極と共通電極間に電圧を印加するこ

とによって、電極間の液晶の分子配列を平面的に変化させ、光の透過率を変調し画像を表示する。この横電界方式では液晶分子の配列変化が電極基板に対して平行に変化することから、光の変調の視野角依存性が少ない。

【０００６】ＴＮ型および横電界型のいずれにおいても、液晶を配向させる手段としては、電極基板上に形成したポリイミド等の配向層表面を樹脂繊維布を用いて擦るラビング法が一般的に行われている。一般的なラビング法は、毛足１～５ｍｍ程度のレーヨンやナイロン布を巻き付けたロールを回転させ、毛先が０．１～０．５ｍｍ程度触れるような状態で基板もしくはロールを移動させ、基板全面を処理する。このラビング法によって、毛先が基板を擦った方向に液晶の配向方位が決まる。

【０００７】基板のラビング時には、基板端面の影響や、実際のアクティブマトリクス型液晶表示素子用のＴＦＴアレイ基板上に形成されている画素電極や外部駆動回路から電気信号を受けるための電極引き出し電極や信号を基板内部に伝えるための信号配線電極のため約０．１～１μｍの凹凸段差の影響により、図４に示すようにラビングロール４１に巻き付けたラビング布４２を回転させ、基板４３を矢印４４の方向にラビング処理を行うと基板端面や段差部が擦られることによって毛先がより分けられ、ラビング布４２の毛に偏在部４５が発生する。

【０００８】また、図５（Ａ）はラビング工程の概略図、図５（Ｂ）はその要部拡大図であり、回転させたラビングロール５１に巻き付けたラビング布５２に電極基板５３を矢印５４の方向に移動させラビング処理を行う。この時の１本の毛５５の直径は１０～３０μｍが一般的であり、毛先が矢印５６の方向へ電極基板５３を擦る時、電極基板５３上に形成された画素電極等の凸部５７の前後には、布が擦れない領域、すなわち、液晶の配向方向が規定できない非配向領域５８ができる。この非配向領域５８は図６に示すような一般的なＴＮモードの液晶表示素子では、対向基板６１に設けた遮光層６２が、アレイ基板６３に形成した電極や配線部の凸部６４によって発生する非配向領域６５が隠れるように貼り合わされるため、非配向領域６５が表示品位に影響しない。ここで、６６は対向共通電極、６７は液晶層、６８は配向層、６９はカラーフィルター層、６１０は画素電極を示している。しかしながら、図７に示すような一般的な横電界型の液晶表示素子では、光透過量をより大きくとるために、対向基板７１に形成する遮光層７２は、配線段差部７３のみを隠すように配置され貼り合わされる。よって、アレイ基板７４を形成した画素電極である櫛形状電極の段差部７５に発生する非配向領域７６は、対向基板７１の遮光層７２に完全には隠れず、非配向領域７６が表示品位に直接影響する。すなわち、部分的な非配向領域７６の大きさの違いが存在すると、表示不良となる。ここで、７７は配向層、７８はカラーフィルター層、７９は液晶層を示している。

【０００９】前記したようにラビング工程においては、ラビング処理を行うことによって基板端面や基板表面の凹凸の影響でラビング布の偏在が発生し、この状態で、横電界モードの液晶表示素子のラビング時には、ラビング布の偏在部と通常部で非配向領域の大きさが異なり、ロールまたは基板の進行方向に影響を与えるために、図４に示すように、表示領域上にスジ状のムラ４６が発生する。このようなムラ４６は、ラビング処理枚数が増えるに従い、布の偏在も顕著になるため、スジムラの発生状況が悪化していく。

【００１０】このスジ状のムラに対しては、非配向領域の低減、すなわち、段差部低減が考えられ、その手段として櫛形状電極上に平坦層を形成する方法が考えられるが、工程の増加によるコスト上昇や歩留まりの低下、また、平坦層により液晶に印加される実効的電圧の現象が起こる。また、上記ラビング法に代わる配向方法として酸化珪素の斜方蒸着やラングミュア・プロジェット膜や化学吸着法による配向膜形成が試みられているが量産性の点でラビング法に大きく劣る。

【００１１】

【発明が解決しようとする課題】本発明では基板に櫛形状電極を有する横電界モードにおいて量産性に優れるラビング法において、前記する従来例に見られる表示ムラのない高品位な表示素子を得ることを目的にするものである。

【００１２】

【課題を解決するための手段】本発明は前記する目的のために、マトリクス状に配置された複数の信号配線と走査配線およびその各交差点に対応して設けたスイッチング素子と、前記スイッチング素子に接続された櫛形状の画素電極と、前記画素電極と咬合して形成された櫛形状の共通電極とを有するアレイ基板と、前記アレイ基板に対向して配置された対向基板と、前記アレイ基板と前記対向基板に挟持された液晶層と、前記アレイ基板と対向基板の外部に配置された２枚の偏光板を有し、前記画素電極と前記共通電極間に、前記アレイ基板と対向基板に対して平行な電界を発生させることにより液晶分子の配列を変化させるアクティブマトリクス型液晶表示素子の製造方法において、前記アレイ基板の表示領域外の外周に前記櫛形状の電極間隔と同じかあるいはそれ以下の間隔で等間隔の凸段差を形成し、前記アレイ基板上に形成した配向層を樹脂繊維布でラビングすることによって液晶の配向方位を規定する製造方法としたものである。

【００１３】また、凸段差は、櫛形状の電極間隔と同じかあるいはそれ以下の間隔で等間隔の凸段差を形成した枠をアレイ基板の外周に配置して形成し、ラビングすることにより本発明の目的を達成するものである。

【００１４】また、櫛形状の電極間隔と同じかあるいはそれ以下の間隔で等間隔の凸段差を形成した基板をラビ

ングした後、アレイ基板をラビングして本発明の目的を達成するものである。

【００１５】

【発明の実施の形態】本発明は各請求項記載の形態で実施できるものであり、請求項１記載のように、マトリクス状に配置された複数の信号配線と走査配線およびその各交差点に対応して設けたスイッチング素子と、前記スイッチング素子に接続された櫛形状の画素電極と、前記画素電極と咬合して形成された櫛形状の共通電極とを有するアレイ基板と、前記アレイ基板に対向して配置された対向基板と、前記アレイ基板と前記対向基板に挟持された液晶層と、前記アレイ基板と対向基板の外部に配置された２枚の偏光板を有し、前記画素電極と前記共通電極間に、前記アレイ基板と対向基板に対して平行な電界を発生させることにより液晶分子の配列を変化させるアクティブマトリクス型液晶表示素子において、前記アレイ基板の表示領域外の外周に前記櫛形状の電極間隔と同じかあるいはそれ以下の間隔で等間隔の凸段差を形成し、アレイ基板をラビング処理することによって液晶の配向方位を規定するものである。

【００１６】また、請求項２記載のように、櫛形状電極を形成したアレイ基板の外周に櫛形状の電極間隔と同じかあるいはそれ以下の間隔で等間隔の凸段差を形成した枠を配置し、ラビングすることによって液晶の配向方位を規定するものである。

【００１７】また、請求項３記載のように、櫛形状電極を形成したアレイ基板の櫛形状の電極間隔と同じかあるいはそれ以下の間隔で等間隔の凸段差を形成した基板をラビングし、その後、櫛形状電極を形成したアレイ基板をラビングすることによって液晶の配向方位を規定するものである。

【００１８】

【実施例】以下、本発明に係わる具体的な実施例について、図面を参照しながら詳細に説明する。

【００１９】（実施例１）図１（Ａ）は本発明の実施例１における液晶表示素子の製造方法に用いた横電界モードのＴＦＴアレイ基板の概略正面図、図１（Ｂ）は図１（Ａ）における（Ｂ）部分の拡大図である。

【００２０】アレイ基板１上には、マトリクス状にスイッチング素子と画素電極を配置した表示領域２、その信号線の引き出し部３、走査線の引き出し部４が形成されている表示領域の周囲には等ピッチの凸段差５が形成されている。図１（Ｂ）はアレイ基板１の表示領域内外の境界部の拡大図である。アレイ基板１上に走査電極６をクロムを用いて図のような形状にパターン形成した。それと同時に共通電極７を画素長辺方向に沿って図のような形状に形成した。なお、共通電極７の幅は５μｍであり、材料はクロムに限定せず、アルミニウム、アルミニウムを主成分とする金属等、導電性単層膜または多層膜を用いても良い。ＴＦＴのゲート絶縁膜として窒化シリコン（SiN_x）をその上に積層させる。次に、ＴＦＴのスイッチ機能を司るスイッチング素子８をプラズマＣＶＤ法によってアモルファスシリコン（α－Ｓｉ）を積層させ、再び、窒化シリコン（SiN_x）の絶縁層形成、パターン化した。その後スパッタリング法によって堆積させたチタン／アルミニウム（Ｔｉ／Ａｌ）の二層を堆積させ、その後ドライエッチングによってスイッチング素子と共に、信号電極９および画素電極１０をパターン形成した。なお、画素電極１０の幅は５μｍであり、材料はチタン／アルミニウム（Ｔｉ／Ａｌ）に限定せず、導電性金属の単層膜または多層膜を用いても良い。そしてこの時、共通電極７と画素電極１０との間隔は１０μｍとした。基板面から３０００Åの凸構造とした。そして、前記絶縁膜形成時に表示領域外において直径５μｍで３０００Åの段差の円形の凸段差５を５μｍの間隔で形成した。なお、凸段差５の材料は、絶縁材料に限定せず導電性金属の単層膜または多層膜を用いても良い。

【００２１】このように完成した薄膜トランジスタアレイ基板と遮光帯を形成した対向カラーフィルター基板に、ポリイミド膜をフレキソ印刷し、乾燥硬化し配向層とし、ラビング処理を行った。ラビング処理は、１本の繊維径が２０μｍで２００００本／ｃｍ^2 の密度のレーヨン布を直径１００ｍｍのロールに巻き付け、ロールを８００ｒｐｍにて回転させ、そして、毛足が基板に０．２ｍｍ押し込まれた状態で、前記アレイ基板と対向基板を所定の方向に処理を行った。ここで、櫛形状電極を形成したアレイ基板１において、ラビング布が表示領域２をラビング処理する前に、表示領域外に形成した等ピッチの凸段差を擦ることによって、ラビング布の偏りが矯正されるため、表示領域の櫛形電極段差部に発生する非配向領域を均一にすることができる。ラビング処理後のアレイ基板１と対向基板を貼り合わせ、液晶を真空注入法にて注入し、液晶表示素子を作製した結果、スジ状のムラは発生しなかった。また、１本のロールに対して２０００枚のラビング処理を行い液晶表示素子を作製したが、表示品位の劣化は見られなかった。

【００２２】なお、本実施例では表示領域に隣接する領域に凸段差を形成したが、図２に示すように凸段差を基板周辺部に形成した場合でも同様な構成のアレイを作製し、同様な方法で横電界型液晶表示素子を作製した結果、凸段差の効果により、ラビング布の偏在が矯正され、ラビングスジの発生は見られなかった。ここで、２１は横電界型のアレイ基板、２２は表示領域、２３は信号線の引き出し部、２４は走査線の引き出し部、２５は凸段差、２６は走査電極、２７は共通電極、２８はスイッチング素子、２９は信号電極、３０は画素電極を示している。

【００２３】また、本実施例では凸段差２５の形状を円形としたが、櫛形状電極と同じかあるいはそれ以下の間

隔で等ピッチであれば段差によるラビング布の矯正効果に変化は見られず、段差の大きさについても、アレイ基板２１の段差と同程度以上であれば同等な結果が得られた。

【００２４】（比較例）前記した、実施例１と同様な方法および電極構成で、基板周辺部に等間隔の凸段差を形成しない場合の、従来からの横電界ＴＦＴアレイ基板を作製し、ラビング処理を行い液晶表示素子を作製した。この結果、ラビング時の基板の進行方向に薄いスジ状のムラが見られた。そして、１本のラビングローラーにおいて１００枚のラビング処理を行うとスジが明確化し、ラビング回数を重ねる度に徐々にスジの発生が顕著になった。

【００２５】（実施例２）図３（Ａ）は本発明の実施例２における液晶表示素子に用いた横電界モードのＴＦＴアレイ基板の概略図、図３（Ｂ）は図３（Ａ）の拡大図である。

【００２６】前記比較例で作製した従来の横電界型液晶表示アレイ基板３１（従来の横電界型の構成）において、ラビング装置の定盤の外周に直径５μｍで１μｍの段差の円形の凸段差を形成した枠を配置し、ラビング処理を行った。ラビング布が基板周辺に配置した等間隔の定盤上に形成した凸段差を擦ることによってラビング布の偏在が矯正され均一なラビング処理が行え、ラビングスジの発生は見られなかった。ここで、３１は従来の横電界型のアレイ基板、３２は表示領域、３３は信号線の引き出し部、３４は走査線の引き出し部、３５は凸段差形成枠、３６は走査電極、３７は共通電極、３８はスイッチング素子、３９は信号電極、４０は画素電極を示している。

【００２７】また、本実施例では凸段差の形状を円形としたが、櫛形状電極と同じかあるいはそれ以下の間隔で等ピッチであれば段差によるラビング布の矯正効果に変化は見られず、段差の大きさについても、アレイ基板の段差と同程度以上であれば同等な結果が得られた。

【００２８】（実施例３）ガラス基板上に３０００ÅのＳｉN_xの膜を形成し、フォトリソグラフィ法によって、幅５μｍで５μｍピッチで３０００Åの段差の凹凸ストライプパターンを形成した基板を作製し、これを従来の横電界櫛型のアレイ基板をラビング処理する前にラビングすることによって、アレイ基板のパターンによって偏在するラビングスジの発生はなかった。

【００２９】なお、本実施例では等ピッチの凹凸パターンを、ストライプパターンとしたが、櫛形状電極と同じかあるいはそれ以下の間隔で等ピッチであれば段差のパターンによるラビング布の矯正効果に変化は見られず、段差の大きさについても、アレイ基板の段差と同程度以上であれば同等な結果が得られた。

【００３０】

【発明の効果】以上説明したように本発明において、下記に記載するような液晶表示装置としての効果が得られる。

【００３１】請求項１記載の発明によれば、基板の表示領域外の外周に形成した等間隔の凸段差が、ラビング時に発生するラビング布の偏在を矯正するために、表示領域が均一にラビングされ、高品位の液晶表示素子を製造することができる。

【００３２】また、請求項２記載の発明によれば、ラビング時の基板周辺に等ピッチの段差を形成した枠を配置することによって、ラビング時に発生するラビング布の偏在が矯正され、表示領域が均一にラビングされ、高品位の液晶表示素子を製造することができる。

【００３３】また、請求項３記載の発明によれば、等ピッチの段差ダミー基板をラビングした後に生産品である基板をラビングする。これによって、ラビング布の偏在が矯正され、表示領域が均一にラビングされ、高品位の液晶表示素子を製造することができる。

【００３４】本発明は、液晶表示パネルを製作する上で非常に利点の多い工法であり、かつ表示性能の高い液晶表示装置を製作することができる。

【図面の簡単な説明】

【図１】（Ａ）本発明の実施例１に係わる液晶表示素子の概略平面図

（Ｂ）（Ａ）中に丸で示した部分の拡大図

【図２】（Ａ）本発明の実施例１に係わる他の液晶表示素子の概略平面図

（Ｂ）（Ａ）中に丸で示した部分の拡大図

【図３】（Ａ）本発明の実施例２に係わる液晶表示素子の概略平面図

（Ｂ）（Ａ）中に丸で示した部分の拡大図

【図４】ラビング布の偏在の概念説明図

【図５】ラビング工程の概念説明図

【図６】ＴＮモードのパネルの概略断面図

【図７】櫛形電極による横電界モードの概略断面図

【符号の説明】

１，２１，３１　アレイ基板

２，２２，３２　表示領域

３，２３，３３　信号線の引き出し部

４，２４，３４　走査線の引き出し部

５，２５　凸段差

６，２６，３６　走査電極

７，２７，３７　共通電極

８，２８，３８　スイッチング素子

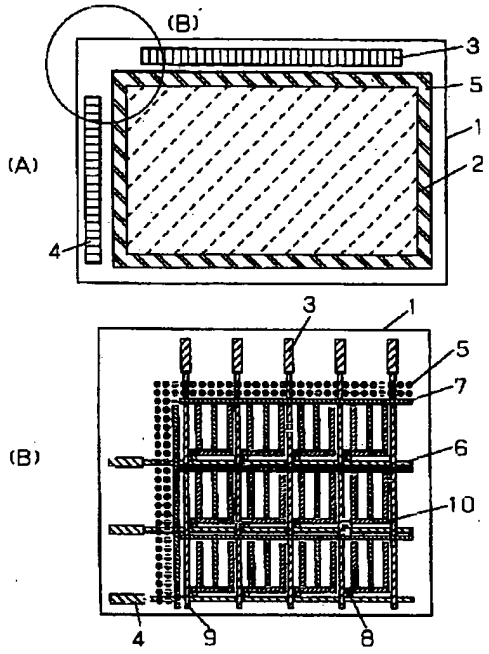
９，２９，３９　信号電極

１０，３０，４０　画素電極

３５　凸段差形成枠

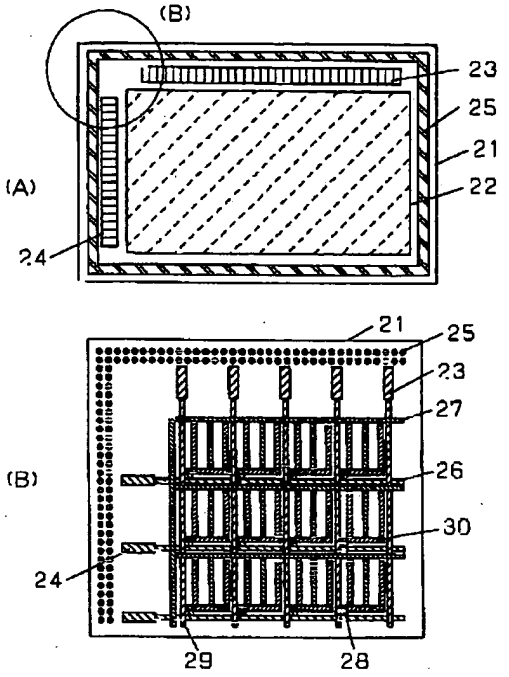
【図1】

1 アレイ基板
2 表示領域
3 信号線の引き出し部
4 走査線の引き出し部
5 凸段差
6 走査電極
7 共通電極
8 スイッチング素子
9 信号電極
10 画素電極

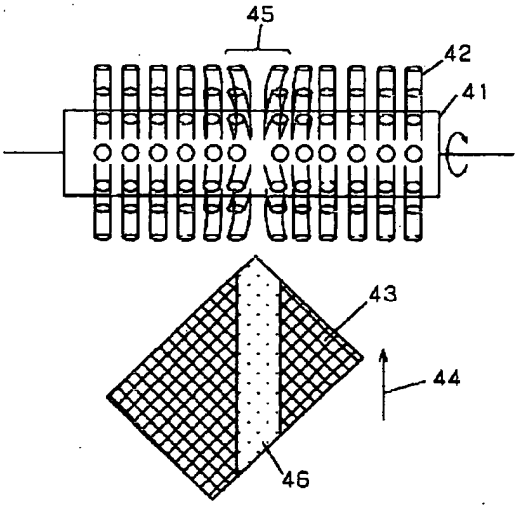


【図2】

21 アレイ基板
22 表示領域
23 信号線の引き出し部
24 走査線の引き出し部
25 凸段差
26 走査電極
27 共通電極
28 スイッチング素子
29 信号電極
30 画素電極



【図4】



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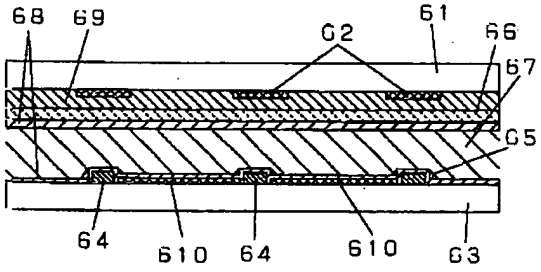
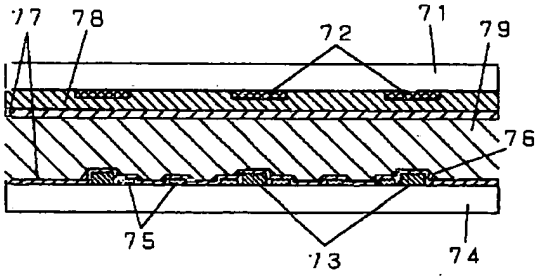
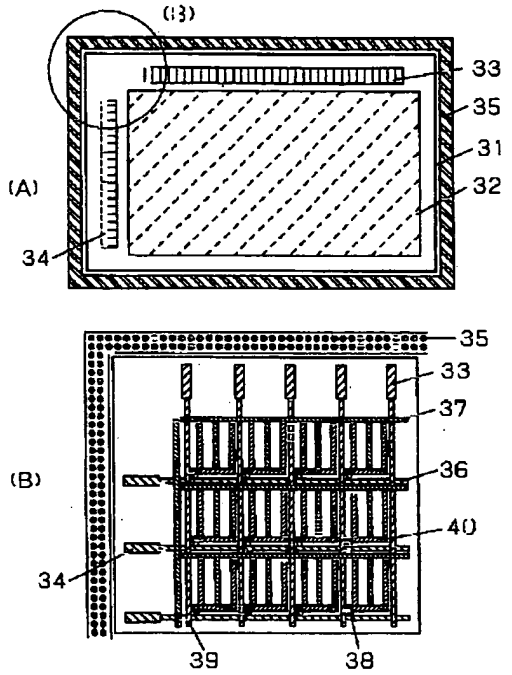


【図7】

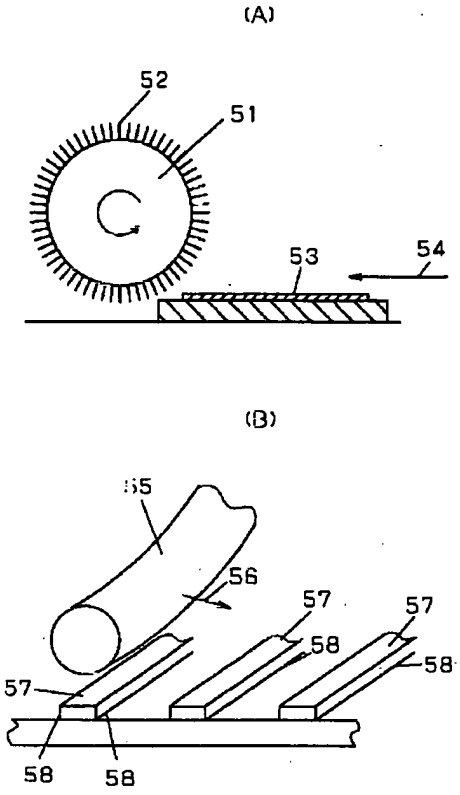


【図3】

31 アレイ基板
32 表示領域
33 信号線の引き出し部
34 走査線の引き出し部
35 凸段差形成枠
36 走査電極
37 共通電極
38 スイッチング素子
39 信号電極
40 画素電極



【図5】



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COLOR FILTER AND LIQUID CRYSTAL DISPLAY DEVICE USING SAME

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[There are no amendments to this patent.]

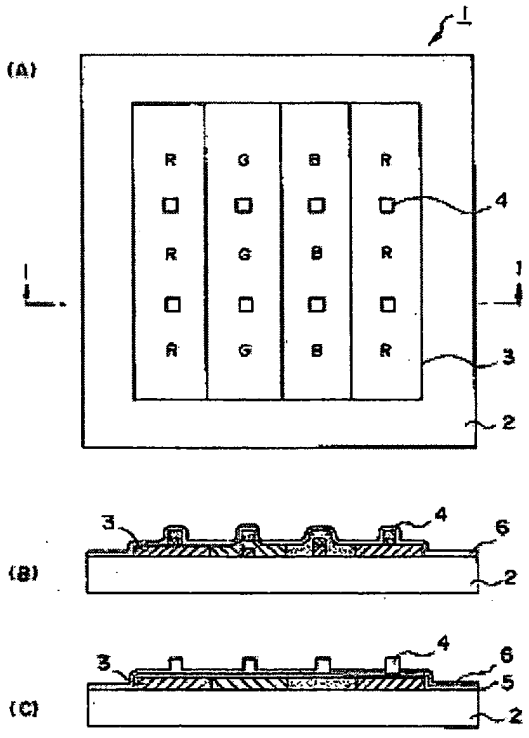
Abstract

Purpose

To provide a color filter for liquid crystals which has columnar members that function to control the gap between the color filter and the opposing substrate, and a liquid crystal display device using said color filter.

Constitution

A color filter for liquid crystals characterized by the following facts: it has columnar members that function to control the gap between the color filter and the opposing substrate, and the columnar members are formed from a photosensitive material mainly consisting of any of polyimide resin, polyvinyl alcohol resin, and acrylic resin. The columnar members can be prepared by forming a transparent photosensitive material on the colored layer, or they can be formed by laminating colored layers. A liquid crystal display device can be obtained by placing the color filter prepared as described and the opposing substrate in contact with each other with the columnar members on the inner side, and then filling the gap with liquid crystal.



Claims

1. A color filter for liquid crystals characterized by the following fact: it has plural columnar members that function to control the gap between the color filter and the opposing substrate, and the columnar members are formed from a photosensitive material mainly consisting of any of polyimide resin, polyvinyl alcohol resin and acrylic resin.

2. A color filter for liquid crystals characterized by the following fact: it has columnar members that function to control the gap between the color filter and the opposing substrate, and each columnar member has a bottom cross-sectional area of 200 μm^2 or larger.

3. A color filter for liquid crystals characterized by the following fact: it has columnar members having function to control the gap between the color filter and the opposing substrate, and each columnar member experiences an amount of plastic deformation under a load of 5 mN of 0.05 μm or less.

4. A color filter for liquid crystals characterized by the following fact: it has columnar members having a function to control the gap between the color filter and the opposing substrate, and said columnar members have a transparent electroconductive film on them, and each columnar member experiences an amount of plastic deformation under a load of 5 mN of 0.12 μm or less.

5. The color filter for liquid crystals described in any of Claims 1-4, characterized by the fact that the columnar members are prepared by forming a transparent photosensitive material on the colored layer of the color filter or the black matrix layer.

6. The color filter for liquid crystals described in any of Claims 1-4, characterized by the fact that the columnar members are formed by laminating colored layers of the color filter.

7. The color filter for liquid crystals described in any of Claims 1-6, characterized by the fact that the top portion of each columnar member is flat.

8. The color filter for liquid crystals described in any of Claims 1-7, characterized by the fact that the columnar members are formed only at positions corresponding to a prescribed colored layer.

9. The color filter for liquid crystals described in any of Claims 1-8, characterized by the fact that the height of the columnar members is 1-8 μm above the surface of the colored layer.

10. The color filter for liquid crystals described in any of Claims 1-9, characterized by the fact that the columnar members are arranged on the black matrix.

11. The color filter for liquid crystals described in any of Claims 1-10, characterized by the fact that the columnar members are arranged in a regular array.

12. A liquid crystal display device characterized by the following facts: it has a color filter which has columnar members having a function to control the gap between the color filter and the opposing substrate; the columnar members are formed from a material mainly consisting

of any of polyimide resin, polyvinyl alcohol resin, and acrylic resin; and the gap formed by placing said color filter and the opposing substrate in contact with each other, with the columnar members on the inner side, is filled with liquid crystal.

13. A liquid crystal display device characterized by the following facts: it has a color filter which has columnar members having a function to control the gap between the color filter and the opposing substrate; the columnar members are formed by laminating the colored layers formed of a material mainly consisting of any of polyimide resin, polyvinyl alcohol resin, and acrylic resin; and the gap formed by placing said color filter and the opposing substrate in contact with each other, with the columnar members on the inner side, is filled with liquid crystal.

14. The liquid crystal display device described in Claim 12 or 13, characterized by the fact that the columnar members having function to control the gap between the color filter and the opposing substrate are also formed in the sealing material coating portion around the circumference of the substrate.

Detailed explanation of the invention

[0001]

Technical field of the invention

The present invention pertains to a liquid crystal display device typically used in personal computers. In particular, the present invention pertains to a color filter characterized by the fact that it has plural minute columnar members that function to control the gap between the color filter and the opposing substrate, and the columnar members are optimized by selecting a prescribed material, shape and strength. Also, the present invention pertains to the liquid crystal display device made using said color filter.

[0002]

Prior art

In a conventional liquid crystal display device, spacers are provided in order to maintain the spacing between the two facing substrates between them, so that the thickness of the liquid crystal layer is kept uniform in the plane. The spacers are usually made of granular gap control material consisting of ball-shaped grains of a plastic or silica. The diameter of the grains used as spacers is in the range of 1.5-8.0 μm, depending on the specific application and thickness of the liquid crystal. The spacers are scattered on one substrate, with the outer peripheral portion being sealed with a sealing material. In said scattering operation, however the placement position is not specified, and the spacers can be positioned at a display pixel portion, and several of them can be lumped together or aggregated. Also, when a voltage is applied or when the cell is transported,

the spacers can move and damage the orienting film. Consequently, in order to specify the setting position and to prevent movement of the spacers, a type of color filter has been proposed with a gap function characterized by the fact that the colored layer of the color filter is formed by laminating three layers, and the obtained three-layer structural portions are used in lieu of spacers (Japanese Kokai Patent Application No. Hei 5[1993]-196946). However, although said patent application disclosed the formation of the three-layer structural body in a black matrix portion, it did not disclose a scheme that can fully meet the requirements of the spacer function. That is, as the black matrix is made finer with the progress in adopting a high numerical aperture, because the three-layer structural member is formed on the black matrix, its size has to be miniaturized. Also, in order to ensure no effect on the pixel display by its quantity even when it is not formed on the black matrix, the quantity should be minimized. That is, it is essential to ensure that the three-layer structural member have a minute size, be few in number, and yet have a high strength.

[0003]

Problems to solve by the invention

The purpose of the present invention is to solve the aforementioned problems of the prior art by providing a color filter and a liquid crystal display device using it, characterized by the fact that by defining the material, size and strength of the columnar members used in lieu of spacers, they can be made sufficiently small to have no effect on the display, and a small number of the columnar members can serve in place of the spacers.

[0004]

Means to solve the problems

In order to solve the aforementioned problem, the first scheme of the present invention provides a color filter for liquid crystals characterized by the following facts: it has plural columnar members having a function to control the gap between the color filter and the opposing substrate, and the columnar members are formed from a photosensitive material mainly consisting of any of polyimide resin, polyvinyl alcohol resin and acrylic resin. For the color filter for liquid crystals made of said material, it is possible to perform highly accurate gap control as the strength of the columnar members is sufficiently high.

[0005]

The second scheme of the present invention provides a color filter for liquid crystals characterized by the following facts: it has columnar members having a function to control the gap between the color filter and the opposing substrate, and each columnar member has a bottom

cross-sectional area of 200 μm^2 or larger. With this color filter for liquid crystal, it is possible to perform highly accurate gap control because the strength of the columnar members is sufficiently high.

[0006]

The third scheme of the present invention provides a color filter for liquid crystals characterized by the following facts: it has columnar members having function to control the gap between the color filter and the opposing substrate, and each columnar member experiences an amount of plastic deformation under a load of 5 mN of 0.05 μm or less. With this color filter for liquid crystal, it is possible to perform highly accurate gap control because the strength of the columnar members is sufficiently high.

[0007]

The fourth scheme of the present invention provides a color filter for liquid crystals characterized by the following facts: it has columnar members having function to control the gap between the color filter and the opposing substrate, and said columnar members have a transparent electroconductive film on them, and each columnar member experiences amount of plastic deformation under a load of 5 mN of 0.12 μm or less. With this color filter for liquid crystal, it is possible to perform highly accurate gap control because the strength of the columnar members is sufficiently high.

[0008]

According to the first scheme of the liquid crystal display device of the present invention, it has a color filter, which has columnar members having function to control the gap between the color filter and the opposing substrate; the columnar members are formed from a material mainly consisting of any of polyimide resin, polyvinyl alcohol resin, and acrylic resin; and the gap formed by placing said color filter and the opposing substrate in contact with each other, with the columnar members on the inner side, is filled with liquid crystal. Consequently, it is possible to obtain a liquid crystal display device with high gap accuracy.

[0009]

According to the second scheme of the liquid crystal display device of the present invention, it has a color filter which has columnar members having a function to control the gap between the color filter and the opposing substrate; the columnar members are formed by laminating the colored layers formed of a material mainly consisting of any of polyimide resin, polyvinyl alcohol resin, and acrylic resin; and the gap formed by placing said color filter and the

opposing substrate in contact with each other, with the columnar members on the inner side, is filled with liquid crystal. As a result, it is possible to obtain a liquid crystal display device with high gap accuracy.

[0010]

Embodiment of the invention

In the following, an embodiment of the present invention will be explained. Figure 1 includes schematic diagrams illustrating the constitution of an example of the color filter for liquid crystals in the present invention. Figure 1(A) is a plan view, and Figure 1(B) is a cross section taken across [line] I-I in Figure 1(A). As shown in Figure 1, color filter (1) for liquid crystals is formed on transparent substrate (2), and the basic structure comprises color filter layers (3) (R, G, B) made of colored layers and columnar members (4). Here, columnar members (4) can be formed by laminating the various colored layers of R, G, B as shown in Figure 1(B), or they can be formed by forming columnar members (4) independently after the formation of the colored layers of R, G, B as shown in Figure 1(C). When they are formed on the colored layers as shown in Figure 1(C), it is preferred that they be made of transparent material so that they do not affect the colored layers. In this case, the transparent material can also play the role of overcoat layer (6).

[0011]

The columnar members can be provided in each of the colored layers as shown in Figure 1, or, if there is no problem with regard to strength, they can also be arranged only on the prescribed colored layer, or they can be arranged with a certain spacing between them. In Figure 1(A), columnar members (4) are shown as having a square cross section. However, this square shape is not the only option, and other cross-sectional shapes, such as round, elliptical, rectangular, etc., can also be adopted. In addition, the columnar members can also be formed on the glass surface other than the non-display portion. It is preferred that the columnar members be formed on the non-display portions, and it is especially preferred that the same columnar members be formed in the sealing material coating portion around the substrate. In the prior art, spacers are blended in the sealing material to ensure a constant spacing between the substrates. Now the columnar members can replace them. For the non-display portions, it is not required that the cross-sectional area of the bottom of the columnar member be made especially minute.

[0012]

On the surface of color filter (1), there are colored layer (3) and transparent electroconductive film layer (ITO) (5). In the case shown in Figure 1(B), it is possible to set said

transparent electroconductive film layer (5) below columnar members (4), and this is beneficial in preventing contact with the opposing substrate. Also, when the color filter of the present invention is adopted in the IPS (In-Plane-Switching) system, transparent electroconductive film layer (5) (ITO) is not needed. Also, as needed, there can be a black matrix layer and an overcoat layer. When the black matrix layer is formed, taking into consideration effective use of the pixel display part, it is preferred that columnar members (4) be formed based on the presence of a black matrix.

[0013]

Also, when an overcoat layer is formed, the overcoat layer can be made of either organic material or inorganic material. When the overcoat layer is made of an organic material, by having photosensitivity of the overcoat material in addition to the function of a conventional protective film, it is possible to form both columnar members (4) and the overcoat layer simultaneously. In this case, for example, the operation can be performed by means of double exposure as a combination of full-surface flash exposure and pattern exposure of only the portion of the columnar members. Also, columnar members (4) can be formed after the formation of transparent electroconductive film layer (5). On the other hand, when the overcoat layer is made of an inorganic material (SiO_2 or the like), it is possible to select a thin film for the overcoat layer. Consequently, when columnar members (4) are formed by laminating the colored layers, it is possible to protect colored layer (3) and columnar members (4) without decreasing amount of colored layer (3) in the gap.

[0014]

When the black matrix is made of a resin-based black matrix, and columnar members (4) are formed on said black matrix, the film thickness of the black matrix layer itself is usually within the range of 1.0-2.0 μm, and the columnar members are formed on it. Consequently, this scheme is effective when one seeks a larger gap amount between columnar members (4) and colored layer (3) and a larger height of the columnar members.

[0015]

When they are formed on the black matrix, and there is a switching function on the side of the opposing substrate, such as in the TFT or IPS system, it is preferred that columnar members (4) be formed at positions avoiding TFTs on the opposing substrate. In addition, when a resin black matrix is formed on TFTs, it is preferred that columnar members (4) be placed on the color filter side so that they correspond to the position of said resin black matrix. However, even when the columnar members are formed at positions avoiding TFTs on the opposing

substrate, TFTs and columnar members (4) still can contact each other due to position shift in the formation of columnar members (4) or position shift in the lamination operation. As a result, TFTs can be damaged.

[0016]

When a resin black matrix is formed on TFTs, and columnar members (4) are set on the color filter side to correspond to the position of the black matrix, if the number of columnar members (4) in the plane is small, the load applied on TFTs rises, so that TFTs can be damaged. When a TFT is damaged, in the normally white mode (a TN liquid crystal is in the 90° twisted state without the application of voltage) often adopted in the conventional TFT system, light can fully pass through the damaged portion whether a voltage is applied to it or not. This corresponds to the monochromatic transmitted light of the color filter. Usually, the visibility rate of transmitted light (Y value), for green is greater than that for red and blue, and the green light is transmitted the most. For example, assume that the damaged TFT corresponds to the green (G) colored portion, because green has a large Y-value, the green color becomes brighter than the other colors. Consequently, it is preferred that columnar members (4) be formed in red (R) or blue (B) portions, avoiding the green portions.

[0017]

It is preferred that the height of columnar members (4) be in the range of 1-8 μm from the surface of the colored layer. If the height is less than 1 μm, it takes a long time to inject the liquid crystal, and the processing time becomes a restrictive factor. On the other hand, as the gap is increased, the response rate falls, and when columns of 8 μm or larger are formed, homogeneity in the coating surface cannot be fully realized even though the columnar members are made of a transparent resin. As a result, it is difficult to realize good in-plane homogeneity in formation of the columnar members by means of 3-color superposition. In addition, when it is too high, the operation of rubbing for the orienting film can cause rubbing portion shadow to develop, and this is undesirable. Usually it is preferred that the height be about 4-6 μm. In the case of a TFT system, experience with spacer scattering in the prior art indicates that an accuracy of about ±0.3 μm is needed. Also, it is preferred that said columnar members (4) be arranged regularly. This can facilitate distinguishing defective protrusions when the color filter is manufactured. Another reason is that when the columnar members are formed equidistantly, force on the opposing substrate surface can be distributed. In addition, it is preferred that the outermost surface of columnar members (4) be flat. If it is flat, by comparison with the point contact for spacer beads in the prior art, planar contact with the opposing substrate takes place, so that the stress can be dispersed.

[0018]

When columnar members (4) are formed by laminating colored layers, and then an overcoat layer is formed from an organic material with only the surface flatness of the colored layers improved, one can adopt the following scheme: the overcoat layer is not formed on the columnar members as it is formed by pattern exposure and development using a pattern with voids corresponding to columnar members (4), so that columnar members (4) alone are exposed. When the opposing substrate has an insulating layer corresponding to columnar members (4), a transparent electroconductive film layer can be formed on columnar members (4), so that contact with the opposing substrate can be prevented.

[0019]

According to the present invention, said color filter layer (3) (R, G, B) and columnar members (4) are formed in a conventional photolithographic operation. That is, on a transparent substrate or a substrate having a black matrix formed on it, spin coating, roll coating or another means is adopted to form a film of the colored photosensitive material with a prescribed film thickness, followed by exposure, development, and processing. The same operation is repeated for R, G, B. Also, as needed, a photosensitive positive type resist is coated on the colored photosensitive material, followed by exposure and development to form a pattern at the necessary portions, and this operation is repeated for R, G, B, forming portions that become the prescribed colored pixels and portions that become the columnar members. When a photosensitive positive resist is used, the portions that become the columnar members can have the photosensitive positive resist left as is without removal by peeling after etching, and the columnar members are then formed together with the colored layer. In this case, the columnar member has a two-layer structure comprising the colored layer and the positive resist layer. This is advantageous in forming the columnar members. The operation for forming the R, G, B colored layers can also be performed as follows: the conventional colored layer (3) alone is formed, and the overcoat layer is selected to have photosensitivity, so that the columnar members are formed only by the overcoat layer, as shown in Figure 1(C). Also, as described above, the overcoat layer can be formed only on the non-columnar portions other than the columnar members, so that flatness of the colored pixel portion can also be improved.

[0020]

Application examples

Examples for test manufacture of color filters

In order to determine the appropriate material, size and strength for the columnar members in order to control the gap, various types of trial products (Tests 1-5) were manufactured and tested for comparative analysis.

Test 1

In this test, the purpose is to check the strength of the material composing the columnar members. Three types of resins, namely, acrylic resin, polyvinyl alcohol resin, and polyimide resin, were used as the feed materials for forming the colored layers that form the columnar members. Among these, acrylic resin and polyvinyl alcohol resin are photosensitive colored materials, while polyimide resin is not photosensitive.

Test 2

In this test, the purpose is to measure the amount of plastic deformation caused by differences in the bottom cross-sectional area of the columnar members. In this test, acrylic resin colored photosensitive material was used to manufacture color filters having columnar members of various sizes and bottom cross-sectional areas. The columnar members were formed by laminating the colored photosensitive materials. In addition, samples were test manufactured by forming ITO film on the surface. The size and cross-sectional area of the columnar members were adjusted by adjusting the pattern size of the photomask in the formation of the columnar members.

Test 3

The purpose of this test is to measure the amount of plastic deformation due to differences in the bottom cross-sectional area of the columnar members. Acrylic transparent photosensitive material was used in forming the various types of columnar members having different sizes and different bottom cross-sectional areas in the color filters manufactured. Acrylic resin colored photosensitive material was used as the colored layer, and only the columnar members were formed from acrylic transparent photosensitive material. As explained above, the size and cross-sectional area of the columnar members were adjusted by changing the pattern size of the photomask in forming the columns. Also, samples with ITO formed on the surface were test manufactured.

Test 4

The purpose of this test is to find out the load-resistance strength of the columnar members. An acrylic colored photosensitive material was used in this test, with the bottom cross-sectional shape of the columnar members being rectangular with dimensions of 15x25 μm. Measurement for the amount of elastic deformation and of plastic deformation was performed while the load was changed.

Test 5

The purpose of this test was to measure the ITO breaking load for samples with different bottom cross-sectional areas of the columnar members. Acrylic colored photosensitive material was used in manufacturing color filters having columnar members of various sizes and bottom cross-sectional areas. An ITO film was then formed on the surface.

No black matrix layer was used in any of said Tests 1-5.

[0021]

Test 1

In the following, the method for forming columnar members with a gap function will be explained based on Test 1. In Test 1, the columnar members are formed at a prescribed interval on the 3-color lines. In the following, an example of the manufacturing method in this case will be explained with reference to Figures 2-4. Figure 2 shows the first process step for one embodiment of the color filter for liquid crystals in the present invention. Figure 2(A) is a plan view; Figure 2(B) is a cross section across a-a in Figure 2(A). Transparent substrate (2) is omitted in Figure 2(A), and the same is true in the following. As shown in Figure 2, first, as the colored material, acrylic negative photosensitive material ("COLOR MOSAIC CR-7001," product of Fuji Hunt Electronics Technology Co., Ltd.) was used to form a stripe of red (R) 3.5 μm thick. Here, because the columnar members are formed in the regions in various colors, in addition to the intrinsically red (R) stripes, red (R) columnar members R_1 were formed with the same thickness of 3.5 μm at prescribed green (G) region and blue (B) region locations. Also, as a test for control purposes, various samples were formed with the size and area of the bottom surface parallel to the substrate of the columnar members listed in Table 3.

[0022]

Figure 3 shows the second process step. Figure 3(A) is its plan view, and Figure 3(B) is a cross section across b-b in Figure 3(A). As shown in Figure 3, as the colored material, acrylic negative photosensitive material ("COLOR MOSAIC CG-7001" manufactured by Fuji Hunt Electronics Technology Co., Ltd.) was used to form a 3.5 μm thick green (G) stripe on the

transparent substrate. With said green (G) stripe, red (R) columnar members R_1 formed beforehand at prescribed locations of the green (G) region were covered. Also, columnar members G_1 were formed on R_1 in the blue (B) region.

[0023]

Figure 4 shows the third process step. Figure 4(A) is its plan view, and Figure 4(B) is a cross section across c-c in Figure 4(A). As shown in Figure 4, as a colored material, acrylic negative photosensitive material ("COLOR MOSAIC CB-7001" manufactured by Fuji Hunt Electronics Technology Co., Ltd.) was used to form a blue (B) stripe of 3.5 μm thick on the transparent substrate. Here, in addition to the intrinsically blue (B) stripe, blue (B) columnar members B_1 were formed on red (R) columnar members R_1 via the green (G) stripe and with a thickness of 3.5 μm. Here, columnar members B_1 were also formed on green (G) columnar members G_1 formed on the red (R) stripe.

[0024]

As a result of the aforementioned processes, in the green (G) stripe pattern region, columnar members of R_1+G+B_1 were formed; in the red (R) stripe pattern region, columnar members of R+G_1+B_1 were formed; and, in the blue (B) stripe pattern region, columnar members of R_1+G_1+B were formed. They were formed as protrusions with a height of 4.7 μm above the surface of the colored layer. The aforementioned formation method is a method applicable to an acrylic photosensitive material and a polyvinyl alcohol photosensitive material used as negative type photosensitive materials. Polyimide group material was used by coating a non-photosensitive material made of a polyimide precursor, followed by coating it with a positive type resist material. After exposure, development, etching, and resist peeling processing, the colored layer was converted to polyimide. As the negative type, an inverted photomask was used as the photomask. In any case, the height of the various layers was adjusted to 4.7 μm. Here, with regard to the mask pattern for forming said columnar members, only the pattern of the columnar member forming portion is added to the photomask for forming the conventional color filter, and there is usually no need to add other specific elements. Said trial products were prepared for the three types of colored photosensitive materials, that is, the acrylic type ("COLOR MOSAIC" manufactured by Fuji Hunt Electronics Technology Co., Ltd.), the polyvinyl alcohol type ("Trial product" manufactured by The Ink Tech Co., Ltd.), and the polyimide type ("Trial product" manufactured by Brewer Science Corp.).

[0025]

Test 2

Using the same manufacturing method as in Test 1, color filter substrate samples were prepared. Here, the same acrylic colored photosensitive material as that used in Test 1 was used to form various samples with different bottom cross-sectional areas of the columnar members ranging from 5x15 μm to 25x25 μm for measuring the amount of plastic deformation for different bottom cross-sectional areas of the columnar members. Said sizes can be realized by adjusting the pattern size of the photomask when the columnar members are formed. Also, samples were prepared by forming transparent electroconductive film layer (5) (1500 Å thick) made of ITO on the colored layers.

[0026]

Test 3

The columnar members were formed from a transparent photosensitive material, and in order to measure the amount of plastic deformation corresponding to different bottom cross-sectional areas, various samples were prepared having columnar members with different bottom cross-sectional areas ranging from 5x15 μm to 25x25 μm. These sizes can be realized by adjusting the pattern size of the photomask when forming the columnar members in said sizes.

[0027]

In the following, the other methods of forming the columnar members having a gap function will be explained with reference to Test 3. In Test 3, the columnar members were formed with a prescribed spacing on the 3-color lines. In the following, an example of the manufacturing method in this case will be explained with reference to Figures 5-7. Figure 5 shows the first process step in another embodiment of the color filter for liquid crystals of the present invention. Figure 5(A) is its plan view, and Figure 5(B) is a cross section across d-d in Figure 5(A). First, as shown in Figure 5, a negative acrylic colored photosensitive material ("COLOR MOSAIC" manufactured by Fuji Hunt Electronics Technology Co., Ltd.) was used to form colored layer (3) comprising red (R) stripes, green (G) stripes and blue (B) stripes on transparent substrate (2). Each colored layer has a film thickness of 1.5 μm. The process of their formation is the same as that for the formation of a conventional color filter. When the columnar members are formed by laminating colored layers, the colored layers themselves should be formed as thick films. On the other hand, when the columnar members are formed by forming a transparent photosensitive material layer after the formation of colored layer (3), the colored layer can be formed thinner. This is an advantage.

[0028]

Figure 6 include cross sections illustrating the second process step. Figure 6(A) is its plan view, and Figure 6(B) is a cross section taken across e-e of Figure 6(A). As shown in Figure 6, a transparent photosensitive material (acrylic photosensitive material) was used to form columnar members (4) on the colored layer. In order to form the columnar members with the prescribed height, a coating layer with film thickness of 5.5 μm was formed, only the portions for the columnar members (4) were exposed via the photomask, and prescribed development processing and drying were performed. As a result, columnar members (4) with a height of 4.7 μm were formed on the colored layer. Figure 7 shows the third process step. Transparent electroconductive film layer (5) made of ITO was next formed on columnar members (4) and colored layer (3) by means of sputtering. Here, the transparent electroconductive film has a film thickness of 1500 Å.

[0029]

Test 4

Using the same manufacturing method as in Test 1, a color filter substrate was manufactured. Here, the same type of acrylic colored photosensitive material as that in Test 1 was used. The size of the bottom cross-sectional area of the columnar members was 15x25 μm, and the total amount of deformation and the amount of plastic deformation were measured when the load applied on the columnar members was changed to determine the amount of elastic deformation.

[0030]

Test 5

Using the same manufacturing method as that in Test 1, a color filter substrate with an attached transparent electroconductive film made of ITO was manufactured. Here, the same acrylic colored photosensitive material as that in Test 1 was used. In order to measure the ITO breaking load for different bottom cross-sectional areas of the columnar members, samples having columnar members with various bottom cross-sectional areas ranging from 5x15 μm to 25x25 μm were prepared. These sizes were prepared by adjusting the pattern size of the photomask when the columnar members were formed. After formation of the color filter with the attached columnar members, a transparent electroconductive film was formed on the columnar members by means of sputtering over the entire surface, with a film thickness of 1500 Å.

[0031]

Evaluation on color filters

Test 1

The strength of the colored layer portion of the color filter prepared in Test 1 (the portion free of the columnar members) was measured using an ultra-micro hardness tester according to the following method.

Measurement method

Measurement equipment: Shimadzu "Dynamic Ultra-micro Hardness Tester DUH-201"

Measurement method: Measured using the indenter indentation test (MODE 1)

Measurement conditions:

Test load: 5.0 mN (0.51 gf)

Holding time: 5 sec

Loading speed: 0.236994 mN/s

Indenter type: 115° triangular pyramid indenter

Figure 8 is a diagram illustrating the load test for determining the dynamic hardness value. First, as shown in Figure 8(A), the load is raised at the aforementioned loading speed to the preset load of 5.0 mN, so that the triangular pyramid indenter with a triangular pyramid shaped tip (Figure 8(C)) is pressed onto the colored layer. After the load of 5.0 mN was reached, it was held for 5 sec. Then, the dynamic hardness value was determined from the load at the time (5.0 mN) and the depth of the indentation (Figure 8(B)).

[0032]

The results are listed in Table 1. It can be seen that there is a [hardness] tendency wherein acrylic group < polyvinyl alcohol group < polyimide group. In Table 1, the measurement units refer to the dynamic hardness values.

Table 1

Colored layer	Type of color filter		
	Acrylic group	PVA base	Polyimide group
R	50.5	53.4	62.8
G	51.8	54.3	56.7
B	54.2	56.9	58.6
Average value	52.2	54.9	59.4

[0033]

Using the same method as described above, the dynamic hardness of the columnar members of the color filter prepared in Test 1 was measured, with the results being listed in Table 2. In this case, also, the following trend was observed just as with the colored layer: acrylic group < polyvinyl alcohol group < polyimide group. In Table 2, the measurement units show the dynamic hardness values. As a result, it is clear that the hardness of the columnar members depends on the type of the resin material used for the colored layer. Compared with the acrylic group, the strength of the columnar members with the polyvinyl alcohol group is 1.13 times as great, and with the polyimide group the strength is 1.27 times as great. This means that when the columnar members having a gap control function are formed on the color filter, assuming 100 acrylic group columnar members should be provided with respect to a prescribed area, the number for the polyvinyl alcohol group becomes 88, and the number for the polyimide group becomes 78. In Table 2, "on R" means columnar members formed on the red colored layer.

[0034]

Table 2

	Type of color filter		
Colored layer	Acrylic group	PVA base	Polyimide group
on R	36.3	43.2	52.4
on G	39.9	44.8	46.3
on B	40.0	43.6	49.2
Average value	38.7	43.9	49.3

[0035]

Test 2

The strength of the columnar members of the color filter prepared in Test 2 was measured using an ultra-micro hardness tester using the following method.

Measurement method

Measurement equipment: Shimadzu "Dynamic Ultra-Micro Hardness Tester DUH-201"

Measurement method: Measured using the loading/unloading test (MODE 2)

Measurement conditions:

Test load: 5.0 mN (0.51 gf)

Holding time: 5 sec

Loading speed: 0.236994 mN/s

Indenter type: Cylindrical indenter 50 μmφ (±2 μm)

[0036]

Figure 9 illustrates the load test for determining the amount of plastic deformation and the amount of elastic deformation. Figure 9(A) shows the time elapsed in the test versus the load at the time. First of all, a cylindrical indenter was used to apply the load to the columnar member portion at a prescribed loading speed until the preset load of 5.0 mN was reached. The preset load was then held for 5 sec. After that, unloading was performed at a prescribed unloading speed (same as the loading speed). This is one measurement cycle. In practice, as shown in Figure 9(B), when the preset load is reached in applying the load, the depth becomes D1, and when the load is removed, the depth returns to D2. Because D2 is the deformation amount after unloading, it represents the amount of plastic deformation, while D1 represents the total amount of deformation under the preset load. Consequently, by subtracting D2 from D1, one can compute the amount of elastic deformation at the preset load.

[0037]

Table 3 lists the results of the measurements obtained under a load of 5 mN as the measurement condition for the columnar members having different sizes of columns formed on the R, G, B colored layers.

[0038]

Table 3

Colored layer	Column size	Column area	Load	D1	D2	Amount of elastic deformation	Amount of plastic deformation
on R	5x15	75	5.01	0.423	0.104	0.139	0.104
	10x10	100	5.006	0.248	0.079	0.169	0.079
	10x20	200	5.008	0.153	0.039	0.114	0.039
	15x15	225	5.004	0.13	0.047	0.083	0.047
	15x25	375	5.009	0.129	0.047	0.082	0.047
	20x20	400	5.005	0.097	0.026	0.071	0.026
	25x25	625	5.004	0.098	0.041	0.057	0.041
on G	5x15	75	5.008	0.165	0.052	0.113	0.052
	10x20	200	5.006	0.152	0.041	0.111	0.041
on B	5x15	75	5.004	0.183	0.046	0.137	0.046
	10x20	200	5.004	0.144	0.039	0.105	0.039

Here, the units of column size, D1, D2, amount of elastic deformation and amount of plastic deformation are μm.

The units of column area are μm^2, and the units of load are mN.

The same is true in the following tables.

[0039]

As can be seen from the results listed in Table 3, for the columnar members formed on colored layer R, the total amount of deformation (D1) changes as the area of the column becomes larger and crosses the boundary of 100 μm^2 and 200 μm^2. The same variation is displayed for the amount of plastic deformation (D2). If the column area of the columnar members is over 200 μm^2, the amount of plastic deformation decreases to lower than 0.05 μm. Then, for a column area of 200 μm^2, the amount of plastic deformation for each colored layer is found to be about 0.04 μm, and nearly the same value is displayed. As shown in Figure 4(B), the constitution of the columnar members differs for the different layers. That is, compared with the columnar members formed on the other colored layers, the columnar members formed on the R layer do not have the side surface of the column covered, and the load is applied directly onto the two-layer structure of the columnar members. Consequently, the amount of plastic deformation for [the column area] of 75 μm^2 is worse for the columnar members formed on the R layer than those formed on the other layers. However, as explained above, for those over 200 μm^2, the values are nearly the same for the various constitutions of the columnar members formed as described above.

[0040]

Consequently, it is possible to explain the fact that the amount of plastic deformation can be suppressed to 0.05 μm or less for a column area of 200 μm^2 or larger. That is, when the bottom cross-sectional area of the columnar members is over 200 μm^2, it is possible to suppress the amount of plastic deformation to 0.05 μm or less regardless of the constitution of the columnar members. When the columnar members with an area of 200 μm^2 are formed in a square shape, each edge becomes about 14 μm, but this does not mean that there is no restriction once the area exceeds 200 μm^2. When the area is made larger, the image quality degrades. However, because it is preferred that the columnar members not be recognizable at the clear vision distance, they should be formed as small as possible. Usually, the resolution of the human eyes (the smallest size at which the for presence of points can be detected) is about 1 min of angle. When this is taken as the reference in computing, the minimum resolution [sic; the highest resolution] when the liquid crystal display is viewed at a distance of about 30 cm becomes about 87 μm. Consequently, for a square with a diagonal dimension of 87 μm, this area becomes about 7570 μm^2.

[0041]

Table 4

Colored layer	Column size	Column area	Load	D1	D2	Amount of elastic deformation	Amount of plastic deformation
	5x15	75	5.006	0.237	0.092	0.145	0.092
	10x10	100	5.006	0.255	0.098	0.157	0.098
	10x20	200	5.004	0.191	0.12	0.071	0.12
on R	15x15	225	5.004	0.187	0.105	0.082	0.105
	15x25	375	5.007	0.157	0.087	0.07	0.087
	20x20	400	5.012	0.163	0.098	0.065	0.098
	25x25	625	5.006	0.16	0.1	0.06	0.1

[0042]

Table 4 lists the measurement values for the samples prepared by forming ITO layer on the R layer in Test 2. Just as with Test 2, shown in Table 3, where there was no ITO layer, it can be seen that the total amount of deformation (D1) changes when the area reaches 100 μm^2 and 200 μm^2. Also, comparison with Table 3 indicates that while the amount of elastic deformation is nearly the same, the amount of plastic deformation displays no dependence on the column size, and has a value of about 0.1 μm. From these features, it can be seen that the amount of elastic deformation depends on the underlying colored columnar members, and the amount of plastic deformation depends on the ITO layer, which is an inorganic film. In this case, when the columnar members are designed assuming a deformation amount of 0.12 μm or less under a load of 5 mN, it is possible to arrange the columnar members with no dependency on the column size. Also, as will be explained later, the ITO film breaking load is much higher, and it is believed that there is no practical problem for liquid crystal display devices caused by ITO breakage.

[0043]

Test 3

The strength of the columnar members of the trial-manufactured color filter samples in Test 3 was measured using the ultra-micro hardness tester using the same method as that in Test 2. The results are listed in Table 5. Here, the measurement was performed in the state before application of the ITO layer (Figure 6(B)).

[0044]

Table 5

Colored layer	Column size	Column area	Load	D1	D2	Amount of elastic deformation	Amount of plastic deformation
	5x15	75	5.014	0.248	0.124	0.124	0.124
	10x10	100	5.008	0.233	0.093	0.140	0.093
	10x20	200	5.011	0.151	0.056	0.095	0.056
on R	15x15	225	5.010	0.132	0.050	0.082	0.050
	15x25	375	5.009	0.131	0.064	0.067	0.064
	20x20	400	5.013	0.144	0.053	0.091	0.053
	25x25	625	5.008	0.120	0.040	0.080	0.040

[0045]

As can be seen from Table 5, when the column area becomes larger, the total amount of deformation (D1) changes when the column area crosses 100 μm^2 and 200 μm^2. This change displays the same pattern as that of the amount of plastic deformation (D2). When the column area of the columnar members is over 200 μm^2, even for the columnar members made of transparent photosensitive material, the amount of plastic deformation is still 0.05 μm or less. Among the samples prepared in Test 3, Table 6 lists the measurement values of those with ITO layer formed on them.

[0046]

Table 6

Colored layer	Column size	Column area	Load	D1	D2	Amount of elastic deformation	Amount of plastic deformation
	5x15	75	5.009	0.283	0.120	0.163	0.122
	10x10	100	5.009	0.351	0.110	0.241	0.110
	10x20	200	5.013	0.212	0.090	0.122	0.090
on R	15x15	225	5.008	0.189	0.111	0.078	0.111
	15x25	375	5.009	0.130	0.056	0.074	0.056
	20x20	400	5.011	0.163	0.108	0.055	0.108
	25x25	625	5.008	0.160	0.084	0.076	0.084

[0047]

Just as with Test 3, shown in Table 5, where there was no ITO layer, it can be seen that the total amount of deformation (D1) changes when the area reaches 100 μm^2 and 200 μm^2. Also, comparison with Table 5 indicates that while the amount of elastic deformation is nearly the same, the amount of plastic deformation displays no dependence on the column size, and has

a value of about 0.1 μm. From these features as in Test 2, it can be seen that the amount of elastic deformation depends on the underlying transparent columnar members, and the amount of plastic deformation depends on the ITO layer, which is an inorganic film. In this case, when the columnar members are designed by assuming a deformation amount of 0.12 μm or less under a load of 5 mN, it is possible to arrange the columnar members with no dependency on the column size.

[0048]

Test 4

The load test of the columnar members of the color filter prepared in Test 4 was performed using the following method. In this case, the cross-sectional area of columnar members (4) is 15x25 μm as described above. The amount of elastic deformation and the amount of plastic deformation were measured by changing the load as a parameter.

Measurement method

Measurement equipment: Shimadzu "Dynamic Ultra-Micro Hardness tester DUH-201"
Measurement method: Measured using the loading/unloading test (MODE 2)
Measurement conditions:
Test load: 5.0-500 mN
Holding time: 5 sec
Loading speed: 0.236994 mN/s
Indenter type: Cylindrical indenter 50 μmφ (±2 μm)

[0049]

Figure 10 is a graph illustrating the deformation amount versus the load on the columnar members, and measurement data. Figure 10(A) is a graph illustrating the measurement results for the columnar member portion of the color filter prepared in Test 4. Figure 10(B) is a table listing the measurement data. As can be seen from the graph, when a load of 100 mN or higher is applied, the elastic deformation and plastic deformation display the same tendency. From this fact, it can be seen that the columnar members are broken. That is, for the columnar members measuring 15x25 μm, each column can sustain a load of 100 mN (10.2 gf), and this value is sufficient for practical applications. However, there is also a limit for such columnar members in practical applications. As can be seen from the graph shown in Figure 10, when a load over 100 mN is applied, the deformation amount changes drastically. Assuming the height of the columnar members is 4 μm at the time of operation when a load of 200 mN is applied, an amount of plastic deformation of 0.5 μm takes place, and the gap control becomes 3.5 μm. In order to

laminate the colored layers to increase the height of the column, the colored layers should usually be made thick, so that design and processing become very difficult to perform. On the other hand, when a load lower than 100 mN is applied, the amount of plastic deformation becomes 0.2 μm or less, and it is possible to design the columnar members by taking such a deformation amount into consideration from the beginning.

[0050]

Of course, when a transparent resin is patterned to form the columnar members after formation of the colored layer, the height of the columnar members finally needed can be designed taking into consideration the composition deformation amounts under said load. As will be explained later, while the amount of plastic deformation of each microball under a load of 5 mN is 0.5 μm as listed in Table 8, the load for the columnar members is 200 mN as aforementioned. That is, it can withstand a load about 40 times higher. As a result, the value is sufficient for practical application.

[0051]

Test 5

The ITO breaking load test for the columnar member portion of the color filter prepared in Test 5 was carried out using the following method. In this case, there are four types of columnar members with cross-sectional areas of 10x10, 15x15, 20x20, and 25x25 μm, respectively. The load for said columnar members was then changed, and the substrates after loading were observed in a microscope to check for ITO breakage, and a load exceeding the breaking level was applied in the test.

Measurement method

Measurement equipment: Shimadzu "Dynamic Ultra-Micro Hardness tester DUH-201"
Measurement method: Measured using the loading/unloading test (MODE 2)
Measurement conditions:
Test load: 5.0-750 mN
Holding time: 5 sec
Loading speed: 0.236994 mN/s
Indenter type: Cylindrical indenter 50 μmφ (±2 μm)

[0052]

Figure 11 shows the results of the ITO breaking load test of the columnar member portion. Figure 11 shows the total amount of deformation under said test load. As can be seen

from the figures, ITO breaking takes place at a load of 200 mN for 10x10 μm, 350 mN for 15x15 μm, 500 mN for 20x20 μm, and 750 mN for 25x25 μm.

Also, it can be seen that the graph that there is an inflection point in ITO breakage. Also, the breaking inflection point depends on the column size. For any of these sizes, the ITO breaking load is usually much higher than the load applied to the columnar members. Consequently, it is clear that such columnar members can function well as gap controlling material.

[0053]

Comparative example

The amount of plastic deformation was measured for the spacers when ball-shaped spacers were used in conventional color filters. That is, on a color filter substrate free of the columnar members but formed otherwise in the same way as in Test 1, spacers with mean grain size of 5.00 ± 0.05 μm and with standard deviation of 0.19 ± 0.01 μm ("Micropearl SPN-205" manufactured by Sekisui Fine Chemical Co., Ltd.) were scattered to prepare the sample, and measurement was performed using the same measurement method as Test 2. The test method is as follows. In the following, the aforementioned spacers will be referred to as "Micropearls."

[0054]

Micropearl test method

A small quantity of Micropearls was added in IPA (isopropyl alcohol, product of Junsei Chemical Co., Ltd.), followed by through agitation to prepare a dispersion. By means of tweezers, a piece of cloth was dipped in the IPA solution with Micropearls dispersed in it. Said piece of cloth was used to wipe the color filter to attach the Micropearls. Then the IPA was evaporated at room temperature. Observation in a microscope found one Micropearl grain attached for each colored pixel, and this was taken as the measurement object. In Table 10, for comparison, measurement was performed on both one Micropearl grain and two Micropearl grains.

[0055]

The results are listed in Tables 7-10. It can be seen from Tables 7 and 8 that the amount of plastic deformation of a Micropearl under a load of 5 mN is about 0.5-0.6 μm, that is, the amount of plastic deformation in this case is about one order of magnitude greater than that of the columnar members of the present invention.

[0056]

Table 7

Sample type	Load	D1	D2	Amount of elastic deformation	Amount of plastic deformation
Standard CF (R) + Micropearl	5.006	1.761	0.606	1.155	0.606
Standard CF (G) + Micropearl	5.01	1.769	0.647	1.122	0.647
Standard CF (B) + Micropearl	5.009	1.803	0.681	1.122	0.681

[0057]

Table 8

Sample type	Load	D1	D2	Amount of elastic deformation	Amount of plastic deformation
Standard CF (R) + ITO + Micropearl	5.014	1.701	0.508	1.193	0.508
Standard CF (G) + ITO + Micropearl	5.014	1.713	0.516	1.197	0.516
Standard CF (B) + ITO + Micropearl	5.004	1.688	0.515	1.173	0.515

[0058]

Table 9

Sample type	Load	D1	D2	Amount of elastic deformation	Amount of plastic deformation
Glass + Micropearl	5.014	1.596	0.423	1.173	0.423
Glass + Micropearl	7.014	1.861	0.516	1.345	0.516

[0059]

Table 10

Sample type	Load	D1	D2	Amount of elastic deformation	Amount of plastic deformation
Standard CF (B) + ITO + 1 Micropearl grain	5.004	1.688	0.515	1.173	0.515
Standard CF (B) + ITO + 2 Micropearl grain	5.014	0.994	0.328	0.666	0.328

[0060]

Comparison between Tables 8 and 9 indicates that while the amount of plastic deformation of the standard color filter + ITO + Micropearl in Table 8 is about 0.51 μm, the amount of plastic deformation is about 0.42 μm for the sample with Micropearls attached to glass (Table 9). The difference between them corresponds to the deformation amount attributed to the color filter itself. It is 0.1 μm or less, and it can be estimated that almost all of the deformation

comes from deformation of the Micropearl. When the load is changed as listed in Table 9, both the total amount of deformation and the amount of plastic deformation change, so that the Micropearl undergoes deformation. In order to check the effect of the number of Micropearl grains on the amount of plastic deformation, measurement was performed on samples having two Micropearl grains for each pixel. The results are listed in Table 10. In order to reduce the amount of plastic deformation, it is necessary to provide plural Micropearl grains for each pixel.

[0061]

In the following, determination of the degree of the load on each spacer will be explained. Assuming a load of 10 kgf is applied over the entirety of a 11.3-inch (diagonal length of the screen) panel. For an 11.3-inch panel, the two edges are usually 172.8x230.4 mm, and the area is about 40,000 mm^2 (400 cm^2). In order to scatter 100-200 spacers per mm^2, the total number of the spacers scattered can reach 4 million to 8 million. When this number is used to divide the 10 kgf load, the load applied to each spacer can be determined to range from 1.25-2.50 mgf.

[0062]

In the following, computations will be performed with more specific data. The pressure applied when the substrates are laminated is in the range of 0.45-0.55 kg/cm^2. Assuming the pressure applied on the substrates when they are laminated is 0.5 kg/cm^2, the overall force applied to the entire substrate is 200 kgf. With this number, the aforementioned load applied to each spacer becomes 25-50 mgf.

[0063]

Here, the test load of 5.0 mN (0.51 gf) corresponds to a load on 10-20 spacers. This corresponds to the quantity of spacers present in 0.1 mm^2 as described above, and because the size of each pixel of an S-VGA (Super Video Graphics Array) is 288x96 μm, this corresponds to 3.6 pixels. That is, the test load of 5.0 mN (0.51 gf) corresponds to about 3 pixels of RGB with the conventional spacers, taking into consideration the inch size of the panel and the specifications of the display.

[0064]

As explained above, the samples of color filters with columnar members formed using acrylic colored material in Test 2 and Test 3 have the capability [to resist] plastic deformation equal to or greater than that of Micropearls, so that they are sufficiently effective as gap control material. On the other hand, for the color filters of Test 1 having columnar members prepared

using the acrylic group, polyvinyl alcohol group and polyimide group colored materials, it has been found that the columnar members made of the acrylic group colored material have a lower hardness than the polyvinyl alcohol group and polyimide group columnar members. As a result, it is believed that if the acrylic group [columnar members] can be sufficiently effective as a gap control material, the other two types of materials can be considered to fully display the function.

[0065]

Application example pertaining to a liquid crystal display device

Based on the aforementioned trial production results, color filters for liquid crystals (two types, that is, a type with columnar members made of the colored photosensitive material in Test 1 and a type with columnar members made of the transparent photosensitive material in Test 3) were prepared having columnar members with a bottom cross-sectional area of 15 x 15 μm made of acrylic photosensitive material and with columnar members measuring 50 x 50 μm formed on the sealing material coating portion around the color filter substrate. Each of them was used to assemble a liquid crystal display device. First, a TFT substrate prepared using the aforementioned trial production method was coated with a polyimide group orienting film and treated for orientation in order to form the opposing substrate. Similarly, a polyimide group orienting film was coated and treated for orientation for the color filter side. Then a sealing material ("STRUCTBOND XN-21-S-B" manufactured by Mitsui Toatsu Chemical Co., Ltd.) was applied on the outer periphery of the side of the color filter substrate. Then the opposing substrate and the color filter substrate were bonded to each other, leaving only the liquid crystal injection part. Finally, liquid crystal was injected into said cell substrates which were then sealed. Then, the prescribed driving circuit and illumination device were provided to complete the liquid crystal display device. In each completed liquid crystal display device, a constant spacing was maintained between the opposing substrate and the color filter, and image display function tests gave excellent results.

[0066]

Effect of the invention

The present invention displays the following significant effects.

① Columnar members are used as alternative spacers, and by selecting the material, size and strength of the columnar members, it is possible to fully achieve the same function as the spacers in the prior art.

② For columnar members made of colored photosensitive material, it is possible by changing the mask pattern to form columnar members with an even spacing between them without excessive processing steps. On the other hand, for columnar members made of

transparent photosensitive material, it is possible to form columnar members at any desired height with good accuracy.

③ In any case, it is possible to form the columnar members with a constant regular relationship, and they can be secured in place. Consequently, there is no degradation of the image display and there is no light scattering caused by shifting as would take occur for spacers in the prior art.

④ Arranging the columnar members in the sealing portion around the color filter substrate eliminates the need to include spacer material in the sealant.

Brief description of the figures

Figure 1 is a schematic diagram illustrating an example of the color filter for liquid crystals in the present invention.

Figure 2 shows the first process step in an embodiment of the color filter for liquid crystals in the present invention.

Figure 3 shows the second process step.

Figure 4 shows the third process step.

Figure 5 shows the first process step in another embodiment of the color filter for liquid crystals in the present invention.

Figure 6 shows its second process step.

Figure 7 shows its third process step.

Figure 8 is a diagram illustrating the load test for determining the dynamic hardness value.

Figure 9 is a diagram illustrating the load test for determining the amount of plastic deformation and the amount of elastic deformation.

Figure 10 shows a graph and measurement data illustrating the deformation amount of the columnar members under load.

Figure 11 is a diagram illustrating the results of the ITO breaking load test for the columnar member portion.

Explanation of the reference symbols

1 Color filter for liquid crystals
2 Transparent substrate
3 Colored layer or color filter layer
4 Columnar member
5 Transparent electroconductive film layer
6 Overcoat layer

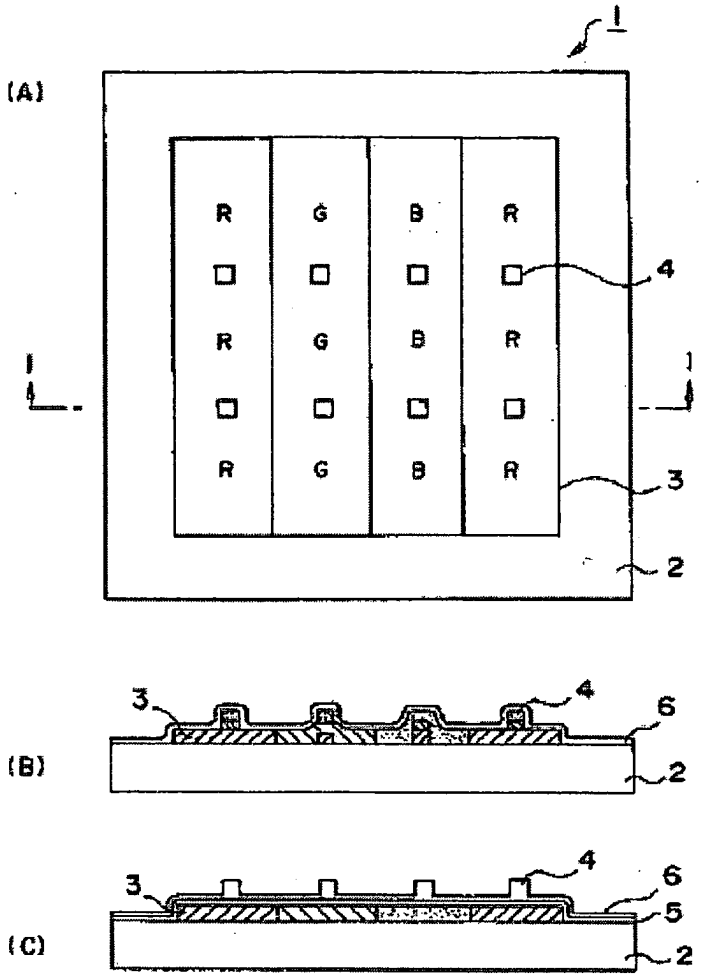


Figure 1

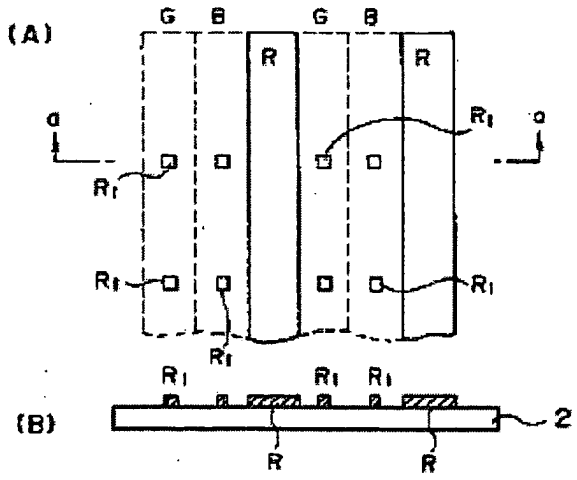


Figure 2

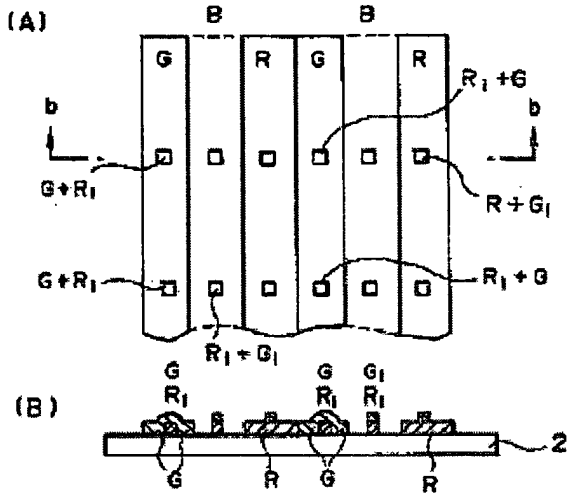


Figure 3

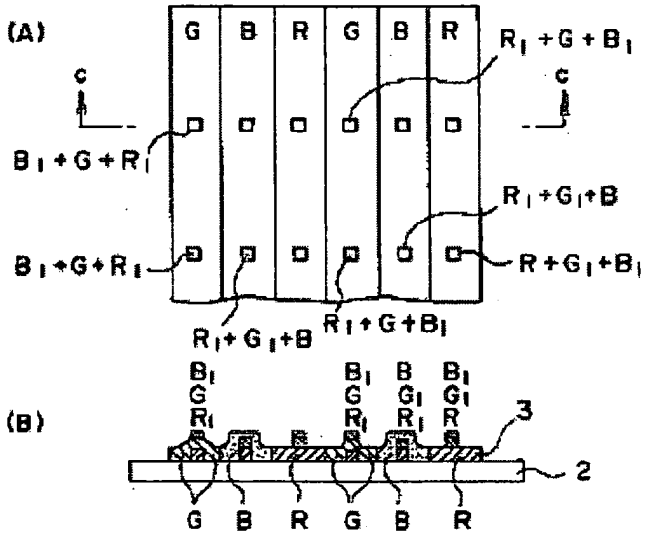


Figure 4

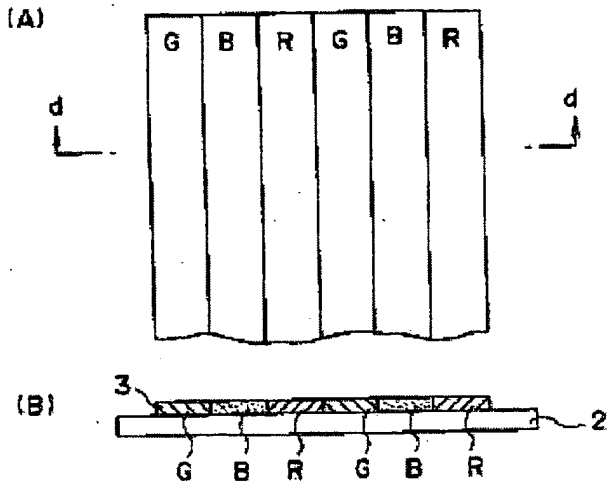


Figure 5

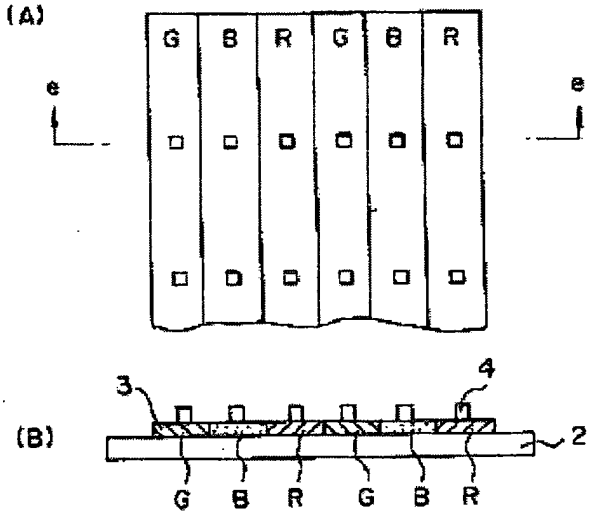


Figure 6

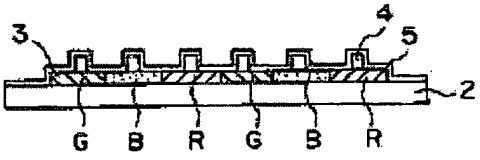


Figure 7

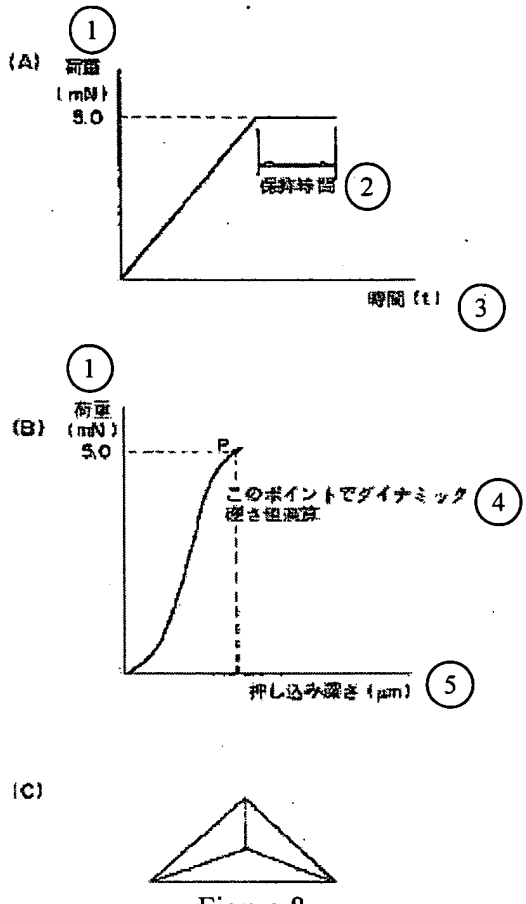


Figure 8

Key:
1 Load (mN)
2 Holding time
3 Time (t)
4 The dynamic hardness value is computed at this point
5 Indentation depth (μm)

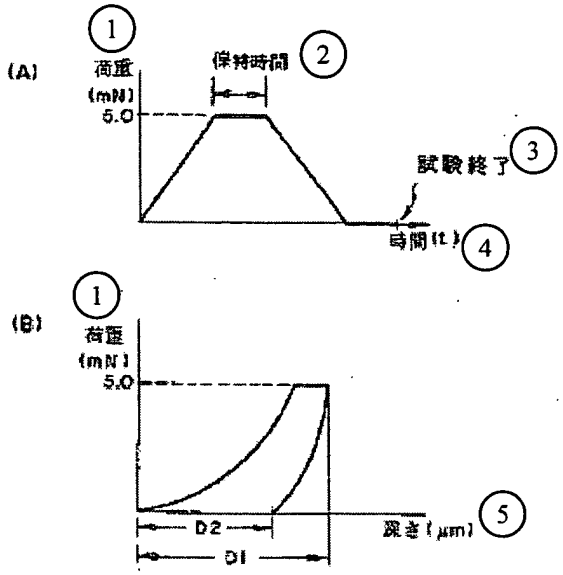
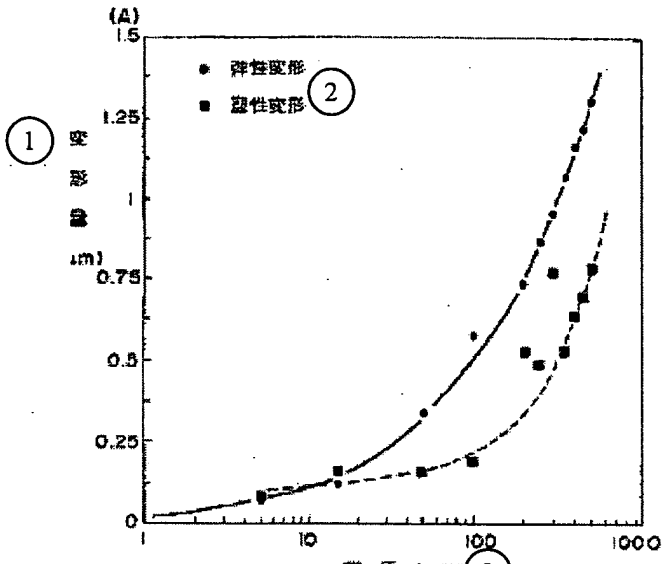


Figure 9

Key:
1 Load (mN)
2 Holding time
3 End of test
4 Time (t)
5 Depth (μm)



(B) パールレス CF (ITO あり)

4

荷重 (mN)	D1 (μm)	D2 (μm)	弾性変形	塑性変形
5.007	0.157	0.087	0.07	0.087
15.005	0.283	0.161	0.122	0.161
50.1	0.507	0.164	0.343	0.164
100.06	0.782	0.201	0.581	0.201
200.2	1.274	0.533	0.741	0.533
250.5	1.366	0.492	0.874	0.492
300.4	1.739	0.776	0.963	0.776
350.2	1.613	0.537	1.076	0.537
400.3	1.814	0.641	1.173	0.641
450.6	1.929	0.702	1.227	0.702
500.5	2.104	0.791	1.313	0.791

5

Figure 10

Key:
1 Deformation amount (μm)
2 Elastic deformation
Plastic deformation
3 Load (mN)
4 Pearl-less CF (with ITO)
5 Load (mN)
D1
D2
Elastic deformation
Plastic deformation

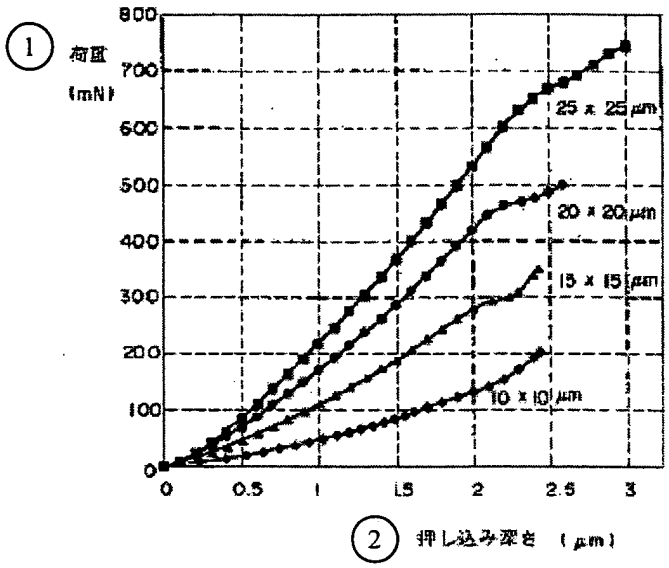


Figure 11

Key: 1 Load (mN)
2 Indentation depth (μm)

February 17, 2009

Re: 6774-119915

To Whom It May Concern:

This is to certify that a professional translator on our staff who is skilled in the Japanese language translated "JP10082909A" from Japanese into English.

We certify that the English translation conforms essentially to the original Japanese language.

K Vitray

Kim Vitray
Operations Manager

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My Commission Expires
March 09, 2011

Vicki L Wunneburger

Vicki Wunneburger
Notary Public

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	1/1343			1/1343		
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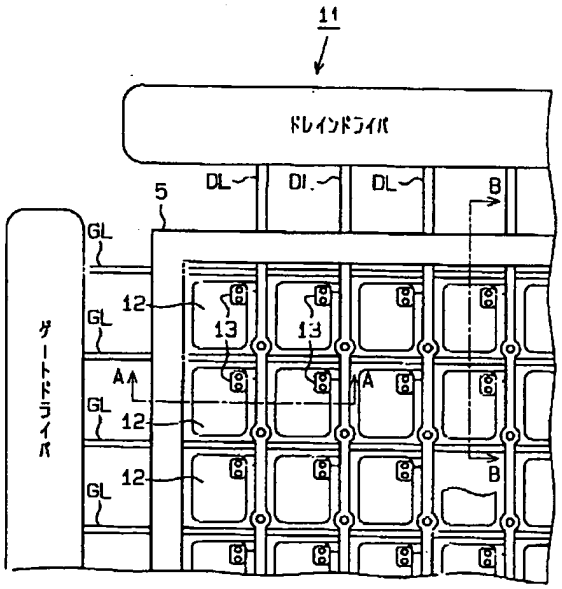
(54)【発明の名称】　膜材がパターン形成された固体装置及びパターン形成方法

(57)【要約】
【課題】例えば薄膜電極が基板表面にパターン形成された液晶表示装置にあって、ブラシスクラバ等による基板洗浄に伴う薄膜電極の損傷を防止する。
【解決手段】ポリシリコン形ＴＦＴ方式アクティブマトリックス液晶表示装置を構成するＴＦＴアレイ側基板１１の透明絶縁基板上にはＩＴＯにて形成される画素電極２２がマトリックス状に設けられている。また、アレイ側基板１１の透明絶縁基板上には、ブラシスクラバ等による基板洗浄の際に画素電極２２が損傷することを防止するために、画素電極２２群の外周を囲むように同画素電極２２より膜厚の薄いダミー膜５が設けられる。



【特許請求の範囲】
【請求項１】表面に適宜の膜材がパターン形成された状態でブラシ洗浄される固体装置において、
当該装置の同一表面において前記膜材の外周を囲むようにパターン形成されたダミー膜を備えることを特徴とする膜材がパターン形成された固体装置。
【請求項２】前記ダミー膜は、その膜厚が前記膜材の膜厚よりも薄くパターン形成されたものである請求項１記載の膜材がパターン形成された固体装置。
【請求項３】前記ダミー膜は、その膜厚が装置外周に向かうにしたがって順次薄くなる勾配を有して若しくは階段状にパターン形成されたものである請求項１または２記載の膜材がパターン形成された固体装置。
【請求項４】前記ダミー膜は、前記膜材と同一材料にてパターン形成されたものである請求項１～３のいずれかに記載の膜材がパターン形成された固体装置。
【請求項５】前記ダミー膜は、前記膜材と異なる材料にてパターン形成されたものである請求項１～３のいずれかに記載の膜材がパターン形成された固体装置。
【請求項６】前記固体装置は液晶表示装置の液晶駆動用半導体素子が設けられる透明絶縁基板であり、前記膜材は同透明絶縁基板の表面に上にパターン形成された画素透明電極である請求項１～５のいずれかに記載の膜材がパターン形成された固体装置。
【請求項７】固体装置の表面に膜材をパターン形成する方法において、
少なくとも前記固体装置の最外周にパターン形成される膜材の膜厚をそれ以外の部分にパターン形成される膜材の膜厚よりも薄くすることを特徴とするパターン形成方法。
【請求項８】固体装置の表面に膜材を着膜する工程と、該着膜した膜材の膜厚がその端部ほど薄くなるようにプラズマ反応圧力を高めたプラズマドライエッチングにて同膜材をエッチングする工程と、
を備えるパターン形成方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、例えば透明電極がパターン形成された液晶表示装置など、膜材がパターン形成された固体装置、及びパターン形成方法に関する。
【０００２】
【従来の技術】従来、表示装置、例えばポリシリコン形ＴＦＴ（Thin Film Transistor：薄膜トランジスタ）方式アクティブマトリックス液晶表示装置等においては、その画素電極としてＩＴＯ（Indium Tin Oxide）等の透明薄膜電極が使用されている。この透明薄膜電極はポリシリコン形ＴＦＴをガラス基板等の上に形成した後にパターニングして形成される。そして、特に歩留まりの向上を図るものに対しては、その後の製造工程に移る前にブラシスクラバ等による基板洗浄が行われている。
【０００３】ここで、図１０～図１２を参照して、上記ブラシスクラバを用いた基板洗浄の概要を説明する。図１０に上記液晶表示装置のＴＦＴアレイ側基板１の部分平面構造を示し、図１１には同図１０のＸ－Ｘ線に沿った断面構造を示す。なお、図１１に示す断面構造においてＴＦＴ等、画素電極以外の液晶駆動にかかる部分の図示は省略する。
【０００４】図１０に示すＴＦＴアレイ側基板１において、ドレインドライバに接続されるドレイン線ＤＬとゲートドライバに接続されるゲート線ＧＬとの交点近傍に液晶表示装置を構成する各表示画素の画素電極２がパターン形成されている。この画素電極２はＴＦＴアレイ側基板１のほぼ全面において所定画素数分、マトリックス状に形成されているが、図１０においてはその一部分のみを示す。
【０００５】また、画素電極２は上述のＩＴＯからなり、コンタクトホール３を介してＴＦＴのソース電極（図示略）に接続されている。また同画素電極２は、図１１に示されように、ＴＦＴアレイ側基板１を構成する透明絶縁基板（ガラス基板等）１ａ上に形成されている。
【０００６】次に、図１２に示す平面図に基づき、ブラシスクラバを使用したＴＦＴアレイ側基板１の洗浄態様を説明する。基板洗浄に際しては同図１２に示されるように、ＴＦＴアレイ側基板１を所定の回転台（図示略）に載置し、同回転台を回転させた状態で同じく回転させたブラシスクラバのブラシ部４を当該基板１の表面に当接させる。そして、同図１２の矢印Ｙ方向にブラシ部４を移動させながら同基板１の表面全体を洗浄する。なおこのとき、薬液を用いた化学的洗浄と併用されることも多い。
【０００７】
【発明が解決しようとする課題】ところで、上述したようなＩＴＯ等の画素電極２がその最上部にパターン形成されたＴＦＴアレイ側基板１をブラシスクラバを使用して洗浄する場合にあっては、図１３に示されるように、画素電極２のうちの上記回転するブラシスクラバのブラシ４ａに最初に当接する電極がその機械的な力によって損傷してしまうことがある。このように基板１の洗浄工程において画素電極２が損傷を被ると、それは画素欠陥となり、ひいては液晶表示装置としての製品歩留りを低下させる要因ともなる。
【０００８】なお、こうした液晶表示装置に限らず、半導体装置等を含めてその表面に膜材がパターン形成され、その後上記ブラシスクラバ等によって表面洗浄される固体装置にあっては、こうした実情も概ね共通したものとなっている。
【０００９】本発明は上記実情に鑑みてなされたものであり、その目的とするところは、ブラシスクラバ等による洗浄に対してその表面にパターン形成された膜材を好

適に保護し、ひいては製品歩留りを向上させることのできる膜材がパターン形成された固体装置及びパターン形成方法を提供することにある。

【００１０】

【課題を解決するための手段】上記の目的を達成するために、請求項１に記載の発明では、表面に適宜の膜材がパターン形成された状態でブラシ洗浄される固体装置において、当該装置の同一表面において前記膜材の外周を囲むようにパターン形成されたダミー膜を備えることをその要旨とする。

【００１１】同構成においては、固体装置の同一表面において前記膜材の外周を囲むようにパターン形成されたダミー膜が備えられる。そのため、固体装置を例えばブラシスクラバ等を使用してブラシ洗浄する場合、ブラシスクラバのブラシは前記パターン形成された膜材と当接する前にまずダミー膜に当接する。そのため、回転するブラシスクラバのブラシの機械的な力によって前記膜材が損傷することは防止される。

【００１２】また請求項２に記載の発明では、請求項１記載の膜材がパターン形成された固体装置において、前記ダミー膜は、その膜厚が前記膜材の膜厚よりも薄くパターン形成されたものであることをその要旨とする。

【００１３】同構成においては、固体装置を例えばブラシスクラバ等を使用してブラシ洗浄する場合、ブラシスクラバのブラシは、まず膜材の膜厚よりも薄くパターン形成されたダミー膜に乗り上げ段差を小さくしてから同膜材に乗り上がるようになる。そのため、回転するブラシスクラバのブラシの機械的な力によって前記膜材が損傷することは好適に防止される。

【００１４】また請求項３に記載の発明では、請求項１または２記載の膜材がパターン形成された固体装置において、前記ダミー膜は、その膜厚が装置外周に向かうにしたがって順次薄くなる勾配を有して若しくは階段状にパターン形成されたものであることをその要旨とする。

【００１５】同構成においては、固体装置を例えばブラシスクラバ等を使用してブラシ洗浄する場合、ブラシスクラバのブラシはダミー膜の勾配若しくは階段に沿って好適に前記膜材に乗り上がるようになる。そのため、回転するブラシスクラバのブラシの機械的な力によって前記膜材が損傷することは好適に防止される。

【００１６】また請求項４に記載の発明では、請求項１～３のいずれかに記載の膜材がパターン形成された固体装置において、前記ダミー膜は、前記膜材と同一材料にてパターン形成されたものであることをその要旨とする。

【００１７】同構成によれば、ダミー膜を形成するための別途マスク等は不要となり、その製造工程が簡略化される。また請求項５に記載の発明では、請求項１～３のいずれかに記載の膜材がパターン形成された固体装置において、前記ダミー膜は、前記膜材と異なる材料にてパターン形成されたものであることをその要旨とする。

【００１８】同構成によれば、ダミー膜の設計等の自由度が高まる。また請求項６に記載の発明では、請求項１～５のいずれかに記載の膜材がパターン形成された固体装置において、前記固体装置は液晶表示装置の液晶駆動用半導体素子が設けられる透明絶縁基板であり、前記膜材は同透明絶縁基板の表面に上にパターン形成された画素透明電極であることをその要旨とする。

【００１９】同構成によれば、液晶表示装置にあって、透明絶縁基板表面のブラシ洗浄に伴う画素透明電極の損傷は好適に防止される。また請求項７に記載の発明では、固体装置の表面に膜材をパターン形成する方法において、少なくとも前記固体装置の最外周にパターン形成される膜材の膜厚をそれ以外の部分にパターン形成される膜材の膜厚よりも薄くすることをその要旨とする。

【００２０】同形成方法においては、膜材の段差が緩和されるため、ブラシ洗浄に伴う同膜材の損傷も好適に防止される。また請求項８に記載の発明では、パターン形成方法において、固体装置の表面に膜材を着膜する工程と、該着膜した膜材の膜厚がその端部ほど薄くなるようにプラズマ反応圧力を高めたプラズマドライエッチングにて同膜材をエッチングする工程と、を備えることをその要旨とする。

【００２１】同形成方法においては、膜材の段差が緩和されるため、ブラシ洗浄に伴う同膜材の損傷も好適に防止されるとともに、製造工数を増やすことなく勾配を有する膜材を得ることができる。

【００２２】

【発明の実施の形態】［第１の実施の形態］以下、本発明にかかる膜材がパターン形成された固体装置をポリシリコン形ＴＦＴ方式アクティブマトリックス液晶表示装置に適用した第１の実施の形態について図１～図４に基づき詳細に説明する。

【００２３】図１は、本実施の形態にかかる固体装置（液晶表示装置）のＴＦＴアレイ側基板１１の部分平面構造を示すものである。また、図２（ａ）は、この図１のＡ－Ａ線に沿った断面構造、図２（ｂ）は同じく図１のＢ－Ｂ線に沿った断面構造をそれぞれ示すものである。

【００２４】図１に示すＴＦＴアレイ側基板１１において、ドレインドライバに接続されるドレイン線ＤＬとゲートドライバに接続されるゲート線ＧＬとの交点近傍に液晶表示装置を構成する各表示画素の画素電極１２がパターン形成されている。この画素電極１２はＴＦＴアレイ側基板１１のほぼ全面において所定画素数分、マトリックス状に形成されているが、図１においてはその一部分のみを示す。

【００２５】また、画素電極１２は上述のＩＴＯからなり、コンタクトホール１３を介してＴＦＴのソース電極（図示略）に接続されている。また同画素電極１２は、

図2に示されように、ＴＦＴアレイ側基板１１を構成する透明絶縁基板（ガラス基板等）１１ａ上に形成されている。

【００２６】ここで本実施の形態にかかる液晶表示装置にあっては、図1に示されるように、マトリックス状に設けられた画素電極１２の外周を連続して囲むようにして、ダミー膜５が設けられている（図1にはその一部のみ示される）。また、図2（ａ）及び（ｂ）に示されるように、同ダミー膜５の膜厚は、画素電極１２の膜厚よりも薄く形成されている。このダミー膜５は、前記ブラシスクラバ（図１２、図１３）を使用してアレイ側基板１１を洗浄する際に、同ブラシスクラバのブラシ４ａによって画素電極１２が損傷することを防止するために設けられている。

【００２７】すなわち、本第１の実施の形態においては、図3に示されるように、前記ブラシ４ａが画素電極１２と当接する際、同ブラシ４ａは、まずダミー膜５に乗り上がり、画素電極１２との段差が小さくなった状態で同画素電極１２に乗り上がる。そのため、回転するブラシ４ａの機械的な力によって画素電極１２自体が損傷することは防止されるようになる。

【００２８】なお、このダミー膜５は画素電極１２と同様にＩＴＯにて形成されてもよいし、その他の材質にて、例えばＡｌ（アルミニウム）、Ｃｒ（クロム）等にて形成されてもよい。

【００２９】次に、図4を参照して、上記ダミー膜５及び画素電極１２の形成方法を説明する。これら膜材のパターン形成に際しては、まず図４（ａ）に示すように、透明絶縁基板１１ａ上にダミー膜５となる薄膜５Ａを成膜する。次に、図４（ｂ）に示すように所定のレジストパターン６を形成し、続いて図４（ｃ）に示すように薄膜５Ａをエッチングする。その後、レジストパターン６を剥離することで、透明絶縁基板１１ａ上に薄膜ダミー配線５が形成される。

【００３０】次に、図４（ｄ）に示すように、透明絶縁基板１１ａ上に上記画素電極１２となるＩＴＯ膜１２Ａを成膜し、その上に所定のレジストパターン６ａを形成する。続いて、この成膜したＩＴＯ膜２Ａをエッチングし、レジストパターン６ａを剥離すると、図４（ｅ）に示されるように、画素電極１２及びダミー膜５が透明絶縁基板１１ａ上に形成されるようになる。

【００３１】以上説明したように、本第１の実施の形態によれば、以下のような効果を得ることができる。

（１）本第１の実施の形態では、液晶表示装置のＴＦＴアレイ側基板１１の透明絶縁基板１１ａ上において、画素電極１２の周囲を連続して囲んで、且つその膜厚が同画素電極１２の膜厚より薄く形成されるダミー膜５が設けられる。そのため、ブラシスクラバを使用して前記基板１１を洗浄する場合にあっても、ブラシスクラバのブラシ４ａが画素電極１２と当接する際、ブラシ４ａはいきなり画素電極１２の側面に衝突せずに、まずダミー膜５に乗り上げて、画素電極１２の段差が小さくなってから同画素電極１２に乗り上げるようになる。そのため、同ブラシ４ａの機械的な力によって画素電極１２が損傷することが防止され、ひいては液晶表示装置としての生産歩留りが向上されるようになる。

【００３２】なお、上記ダミー膜５の形状は、図1に示したような画素電極１２の外周を連続して囲む形状に限られない。他に例えば、図5に示すように、画素電極１２の形状に対応して切断された形状となるダミー膜５ａの集合として同画素電極１２の外周を囲む形状としてもよい。このダミー膜として要は、透明絶縁基板１１ａ上において画素電極１２より同基板端側にあって画素電極１２の周囲を囲むように設けられるとともに、その膜厚が画素電極１２の膜厚より薄く形成されるものであればよい。

【００３３】また、上述のようにダミー膜５は画素電極１２と同様にＩＴＯにて形成されてもよいし、その他の材質にて、例えばＡｌ（アルミニウム）、Ｃｒ（クロム）等にて形成されてもよいが、ＩＴＯにて形成される場合は、画素電極１２をパターン形成する工程において一括してダミー膜５をパターン形成することができる。すなわち、ダミー膜５を形成するための別途マスク等は一切不要であり、その製造工数、製造コストを低く抑えることが可能となる。一方、ダミー膜５をＩＴＯ以外の材質にて形成する場合は、同ダミー膜５の設計等の自由度が高まる。

［第２の実施の形態］次に、本発明にかかる膜材がパターン形成された固体装置を同じくポリシリコン形ＴＦＴ方式アクティブマトリックス液晶表示装置に適用した第２の実施の形態について図６～図９に基づき詳細に説明する。

【００３４】図6は本実施の形態にかかる固体装置（液晶表示装置）のＴＦＴアレイ側基板２１の部分平面構造を示すものである。図７（ａ）は、この図６のＣ－Ｃ線に沿った断面構造、図７（ｂ）は、同じく図６のＤ－Ｄ線に沿った断面構造をそれぞれ示すものである。

【００３５】ここでは第１の実施の形態との相違点を中心に説明する。本第２の実施の形態の前記第１の実施の形態との相違点は、図６に示されるように、マトリックス状に設けられた画素電極２２の外周を囲むダミー膜として、同画素電極２２を２重に囲むダミー電極２２ａ，２２ｂが設けられている点にある（図６にはその一部のみ示される）。また、これらダミー電極２２ａ，２２ｂの平面形状は画素電極２２と同一に形成されるとともに、その膜厚は画素電極２２の膜厚に比べて薄く形成される。さらに、図７（ａ），（ｂ）に示されるように、同ダミー電極２２ａ，２２ｂの表面は、その膜厚が画素電極２２からアレイ側基板２１端部に向けて、すなわち図７（ａ）及び（ｂ）においてはその右側から左側に向

けて薄くなるように勾配を有して形成されている。なお、このダミー電極２２ａ，２２ｂは画素電極２２と同様にＩＴＯにて形成される。

【００３６】そのため、本第２の実施の形態においては、上述したようなブラシスクラバを用いた基板２１の洗浄の際、図８に示されるように、そのブラシ４ａは、ダミー電極２２ａからダミー電極２２ｂの表面の傾斜に沿うようにして画素電極２２上に乗り上げるようになる。このため、本第２の実施の形態によっても、回転するブラシ４ａの機械的な力によって画素電極２２が損傷することは好適に防止されるようになる。

【００３７】次に、図９を参照して、上記ダミー配線２２ａ，２２ｂ及び画素電極２２の形成方法を説明する。これら膜材のパターン形成に際しては、まず図９（ａ）に示すように、透明絶縁基板２１ａ上にダミー電極２２ａ，２２ｂ及び画素電極２２となるＩＴＯ膜２２Ａを成膜する。次に、図９（ｂ）に示すように、透明絶縁基板２１ａの端部に形成されるＩＴＯ膜２２Ａの膜厚が、その中央部に形成されるＩＴＯ膜２２Ａに対して徐々に薄くなるように同ＩＴＯ膜２２Ａの表面をエッチングする。

【００３８】このエッチング方法としては、例えばプラズマを用いたドライエッチング法において、反応圧力を通常の圧力（約１８ｍＴｏｒｒ）より高く、例えば２０ｍＴｏｒｒとする方法が有効である。すなわちここでは、上記エッチングにかかるプラズマ反応圧力を高くすると、基板端ほど深く、いわばアンバランスにエッチングされることを積極的に利用する。

【００３９】続いて、図９（ｃ）に示すように、このエッチングされたＩＴＯ膜２２Ａ上に所定のレジストパターン６ｂを形成する。そしてＩＴＯ膜２２Ａをエッチングし、レジストパターン６ｂを剥離すると、図９（ｄ）に示されるように、画素電極２２及びダミー電極２２ａ，２２ｂが透明絶縁基板２１ａ上に形成されるようになる。

【００４０】以上説明したように、本第２の実施の形態によれば、以下のような効果を得ることができる。

（１）本第２の実施の形態では、ダミー電極２２ａ，２２ｂの膜厚が透明絶縁基板２１ａの外側に向かうにしたがい薄くなるように形成される。そのため同基板２１ａを例えばブラシスクラバを使用して洗浄する場合であれ、ブラシスクラバのブラシ４ａが画素電極２２と当接する際、同ブラシ４ａは好適に画素電極２２に乗り上がるようになる。そのため、回転するブラシスクラバのブラシ４ａの機械的な力によって画素電極２２が損傷することは好適に防止される。

【００４１】（２）本第２の実施の形態では、ダミー電極２２ａ，２２ｂが画素電極２２と同質のＩＴＯによってパターン形成される。そのため、画素電極２２をパターン形成する工程において一括してダミー電極２２ａ，２２ｂをパターン形成することができる。すなわち、ダミー電極２２ａ，２２ｂを形成するための別途マスク等は一切不要であり、その製造工数、製造コストを低く抑えることが可能となる。

【００４２】（３）本第２の実施の形態では、ダミー電極２２ａ，２２ｂの表面の傾斜を、画素電極２２の形成も含めたＩＴＯのエッチング工程において、プラズマ反応圧力を積極的に高めることにより形成した。すなわち、それらダミー電極２２ａ，２２ｂの表面の傾斜すら、何ら別途の工程を追加することなく形成することができる。

【００４３】なお、上記第２の実施の形態は以下のようにその構成を変更して実施することもできる。

・上記第２の実施の形態においては、画素電極２２のダミー膜として、同画素電極２２の外周を２重に囲むようにその膜厚に勾配を有するダミー電極２２ａ，２２ｂを形成する例を示したが、これに限定されない。この膜厚に勾配を有するダミー電極は画素電極２２の外周を１重に囲むように形成されるものであってもよい。

【００４４】・上記第２の実施の形態においては、画素電極２２のダミー膜として、その平面形状が画素電極２２と同一に形成されるダミー電極２２ａ，２２ｂを形成する例を示したが、これに限定されない。他に例えば、薄膜ダミー配線２２ａ，２２ｂの平面形状は２画素分の面積を有する平面形状としてもよいし、あるいは３画素分、４画素分の面積を有する平面形状としてもよい。また逆に、１画素分の面積よりも面積が小さくなる形状としてもよい。要は、画素電極２２と同一面積である必要はない。また、画素電極２２を含めてダミー電極２２ａ，２２ｂの材質がＩＴＯである必要はなく、構造的にはそれら画素電極２２及びダミー電極２２ａ，２２ｂが同一材料である必要もない。

【００４５】その他、先の第１の実施の形態も含めて、前記各実施の形態では、ダミー膜として形成される膜材（ダミー膜５やダミー電極２２ａ，２２ｂ）がいずれも画素電極（１２，２２）よりも膜厚が薄く形成される場合について例示したが、その限りでもない。すなわち、画素電極をそのブラシによる洗浄に伴う損傷から保護することができればダミー膜自体は損傷されてもよく、例えば画素電極と同一の膜厚にするなど、必ずしも画素電極より薄い膜厚とする必要はない。また、特にダミー膜が金属膜（Ａｌ等）にて形成され下地との密着性が良い場合にも、必ずしも画素電極より薄い膜厚とする必要はない。

【００４６】また、第１の実施の形態のダミー膜５にも、第２の実施の形態に示したダミー電極２２ａ，２２ｂのような勾配を設けてもよい。また、これらダミー膜５及びダミー電極２２ａ，２２ｂに勾配を設ける代わりに、それらの膜厚が装置外周に向かうにしたがって階段状に順次薄くなるように形成されるものとしてもよい。

なお、この膜厚が階段状に順次薄くなる態様は、複数のダミー膜によって階段状とされるものであってもよいし、単一のダミー膜上においても階段状とされものであってもよい。

【００４７】また、前記各実施の形態では、固体装置の最外周にパターン形成される膜材をダミー膜（ダミー膜５やダミー電極２２ａ）として形成する例を示したがその限りでもない。同膜材はダミー膜としてではなく、他に例えば電極等として形成されるものであってもよい。

【００４８】また、上記各実施の形態においては、本発明にかかる膜材がパターン形成された固体装置をポリシリコン形ＴＦＴ方式アクティブマトリックス液晶表示装置に適用した例を示したが、これに限定されない。他に例えば、同固体装置をアモルファスシリコン形ＴＦＴアクティブマトリクス液晶表示装置に適用してもよいし、パッシブマトリクス液晶表示装置に適用してもよい。さらに液晶表示装置に限定されず、例えば太陽電池セル等、薄膜電極が基板上にパターン形成されるものであれば同様にこの発明を適用することができる。そしてさらには、これら薄膜電極がパターン形成されるものに限らず、ＬＳＩ等の半導体装置にあっても、電極その他の膜材が基板表面にパターン形成され、その状態で前記ブラシスクラバ等による洗浄が行われる固体装置でさえあれば、やはり同様に本発明を適用することはできる。

【００４９】

【発明の効果】請求項１の発明によれば、固体装置を例えばブラシスクラバ等を使用してブラシ洗浄する場合、ブラシスクラバのブラシは前記パターン形成された膜材と当接する前にまずダミー膜に当接する。そのため、回転するブラシスクラバのブラシの機械的な力によって同膜材が損傷することは防止される。

【００５０】請求項２の発明によれば、同様にブラシ洗浄する場合、ブラシスクラバのブラシは、まず膜材の膜厚よりも薄くパターン形成されたダミー膜に乗り上げ段差を小さくしてから同膜材に乗り上がるようになる。そのため、回転するブラシスクラバのブラシの機械的な力によって同膜材が損傷することは好適に防止される。請求項３の発明によれば、同様にブラシ洗浄する場合、ブラシスクラバのブラシはダミー膜の勾配若しくは階段に沿って好適に膜材に乗り上がるようになる。そのため、回転するブラシスクラバのブラシの機械的な力によって同膜材が損傷することは好適に防止される。

【００５１】請求項４の発明によれば、前記ダミー膜の製造工程が簡略化される。請求項５の発明によれば、前記ダミー膜の設計等の自由度が高まる。請求項６の発明によれば、液晶表示装置にあって、透明絶縁基板表面のブラシ洗浄に伴う画素透明電極の損傷は好適に防止される。

【００５２】請求項７の発明によれば、膜材の段差が緩和されるため、ブラシ洗浄に伴う同膜材の損傷も好適に防止される。請求項８の発明によれば、膜材の段差が緩和されるため、ブラシ洗浄に伴う同膜材の損傷も好適に防止されるとともに、製造工数を増やすことなく勾配を有する膜材を得ることができる。

【図面の簡単な説明】

【図１】この発明にかかる固体装置の第１の実施の形態を示す部分平面図。

【図２】図１のＡ－Ａ線及びＢ－Ｂ線に沿った部分断面図。

【図３】第１の実施の形態の固体装置に対する洗浄の態様を示す部分断面図。

【図４】第１の実施の形態の固体装置の製造手順を示す断面図。

【図５】第１の実施の形態の他の実施の態様を示す部分平面図。

【図６】この発明にかかる固体装置の第２の実施の形態を示す部分平面図。

【図７】図６のＣ－Ｃ線及びＤ－Ｄ線に沿った部分断面図。

【図８】第２の実施の形態の固体装置に対する洗浄の態様を示す部分断面図。

【図９】第２の実施の形態の固体装置の製造手順を示す断面図。

【図１０】従来の固体装置（液晶表示装置）の平面構造を示す部分平面図。

【図１１】図１０のＸ－Ｘ線に沿った部分断面図。

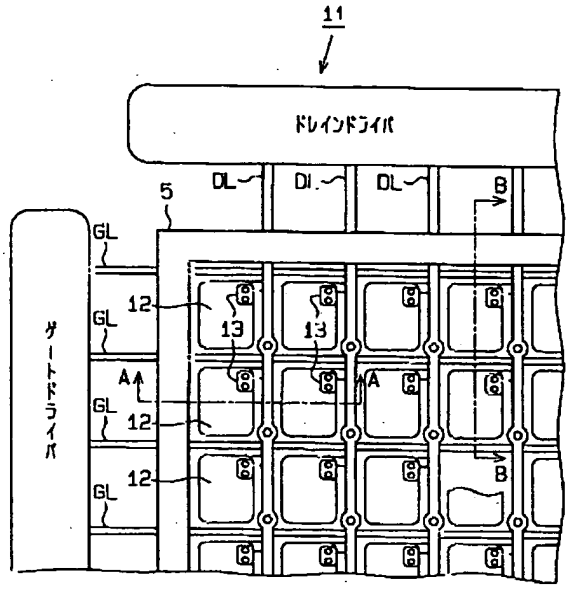
【図１２】ブラシスクラバによる基板洗浄態様を示す平面図。

【図１３】従来の固体装置に対する洗浄の態様を示す部分断面図。

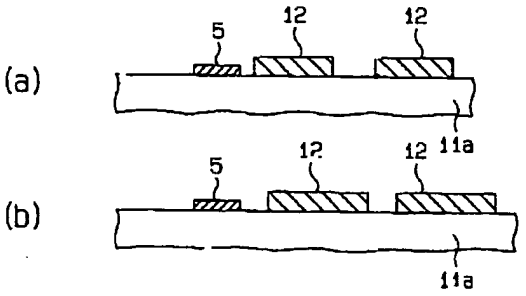
【符号の説明】

４ａ…ブラシスクラバのブラシ、５…ダミー膜、６，６ａ，６ｂ…レジスト膜、１１，２１…ＴＦＴアレイ側基板、１１ａ，２１ａ…透明絶縁基板、１２，２２…画素電極（ＩＴＯ薄膜電極）、２２ａ，２２ｂ…ダミー電極。

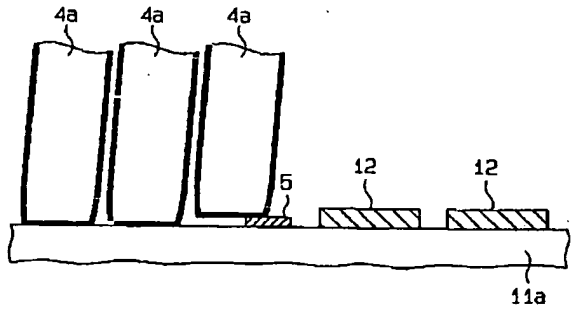
【図1】



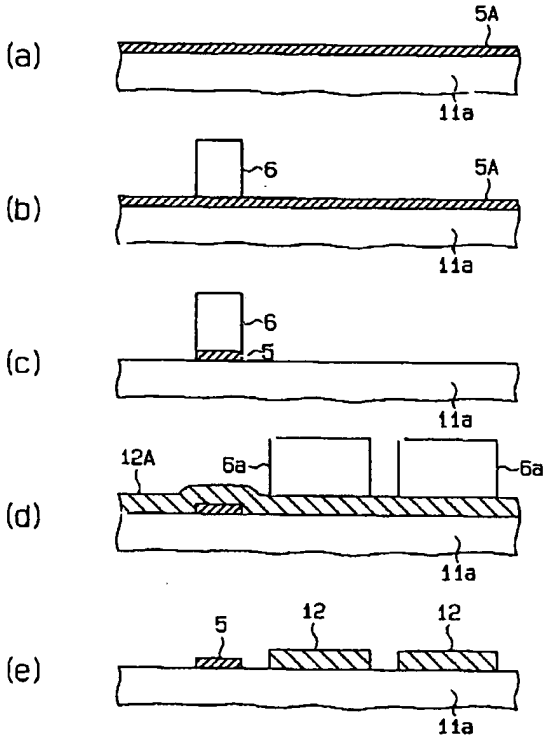
【図2】



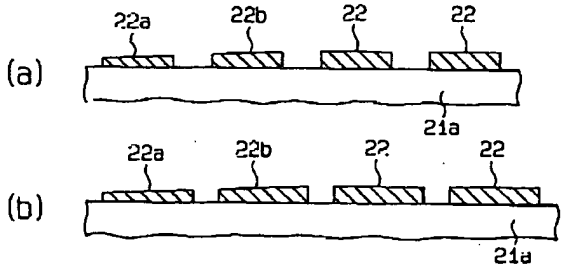
【図3】



【図4】



【図7】



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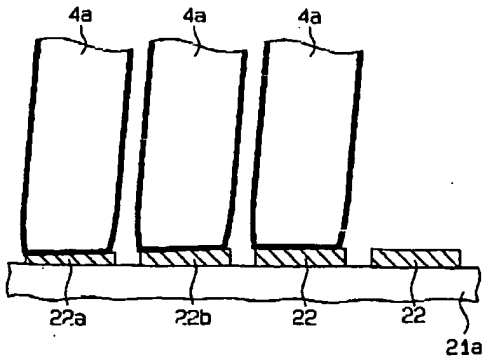
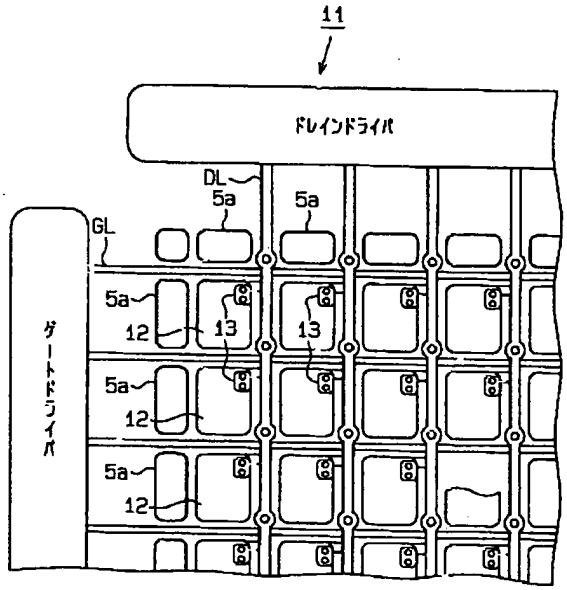
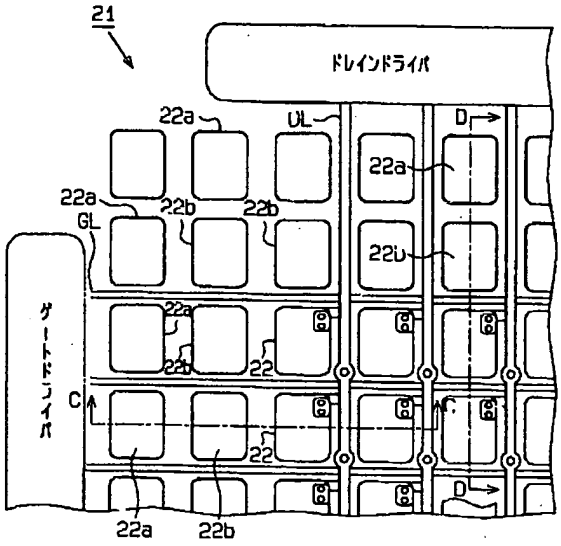


【図5】



【図6】



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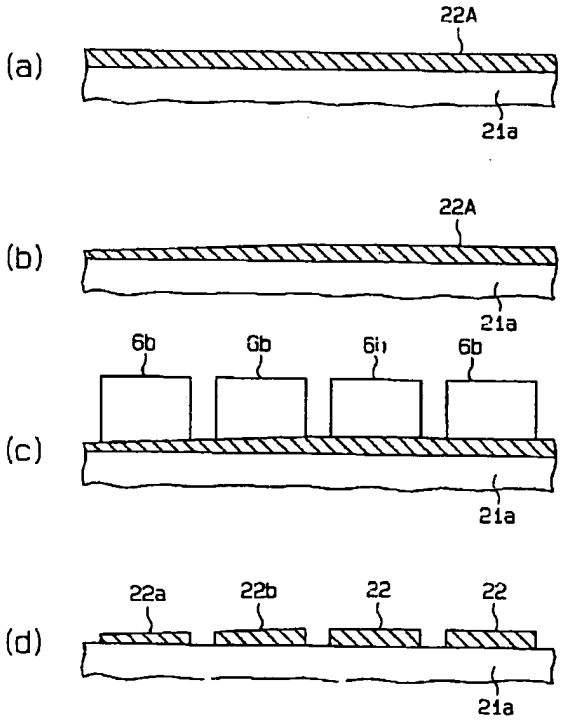
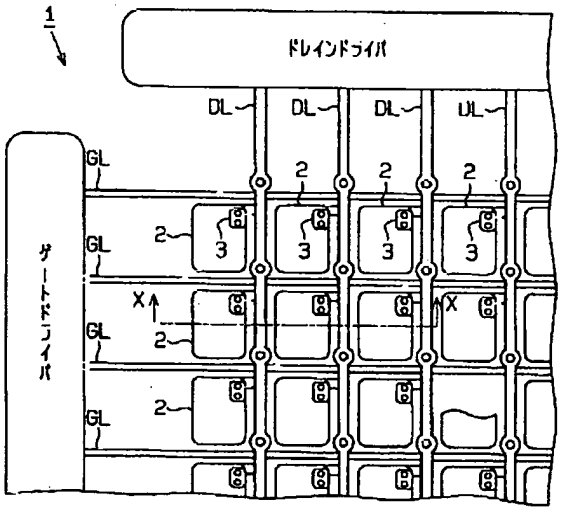
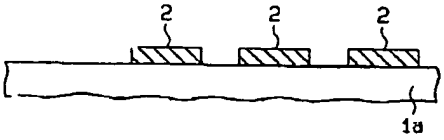


【図10】



【図11】



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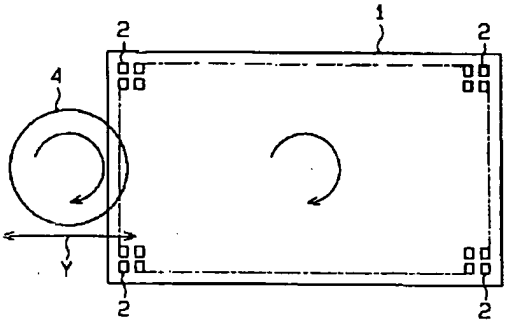
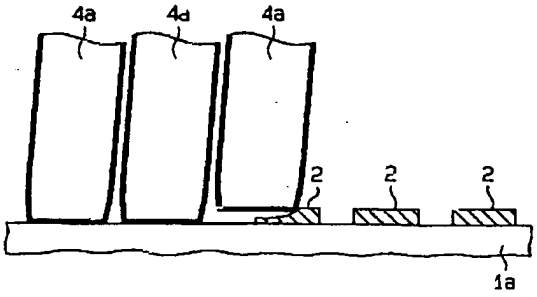


【図13】



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LIQUID CRYSTAL DISPLAY DEVICE

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[There are no amendments to this patent.]

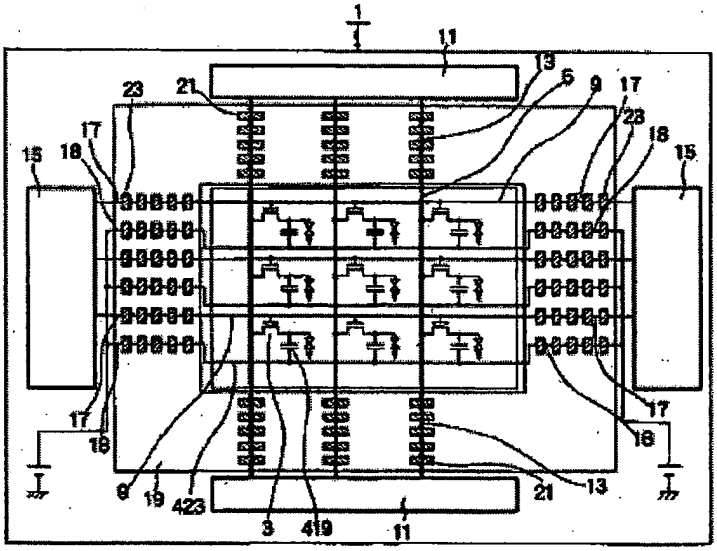
Abstract

Objective

To make the so-called cell gap between two opposing substrates of a liquid crystal display device uniform in order to provide image with good image quality and display contrast.

Constitution

Substrate gap adjusting region 33 or substrate gap adjusting layers 21, 23, 25, 27, 29, 31 used for keeping the gap between substrates uniform are arranged in the region where sealing material 19 is coated, that is, the region between driver circuits 11, 15 formed on the periphery of the substrates in a driver circuit integrated-type liquid crystal display element and the display region where the pixel electrodes 7 of the liquid crystal cells are arranged. In this way, the gap between the two opposing substrates that form the liquid crystal cells can be kept uniform at any position.



Claims

1. A liquid crystal display device comprising a switching element array substrate having switching elements, scanning lines and signal lines connected to said switching elements, and pixel electrodes connected to said switching elements, a scanning line driver circuit connected to said scanning lines, a signal line driver circuit connected to said signal lines, an opposing substrate having counter electrodes arranged opposite said pixel electrodes with a gap between

them to form a display region and bonded to said switching element array substrate with a sealing material formed around said display region, and an optical modulation layer sealed with said sealing material on its periphery and interposed in the substrate gap between said switching element array substrate and opposing substrate, characterized by the fact that

a substrate gap adjusting region that uniformly adjusts the substrate gap in the region between said display region and said scanning line driver circuit and the substrate gap in the region between said display region and said signal line driver circuit is formed in the region between said display region including the part covered with said sealing material and said scanning line driver circuit and/or the region between said display region and said signal line driver circuit.

2. A liquid crystal display device comprising a switching element array substrate having switching elements, scanning lines and signal lines connected to said switching elements, and pixel electrodes connected to said switching elements, a scanning line driver circuit connected to said scanning lines, a signal line driver circuit connected to said signal lines, an opposing substrate having counter electrodes arranged opposite said pixel electrodes with a gap between them to form a display region and bonded to said switching element array substrate with a sealing material formed around said display region, and an optical modulation layer sealed with said sealing material on its periphery and interposed in the substrate gap between said switching element array substrate and opposing substrate, characterized by the fact that

substrate gap adjusting layers that uniformly adjust the substrate gap in the region between said display region and said scanning line driver circuit and the substrate gap in the region between said display region and said signal line driver circuit is formed in the region between said display region including the part covered with said sealing material and said scanning line driver circuit and/or the region between said display region and said signal line driver circuit.

3. A liquid crystal display device comprising a switching element array substrate having switching elements, scanning lines connected to said switching elements, signal lines arranged to intersect said scanning lines, pixel electrodes connected to said signal lines, scanning line driver circuits arranged along the two edges at the two ends of the substrate so that they are connected to the two ends of said scanning lines, and signal line driver circuits arranged along two edges at the two ends of the substrate different from said two edges at the two ends of the substrate where said scanning line driver circuits are formed so that they are connected to the two ends of said signal lines, an opposing substrate having counter electrodes arranged opposite said pixel electrodes with a gap between them to form a display region and bonded to said switching element array substrate with a sealing material formed around said display region, and an optical modulation layer sealed with said sealing material on its periphery and interposed in the substrate

gap between said switching element array substrate and opposing substrate, characterized by the fact that

substrate gap adjusting layers that uniformly adjust the substrate gap in the region between said display region and said scanning line driver circuit and the substrate gap in the region between said display region and said signal line driver circuit is formed in the region between said display region including the part covered with said sealing material and said scanning line driver circuit and/or the region between said display region and said signal line driver circuit.

4. A liquid crystal display device comprising a switching element array substrate having switching elements, scanning lines connected to said switching elements, signal lines arranged to intersect said scanning lines, pixel electrodes connected to said signal lines, a scanning line driver circuit arranged along one edge of the substrate such that it is connected to one end of said scanning lines while the other end of the scanning lines is in an electrically open state, a signal line driver circuit arranged one edge away from said edge of the substrate along which said scanning line driver circuit is arranged such that it is connected to one end of said signal lines while the other end of the signal lines is in an electrically open state, an opposing substrate having counter electrodes arranged opposite said pixel electrodes with a gap between them to form a display region and bonded to said switching element array substrate with a sealing material formed around said display region, and an optical modulation layer sealed with said sealing material on its periphery and interposed in the substrate gap between said switching element array substrate and opposing substrate, characterized by the fact that

substrate gap adjusting region or substrate gap adjusting layers, which adjust the substrate gap between said switching element array substrate and said opposing substrate to a uniform gap that is equal in both directions parallel to one edge of said substrate along which said scanning line driver circuit is arranged and the direction parallel to one edge of said substrate along which said signal line driver circuit is arranged, are arranged along the direction parallel to one edge of said substrate along which said scanning line driver circuit is arranged and/or the direction parallel to one edge of said substrate along which said signal line driver circuit is arranged in the outer peripheral part of said display region including the part covered with said sealing material.

5. The liquid crystal display device described in any of Claims 1-4 characterized by the fact that

said substrate gap adjusting region or substrate gap adjusting layers are formed superimposed on said scanning lines and/or signal lines.

6. The liquid crystal display device described in any of Claims 1-4 characterized by the fact that

said substrate gap adjusting region or said substrate gap adjusting layers are formed along the scanning lines or signal lines.

7. The liquid crystal display device described in any of Claims 1-6 characterized by the fact that

at least one of the materials used for said liquid crystal display device is used as the material for forming said substrate gap adjusting layers.

8. The liquid crystal display device described in any of Claims 1-7 characterized by the fact that

the substrate gap adjusting layers formed in the region between said display region and scanning line driver circuit is formed using the material of said signal lines, whereas the substrate gap adjusting layers formed in the region between said display region and said signal line driver circuit is formed using the material of said scanning lines.

9. The liquid crystal display device described in any of Claims 1-8 characterized by the fact that

said substrate gap adjusting region or substrate gap adjusting layers are electrically insulated from said scanning lines and signal lines.

10. The liquid crystal display device described in any of Claims 1-9 characterized by the fact that

the substrate gap in said display region is adjusted uniformly by said substrate gap adjusting region or substrate gap adjusting layers.

Detailed explanation of the invention

[0001]

Industrial application field

The present invention pertains to a liquid crystal display device. In particular, the present invention pertains to a liquid crystal display device having a configuration, wherein two substrates are bonded to each other with a uniform gap between them.

[0002]

Prior art

In recent years, in order to increase the image processing speed of liquid crystal display devices and improve the display image quality, so-called active matrix type liquid crystal display devices where switching thin film transistors (referred to as TFTs hereinafter) are disposed corresponding to display picture elements (pixels) have been developed.

[0003]

Switching TFTs that contain amorphous silicon (a-Si) or polysilicon (poly-Si) have been widely used for such active matrix type liquid crystal display devices.

[0004]

In particular, poly-Si TFTs are easy to move and are incorporated as driver circuits with switching TFTs corresponding to pixels on the same substrate from the processing coordination standpoint. Thus, it is known that poly-Si is a structural material of TFTs suitable for active matrix type liquid crystal display devices, which should be small and have precise display characteristics.

[0005]

A switching element array substrate for use in a conventional active matrix type liquid crystal display device will now be described. Figure 9 is a plan view illustrating a switching element array substrate. Figure 10 is a cross-sectional view along A-A', illustrating signal lines of a portion covered with a sealing material. Figure 11 is a cross-sectional view along B-B', illustrating scanning lines of the portion covered with a sealing material. In order to simplify the explanation, in Figure 9, the pixel part of the liquid crystal cell has been simplified to 9 pixels. In addition to the elements shown in the figure, auxiliary capacitor Cs, auxiliary capacitor line connected thereto, and the like are also formed on a TFT substrate. However, they have been omitted from Figure 9 in order to simplify the explanation.

[0006]

As shown in Figure 9, each TFT 503 that is used as the switching element of the pixel part is formed on a switching element array substrate 501 of the liquid crystal display device. The drain of TFT 503 is connected to signal line 505, the source is connected to pixel electrode 507, and the gate is connected to scanning line 509.

[0007]

Signal line 505 extends to the outside of a display region surrounded with sealing material 511 through the portion covered with sealing material 511 and is connected to signal driver circuit 513. Scanning line 509 extends to the outside of a display region surrounded with sealing material 511 through the portion covered with sealing material 511 and is connected to scanning line driver circuit 515.

[0008]

As shown in Figure 10, which is a cross-sectional view along line A-A', the portion of signal line 505 covered with sealing material comprises interlayer insulating film 601 made of SiOx, for example, and formed on glass substrate 600, signal line 505 formed by patterning an Al/Cr film, and protective film 603.

[0009]

As shown in Figure 11, which is a cross-sectional view along B-B', the portion of scanning line 509 covered with sealing material 511 comprises scanning line 509 formed by patterning a polysilicon film formed on glass substrate 600 and doped with an impurity in order to reduce its resistance, interlayer insulating film 601, and protective film 603.

[0010]

Said switching element array substrate 501 and an opposing substrate (not shown in the figure) having counter electrodes made of ITO and having an alignment film formed on its surface are arranged opposite each other. Sealing material (acting as sealing material and adhesive) 511 is printed or coated with a prescribed width to cover part of signal line 505 in the region between signal line driver circuit 513 and the display region and a portion of scanning line 509 in the region between scanning line driver circuit 515 and the display region. A superimposition pressure is applied to the two substrates to bond them together with the alignment directions of the alignment films of the two substrates perpendicular to each other. A liquid crystal composition (not shown in the figure) is sealed/interposed as an optical modulating layer in the liquid crystal cell in the so-called vacant cell state formed by the gap between the two substrates and the sealing material. In this way, a liquid crystal display device is formed.

[0011]

Sealing material 511 used for bonding said two substrates is formed by mixing a spacer with a bonding agent. The spacer is made, for example, from a gap controlling element with the same diameter and length as the gap to be maintained for the substrates. For example, the spacer is made of needle-like glass fibers with a diameter of 5 μm and a length of 20 μm to 200 μm. The sealing material is printed or coated over the aforementioned region to keep the gap between the two substrates uniform.

[0012]

In the liquid crystal display device manufactured as described above, however, at the portion of each signal line 505, since the interlayer insulating film (0.45 μm), the Al/Cr dual

layer (0.8 μm/0.05 μm) and the protective film (0.3 μm) are formed, the thickness measured from the front surface of the substrate 600 covered with the sealing material 511 of the switching element array substrate 501 to the protective film 603 (i.e., the gap between the substrates) is 1.6 μm. On the other hand, at the portion of the scanning line 509, since the polysilicon film (0.4 μm), the layer insulating film (0.45 μm), and the protective film (0.3 μm) are formed, the thickness measured from the front surface of the substrate 600 covered with the sealing material 511 of the switching element array substrate 501 to the protective film 603 is 1.15 μm. The difference in thickness at these portions is 1.6 μm-1.15 μm = 0.45 μm. In other words, the gap variation of the substrates held by the sealing material 511 can be as high as approximately 10% of 5 μm, which is the gap between the substrates. The difference in thickness of the sealing material 511 at the two portions results in an on-screen deviation formed by the gap between the two substrates. Thus, the image displayed on the screen (display region) will be uneven. Specifically, the substrate gap in the vertical direction of the screen does not match the substrate gap in the horizontal direction of the screen. Thus, the two substrates are not positioned exactly parallel to each other. Therefore, serious display unevenness will occur.

[0013]

As described above, the difference between the height of the sealing material over the scanning lines 509 and the height of the sealing material over the signal lines 505 results from the differences in layer structure and film thickness. However, when TFTs are formed, the difference between the layer structure of the scanning lines 509 and the layer structure of the signal lines 505 is inevitable. In other words, scanning lines 509 and signal lines 505 are usually formed on different layers via interlayer insulating layer 601 to realize insulation. In each TFT 503, the gate (or gate electrode) is connected to the scanning line 509. The drain (or drain electrode) is connected to the signal line 505. The gate and drain of the TFT 503 are formed on different layers via a semiconductor layer. The processing conditions for these layers are remarkably different from each other regardless of whether the gate electrode is disposed over the semiconductor layer (i.e., a staggered structure) or below the semiconductor layer (i.e., a non-staggered structure). Thus, scanning lines 509 and signal lines 505 should be formed on different layers with different thickness. The thickness of the portion of the scanning lines 509 on which the sealing material is formed is necessarily different from the thickness of the portion of the signal lines 505 on which the sealing material is formed. In addition, the thickness of these portions varies during their fabrication processes.

[0014]

The length of the glass fibers is in the range of 20 μm to 200 μm and the end surfaces thereof are usually sharp. Thus, when the glass fibers are positioned over signal lines 505 and scanning lines 509 and bonded to them with applied pressure via protective film 603, the glass fibers occasionally damage the signal lines 505 and scanning lines 509.

[0015]

To obtain a high quality display image, color and contrast should be improved. Color unevenness takes place due to interference of light through the liquid crystal display panel because of the nonuniform gap between two substrates of the panel. In addition, the difference in the electric fields applied to the liquid crystal composition and the difference in the retardation result in uneven contrast and color unevenness. To obtain a multi-gradation display image and a high resolution display image, a liquid crystal composition that has a fast voltage-response characteristic is used. The light transmittivity of a liquid crystal composition with a fast voltage-response characteristic largely varies with the retardation. Thus, when the gap between the substrates is nonuniform, the retardation significantly varies. As a result, the nonuniformity of the brightness of the displayed image deteriorates significantly, which exerts a very adverse effect on the image display quality. In particular, in the case of a projection-type liquid crystal display device with three liquid crystal display devices, this problem can be very serious.

[0016]

For a display image quality of such a liquid crystal device, in reality, the variation of the gap between the two substrates should be decreased to around 0.1 μm or less. To realize high quality display images, problems that cause an image to be uneven other than fabrication errors should be eliminated.

[0017]

Problems to be solved by the invention

As described above, in the conventional liquid crystal display device, since the substrate gap at the portion where the scanning lines are covered with sealing material (namely, the thickness measured from the front surface of the substrate to the upper surface of the protective film over the scanning lines) differs from the substrate gap at the portion where the signal lines are covered with the sealing material (thickness measured from the front surface of the substrate to the upper surface of the protective film over the signal lines), the substrate gap determined by the height of the sealing material on the side where the scanning lines are arranged becomes different from the substrate gap determined by the height of the sealing material on the side

where the signal lines are arranged. As a result, uneven color, uneven contrast, and so forth take place in a display image, thereby degrading the display image characteristics.

[0018]

The objective of the present invention is to solve the aforementioned problem by providing a liquid crystal display device in which the gap between two substrates is uniform in order to improve the image quality and display contrast.

[0019]

Means to solve the problem

The present invention provides a liquid crystal display device comprising a switching element array substrate having switching elements, scanning lines and signal lines connected to said switching elements, and pixel electrodes connected to said switching elements, a scanning line driver circuit connected to said scanning lines, a signal line driver circuit connected to said signal lines, an opposing substrate having counter electrodes arranged opposite said pixel electrodes with a gap between them to form a display region and bonded to said switching element array substrate with a sealing material formed around said display region, and an optical modulation layer sealed by said sealing material on its periphery and interposed in the substrate gap between said switching element array substrate and opposing substrate, characterized by the fact that a substrate gap adjusting region that uniformly adjusts the substrate gap in the region between said display region and said scanning line driver circuit and the substrate gap in the region between said display region and said signal line driver circuit is formed in the region between said display region including the part covered with said sealing material and said scanning line driver circuit and/or the region between said display region and said signal line driver circuit.

[0020]

The present invention also provides a liquid crystal display device comprising a switching element array substrate having switching elements, scanning lines and signal lines connected to said switching elements, and pixel electrodes connected to said switching elements, a scanning line driver circuit connected to said scanning lines, a signal line driver circuit connected to said signal lines, an opposing substrate having counter electrodes arranged opposite said pixel electrodes with a gap between them to form a display region and bonded to said switching element array substrate with a sealing material formed around said display region, and an optical modulation layer sealed with said sealing material on its periphery and interposed in the substrate gap between said switching element array substrate and opposing substrate,

characterized by the fact that substrate gap adjusting layers that uniformly adjust the substrate gap in the region between said display region and said scanning line driver circuit and the substrate gap in the region between said display region and said signal line driver circuit is formed in the region between said display region including the part covered with said sealing material and said scanning line driver circuit and/or the region between said display region and said signal line driver circuit. The aforementioned substrate gap adjusting region or substrate gap adjusting layer may be any element that can keep the substrate gap in the region between said display region including the portion covered with said sealing material and said scanning line driver circuit equal to the substrate gap in the region between said display region and said signal line driver circuit. For example, an organic material with a high insulating property can be formed over the regions that are covered with the sealing material so that the substrate gap becomes equal. The sealing material that also serves as a bonding agent is thinly coated over the substrate so as to bond this substrate to the opposing substrate. Or part of the circuit structural elements of the liquid crystal driver circuits may be used as the substrate gap adjusting region or substrate gap adjusting layer. Or the lead-out wiring of the scanning lines that connects the scanning line driver circuits and the lead-out wiring of the signal lines that connects the signal line driver circuits may be formed as the substrate gap adjusting region or substrate gap adjusting layer. The height of the lead-out wiring of the scanning lines should be equal to the height of the lead-out wiring of the signal lines. The material of the scanning lines may be different from the material of its lead-out wiring. The material of the signal lines may be different from the material of its lead-out wiring. The material of the lead-out wiring of the scanning lines and the signal lines may be different from the material of the scanning lines and the signal lines.

[0021]

The present invention is also characterized by the fact that, in the aforementioned liquid crystal display device, said substrate gap adjusting region or substrate gap adjusting layers are formed superimposed with said scanning lines and/or signal lines. The substrate gap adjusting layer may be patterned over the scanning lines and signal lines so that the layer is parallel or perpendicular to the lines. The substrate gap adjusting layer may be formed with a straight or zigzag pattern. The substrate gap adjusting layer may be formed above or below the scanning lines and signal lines. In any case, when the substrate gap adjusting layer can keep the substrate gap at the regions between the display region and the scanning line driver circuit equal to the substrate gap at the regions between the display region and the signal line driver circuits, any layer sequence may be selected and any pattern may be used. Also, the substrate gap adjusting layer may be formed over the auxiliary capacitor lines and the like.

[0022]

The present invention is also characterized by the fact that, in the aforementioned liquid crystal display device, said substrate gap adjusting region or said substrate gap adjusting layers are formed along the scanning lines or signal lines. For example, the shape of the substrate gap adjusting layer may be columnar so that it does not interfere with the signal lines and scan lines. The substrate gap adjusting layer may be patterned parallel to the scanning lines and signal lines so as not to connect to the lines. In addition to the scanning lines and signal lines, the substrate gap adjusting layer may be patterned parallel to the auxiliary capacitor lines, for example.

[0023]

The present invention is also characterized by the fact that at least one of the materials used for the liquid crystal display device is used for the substrate gap adjusting layer.

[0024]

It is preferred that the materials used for the liquid crystal display device as described above be used since the substrate gap adjusting layers can be easily formed.

[0025]

The present invention is also characterized by the fact that the substrate gap adjusting layer that is formed in the region between the display region and the scanning line driver circuit is formed on the same layer and with the same material as the signal lines, whereas the substrate gap adjusting layer that is formed in the region between the display region and the signal line driver circuit is formed on the same layer and with the same material as the scanning lines. In this case, the material and shape of the substrate gap adjusting layer should be selected and formed so that no short circuits are formed between the scanning lines or between the signal lines by the substrate gap adjusting layer. For example, the substrate gap adjusting layer may be formed as an insulator using interlayer insulating film or the like. When the substrate gap adjusting layer is formed from a conductive material, it should be patterned so that it does not form short circuits between the adjacent scanning lines or signal lines.

[0026]

Consequently, according to the liquid crystal display device of the present invention, the substrate gap adjusting region or substrate gap adjusting layer may be electrically insulated from the aforementioned scanning lines and signal lines.

[0027]

According to the present invention, the substrate gap at the display region is adjusted by the substrate gap adjusting region or substrate gap adjusting layer to be uniform. In other words, since the substrate gap in the region between said display region and the scanning line driver circuit and in the region between the display region and the signal line driver circuit, that is, the substrate gap adjusting region, which includes the region covered with the sealing material, is kept uniform, the entire substrate gap that separates the two opposing substrates can be maintained to be uniform. In this case, the substrates should be less skewed and twisted. Therefore, according to the present invention, the substrate gap holding element (the so-called spacer) that has been used in the display regions of conventional apparatuses can be omitted, and the image quality can be improved.

[0028]

The present invention is particularly suitable for the so-called driver circuit incorporated type liquid crystal display device, wherein the scanning line driver circuits and signal line driver circuits are formed over the switching element array substrate that also has the scanning lines and signal lines, and the lead-out wiring extends from pixel portions in four directions. However, the present invention is not limited to this constitution. For example, in another possible constitution, one end of each scanning line is connected to a scanning line driver circuit and the other end is electrically open, and one end of each signal line is connected to a signal line driver circuit and the other end is electrically open, so that the other ends are not connected to lead-out wiring extending from the sealing material. In this case, substrate gap adjusting regions or substrate gap adjusting layers that adjust the substrate gap at the regions covered with the sealing material on the other side may be newly formed so as to keep the thickness of the substrate gap equal over the entire region of the sealing material.

[0029]

As the switching elements, three-terminal elements such as TFT (Thin-Film Transistors), two-terminal elements such as MIM (Metal-Insulator-Metal) may be preferably used.

[0030]

As the optical modulating layer, a liquid crystal composition, such as TN (Twisted Nematic) type or STN (Super Twisted Nematic) type, each of which has an optical modulating function, a polymer dispersing type in which a liquid crystal material is dispersed in a resin matrix, another polymer dispersing type in which a capsule-shaped liquid crystal material is contained in a resin, or the like may be preferably used.

[0031]

Operation

When the substrate gap adjusting region or substrate gap adjusting layer that maintains the substrate gap in the region covered with the sealing material, that is, in the region where the sealing material is formed between the driver circuit part and the liquid crystal cell part formed at peripheral portions of the substrate for the driver circuit incorporated liquid crystal display device, the gap between the two substrates can be maintained to be uniform in all locations.

[0032]

Specifically, when the substrate gap at the signal lines and the substrate gap at the scanning lines in the portion covered with the sealing material are kept equal, the substrate gap in the direction that the scanning lines extend and the substrate gap in the direction that the signal lines extend (the longitudinal and lateral directions of the substrate) between the two opposing substrates can be held uniform over the entire surface of the liquid crystal cells. Thus, uneven color and uneven contrast can be suppressed over the entire surface of the liquid crystal cells, and a high quality display image can be obtained.

[0033]

Application examples

In the following, an application example of the liquid crystal display device of the present invention will be explained in detail based on figures.

[0034]

Application Example 1

Figure 1 is a plan view illustrating the TFT array substrate of the liquid crystal display device disclosed in the present invention. Figure 2(a) is an enlarged plan view illustrating the structure in the vicinity of the signal lines in the region between the display region and the signal line driver circuit. Figure 2(b) is its cross-sectional view along C-C'. Figure 3(a) is an enlarged plan view illustrating the construction in the vicinity of the scanning lines in the region between the display region and the scanning line driver circuit. Figure 3(b) is its cross-sectional view along D-D'. Figure 4(a) is an enlarged view illustrating the pixel portion of the liquid crystal display device disclosed in the present invention. Figure 4(b) is its cross-sectional view along line E-E'. In Figures 2 and 3, elements in the plan views that are made of the same material have been cross-hatched for better comprehension. In the figures and explanations of the individual application examples, for the sake of simplicity of description, the pixel portion inside liquid

crystal cell has been simplified to 9 pixels. Also, the profile line of the opposing substrate positioned opposite the TFT array substrate is nearly the same as the outer profile line of the sealing material. For the sake of simplicity, the illustration and description of the opposing substrate for each application example will be omitted.

[0035]

As shown in Figure 1, TFTs 3 are formed as switching elements in the display region on TFT array substrate 1 of the liquid crystal display device. The drain 411 of each TFT 3 is connected to a signal line 5 through a contact hole 417. The source 409 is connected to a pixel electrode 7 through a contact hole 415 and a conductive pattern. The gate 405 is connected to a scanning line 9. Signal lines 5 that apply a predetermined image signal voltage are connected to a signal line driver circuit 11 that sequentially drives signal lines 5 through lead-out wiring portions 13 of the signal lines 5. Scanning lines 9 that apply a scanning voltage (scanning pulse) that turns on/off TFT 3 to the gate 405 of each TFT is connected to a scanning line driver circuit 15 that sequentially drives the scanning lines through lead-out wiring portions 17. Said signal line 5 is incorporated with its lead-out wiring portion 13. Lead-out wiring portion 13 essentially extends from signal line 5. Likewise, the scanning line 9 is incorporated with its lead-out wiring portion 17. Lead-out wiring portion 17 essentially extends from scanning line 9.

[0036]

Substrate gap adjusting elements 21, 23 are formed in the regions where the lead-out wiring portions 13 of signal lines 15 and the lead-out wiring portions 17 of scanning lines 9 are covered with sealing material 19.

[0037]

Each substrate gap adjusting layer 21 is made of the same film as the lead-out wiring portion 17 of scanning line 9 and patterned over the lead-out wiring portion 13 of signal line 5. Likewise, each substrate gap adjusting layer 23 is made of the same film as the lead-out wiring portions 13 of signal line 5 and patterned over the lead-out wiring portions 17 of signal line 9.

[0038]

As shown in the cross-sectional view in Figure 2(b), the structure in the vicinity of the lead-out wiring portion 13 of signal line 5 comprises the substrate gap adjusting layer 21 made of a patterned polysilicon film formed on a glass substrate 200 and doped with an impurity in order to reduce its resistance, an interlayer insulating film 201, the lead-out wiring portion 13 of signal

line 5 formed by patterning an Al/Cr film, and a protective film 205 formed in that order from the bottom.

[0039]

On the other hand, as shown in the cross-sectional view in Figure 3(b), the structure in the vicinity of the lead-out wiring portion 17 of scanning line 9 comprises the lead-out wiring portion 17 of scanning line 9 made of a patterned polysilicon film formed on a glass substrate 200 and doped with an impurity in order to reduce its resistance, an interlayer insulating film 201, the substrate gap adjusting layer 23 formed by patterning an Al/Cr film, and a protective film 205.

[0040]

Thus, both the layer structure in the region in the vicinity of the lead-out wiring portion 13 of signal line 5 and the layer structure in the region in the vicinity of the lead-out wiring portion 17 of scanning line 9 are formed by laminating the low-resistance polysilicon film doped with an impurity, the interlayer insulating film, the Al/Cr film, and the protective film in that order from the bottom on glass substrate 200. Thus, although the layer structures are formed with different patterns, since they are otherwise the same as described above, the overall thicknesses t1, t2 from the substrate surface are equal except for fabrication errors. As a result, the difference between t_1, which is the thickness of the lead-out wiring portion 13 of the signal line 5, and t_2, which is the thickness of the lead-out wiring portion 17 of the scanning line 9 can be restrained to 0.1 μm or less.

[0041]

The TFT array substrate 1 and the opposing substrate (not shown in the figure) that has counter electrodes made of ITO and an alignment film are positioned facing each other. A sealing material (that also serves as a bonding agent) is printed over the lead-out wiring portions 13 of the signal lines 5, which are connected to signal line driver circuit 11, and over the lead-out wiring portions 17 of the scanning lines 9, which are connected to scanning line driver circuit 15. The two substrates are pressed against each other to be bonded together, with the alignment directions of the alignment films on the two substrates perpendicular to each other. A liquid crystal composition as an optical modulation layer (not shown in the figure) that has positive dielectric anisotropy is filled in so-called empty cells defined by both the substrates and sealing material 19. In this manner, the liquid crystal display device is formed.

[0042]

Next, a fabrication method of the said TFT array substrate 1 will be described. An amorphous silicon film that becomes active layer 401 of TFT channel regions for switching elements and the active layer of TFT that forms the driver circuits (not shown in the figure) is formed over a quartz substrate as a transparent insulating substrate. The amorphous silicon film is made by low-pressure CVD. The amorphous silicon film is converted to a polysilicon film by means of solid-state growth performed at 600° C for 24 h, followed by patterning.

[0043]

Next, a gate insulating film 403 is formed by thermal oxidization. Then, a second low-resistance polysilicon film is formed by low-pressure CVD. This second polysilicon film is used to form the gates 405 of the TFTs, the scanning lines 9 and its lead-out wiring portions 17, and the substrate gap adjusting elements 21.

[0044]

As an n-type dopant, P (phosphorous) is injected by means of ion injection on both sides of gate 405 to lower the resistance to form source 409, drain 411 of TFT 3.

[0045]

An interlayer insulating film 201 is formed by low-pressure CVD, and contact holes 415 and 417 are formed thereon.

[0046]

Each auxiliary capacitor 419, which is a MOS capacitor, is integrated with active layer 401 and is formed between part of pixel electrode 7 and interlayer insulating film 201 with overlying auxiliary capacitor line 423. In this way, the capacitor is formed as auxiliary capacitor Cs connected in parallel with the pixel. The auxiliary capacitor line 423 is formed integrally using the same material in the same layer as the lead-out wiring portion 18 in a region covered by the sealing material 19. The auxiliary capacitor line 423 (and its lead-out wiring portion 18) may be formed in the same manner as a conventional auxiliary capacitor line by patterning the film used for gate 405 in the same step of forming gate 405. Alternatively, despite the disadvantage that the film forming steps and the like are increased, the auxiliary capacitor line 423 and the lead-out wiring portion 18 may be formed from another material than that used for the gate 405. Although the number of film forming steps is increased, the material of the auxiliary capacitor lines 423 and its lead-out wiring portions 18 may be formed from another

material than that used for gate 405. The material of the auxiliary capacitor lines 423 or its lead-out wiring portions 18 may be different from the material of gate 405.

[0047]

The drain 411 of TFT 3 is connected to signal line 5 through contact hole 417, and source 409 is connected to pixel electrode 7 through contact hole 415 and an electroconductive pattern. Gate 405 is connected to scanning line 9. Said signal line 5 has a two-layer structure of Al/Cr. It is formed to connect to signal line driver circuit 11 through lead-out wiring portion 13 that extends signal line 5. Also, scanning line 9 made of a low-resistance polysilicon film doped with an impurity is connected to scanning line driver circuit 15 through the lead-out wiring portion 17 of the scanning line.

[0048]

Substrate gap adjusting layers 23, 21 formed with the same overall thickness from the substrate surface are formed as a layer of polysilicon film formed from the same material as scanning line 9 on lead-out wiring portion 13 of signal line and as a layer of Al/Cr film formed from the same material as signal line 5 on the lead-out wiring portion 17 of scanning line 9, as shown in Figures 2 and 3, at least partially over the two different lead-out wiring portions, respectively. Said substrate gap adjusting layers are formed to be larger than the width of each lead-out wiring portion and of appropriate size so that they are not connected to the adjacent lead-out wiring portions.

[0049]

Said substrate gap adjusting layers 21, 23 can be formed in a linear pattern as shown in Figure 2 or in a zigzag pattern as shown in Figure 3.

[0050]

Protective film 205 made of SiNx is formed as the top layer of the various patterns to cover said patterns.

[0051]

A polyimide film is formed along with an opposing substrate (not shown in the figure) on the surface of said TFT array substrate 1. The polyimide film is rubbed to align the film (not shown in the figure). Also, spacers (not shown in the figure) are distributed over the surface of the opposing substrate. A sealing material 19, prepared by mixing a photocuring epoxy-based adhesive and glass fibers as gap control material in a weight ratio of 0.1% with respect to the

adhesive, is applied to the area of each lead-out wiring portion except for the injection opening (not shown in the figure). Said sealing material 19 also acts as an adhesive. The two substrates are bonded together by irradiating UV (ultraviolet) light after alignment. It is also possible to use a thermosetting sealing material that can also act as adhesive as said sealing material 19.

[0052]

A liquid crystal composition (not shown in the figure) is then injected from the injection opening using a conventional method, and the injection opening is then sealed with a UV-curable resin to complete the liquid crystal display device.

[0053]

The liquid crystal display device manufactured this way can keep the gap between the two substrates uniform by forming substrate gap adjusting layers 21, 23 with the same overall thickness at least partially on each lead-out wiring portion. In particular, by keeping the thickness of the lead-out wiring portion 13 of signal line 5 equal to the thickness of the lead-out wiring portion 17 of scanning line 9, the substrate gap can be kept uniform along the scanning lines (lateral direction) and the signal lines (longitudinal direction) between the two opposing substrates. In this way, the positional color unevenness or contrast unevenness can be restrained in the display region (screen), and good display quality can be realized.

[0054]

Also, since the glass fibers are arranged by coating sealing material 19 on the lead-out wiring portion 13 of signal line 5 and the lead-out wiring portion 17 of scanning line 9 as described above, scanning line driver circuit 15 and signal line driver circuit 11 can be prevented from becoming damaged by the glass fibers in sealing material 19 as opposed to the conventional liquid crystal display device, wherein sealing material 19 is applied on scanning line driver circuit 15 or signal line driver circuit 11.

[0055]

It is also possible to prevent the occurrence of burning when voltage is applied from the aforementioned drive circuits to the liquid crystal as opposed to the case when only the outside of the scanning line or signal line is sealed with the sealing material.

[0056]

If the substrate gap adjusting layers 21, 23 of each of lead-out wiring portions 13, 17, 18 are formed wider than each of lead-out wiring portions 13, 17, 18 and not in contact with

adjacent lead-out wiring portions 13, 17, 18, even if a pattern dislocation occurs due to mask misalignment or the like during the fabrication process, said substrate gap adjusting layers 21, 23 can always be formed on lead-out wiring portions 13, 17, 18. Also, even if an interlayer short circuit occurs due to poor insulation of interlayer insulating layer 201 between lead-out wiring portions 13, 17, 18 and said substrate gap adjusting layers 21, 23, short circuits to other lead-out wiring portions can be prevented.

[0057]

When the substrate gap adjusting layers 21 and 23 are formed in a linear or zigzag pattern that has a plurality of rows, gap adjusting elements, such as glass fibers, can be easily formed on the plurality of substrate gap adjusting layers 21 and 23. Thus, the gap between the two substrates is made reliably uniform over a wider area.

[0058]

In the aforementioned application example, the substrate gap adjusting layers 21 and 23 formed on lead-out wiring portions 13, 17, 18 are applied to a four-layer structure consisting of a polysilicon film, a layer insulating film, an Al/Cr dual-layer film, and a protecting film. However, the present invention is not limited to this layer structure. In this application example, in addition to Al/Cr, as a material of the scanning lines, signal lines, and the like, for example, WSi_x, $MoSi_x$, or Al/Ti may preferably be used. In particular, when a silicide, such as WSi_x, is used, hillocks, which usually appear when Al or the like is used as the wiring material, can be advantageously suppressed. In addition, when another layer insulating film and ITO are interposed, for example, the Al/Cr dual-layer film and the protective film, not only can the gap between the substrates be made uniform, but also the signal lines made of the Al/Cr dual-layer film can be prevented from becoming damaged by the glass fibers.

[0059]

As a material used for forming gate electrodes, for example, doped p-Si containing an impurity for lowering resistance, WSi_x, or $MoSi_x$ may be preferably used. With such a material, the resistance of the electrode can be reduced.

[0060]

In this application example, the substrate gap adjusting layers 21 and 23 are formed, for example, in a linear pattern on the side of the lead-out wiring portion 13 of the signal line and in a zigzag pattern on the side of the lead-out wiring portion 17 of the scanning line. However, it should be noted that the present invention is not limited to these patterns. Instead, when the

substrate gap adjusting layers 21 and 23 formed over the respective lead-out wiring portions do not contact adjacent lead-out wiring portions, both the substrate gap adjusting layers 21 and 23 may be formed in a linear pattern or a zigzag pattern. Or, as opposed to this application example, a zigzag pattern can be adopted on the side of the lead-out wiring portions 13 of the signal lines, while a linear pattern is adopted on the side of the lead-out wiring portion 17 of the scanning lines.

[0061]

Moreover, the material of the substrate gap adjusting layers 21 and 23 is not limited to the material used in the liquid crystal display device of this application example. For example, the substrate gap adjusting layers 21 and 23 may be formed with an insulating material that is different from the material of scanning lines 9 and signal lines 5. With this insulating material, even if the substrate gap adjusting layers 21 and 23 contact adjacent scanning lines or adjacent signal lines due to pattern dislocation during fabrication, the occurrence of short-circuit defect can be prevented.

[0062]

However, if the substrate gap adjusting layers 21 and 23 are made of the material used for signal lines 5 or scanning lines 9 or the material used for the active layer of each TFT 3, the fabrication process and the construction of the liquid crystal display apparatus can preferably be simplified.

[0063]

In this application example, the widths of the substrate gap adjusting layers 21 and 23 are equal to or several times larger than those of the lead-out wiring portions 13, 17, and 18. However, the present invention is not limited to these widths. For example, the widths of the substrate gap adjusting layers may be equal to the width of sealing material 19.

[0064]

Moreover, in this application example, glass fibers are used as the material of the gap controlling element mixed with the sealing material. However, as long as the gap between the substrates can be kept uniform, it is also possible to use granular space controlling elements (such as micro-beads). Or, the mixing of the gap controlling elements, such as glass fibers, may be omitted.

[0065]

Since the liquid crystal display device disclosed in this application example with the aforementioned configuration can make the gap between two opposing substrates that is, the so-called cell gap, uniform, a high-quality, high-contrast display image can be realized.

[0066]

With three liquid crystal display panels disclosed in the aforementioned application example of the present invention, a projection type liquid crystal display device (the so-called projection type liquid crystal display device) having a light source, a light source color separation system, liquid crystal display panel, a color combination system, and a projection lens system that were disposed in this order was fabricated. With this device, the image display characteristics were studied. The experimental results showed that the device displayed images without color unevenness or uneven contrast.

[0067]

Forming the driver circuits on all four sides of the substrate and connecting the driver circuits to both ends of the scanning lines and the signal lines, as in the liquid crystal display device disclosed in the first application example, provides redundancy. Thus, even if one driver circuit malfunctions, the other driver circuit can work to ensure normal driving. When both driver circuits are operated, distortion and inadequate brightness, due to a reduction in the amplitude of the scanning voltage waveform or signal voltage waveform, can be prevented. In this case, since the driver circuits are not covered with the sealing material or the opposing substrate, a defect in the liquid crystal display device can be advantageously repaired with a laser, for example.

[0068]

Application Example 2

Figure 5 is a plan view illustrating the liquid crystal display device disclosed in the second application example. For simplicity, the same parts as those in the first application example are represented by the same symbols and their detailed description is omitted. Thus, only the feature unique to the second application example will be described.

[0069]

The liquid crystal display device disclosed in the second application example has the following features: in the region approximately covered with sealing material 19 between the display region where pixel electrodes 7 are arranged on the inner side surrounded by sealing

material 19 and scanning line driver circuit 15, substrate gap adjusting layer 25 is formed by patterning along the lead-out wiring portions 17 of scanning lines 9 and the lead-out wiring portions 18 of auxiliary capacitor lines 423, and substrate gap adjusting layer 27 is formed and patterned along the narrow portions between the lead-out wiring portions 13 of signal lines 5.

[0070]

When both substrate gap adjusting layers 25 and 27 are made from the same materials that were used to make the liquid crystal display device, the formation process and construction of substrate gap adjusting layers 25 and 27 can be simplified since the subsequent step for forming the substrate gap adjusting layers from a different material can be omitted.

[0071]

For example, in this application example, both substrate gap adjusting layers 25 and 27 are made from the same materials that were used in the first application example. In other words, by using the material for forming scanning lines 9 (and its lead-out wiring portions 17), signal lines 5 (and its lead-out wiring portions 13), interlayer insulating film 201, and [sic; or] protective film 205, the height of the substrate gap adjusting layer 25 formed on the side of the lead-out wiring portion 17 of each scanning line 9 measured from the top surface of substrate 200 will be equal to the height of the substrate gap adjusting layers 27 formed on the side of the lead-out wiring portion 13 of each signal line 5 measured from the top surface of substrate 200. The substrate gap adjusting layers 25 and 27 are formed so that they are higher than the other structural portions, such as the TFT 3, storage capacitors 419, and storage capacitor lines 423. Thus, the substrate gap adjusting layers can support the lead-out wiring portions 17 of the scanning lines 9 and the lead-out wiring portions 13 of the signal lines 5 at the same height.

[0072]

The layer constructions and materials of scanning lines 9, the lead portions 17 of scanning lines 9, signal lines 5, the lead portions 13 of signal lines 5, TFT 3, auxiliary capacitor lines 423, sealing material 19, scanning line drive circuits 15, and signal line drive circuits 11 are the same as those in the first application example.

[0073]

According to the liquid crystal display device of the second application example, since the gap between the two opposing substrates, that is, the cell gap, is uniform, high-quality, high-contrast image display can be realized.

[0074]

The materials that can be used are not limited to those used in this application example. For example, other materials, different from those used for the liquid crystal display device, may be used for substrate gap adjusting layers 25 and 27 to form substrate gap adjusting layers 25, 27 in single layers. In this case, since the thickness of substrate gap adjusting layers 25 and 27 is larger than that of other structural portions, materials that can be easily formed and whose thickness can be easily controlled should be selected.

[0075]

In the second application example, the substrate gap adjusting layers are formed both on the side of the lead-out wiring portions 17 of scanning lines 9 and on the side of the lead-out wiring portions 13 of signal lines 5. However, the present invention is not limited in this way, since they may be formed on just one side. In this case, the substrate gap adjusting layers are formed on the side on which the heights of other structural portions are lower in the region covered with sealing material 19, and the height of these layers is brought up flush with the higher side.

[0076]

In this application example, substrate gap adjusting layers 25 and 27 are formed appropriately so that they are not in contact with the lead-out wiring portions 13, 17, and 18 at all. However, the present invention is not limited to this structure, since the substrate gap adjusting layers 25 and 27 may be formed alongside and in contact with [one of] the lead-out wiring portions 13, 17, and 18. The substrate gap adjusting layers 25 and 27 may be formed in the same pattern so long as they do not bridge the adjacent lead-out wiring portions 13, 17, and 18. That is the patterns of the substrate gap adjusting layers 25 and 27 of the second application example may be variously modified insofar as there are no interconnection between lead-out wiring portions 13, 17, and 18. For example, the substrate gap adjusting layers may be formed in long patterns alongside the lead-out wiring portions 13, 17, and 18.

[0077]

Application Example 3

Figures 6, 7 are plan views illustrating the liquid crystal display device disclosed in the third application example. In the explanation of the third application example and Figures 6, 7, for the sake of simplicity, the same parts as the first application example are represented by the same symbols. Only features that are unique to the third application example will be described.

[0078]

In the liquid crystal display device according to the third application example, lead-out wiring portions 17 of scanning lines 9 and lead-out wiring portions 18 of auxiliary capacitor lines 423 are formed by patterning a single layer of film made from a material different than scanning lines 9 and auxiliary capacitor lines 423, such as high-conductivity aluminum (Al), in the region covered by sealing material 19 between the display region where pixel electrodes 7 are formed on the inner side surrounded by sealing material and scanning line driver circuit 15. The lead-out wiring portions 17 and 18 are also used as substrate gap adjusting layers 29 in this application example. The lead-out wiring portions 13 connected to signal lines 5 are formed using a material different than signal lines 5, such as said Al, and said lead-out wiring portions 13 are also used as substrate adjusting layer 31.

[0079]

Both substrate gap adjusting layers 29 and 31 are formed to the same height from the top surface of substrate 200. Thus, the substrate gap on the side of the lead-out wiring portions 17 of scanning lines 9 and the substrate gap on the side of lead-out wiring portions 13 of signal lines 5 can be kept equal.

[0080]

The constructions and materials of other structural portions, such as scanning lines 9, the lead-out wiring portions 17 of scanning lines 9, signal lines 5, the lead-out wiring portions 13 of signal lines 5, TFT 3, auxiliary capacitor lines 423, sealing material 19, scanning line driver circuit 15, and signal line driver circuit 11 are the same as those of the first application example.

[0081]

In the liquid crystal display device disclosed in the second [sic; third] application example with the aforementioned configuration, since the gap between the two opposing substrates, that is, the cell gap, is kept uniform, a high-quality, high-contrast display image can be realized.

[0082]

The materials that can be used are not limited to those described above. The material of the substrate gap adjusting layers 29 and 31 is not limited to Al. Instead, they may be formed from three laminated layers of Cr/Mo/Cr. It is also possible to use p-Si with dopants injected so

as to lower the resistance. Examples of low-resistance materials are silicide compounds, such as WSi_x and $MoSi_x$.

[0083]

In the aforementioned application example, the substrate gap adjusting layers 29, 31 are formed both on the side of the lead-out wiring portions 17 of scanning lines 9 and on the side of the lead-out wiring portions 13 of signal lines 5. However, the present invention is not limited to this structure, since they may be formed on just one side. In this case, the substrate gap adjusting layers are formed on the side on which the heights of other structural portions are lower in the region covered with sealing material 19, and the height of these layers is brought flush with the higher side.

[0084]

In this application example, the lead-out wiring portions 13, 17, and 18 are formed as the substrate gap adjusting layers 29 and 31. However, the present invention is not limited to this structure, since, for example, the lead-out wiring portions 13 and 17 may be formed as substrate gap adjusting layers 29, 31 that are separated from signal line 5 and scanning line 9, respectively. In addition, the auxiliary capacitor lines 423 and the lead-out wiring portions 18 may be formed integrally on the same layer using the same material instead of being used as substrate gap adjusting layer 29. In other words, the substrate gap adjusting layers 29 and 31 are formed so that the substrate gap on the side of the lead-out wiring portions 13 of the scanning lines 9 is equal to the substrate gap on the side of the lead-out wiring portions 17 of the signal lines 5. Depending on the layer structure of the liquid crystal display device, only one of the lead-out wiring portions 13, 17, or 18 may be used as the substrate gap adjusting layer, or any two of said lead-out wiring portions may be used as the substrate gap adjusting layers.

[0085]

In the aforementioned application example, the planar patterns of the substrate gap adjusting layers 29 and 31 are formed with narrow lines whose width is similar to that of the lead-out wiring portions 13, 17, and 18. However, said patterns may be formed with a large width. In this case, however, substrate gap adjusting layers 29, 31 should be spaced apart from each other so as to prevent the occurrence of short circuits between them. In the third application example, since the substrate gap adjusting layers 29 and 31 are also used as the lead line portions 13, 17, and 18, said substrate gap adjusting layers 29, 31 are made of a conductive material. Thus, if the adjacent patterns are in contact with each other, they will short-circuit. Therefore, the patterns of the substrate gap adjusting layers 29 and 31 may be changed in various

ways as long as at least the adjacent lead-out wiring portions 13, 17, and 18 are formed so that they are not short-circuited to each other.

[0086]

In the third application example, a liquid crystal display device with driver circuits disposed on four sides of the peripheral portions of the substrate is shown. However, the present invention is not limited to this structure. Instead, the present invention may be applied to a liquid crystal display device with the structure shown in Figure 7. In this liquid crystal display device, a scanning line driver circuit 15 is disposed on one side of the peripheral portions of the TFT array substrate 1 and is connected to one end of each of the scanning lines 9. The other end of each of the scanning lines 9 is kept open. Likewise, the signal line driver circuit 11 is disposed on one of two sides perpendicular to the side of said scanning line driver circuit and is connected to one end of each of the signal lines 5. The other end of each of the signal lines 5 is kept open.

[0087]

In this case, lead line portions 13 in the region approximately covered with sealing material 19 formed between signal lines 5 and signal line driver circuit 11 and lead line portions 17 and 18 in the region nearly covered with sealing material 19 disposed between scanning lines 9 and scanning line driver circuit 15 are also used as the substrate gap adjusting layers 29 and 31 in the same way as described in the aforementioned application example. In this case, the substrate gap adjusting layers 30 and 32 that are similar to lead line portions 13, 17, and 18 may also be formed on the open end side of the signal lines 5 and scanning lines 9, respectively. The substrate gap adjusting layers 30 and 32 may be electrically connected to signal lines 5 and the scanning lines 9, respectively, or formed as so-called dummy patterns so that they are disconnected from the signal lines and the scanning lines. In the example shown in Figure 7, substrate gap adjusting layer 30 is incorporated with the signal lines and electrically connected thereto. On the other hand, substrate gap adjusting layer 32 is disconnected from scanning lines 9 but is incorporated with and electrically connected to auxiliary capacitor lines 423. Said substrate gap adjusting layers 30 and 32 may be electrically insulated from each other (or as patterns). In contrast, said substrate gap adjusting layers 30 and 32 may be electrically connected to each other (or as patterns).

[0088]

Thus, even in the liquid crystal display device with driver circuits connected to only one end of the scanning lines and signal lines, when substrate gap adjusting layers 30 and 32 are formed at the other end as described above, the gap between TFT array substrate 1 and the

opposing substrate can be kept uniform in the direction parallel to one edge of the substrate where scanning line driver circuit 15 is arranged and in the direction parallel to one edge of the substrate where signal line driver circuit 11 is arranged.

[0089]

The present invention is not limited to this structure. The scanning line driver circuits 15 may be disposed on both sides of the substrate so that they are connected to both ends of scanning lines 9. On the other hand, signal line driver circuit 11 may be disposed only on one side of the substrate so that it is connected to only one end of signal lines 5 while the other end is kept open. In this case, as shown in Figure 7, a dummy pattern with the same height as substrate gap adjusting layers 31 may be formed and used as substrate gap adjusting layer 30.

[0090]

Application Example 4

Figure 8 is a plan view illustrating the liquid crystal display device disclosed in the fourth application example. For the sake of simplicity, in the explanation of the fourth application example and Figure 8, the same parts as those in the first application example are represented by the same respective symbols. Only features unique to the fourth application example will be described.

[0091]

In the liquid crystal display device disclosed in the fourth application example, storage capacitors are formed outside the display region. In particular, the storage capacitors are formed in the region covered with sealing material.

[0092]

As shown in Figure 8(a), the region approximately covered with sealing material 19 between the display region where pixel electrodes are arranged on the inner side surrounded by sealing material 19 and scanning line driver circuit 15, and the region approximately covered with sealing material 19 between the display region where pixel electrodes are arranged on the inner side surrounded by sealing material 19 and signal line driver circuit 11 are substrate gap adjusting regions 33 that keep the substrate gap between the two opposing substrates uniform in both the longitudinal and lateral directions. More specifically, storage capacitor 35 is formed along lead-out wiring portion 13 in said substrate gap adjusting region 33. One end is connected to lead-out wiring portion 13, while a prescribed voltage is applied to the other end. The substrate gap on the side of the lead-out wiring portion 1 of signal line 5 is supported by the

height of said storage capacitor 35 from the top surface of substrate 200. Said storage capacitor 35 is used to adjust the substrate gap in said substrate gap adjusting region 33. On the other hand, said storage capacitor is used to keep the video signal voltage at an appropriate level for each of signal lines 5 to which a storage capacitor is connected.

[0093]

Said storage capacitors 35 may be formed inside or outside the display region other than the region covered with sealing material 19. It is also possible to form storage capacitors 35 in the driver circuits. However, when the auxiliary capacitors 35 are formed in the region covered with sealing material 19, as described in the aforementioned application example, storage capacitors 35 can also be used as the substrate gap adjusting layers. Thus, this application example is preferable from this standpoint.

[0094]

As shown in Figure 8(b), each of auxiliary capacitors 35 is formed in the following manner. A lower electrode 701 on the same layer and made of the same material as scanning line 9 or gate 405 is formed over substrate 200. An interlayer insulating film 201, which is a dielectric layer, is formed over the lower electrode. An upper electrode 703 is formed over dielectric layer 201 using the same material as signal lines 5 and its lead-out wiring portions 13. Thus, the interlayer insulating film 201, which is a dielectric layer, is sandwiched between the upper electrode 703 and the lower electrode 701. In this way, the main part of storage capacitor 35 is formed. A protective film 205 is formed to cover and protect the main part. When the main part of storage capacitor 35 is formed with the material of the liquid crystal display device as described above, the layer construction and the fabrication process can be advantageously simplified.

[0095]

The height of storage capacitors 35 from the top surface of substrate 200 is the same as the height of the part where the lead-out wiring portions 18 of the auxiliary capacitor line 423 is formed from the top surface of substrate 200. In other words, the layer structure of lead-out wiring portion 18 is comprised of the same material and has the same thickness as lower electrode 701, as interlayer insulating material 201, as upper electrode 703, or protective film 205, sequentially from the bottom in the same way as the layer construction of storage capacitor 35 shown in Figure 8(b), so that the height of storage capacitor 35 from the top surface of substrate 200 will be equal to the height of the highest portion in the layer construction of the lead-out wiring portion 18 of auxiliary capacitor line 423. In this case, the upper-layer portion of

lead-out wiring portion 18 formed with the same material and the same thickness as upper electrode 703 is not connected to an external power supply, unlike storage capacitor 35. Since its potential floats, the stray capacitance of said lead-out wiring portion 18 that may adversely affect the display (that is, poor brightness, delay, etc., due to the current passing through said lead-out wiring portion 18) is so small that it can be practically ignored.

[0096]

In this way, the substrate gap on the side of the lead-out wiring portion 17 of scanning line 9 can be kept equal to the substrate gap on the side of the lead-out wiring portion 13 of signal line 5.

[0097]

Otherwise, the structure and materials of scanning lines 9, the lead-out wiring portions 17 of scanning lines 9, signal lines 5, the lead-out wiring portions 13 of signal lines 5, TFT 3, the region covered by sealing material 19, scanning line driver circuits 15, and signal line driver circuits 11 are the same as those in the first application example.

[0098]

In the liquid crystal display device disclosed in the fourth application example, the substrate gap between the two opposing substrates, that is, the cell gap can be kept uniform. Therefore, a high-quality, high-contrast image display can be realized.

[0099]

In the aforementioned application example, storage capacitors 35 formed on the lead-out wiring portions 13 of signal lines 5 are used to adjust the substrate gap in substrate gap adjusting regions 33. However, the present invention is not limited to this configuration.

[0100]

Instead, part or all of signal line driver circuits 11 and scanning line driver circuits 15 formed on substrate 200 (namely, the so-called incorporated driver circuit type) are formed in the substrate gap adjusting region 33 covered with sealing material 19 so that the substrate gap on the side of the lead-out wiring portions 13 of signal lines 5 is kept equal to the substrate gap on the side of the lead-out wiring portions 17 of scanning lines 9 depending on the height of some or all of the structural portions of signal line driver circuit 11 and scanning line driver circuit 15.

[0101]

Alternatively, when storage capacitors 35 formed in the substrate gap adjusting region 33 as described above are used to adjust the support height of the substrate on the side of the lead-out wiring portions 13 of signal lines 5, the substrate gap is adjusted. On the other hand, when the substrate gap adjusting layers 23, 25, and 29 are formed on the side of the lead-out wiring portions 17 of scanning lines 9 as described in the aforementioned first to third application examples to adjust the support height of the substrate on the side of the lead-out wiring portions 17 of scanning lines 9, the substrate gap can be adjusted, and the substrate gaps on both sides can be adjusted to be equal. Moreover, the substrate gap adjusting layers 23, 25, and 29 may be formed not only on the lead-out wiring portions 18 of auxiliary capacitor lines 423 but also on both the lead-out wiring portions 17 of scanning lines 9 and the lead-out wiring portions 13 of signal lines 5.

[0102]

Thus, the substrate gap in substrate gap adjusting region 33 can be kept uniform both in longitudinal and lateral directions of the substrate.

[0103]

According to the present invention, since the gap between the two substrates can be kept uniform in the longitudinal and lateral directions by the substrate gap adjusting region or the substrate gap adjusting layers described in the conventional application examples, if the rigidity of the two substrates in the planar direction is high enough, the spacers of the conventional liquid crystal display device, which are arranged in the display region where the pixel electrodes are disposed, can be omitted. In the display region where the pixel electrodes are disposed, it is recommended not to place an element whose transmittivity is different from the liquid crystal regardless of whether the density of the element is low. Consequently, according to the present invention, since the spacers can be omitted, the image quality is improved.

[0104]

In the aforementioned first to fourth application examples, the active layers use so-called poly-Si TFTs made of polysilicon. However, it should be noted that the present invention can be applied to various structures using monocrystalline Si TFTs or a-Si TFTs as switching TFTs, staggered type TFTs, inverted-staggered type TFTs, two-terminal type devices such as MIM devices, or the like besides poly-Si TFTs.

[0105]

In addition, the scanning line driver circuits and the signal line driver circuits are formed simultaneously using p-Si in the same way as the switching TFTs. However, the driver circuits may also be solely made of monocrystalline Si. Or, for the driver circuits, a liquid crystal display driver LSI may be mounted on a glass substrate, using the COG (Chip On Glass) method.

[0106]

Although it is not shown in the figure, a second sealing material that is different from the aforementioned sealing material may be formed outside the driver circuits so as to protect the driver circuits from external humidity, temperature changes, and so forth to improve their durability.

[0107]

In the aforementioned application examples, the opposing substrate is smaller than the external size of the TFT array substrate. However, the present invention is not limited to this structure. When a plurality of liquid crystal display panels are formed on a large glass substrate, the external size of the opposing substrate may be greater than or equal to the size of the TFT array substrate so as to simplify the scribing process that is performed after the liquid crystal layer is injected between the two opposing substrates.

[0108]

In addition, needless to say, it is also possible to make various modifications to the materials used for forming each portion of the liquid crystal display device of the present invention without deviating from the essence of the present invention.

[0109]

As explained in detail above, according to the present invention, the substrate gap between the two opposing substrates in a liquid crystal display device (the so-called cell gap) can be kept uniform so that a high-quality, high-contrast image display can be realized.

Brief description of the figures

Figure 1 is a diagram illustrating the structure of the liquid crystal display device disclosed in the first application example.

Figure 2 is a diagram illustrating the structure in the vicinity of the lead-out wiring portion 13 of signal line 5 in the liquid crystal display device in the first application example.

Figure 3 is a diagram illustrating the structure in the vicinity of the lead-out wiring portion 17 of scanning line 9 in the liquid crystal display device in the first application example.

Figure 4 is a diagram illustrating the structure of one pixel portion in the liquid crystal display device in the first application example.

Figure 5 is a diagram illustrating the structure of the liquid crystal display device in the second application example.

Figure 6 is a diagram illustrating the structure of the liquid crystal display device in the third application example.

Figure 7 is a diagram illustrating the structure of the liquid crystal display device when the driver circuits are arranged on one side in the liquid crystal display device in the third application example.

Figure 8 is a diagram illustrating the structure of the liquid crystal display device in the fourth application example.

Figure 9 is a diagram illustrating the structure of a conventional liquid crystal display device.

Figure 10 is a diagram illustrating the structure in the vicinity of the lead-out wiring portion of signal line 505 in the conventional liquid crystal display device.

Figure 11 is a diagram illustrating the structure in the vicinity of the lead-out wiring portion of scanning line 509 in the conventional liquid crystal display device.

Explanation of symbols

1	TFT array substrate
3	TFT
5	Signal line
7	Pixel electrode
9	Scanning line
11	Signal line driver circuit
13	Lead-out wiring portion of signal line
15	Scanning line driver circuit
17	Lead-out wiring portion of scanning line
19	Sealing material
21, 23	Substrate gap adjusting elements

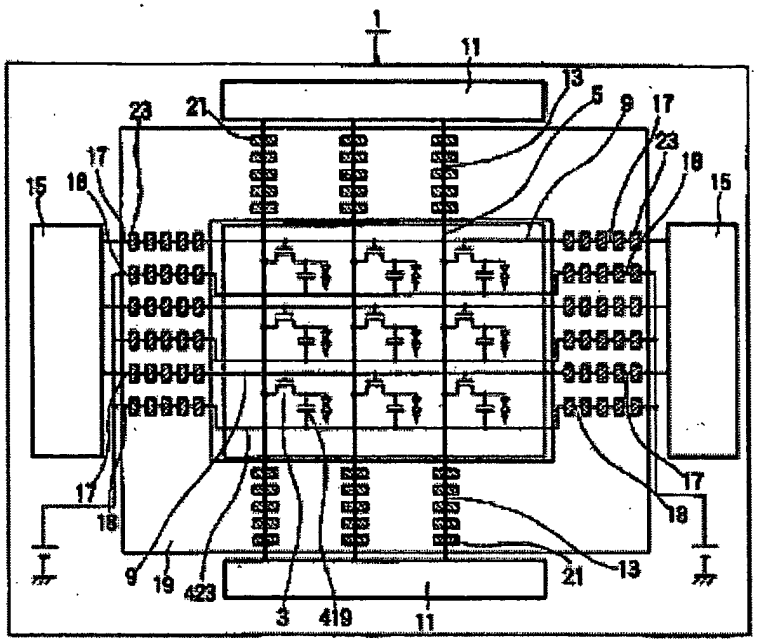


Figure 1

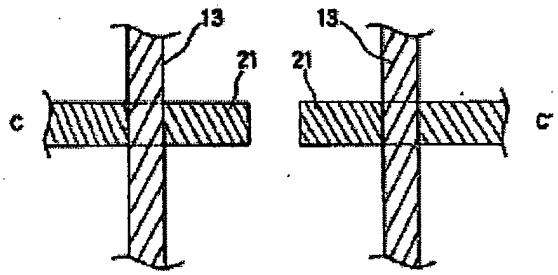


Figure 2(a) Enlarged view of the lead-out wiring portion of the signal line

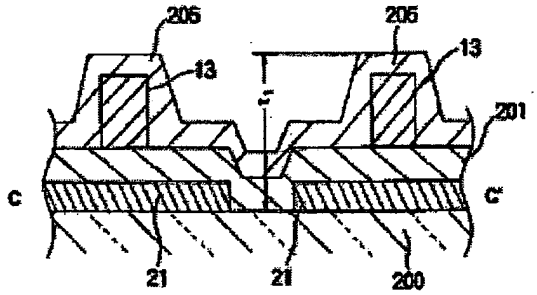


Figure 2(b) Cross-sectional view along C-C'

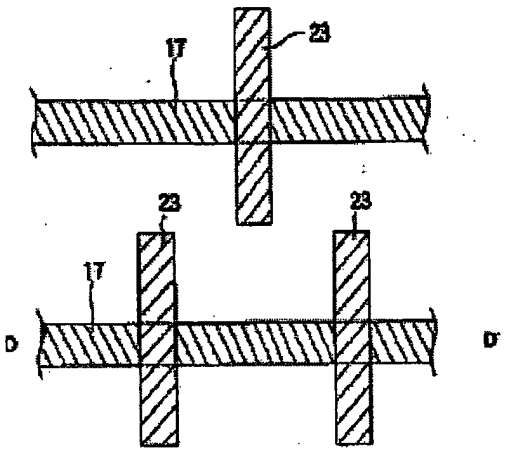


Figure 3(a) Enlarged view of the lead-out wiring portion of the scanning line

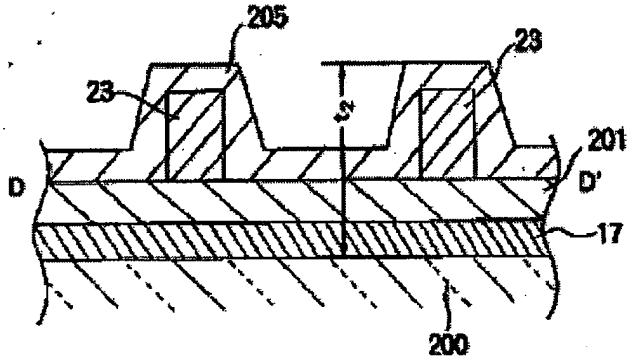


Figure 3(b) Cross-sectional view along D-D'

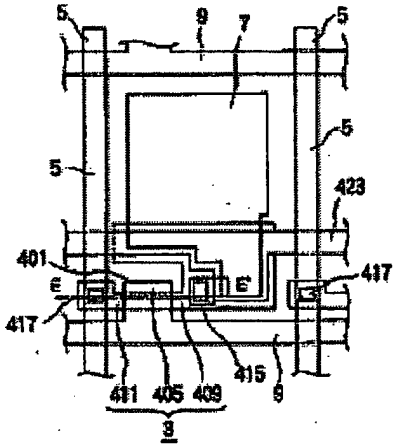


Figure 4(a) Plan view of the pixel portion

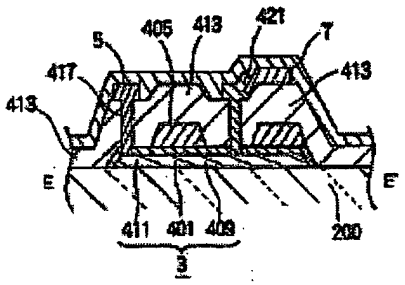


Figure 4(d) Cross-sectional view along E-E'

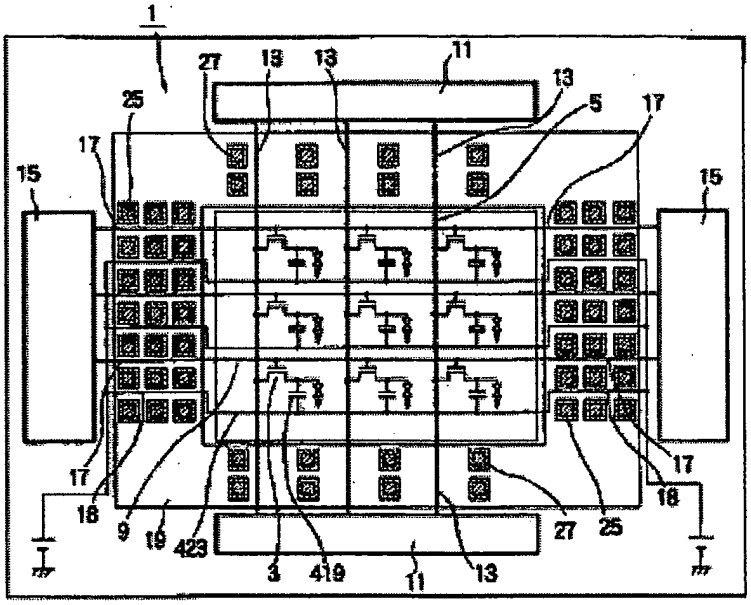


Figure 5

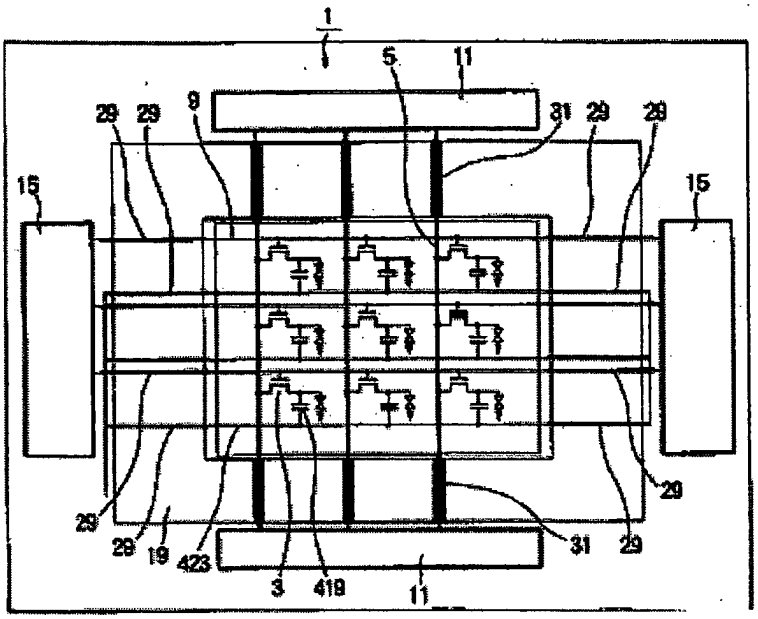


Figure 6

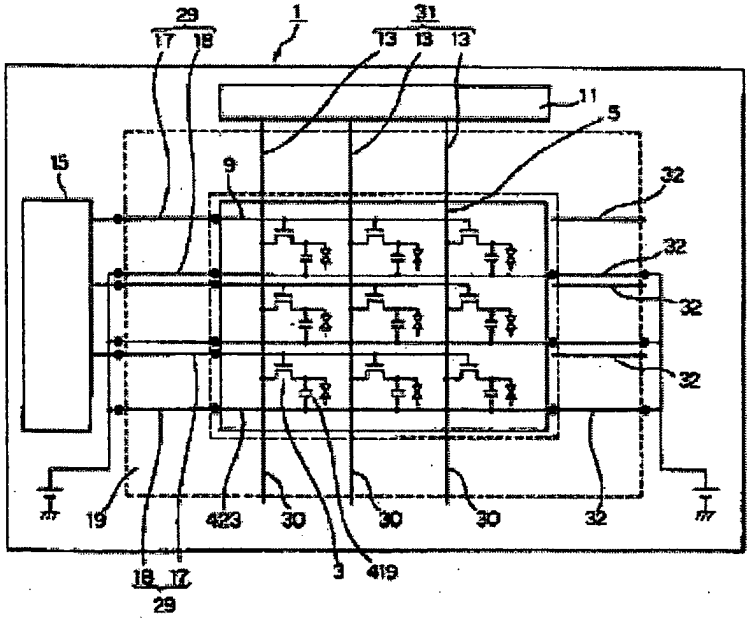
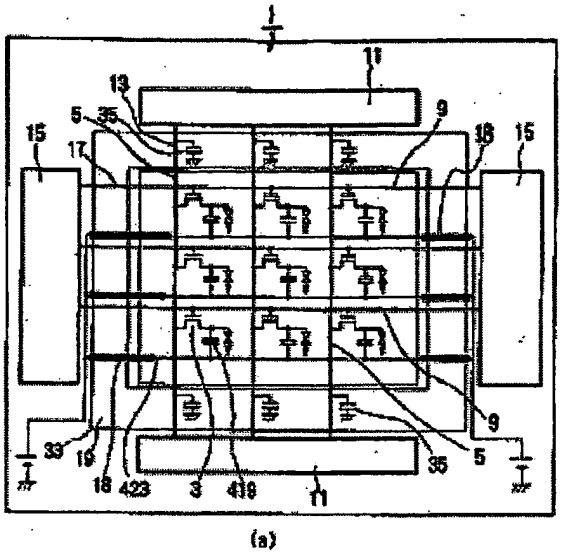
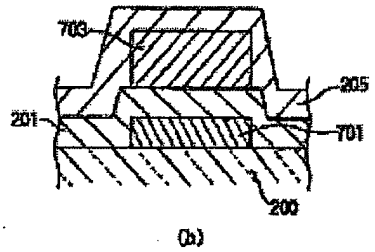


Figure 7



(a)



(b)

Figure 8

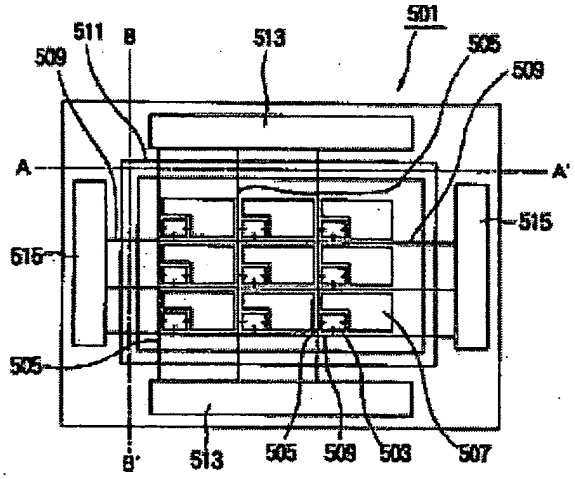


Figure 9

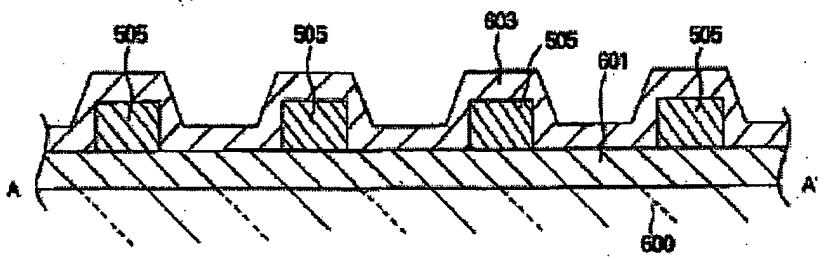


Figure 10

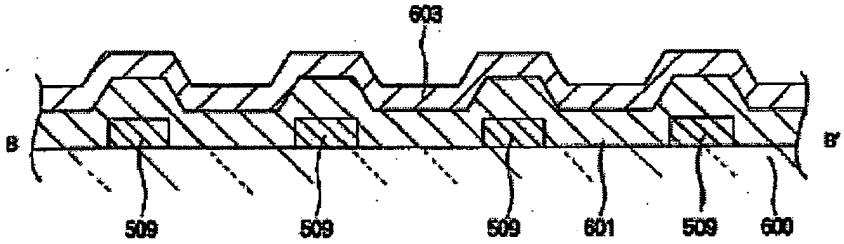


Figure 11

February 17, 2009

Re: 6774-119926

To Whom It May Concern:

This is to certify that a professional translator on our staff who is skilled in the Japanese language translated "JP06082811A" from Japanese into English.

We certify that the English translation conforms essentially to the original Japanese language.

Kim Vitray
Operations Manager

Subscribed and sworn to before me this 17th day of February, 2009.

VICKI L. WUNNEBURGER
Notary Public, State of Texas
My Commission Expires
March 09, 2011

Vicki Wunneburger
Notary Public

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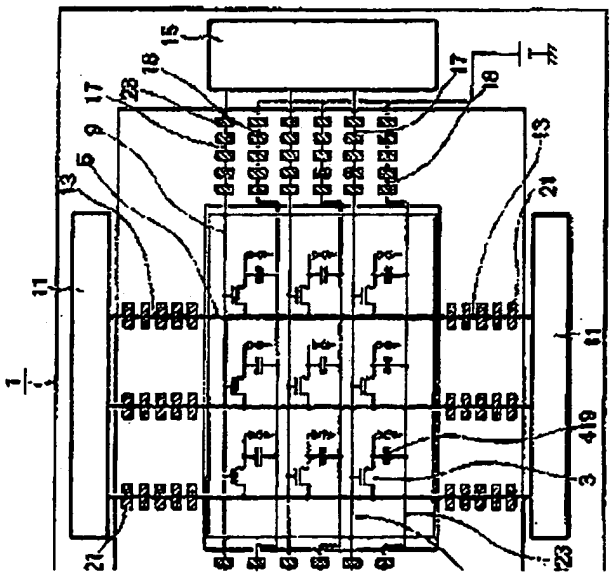
(54)【発明の名称】　液晶表示装置

(57)【要約】

【目的】　液晶表示装置において対向配置される２枚の基板間隙いわゆるセルギャップを均一化して、良好な画質や表示コントラストの画像表示を実現する。

【構成】　シール材１９が塗布される領域、つまり駆動回路一体型の液晶表示素子における基板周辺部に作り込まれた駆動回路部１１、１５と液晶セルの画素電極７が配列された表示領域との間の領域における基板間隙が等しくなるような基板間隙調整領域３３あるいは基板間隙調整層２１、２３、２５、２７、２９、３１を設けることで、対向配置されて液晶セルを形成する２枚の基板間隙をどの位置においても均一な間隙に保つことができる。



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【特許請求の範囲】

【請求項1】　スイッチ素子と前記スイッチ素子に接続された走査線および信号線と前記スイッチ素子に接続された画素電極とを有するスイッチ素子アレイ基板と、前記走査線に接続された走査線駆動回路と、前記信号線に接続された信号線駆動回路と、前記画素電極に間隙を有して対向配置され表示領域を形成する対向電極を有し前記表示領域の周囲に形成されたシール材によって前記スイッチ素子アレイ基板に接着された対向基板と、周囲を前記シール材によって封止され前記スイッチング素子アレイ基板と前記対向基板との基板間隙に挟持された光変調層とを有する液晶表示装置において、

前記表示領域と前記走査線駆動回路との間の領域における基板間隙と前記表示領域と前記信号線駆動回路との間の領域における基板間隙とを均一に調整する基板間隙調整領域を、前記シール材によって覆われる部分を含む前記表示領域と前記走査線駆動回路との間の領域および前記表示領域と前記信号線駆動回路との間の領域のうち少なくともいずれか一方の領域に設けたことを特徴とする液晶表示装置。

【請求項2】　スイッチング素子と前記スイッチング素子に接続された走査線および信号線と前記スイッチング素子に接続された画素電極とを有するスイッチング素子アレイ基板と、前記走査線に接続された走査線駆動回路と、前記信号線に接続された信号線駆動回路と、前記画素電極に間隙を有して対向配置され表示領域を形成する対向電極を有し前記表示領域の周囲に形成されたシール材によって前記スイッチング素子アレイ基板に接着された対向基板と、周囲を前記シール材によって封止され前記スイッチング素子アレイ基板と前記対向基板との基板間隙に挟持された光変調層とを有する液晶表示装置において、

前記表示領域と前記走査線駆動回路との間の領域における基板間隙と前記表示領域と前記信号線駆動回路との間の領域における基板間隙とを均一な間隙に調整する基板間隙調整層を、前記シール材によって覆われる部分を含む前記表示領域と前記走査線駆動回路との間の領域および前記表示領域と前記信号線駆動回路との間の領域のうち少なくともいずれか一方に設けたことを特徴とする液晶表示装置。

【請求項3】　スイッチング素子と前記スイッチング素子に接続された走査線および該走査線に交差するように配置された信号線と前記スイッチング素子に接続された画素電極と、前記走査線の両端にそれぞれ接続されるように基板両端の3辺に沿ってそれぞれ配置された走査線

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向電極を有し前記表示領域の周囲に形成されたシール材によって前記スイッチング素子アレイ基板に接着された対向基板と、周囲を前記シール材によって封止され前記スイッチング素子アレイ基板と前記対向基板との基板間隙に挟持された光変調層とを有する液晶表示装置において、

前記表示領域と前記走査線駆動回路との間の領域における基板間隙と前記表示領域と前記信号線駆動回路との間の領域における基板間隙とを均一な間隙に調整する基板間隙調整層を、前記シール材によって覆われる部分を含む前記表示領域と前記走査線駆動回路との間の領域および前記表示領域と前記信号線駆動回路との間の領域のうち少なくともいずれか一方に設けたことを特徴とする液晶表示装置。

【請求項4】　スイッチング素子と前記スイッチング素子に接続された走査線および該走査線に交差するように配置された信号線と前記スイッチング素子に接続された画素電極と、前記走査線の一端に接続されて該走査線の他端は電気的に解放状態となるように基板の1辺に配置された走査線駆動回路と、前記信号線の一端に接続されて該信号線の他端は電気的に解放状態となるように前記走査線駆動回路の配置された前記基板の1辺とは異なる向きの1辺に配置された信号線駆動回路とを有するスイッチング素子アレイ基板と、前記画素電極に間隙を有して対向配置され表示領域を形成する対向電極を有し前記表示領域の周囲に形成されたシール材によって前記スイッチング素子アレイ基板に接着された対向基板と、周囲を前記シール材によって封止され前記スイッチング素子アレイ基板と前記対向基板との基板間隙に挟持された光変調層とを有する液晶表示装置において、

前記スイッチング素子アレイ基板と前記対向基板との間の基板間隙を、前記走査線駆動回路の配置された前記基板の1辺と平行な方向と前記信号線駆動回路の配置された前記基板の1辺と平行な方向とで等しく均一な間隙に調整する基板間隙調整領域または基板間隙調整層を、前記シール材によって覆われる部分を含む前記表示領域の外周部のうち前記走査線駆動回路の配置された前記基板の1辺と平行な方向および前記信号線駆動回路の配置された前記基板の1辺と平行な方向のうち少なくともいずれか一方に設けたことを特徴とする液晶表示装置。

【請求項5】　請求項1乃至請求項4記載の液晶表示装置において、

前記基板間隙調整領域または前記基板間隙調整層を、走査線および信号線のうち少なくとも一方に重なるように設けたことを特徴とする液晶表示装置。

【請求項7】　請求項1乃至請求項6記載の液晶表示装置において、
前記基板間隙調整層の形成材料として前記液晶表示装置に用いられる材料のうち少なくとも一つの材料を用いたことを特徴とする液晶表示装置。
【請求項8】　請求項1乃至請求項7記載の液晶表示装置において、
前記表示領域と前記走査線駆動回路との間の領域に形成される基板間隙調整層を、前記信号線の形成材料を用いて形成し、前記表示領域と前記信号線駆動回路との間の領域に形成される基板間隙調整層を、前記走査線の形成材料を用いて形成してなることを特徴とする液晶表示装置。
【請求項9】　請求項1乃至請求項8記載の液晶表示装置において、
前記基板間隙調整領域または前記基板間隙調整層が、前記走査線および前記信号線と電気的に絶縁されていることを特徴とする液晶表示装置。
【請求項10】　請求項1乃至請求項9記載の液晶表示装置において、
前記表示領域における基板間隙を、前記基板間隙調整領域または前記基板間隙調整層によって均一に調整してなることを特徴とする液晶表示装置。
【発明の詳細な説明】
【0001】
【産業上の利用分野】本発明は液晶表示装置に関するもので、特に2枚の基板間隙を均一に接合する構造を有する液晶表示装置に関する。
【0002】
【従来の技術】近年、液晶表示装置の画像処理の高速化や、表示画像の高品位化を実現するために、表示画素ごとにスイッチング用の薄膜トランジスタ（以下ＴＦＴと略称）を設けた、いわゆるアクティブマトリクス型液晶表示装置が開発されている。
【0003】このようなアクティブマトリクス型液晶表示装置のスイッチング用ＴＦＴとしては、非晶質シリコン（ａ－Ｓｉ）、または多結晶シリコン（ｐｏｌｙ－Ｓｉ）を用いたＴＦＴが一般に用いられている。
【0004】特にｐｏｌｙ－Ｓｉは移動度が大きく、プロセス整合性の点からも駆動回路として画素領域のスイッチング用ＴＦＴ等と同一基板上に一体に形成できるため、小型で高精細な表示能力が要求されるアクティブマトリックス型液晶表示装置に好適なＴＦＴの形成材料であることが知られている。
【0005】このような従来のアクティブマトリクス型

Ｂ－Ｂ´断面図である。なお図9においては説明の簡潔化のために、特に液晶セル内部の画素部分を9画素に簡略化して示した。また実際のＴＦＴ基板には図示の他にも例えば補助容量Ｃｓやこれに接続される補助容量線等が形成されているが、図9においては説明の簡潔化のためにそれらの図示は省略している。
【0006】図9に示すように、液晶表示装置のスイッチング素子アレイ基板501の画素部のスイッチング素子としてＴＦＴ503が形成され、このＴＦＴ503のドレインは信号線505に、ソースは画素電極507に、ゲートは走査線509に各々接続されている。
【0007】そして信号線505は、シール材511に覆われた部分を通ってそのシール材511で囲まれた表示領域の外部にまで延伸し、信号線駆動回路513に接続されている。また走査線509は、シール材511に覆われた部分を通ってそのシール材511で囲まれた表示領域の外部にまで延伸し、走査線駆動回路515に接続されている。
【0008】信号線505のシール材511で覆われた部分は、図10のＡ－Ａ´断面図に示すように、ガラス基板600上に形成された例えばＳｉＯ2からなる層間絶縁膜601、Ａｌ／Ｃｒ膜をパターンニングして形成された信号線505、保護膜603から形成されている。
【0009】一方、走査線509のシール材511で覆われた部分は、図11のＢ－Ｂ´断面図に示すように、ガラス基板600上に成膜され不純物が添加されて低抵抗化された多結晶シリコン膜をパターンニングしてなる走査線509、層間絶縁膜601、保護膜603で構成されている。
【0010】そしてこのスイッチング素子アレイ基板501と、ＩＴＯからなる対向電極を有しその表面に配向膜が形成された対向基板（図示省略）とを対向配置し、信号線駆動回路513と表示領域との間にある領域の信号線505の一部および走査線駆動回路515と表示領域との間の領域にある走査線509の一部を覆うようにシール材（封止材兼接着剤）511を所定の幅で印刷あるいは塗布し、両基板の配向膜の配向方向が直交するように両基板を重ね合わせ圧力を加えながら接合して、両基板の間隙とシール材とによって形成されるいわゆる空セル状態の液晶セルに光変調層として液晶組成物（図示省略）を封入・挟持させることで液晶表示装置を製作している。
【0011】ところで、前記の2枚の基板を接合するためのシール材511としては従来一般に、保持すべき所

ように制御している。

【0012】しかしながら、上記のように製作された液晶表示装置においては、スイッチング素子アレイ基板501のシール材511で覆われる部分の基板600表面から保護膜603までの厚さ（つまり2枚の基板どうしの基板間隙）は、信号線505の部分では層間絶縁膜（0.45μm）＋Al／Cr 2層構造（0.8μm／0.05μm）＋保護膜（0.3μm）でトータル厚さ1.6μmとなる一方、走査線509の部分では多結晶シリコン膜（0.4μm）＋層間絶縁膜（0.45μm）＋保護膜（0.3μm）でトータル厚さ1.15μmとなってその厚さが異なるものとなる。この両者の厚さの差は1.6μm－1.15μm＝0.45μm程度にもなる。この厚さの差、つまりシール材511の高さによって支持される基板間隙の差は、例えば一般的な基板間隙が5μmとするとその約10%にも相当するため、このようなシール材511の高さの差によって2枚の基板間隙の画面内での位置的なばらつきができ、これに起因して画面（表示領域）内で表示むらが発生するという問題があった。特に画面の縦方向での基板間隙と横方向での基板間隙とが不均一になるため、全体的には2枚の基板は平行を欠いた配置となるため、表示むらが顕著に発生するという問題がある。

【0013】このようなシール材が形成された領域における走査線509上のシール材上面と信号線505上のシール材上面の高さの差は、その走査線509部分と信号線505部分との層構造および膜厚の違いに起因していることは上記の通りであるが、このような走査線509の層構造と信号線505の層構造との違いは、一般にTFTを形成する上で不可避的に存在するものである。すなわち、一般に走査線509と信号線505とは層間絶縁膜601等を介して異なった層に形成されて絶縁が図られている。このときTFT503内部でそのゲート（またはゲート電極）と走査線509とが接続され、ドレイン（またはドレイン電極）と信号線505とが接続される。そしてTFT503のゲートとドレインとは半導体層を介して異なる層に形成されており、しかもこれらの各層はプロセス条件が極めて大きく異なる。これはTFTの構造としてゲート電極が半導体層の上層に配置された構造（即ちスタガ型の場合）でも、逆に下に配置された構造（即ち逆スタガ型の場合）でも、いずれの場合でも同様である。したがって走査線509と信号線505とは異なった層に異なった膜厚で形成することが必要となり、シール材が形成された領域における走査線509部分と信号線505部分とでの高さの差が一般に不可避的に存在することになるのである。そして製造プロセスにおいて信号線505、走査線509の上にこれを配置し圧力を加えて接着する際に、信号線505、走査線509をこのガラスファイバが傷つけてしまうという問題もある。

【0015】良好な表示を得るためには、2枚の基板間隙が不均一であることで生じる光の干渉による色付きや色むらや、液晶組成物に実際に印加される電界が異なることやリタデーションの違いによるコントラストむらや色むらなどの表示むらを低減しなければならない。特に多階調表示や高精細で高画質な画像表示を行なうためには、印加電圧応答性の高い液晶組成物が用いられる。このような印加電圧応答性の高い液晶組成物は一般にリタデーションの変化に対して光透過特性が急峻に変化するため、基板間隙が不均一であるとリタデーションのばらつきが大きくなり、表示画像の輝度の位置的な均一性が著しく低下して画像表示品質に大きな悪影響を及ぼすことになる。特に3枚の液晶表示素子を用いて表示を行なう投射型液晶表示装置の場合に、上記の問題はいっそう顕著なものとなる。

【0016】したがってこのような液晶表示装置において画像表示の表示品位を考えた場合、2枚の基板間隙のばらつきは少なくとも±0.1μm以下程度にまでは小さくすることが実際上必要であり、製造プロセスによる誤差以外の不均一化の要因を避けることが高品位な画像再現性を実現するために必要である。

【0017】

【発明が解決しようとする課題】上述のように、従来の液晶表示装置においては走査線がシール材によって覆われた部分の基板間隙（基板表面から走査線上の保護膜上面までのトータルの厚さ）と、信号線がシール材によって覆われた部分の基板間隙（基板表面から信号線上の保護膜上面までのトータルの厚さ）とが異なるため、走査線が列設された側のシール材の高さで支えられた基板間隙と信号線が列設された側のシール材で支えられた基板間隙とが互いに不均一になり、表示画像に色むらやコントラストむら等が生じて画像表示性能が低劣なものとなるという問題があった。

【0018】本発明はこのような問題を解決するためになされたもので、その目的は、2枚の基板間隙を均一化して画質や表示コントラストを良好なものとした液晶表示装置を提供することにある。

【0019】

【課題を解決するための手段】本発明の液晶表示装置は、スイッチング素子と前記スイッチング素子に接続された走査線および信号線と前記スイッチング素子に接続された画素電極とを有するスイッチング素子アレイ基板

と．前記スイッチング素子アレイ基板と前記対向基板との基板間隙に周囲を前記シール材によって封止されて封入・狭持された光変調層とを有する液晶表示装置において．前記表示領域と前記走査線駆動回路との間の領域における基板間隙と前記表示領域と前記信号線駆動回路との間の領域における基板間隙とを均一に調整する基板間隙調整領域を．前記シール材によって覆われる部分を含む前記表示領域と前記走査線駆動回路との間の領域および前記表示領域と前記信号線駆動回路との間の領域のうち少なくともいずれか一方の領域に設けたことを特徴としている。

【００２０】また、本発明の液晶表示装置は、スイッチング素子と前記スイッチング素子に接続された走査線および信号線と前記スイッチング素子に接続された画素電極とを有するスイッチング素子アレイ基板と、前記走査線に接続された走査線駆動回路と、前記信号線に接続された信号線駆動回路と、前記画素電極に間隙を有して対向配置され表示領域を形成する対向電極を有し前記表示領域の周囲に形成されたシール材によって前記スイッチング素子アレイ基板に接着された対向基板と、前記スイッチング素子アレイ基板と前記対向基板との基板間隙に周囲を前記シール材によって封止されて封入・狭持された光変調層とを有する液晶表示装置において、前記表示領域と前記走査線駆動回路との間の領域における基板間隙と前記表示領域と前記信号線駆動回路との間の領域における基板間隙とを均一な間隙に調整する基板間隙調整層を．前記シール材によって覆われる部分を含む前記表示領域と前記走査線駆動回路との間の領域および前記表示領域と前記信号線駆動回路との間の領域のうち少なくともいずれか一方に設けたことを特徴としている。なお上記の基板間隙調整領域あるいは基板間隙調整層としては．前記シール材によって覆われる部分を含む前記表示領域と前記走査線駆動回路との間の領域における基板間隙と前記表示領域と前記信号線駆動回路との間の領域における基板間隙とを等しく揃えることのできる領域あるいは層であればどのようなものを用いてもよい。例えば．前記のシール材によって覆われる部分に電気絶縁性の良好な有機材料を均一かつ所望の基板間隙に等しい厚に形成し、その上に接着剤と兼用の前記シール材を薄く塗布して、２枚の基板を接着することなども可能である。あるいは．液晶駆動回路系の回路構成要素の一部分を上記の基板間隙調整領域あるいは基板間隙調整層として用いてもよい。あるいは．走査線と走査線駆動回路とを接続する走査線用引き出し配線を走査線とは別の材料を用いて設ける．あるいは信号線と信号線駆動回路とを

基板間隙調整領域あるいは基板間隙調整層として用いてもよい。

【００２１】また、本発明は、上記の液晶表示装置において．前記基板間隙調整領域または前記基板間隙調整層を走査線および信号線のうち少なくとも一方に重なるように設けたことを特徴としている。その基板間隙調整層としては、前記の走査線や信号線に対して直交して交差部が重なるようなパターンに形成してもよく、あるいは平行に重なるようなパターンに形成してもよい。またこのとき直線状または千鳥状のパターンに配置してもよい。またこの基板間隙調整層は走査線や信号線の上層に形成してもよく．あるいは下層に形成してもよい。いずれの場合も、前記表示領域と前記走査線駆動回路との間の領域における基板間隙と前記表示領域と前記信号線駆動回路との間の領域における基板間隙とを等しく揃えることができれば．どのような積層順に形成してもよく、あるいはどのようなパターンに形成してもよい。またさらに前記の基板間隙調整層は補助容量線などに重なるように配置してもよいことは言うまでもない。

【００２２】また、本発明は、上記の液晶表示装置において．前記基板間隙調整領域または前記基板間隙調整層を．走査線および信号線に沿って設けたことを特徴としている。例えば列設された走査線どうしの間の領域や信号線どうしの間の領域に走査線や信号線との接触を避けて柱状に前記基板間隙調整層を設けてもよく、あるいは走査線や信号線と平行なパターンに前記基板間隙調整層を設けてもよい。また走査線および信号線のみならず例えば補助容量線に沿っても設けるようにしてもよい。

【００２３】また、本発明は、前記基板間隙調整層の形成材料として．前記基板間隙調整層を形成すべき液晶表示装置に用いられる材料のうち少なくとも一つの材料を用いたことを特徴としている。

【００２４】このように液晶表示装置に用いられる材料を用いて前記基板間隙調整層を簡易に形成することができるので好ましい。

【００２５】また、本発明は、前記表示領域と前記走査線駆動回路との間の領域に形成される基板間隙調整層を前記信号線の形成材料を用いて前記信号線と同層に形成し．前記表示領域と前記信号線駆動回路との間の領域に形成される基板間隙調整層を前記走査線の形成材料を用いて前記走査線と同層に形成してなることを特徴としている。ただしこのとき、基板間隙調整層によって列設された走査線どうしや列設された信号線どうしが短絡することのないように基板間隙調整層の材質あるいは形状を設定しておくことは言うまでもない．例えば基板間隙調

において、前記基板間隙調整領域または前記基板間隙調整層が前記走査線および前記信号線と電気的に絶縁されているようにしてもよい。

【００２７】また、本発明は、前記表示領域における基板間隙を前記基板間隙調整領域または前記基板間隙調整層によって均一に調整してなることを特徴としている。すなわち、前記表示領域と前記走査線駆動回路との間の領域および前記表示領域と前記信号線駆動回路との間の領域つまりシール材で覆われた領域を含む前記基板間隙調整領域における基板間隙を均一に支持することにより、対向する２枚の基板全体の基板間隙を均一に支持することができる。このとき基板としては反りや撓じれの十分小さなものを用いることは言うまでもない。このようにすることで、従来一般に表示領域内に用いられていた基板間隙保持部材（いわゆるスペーサ）を省略して、表示画像のさらなる画質向上を図ることができるので好ましい。

【００２８】なお、本発明は前記走査線駆動回路および前記信号線駆動回路が前記走査線や前記信号線が配設された前記スイッチング素子アレイ基板上に配設されたいわゆる駆動回路一体型で、画素部から四方向に各引出し配線が伸びた構造の液晶表示装置において特に好適な技術である。しかしこれのみにはもちろん限定されず、例えば走査線の一端に走査線駆動回路が、信号線の一端に信号線駆動回路が接続され、他端はいずれも電気的に解放となっておりシール材から外に出る引き出し配線を他端側には有さないものについても、他端側のシール材を含んだ基板間隙の厚さを調整する基板間隙調整領域あるいは基板間隙調整層を新たに設けるなどして、シール材全体にわたって基板間隙の厚さを調整して均一にしてもよい。

【００２９】また、上記のスイッチング素子としては、例えばＴＦＴ（Thin Film Transistor）のような３端子素子や、ＭＩＭ（Metal Insulator Metal）素子のような２端子素子などが好適に用いられる。

【００３０】また、上記の光変調層としては、例えばＴＮ（Twisted Nematic）型やＳＴＮ（Super Twisted Nematic）型などの光変調作用を有する液晶組成物、あるいは樹脂マトリックス中に液晶材料を分散してなる高分子分散型またはカプセル状の液晶材料が樹脂中に含有された高分子分散型等の液晶層を好適に用いることができる。

【００３１】

【作用】シール材が塗布される領域、つまり駆動回路一体型の液晶表示素子における基板周辺部に作り込まれた

【００３２】特にシール材に覆われる部分の信号線上の基板間隙と走査線上の基板間隙とを均一化することで、対向する２枚の基板どうしの走査線列に沿った方向と信号線列に沿った方向での（基板の縦横両方向での）基板間隙を液晶セル全体にわたって均一化することができるので、液晶セル全体にわたって表示画像の色むらやコントラストむらを抑えて均一で良好な表示画面を実現することができる。

【００３３】

【実施例】以下、本発明に係る液晶表示装置の一実施例を、図面に基づいて詳細に説明する。

【００３４】（実施例１）図１は本発明に係る液晶表示装置のＴＦＴアレイ基板を示す平面図である。図２（ａ）は表示領域と信号線駆動回路との間の領域における信号線を中心としてその近傍を拡大して示す平面図、図２（ｂ）はそのＣ－Ｃ´断面図である。また図３（ａ）は表示領域と走査線駆動回路との間の領域における走査線を中心としてその近傍を拡大して示す平面図、図３（ｂ）はそのＤ－Ｄ´断面図である。また図４（ａ）は本発明に係る液晶表示装置の画素部分を拡大して示す平面図、図４（ｂ）はそのＥ－Ｅ´断面図である。なお上記の図２、３では、平面図においても図示の理解を容易なものとするために同一の材料で形成される部位に同じ斜線を付して示している。また、以降の各実施例における平面図および説明においては説明の簡潔化のために、液晶セル内部の画素部分を９画素に簡略化して示している。また、ＴＦＴアレイ基板に対向配置される対向基板の輪郭線はシール材の外側の輪郭線とほぼ重なる位置にあるものとして、図面の簡潔化のために対向基板の図示は以降の図面および説明においては省略している。

【００３５】図１に示すように、この液晶表示装置のＴＦＴアレイ基板１の表示領域のスイッチング素子としてＴＦＴ３が形成され、このＴＦＴ３のドレイン４１１はコンタクトホール４１７を通じて信号線５に、ソース４０９はコンタクトホール４１５、導電パターンを通して画素電極７に、ゲート４０５は走査線９に各々接続され、さらに所定の映像信号電圧を供給する信号線５は、それを順次駆動させる信号線駆動回路１１に信号線５の引出し配線部分１３を介して、また各ＴＦＴのゲート４０５にそのＴＦＴ３のオン・オフを行なわせる走査電圧（走査パルス）を供給する走査線９は、それを順次駆動させる走査線駆動回路１５に引き出し配線部分１７を介して接続されている。前記の信号線５とその引出し配線部分１３とは一体形成されており、実質的には引出し配

3．走査線9の引き出し配線部分17のシール材19で覆われた部分には、それぞれ基板間隙調整部材21、23が形成されている。

【0037】信号線5の引き出し配線部分13に重なるように設けられた基板間隙調整層21は、走査線9の引き出し配線部分17を形成する材料と同じ膜をパターンニングして形成したもので．また走査線9の引き出し配線部分17の基板間隙調整層23は．信号線5の引き出し配線部分13を形成する材料つまり信号線5の材料と同じ膜をパターンニングして形成したものである。

【0038】信号線5の引き出し配線部分13の近傍の構造は、図2（b）の断面図に示すように、ガラス基板200上に成膜され不純物が添加されて低抵抗化された多結晶シリコン膜をパターンニングしてなる基板間隙調整層21、層間絶縁膜201、Al／Cr膜をパターンニングしてなる信号線5の引き出し配線部分13．保護膜205でこの順に下層から形成されている。

【0039】また走査線9の引き出し配線部分17の近傍の構造は、図3（b）の断面図に示すように．ガラス基板200上に成膜され不純物が添加されて低抵抗化された多結晶シリコン膜をパターンニングしてなる走査線9の引き出し配線部分17．層間絶縁膜201．Al／Cr膜をパターンニングしてなる基板間隙調整層23、保護膜205で構成されている。

【0040】このように．信号線5の引き出し配線部分13の部分の層構造と、走査線9の引き出し配線部分17の部分の層構造はともに．ガラス基板200上に不純物が添加され低抵抗化された多結晶シリコン膜．層間絶縁膜．Al／Cr膜、保護膜が下からこの順で積層されている。したがってパターンニングで異なったパターンに形成されているが、層構造はこのように同様の層構造となっているので、その基板表面からのトータルの厚さ t_1．t_2 は．製造時の誤差などを除いて等しくなっている。その結果．信号線5の引き出し配線部分13の厚さ t_1 と走査線9の引き出し配線部分17の厚さ t_2 との差は 0.1μm以下にまで抑えられている。

【0041】そしてこのTFTアレイ基板1と．ITOからなる対向電極を有しその表面に配向膜が形成された対向基板（図示省略）とが対向配置され、信号線駆動回路11に接続される信号線5の引き出し配線部分13および走査線駆動回路15に接続される走査線9の引き出し配線部分17の上にシール材（シール材兼接着剤）19を印刷し、両基板の配向膜の配向方向が直交するように両基板を重ね合わせて圧力を加えて接着し、両基板の間隙とシール材19とにより形成されるいわゆるセル

ッチング素子としてTFTのチャンネルなどの活性層401および駆動回路を構成するTFTなどの活性層（図示省略）となる非結晶シリコン膜を低圧CVD法で成膜し．600℃で24時間の固相成長を行ない、多結晶化してパターニングする。

【0043】次にゲート絶縁膜403を熱酸化法で形成し．低圧CVD法により低抵抗化した第2の多結晶シリコン膜を成膜するが、これはTFTのゲート405および走査線9および引き出し配線部分17および基板間隙調整部材21となる。

【0044】ゲート405両側には．n型ドーパントであるP（燐）をイオン注入法で打ち込み低抵抗化してTFT3のソース409、ドレイン411を形成する。

【0045】さらに、層間絶縁膜201を低圧CVD法で成膜し、これにコンタクトホール415、417を形成する。

【0046】MOS容量である補助容量419は．活性層401と一体で画素電極7の一部と層間絶縁膜201を挟んで上部に補助容量線423があり、これらによって画素に並列に接続される補助容量C_sとして形成されている。補助容量線423は、シール材19に概ね覆われる領域の引き出し配線部分18と同層に同じ材料で一体形成されている。この補助容量線423（およびその引き出し配線部分18）は．例えば通常の補助容量線の形成と同様にゲート405を形成する膜を、ゲート405の形成と同じ工程でパターニングして形成することが可能である。あるいは、成膜工程等が増えるというデメリットはあるが．補助容量線423およびその引き出し配線部分18をゲート405とは別の材料から形成してもよい。あるいは補助容量線423と引き出し配線部分18のうちいずれか一方をゲート405とは別の材料から形成してもよい。

【0047】次にTFT3のドレイン411はコンタクトホール417を通して信号線5に．ソース409はコンタクトホール415、導電パターンを通して画素電極7に．ゲート405は走査線9に各々接続される。この信号線5はAl／Cr 2層構造からなり信号線駆動回路11に信号線5を延伸してなる引き出し配線部分13を通して接続するように形成される。また不純物が添加され低抵抗化された多結晶シリコン膜よりなる走査線9は走査線駆動回路15に走査線引き出し配線部分17を通して接続される。

【0048】これら 2つの異なる引き出し配線部分上の少なくとも一部に、図2及び図3に示したように信号線5の引き出し配線部分13下には走査線9と同じ材料の

大きく、かつ隣接する引き出し配線部分に接続しない大きさに形成する。

【００４９】このとき、この基板間隙調整層２１、２３の配置は、図２に示すような直線状配置としてもよく、あるいは図３に示すような千鳥状配置としてもよい。

【００５０】そして各パターンの最上層にはそれら各パターンを覆うようにＳｉ３Ｎ４からなる保護膜２０５を形成する。

【００５１】上述したＴＦＴアレイ基板１には対向基板（図示省略）とともに、その表面にポリイミド膜を形成し、これにラビング処理を行なって配向膜（図示省略）を形成する。さらに、対向基板の表面にスペーサ（図示省略）を散布し、注入口（図示省略）を除いて各引き出し配線部分部分に、接着剤に対して重量比 0.1%のガラスファイバを間隙制御材として光硬化型のエポキシ系接着剤に混合してなるシール材１９を配置しこのシール材１９を封止材兼接着剤として用いて、２枚の基板を位置合わせして組み合わせＵＶ（紫外）光を照射して接着する。このシール材１９の材料としては、上記の他にも熱硬化型の封止材兼接着剤などを用いてもよい。

【００５２】その後、注入口より通常の方法を用いて液晶組成物（図示省略）を注入し、注入口を紫外線硬化性樹脂で封止して液晶表示装置を完成する。

【００５３】このようにして製造された液晶表示装置は、各引き出し配線部分上の少なくとも一部に、そのトータルの厚さが等しくなるような基板間隙調整層２１、２３を設けることで、２枚の基板間隙を均一に保つことができる。特に、信号線５の引き出し配線部分１３と走査線９の引き出し配線部分１７との厚さを均一にすることで、対向する２枚の基板どうしの走査線方向（横方向）と信号線方向（縦方向）での基板間隙を均一化することができる。これにより、表示領域（画面）内での位置的な色むらやコントラストむらを抑えて、良好な表示を実現することができる。

【００５４】また、上記のように信号線５の引き出し配線部分１３や走査線９の引き出し配線部分１７にシール材１９を塗布しガラスファイバを配置しているので、このシール材１９を走査線駆動回路１５や信号線駆動回路１１の上に設けた構造の従来の液晶表示装置と比べて、走査線駆動回路１５や信号線駆動回路１１がシール材１９のガラスファイバから傷つけられることを避けることもできる。

【００５５】また、走査線あるいは信号線駆動回路外側のみをシール材によって封止する場合に比べて液晶に前記の駆動回路からの電圧が印加される境き付きなどのはっ成すれば、製造プロセス中でマスクずれなどによるパターンずれが生じてもこの基板間隙調整層２１、２３は常に各引き出し配線部分１３、１７、１８上に形成され、また引き出し配線部分１３、１７、１８とこの基板間隙調整層２１、２３とが例えば層間絶縁層２０１の絶縁不良などで層間ショートした場合でも、その他の引き出し配線部分とのショートを防ぐことができる。

【００５７】また、基板間隙調整層２１、２３の配置パターンを、直線状もしくは千鳥状等に複数列に形成することにより、ガラスファイバのような間隙制御材が複数の基板間隙調整層２１、２３に配置されやすくなることで、より一層広い部分で確実に基板間隙の均一化を図ることができる。

【００５８】なお上記の実施例では、引き出し配線部分１３、１７、１８上に形成された基板間隙調整層２１、２３を、多結晶シリコン膜、層間絶縁膜、Ａｌ／Ｃｒ２層構造、保護膜の４層構造に適用する方法を述べてきたが、この部分の構造は、本実施例のみには限定しない。上記実施例では、走査線や信号線等を形成する材料としてＡｌ／Ｃｒ以外にも、例えばＷＳｉ２、ＭｏＳｉ２、Ａｌ／Ｔｉなどを好適に用いることができる。特に前記のＷＳｉ２のようなシリサイドを用いることにより、Ａｌなどを配線材料として用いた場合に生じることの多かったヒロックを抑えることができるので好ましい。またこの他にも、例えばＡｌ／Ｃｒ２層構造と保護膜との間に層間絶縁膜とＩＴＯをさらに形成すれば、基板間隙が一定に保たれる効果のみならず、さらにファイバによって生じるＡｌ／Ｃｒ２層構造の信号線の傷つき等をも避けることが可能となる。

【００５９】また、ゲート電極を形成する材料としても、上記実施例の他にも例えば不純物打ち込みによって低抵抗化したドープドｐ－Ｓｉや、ＷＳｉ２やＭｏＳｉ２を好適に用いることができる。このような材料を用いることにより、配線のさらなる低抵抗化を図ることができるので好ましい。

【００６０】また、基板間隙調整層２１、２３の配置の一例として本実施例においては信号線引き出し配線部分１３側に直線状配置を、走査線引き出し配線部分１７側に千鳥状配置を採用した場合を示したが、この配置法は本実施例のみには限定しないことは言うまでもない。各引き出し配線部分上に形成された基板間隙調整層２１、２３が隣接する引き出し配線部分に接触しないようなパターンであれば、両方の基板間隙調整層２１、２３ともに直線状配置あるいは千鳥状配置のパターンや、本実施例とは逆に、信号線引き出し配線部分１３側に千鳥状配

とは別に絶縁体材料を用いて基板間隙調整層２１．２３を形成してもよい。このような絶縁体を用いることにより．基板間隙調整層２１．２３が製造時のパターンずれなどによって隣り合う複数本の走査線どうしあるいは信号線どうしに接触してしまった場合でも、短絡欠陥の発生を避けることができる。

【００６２】ただし上記実施例で示したように信号線５や走査線９に用いた材料やＴＦＴ３の活性層に用いた材料と同じ材料を用いて基板間隙調整層２１．２３を形成すれば、製造工程および構造をより簡易なものとすることができるので好ましい。

【００６３】また基板間隙調整層２１．２３の幅は、本実施例では各引き出し配線部分１３．１７、１８の幅と同程度から数倍程度の幅としているが．これのみには限定しない。例えばシール材１９の幅と同じ程度の幅にしてもよい。

【００６４】さらに、シール材に混合する間隙制御材としてはガラスファイバを用いたが、基板間隙が均一に保てるのであれば．この他にも例えば粒状の（ミクロパールのような）間隙制御材を用いてもよい。あるいはそのようなガラスファイバなどの間隙制御材の混合を省略することもできる。

【００６５】このような構造に形成された本実施例の液晶表示装置は．対向配置される２枚の基板間隙．いわゆるセルギャップを均一化して良好な画質や表示コントラストの画像表示を実現することができる。

【００６６】また、上記実施例で示したような本発明に係る液晶表示パネルを３枚用いて、光の経路が．光源、光源光の色分解系、液晶表示パネル．色合成系．投射レンズ系の順に配置して投射型液晶表示装置（いわゆるプロジェクション型液晶表示装置）を製作し、表示を行なわせてその画像表示性能を検証したところ、色むらやコントラストむらのない均一で良好な表示が得られた。

【００６７】上記の第１の実施例の液晶表示装置のように基板の四辺に駆動回路を形成し走査線や信号線の両端にそれぞれ駆動回路を接続する場合には、冗長性を得ることができ一方の駆動回路に動作不良が生じても他方を動作させて正常な駆動を行なうことが可能である。あるいは両端の駆動回路を動作させることで走査電圧波形や信号電圧波形の電圧傾斜に起因した歪みや鈍りを防ぐことができる。また上記の場合、駆動回路がシール材や対向基板に覆われていないので例えばレーザリペアのような欠陥修復を簡易に施すことができるという利点もあり．好ましい。

【００６８】（実施例２）図５は第２の実施例の液晶表

【００６９】この第２の実施例の液晶表示装置においては．シール材１９で囲まれた内側の画素電極７が配列された表示領域と走査線駆動回路１５との間のシール材１９によって覆われる領域に、列設された走査線９の引き出し配線部分１７および補助容量線４２３の引き出し配線部分１８に沿って基板間隙調整層２５をパターニング形成するとともに、列設された信号線５の引き出し配線部分１３どうしの狭間の部分に沿って基板間隙調整層２７を成膜．パターニングして配置したことを特徴としている。

【００７０】前記の基板間隙調整層２５、２７は．ともにこの液晶表示装置の形成材料を用いて形成するようにすれば、基板間隙調整層２５、２７を別の材料を用いて新たに形成するための成膜工程などを省略することができるので、その構造および製造工程を簡易なものとすることができて好ましい。

【００７１】例えば本実施例では、基板間隙調整層２５．２７の形成材料として．前述の第１の実施例と同様の材料、つまり走査線９（および引き出し配線部分１７）の形成材料と、信号線５（および引き出し配線部分１３）の形成材料と、層間絶縁膜の形成材料２０１と、保護膜の形成材料２０５とを用いて．走査線９の引き出し配線部分１７側に設けられる基板間隙調整層２５の基板２００上面からの高さと信号線５の引き出し配線部分１３側に設けられる基板間隙調整層２７の基板２００上面からの高さとを同じ高さに形成している。このときこれら基板間隙調整層２５．２７の高さは、例えばＴＦＴ３や補助容量４１９や補助容量線４２３など、その他の構成部位の高さよりも高い高さに形成する。このようにして．走査線９の引き出し配線部分１７側の基板間隙と信号線５の引き出し配線部分１３側の基板間隙とを等しく支持することができる。

【００７２】そしてその他の走査線９．走査線９の引き出し配線部分１７、信号線５、信号線５の引き出し配線部分１３、ＴＦＴ３、補助容量線４２３、シール材１９の形成領域、走査線駆動回路１５、信号線駆動回路１１などの各部位は第１の実施例と同様の構造および材料で形成されている。

【００７３】このような構造に形成された第２の実施例の液晶表示装置においても．対向配置される２枚の基板間隙．いわゆるセルギャップを均一化して、良好な画質や表示コントラストの画像表示を実現することができる。

【００７４】なお、用いることができる材料としては、上記のような材料構成のみには限定しない。例えば基板

で、成膜や膜厚制御が容易な材料を用いることが望ましいことは言うまでもない。

【0075】また、上記実施例では基板間隙調整層を走査線9の引き出し配線部分17側のと信号線5の引き出し配線部分13側との両方に配置したが、これのみには限定せず、いずれか一方の側のみに設けてもよい。このとき基板間隙調整層はシール材19で覆われる領域内におけるその他の構成部位の高さが低い方の側に設けて、その高さを高い方の側に揃えるようにすることは言うまでもない。

【0076】また、上記実施例では基板間隙調整層25、27を引き出し配線部分13、17、18と全て非接触に配置したが、これのみには限定せず、例えば各引き出し配線部分13、17、18に対して沿うように基板間隙調整層25、27を列設し、かつ隣り合う引き出し配線部分13、17、18には同じ一つの基板間隙調整層25、27のパターンが接触しないような配置に形成してもよい。このような少なくとも隣り合う引き出し配線部分13、17、18どうしが短絡しないような配置であれば、第2の実施例における基板間隙調整層25、27のパターンは種々の変更が可能である。例えば引き出し配線部分13、17、18に平行に長いパターンに形成することなども可能である。

【0077】（実施例3）図6、図7は第3の実施例の液晶表示装置を示す平面図である。なおこの第3の実施例の説明および図6、図7においては、説明の簡潔化のために第1の実施例と同様の部位には同じ番号を付して示すとともに、この第3の実施例における特徴的な部分を中心として説明する。

【0078】この第3の実施例の液晶表示装置においては、シール材19で囲まれた内側の画素電極7が形成された表示領域と走査線駆動回路15との間のシール材19によって概ね覆われる領域に、走査線9に接続される引き出し配線部分17および補助容量線423に接続される引き出し配線部分18を走査線9および補助容量線423とは別の材料、例えば導電性の良好なAl（アルミニウム）を単層に成膜およびパターニングして形成し、この引き出し配線部分17、18を基板間隙調整層29として兼用するとともに、信号線5に接続される引き出し配線部分13を信号線5とは別の材料を用いて例えば前記のAlを材料として形成して、この引き出し配線部分13を基板間隙調整層31として兼用することを特徴としている。

【0079】前記の基板間隙調整層29、31は、ともに基板200下面からの高さが同じ高さに形成される。部分13、TFT3、補助容量線423、シール材19、走査線駆動回路15、信号線駆動回路11などの各部位は第1の実施例と同様の構造および材料で形成されている。

【0081】このような構造に形成された第2の実施例の液晶表示装置においても、対向配置される2枚の基板間隙、いわゆるセルギャップを均一化して、良好な画質や表示コントラストの画像表示を実現することができる。

【0082】なお、用いることができる材料としては、上記のような材料のみには限定しない。基板間隙調整層29、31を形成する材料としては、上記のような単層のAlの他にも、例えばCr／Mo／Crの3層に積層することなども可能である。あるいはドーパントを打ち込んで低抵抗化したp－Siを用いてもよい。このような低抵抗化を図ることのできる材料としては、例えばWSi、やMoSi、のようなシリサイドを好適に用いることができる。

【0083】また、上記実施例では基板間隙調整層29、31を走査線9の引き出し配線部分17側と信号線5の引き出し配線部分13側との両方に配置したが、これのみには限定せず、いずれか一方の側のみに設けてもよい。このとき基板間隙調整層はシール材19で覆われる領域内におけるその他の構成部位の高さが低い方の側に設けて、高さを高い方の側に揃えるようにすることは言うまでもない。

【0084】また、上記実施例では引き出し配線部分13、17、18の全てを基板間隙調整層29、31としたが、これのみには限定せず、例えば引き出し配線部分13、17はそれぞれ信号線5、走査線9とは別体でそれぞれ基板間隙調整層29、31として形成する一方、補助容量線423とその引き出し配線部分18とは同層で同じ材料から一体形成して、基板間隙調整層29としては用いないようにしてもよい。つまり走査線9の引き出し配線部分13側と信号線5の引き出し配線部分17側とが等しい基板間隙に支持されるように基板間隙調整層29、31を配置すればよい。この他にも、液晶表示装置の層構造によっては引き出し配線部分13、17、18のうちいずれか1種類のみを基板間隙調整層として兼用するようにする、あるいはいずれか2種類を基板間隙調整層として兼用するようにしてもよいことは言うまでもない。

【0085】また、上記実施例では基板間隙調整層29、31の平面的パターンを引き出し配線部分13、17、18と同程度の幅の細線に形成したが、この他に

用される構造をとっているため、基板間隙調整層２９、３１は導電性材料から形成されているので、隣り合うパターンどうしが接触すると短絡不良を引き起こすためである。このように少なくとも隣り合う引き出し配線部分１３、１７、１８どうしが短絡しないような配置であれば、上記の第３の実施例における基板間隙調整層２９、３１のパターンは種々変更が可能である。

【００８６】上記実施例では、基板の周辺部の 4辺に駆動回路が配置された液晶表示装置について示したが、本発明はこれのみには限定しない。この他にも、例えば図７に示すように、走査線駆動回路１５がＴＦＴアレイ基板１の周辺部の 1辺だけに配置されて走査線９の一端に接続され、走査線９の他端は解放状態になっており、信号線駆動回路１１も基板の周辺部の前記走査線駆動回路が配置された辺に直交する方向の 2辺のうちの 1辺側だけに配置されて信号線５の一端に接続され、信号線５の他端は解放状態になっているような液晶表示装置においても適用可能である。

【００８７】この場合には、信号線５と信号駆動回路１１との間のシール材１９に概ね覆われる領域における引き出し配線部分１３、および走査線９と走査線駆動回路１５との間のシール材１９に概ね覆われる領域における引き出し配線部分１７、１８を上記の実施例と同様に基板間隙調整層２９、３１として兼用する一方、信号線５および走査線９それぞれの解放端側にも、前記の引き出し配線部分１３、１７、１８と同様の基板間隙調整層３０、３２を設けておくことは言うまでもない。この基板間隙調整層３０、３２は、それぞれ信号線５、走査線９に電気的に接続されるように設けてもよく、あるいは切り離していわゆるダミーパターンとして設けてもよい。図７に示した一例では、基板間隙調整層３０は信号線５と一体形成されて電気的に接続されている。一方、基板間隙調整層３２は、走査線９とは切り離されて設けられており補助容量線４２３とは一体形成されて電気的に接続されている。この他にも、例えば基板間隙調整層３０、３２は全て電気的に（あるいはパターンとして）切り離された構造に形成してもよい。あるいは逆に、基板間隙調整層３０、３２は全て電気的に（あるいはパターンとして）接続された構造に形成してもよい。

【００８８】このように駆動回路が走査線や信号線の一端のみに接続された液晶表示装置の場合においても、上記のようにその他端側にも基板間隙調整層３０、３２を設けることにより、ＴＦＴアレイ基板１と対向基板との間の基板間隙を、走査線駆動回路１５の配置された基板 1辺に平行な方向と信号線駆動回路１１の配置された基

号線５の一端だけに接続され他端は解放となるように基板の 1辺側だけに設けられているような場合などにも、本発明が適用可能であることは言うまでもない。そのような場合にも、信号線５の解放端側に上記の図７に示したような場合と同様に基板間隙調整層３１と同様の基板間隙調整層３１と等しい高さに揃えたダミーパターンを設けて、これを基板間隙調整層３０として用いるようにすればよい。

【００９０】（実施例４）図８は第４の実施例の液晶表示装置を示す平面図である。なおこの第４の実施例の説明および図８においては、説明の簡潔化のために第１の実施例と同様の部位には同じ番号を付して示すとともに、この第４の実施例における特徴的な部分を中心として説明する。

【００９１】この第４の実施例の液晶表示装置においては、表示領域外に蓄積容量を設けた場合を示しており、特にシール材で覆われた領域内にその蓄積容量を設けたことを特徴としている。

【００９２】図８（ａ）に示すようにシール材１９で囲まれた内側の画素電極７が配列された表示領域と走査線駆動回路１５との間のシール材１９によって概ね覆われる領域およびシール材１９で囲まれた内側の画素電極７が配列された表示領域と信号線駆動回路１１との間のシール材１９によって概ね覆われる領域が、対向する 2枚の基板どうしの基板間隙を縦横方向ともに均一な間隙に調整する基板間隙調整領域３３であることを特徴としている。具体的には、この基板間隙調整領域３３において引き出し配線部分１３に沿って蓄積容量３５が形成されるとともに引き出し配線１３にその一端が接続され他端は所定の電圧に接続されている。そしてこの蓄積容量３５の基板２００上面からの高さによって信号線５の引き出し配線１３側の基板間隙が支持されている。この蓄積容量３５は、このような基板間隙調整領域３３における基板間隙調整のために用いられる一方、それぞれが接続された信号線５の 1ラインごとに映像信号電圧を表示に適した値に保持するために設けられているものである。

【００９３】この蓄積容量３５は、上記のようなシール材１９によって覆われた領域以外にも、表示領域内に設けてもよく、表示領域外に設けてもよい。あるいは蓄積容量３５を駆動回路内部に作り込んでもよいことは言うまでもない。ただし、上記実施例のようにシール材１９に覆われる領域に設けることにより、実質的にこの蓄積容量３５を基板間隙調整層として兼用することができるという利点があるため、この点で上記実施例は好ましいものである。

に用いる材料から上電極７０３を形成し、この上電極７０３と前記の下電極７０１との間で誘電体層としての層間絶縁膜２０１を挟むことにより、蓄積容量３５の主要部を構成する構造となっている。そしてそれを覆って保護するようように保護膜２０５が形成されている。このように液晶表示装置の形成材料を用いて蓄積容量３５の主要部を構成すれば、その層構造および製造工程を簡易なものとすることができるので好ましい。

【００９５】この蓄積容量３５の基板２００上面からの高さは、補助容量線４２３の引き出し配線部分１８が形成された部分の基板２００上面からの高さに揃えて均一な高さに形成されている。つまり蓄積容量３５の基板２００上面からの高さと、補助容量線４２３の引き出し配線部分１８の層構造の最上部の高さとが等しく均一になるように、引き出し配線部分１８の層構造が図８（ｂ）に示す蓄積容量３５の層構造と同様に、下層から順に下電極７０１と同じ膜厚の同じ材料、層間絶縁膜２０１と同じ膜厚の同じ材料、上電極７０３と同じ膜厚の同じ材料、保護膜２０５、という層構造に形成されている。このとき、上電極７０３と同じ膜厚の同じ材料で形成された引き出し配線部分１８の上層部分は蓄積容量３５とは異なり外部の電源に接続されておらずフローティング状態となっているので、この引き出し配線部分１８には表示に対して実質的に悪影響を与えるような電気容量（つまりこの引き出し配線部分１８を通る電流の鈍りや遅延など）はほとんど無視できるほど小さいものとなっている。

【００９６】このようにして、走査線９の引き出し配線部分１７側の基板間隙と信号線５の引き出し配線部分１３側の基板間隙とを等しく支持することができる。

【００９７】そしてその他の走査線９、走査線９の引き出し配線部分１７、信号線５、信号線５の引き出し配線部分１３、ＴＦＴ３、シール材１９の形成領域、走査線駆動回路１５、信号線駆動回路１１などの各部位は第１の実施例と同様の構造および材料で形成されている。

【００９８】このような構造に形成された第４の実施例の液晶表示装置においても、対向配置される２枚の基板間隙、いわゆるセルギャップを均一化して、良好な画質や表示コントラストの画像表示を実現することができる。

【００９９】なお、上記実施例では基板間隙調整領域３３において基板間隙調整のために信号線５の引き出し配線部分１３に配置される蓄積容量３５を用いたが、本発明はこれのみには限定しない。

【０１００】この他にも例えば基板２００上に形成される信号線５の引き出し配線部分１３側と走査線９の引き出し配線部分１７側との基板間隙を均一に支持するような構造に形成してもよい。

【０１０１】あるいは、基板間隙調整領域３３において上記のように蓄積容量３５を用いて信号線５の引き出し配線部分１３側の基板の支持高さを調整することにより基板間隙を調整するとともに、その一方で走査線９の引き出し配線部分１７側には前述の第１乃至第３の実施例で示したような基板間隙調整層２３、２５、２９を形成して、走査線９の引き出し配線部分１７側の基板の支持高さを調整することにより基板間隙を調整して、両側の基板間隙を等しく均一に調整することも可能である。また補助容量線４２３の引き出し配線部分１８のみならず、走査線９の引き出し配線部分１７および信号線５の引き出し配線部分１３の両方にも基板間隙調整層２３、２５、２９のような基板間隙調整層を形成してもよいことは言うまでもない。

【０１０２】このように基板間隙調整領域３３において基板の縦横両方向にわたって基板間隙を均一に保持することができる。

【０１０３】なお、本発明によれば、以上の各実施例で示したような基板間隙調整領域あるいは基板間隙調整層によって２枚の基板の基板間隙を基板の縦横両方向にわたって等しく保つことができるので、２枚の基板の面方向での剛性が十分なものであれば、従来の液晶表示装置において画素電極が配列された表示領域に散布されていたスペーサを省略することも可能である。このような画素電極が配列された表示領域には、低密度とは言えどもスペーサのような液晶とは透過率の異なる部材を配置しないことが望ましい。したがって本発明を用いてスペーサを省略することによって、画質のさらなる向上を図ることができる。

【０１０４】また、以上の第１乃至第４の実施例においては、活性層が多結晶シリコンからなるいわゆるｐｏｌｙ－Ｓｉ ＴＦＴを用いた場合について述べたが、この他にも、ｐｏｌｙ－Ｓｉ ＴＦＴのみならず単結晶ＳｉＴＦＴあるいはａ－Ｓｉ ＴＦＴをスイッチング用のＴＦＴとして用いた場合や、ＴＦＴのなかでもスタガ型ＴＦＴ構造の場合も逆スタガ型ＴＦＴ構造の場合も、あるいはＭＩＭ素子のような２端子素子を用いた場合においても、本発明の技術は適用可能であることは言うまでもない。

【０１０５】また、走査線駆動回路や信号線駆動回路はスイッチング用のＴＦＴと同様にｐ－Ｓｉを用いて同時に形成する場合を示したが、例えば駆動回路のみを単結晶Ｓｉで形成してもよく、あるいは駆動回路として液晶

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LIQUID CRYSTAL CELL

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[There are no amendments to this patent.]

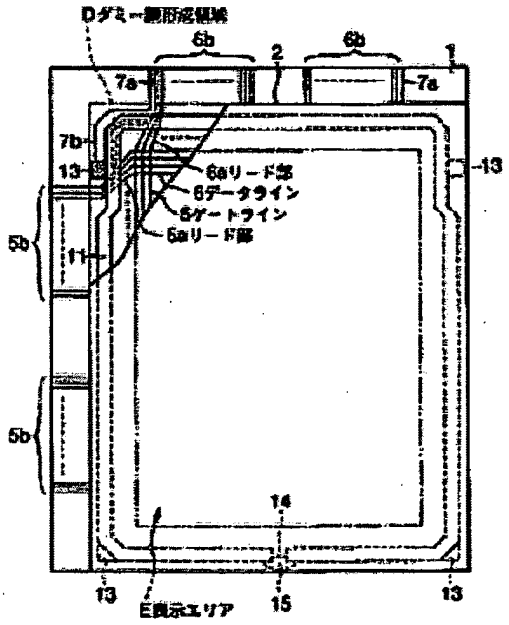
Abstract

Purpose

To minimize the variation of cell gaps.

Constitution

In the liquid crystal cell, liquid crystal is sealed between a pair of substrates (1), (2) bonded to each other via frame-like sealant (11) consisting of a resin including a gap material and, at the same time, on the inner surfaces of said pair of substrates (1), (2), electrodes corresponding to display area E and lead parts (5a), (6a) extending to the outer side of said sealant (11) are formed, respectively; in this liquid crystal cell, plural dummy films with film thicknesses nearly equal to that of said lead parts (5a), (6a) are formed on the joint part joined by the sealant (11) on the inner surface of at least one substrate (1) at a prescribed interval over almost the entire area, excluding the areas passing said lead parts.



Key:
- 5 Gate line
- 5a Lead part
- 6 Data line
- 6a Lead part
- D Dummy film forming region
- E Display area

Claims

1. A liquid crystal cell characterized by the following facts: liquid crystal is sealed between a pair of substrates bonded to each other via a frame-like sealant consisting of a resin including a gap material that defines the cell gap, and at the same time, on the inner surfaces of

said pair of substrates, electrodes corresponding to the display area and lead parts extending to the outer side of said sealant are formed, respectively;

in this liquid crystal cell, plural dummy films with film thicknesses nearly equal to that of said lead parts are formed on the joint part joined by the sealant on the inner surface of at least one substrate at a prescribed interval over almost the entire area, excluding the areas passing said lead parts.

2. A liquid crystal cell of the active matrix type, characterized by the following facts: liquid crystal is sealed between a pair of substrates bonded to each other via a frame-like sealant consisting of a resin including a gap material that defines the cell gap, and, at the same time, on the inner surfaces of one substrate, plural pixel electrodes arranged in a matrix configuration corresponding to the display area, plural thin-film transistors connected to said pixel electrodes, respectively, gate lines and data lines for supplying a gate signal and data signal to said thin-film transistors, and lead parts extending from said lines to the outer side of said sealant are formed, on the inner surface of the other substrate, a light-shielding film opening at the parts corresponding to the various pixels, opposing electrodes corresponding to the entire region of said display area, and lead parts extending out from said opposing electrode and said light-shielding film are formed;

in this active matrix type liquid crystal cell, the outer peripheral parts of both said opposing electrodes and said light-shielding film are formed with a contour corresponding to the interior of the joint part made of said sealant.

3. The liquid crystal cell described in Claim 2 characterized by the fact that the outer peripheral edges of said opposing electrodes and said light-shielding film are on the inner side with respect to the outer periphery of the sealant.

4. The liquid crystal cell described in Claim 2 characterized by the fact that plural dummy films with film thicknesses nearly equal to that of the lead parts are set at a prescribed interval over almost the entire region, excluding the regions where said lead parts pass, on the joint part made of the sealant on the inner surface of one substrate.

5. The liquid crystal cell described in Claim 4 characterized by the fact that the dummy films are set on the inner side with respect to the outer periphery of the sealant.

6. The liquid crystal cell described in Claim 5 characterized by the fact that the dummy films are formed in linear shape along the width direction of the sealant, and the ratio of the spacing between the dummy films to the width of the dummy film is less than the ratio of the interval between the lead parts to the width of the lead part.

Detailed explanation of the invention

[0001]

Technical field of the invention

The present invention pertains to a liquid crystal cell for use in a liquid crystal display device. It provides a liquid crystal cell with a more uniform cell gap.

[0002]

Prior art

In addition to the generally used TN type, there are other types of the liquid crystal display devices, such as STN type with twist angle of the liquid crystal molecules as large as in the range of 180° to 270°, the birefringence effect type that can execute a colored display without using a color filter, and types using ferroelectric liquid crystal or antiferroelectric liquid crystal, etc. Said liquid crystal display devices usually have the following structure: a liquid crystal cell is sandwiched between a pair of polarization sheets. For the birefringence effect type liquid crystal display device, a phase difference plate may be set between the liquid crystal cell and the polarization sheet.

[0003]

For said liquid crystal cell, a pair of substrates made of glass or the like are bonded to each other via a frame-like sealant made of a resin having gap members for defining the cell gap (spacing between substrates), and a liquid crystal is sealed in the region defined by said sealant between said substrates. Consequently, on the inner surfaces of said pair of substrates, transparent electrodes corresponding to the display area and lead parts extending to the outer side of said sealant are formed, respectively.

[0004]

An orienting film that covers said electrodes and defines the orientation state of the liquid crystal molecules is applied to the inner surfaces of the display areas of said pair of substrates. In the liquid crystal cell for use in the liquid crystal display device that can affect a colored display by means of color filters (TN type, STN type, ferroelectric liquid crystal display device, etc.), color filters are set on the inner surface of one substrate (below the electrodes or between said electrodes and the orienting film).

[0005]

Problems to be solved by the invention

However, the display characteristics of said liquid crystal display device depends on the layer thickness of the liquid crystal cell and the orientation of the liquid crystal molecules. Consequently, in order to realize a high-quality display without display unevenness, it is necessary to ensure a uniform thickness of the liquid crystal layer, that is, the cell gap, of the liquid crystal cell over the entire cell.

[0006]

Here, the cell gap is defined by the gap members mixed in the sealant for bonding the two substrates to each other. Because the cell gap of the region where the lead part of the joint part made of said sealant passes is defined by the gap members on the lead part, while the cell gap of the remaining region is defined by the gap members contacting the substrate surfaces, there is variation in the cell gap of said liquid crystal cell corresponding to the film thickness of said lead part.

[0007]

The variation of the cell gap, that is, the difference in the cell gap between the region where the lead part passes and the remaining region of said joint part, is about 0.3-0.4 μm for the active matrix type liquid crystal cell using thin-film transistors as the active elements. This precision is a small problem for the conventionally used TN type liquid crystal display devices.

[0008]

However, for the STN type and birefringence effect type liquid crystal display devices as well as the ferroelectric liquid crystal display devices, even a small variation in the cell gap of the liquid crystal cell affects the display characteristics. For example, in the birefringence effect type liquid crystal display device that displays plural colors by means of a change in the value of $\Delta n \cdot d$ (the product of refractive index anisotropism Δn and liquid crystal layer thickness d) of the liquid crystal cell corresponding to the applied voltage, even a small variation in the cell gap appears as color unevenness. The purpose of the present invention is to solve the aforementioned problems of the prior art by providing a liquid crystal cell that can minimize the variation in the cell gap.

[0009]

Means to solve the problems

The present invention provides a liquid crystal cell characterized by the following facts: for the liquid crystal cell, liquid crystal is sealed between a pair of substrates bonded to each other via a frame-like sealant consisting of a resin including a gap material that defines the cell gap, and, at the same time, on the inner surfaces of said pair of substrates, electrodes corresponding to the display area and lead parts extending to the outer side of said sealant are formed, respectively; in this liquid crystal cell, plural dummy films with film thicknesses nearly equal to that of said lead parts are formed on the joint part of the inner surface of at least one substrate at a prescribed interval over almost the entire area, excluding the areas passing said lead parts.

[0010]

According to the present invention, the cell gap of the region where the lead part passes among the parts of the joint part made of the sealant is defined by the gap members on said lead part, while the cell gap of the remaining region is defined by the gap members on the dummy film having almost the same film thickness as that of said lead part. Consequently, it is possible to minimize the variation of the cell gap.

[0011]

Also, the present invention provides a liquid crystal cell characterized by the following facts: in the liquid crystal cell of the active matrix type, liquid crystal is sealed between a pair of substrates bonded to each other via a frame-like sealant consisting of a resin including a gap material that defines the cell gap, and, at the same time, on the inner surfaces of one substrate, plural pixel electrodes set in a matrix configuration corresponding to the display area, plural thin-film transistors connected to said pixel electrodes, respectively, gate lines and data lines for supplying gate signal and data signal to said thin-film transistors, and lead parts extending from said lines to the outer side of said sealant are formed, on the inner surface of the other substrate, a light-shielding film opening at the parts corresponding to the various pixels, opposing electrodes corresponding to the entire region of said display area, and lead parts extending out from said opposing electrode and said light-shielding film are formed; in this active matrix type liquid crystal cell, both said opposing electrodes and the outer peripheral parts of said light-shielding film are formed with a contour corresponding to the interior of the joint part made of said sealant.

[0012]

According to the present invention, the cell gap of the region where the lead parts extending from the opposing electrodes and the light-shielding film among the regions of the boding part made of the sealant pass is defined by the gap members on said lead parts, while the cell gap of the remaining region is defined by the gap members on the outer peripheral part of the opposing electrodes and light-shielding film. Because the film thickness of the outer peripheral part of said opposing electrodes and light-shielding film and the film thickness of said lead part are equal, it is possible to minimize the variation of the cell gap.

[0013]

According to the present invention, the following scheme is preferred: the outer peripheral edges of said opposing electrodes and said light-shielding film are on the inner side with respect to the outer periphery of the sealant. As a result, the outer peripheral part of the sealant and the substrate surfaces can be directly in close contact with each other so that the sealing property can be improved. At the same time, it is possible to prevent external impurities from passing through the opposing electrodes and the light-shielding film and entering the cell.

[0014]

In addition, for said active matrix type liquid crystal cell, the following scheme is preferred: plural dummy films with film thicknesses nearly equal to that of the lead parts are set at a prescribed spacing over almost the entire region, excluding the regions where said lead parts pass, on the joint part made of the sealant on the inner surface of one substrate where said pixel electrodes, thin-film transistors, gates, and data lines are formed. In this way, it is possible to eliminate variation in the cell gap almost entirely.

[0015]

Also, according to the present invention, the following scheme is preferred: the dummy films are set on the inner side with respect to the outer periphery of the sealant. In this way, the outer peripheral part of the sealant is in direct close contact with the substrate surfaces, so that a high sealing property can be realized, and, at the same time, it is possible to prevent external impurities from passing through said dummy film and entering the cell.

[0016]

When said dummy film is formed on the inner side with respect to the outer periphery of the sealant, the following scheme is preferred: the dummy films are formed in linear shape along the width direction of the sealant, and the ratio of the spacing between the dummy films to the

width of the dummy films is less than that ratio of the interval between the lead parts to the width of the lead parts. In this way, the number of gap members per unit area of the lead part passing through the entire width of said joint part is larger than the number of the gap members per unit area of the dummy film with the length smaller than the width of said joint part, so that for the density of the gap members on the lead parts and on the dummy films that are effective in defining the cell gap, the value of the density on the lead part with larger length in the width direction of said joint part is less than that on the dummy film with smaller length in the width direction of said joint part. Consequently, the effect of the gap members in defining the cell gap is nearly the same over the entire circumference of the joint part, and it is possible to further reduce the variation in the cell gap.

[0017]

Embodiment of the invention

In the following, an explanation will be given regarding embodiments of the present invention with reference to figures. Figures 1-5 illustrate Application Example 1 of the present invention. Figure 1 is a plan view of the liquid crystal cell. Figure 2 is a plan view of one substrate of said liquid crystal cell. Figure 3 is an enlarged view of a part of Figure 2. Figure 4 is an enlarged plan view of a part of said liquid crystal cell. Figure 5 includes enlarged cross-sectional views illustrating a part of said liquid crystal cell. (a) is a cross-sectional view along A-A in Figure 3. (b) is a cross-sectional view along B-B in Figure 3.

[0018]

As shown in Figures 1-5, the liquid crystal cell in this application example is prepared by bonding a pair of transparent substrates (1), (2) made of glass or the like via frame-like sealant (11), and then sealing the liquid crystal (not shown in the figure) into the region defined by said substrates (1), (2) and said sealant (11). On the inner surfaces of said pair of substrates (1), (2), transparent electrodes corresponding to display area E and lead parts extending to the outer side of sealant (11) are formed, respectively.

[0019]

The liquid crystal cell in this application example is of the active matrix type using thin-film transistors (hereinafter referred to as TFTs) as the active elements. On the inner surface of one substrate among said pair of substrates (1), (2), such as rear side substrate (1), as shown in Figures 1-3, plural transparent pixel electrodes (3) set in a matrix configuration corresponding to display area E, plural TFTs (4) connected to said pixel electrodes (3), respectively, gate lines (5) and data lines (6) for supplying gate signals and data signals to said TFTs (4), and lead

parts (5a), (6a) extending from said lines (5), (6) to the outer side of sealant (11) are formed. The end parts of said lead parts (5a), (6a) are used as connecting terminals (5b), (6b) for the driver.

[0020]

In the figure, said TFTs (4) are shown in a simplified way. Each of TFTs (4) is composed of the following parts: a gate electrode formed on substrate (1), a gate insulating film covering said gate electrode, an i-type semiconductor film formed opposite to said gate electrode on said gate insulating film, and a source electrode and a drain electrode formed via n-type semiconductor on the two side parts of said i-type semiconductor film. Said gate lines (5) are formed as wiring on substrate (1), and the gate electrodes of TFTs (4) are formed integrally on substrate (1). The gate insulating film (transparent film) of said TFTs (4) are formed on the entire region of said display area E. Said data lines are formed as wiring on said gate insulating film and are connected to the drain electrodes of TFTs (4). Said pixel electrodes (3) are formed on the gate insulating film, and they are connected to the source electrodes of TFTs (4).

[0021]

On the inner surface of said rear side substrate (1), near each of the corner parts, relay electrode (7) for connecting to the opposing electrode set on the other substrate (outer side substrate) (2) is formed such that it partially or entirely projects to the outer side of the joint part made of sealant (11).

[0022]

Among said relay electrodes (7), the relay electrode (7) set at the corner part between the substrate edge part where gate line terminals (5b) are set and the substrate edge part where data line terminals (6b) are set is connected to the terminal on one side among driver connecting terminals (7a) formed on the two end sides of the group of data line terminals (6b) via lead wiring (7b) set along the outer periphery of said joint part. On the other hand, relay electrodes (7) set at the remaining three corner parts are commonly connected by lead wiring (7c) set by wiring along the outer periphery of said joint part, and are connected via said lead wiring (7c) to terminals (7a) as the other end side of the group of data line terminals (6b).

[0023]

In addition, as shown in Figures 1-3, among the joint parts made of sealant (11) on the inner surface of said rear side substrate (1), almost the entire region (the area encircled by broken lines in Figures 1, 2), excluding the regions where lead parts (5a), (6a) of gate lines (5) and data lines (6) pass and the parts where relay electrodes (7) overlap, (the region defined by the broken

line in Figure 2) is considered the dummy film forming region D. In said dummy film forming region D, plural dummy films (8) are set at a prescribed interval over the entire region of said dummy film forming region D.

[0024]

Said dummy films (8) are set on the inner side with respect to the outer periphery of said sealant (11). In this application example, dummy films (8) are formed as fine linear parts along the width direction of sealant (11). Said linear dummy films (8) are set from the position near the inner side of the joint part with respect to the inner periphery of the joint part made of sealant (11) to nearly the central part of the width of the joint part.

[0025]

Said dummy films (8) are formed with width slightly larger than that of lead parts (5a), (6a) of said gate lines (5) and data lines (6). The spacing between dummy films (8), (8) is set to be smaller than the spacing between lead parts (5a), (5a) and (6a), (6a).

[0026]

That is, for example, if the diagonal size of the display screen is 4.7 inches, and the liquid crystal cell has 240×640 pixels, the width of said lead parts (5a), (6a) is about 30 μm, and the spacing between said lead parts (5a), (5a), (6a), (6a) is about 150 μm. In this application example, dummy films (8) are formed in a linear shape with a length about half the width of the joint part, and, at the same time, the width of dummy films (8) is about 50 μm, and the spacing between dummy films (8), (8) is set at about 50 μm.

[0027]

Said dummy films (8) and relay electrodes (7) are formed as metal films (such as aluminum alloy films), like gate lines (5) formed by the wiring on substrate (1). Also, said data lines (6) are formed as a metal film (such as aluminum alloy film) with nearly the same film thickness as that of said gate lines (5).

[0028]

Consequently, the film thickness of said dummy films (8) and relay electrodes (7) is equal to that of lead parts (5a) of gate lines (5) (about 0.3-0.4 μm), and it is also nearly equal to the film thickness of lead parts (6a) of data lines (6).

[0029]

As shown in Figure 4, on the inner surface of outside substrate (2), light-shielding film (9) with openings formed in the parts corresponding to the various pixels and opposing electrode (10) facing all of said pixel electrodes (3), as well as lead parts (10a), (9a) extending from the vicinity of the corner parts of opposing electrode (10) and light-shielding film (9) to the outer side of sealant (11) are formed. The end parts of said lead parts (10a), (9a) are set facing relay electrodes (7) formed on said rear side substrate (1).

[0030]

Said opposing electrode (10) is a film-shaped transparent electrode corresponding to the entire region of display area E. Said opposing electrode (10) is formed over the entire region of the liquid crystal sealed-in region surrounded with sealant (11), with its outer peripheral part formed in a size with a small superimposed width on the inner peripheral edge of said sealant (11).

[0031]

In this application example, opposing electrode (10) is formed on the surface of outside substrate (2), and light-shielding film (9) is formed thereon. Said light-shielding film (9) is a laminated film consisting of a chromium film and a chromium oxide film. Here, the chromium oxide film with low reflectivity is set facing the outer surface of outside substrate (2), that is, the display surface.

[0032]

The contours of said light-shielding film (9) and its lead part (9a) are slightly smaller than that of opposing electrode (10) and plasma generating region (10a), and, on lead part (9a) of said light-shielding film (9), opening (9b) is formed to expose lead part (10a) of said opposing electrode (10).

[0033]

Although not shown in the figure, on the inner surface of said rear side substrate (1), an orienting film is formed to cover said pixel electrodes (3) and TFTs (4). On the inner surface of said outside substrate (2), an orienting film for covering said opposing electrode (10) and light-shielding film (9) is formed. Said orienting films are made of polyimide or other horizontal orienting agent, and an orientation process is performed by rubbing the film surface.

[0034]

Said orienting films are formed over the entire region of display area E by avoiding the bonding parts made of sealant (11) so that its outer periphery does not superpose sealant (11).

[0035]

On the other hand, said sealant (11) is made of a thermosetting or light-curable resin. Mixed in the resin are ball-shaped gap members (12) for defining the cell gap (resin grains or grains made of metal or the like and having the entire outer surface coated with resin) (see Figure 5).

[0036]

The liquid crystal cell in this application example is prepared as follows: on one of said pair of substrates (1), (2), e.g., rear side substrate (1), said sealant (11) is printed to form a frame-like pattern to define the liquid crystal sealed region. On each lead part (10a) of said opposing electrode (10) on the other substrate, that is, outside substrate (2), conductive material (13) with gold grains mixed in a thermosetting or light-curable resin (see Figure 1) is applied dropwise. Then, said two substrates (1), (2) are superimposed under pressure, so that the spacing (cell gap) between said substrates (1), (2) is adjusted to the spacing defined by gap members (12) in sealant (11). In this state, sealant (11) and said conductive material (13) are cured so that said two substrates (1), (2) are bonded to each other for assembly.

[0037]

As the liquid crystal cell is assembled in this way, lead parts (10a) of opposing electrode (10) on outside substrate (2) are electrically connected via relay electrodes (7) of rear side substrate (1) and said conductive material (13) in the exposed parts on the periphery of lead part (9a) of said light-shielding film (9) and in said opening (9b).

[0038]

Also, inside said liquid crystal cell, that is, in the liquid crystal sealed region defined by sealant (11) of two substrates (1), (2), liquid crystal injection port (14) (see Figure 1), formed as a partial void in said sealant (11), is used to inject and fill the liquid crystal using the vacuum injection method. Then, said liquid crystal injection port (14) is sealed with sealing resin (15).

[0039]

The molecules of the liquid crystal sealed in the liquid crystal cell have their orientation direction defined near substrates (1), (2) by means of the orienting films formed on said two

substrates (1), (2), and they are oriented in the prescribed orientation state, such as in the twisted orientation state, between substrates (1), (2).

[0040]

For said liquid crystal cell of the present invention, among said pair of substrates (1), (2), on the joint part made of sealant (11) on the inner surface of rear side substrate (1) where pixel electrodes (3), TFTs (4), gate lines (5) and data lines (6) are formed, plural dummy films (8) are formed at prescribed intervals over almost the entire region, excluding the regions where lead parts (5a), (6a) of gate lines (5) and data lines (6) pass. As a result, the cell gap of the regions where lead parts (5a), (6a) pass among the regions of the joint part made of sealant (11) is defined by gap member (12) on said lead parts (5a), (6a), while the cell gap of the remaining region is defined by the gap members on dummy films (8) having nearly the same film thickness as that of said lead parts (5a), (6a).

[0041]

In said liquid crystal cell, because the film thickness of said dummy films (8) is nearly equal to that of lead parts (5a), (6a), the cell gap defined by gap member (12) on lead parts (5a), (6a) is nearly equal to that defined by the gap members on dummy films (8). Consequently, it is possible to minimize the variation of the cell gap.

[0042]

As a result, when said liquid crystal cell is used in the liquid crystal display device of the birefringence effect type that displays plural colors by means of changing the value of $\Delta n \cdot d$ of the liquid crystal cell corresponding to the applied voltage by exploiting the birefringence effect of the liquid crystal (or the birefringence effect of the liquid crystal and the phase difference sheet) and the polarization effect of the polarization sheet, there is little variation in color caused by variation in the cell gap of the liquid crystal cell, and it is possible to realize a high-quality color display.

[0043]

Also, in said liquid crystal cell, because said dummy films (8) are set on the inner side with respect to the outer periphery of sealant (11), the outer peripheral part of sealant (11) can make direct close contact with the surfaces of substrates (1), (2), so that a high sealing property can be realized, and, at the same time, it is possible to prevent external impurities from passing through said dummy films (8) and entering the cell.

[0044]

Also, in said application example, while dummy films (8) are formed in a linear shape along the width direction of said sealant (11), the width of dummy films (8) is selected to be larger than that of lead parts (5a), (6a), and the spacing between dummy films (8), (8) is smaller than the spacing between lead parts (5a), (5a) and (6a), (6a). As a result, the ratio of the spacing between dummy films (8) to the width of dummy films (8) is less than the ratio of the spacing between lead parts (5a), (6a) to the width of said lead parts (5a), (6a), so that the number of gap members (12) of each lead part on lead parts (5a), (6a) passing through the entire width of said joint part can be balanced by the number of gap members (12) for each dummy film on dummy films (8) with the length smaller than the width of said joint part.

[0045]

That is, in said application example, the number of gap members (12) for each dummy film on dummy films (8) with the length smaller than the width of said joint part is larger than the number of gap members (12) of each lead part on lead parts (5a), (6a) passing through the entire width of said joint part. Consequently, for the density of gap members (12) on the lead parts and dummy film effective in defining the cell gap, the density on lead parts (5a), (6a) with the smaller length in the width direction of said joint part is lower than that on dummy films (8) with the smaller length in the width direction of said joint part. Consequently, the effect of said gap members (12) in defining the cell gap is nearly the same over the entire circumference of the joint part, and the variation of the cell gap can be further reduced.

[0046]

Figure 5 shows gap members (12) in an exaggerated form in the figure for clarity. For a liquid crystal cell for use in a birefringence effect type liquid crystal display device, the cell gap is set at 4-5 μm using gap members with diameter of 4-5 μm. On the other hand, the width of sealant (11) is about 1000 μm. Consequently, in practice, plural gap members (12) are distributed on the lead parts and the dummy films.

[0047]

Said first application example is not limited to the active matrix type display using TFTs as the active elements. For example, it may also be adopted in the active matrix type liquid crystal cell using MIM-structure nonlinear resistance elements as the active elements and the simple matrix type liquid crystal cell, etc.

[0048]

For said active matrix type liquid crystal cell using said nonlinear resistance elements as the active elements, on the inner surface of one substrate, plural pixel electrodes set in matrix configuration, plural active elements connected to said pixel electrodes, respectively, and signal supply lines for supplying an on signal to the active elements on each row are set. On the other substrate, plural opposing electrodes divided into each pixel columns are set. Here, on the bonding part made of sealant on the inner surface of said one substrate, plural dummy films with film thicknesses nearly equal to that of the lead parts of said signal supplying lines are set with a prescribed spacing between them on almost the entire region excluding the regions where said lead parts pass. On said bonding part on the inner surface of the other substrate, plural dummy films with film thicknesses nearly equal to that of the lead parts of said opposing electrodes are set with a prescribed spacing between them over almost the entire region excluding the region where said lead parts pass. As a result, it is possible to have a uniform cell gap.

[0049]

For said simple matrix type liquid crystal cell, on the inner surface of one substrate, plural scanning electrodes are set along the row direction. On the other substrate, plural scanning electrodes are set along the column direction. Here, on the bonding part made of the sealant on the inner surface of said one substrate, plural dummy films with film thicknesses nearly equal to that of the lead parts of said scanning electrodes are formed with a prescribed spacing between them over almost the entire region excluding the region where said lead parts pass. On said bonding part on the inner surface of the other substrate, plural dummy films with nearly the same film thickness as that of the lead parts of said signal electrodes are formed with a prescribed spacing between them on almost the entire region excluding the region where said lead parts pass. As a result, it is possible to have a uniform cell gap.

[0050]

Figures 6 and 7 illustrate Application Example 2 of the present invention. Figure 6 is a plan view illustrating a part of the substrate where the opposing electrodes are formed. Figure 7 includes enlarged cross-sectional views illustrating a part of said liquid crystal cell. (a) is a cross-sectional view taken across A'-A' in Figure 6, and (b) is a cross-sectional view taken across B'-B' in Figure 6.

[0051]

This application example provides a further improved version of the liquid crystal cell in said Application Example 1. It provides an active matrix type liquid crystal cell using TFTs as

the active elements. In this liquid crystal cell, both opposing electrode (10) and light-shielding film (9) formed on outside substrate (2) have a contour such that the outer peripheral part is formed corresponding to within the joint part made of sealant (11).

[0052]

In this application example, the contour containing lead part (9a) of light-shielding film (9) is the same as that of opposing electrode (10) (the contour containing lead part (10a)), and, at the same time, said opposing electrode (10) and light-shielding film (9) are formed of an appropriate size such that the outer peripheral edge of the part other than said lead parts (10a), (9a) is located on the inner side with respect to the outer periphery of sealant (11) (here, the outer peripheral edge is at about the middle of the width of sealant (11)).

[0053]

For the liquid crystal cell in this application example, the constitution is the same as that in said Application Example 1, except that said opposing electrode (10) and light-shielding film (9) are formed with said contour. The same symbols as those adopted in the above are adopted, and they will not be explained again.

[0054]

For the liquid crystal cell in this application example, the cell gap of the region where lead parts (10a), (9a) extending from opposing electrode (10) and light-shielding film (9) among the regions of the joint part made of sealant (11) is defined by gap members (12) on lead parts (10a), (9a), while the cell gap of the remaining region is defined by gap members (12) on the outer peripheral part of opposing electrode (10) and light-shielding film (9). Because the film thickness of the outer peripheral part of opposing electrode (10) and light-shielding film (9) is equal to that of said lead parts (10a), (9a), the variation of the cell gap can be minimized.

[0055]

That is, for the liquid crystal cell in said Application Example 1, as shown in Figure 4, only opposing electrode (10) is superimposed with sealant (11), while light-shielding film (9) is not superimposed on sealant (11). Consequently, among the regions of the joint part made of sealant (11) on the inner surface of said outside substrate (2), the region where said lead parts (10a), (9a) pass has a thicker film thickness than the region overlapped with only the outer peripheral part of said opposing electrode (10) by the film thickness of light-shielding film (9).

[0056]

While the film thickness of opposing electrode (10) is about 0.05 μm, the film thickness of light-shielding film (9) made of a laminate of a chromium film and a chromium oxide film is about 0.20 μm. Consequently, there is a step of about 0.20 μm between the region of said bonding part of outside substrate (2) where lead parts (10a), (9a) pass and the region where only the outer peripheral part of opposing electrode (10) overlaps.

[0057]

Consequently, for the liquid crystal cell in said Application Example 1, in the region of said bonding part where lead parts (10a), (9a) of opposing electrode (10) and light-shielding film (9) pass, the cell gap is larger by the film thickness of light-shielding film (9).

[0058]

Now, in Application Example 2, both opposing electrode (10) and light-shielding film (9) are formed such that the outer peripheral part has a contour corresponding to within the bonding part made of sealant (11). Consequently, there is no step between the region of said bonding part of outside substrate (2) where lead parts (10a), (9a) pass and the region where the outer peripheral parts of opposing electrode (10) and light-shielding film (9) overlap. Consequently, it is possible to minimize the variation of the cell gap.

[0059]

Also, in this application example, as in said Application Example 1, on the bonding part made of sealant (11) on the inner surface of rear side substrate (1), plural dummy films (8) with film thicknesses nearly equal to that of lead parts (5a), (6a) of gate lines (5) and data lines (6) are formed with a prescribed spacing between them on almost the entire region excluding the region where said lead parts (5a), (6a) pass. Consequently, it is possible to almost entirely eliminate the variation of the cell gap.

[0060]

Consequently, when the liquid crystal cell in this application example is used on a birefringence effect type liquid crystal display device, there is no variation in color caused by variation of the cell gap of the liquid crystal cell, and it is possible to realize an even higher quality of color display.

[0061]

Also, for the liquid crystal cell of said Application Example 2, the outer peripheral edges of opposing electrode (10) and light-shielding film (9) of outside substrate (2) are positioned on the inner side from the outer periphery of sealant (11), and dummy films (8) formed on rear side substrate (1) are also on the inner side from the outer periphery of sealant (11), so that it is possible to have the outer peripheral part of sealant (11) in direct close contact with the surfaces of two substrates (1), (2), so that a high sealing property can be realized. At the same time, it is possible to prevent the external impurities from passing through opposing electrode (10) and light-shielding film (9) or through dummy films (8) and entering the cell.

[0062]

The present invention is not limited to the liquid crystal cell for use in the birefringence effect type liquid crystal display device. It may also be adopted in the liquid crystal cells for use in the STN type liquid crystal display device and ferroelectric liquid crystal display device, for which even a small variation can influence the display characteristics, as well as the TN type liquid crystal display device.

[0063]

Effects of the invention

The present invention provides a liquid crystal cell characterized by the following facts: for the liquid crystal cell, liquid crystal is sealed between a pair of substrates bonded to each other via a frame-like sealant consisting of a resin including gap material that defines the cell gap, and, at the same time, on the inner surfaces of said pair of substrates, electrodes corresponding to the display area and lead parts extending to the outside of said sealant are formed, respectively; for this liquid crystal cell, plural dummy films with film thicknesses nearly equal to that of said lead parts are formed on the joint part joined by the sealant on the inner surface of at least one substrate at a prescribed interval over almost the entire region, excluding the regions where said lead parts pass. Consequently, it is possible to minimize the variation of the cell gap.

[0064]

Also, the present invention provides a liquid crystal cell characterized by the following facts: for the liquid crystal cell of the active matrix type, liquid crystal is sealed between a pair of substrates bonded to each other via a frame-like sealant consisting of a resin including gap material that defines the cell gap, and, at the same time, on the inner surfaces of one substrate, plural pixel electrodes set in matrix configuration corresponding to the display area, plural thin-

film transistors connected to said pixel electrodes, respectively, gate lines and data lines for supplying gate signal and data signal to said thin-film transistors, and lead parts extending from said lines to the outside of said sealant are formed, on the inner surface of the other substrate, a light-shielding film opening at the parts corresponding to the various pixels, opposing electrode corresponding to the entire region of said display area, and lead parts extending out from said opposing electrode and said light-shielding film are formed; in this active matrix type liquid crystal cell, both said opposing electrode and said light-shielding film have their outer peripheral parts formed with a contour corresponding to the interior of the joint part made of said sealant. Consequently, it is possible to minimize the variation of the cell gap.

[0065]

According to the present invention, the outer peripheral edges of said opposing electrode and said light-shielding film are on the inner side with respect to the outer periphery of the sealant. As a result, the outer peripheral part of the sealant and the substrate surfaces can be in direct close contact with each other so that the sealing property can be improved. At the same time, it is possible to prevent external impurities from passing through the opposing electrode and the light-shielding film and entering the cell.

[0066]

In addition, for said active matrix type liquid crystal cell, plural dummy films with film thicknesses nearly equal to that of the lead parts are set at a prescribed spacing over almost the entire region, excluding the regions where said lead parts pass, on the joint part made of the sealant on the inner surface of one substrate where said pixel electrodes, thin-film transistors, gates, and data lines are formed. In this way, it is possible to eliminate the variation in the cell gap almost entirely.

[0067]

Also, according to the present invention, the dummy films are set on the inner side with respect to the outer periphery of the sealant. In this way, the outer peripheral part of the sealant is in close direct contact with the substrate surfaces, so that a high sealing property can be realized, and, at the same time, it is possible to prevent external impurities from passing through said dummy film and entering the cell.

[0068]

When said dummy film is formed on the inner side with respect to the outer periphery of the sealant, the dummy films are formed in a linear shape along the width direction of the

sealant, and the ratio of the spacing between the dummy films to the width of the dummy film is smaller than that ratio of the spacing between the lead parts to the width of the lead part. In this way, the number of gap members per unit area of the lead part passing through the entire width of said joint part is larger than the number of gap members per unit area of the dummy film with a length smaller than the width of said joint part, so that for the density of the gap members per the lead parts and on the dummy films that are effective in defining the cell gap, the value of the density on the lead part with larger length in the width direction of said joint part is smaller than that on the dummy film with smaller length in the width direction of said joint part. Consequently, the effect of the gap members in defining the cell gap is nearly the same over the entire circumference of the joint part, and it is possible to further reduce the variation in the cell gap.

Brief description of the figures

Figure 1 is a plan view of the liquid crystal cell in Application Example 1 of the present invention.

Figure 2 is a plan view of one of the substrates of said liquid crystal cell.

Figure 3 is an enlarged view of a part of Figure 2.

Figure 4 is an enlarged plan view illustrating a part of the other substrate of said liquid crystal cell.

Figure 5 includes enlarged cross-sectional views illustrating a part of said liquid crystal cell. (a) is a cross-sectional view along A-A in Figure 3. (b) is a cross-sectional view along B-B in Figure 3.

Figure 6 is a plan view illustrating a part of the substrate where the opposing electrode is formed in Application Example 2 of the present invention.

Figure 7 includes enlarged cross-sectional views illustrating a part of said liquid crystal cell. (a) is a cross-sectional view along A'-A' in Figure 6. (b) is a cross-sectional view along B'-B' in Figure 6.

Explanation of symbols

E	Display area
1, 2	Substrate
3	Pixel electrode
4	TFT
5	Gate line
5a, 6a	Lead part
6	Data line

7	Relay electrode
8	Dummy film
9	Light-shielding film
9a, 10a	Lead part
10	Opposing electrode
11	Sealant
12	Gap member
13	Conductive material

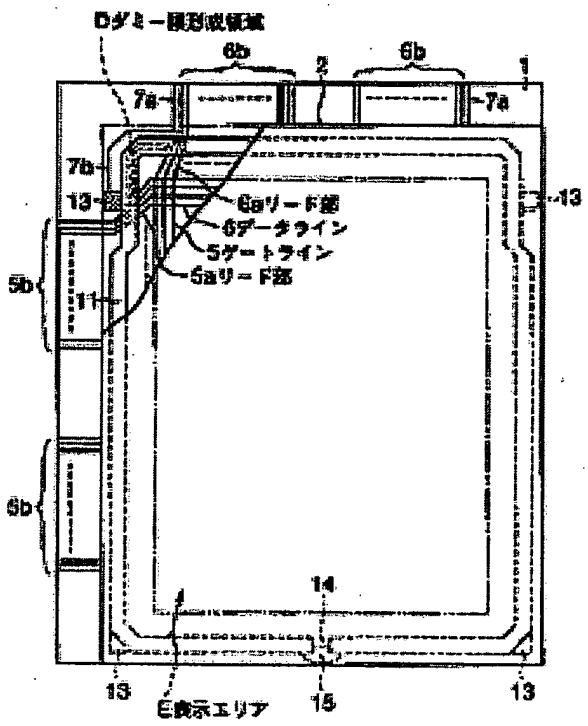


Figure 1

Key:

5	Gate line
5a	Lead part
6	Data line
6a	Lead part
D	Dummy film forming region
E	Display area

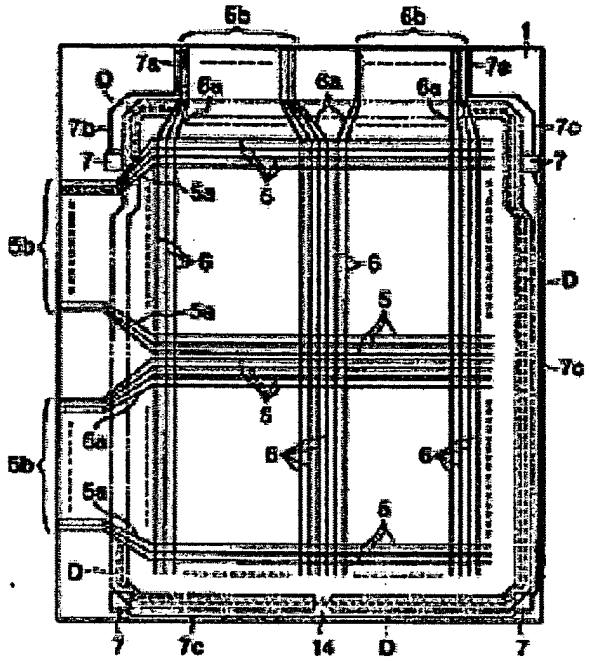


Figure 2

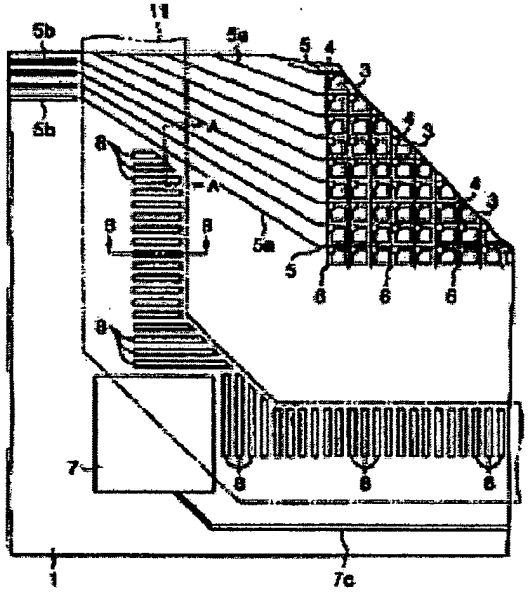


Figure 3

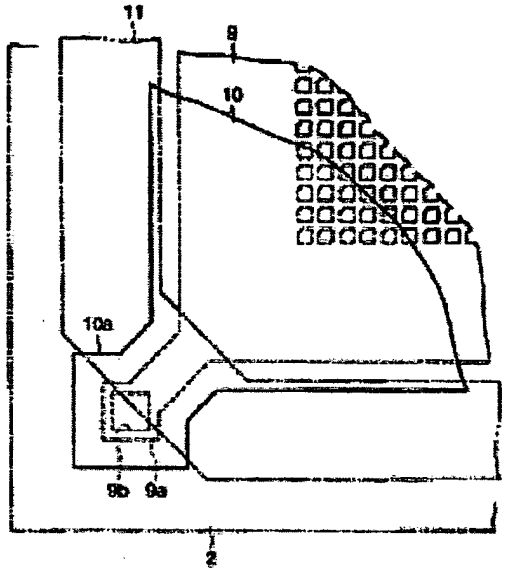


Figure 4

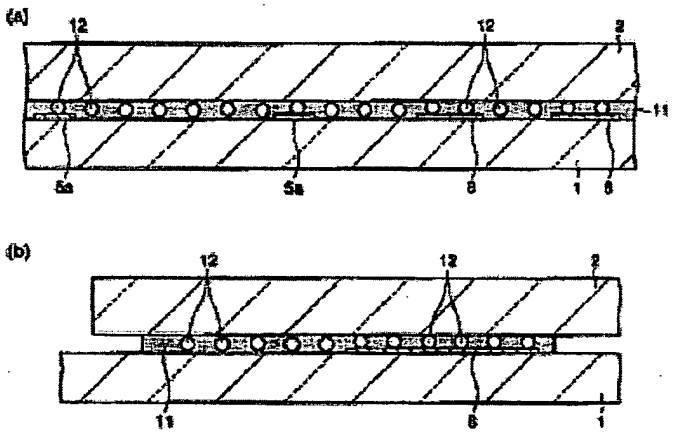


Figure 5

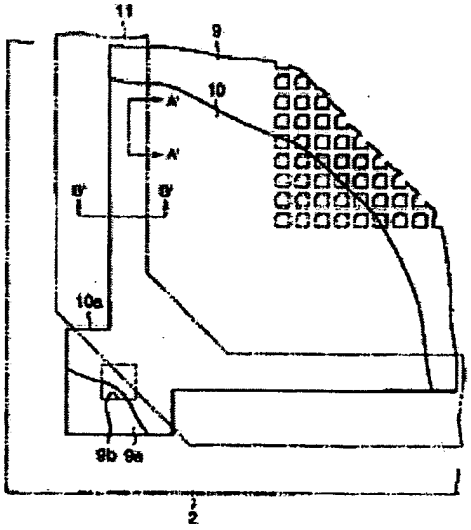


Figure 6

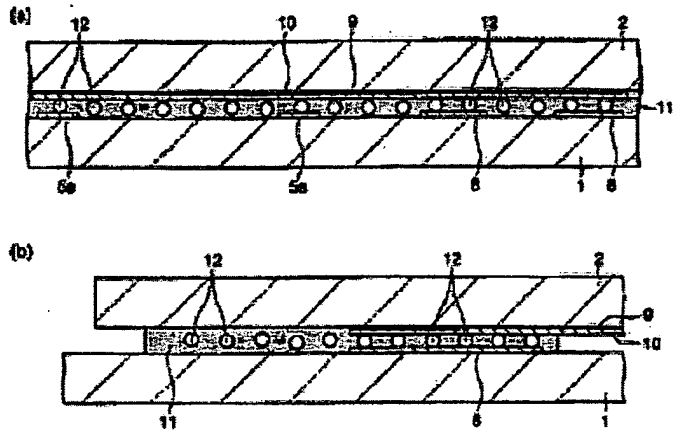


Figure 7

February 11, 2009

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To Whom It May Concern:

This is to certify that a professional translator on our staff who is skilled in the Japanese language translated "JP09197415A" from Japanese into English.

We certify that the English translation conforms essentially to the original Japanese language.

K Vitray

Kim Vitray
Operations Manager

Subscribed and sworn to before me this 11th day of February, 2009.

VICKI L. WUNNEBURGER
Notary Public, State of Texas
My Commission Expires
March 09, 2011

Vicki L Wunneburger

Vicki Wunneburger
Notary Public

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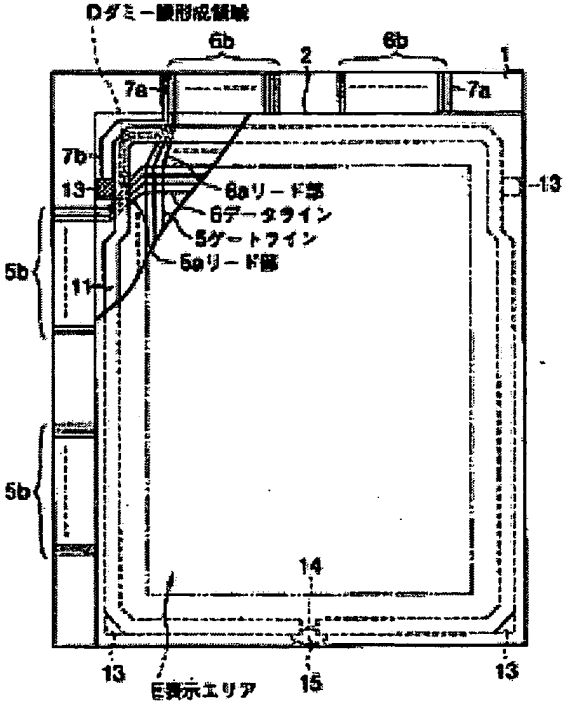
(54)【発明の名称】　液晶セル

(57)【要約】
【課題】セルギャップのばらつきを極く小さくする。
【解決手段】ギャップ材を混入した樹脂からなる枠状のシール材１１を介して接合された一対の基板１，２間に液晶が封入されるとともに、前記一対の基板１，２の内面にそれぞれ、表示エリアＥに対応する電極と、前記シール材１１の外側に延出するリード部５ａ，６ａとが形成された液晶セルにおいて、少なくとも一方の基板１の内面の前記シール材１１による接合部に、前記リード部５ａ，６ａとほぼ同じ膜厚の複数のダミー膜を、前記リード部が通っている領域を除くほぼ全域にわたって所定間隔で設けた。



【特許請求の範囲】
【請求項１】セルギャップを規制するギャップ材を混入した樹脂からなる枠状のシール材を介して接合された一対の基板間に液晶が封入されるとともに、前記一対の基板の内面にそれぞれ、表示エリアに対応する電極と、前記シール材の外側に延出するリード部とが形成された液晶セルにおいて、
少なくとも一方の基板の内面の前記シール材による接合部に、前記リード部とほぼ同じ膜厚の複数のダミー膜を、前記リード部が通っている領域を除くほぼ全域にわたって所定間隔で設けたことを特徴とする液晶セル。
【請求項２】セルギャップを規制するギャップ材を混入した樹脂からなる枠状のシール材を介して接合された一対の基板間に液晶が封入されるとともに、一方の基板の内面に、表示エリアに対応させてマトリックス状に配列された複数の画素電極と、これらの画素電極にそれぞれ接続された複数の薄膜トランジスタと、これらの薄膜トランジスタにゲート信号およびデータ信号を供給するゲートラインおよびデータラインと、これらのラインから前記シール材の外側に延出するリード部とが形成され、他方の基板の内面に、各画素に対応する部分が開口する遮光膜と、前記表示エリアの全域に対応する対向電極と、この対向電極および前記遮光膜から前記シール材の外側に延出するリード部とが形成されたアクティブマトリックス型の液晶セルにおいて、
前記前記対向電極と遮光膜の両方を、その外周部が前記シール材による接合部内に対応する外形に形成したことを特徴とする液晶セル。
【請求項３】対向電極と遮光膜の外周縁は、シール材の外周よりも内側にあることを特徴とする請求項２に記載の液晶セル。
【請求項４】一方の基板の内面のシール材による接合部に、リード部とほぼ同じ膜厚の複数のダミー膜が、前記リード部が通っている領域を除くほぼ全域にわたって所定間隔で設けられていることを特徴とする請求項２に記載の液晶セル。
【請求項５】ダミー膜は、シール材の外周よりも内側に設けられていることを特徴とする請求項１または請求項４に記載の液晶セル。
【請求項６】ダミー膜は、シール材の幅方向に沿う線状に形成されており、このダミー膜の幅に対する各ダミー膜の間隔の比が、リード部の幅に対する各リード部の間隔の比よりも小さいことを特徴とする請求項５に記載の液晶セル。

【発明の詳細な説明】
【０００１】
【発明の属する技術分野】この発明は液晶表示装置に用いる液晶セルに関するものであって、セルギャップの均一度をより高くしたものである。
【０００２】
【従来の技術】液晶表示装置には、一般に利用されているＴＮ型のもののほかに、液晶分子のツイスト角を１８０°～２７０°と大きくしたＳＴＮ型、カラーフィルタを用いずに着色した表示を得る複屈折効果型、強誘電性液晶または反強誘電性液晶を使用するもの等があり、これらの液晶表示装置は、一般に、液晶セルと、この液晶セルをはさんで配置された一対の偏光板とで構成されている。なお、複屈折効果型の液晶表示装置には、液晶セルと偏光板との間に位相差板を配置しているものもある。
【０００３】上記液晶セルは、ガラス等からなる一対の基板を、セルギャップ（基板間隙）を規制するギャップ材を混入した樹脂からなる枠状のシール材を介して接合し、これらの基板間の前記シール材で囲まれた領域に液

晶を封入したもので、前記一対の基板の内面にはそれぞれ、表示エリアに対応する透明な電極と、前記シール材の外側に延出するリード部とが形成されている。
【０００４】なお、前記一対の基板の表示エリアの内面には、前記電極を覆って、液晶分子の配向状態を規制する配向膜が設けられている。また、カラーフィルタを用いて着色した表示を得る液晶表示装置（ＴＮ型、ＳＴＮ型、強誘電性液晶表示装置等の）に用いられる液晶セルでは、いずれか一方の基板の内面（電極の下あるいは前記電極と配向膜との間）にカラーフィルタを設けている。
【０００５】
【発明が解決しようとする課題】ところで、上記液晶表示装置の表示特性は、液晶層の層厚や液晶分子の配向状態によって変化するため、表示むらの無い高品質の表示を得るには、液晶セルの液晶層厚、つまりセルギャップを、セル全体にわたって均一にすることが必要である。
【０００６】このセルギャップは、両基板を接合するシール材に混入されたギャップ材で規制されているが、前記シール材による接合部のうちのリード部が通っている領域のセルギャップは、リード部の上のギャップ材で規制され、他の領域のセルギャップは、基板面に接するギャップ材で規制されるため、上記液晶セルのセルギャップには、前記リード部の膜厚に応じたばらつきがある。
【０００７】このセルギャップのばらつき、つまり、前記接合部のうちのリード部が通っている領域と他の領域とのセルギャップの差は、例えば薄膜トランジスタを能動素子とするアクティブマトリックス型液晶セルの場合で０．３～０．４μｍ程度であり、一般に利用されているＴＮ型液晶表示装置ではほとんど問題にならない精度である。
【０００８】しかし、ＳＴＮ型、複屈折効果型の液晶表示装置や、強誘電性液晶表示装置等においては、液晶セルのセルギャップの僅かなばらつきも表示特性に影響し、例えば、液晶の複屈折効果（または液晶および位相差板の複屈折効果）と偏光板の偏光作用とを利用し、印加電圧に対応した液晶セルのΔｎ・ｄ（液晶の屈折率異方性Δｎと液晶層厚ｄとの積）の変化によって複数の色を表示する複屈折効果型の液晶表示装置では、僅かなセルギャップのばらつきが表示の色むらとなって現れる。この発明は、セルギャップのばらつきを極く小さくすることができる液晶セルを提供することを目的としたものである。
【０００９】
【課題を解決するための手段】この発明は、セルギャップを規制するギャップ材を混入した樹脂からなる枠状のシール材を介して接合された一対の基板間に液晶が封入されるとともに、前記一対の基板の内面にそれぞれ、表示エリアに対応する電極と、前記シール材の外側に延出するリード部とが形成された液晶セルにおいて、少なくとも一方の基板の内面の前記シール材による接合部に、前記リード部とほぼ同じ膜厚の複数のダミー膜を、前記リード部が通っている領域を除くほぼ全域にわたって所定間隔で設けたことを特徴とするものである。
【００１０】この発明によれば、シール材による接合部のうちのリード部が通っている領域のセルギャップが、前記リード部の上のギャップ材で規制され、他の領域のセルギャップが、前記リード部とほぼ同じ膜厚を有するダミー膜の上のギャップ材で規制されるため、セルギャップのばらつきを極く小さくすることができる。
【００１１】また、この発明は、セルギャップを規制するギャップ材を混入した樹脂からなる枠状のシール材を介して接合された一対の基板間に液晶が封入されるとともに、一方の基板の内面に、表示エリアに対応させてマトリックス状に配列された複数の画素電極と、これらの画素電極にそれぞれ接続された複数の薄膜トランジスタと、これらの薄膜トランジスタにゲート信号およびデータ信号を供給するゲートラインおよびデータラインと、これらのラインから前記シール材の外側に延出するリー

ド部とが形成され、他方の基板の内面に、各画素に対応する部分が開口する遮光膜と、前記表示エリアの全域に対応する対向電極と、この対向電極および前記遮光膜から前記シール材の外側に延出するリード部とが形成されたアクティブマトリックス型の液晶セルにおいて、前記対向電極と前記遮光膜の両方を、その外周部が前記シール材による接合部内に対応する外形に形成したことを特徴とするものである。

【００１２】この発明によれば、シール材による接合部のうちの対向電極および遮光膜から延出するリード部が通っている領域のセルギャップが、前記リード部の上のギャップ材で規制され、他の領域のセルギャップが、対向電極および遮光膜の外周部の上のギャップ材で規制されるが、前記対向電極および遮光膜の外周部と前記リード部の膜厚は同じであるため、セルギャップのばらつきを極く小さくすることができる。

【００１３】この発明において、前記対向電極と遮光膜の外周縁は、シール材の外周よりも内側にあるのが望ましく、このようにすれば、シール材の外周部分と基板面とを直接密着させて高いシール性を得ることができるとともに、外部から不純物が対向電極および遮光膜を伝ってセル内に侵入するのを防止することができる。

【００１４】また、上記アクティブマトリックス型の液晶セルにおいては、画素電極および薄膜トランジスタとゲート，データラインを形成した上記一方の基板の内面のシール材による接合部に、前記ゲート，データラインのリード部とほぼ同じ膜厚の複数のダミー膜を、前記接合部のうちの前記リード部が通っている領域を除くほぼ全域にわたって所定間隔で設けるのがさらに好ましく、このようにすれば、セルギャップのばらつきをほぼ完全に無くすことができる。

【００１５】この発明において、上記ダミー膜は、シール材の外周よりも内側に設けるのが望ましく、このようにすれば、シール材の外周部分を基板面に直接密着させて高いシール性を得ることができるとともに、外部から不純物が前記ダミー膜を伝ってセル内に侵入するのを防止することができる。

【００１６】また、前記ダミー膜をシール材の外周よりも内側に設ける場合は、このダミー膜をシール材の幅方向に沿う線状に形成するとともに、前記ダミー膜の幅に対する各ダミー膜の間隔の比を、前記リード部の幅に対する各リード部の間隔の比よりも小さくするのが望ましく、このようにすれば、前記接合部をその全幅にわたって通っているリード部の上にある単位面積当たりのギャップ材の数よりも、前記接合部の幅より小さい長さのダミー膜の上にある単位面積当たりのギャップ材の数が多くなり、セルギャップの規制に有効なリード部上およびダミー膜上のギャップ材の密度が、前記接合部の幅方向の長さが小さい各ダミー膜上に比べて前記接合部の幅方向の長さが大きい各リード部上の方が小さくなるから、これらのギャップ材によるセルギャップの規制効果を接合部全周にわたってほぼ等しくし、セルギャップのばらつきをより小さくすることができる。

【００１７】

【発明の実施の形態】以下、この発明の実施の形態を図面を参照して説明する。図１～図５はこの発明の第１の実施例を示しており、図１は液晶セルの平面図、図２はその一方の基板の平面図、図３は図２の一部分の拡大図、図４は他方の基板の一部分の拡大平面図である。図５は前記液晶セルの一部分の拡大断面図であって、（ａ）は図３のＡ－Ａ線に沿った断面図、（ｂ）は図３のＢ－Ｂ線に沿った断面図である。

【００１８】この実施例の液晶セルは、図１～図５に示すように、ガラス等からなる一対の透明基板１，２を枠状のシール材１１を介して接合し、これらの基板１，２間の前記シール材１１で囲まれた領域に液晶（図示せず）を封入したもので、前記一対の基板１，２の内面にはそれぞれ、表示エリアＥに対応する透明な電極と、前記シール材１１の外側に延出するリード部とが形成され

ている。
【００１９】なお、この実施例の液晶セルは、薄膜トランジスタ（以下、ＴＦＴと記す）を能動素子とするアクティブマトリックス型のものであり、一対の基板１，２のうちの一方、例えば裏側基板１の内面には、図１～図３に示すように、表示エリアＥに対応させてマトリックス状に配列された複数の透明画素電極３と、これらの画素電極３にそれぞれ接続された複数のＴＦＴ４と、これらのＴＦＴ４にゲート信号およびデータ信号を供給するゲートライン５およびデータライン６と、これらのライン５，６から前記シール材１１の外側に延出するリード部５ａ，６ａとが形成されており、これらのリード部５ａ，６ａの端部は駆動回路との接続端子５ｂ，６ｂとされている。
【００２０】なお、図では上記ＴＦＴ４を簡略化して示しているが、このＴＦＴ４は、基板１上に形成されたゲート電極と、このゲート電極を覆うゲート絶縁膜と、このゲート絶縁膜の上に前記ゲート電極と対向させて形成されたｉ型半導体膜と、このｉ型半導体膜の両側部の上にｎ型半導体膜を介して形成されたソース電極およびドレイン電極とからなっており、上記ゲートライン５は基板１上に配線され、ＴＦＴ４のゲート電極は前記ゲートラインに一体に形成されている。また、前記ＴＦＴ４のゲート絶縁膜（透明膜）は、表示エリアＥの全域にわたって形成されており、上記データラインは、前記ゲート絶縁膜の上に配線されてＴＦＴ４のドレイン電極に接続され、画素電極３はゲート絶縁膜の上に形成されてＴＦＴ４のソース電極に接続されている。
【００２１】また、上記裏側基板１の内面には、その各コーナー部の付近にそれぞれ、他方の基板（表側基板）２に設けた対向電極を駆動回路に接続するための中継電極７が、その一部または全部を上記シール材１１による接合部の外側に突出させて形成されている。
【００２２】これらの中継電極７のうち、ゲートライン端子５ｂが配列された基板縁部とデータライン端子６ｂが配列された基板縁部との間のコーナー部に設けられた中継電極７は、データライン端子６ｂ群の両端側にそれぞれ形成した駆動回路接続端子７ａのうちの一端側の端子に、前記接合部の外周に沿わせて配線したリード配線７ｂを介してつながっており、他の３つのコーナー部に設けられた各中継電極７は、前記接合部の外周に沿わせて配線したリード配線７ｃにより共通接続され、このリード配線７ｃを介してデータライン端子６ｂ群の他端側の端子７ａにつながっている。
【００２３】さらに、図１～図３に示すように、上記裏側基板１の内面のシール材１１による接合部のうち、ゲートライン５およびデータライン６のリード部５ａ，６ａが通っている領域と上記中継電極７がラップしている部分とを除くほぼ全域（図１および図２に破線で囲んで示した領域）は、ダミー膜形成領域Ｄとされており、この領域Ｄにはその全域にわたって、複数のダミー膜８が図３のように所定間隔で設けられている。
【００２４】これらのダミー膜８は、上記シール材１１の外周よりも内側に設けられている。この実施例では、ダミー膜８を、シール材１１の幅方向に沿う細幅の線状に形成し、この線状ダミー膜８を、前記シール材１１による接合部の内周より若干接合部内側に片寄った位置から接合部幅のほぼ中間位置にわたって設けている。
【００２５】また、このダミー膜８は、上記ゲートライン５およびデータライン６のリード部５ａ，６ａの幅よりもある程度大きな幅に形成されており、各ダミー膜８，８の間隔は、各リード部５ａ，５ａおよび６ａ，６ａの間隔よりも小さく設定されている。
【００２６】すなわち、例えば、表示画面の対角サイズが４．７インチで２４０×６４０ドットの画素数の液晶セルの場合、前記リード部５ａ，６ａの幅は約３０μｍ、各リード部５ａ，５ａおよび６ａ，６ａの間隔は約１５０μｍであるが、この実施例では、前記ダミー膜８を接合部幅のほぼ半分の長さの線状に形成したことあ

わせて、ダミー膜８の幅を約５０μｍ、各ダミー膜８，８の間隔を約５０μｍに設定している。

【００２７】さらに、このダミー膜８と上記中継電極７は、基板１上に配線した上記ゲートライン５と同じ金属膜（例えばアルミニウム系合金膜）で形成されており、また、上記データライン６は、前記ゲートライン５とほぼ同じ膜厚の金属膜（例えばアルミニウム系合金膜）で形成されている。

【００２８】したがって、上記ダミー膜８と中継電極７の膜厚は、ゲートライン５のリード部５ａの膜厚（０．３～０．４μｍ程度）と同じであり、またデータライン６のリード部６ａの膜厚ともほぼ同じである。

【００２９】また、表側基板２の内面には、図４に示すように、各画素に対応する部分が開口する遮光膜９と、上記画素電極３の全てに対向する対向電極１０と、この対向電極１０および前記遮光膜９の各コーナー部付近からシール材１１の外側に延出するリード部１０ａ，９ａとが形成されており、このリード部１０ａ，９ａの端部は、上記裏側基板１に形成した各中継電極７にそれぞれ対向している。

【００３０】上記対向電極１０は、表示エリアＥの全域に対応する一枚膜状の透明電極であり、この対向電極１０は、シール材１１で囲まれる液晶封入領域の全域に、その外周部が上記シール材１１の内周縁と僅かな重なり幅でラップする大きさに形成されている。

【００３１】また、この実施例では、基板２面に対向電極１０を形成し、その上に遮光膜９を形成している。この遮光膜９は、クロム膜と酸化クロム膜との積層膜からなっており、低反射膜である酸化クロム膜が、表示面つまり表側基板２の表面に対向している。

【００３２】この遮光膜９およびそのリード部９ａは、上記対向電極１０およびそのリード部１０ａの外形よりも若干小さい外形に形成されており、この遮光膜９のリード部９ａには、対向電極１０のリード部１０ａを露出させる開口９ｂが設けられている。

【００３３】また、図では省略しているが、上記裏側基板１の内面には、上記画素電極３やＴＦＴ４を覆って配向膜が形成され、上記表側基板２の内面には、対向電極１０および遮光膜９を覆って配向膜が形成されている。これらの配向膜は、ポリイミド等の水平配向剤からなっており、その膜面にラビングによる配向処理が施されている。

【００３４】なお、これらの配向膜は、その外周がシール材１１と重ならないように、シール材１１による接合部を避けて、少なくとも表示エリアＥの全域にわたって設けられている。

【００３５】一方、上記シール材１１は、熱硬化性または光硬化性樹脂からなっており、その樹脂中には、セルギャップを規制するための球形ギャップ材（樹脂粒または金属等からなる粒子の表面全体を樹脂コーティングしたもの）１２（図５参照）が混入されている。

【００３６】そして、この実施例の液晶セルは、上記一対の基板１，２のいずれか一方、例えば裏側基板１に上記シール材１１を液晶封入領域を囲む枠状に印刷し、他方の表側基板２の上記対向電極１０の各リード部１０ａの上にそれぞれ熱硬化性または光硬化性樹脂に金粒子を混入した導通材１３（図１参照）を滴下した後、両基板１，２を重ね合わせて加圧することによってこれらの基板１，２間の間隙（セルギャップ）をシール材１１中のギャップ材１２で規制される間隙に調整し、その状態でシール材１１および前記導通材１３を硬化させて両基板１，２を接合することにより組み立てられている。

【００３７】このようにして液晶セルを組み立てると、表側基板２の対向電極１０の各リード部１０ａが、上記遮光膜９のリード部９ａの周囲および上記開口９ｂ内の露出部において、裏側基板１の各中継電極７と上記導通材１３を介して電気的に接続される。

【００３８】また、この液晶セルの内部、つまり両基板１，２のシール材１１で囲まれて液晶封入領域には、前

記シール材１１を部分的に欠落させて形成しておいた液晶注入口（図１参照）１４から真空注入法によって液晶が注入充填され、その後、前記注入口１４が封止樹脂１５によって封止される。

【００３９】この液晶セル内に封入された液晶の分子は、両基板１，２にそれぞれ設けた配向膜によってそれぞれの基板１，２の近傍における配向方向を規制され、両基板１，２間において所定の配向状態、例えばツイスト配向状態に配向される。

【００４０】この実施例の液晶セルによれば、その一対の基板１，２のうち、画素電極３とＴＦＴ４とゲートライン５およびデータライン６を形成した裏側基板１の内面のシール材１１による接合部に、前記ゲートライン５およびデータライン６のリード部５ａ，６ａが通っている領域を除くほぼ全域にわたって複数のダミー膜８を所定間隔で設けているため、シール材１１による接合部のうちのリード部５ａ，６ａが通っている領域のセルギャップが、前記リード部５ａ，６ａの上のギャップ材１２で規制され、他の領域のセルギャップが、前記リード部５ａ，６ａとほぼ同じ膜厚を有するダミー膜８の上のギャップ材で規制される。

【００４１】そして、この液晶セルでは、上記ダミー膜８の膜厚を上記リード部５ａ，６ａの膜厚とほぼ同じにしているため、リード部５ａ，６ａの上のギャップ材１２で規制されるセルギャップと、ダミー膜８の上のギャップ材で規制されるセルギャップとはほぼ同じであり、したがって、セルギャップのばらつきを極く小さくすることができる。

【００４２】このため、例えば液晶の複屈折効果（または液晶および位相差板の複屈折効果）と偏光板の偏光作用とを利用し、印加電圧に対応した液晶セルのΔｎ・ｄの変化によって複数の色を表示する複屈折効果型の液晶表示装置に上記液晶セルを用いれば、液晶セルのセルギャップのばらつきによる色むらの発生がほとんど無い、高品質のカラー表示を実現することができる。

【００４３】また、上記液晶セルでは、上記ダミー膜８を、シール材１１の外周よりも内側に設けているため、シール材１１の外周部分を基板１，２面に直接密着させて高いシール性を得ることができるとともに、外部から不純物が前記ダミー膜８を伝ってセル内に侵入するのを防止することができる。

【００４４】しかも、上記実施例では、前記ダミー膜８をシール材１１の幅方向に沿う線状に形成するとともに、ダミー膜８の幅をリード部５ａ，６ａの幅よりも大きくし、各ダミー膜８，８の間隔を各リード部５ａ，５ａおよび６ａ，６ａの間隔よりも小さくすることにより、このダミー膜８の幅に対する各ダミー膜８の間隔の比を、上記リード部５ａ，６ａの幅に対する各リード部５ａ，６ａの間隔の比よりも小さくしているため、上記接合部をその全幅にわたって通っているリード部５ａ，６ａの上にある１つのリード部当たりのギャップ材１２の数と、前記接合部の幅より小さい長さのダミー膜８の上にある１つのダミー膜当たりのギャップ材１２の数とをバランスさせることができる。

【００４５】すなわち、上記実施例によれば、前記接合部をその全幅にわたって通っているリード部５ａ，６ａの上にある単位面積当たりのギャップ材１２の数よりも、前記接合部の幅より小さい長さのダミー膜８の上にある単位面積当たりのギャップ材１２の数が多くなり、セルギャップの規制に有効なリード部上およびダミー膜上のギャップ材１２の密度が、前記接合部の幅方向の長さが小さい各ダミー膜８上に比べて前記接合部の幅方向の長さが大きい各リード部５ａ，６ａ上の方が小さくなるから、これらのギャップ材１２によるセルギャップの規制効果を接合部全周にわたってほぼ等しくし、セルギャップのばらつきをより小さくすることができる。

【００４６】なお、図５では図面を簡易化するためにギャップ材１２を大きく誇張して示したが、例えば複屈折効果型液晶表示装置に用いる液晶セルでは、直径が４～

５μｍギャップ材を用いてセルギャップを４～５μｍに設定しており、これに対してシール材１１の幅は約１０００μｍであるため、実際には、リード部上およびダミー膜上にそれぞれ多数のギャップ材１２が分布している。

【００４７】上記第１の実施例は、ＴＦＴを能動素子とするアクティブマトリックス型のものに限らず、例えば、ダイオードのような特性をもったＭＩＭ構造の非線形抵抗素子を能動素子とするアクティブマトリックス型の液晶セルや、単純マトリックス型の液晶セル等にも適用することができる。

【００４８】上記非線形抵抗素子を能動素子とするアクティブマトリックス型の液晶セルは、一方の基板の内面に、マトリックス状に配列された複数の画素電極と、これらの画素電極にそれぞれ接続された複数の能動素子と、各行の能動素子にオン信号を供給するための信号供給ラインを設け、他方の基板に各画素列ごとに分割された複数本の対向電極を設けた構成であるが、前記一方の基板の内面のシール材による接合部に、前記信号供給ラインのリード部とほぼ同じ膜厚の複数のダミー膜を前記リード部が通っている領域を除くほぼ全域にわたって所定間隔で設け、他方の基板の内面の前記接合部に、前記対向電極のリード部とほぼ同じ膜厚の複数のダミー膜を前記リード部が通っている領域を除くほぼ全域にわたって所定間隔で設ければ、セルギャップを均一にすることができる。

【００４９】また、上記単純マトリックス型の液晶セルは、一方の基板の内面に、行方向に沿う複数本の走査電極を設け、他方の基板に列方向に沿う複数本の信号電極を設けた構成であるが、前記一方の基板の内面のシール材による接合部に、前記走査電極のリード部とほぼ同じ膜厚の複数のダミー膜を前記リード部が通っている領域を除くほぼ全域にわたって所定間隔で設け、他方の基板の内面の前記接合部に、前記信号電極のリード部とほぼ同じ膜厚の複数のダミー膜を前記リード部が通っている領域を除くほぼ全域にわたって所定間隔で設ければ、セルギャップを均一にすることができる。

【００５０】図６および図７はこの発明の第２の実施例を示しており、図６は対向電極を形成した基板の一部分の平面図、図７は前記液晶セルの一部分の拡大断面図であって、（ａ）は図６のＡ′－Ａ′線に沿った断面図、（ｂ）は図６のＢ′－Ｂ′線に沿った断面図である。

【００５１】この実施例は、上記第１の実施例の液晶セルをさらに改良したものであり、ＴＦＴを能動素子とするアクティブマトリックス型の液晶セルにおいて、上記表側基板２に設ける対向電極１０と遮光膜９の両方を、その外周部がシール材１１による接合部内に対応する外形に形成したものである。

【００５２】この実施例では、遮光膜９のリード部９ａを含む外形を、対向電極１０の外形（リード部１０ａを含む外形）と同じにするとともに、この対向電極１０および遮光膜９を、そのリード部１０ａ，９ａ以外の部分の外周縁がシール材１１の外周よりも内側（ここでは、外周縁がシール材１１の幅のほぼ中間）に位置する大きさに形成している。

【００５３】なお、この実施例の液晶セルは、上記対向電極１０と遮光膜９を上記のような外形に形成した点を除けば、他の構成は第１の実施例のものと同じであるから、重複する説明は、図において対応するものに同符号を付して省略する。

【００５４】この実施例の液晶セルによれば、シール材１１による接合部のうちの対向電極１０および遮光膜９から延出するリード部１０ａ，９ａが通っている領域のセルギャップが、前記リード部１０ａ，９ａの上のギャップ材１２で規制され、他の領域のセルギャップが、対向電極１０および遮光膜９の外周部の上のギャップ材１２で規制されるが、前記対向電極１０および遮光膜９の外周部と前記リード部１０ａ，９ａの膜厚は同じであるため、セルギャップのばらつきを極く小さくすることが

できる。
【００５５】すなわち、上記第１の実施例の液晶セルでは、図４に示したように、対向電極１０だけがシール材１１と重なっており、遮光膜９はシール材１１に重なっていないため、上記表側基板２の内面のシール材１１による接合部のうち、上記リード部１０ａ，９ａが通っている領域が、対向電極１０の外周部だけがラップしている領域よりも、遮光膜９の膜厚分だけ高くなっている。
【００５６】なお、対向電極１０の膜厚は０．０５μｍ程度であるのに対して、クロム膜と酸化クロム膜との積層膜からなる遮光膜９の膜厚は約０．２０μｍであり、したがって、表側基板２の上記接合部におけるリード部１０ａ，９ａが通っている領域と対向電極１０の外周部だけがラップしている領域との段差は約０．２０μｍである。
【００５７】このため、上記第１の実施例の液晶セルでは、上記接合部の対向電極１０および遮光膜９のリード部１０ａ，９ａが通っている領域において、セルギャップが遮光膜９の膜厚分だけ大きくなる。
【００５８】しかし、この第２の実施例では、対向電極１０と遮光膜９の両方を、その外周部がシール材１１による接合部内に対応する外形に形成しているため、表側基板２の上記接合部におけるリード部１０ａ，９ａが通っている領域と、対向電極１０と遮光膜９の外周部がラップしている領域との間には段差がなく、したがって、セルギャップのばらつきを極く小さくすることができる。
【００５９】しかも、この実施例では、上記第１の実施例と同様に、裏側基板１の内面のシール材１１による接合部に、ゲートライン５およびデータライン６のリード部５ａ，６ａとほぼ同じ膜厚の複数のダミー膜８を、前記リード部５ａ，６ａが通っている領域を除くほぼ全域にわたって所定間隔で設けているため、セルギャップのばらつきをほぼ完全に無くすことができる。
【００６０】このため、この実施例の液晶セルを複屈折効果型の液晶表示装置に用いれば、液晶セルのセルギャップのばらつきによる色むらの発生が無い、より高品質のカラー表示を実現することができる。
【００６１】また、この第２の実施例の液晶セルでは、表側基板２の対向電極１０と遮光膜９の外周縁がシール材１１の外周よりも内側にあり、また、裏側基板１に形成したダミー膜８もシール材１１の外周よりも内側にあるため、シール材１１の外周部分と両基板１，２面に直接密着させて高いシール性を得ることができるとともに、外部から不純物が対向電極１０および遮光膜９、あるいはダミー膜８を伝ってセル内に侵入するのを防止することができる。
【００６２】なお、この発明は、複屈折効果型液晶表示装置に用いる液晶セルに限らず、液晶セルのセルギャップの僅かなばらつきが表示特性に影響するＳＴＮ型液晶表示装置や強誘電性液晶表示装置に用いる液晶セルにも適用できるし、またＴＮ型液晶表示装置に用いる液晶セルにも適用できる。
【００６３】
【発明の効果】この発明は、セルギャップを規制するギャップ材を混入した樹脂からなる枠状のシール材を介して接合された一対の基板間に液晶が封入されるとともに、前記一対の基板の内面にそれぞれ、表示エリアに対応する電極と、前記シール材の外側に延出するリード部とが形成された液晶セルにおいて、少なくとも一方の基板の内面の前記シール材による接合部に、前記リード部とほぼ同じ膜厚の複数のダミー膜を、前記リード部が通っている領域を除くほぼ全域にわたって所定間隔で設けたことを特徴とするものであるから、セルギャップのばらつきを極く小さくすることができる。
【００６４】また、この発明は、セルギャップを規制するギャップ材を混入した樹脂からなる枠状のシール材を介して接合された一対の基板間に液晶が封入されるとともに、一方の基板の内面に、表示エリアに対応させてマ

トリックス状に配列された複数の画素電極と、これらの画素電極にそれぞれ接続された複数の薄膜トランジスタと、これらの薄膜トランジスタにゲート信号およびデータ信号を供給するゲートラインおよびデータラインと、これらのラインから前記シール材の外側に延出するリード部とが形成され、他方の基板の内面に、各画素に対応する部分が開口する遮光膜と、前記表示エリアの全域に対応する対向電極と、この対向電極および前記遮光膜から前記シール材の外側に延出するリード部とが形成されたアクティブマトリックス型の液晶セルにおいて、前記対向電極と前記遮光膜の両方を、その外周部が前記シール材による接合部内に対応する外形に形成したものであるから、セルギャップのばらつきを極く小さくすることができる。

【００６５】この発明において、前記対向電極と遮光膜の外周縁がシール材の外周よりも内側にあれば、シール材の外周部分と基板面とを直接密着させて高いシール性を得ることができるとともに、外部から不純物が対向電極および遮光膜を伝ってセル内に侵入するのを防止することができる。

【００６６】また、上記アクティブマトリックス型の液晶セルにおいて、画素電極および薄膜トランジスタとゲート，データラインを形成した上記一方の基板の内面のシール材による接合部に、前記ゲート，データラインのリード部とほぼ同じ膜厚の複数のダミー膜を、前記接合部のうちの前記リード部が通っている領域を除くほぼ全域にわたって所定間隔で設ければ、セルギャップのばらつきをほぼ完全に無くすことができる。

【００６７】この発明において、上記ダミー膜を、シール材の外周よりも内側に設ければ、シール材の外周部分を基板面に直接密着させて高いシール性を得ることができるとともに、外部から不純物が前記ダミー膜を伝ってセル内に侵入するのを防止することができる。

【００６８】また、前記ダミー膜をシール材の外周よりも内側に設ける場合、このダミー膜をシール材の幅方向に沿う線状に形成するとともに、前記ダミー膜の幅に対する各ダミー膜の間隔の比を、前記リード部の幅に対する各リード部の間隔の比よりも小さくすれば、前記接合部をその全幅にわたって通っているリード部の上にある単位面積当たりのギャップ材の数よりも、前記接合部の幅より小さい長さのダミー膜の上にある単位面積当たりのギャップ材の数が多くなり、セルギャップの規制に有効なリード部上およびダミー膜上のギャップ材の密度が、前記接合部の幅方向の長さが小さい各ダミー膜上に比べて前記接合部の幅方向の長さが大きい各リード部上の方が小さくなるから、これらのギャップ材によるセルギャップの規制効果を接合部全周にわたってほぼ等しくし、セルギャップのばらつきをより小さくすることができる。

【図面の簡単な説明】

【図１】この発明の第１の実施例を示す液晶セルの平面図。

【図２】前記液晶セルの一方の基板の平面図。

【図３】図２の一部分の拡大図。

【図４】前記液晶セルの他方の基板の一部分の拡大平面図。

【図５】前記液晶セルの一部分の拡大断面図であって、（ａ）は図３のＡ－Ａ線に沿った断面図、（ｂ）は図３のＢ－Ｂ線に沿った断面図。

【図６】この発明の第２の実施例を示す対向電極を形成した基板の一部分の平面図。

【図７】前記液晶セルの一部分の拡大断面図であって、（ａ）は図６のＡ´－Ａ´線に沿った断面図、（ｂ）は図６のＢ´－Ｂ´線に沿った断面図。

【符号の説明】

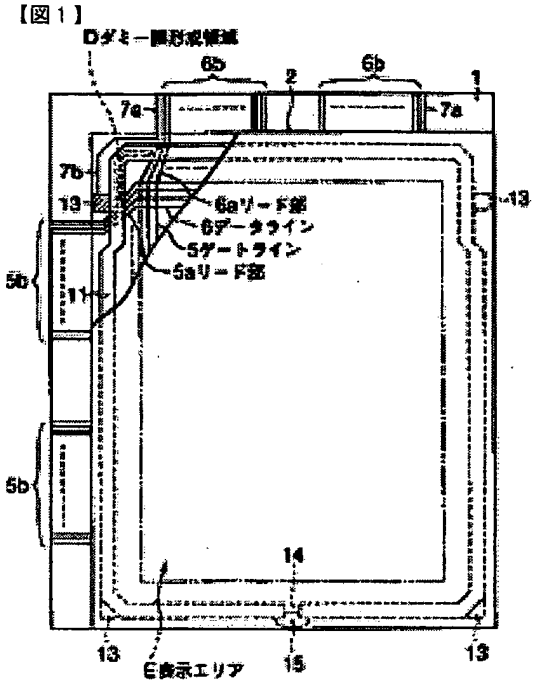
Ｅ…表示エリア

１，２…基板

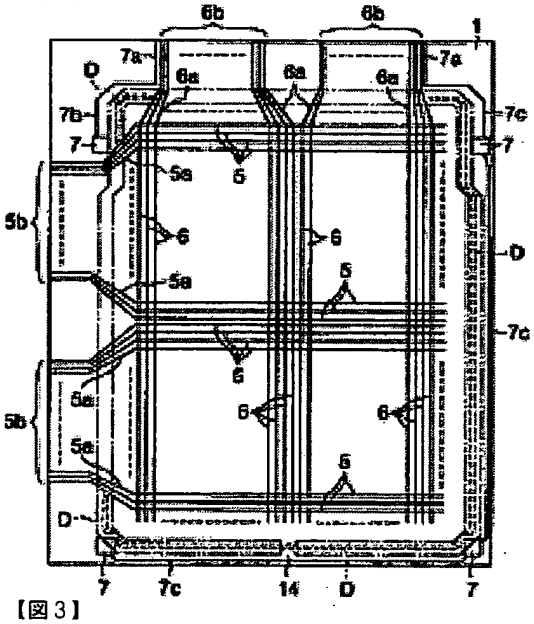
３…画素電極

4…ＴＦＴ
5…ゲートライン
6…データライン
5ａ，６ａ…リード部
7…中継電極
8…ダミー膜
9…遮光膜
１０…対向電極
9ａ，１０ａ…リード部
１１…シール材
１２…ギャップ材
１３…導通材

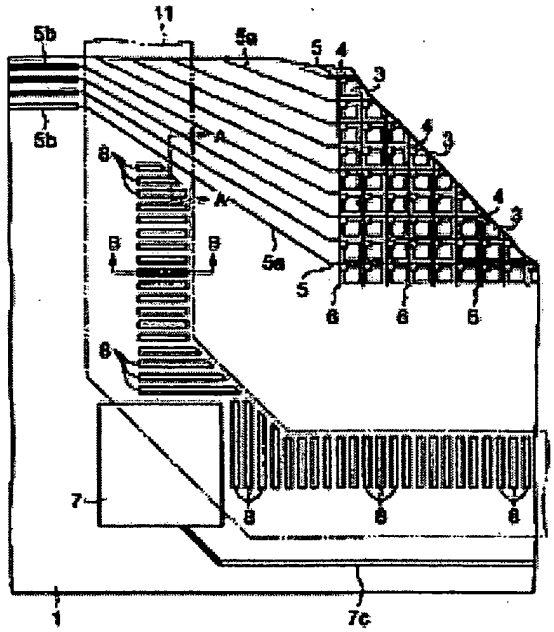
【図１】



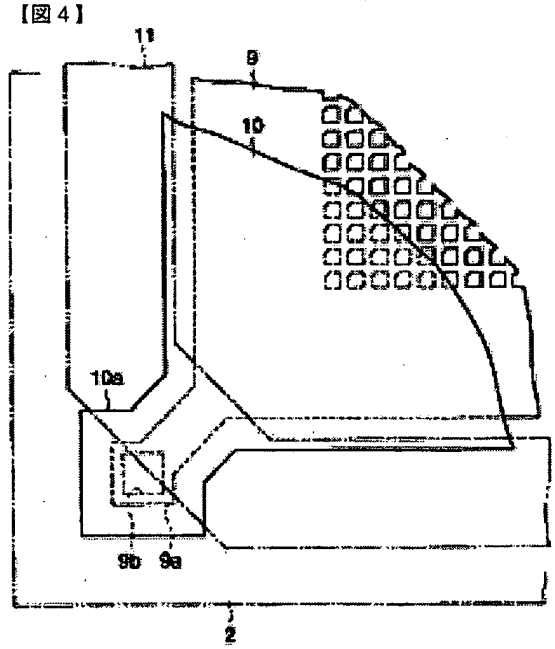
【図２】



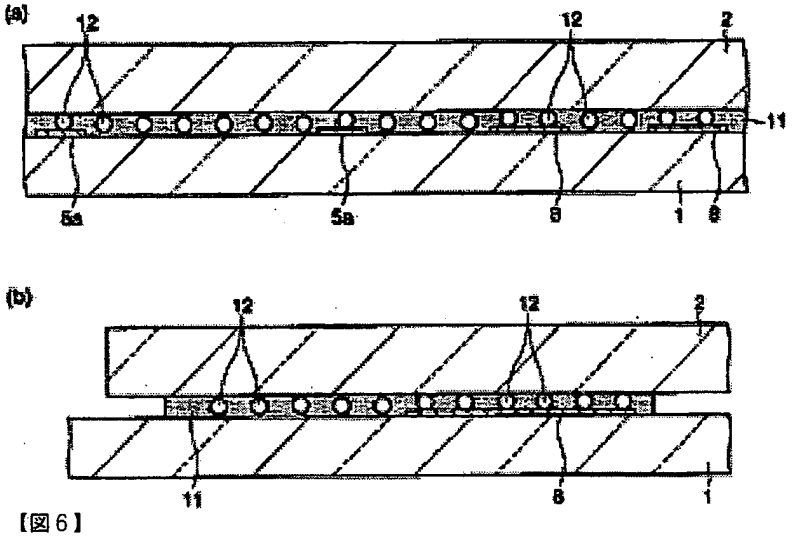
【図３】



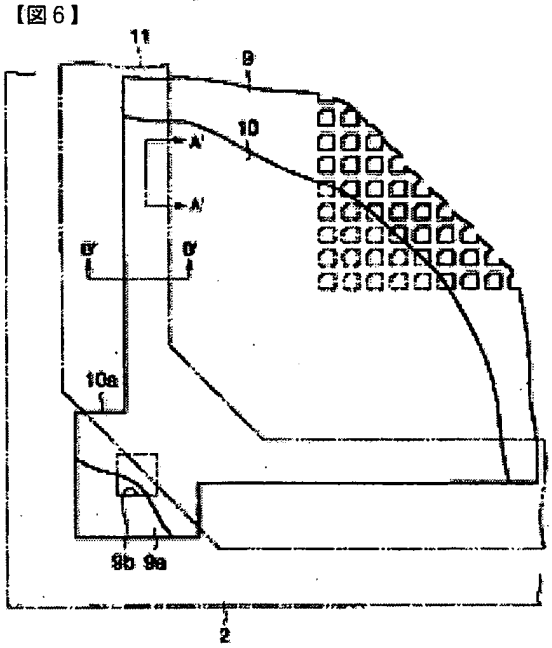
【図４】



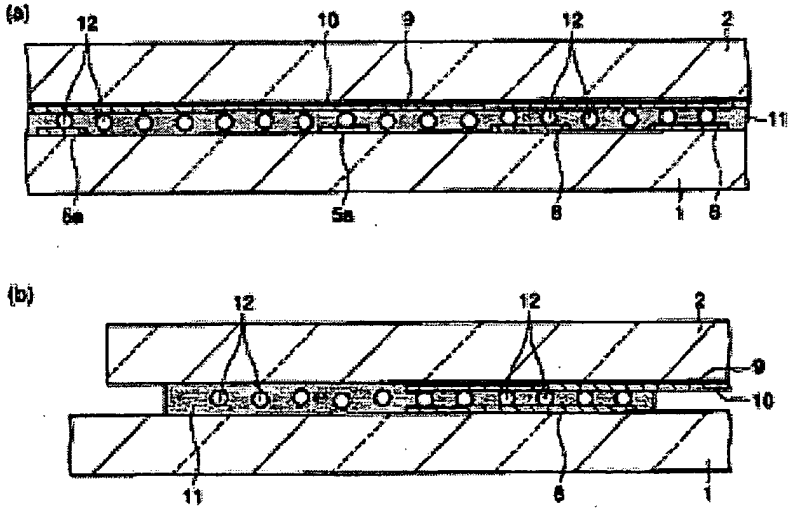
【図５】


(a)
12
12
2
11
5a
5a
6
1
8
(b)
12
12
2
11
6
1

【図６】


11
9
10
A'
A
B'
B
10a
9b
9a
2

【図７】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PATENT NUMBER and ISSUE DATE 6889629

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U.S. UTILITY Patent Application

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**APPLICANTS: Tsujimura Takatoshi; Makita Atsuya; Arai Toshiaki;

**CONTINUING DATA VERIFIED: NONE CME

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 2001-029587 02/06/2001 CME

PG-PUB DO NOT PUBLISH ☐ RESCIND ☐

Foreign priority claimed ☑ yes ☐ no
35 USC 119 conditions met ☑ yes ☐ no
Verified and Acknowledged Examiner's Initials C. Everhart

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Primary Examiner

PREPARED FOR ISSUE

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Total Claims	Print Claim for O.G.
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Sheets Drwg.	Figs. Drwg.	Print Fig.
11	12	1

Application Examiner

FILED WITH: ☐ DISK (CRF) ☐ CD-ROM
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10068500

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10/068500
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2.	Priority	2/5/02	32.		
3.	Rejection 3 months	5/29/03 CH	33.		
4.	Amend't A	8-29-03	34.		
5.	Allowance	10/01/03 mm	35.		
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SEARCH

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INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
438	25	9-24-03	cme

SEARCH NOTES

(List databases searched. Attach search strategy inside.)

	Date	Exmr.
WEST (pixel# same dummy same pad#)	5-19-03	cme
WEST ((pad#/same dummy) and (lcd or (liquid adj crystal adj display))	9-24-03	cme

ISSUE SLIP STAPLE AREA (for additional cross-references)

ISSUING CLASSIFICATION

ORIGINAL CLASS	ORIGINAL SUBCLASS	CROSS REFERENCE(S) CLASS	CROSS REFERENCE(S) SUBCLASS (ONE SUBCLASS PER BLOCK)						
438	26	438	149	73					
INTERNATIONAL CLASSIFICATION		257	72	748					
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INDEX OF CLAIMS

✓ ..... Rejected - (Through numeral) ... Canceled N ..... Non-elected A ..... Appeal
= ..... Allowed + ... Restricted I ..... Interference O ..... Objected

Claim Final	Claim Original	Date 5/19/03	Date 9/24/03
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3	4	I	
4	5	I	
5	6	I	
6	7	I	
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8	9	I	
9	10	✓	
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11	13	I	
12	14	I	
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14	16	I	
15	17	I	
16	18	✓	
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Claim Final	Claim Original	Date
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8/29/03 101

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US006689629B2

(12) **United States Patent**
Tsujimura et al.

(10) **Patent No.: US 6,689,629 B2**
(45) **Date of Patent: Feb. 10, 2004**

(54) **ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE**

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(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 54 days.

(21) Appl. No.: **10/068,500**

(22) Filed: **Feb. 5, 2002**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

Feb. 6, 2001 (JP) 2001-029587

(51) **Int. Cl.**[7] **H01L 21/00**

(52) **U.S. Cl.** **438/25**; 438/149; 438/73; 257/72; 257/748

(58) **Field of Search** 438/25, 22, 30, 438/149, 73; 257/72, 748

(56) **References Cited**

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6,163,356 A * 12/2000 Song et al. 349/152

* cited by examiner

Primary Examiner—Caridad Everhart
(74) *Attorney, Agent, or Firm*—Tiffany L. Townsend

(57) **ABSTRACT**

Disclosed is to provide an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display.

The present invention is an array substrate for display, which includes: a thin film transistor array formed on an insulating substrate 1; a plurality of wirings 23 and 24 arranged on the insulating substrate 1; connection pads 25 and 27 arranged on unilateral ends of the wirings 23 and 24 and respectively connected therewith; and pixel electrodes 22, wherein dummy conductive patterns 29 are arranged between the ends of the connection pads 25 and 27 and ends of the pixel electrodes 22.

16 Claims, 11 Drawing Sheets

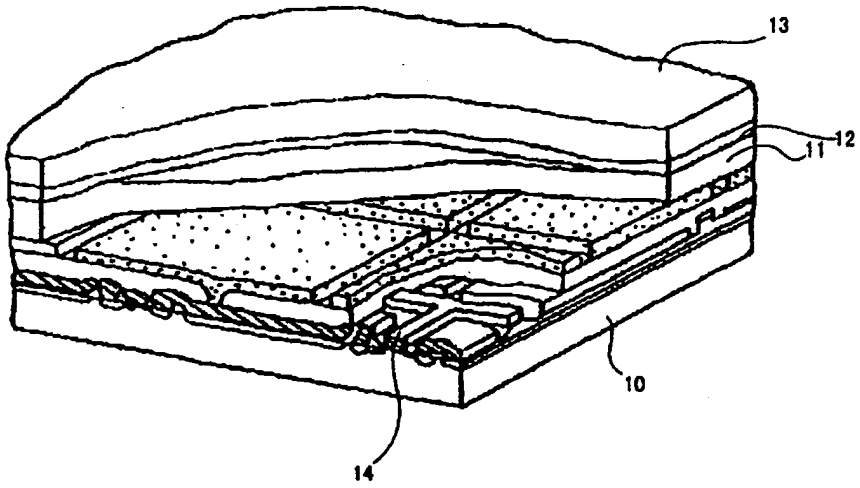


FIG. 1

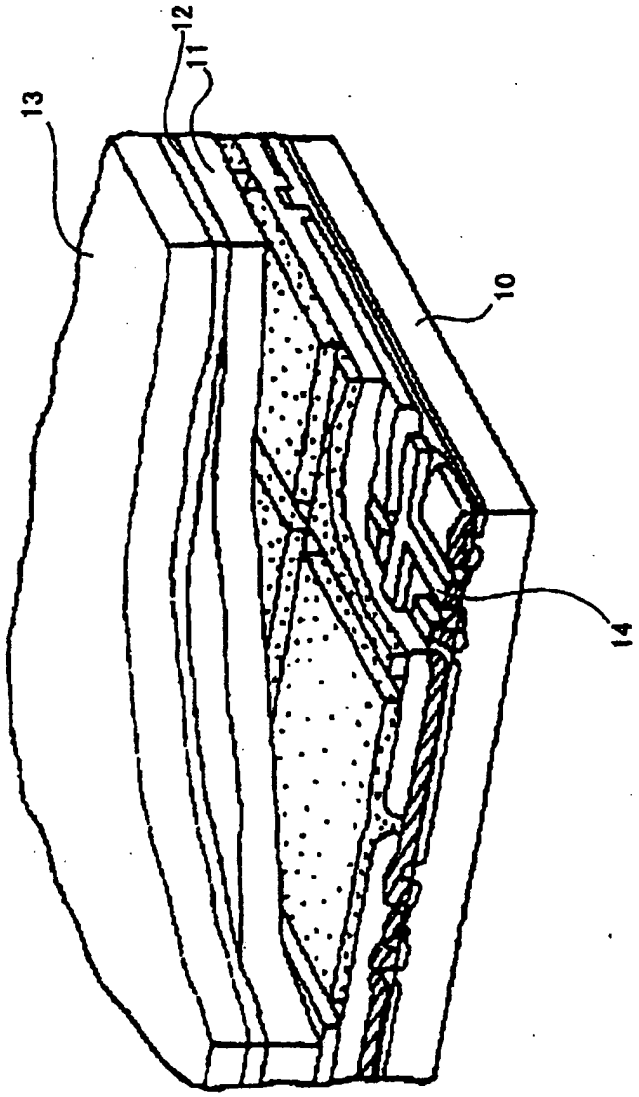


FIG. 2

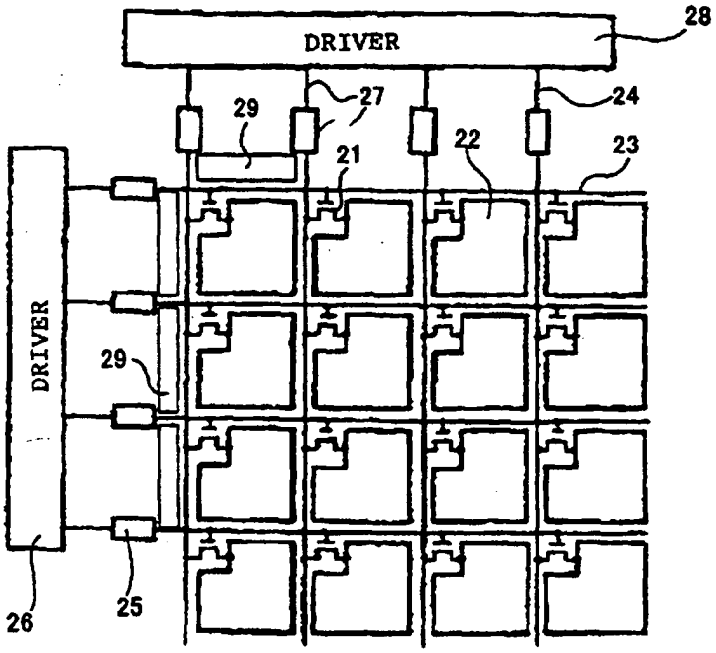


FIG. 3

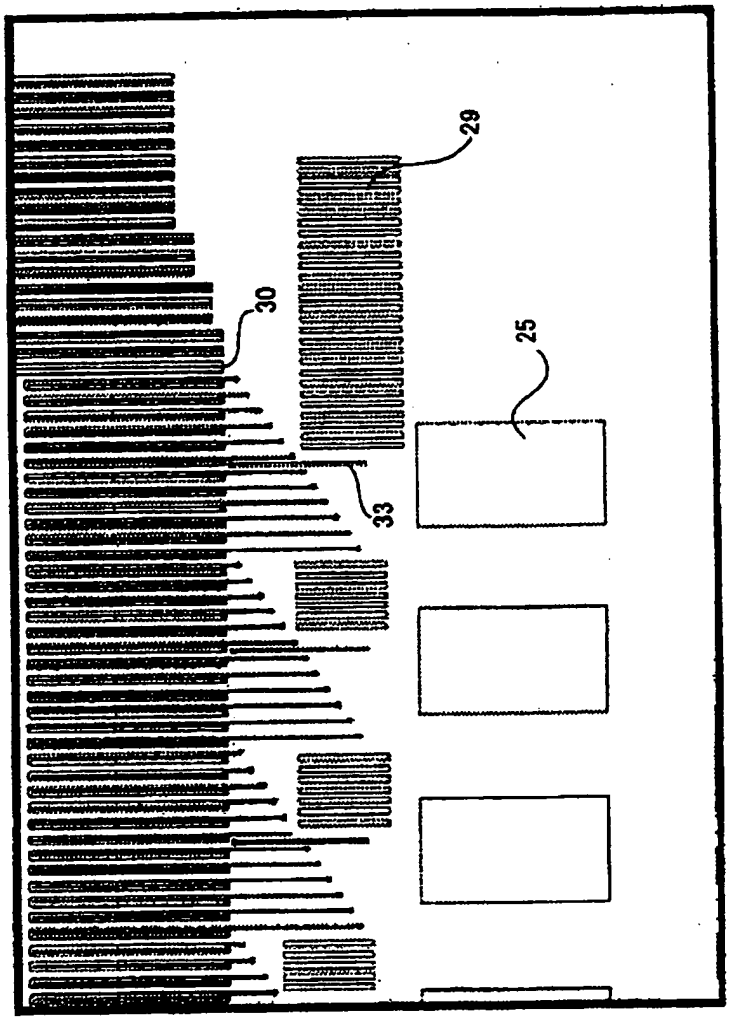


FIG. 4

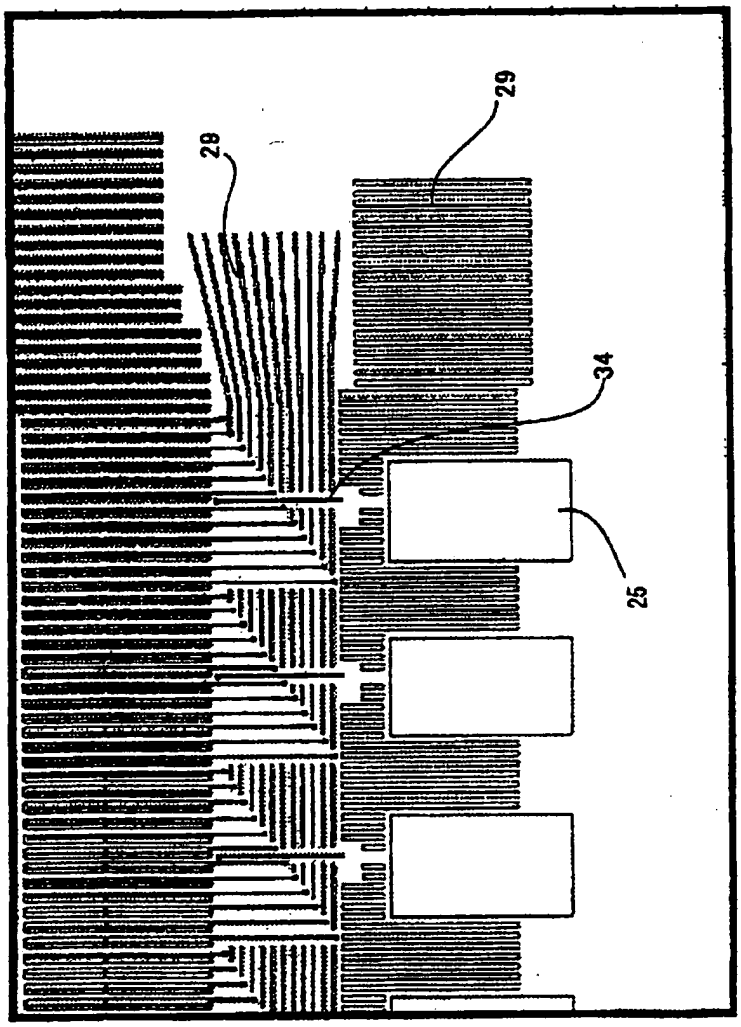


FIG. 5

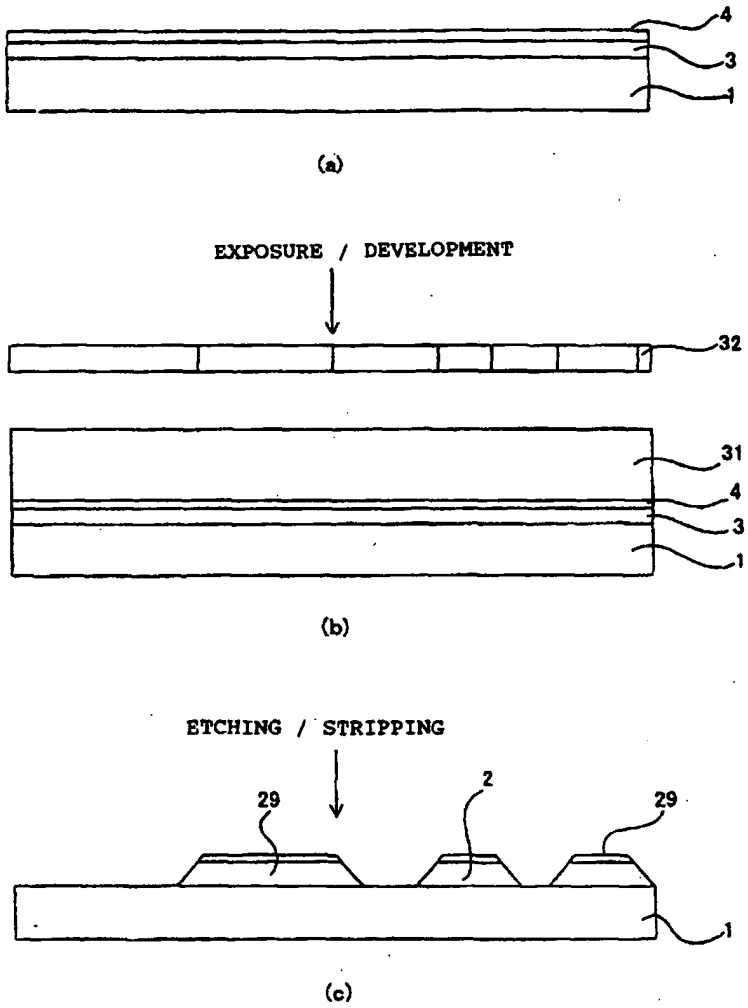

4
3
1
(a)
EXPOSURE / DEVELOPMENT
32
31
4
3
1
(b)
ETCHING / STRIPPING
29
2
29
1
(c)

FIG. 6

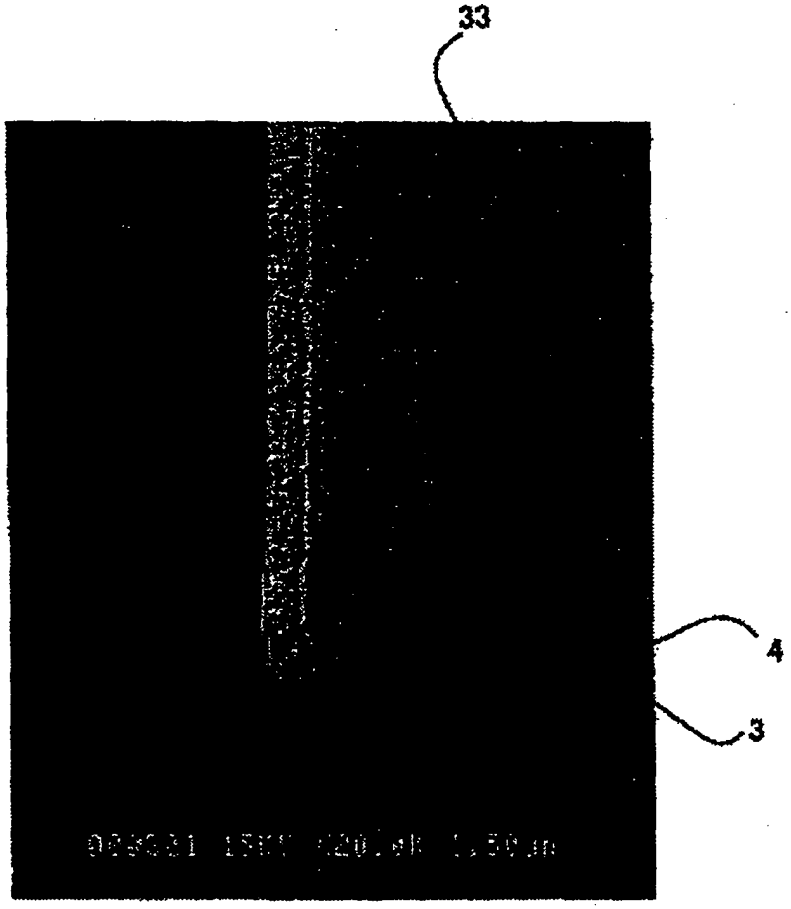


FIG. 7

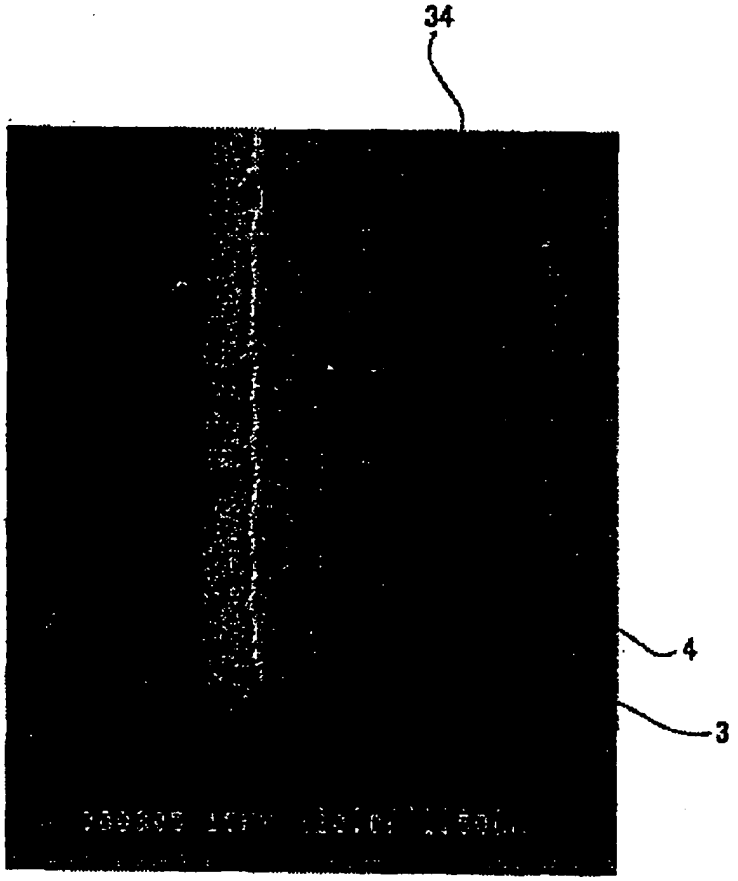


FIG. 8

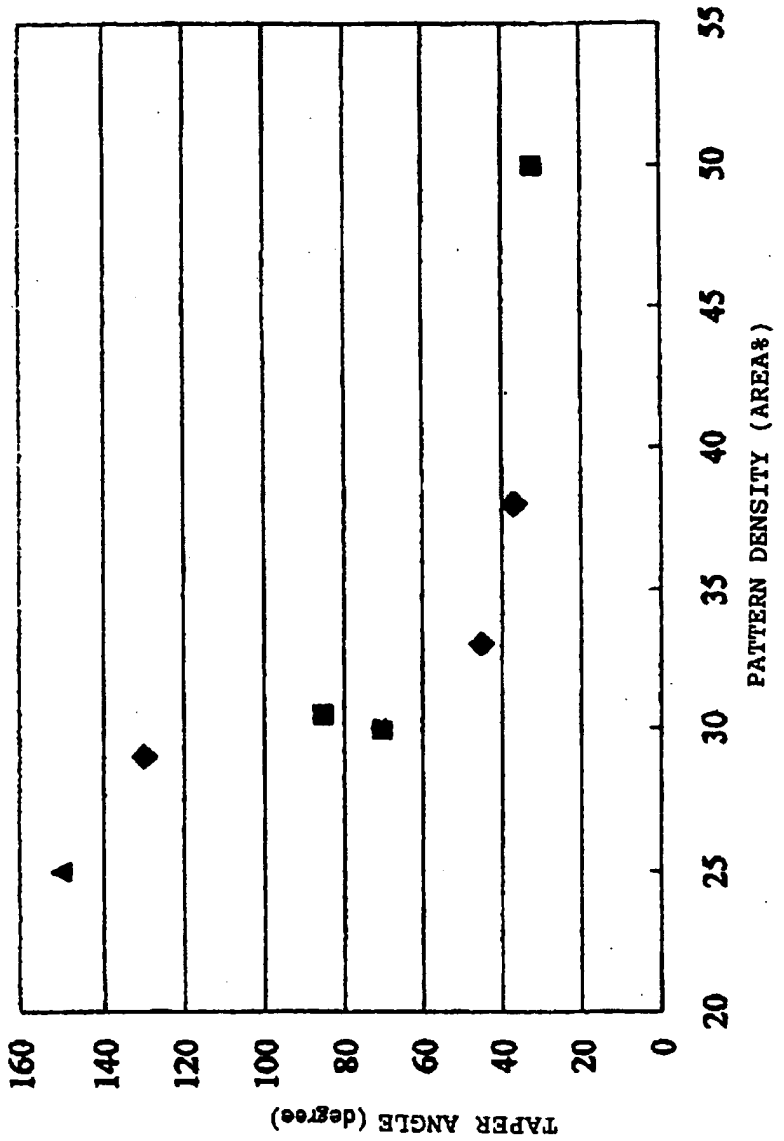

PATTERN DENSITY (AREA%)
20
25
30
35
40
45
50
55
TAPER ANGLE (degree)
160
140
120
100
80
60
40
20
0

FIG. 9

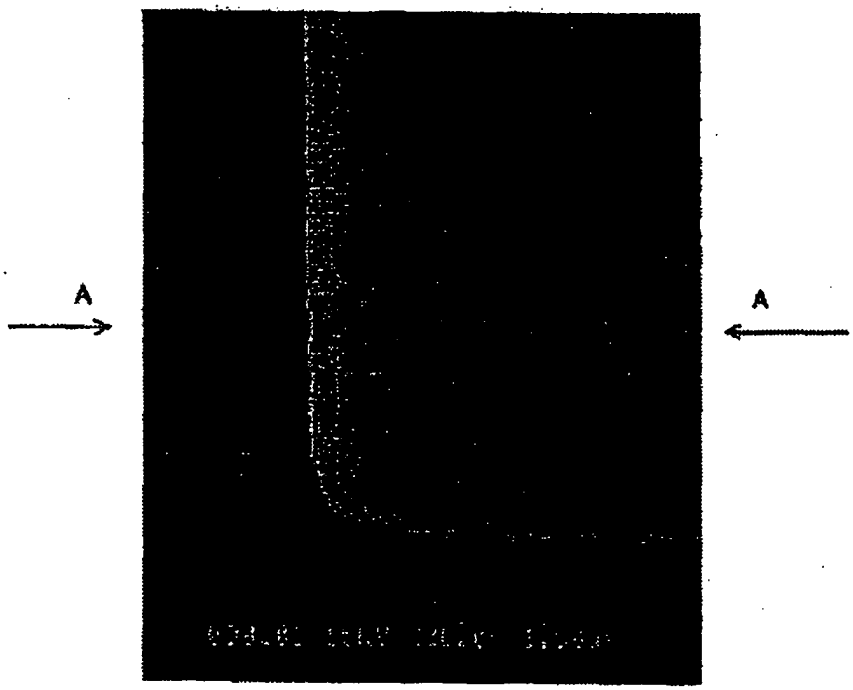


FIG. 10

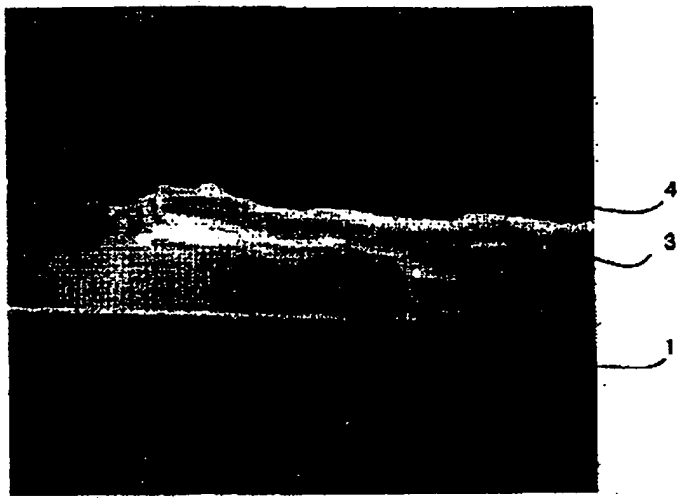


FIG. 11

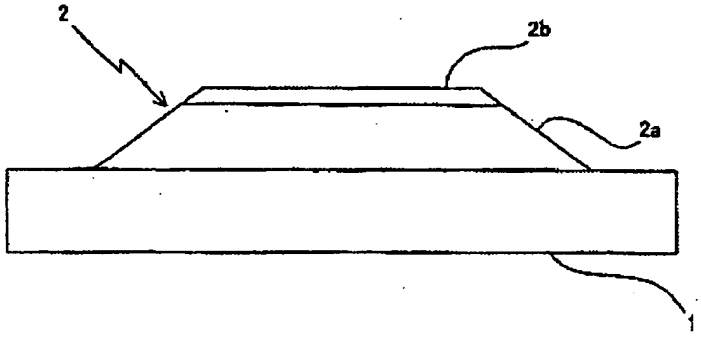
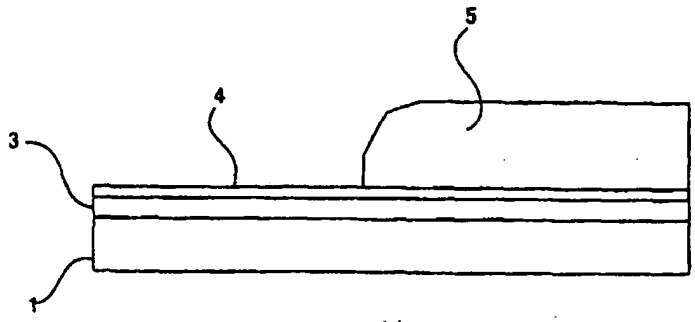
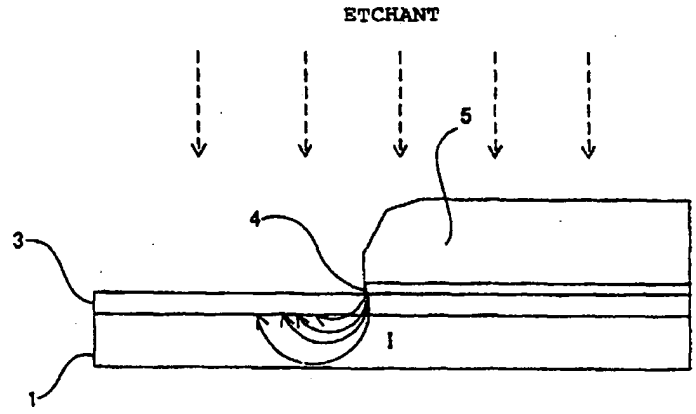


FIG. 12



(a)



(b)

ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

BACKGROUND OF THE INVENTION

The present invention relates to an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display.

A display device using a thin film transistor (TFT) array has been frequently used owing to low power consumption and capability of downsizing the display device. The thin film transistor array is manufactured by forming thin film transistors, each being composed of electrodes such as a gate electrode, a source electrode and a drain electrode, wirings such as scan lines and signal lines connected with the above-mentioned electrodes, and pixel electrodes on an insulating substrate.

In recent years, a higher operating speed, a higher resolution and a larger size have been required for the display device described above in many cases. A high speed and a high density have been required for each constituent component of the array for display, which forms a display device. Particularly, in order to operate the thin film transistor array at a high speed, it is preferable to use low-resistance aluminum (Al) for the wirings such as the scan lines and the signal lines since delay in gate pulses can be reduced and a writing speed to the thin film transistor can be increased.

Incidentally, aluminum tends to be easily oxidized in spite of its low resistance. Therefore, in many cases, wiring using aluminum is constituted as a two-layer structure, in which aluminum is used as a lower conductive material, and a material harder to be oxidized than aluminum such as chromium, tantalum, titanium or molybdenum is used as an upper conductive material. FIG. **11** is a view schematically showing a state where wiring **2** is deposited on an insulating substrate **1**. A lower conductive material film **2***a* is deposited on an insulating substrate **1** made of such as glass, and an upper conductive material film **2***b* is deposited on the lower conductive material film **2***a*. Each of these films **2***a* and **2***b* is patterned by, for example, a proper etching process so as to have tapered ends.

In order to form a tapered shape shown in FIG. **11**, an etching rate for the upper conductive material is required to be increased. In order to form the tapered shape shown in FIG. **11**, various methods have been proposed up to now. For example, in the gazette of Japanese Patent Laid-Open No. Hei 10 (1998)-90706, a method has been proposed, in which dummy connection pads are provided on sides opposite to scan line connection pads and signal line connection pads, respectively. According to this method, over etching due to an etchant that will be relatively increased by lowering wiring density at ends of the substrate is prevented. Thus, undercut of a lower conductive material **3** is prevented, and an interlayer short circuit is prevented by imparting a proper tapered shape to the wiring **2**.

However, though this method enables evenness of etching at the ends of the thin film transistor array substrate to be improved, the method cannot effectively prevent the undercut of the signal lines in a region where the wiring density is apt to be lowered from ends of the pixel electrodes to the connection pads, for example, in a portion where drawing wiring is formed.

Moreover, in the gazette of Japanese Patent Laid-Open No. Hei 10 (1998)-240150, disclosed is a method of forming a tapered shape at an angle ranging from 20 degrees to 70 degrees on wiring constituted of two layers, in which a pad formed of aluminum and metal such as molybdenum formed on the aluminum is subjected to wet etching. According to this method, a specified tapered shape can be imparted to the wiring formed of a conductive film of a two-layer structure by the wet etching. However, the method never discloses a method of evenly etching a substrate region while maintaining a selection ratio thereof even in the substrate region where the wiring density is lowered.

FIGS. **12**A and **12**B are enlarged schematic views for explaining a patterning process using a conventionally used wet process in order to impart the above-described tapered shape to the wiring. As shown in FIG. **12**A, the lower conductive material **3** and an upper conductive material **4** are deposited on the insulating substrate **1** by a method such as physical vapor deposition. FIG. **12**A shows that a photoresist film **5** is coated on a film of the upper conductive material **4** and is patterned in a desired shape. The respective films are etched by an etchant such as a solution of phosphoric acid, nitric acid, acetic acid or mixtures thereof, and desired tapered shapes are formed thereon.

FIG. **12**B is a view for explaining an electrochemical process generated as each film is being etched when the wiring constituted of the upper conductive material **4** and the lower conductive material **3** is subjected to wet etching. In FIG. **12**B, an internal layer portion of the upper conductive material **4** coated with the photoresist film **5** is not dissolved However, at the end of the photoresist film **5**, the upper conductive material **4** is dissolved by the etchant. When the wiring is formed by the wet etching, the upper conductive material **4** protected by the photoresist film **5** is further dissolved in a lateral direction from the end of the photoresist film **5** to turn into positive ions, and electrons emitted as a result are supplied to the lower conductive material **3**. Thus, the upper conductive material **4** serves as an anode. In this connection, the lower conductive material **3** comes to serve as a cathode. Accordingly, an electrochemical cell is formed. Here, when the etching rate for the upper conductive material **4** is increased to form a required tapered shape, the density of the electrons generated by dissolving the upper conductive material **4** and flowing to the lower conductive material **3** is increased accompanied with an increase of a dissolution rate of the upper conductive material **4**. FIG. **12**B schematically shows currents I flowing from the upper conductive material **4** to the lower conductive material **3**.

As the etching rate is increased, the density of the current flowing to an area of the upper conductive material **4**, which is exposed to the etchant, exceeds a current density causing passivity of the upper conductive material **4**. In such a case, the upper conductive material **4** is passivated not to be dissolved by the etchant, and only the lower conductive material **3** is dissolved accompanied with the progress of the etching, resulting in the occurrence of the undercut. When such undercut occurs, the wiring, for example, the gate wiring cannot be sufficiently coated with an insulating film in some cases, thus causing inconvenience such as an interlayer short circuit, resulting in lowering a yield of the display device.

SUMMARY OF THE INVENTION

The present invention was made with the foregoing problems in mind. An object of the present invention is to

provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of being etched at a sufficiently high etching rate and a sufficient selection ratio, eliminating undercut, and providing a large-sized and high-resolution display device.

The foregoing object of the present invention is achieved by providing the array substrate for display, the method of manufacturing an array substrate for display and the display device using the array substrate for display of the present invention.

Specifically, according to the present invention, provided is an array substrate for display, comprising: a thin film transistor array formed on an insulating substrate; a plurality of wirings arranged on the insulating substrate; connection pads arranged on unilateral ends of the wirings and respectively connected with the wirings; pixel electrodes, and dummy conductive patterns arranged between the ends of the connection pads and ends of the pixel electrodes. The dummy conductive patterns can occupy 30 area % or more. In the present invention, the dummy conductive patterns can be formed as any of land patterns and line-and-space patterns. In the present invention, the wirings are constituted of a lower conductive material and an upper conductive material, and the lower conductive material can be any one of aluminum and an aluminum alloy. In the present invention, the upper conductive material has a passivating potential. The upper conductive material can be any one of molybdenum and a molybdenum alloy.

According to the present invention, provided is a method of manufacturing an array substrate for display, the method comprising the steps of: forming a thin film transistor array including: a plurality of wirings arranged on an insulating substrate; and connection pads arranged on unilateral ends of the wirings and respectively connected with the wirings; forming pixel electrodes; and forming dummy conductive patterns between ends of the connection pads and ends of the pixel electrodes. In the present invention, it is preferable that the dummy conductive patterns be formed so as to occupy 30 area % or more. In the present invention, the dummy conductive patterns can be formed as any of land patterns and line-and-space patterns. In the present invention, the wirings are constituted of a lower conductive material and an upper conductive material, the lower conductive material can be any one of aluminum and an aluminum alloy, and the upper conductive material can be any one of molybdenum and a molybdenum alloy. In the present invention, the wirings are formed by wet etching.

Moreover, in the present invention, provided is a display device, comprising the array substrate for display mentioned above.

In the present invention, the display device used as a liquid crystal display device or an electroluminescence display device can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings.

FIG. **1** is a view showing an embodiment of a liquid crystal display device using an array substrate for display of the present invention.

FIG. **2** is a top plan view of the array substrate for display of the present invention.

FIG. **3** is an enlarged view showing a dummy conductive pattern in the present invention.

FIG. **4** is an enlarged view showing another dummy conductive pattern in the present invention.

FIGS. **5**A to **5**C are views illustrating a method of manufacturing the array substrate for display of the present invention.

FIG. **6** is an electron microscope photograph showing a pattern shape of wiring in the case of using the dummy conductive pattern shown in FIG. **3**.

FIG. **7** is an electron microscope photograph showing a pattern shape of wiring in the case of using the dummy conductive pattern shown in FIG. **4**.

FIG. **8** is a graph showing a relation between a taper angle of the wiring and a pattern density of the wiring.

FIG. **9** is an electron microscope photograph showing a wiring shape in the case of performing etching without using the dummy conductive pattern.

FIG. **10** is an electron microscope photograph showing a sectional shape of the wiring shape shown in FIG. **9**.

FIG. **11** is a schematic view showing a tapered shape of the wiring.

FIGS. **12**A and **12**B are views showing currents formed by a cell formed during an etching process.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinbelow, description will be made in detail for the present invention with reference to embodiments shown in the accompanying drawings. However, the present invention is not limited to the embodiments shown in the drawings.

FIG. **1** is a partially cutaway perspective view showing an embodiment of a display device using an array substrate for display of the present invention. As shown in FIG. **1**, the display device of the present invention is constituted by sequentially laminating a liquid crystal layer **11**, a transparent electrode **12** and a glass substrate **13** on an array substrate **10** for display, which is formed on an insulating substrate. Wiring **14** formed on the insulating substrate **10** is extended to an end (not shown) of the array substrate for display, and is connected with a driving system (not shown) through a connection pad (not shown).

FIG. **2** is a top plan view of the display device using the array substrate **10** for display of the present invention, which is shown in FIG. **1**. In the array substrate **10** for display of the present invention, a plurality of thin film transistors **21** constitute an array. A pixel electrode **22** is connected with each thin film transistor **21** that controls a potential of the pixel electrode. In the array substrate **10** for display shown in FIG. **2**, what is further shown is that a scan line **23** and a signal line **24** are connected with each thin film transistor **21**.

The respective scan lines **23** are connected with a driver **26** through scan line connection pads **25**, and the respective signal lines **24** are connected with a driver **28** through signal line connection pads **27**. These scan lines **23** and the signal lines **24** are formed so as to have the same constitution. As shown in FIG. **11**, each of these lines is constituted of the lower conductive material **3** and the upper conductive material **4**.

In the present invention, aluminum can be used for the lower conductive material **3** usable as wiring from a viewpoint of lowering resistance thereof. Moreover, it is preferable to use molybdenum (Mo) for the upper conductive material **4** usable in the present invention from a viewpoint of protecting the aluminum. However in the present invention, besides the aluminum, an aluminum alloy can be used for the lower conductive material **3**. Moreover, for the

upper conductive material 4, alloys of chromium, tantalum, titanium and molybdenum can be used. Film thickness of the lower conductive material 3 is not particularly limited, but film thickness of the upper conductive material 4 is preferably thick since a current tends to be concentrated thereto as the film thickness becomes thinner. However, a problem regarding stress occurs as the thickness becomes thicker. Therefore, in the present invention, it is preferable to set the film thickness of the upper conductive material 4 in a range of 30 to 100 nm.

The present invention makes it possible to prevent undercut of the lower conductive material 3, which occurs due to passivity of the upper conductive material 4. In the present invention, the term "passivity" is referred to as a phenomenon that metal such as molybdenum or a metal alloy such as a molybdenum alloy becomes insoluble in an acid or alkaline etchant. For example, the term "passivity" is referred to as a phenomenon that metal serving as an anode becomes insoluble in such etchant. In the present invention, specifically as for such passivated metal or a metal alloy, metal or a metal alloy with a passivating potential, that is, a Flade potential can be mentioned. Note that, in the present invention, the Flade potential is referred to as a potential which causes a current density for passivating metal, which is described in the Encyclopedia Chimica (miniature edition 32nd printing, issued by Kyoritsu Shuppan Co., Ltd., edited by editorial committee of the Encyclopedia Chimica), vol. 7, p. 911.

Furthermore, in the embodiment shown in FIG. 2, dummy conductive patterns 29 are disposed between the pixel electrodes 22 and each scan line connection pad 25 and between the pixel electrodes 22 and each signal line connection pad 27. Thus, the wiring density is increased. Therefore, it is made possible to form good wiring over the entire surface of the array substrate for display without causing defects such as undercut and a mouse hole of the lower conductive material 3 during etching for the scan lines 23 and the signal lines 24. Each of these dummy conductive patterns 29 can be formed as a two-layers structure with the same materials as those of the scan lines 23 and the signal lines 24 at the same time when the patterning is performed therefor.

FIG. 3 is an enlarged view showing a portion where the dummy conductive pattern 29 is formed in the embodiment of the array substrate 10 for display of the present invention shown in FIG. 2. FIG. 3 shows the dummy conductive pattern 29 formed as a line-and-space pattern between the connection pad 25 and an end 30 of the pixel electrode. In the present invention, the dummy conductive pattern 29 can be formed as the line-and-space pattern shown in FIG. 3. Alternatively, the dummy conductive pattern 29 can be formed as a land pattern completely coating a region where the dummy conductive pattern 29 is formed.

In any case of the patterns, in the present invention, it is preferable that the wiring density of the dummy conductive patterns 29 themselves be 30% or more on an area of a specified surface from a viewpoint of forming a properly tapered shape on the lower conductive material 3 without forming the undercut thereto while dissolving the upper conductive material 4 at a required rate.

Moreover, when the dummy conductive patterns 29 are arranged in the present invention, it is more preferable that the dummy conductive patterns 29 be formed between the end 30 of the pixel electrode 22 and each connection pads 25 and 27 so that the wiring density including the dummy conductive patterns 29 can be 30% or more on the area of a specified surface. In the present invention, the term "wiring density" refers to an area ratio of an area of portions where the signal lines, the scan lines, the drawing lines, and the dummy conductive patterns are formed on an area of a specified region where the dummy conductive patterns are formed.

FIG. 4 is a view showing another embodiment of the dummy conductive pattern 29 of the present invention. In the embodiment shown in FIG. 4, the dummy conductive pattern 29 is disposed so that the wiring density thereof, which is specified at 30% or more, is further increased, thus reducing concentration of electric current to exposed portions of the upper conductive material to the etchant during the etching. As shown in FIG. 4, the dummy conductive pattern 29 may have any shapes and any patterns. Moreover, any combination of a plural type of the dummy conductive patterns 29 can be used.

FIGS. 5A, 5B and 5C are views showing an embodiment of a method of manufacturing the array substrate 10 for display of the present invention. With reference to FIG. 5, description will be made for the method of manufacturing the array substrate 10 for display of the present invention, exemplifying a case where the thin film transistor 21 of a reverse stagger type is formed. First, as shown in FIG. 5A, the lower conductive material 3 using aluminum and the upper conductive material 4 using molybdenum are deposited on the transparent or untransparent insulating substrate 1, thus forming a film.

Next, as shown in FIG. 5B, photoresist 31 is coated on the film. The photoresist is exposed and developed by use of a photo mask 32 provided with patterns for forming the dummy conductive patterns 29 in portions where the wiring density is lowered between the pixel electrodes and the connection pads, which are not particularly shown.

Subsequently, etching is performed by use of an etchant such as a solution of phosphoric acid, nitric acid, acetic acid and mixtures thereof, thus forming the wiring 2 and the dummy conductive patterns 29. The dummy conductive patterns 29 are arranged in the portions where the wiring density is low. Thus, it is made possible to form wirings having good tapered shape as shown in FIG. 5C even in regions where the conductive material such as molybdenum tends to be passivated. A taper angle can be set in a range of 20 degrees to 70 degrees by adjusting a composition of the etchant and etching conditions. It is more preferable to set the taper angle in a range of about 20 degrees to about 60 degrees.

Thereafter, in the present invention, gate insulating films, the gate electrodes, the source electrodes, the drain electrodes, the pixel electrodes and the like are formed, thus the array substrate 10 for display of the present invention is manufactured. In the present invention, the dummy conductive patterns 29 may be removed if necessary. Alternatively, the dummy conductive patterns 29 may be left as they are without being eliminated.

FIG. 6 is an electron microscope photograph showing a shape of the wiring 33 shown in FIG. 3, which was obtained when the dummy conductive pattern 29 shown in FIG. 3 was provided and the etching was performed. In this case, molybdenum was used for the upper conductive material 4, and aluminum was used for the lower conductive material 3. The film thickness of molybdenum is about 50 nm, and wet etching is performed by use of an etchant of a mixed solution of phosphoric acid, nitric acid and acetic acid. As shown in FIG. 6, a good tapered shape is formed even in a wiring portion where the undercut is formerly apt to occur by forming the dummy conductive pattern 29.

FIG. 7 is a photograph showing a shape of the wiring 34 shown in FIG. 4, which was obtained when the dummy conductive pattern 29 shown in FIG. 4 was formed and the etching was performed under the same conditions as those in FIG. 6. As shown in FIG. 7, even when the density of the dummy conductive pattern 29 is increased, a good tapered shape is obtained.

FIG. 8 is a graph plotting values of the taper angle of the formed wiring relative to values of the pattern density (area %) of the wiring including the portions of the dummy conductive patterns 29 on the substrate when the dummy conductive patterns 29 are arranged. As shown in FIG. 8, the taper angle of the wiring obtained by the etching is reduced as the pattern density of the wiring is increased, and a more gentle taper is formed. Therefore, it is understood that the upper conductive material 4 can impart a sufficient selective ratio to the etching of the lower conductive material 3 by arranging the dummy conductive patterns 29.

FIG. 9 is an electron microscope photograph showing, for comparison, a shape of wiring obtained when etching is performed by use of the array substrate 10 for display, which has the same pattern as those shown in FIGS. 3 and 4, but without forming the dummy conductive patterns 29 at all. As shown in FIG. 9, large undercut occurs in the wiring since the molybdenum used for the upper conductive material 4 is passivated, and only the etching for the aluminum as the lower conductive material 3 progresses.

FIG. 10 is an electron microscope photograph showing a cross section taken along a cutting plane line A—A of the wiring shown in FIG. 9. As shown in FIG. 10, the etching for the aluminum used for the lower conductive material 3 progresses more than that for the molybdenum used for the upper conductive material 4, resulting in the occurrence of the great undercut.

The present invention can be applied not only to the thin film transistor of a reverse stagger type as described above but also to a thin film transistor of a top gate type including wiring formed of aluminum and any metal other than the aluminum, of which passivating current density is known.

Moreover, although the array device for display of the present invention can be applied to a liquid crystal display device using a transparent insulating substrate made of such as glass, the array device for display of the present invention can be also used as an organic or inorganic electroluminescence device, wherein an untransparent insulating substrate is used and an array for display is formed on the insulating substrate.

As described above, according to the present invention, it is made possible to provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of being etched at a sufficiently high etching rate and a sufficient selection ratio, and eliminating the under cut and the lowering of a yield in manufacturing due to the inconvenience such as an interlayer short circuit. Moreover, according to the present invention, it is made possible to provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of providing a large-sized and high-resolution display device.

Although the preferred embodiments of the present invention have been described in detail, it should be understood that various changes, substitutions and alternations can be made therein without departing from spirit and scope of the inventions as defined by the appended claims.

What is claimed is:

1. An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wiring arranged on the insulating substrate. each wiring having a first end, the wiring in communication with at least one of the transistors in the thir film array;

connections pads, each connection pad contacting the firs: end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring

2. The array substrate for display according to claim 1 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

3. The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.

4. The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

5. The array substrate for display according to claim 3 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

6. The array substrate for display according to claim 5 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

7. The array substrate for display according to claim 4 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

8. The array substrate for display according to claim 5 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

9. A meted for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array formed on the insulating substrate, each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

10. The method for forming an array substrate for display according to claim 9 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials

11. The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring materials is selected from the group consisting of aluminum and aluminum alloys.

12. The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

13. The method for forming an array substrate for display according to claim 11 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and allays thereof.

14. The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

15. The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

16. The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

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TITLE

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APPLICANT: Takatoshi Tsujimura, et al.

FOR: ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

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ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

Abstract of the disclosure

Disclosed is to provide an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display.

The present invention is an array substrate for display, which includes: a thin film transistor array formed on an insulating substrate 1; a plurality of wirings 23 and 24 arranged on the insulating substrate 1; connection pads 25 and 27 arranged on unilateral ends of the wirings 23 and 24 and respectively connected therewith; and pixel electrodes 22, wherein dummy conductive patterns 29 are arranged between the ends of the connection pads 25 and 27 and ends of the pixel electrodes 22.

ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

Background of the Invention

The present invention relates to an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display.

A display device using a thin film transistor (TFT) array has been frequently used owing to low power consumption and capability of downsizing the display device. The thin film transistor array is manufactured by forming thin film transistors, each being composed of electrodes such as a gate electrode, a source electrode and a drain electrode, wirings such as scan lines and signal lines connected with the above-mentioned electrodes, and pixel electrodes on an insulating substrate.

In recent years, a higher operating speed, a higher resolution and a larger size have been required for the display device described above in many cases. A high speed and a high density have been required for each constituent component of the array for display, which forms a display device. Particularly, in order to operate the thin film transistor array at a high speed, it is preferable to use low-resistance aluminum (Al) for the wirings such as the scan lines and the signal lines since delay in gate pulses can be reduced and a writing speed to the thin film transistor can be increased.

Incidentally, aluminum tends to be easily oxidized in spite of its low resistance. Therefore, in many cases, wiring using aluminum is constituted as a two-layer structure, in which aluminum is used as a lower conductive material, and a material harder to be oxidized than aluminum such as chromium, tantalum, titanium or molybdenum is used as an upper conductive material. Fig. 11 is a view schematically showing a state where wiring 2 is deposited on an insulating substrate 1. A lower conductive material film 2a is deposited on an insulating substrate 1 made of such as glass, and an upper conductive material film 2b is

deposited on the lower conductive material film 2a. Each of these films 2a and 2b is patterned by, for example, a proper etching process so as to have tapered ends.

In order to form a tapered shape shown in Fig. 11, an etching rate for the upper conductive material is required to be increased. In order to form the tapered shape shown in Fig. 11, various methods have been proposed up to now. For example, in the gazette of Japanese Patent Laid-Open No. Hei 10 (1998)-90706, a method has been proposed, in which dummy connection pads are provided on sides opposite to scan line connection pads and signal line connection pads, respectively. According to this method, over etching due to an etchant that will be relatively increased by lowering wiring density at ends of the substrate is prevented. Thus, undercut of a lower conductive material 3 is prevented, and an interlayer short circuit is prevented by imparting a proper tapered shape to the wiring 2.

However, though this method enables evenness of etching at the ends of the thin film transistor array substrate to be improved, the method cannot effectively prevent the undercut of the signal lines in a region where the wiring density is apt to be lowered from ends of the pixel electrodes to the connection pads, for example, in a portion where drawing wiring is formed.

Moreover, in the gazette of Japanese Patent Laid-Open No. Hei 10 (1998)-240150, disclosed is a method of forming a tapered shape at an angle ranging from 20 degrees to 70 degrees on wiring constituted of two layers, in which a pad formed of aluminum and metal such as molybdenum formed on the aluminum is subjected to wet etching. According to this method, a specified tapered shape can be imparted to the wiring formed of a conductive film of a two-layer structure by the wet etching. However, the method never discloses a method of evenly etching a substrate region while maintaining a selection ratio thereof even in the substrate region where the wiring density is lowered.

Figs. 12A and 12B are enlarged schematic views for explaining a patterning process using a conventionally used wet process in order to impart the above-described tapered shape to the wiring. As shown in Fig. 12A, the lower conductive material 3 and an upper conductive material 4 are deposited on the insulating substrate 1 by a method such as physical vapor deposition. Fig. 12A shows that a photoresist film 5 is coated on a film of the

upper conductive material 4 and is patterned in a desired shape. The respective films are etched by an etchant such as a solution of phosphoric acid, nitric acid, acetic acid or mixtures thereof, and desired tapered shapes are formed thereon.

Fig. 12B is a view for explaining an electrochemical process generated as each film is being etched when the wiring constituted of the upper conductive material 4 and the lower conductive material 3 is subjected to wet etching. In Fig. 12B, an internal layer portion of the upper conductive material 4 coated with the photoresist film 5 is not dissolved. However, at the end of the photoresist film 5, the upper conductive material 4 is dissolved by the etchant. When the wiring is formed by the wet etching, the upper conductive material 4 protected by the photoresist film 5 is further dissolved in a lateral direction from the end of the photoresist film 5 to turn into positive ions, and electrons emitted as a result are supplied to the lower conductive material 3. Thus, the upper conductive material 4 serves as an anode. In this connection, the lower conductive material 3 comes to serve as a cathode. Accordingly, an electrochemical cell is formed. Here, when the etching rate for the upper conductive material 4 is increased to form a required tapered shape, the density of the electrons generated by dissolving the upper conductive material 4 and flowing to the lower conductive material 3 is increased accompanied with an increase of a dissolution rate of the upper conductive material 4. Fig. 12B schematically shows currents I flowing from the upper conductive material 4 to the lower conductive material 3.

As the etching rate is increased, the density of the current flowing to an area of the upper conductive material 4, which is exposed to the etchant, exceeds a current density causing passivity of the upper conductive material 4. In such a case, the upper conductive material 4 is passivated not to be dissolved by the etchant, and only the lower conductive material 3 is dissolved accompanied with the progress of the etching, resulting in the occurrence of the undercut. When such undercut occurs, the wiring, for example, the gate wiring cannot be sufficiently coated with an insulating film in some cases, thus causing inconvenience such as an interlayer short circuit, resulting in lowering a yield of the display device.

Summary of the Invention

The present invention was made with the foregoing problems in mind. An object of the present invention is to provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of being etched at a sufficiently high etching rate and a sufficient selection ratio, eliminating undercut, and providing a large-sized and high-resolution display device.

The foregoing object of the present invention is achieved by providing the array substrate for display, the method of manufacturing an array substrate for display and the display device using the array substrate for display of the present invention.

Specifically, according to the present invention, provided is an array substrate for display, comprising: a thin film transistor array formed on an insulating substrate; a plurality of wirings arranged on the insulating substrate; connection pads arranged on unilateral ends of the wirings and respectively connected with the wirings; pixel electrodes, and dummy conductive patterns arranged between the ends of the connection pads and ends of the pixel electrodes. The dummy conductive patterns can occupy 30 area% or more. In the present invention, the dummy conductive patterns can be formed as any of land patterns and line-and-space patterns. In the present invention, the wirings are constituted of a lower conductive material and an upper conductive material, and the lower conductive material can be any one of aluminum and an aluminum alloy. In the present invention, the upper conductive material has a passivating potential. The upper conductive material can be any one of molybdenum and a molybdenum alloy.

According to the present invention, provided is a method of manufacturing an array substrate for display, the method comprising the steps of: forming a thin film transistor array including: a plurality of wirings arranged on an insulating substrate; and connection pads arranged on unilateral ends of the wirings and respectively connected with the wirings; forming pixel electrodes; and forming dummy conductive patterns between ends of the connection pads and ends of the pixel electrodes. In the present invention, it is preferable that the dummy conductive patterns be formed so as to occupy 30 area% or more. In the present invention, the dummy conductive patterns can be formed as any of land patterns and

line-and-space patterns. In the present invention, the wirings are constituted of a lower conductive material and an upper conductive material, the lower conductive material can be any one of aluminum and an aluminum alloy, and the upper conductive material can be any one of molybdenum and a molybdenum alloy. In the present invention, the wirings are formed by wet etching.

Moreover, in the present invention, provided is a display device, comprising the array substrate for display mentioned above.

In the present invention, the display device used as a liquid crystal display device or an electroluminescence display device can be provided.

Brief Description of the Drawings

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings.

[Figure 1]

Fig. 1 is a view showing an embodiment of a liquid crystal display device using an array substrate for display of the present invention.

[Figure 2]

Fig. 2 is a top plan view of the array substrate for display of the present invention.

[Figure 3]

Fig. 3 is an enlarged view showing a dummy conductive pattern in the present invention.

[Figure 4]

Fig. 4 is an enlarged view showing another dummy conductive pattern in the present invention.

[Figure 5]

Figs. 5A to 5C are views illustrating a method of manufacturing the array substrate for display of the present invention.

[Figure 6]

Fig. 6 is an electron microscope photograph showing a pattern shape of wiring in the case of using the dummy conductive pattern shown in Fig. 3.

[Figure 7]

Fig. 7 is an electron microscope photograph showing a pattern shape of wiring in the case of using the dummy conductive pattern shown in Fig. 4.

[Figure 8]

Fig. 8 is a graph showing a relation between a taper angle of the wiring and a pattern density of the wiring.

[Figure 9]

Fig. 9 is an electron microscope photograph showing a wiring shape in the case of performing etching without using the dummy conductive pattern.

[Figure 10]

Fig. 10 is an electron microscope photograph showing a sectional shape of the wiring shape shown in Fig. 9.

[Figure 11]

Fig. 11 is a schematic view showing a tapered shape of the wiring.

[Figure 12]

Figs. 12A and 12B are views showing currents formed by a cell formed during an etching process.

Detailed Description of the Preferred Embodiments

Hereinbelow, description will be made in detail for the present invention with reference to embodiments shown in the accompanying drawings. However, the present invention is not limited to the embodiments shown in the drawings.

Fig. 1 is a partially cutaway perspective view showing an embodiment of a display device using an array substrate for display of the present invention. As shown in Fig. 1, the display device of the present invention is constituted by sequentially laminating a liquid crystal layer 11, a transparent electrode 12 and a glass substrate 13 on an array substrate 10

for display, which is formed on an insulating substrate. Wiring 14 formed on the insulating substrate 10 is extended to an end (not shown) of the array substrate for display, and is connected with a driving system (not shown) through a connection pad (not shown).

Fig. 2 is a top plan view of the display device using the array substrate 10 for display of the present invention, which is shown in Fig. 1. In the array substrate 10 for display of the present invention, a plurality of thin film transistors 21 constitute an array. A pixel electrode 22 is connected with each thin film transistor 21 that controls a potential of the pixel electrode. In the array substrate 10 for display shown in Fig. 2, what is further shown is that a scan line 23 and a signal line 24 are connected with each thin film transistor 21.

The respective scan lines 23 are connected with a driver 26 through scan line connection pads 25, and the respective signal lines 24 are connected with a driver 28 through signal line connection pads 27. These scan lines 23 and the signal lines 24 are formed so as to have the same constitution. As shown in Fig. 11, each of these lines is constituted of the lower conductive material 3 and the upper conductive material 4.

In the present invention, aluminum can be used for the lower conductive material 3 usable as wiring from a viewpoint of lowering resistance thereof. Moreover, it is preferable to use molybdenum (Mo) for the upper conductive material 4 usable in the present invention from a viewpoint of protecting the aluminum. However in the present invention, besides the aluminum, an aluminum alloy can be used for the lower conductive material 3. Moreover, for the upper conductive material 4, alloys of chromium, tantalum, titanium and molybdenum can be used. Film thickness of the lower conductive material 3 is not particularly limited, but film thickness of the upper conductive material 4 is preferably thick since a current tends to be concentrated thereto as the film thickness becomes thinner. However, a problem regarding stress occurs as the thickness becomes thicker. Therefore, in the present invention, it is preferable to set the film thickness of the upper conductive material 4 in a range of 30 to 100 nm.

The present invention makes it possible to prevent undercut of the lower conductive material 3, which occurs due to passivity of the upper conductive material 4. In the present invention, the term "passivity" is referred to as a phenomenon that metal such as

molybdenum or a metal alloy such as a molybdenum alloy becomes insoluble in an acid or alkaline etchant. For example, the term "passivity" is referred to as a phenomenon that metal serving as an anode becomes insoluble in such etchant. In the present invention, specifically as for such passivated metal or a metal alloy, metal or a metal alloy with a passivating potential, that is, a Flade potential can be mentioned. Note that, in the present invention, the Flade potential is referred to as a potential which causes a current density for passivating metal, which is described in the Encyclopedia Chimica (miniature edition 32nd printing, issued by Kyoritsu Shuppan Co., Ltd., edited by editorial committee of the Encyclopedia Chimica), vol. 7, p. 911.

Furthermore, in the embodiment shown in Fig. 2, dummy conductive patterns 29 are disposed between the pixel electrodes 22 and each scan line connection pad 25 and between the pixel electrodes 22 and each signal line connection pad 27. Thus, the wiring density is increased. Therefore, it is made possible to form good wiring over the entire surface of the array substrate for display without causing defects such as undercut and a mouse hole of the lower conductive material 3 during etching for the scan lines 23 and the signal lines 24. Each of these dummy conductive patterns 29 can be formed as a two-layers structure with the same materials as those of the scan lines 23 and the signal lines 24 at the same time when the patterning is performed therefor.

Fig. 3 is an enlarged view showing a portion where the dummy conductive pattern 29 is formed in the embodiment of the array substrate 10 for display of the present invention shown in Fig. 2. Fig. 3 shows the dummy conductive pattern 29 formed as a line-and-space pattern between the connection pad 25 and an end 30 of the pixel electrode. In the present invention, the dummy conductive pattern 29 can be formed as the line-and-space pattern shown in Fig. 3. Alternatively, the dummy conductive pattern 29 can be formed as a land pattern completely coating a region where the dummy conductive pattern 29 is formed.

In any case of the patterns, in the present invention, it is preferable that the wiring density of the dummy conductive patterns 29 themselves be 30% or more on an area of a specified surface from a viewpoint of forming a properly tapered shape on the lower conductive material 3 without forming the undercut thereto while dissolving the upper

conductive material 4 at a required rate.

Moreover, when the dummy conductive patterns 29 are arranged in the present invention, it is more preferable that the dummy conductive patterns 29 be formed between the end 30 of the pixel electrode 22 and each connection pads 25 and 27 so that the wiring density including the dummy conductive patterns 29 can be 30% or more on the area of a specified surface. In the present invention, the term "wiring density" refers to an area ratio of an area of portions where the signal lines, the scan lines, the drawing lines, and the dummy conductive patterns are formed on an area of a specified region where the dummy conductive patterns are formed.

Fig. 4 is a view showing another embodiment of the dummy conductive pattern 29 of the present invention. In the embodiment shown in Fig. 4, the dummy conductive pattern 29 is disposed so that the wiring density thereof, which is specified at 30% or more, is further increased, thus reducing concentration of electric current to exposed portions of the upper conductive material to the etchant during the etching. As shown in Fig. 4, the dummy conductive pattern 29 may have any shapes and any patterns. Moreover, any combination of a plural type of the dummy conductive patterns 29 can be used.

Figs. 5A, 5B and 5C are views showing an embodiment of a method of manufacturing the array substrate 10 for display of the present invention. With reference to Fig. 5, description will be made for the method of manufacturing the array substrate 10 for display of the present invention, exemplifying a case where the thin film transistor 21 of a reverse stagger type is formed. First, as shown in Fig. 5A, the lower conductive material 3 using aluminum and the upper conductive material 4 using molybdenum are deposited on the transparent or untransparent insulating substrate 1, thus forming a film.

Next, as shown in Fig. 5B, photoresist 31 is coated on the film. The photoresist is exposed and developed by use of a photo mask 32 provided with patterns for forming the dummy conductive patterns 29 in portions where the wiring density is lowered between the pixel electrodes and the connection pads, which are not particularly shown.

Subsequently, etching is performed by use of an etchant such as a solution of phosphoric acid, nitric acid, acetic acid and mixtures thereof, thus forming the wiring 2 and

the dummy conductive patterns 29. The dummy conductive patterns 29 are arranged in the portions where the wiring density is low. Thus, it is made possible to form wirings having good tapered shape as shown in Fig. 5C even in regions where the conductive material such as molybdenum tends to be passivated. A taper angle can be set in a range of 20 degrees to 70 degrees by adjusting a composition of the etchant and etching conditions. It is more preferable to set the taper angle in a range of about 20 degrees to about 60 degrees.

Thereafter, in the present invention, gate insulating films, the gate electrodes, the source electrodes, the drain electrodes, the pixel electrodes and the like are formed, thus the array substrate 10 for display of the present invention is manufactured. In the present invention, the dummy conductive patterns 29 may be removed if necessary. Alternatively, the dummy conductive patterns 29 may be left as they are without being eliminated.

Fig. 6 is an electron microscope photograph showing a shape of the wiring 33 shown in Fig. 3, which was obtained when the dummy conductive pattern 29 shown in Fig. 3 was provided and the etching was performed. In this case, molybdenum was used for the upper conductive material 4, and aluminum was used for the lower conductive material 3. The film thickness of molybdenum is about 50 nm, and wet etching is performed by use of an etchant of a mixed solution of phosphoric acid, nitric acid and acetic acid. As shown in Fig. 6, a good tapered shape is formed even in a wiring portion where the undercut is formerly apt to occur by forming the dummy conductive pattern 29.

Fig. 7 is a photograph showing a shape of the wiring 34 shown in Fig. 4, which was obtained when the dummy conductive pattern 29 shown in Fig. 4 was formed and the etching was performed under the same conditions as those in Fig. 6. As shown in Fig. 7, even when the density of the dummy conductive pattern 29 is increased, a good tapered shape is obtained.

Fig. 8 is a graph plotting values of the taper angle of the formed wiring relative to values of the pattern density (area%) of the wiring including the portions of the dummy conductive patterns 29 on the substrate when the dummy conductive patterns 29 are arranged. As shown in Fig. 8, the taper angle of the wiring obtained by the etching is reduced as the pattern density of the wiring is increased, and a more gentle taper is formed.

Therefore, it is understood that the upper conductive material 4 can impart a sufficient selective ratio to the etching of the lower conductive material 3 by arranging the dummy conductive patterns 29.

Fig. 9 is an electron microscope photograph showing, for comparison, a shape of wiring obtained when etching is performed by use of the array substrate 10 for display. which has the same pattern as those shown in Figs. 3 and 4, but without forming the dummy conductive patterns 29 at all. As shown in Fig. 9, large undercut occurs in the wiring since the molybdenum used for the upper conductive material 4 is passivated, and only the etching for the aluminum as the lower conductive material 3 progresses.

Fig. 10 is an electron microscope photograph showing a cross section taken along a cutting plane line A-A of the wiring shown in Fig. 9. As shown in Fig. 10, the etching for the aluminum used for the lower conductive material 3 progresses more than that for the molybdenum used for the upper conductive material 4, resulting in the occurrence of the great undercut.

The present invention can be applied not only to the thin film transistor of a reverse stagger type as described above but also to a thin film transistor of a top gate type including wiring formed of aluminum and any metal other than the aluminum, of which passivating current density is known.

Moreover, although the array device for display of the present invention can be applied to a liquid crystal display device using a transparent insulating substrate made of such as glass, the array device for display of the present invention can be also used as an organic or inorganic electroluminescence device, wherein an untransparent insulating substrate is used and an array for display is formed on the insulating substrate.

As described above, according to the present invention, it is made possible to provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of being etched at a sufficiently high etching rate and a sufficient selection ratio, and eliminating the under cut and the lowering of a yield in manufacturing due to the inconvenience such as an interlayer short circuit. Moreover, according to the present invention, it is made possible to provide

an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of providing a large-sized and high-resolution display device.

Although the preferred embodiments of the present invention have been described in detail, it should be understood that various changes, substitutions and alternations can be made therein without departing from spirit and scope of the inventions as defined by the appended claims.

What Is Claimed Is:

1. An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

2. The array substrate for display according to claim 1 wherein the dummy conductive patterns comprise at least about 30% of the area of the insulating substrate.

3. The array substrate for display according to claim 1 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

4. The array substrate for display according to claim 3 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.

5. The array substrate for display according to claim 3 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

6. The array substrate for display according to claim 4 wherein the upper layer wiring

material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

7. The array substrate for display according to claim 6 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

8. The array substrate for display according to claim 5 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

9. The array substrate for display according to claim 6 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

10. A method for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array formed on the insulating substrate;

forming a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

11. The method for forming an array substrate for display according to claim 10 wherein the dummy conductive patterns comprise at least about 30% of the area of the insulating

substrate.

12. The method for forming an array substrate for display according to claim 10 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

13. The method for forming an array substrate for display according to claim 12 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.

14. The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

15. The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

16. The method for forming an array substrate for display according to claim 15 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

17. The method for forming an array substrate for display according to claim 14 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

18. The method for forming an array substrate for display according to claim 15 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

Docket No.
JP920000310US1

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
2001-029587	Japan	06/02/2001	☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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Jay H. Anderson, Registration No. 38,371;
Ira D. Blecker, Registration No. 29,894;
Steven Capella, Registration No. 33,086;
Harold Huberfeld, Registration No. 26,665;
Todd M. C. Li, Registration No. 45,554;
Susan M. Murray, Registration No. 38,252;
Daryl K. Neff, Registration No. 38,253;
Margaret A. Pepper, Registration No. 45,008;
H. Daniel Schnurmann, Registration No. 35,791;
Eugene I. Shkurko, Registration No. 36,678;
William P. Skladony, Registration No. 33,787;
Steven J. Soucar, Registration No. 32,440;
Tiffany L. Townsend, Registration No. 43,199;
all of INTERNATIONAL BUSINESS MACHINES CORPORATION; John E. Hoel, Registration No, 26,279;
Christopher A. Hughes, Registration No. 26,914;
Edward A. Pennington, Registration No. 32,588;
Joseph C. Redmond, Jr., Registration No. 18,753; all of MORGAN & FINNEGAN, L.L.P.

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Bldg. 300-482 2070 Route 52
Hopewell Junction, New York 12533-6531

Direct Telephone Calls to: *(name and telephone number)*
Tiffany L. Townsend (845) 894-3668

Full name of sole or first inventor
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Sole or first inventor's signature — Date

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Citizenship
JAPAN

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Atsuya Makita

Second inventor's signature — Date

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Citizenship
JAPAN

Post Office Address
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Third inventor's signature Date
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Citizenship **JAPAN**
Post Office Address **1-55-19 Sakuragaoka, Hodogaya-ku, Yokohama-shi, Kanagawa-ken, Japan**

Full name of fourth inventor, if any
Fourth inventor's signature Date
Residence
Citizenship
Post Office Address

Full name of fifth inventor, if any
Fifth inventor's signature Date
Residence
Citizenship
Post Office Address

Full name of sixth inventor, if any
Sixth inventor's signature Date
Residence
Citizenship
Post Office Address

AUTHORIZATION TO FILE U.S. PATENT APPLICATION IBM DOCKET NO.

JP9-2000-0310

As a below named inventor, of an invention initially entitled

ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

identified by the above IBM Docket Number, pursuant to 37 CFR 1.41(C), I hereby authorize the attorney or agent designated by IBM Corporation to file on my behalf in the United States Patent and Trademark office, an application for patent on the above identifies the invention.

Whereas the title used on the subsequently prepared patent application may vary from the above initial title, the unique docket number identifies the invention.

Takatoshi Tsujimura — Takatoshi Tsujimura 8/28/2000

FULL NAME OF SOLE OR FIRST INVENTOR INVENTOR'S SIGNATURE DATE

Atsuya Makita — Atsuya Makita 8/28/2000

FULL NAME OF SECOND JOINT INVENTOR INVENTOR'S SIGNATURE DATE

Toshiaki Arai — Toshiaki Arai 8/28/2000

FULL NAME OF THIRD JOINT INVENTOR INVENTOR'S SIGNATURE DATE

FULL NAME OF FORTH JOINT INVENTOR INVENTOR'S SIGNATURE DATE

FULL NAME OF FIFTH JOINT INVENTOR INVENTOR'S SIGNATURE DATE

FIG. 1

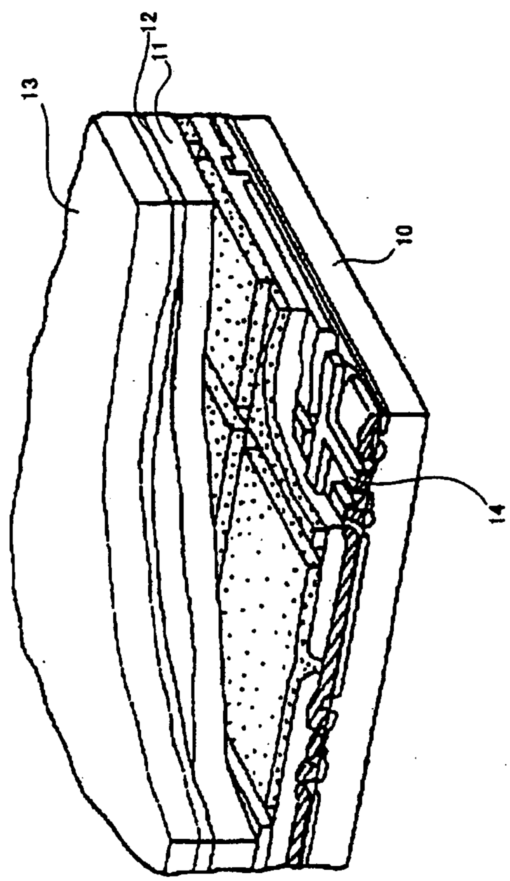


FIG. 2

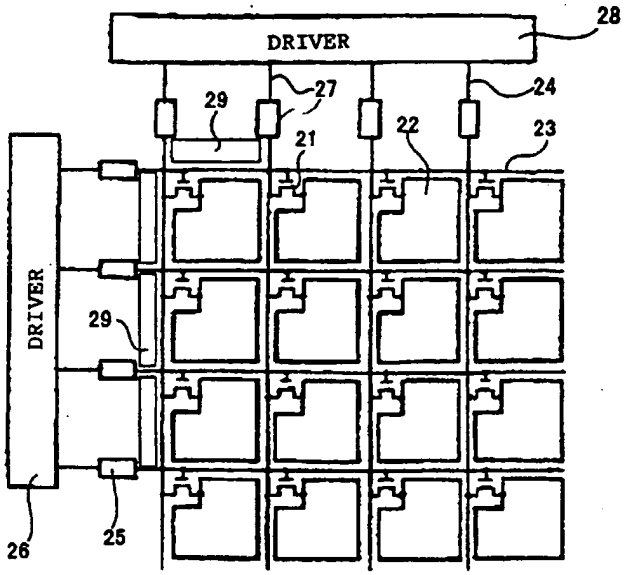
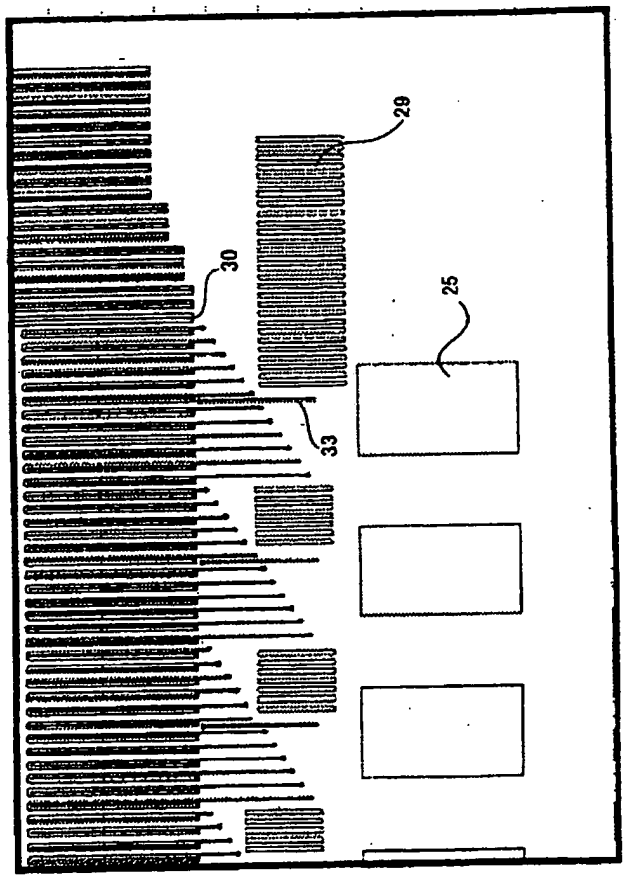


FIG. 3



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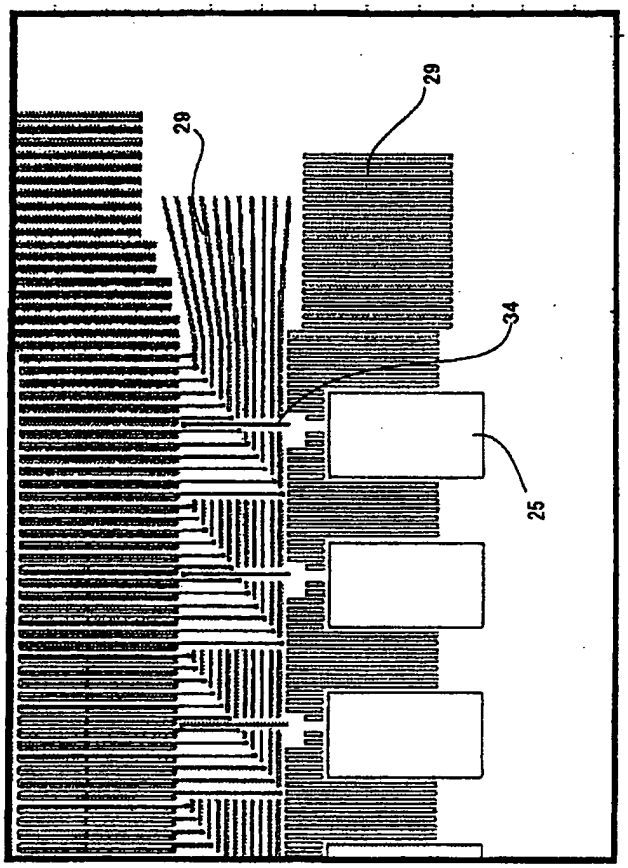


FIG. 5

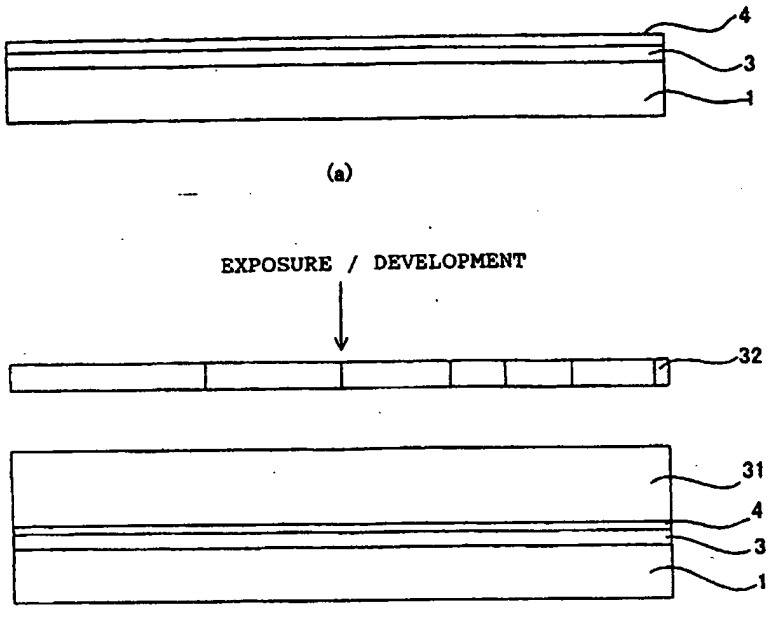
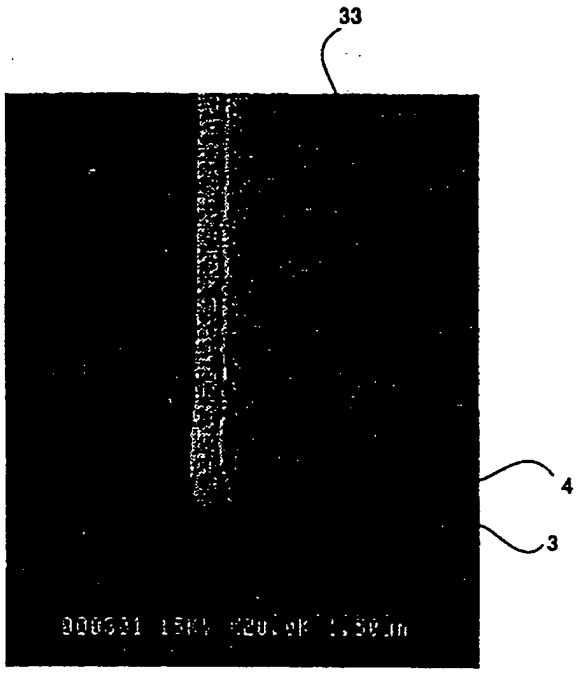


FIG. 6



PRINT OF DRAWINGS
AS ORIGINALLY FIL

FIG. 7

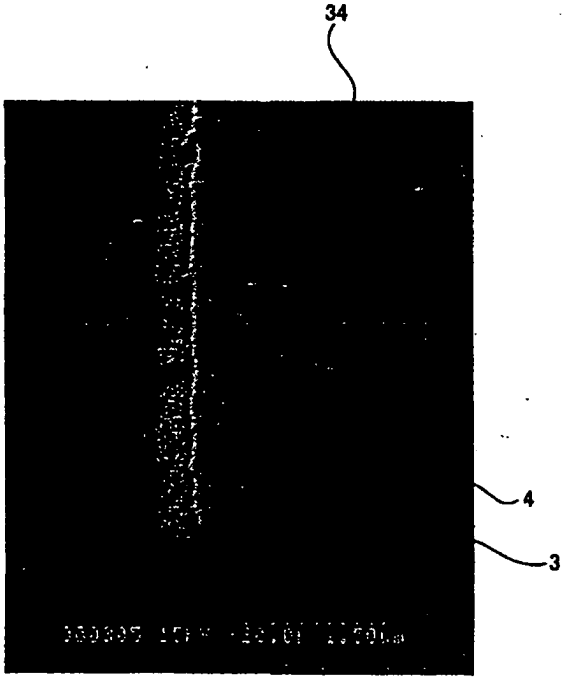


FIG. 8

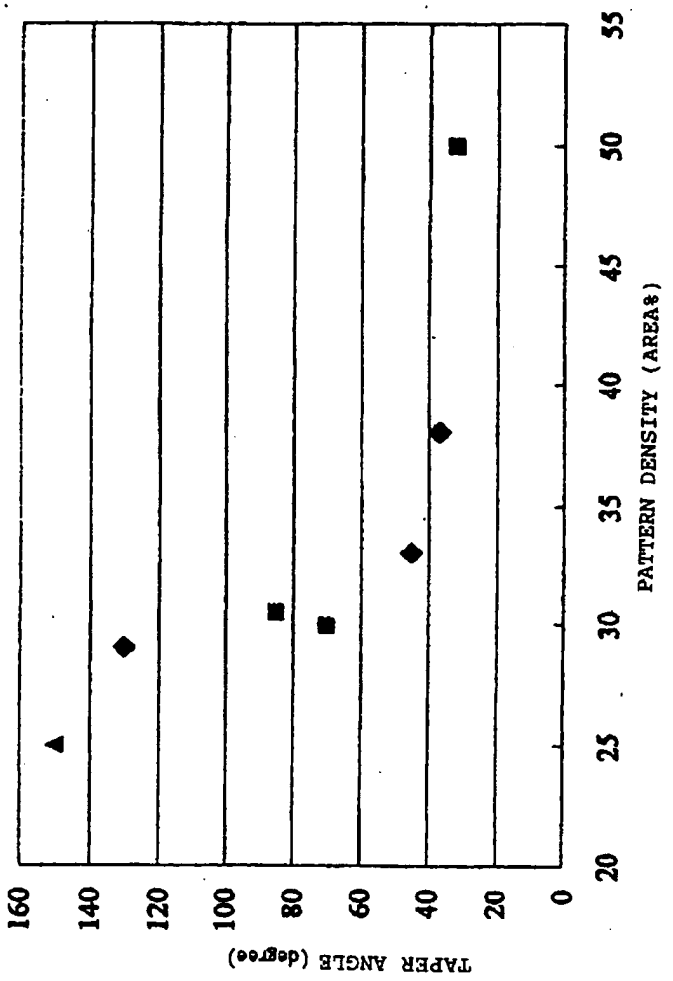


FIG. 9

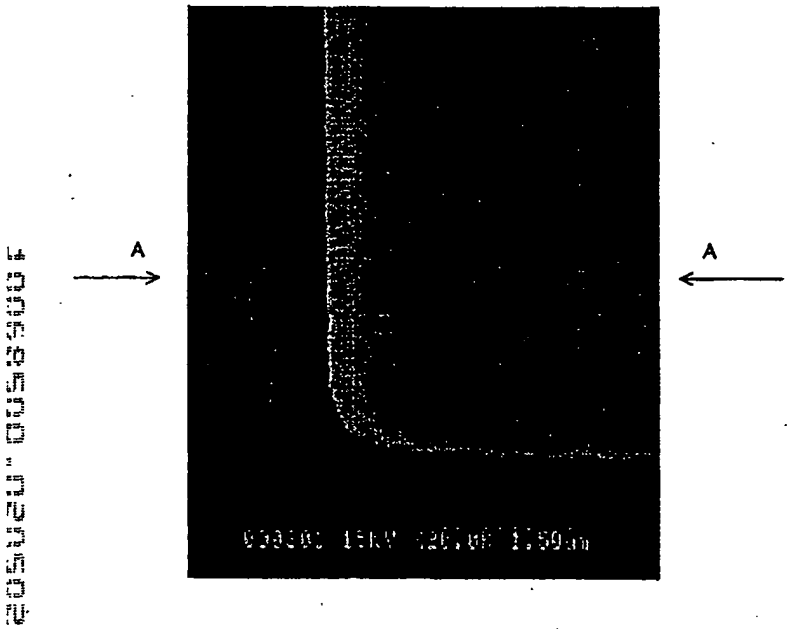


FIG. 10

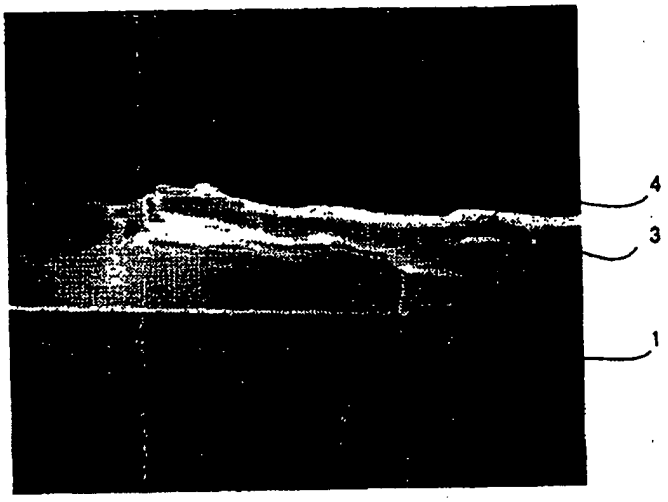


FIG. 11

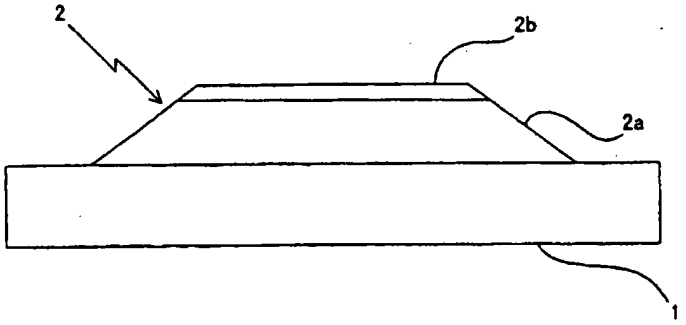
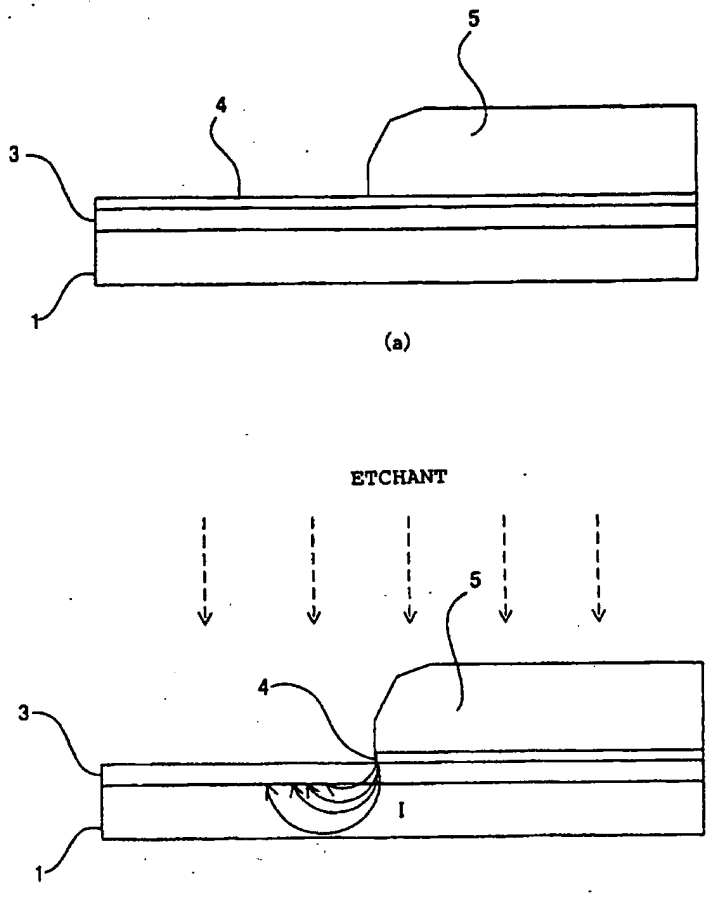


FIG. 12



02-08-02 A

Express Mail Label No. ET9267[illegible]8US

02/05/02 PTO 09551 U.S. PTO

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. JP920000310US1
Total Pages in this Submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE
Assignee Name: International Business Machines Corporation
Assignee Residence: Armonk, New York

JL000 U.S. PTO 10/060500 02/05/02

and invented by:

Takatoshi Tsujimura, et al.

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having **16** pages and including the following:
   - a. ☒ Descriptive Title of the Invention
   - b. ☐ Cross References to Related Applications *(if applicable)*
   - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - d. ☐ Reference to Microfiche Appendix *(if applicable)*
   - e. ☒ Background of the Invention
   - f. ☒ Brief Summary of the Invention
   - g. ☒ Brief Description of the Drawings *(if drawings filed)*
   - h. ☒ Detailed Description
   - i. ☒ Claim(s) as Classified Below
   - j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL **(Large Entity)** *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Docket No. **JP920000310US1** Total Pages in this Submission

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   - a. ☒ Formal — Number of Sheets **11**
   - b. ☐ Informal — Number of Sheets ______

4. ☒ Oath or Declaration
   - a. ☐ Newly executed *(original or copy)* ☒ Unexecuted
   - b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   - c. ☒ With Power of Attorney ☐ Without Power of Attorney
   - d. ☐ <u>*DELETION OF INVENTOR(S)*</u>
     Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☒ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   - a. ☐ Paper Copy
   - b. ☐ Computer Readable Copy *(identical to computer copy)*
   - c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☒ Certificate of Mailing

    ☐ First Class ☒ Express Mail *(Specify Label No.)*: **ET926726378US**

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity) *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Docket No. JP920000310US1
	Total Pages in this Submission

Accompanying Application Parts (Continued)

15. ☒ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Request That Application Not Be Published Pursuant To 35 U.S.C. 122(b)(2)

17. ☐ Pursuant to 35 U.S.C. 122(b)(2), Applicant hereby requests that this patent application not be published pursuant to 35 U.S.C. 122(b)(1). Applicant hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing of the application.

Warning

An applicant who makes a request not to publish, but who subsequently files in a foreign country or under a multilateral international agreement specified in 35 U.S.C. 122(b)(2)(B)(i), must notify the Director of such filing not later than 45 days after the date of the filing of such foreign or international application. A failure of the applicant to provide such notice within the prescribed period shall result in the application being regarded as abandoned, unless it is shown to the satisfaction of the Director that the delay in submitting the notice was unintentional.

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
JP920000310US1
Total Pages in this Submission

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS EXPRESS MAIL IN AN ENVELOPE ADDRESSED TO: U.S. PATENT AND TRADEMARK OFFICE, P.O. Box 2327, ARLINGTON, VA 22202. THE APPLICANT AND/OR ATTORNEY REQUESTS THE DATE OF DEPOSIT AS THE FILING DATE.

Express Mail No: ET926726378US

Date of Deposit: February 5, 2002

Name of Person Making Deposit: Karen Cing-Mars

Signature: Karen Cing-Mars 2/5/02

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	18	- 20 =	0	x	$18.00	$0.00
Indep. Claims	2	- 3 =	0	x	$84.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$740.00
OTHER FEE *(specify purpose)* _____						$0.00
					TOTAL FILING FEE	$740.00

☐ A check in the amount of to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 09-0458 as described below. A duplicate copy of this sheet is enclosed.

- ☒ Charge the amount of $740.00 as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Tiffany L. Townsend
Signature

Dated: February 5, 2002

Tiffany L. Townsend, Attorney
Registration No. 43,199
Telephone: (845) 894-3668
Fax: (845) 892-6363

cc:
FI-044

P01ULRG/REV05

File History Report

☐ Paper number _____ is missing from the United States Patent and Trademark Office's original copy of the file history. No additional information is available.

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- ☐ **PTO 892**
- ☐ **PTO 948**
- ☐ **PTO 1449**
- ☐ **PTO 1474**
- ☐ **Assignment**

Additional comments
Cover Sheet Is Missing

#2
00 310

日 本 国 特 許 庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office

出願年月日
Date of Application: ２００１年 ２月 ６日

出願番号
Application Number: 特願２００１－０２９５８７

出願人
Applicant(s): インターナショナル・ビジネス・マシーンズ・コーポレーション

２００１年 ５月２５日

特許庁長官
Commissioner,
Japan Patent Office 及川耕造

出証番号 出証特２００１－３０４４０１６

特２００１－０２９５８７

【書類名】　特許願
【整理番号】　JP9000310
【提出日】　平成13年 2月 6日
【あて先】　特許庁長官　殿
【国際特許分類】　G02F 1/1343
G02F 1/36
G09F 9/00
【発明者】
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【プルーフの要否】　要

【書類名】　明細書

【発明の名称】　表示装置用アレイ基板、アレイ基板の製造方法、および該アレイ基板を用いた表示デバイス

【特許請求の範囲】

【請求項１】　絶縁性基板上に形成された薄膜トランジスタアレイと、該絶縁性基板上に配置された複数の配線と、該配線の一端に配置され前記配線にそれぞれ接続される接続パッドと、画素電極とを含む表示用アレイ基板であって、前記接続パッドの端部と画素電極端部との間にダミー導体パターンが配置された表示用アレイ基板。

【請求項２】　前記ダミー導体パターンは、３０面積％以上である、請求項１に記載の表示用アレイ基板。

【請求項３】　前記ダミー導体パターンは、ランド・パターンまたはライン・アンド・スペース・パターンとされる、請求項１に記載の表示用アレイ基板。

【請求項４】　前記配線は、下部導電材と上部導電材とから構成され、前記下部導電材は、アルミニウムまたはアルミニウム合金である、請求項１に記載の表示用アレイ基板。

【請求項５】　前記上部導電材は、不動態化電位を有する、請求項４に記載の表示用アレイ基板。

【請求項６】　前記上部導電材は、モリブデンまたはモリブデン合金である、請求項４または５に記載の表示用アレイ基板。

【請求項７】　絶縁性基板上に配置された複数の配線と該配線の一端に配置され前記配線にそれぞれ接続される接続パッドとを含む薄膜トランジスタアレイを形成する工程と、

画素電極を形成する工程と、

前記接続パッドの端部と画素電極端部との間にダミー導体パターンを形成する工程とを含む表示用アレイ基板の製造方法。

【請求項８】　前記ダミー導体パターンを、３０面積％以上となるように形成する、請求項７に記載の表示用アレイ基板の製造方法。

【請求項９】　前記ダミー導体パターンを、ランド・パターンまたはライン・

アンド・スペース・パターンとして形成する、請求項７に記載の表示用アレイ基板の製造方法。

【請求項１０】　前記配線は、下部導電材と上部導電材とから構成され、前記下部導電材は、アルミニウムまたはアルミニウム合金であり、前記上部導電材は、モリブデンまたはモリブデン合金である請求項７～９のいずれか１項に記載の表示用アレイ基板の製造方法。

【請求項１１】　前記配線は、ウエット・エッチングにより形成される、請求項７～請求項１０のいずれか１項に記載の表示用アレイ基板の製造方法。

【請求項１２】　請求項１～請求項６に記載の表示用アレイ基板を含む、表示デバイス。

【請求項１３】　液晶ディスプレイ・デバイスとして使用される、請求項１２の表示デバイス。

【請求項１４】　エレクトロ・ルミネッセンス・ディスプレイ・デバイスとして使用される、請求項１２に記載の表示デバイス。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】

本発明は、表示用アレイ基板、該表示用アレイ基板の製造方法、および該表示用アレイ基板を使用した表示デバイスに関する。

【０００２】

【従来の技術】

薄膜トランジスタ（ＴＦＴ）アレイを使用した表示デバイスは、低消費電力であること、および表示デバイスを小型化できること、といったことから多用されている。薄膜トランジスタアレイは、絶縁性基板上に、ゲート電極、ソース電極、ドレイン電極といった電極とからなる薄膜トランジスタと、各電極に接続される走査線、信号線といった配線と、画素電極とを形成することにより製造される。

【０００３】

近年では、上述した表示デバイスにはより高速動作化、高精細化、大型化が求

められることが多く、表示デバイスを形成する表示用アレイの各構成要素には、高速化、および高密度化が求められる。特に、薄膜トランジスタアレイを高速で動作させるためには、走査線、信号線といった配線に低抵抗のアルミニウム（Ａｌ）を使用することが、ゲート・パルスの遅延を低下させることができ、薄膜トランジスタへの書込み速度を高めることができるので好ましい。

【０００４】

ところで、アルミニウムは抵抗が低いものの容易に酸化され易いという性質を有しているため、アルミニウムを使用した配線は、多くの場合、アルミニウムを下部導電材として用い、より酸化されにくい、クロム、タンタル、チタン、モリブデンといった材料を上部導電材として用いる、２層構造として構成されている。図１１は、絶縁性基板１上に配線２が形成されたところを模式的に示した図である。ガラスなどの絶縁性基板１上には、下部導電材の膜２ａが堆積されており、この膜２ａの上側に上部導電材の膜２ｂが堆積されている。膜２ａおよび膜２ｂは、それぞれ例えば適切なエッチングプロセスにより、テーパが付けられた端部となるようにパターンニングされる。

【０００５】

図１１に示したテーパ形状を形成するためには、上部導電材のエッチング速度を高める必要がある。図１１に示したテーパ形状を形成するため、これまで種々の方法が提案されている。例えば、特開平１０－９０７０６号公報においては、走査線接続パッドおよび信号線接続パッドのぞれぞれ反対側にダミー接続パッドを設ける方法が提案されている。この方法によれば、配線密度が基板端部において低下して、相対的に増加することになるエッチャントによるオーバー・エッチングを防止することにより下部導電材３のアンダーカットを防止すると共に、適切なテーパを配線２へと付与することで層間ショートを防止している。

【０００６】

しかしながら、この方法は、薄膜トランジスタアレイ基板の端部におけるエッチングの均一性を向上させることは可能とするものの、画素電極の端部から、接続パッドまでの間において例えば引出し配線が形成される部分など、配線密度が低下しがちになる領域における信号線のアンダーカットを、効果的に防止するこ

とはできない。

【０００７】

また、特開平１０－２４０１５０号公報では、アルミニウムと、このアルミニウムの上部に形成されたモリブデンといった金属から形成されるパッドとを湿式でエッチングすることにより、２層で構成された配線に対して２０～７０°のテーパ角度を形成する方法が開示されている。この方法は湿式エッチングにより、２層構成の導電膜から形成された配線に対して所定のテーパを付与することができるものの、配線密度の低下する基板領域においても選択比を維持させつつ、均一なエッチングを行う方法については何ら開示するものではない。

【０００８】

【発明が解決しようとする課題】

図１２は、配線に対して上述したテーパ形状を与えるためにこれまで用いられているウエット・プロセスを用いたパターニング・プロセスの拡大模式図である。絶縁性基板１上には、図１２（ａ）に示すように、下部導電材３と、上部導電材４とがフィジカル・ベーパ・デポジッションといった方法により成膜されている。図１２（ａ）においては、フォトレジスト膜５が、上部導電材４の膜の上に塗布されて、所望された形状にパターニングされているのが示されている。各膜は、リン酸、硝酸、酢酸、及びこれらの混合物などの水溶液といったエッチャントによりエッチングされて、所望するテーパ形状が形成されることになる。

【０００９】

図１２（ｂ）は、上部導電材４と下部導電材３とから構成される配線を、ウエット・エッチングする場合に、各膜のエッチングに伴って発生する電気化学的プロセスを示した図である。図１２（ｂ）においては、フォトレジスト膜５に被覆された上部導電材４の内側層部分は溶解しないものの、フォトレジスト膜５の端部では、上部導電材がエッチャントにより溶解されることになる。ウエット・エッチングにより配線を形成する場合には、フォトレジスト膜５により保護された上部導電材４は、フォトレジスト端部から横方向へとさらに溶解して陽イオンとなり、その結果放出される電子が下部導電材３に向かって電子を供給するので、アノードとして機能する。また、下部導電材３は、このためカソードとして作用

することとなり電気化学的な電池を形成する。ここで、必要とされるテーパ形状を形成させるために上部導電材４のエッチング速度を高めて行くと、上部導電材４が溶解することにより発生し、下部導電材３へと流れる電子の密度が、上部導電材４の溶解速度が増加するにつれ、増大することになる。図１２（ｂ）においては、上部導電材４から下部導電材３へと流れる電流Ｉが模式的に示されている。

【００１０】

エッチング速度が高まるにつれ、上部導電材４のエッチャントに露出した面積に対して流れる電流の密度は、上部導電材４の不動態化電流密度を超えることになる。このような場合、上部導電材４は不動態化しエッチャントにより溶解されなくなり、エッチングの進行と共に下部導電材３の溶解のみが進行してその結果アンダーカットが発生することになる。このようなアンダーカットが発生すると、例えばゲート配線といった配線を絶縁膜により充分に被覆することができない場合も生じ、これが層間ショートといった不都合を生じさせ、表示デバイスの歩留まりを低下させることになっていた。

【００１１】

本発明は、上記問題点に鑑みてなされたものであり、充分なエッチング速度及び選択比でエッチングを行うことを可能とすると共に、アンダーカットを発生させず、さらには、大型、かつ高精細な表示デバイスを提供することを可能とする、表示用アレイ基板、表示用アレイ基板の製造方法および該表示用アレイ基板を用いた表示デバイスを提供することを目的とする。

【００１２】

【課題を解決するための手段】

本発明の上記目的は、本発明の表示用アレイ基板、表示用アレイ基板の製造方法および表示デバイスを提供することにより達成される。

【００１３】

すなわち、本発明の請求項１の発明によれば、絶縁性基板上に形成された薄膜トランジスタアレイと、該絶縁性基板上に配置された複数の配線と、該配線の一端に配置され前記配線にそれぞれ接続される接続パッドと、画素電極とを含む表

示用アレイ基板であって、前記接続パッドの端部と画素電極端部との間にダミー導体パターンが配置された表示用アレイ基板が提供される。前記ダミー導体パターンは、３０面積％以上とすることができる。本発明においては、前記ダミー導体パターンは、ランド・パターンまたはライン・アンド・スペース・パターンとすることができる。本発明においては、前記配線は、下部導電材と上部導電材とから構成され、前記下部導電材は、アルミニウムまたはアルミニウム合金とすることができる。本発明においては、前記上部導電材は、不動態化電位を有する。前記上部導電材は、モリブデンまたはモリブデン合金とすることができる。

【００１４】

本発明によれば、絶縁性基板上に配置された複数の配線と該配線の一端に配置され前記配線にそれぞれ接続される接続パッドとを含む薄膜トランジスタアレイを形成する工程と、画素電極を形成する工程と、前記接続パッドの端部と画素電極端部との間にダミー導体パターンを形成する工程とを含む表示用アレイ基板の製造方法が提供される。本発明においては、前記ダミー導体パターンは、３０面積％以上となるように形成することが好ましい。また、本発明においては、前記ダミー導体パターンを、ランド・パターンまたはライン・アンド・スペース・パターンとして形成することができる。本発明においては、前記配線は、下部導電材と上部導電材とから構成され、前記下部導電材は、アルミニウムまたはアルミニウム合金であり、前記上部導電材は、モリブデンまたはモリブデン合金とすることができる。本発明においては、前記配線は、ウエット・エッチングにより形成される。

【００１５】

さらに、本発明においては、請求項１～請求項６に記載の表示用アレイ基板を含む、表示デバイスが提供される。

【００１６】

本発明においては、液晶ディスプレイ・デバイスまたはエレクトロ・ルミネッセンス・ディスプレイ・デバイスとして使用される表示デバイスを提供することができる。

【００１７】

【発明の実施の形態】

以下、本発明を図面に示した実施の形態をもって詳細に説明するが、本発明は、図面に示した実施の形態に限定されるものではない。

【００１８】

図１は、本発明の表示用アレイ基板を使用した表示デバイスの実施の形態を示した一部切り欠き斜視図である。図１に示すように、本発明の表示デバイスは、絶縁性基板上に形成された表示用アレイ基板１０の上に、順次、液晶層１１と、透明電極１２と、ガラス基板１３とが積層されて構成されている。絶縁性基板１０上に形成された配線１４は、表示用アレイ基板の図示しない端部まで延ばされていて、図示しない接続パッドを介して図示しない駆動システムへと接続されている。

【００１９】

図２は、図１において示した本発明の表示用アレイ基板１０を使用した表示デバイスの上面図である。本発明の表示用アレイ基板１０は、複数の薄膜トランジスタ２１がアレイとして構成されており、各薄膜トランジスタ２１には、画素電極２２が接続され、薄膜トランジスタ２１により電位が制御されている。図２に示した表示用アレイ基板１０においては、さらに薄膜トランジスタ２１には、それぞれ走査線２３および信号線２４が接続されているのが示されている。

【００２０】

それぞれの走査線２３は、走査線接続パッド２５を介してドライバ２６へと接続されており、それぞれの信号線２４は、信号線接続パッド２７を介してドライバ２８へと接続されている。これらの走査線２３および信号線２４は、それぞれ同一の構成として形成されていて、図１１に示したように、下部導電材３と、上部導電材４とから構成されている。

【００２１】

本発明において、配線として用いることができる下部導電材３としては、抵抗を低めるという観点からアルミニウムを使用することができる。また、本発明において用いることができる上部導電材４としては、アルミニウムの保護を行うといった点から、モリブデン（Ｍｏ）を使用することが好ましい。しかしながら、

本発明においては下部導電材３としては、アルミニウムの他、アルミニウム合金を使用することもでき、また、上部導電材４としては、クロム、タンタル、チタン、モリブデンの合金を使用することもできる。下部導電材３の膜厚は特に制限はないが、上部導電材の膜厚は、薄くなればなるほど、電流が集中し易くなるので、厚いことが好ましい。しかしながら、厚くなればなるほど応力の問題も発生するので、本発明においては、上部導電材４の膜厚としては、３０ｎｍ～１００ｎｍとすることが好ましい。

【００２２】

本発明は、上部導電材４が不動態化することにより発生する下部導電層３のアンダーカットを防止することを可能とするものである。本発明において不動態化とは、酸またはアルカリといったエッチャントに対して例えばモリブデンといった金属または金属合金が溶解しなくなる現象をいい、例えばアノードとして作用する金属が溶解しなくなることを意味する。このような不動態化する金属または金属合金としては、具体的には、例えば本発明においては、不動態化電位、すなわち、フラーデ電位を有する金属または金属合金を挙げることができる。なお、本発明においては、フラーデ電位とは、化学大辞典（縮刷版第３２刷、共立出版株式会社発行、化学大辞典編集委員会編）、第７巻、第９１１頁に記載の、金属が不動態化する電流密度を生じさせる電位を意味する。

【００２３】

さらに、図２に示した実施の形態においては、画素電極２２と各接続パッド２５，２７との間は、ダミー導体パターン２９を配置することにより、配線密度が高められている。このため走査線２３および信号線２４のエッチング時に下部導電材３のアンダーカットや、マウス・ホール欠陥を生じさせずに表示用アレイ基板全面にわたり、良好な配線を形成することが可能となる。このダミー導体パターン２９は、上述した走査線２３および信号線２４と同一の材料の２層構造としてパターンニングを行う際に同時に形成することができる。

【００２４】

図３は、図２に示した本発明の表示用アレイ基板１０の実施の形態において、ダミー導体パターン２９が形成された部分を拡大して示した図である。図３に示

したダミー導体パターン２９は、ダミー導体パターン２９が接続パッド２５と、画素電極の端部３０との間において、ライン・アンド・スペース・パターンとして形成されているのが示されている。本発明においては、ダミー導体パターン２９は、図３に示すライン・アンド・スペース・パターンとして形成することができるし、本発明においては、ダミー導体パターン２９として、ダミー導体パターン２９が形成される領域を完全に被覆するランド・パターンを用いることもできる。

【００２５】

いずれのパターンを用いる場合であっても、本発明においては、ダミー導体パターン２９自体の配線密度が３０％以上となるように形成することが、上部導電材４を必要な速度で溶解させつつ、下部導電材３に対してアンダーカットを形成させずに適切なテーパを形成させる点で好ましい。

【００２６】

さらに、本発明においてはダミー導体パターン２９を配置する場合には、ダミー導体パターン２９を、画素電極２２の端部３０と接続パッド２５，２７との間において、ダミー導体パターン２９を含む配線密度が３０％以上となるように形成することがさらに好ましい。本発明において、配線密度とは、ダミー導体パターンが形成される所定の領域の面積において、信号線、走査線、引き出し線といった配線が形成されている部分の面積の面積比をいうものとする。

【００２７】

図４は、本発明のダミー導体パターン２９の別の実施の形態を示した図である。図４に示した実施の形態においては、配線密度３０％以上のダミー導体パターン２９が、さらに高い密度で配置されており、エッチング時に上部導電材４のエッチャントへの露出部への電流の集中を、より低減させている。図４に示されているように、ダミー導体パターン２９は、いかなる形状、パターンを有していても良く、複数種類のダミー導体パターン２９をいかなるようにでも組み合わせて使用することができる。

【００２８】

図５は、本発明の表示用アレイ基板１０の製造方法の実施の形態を示した図で

ある。図５においては、本発明の表示用アレイ基板１０の製造方法を逆スタガ型の薄膜トランジスタ１１を形成する場合を例として説明する。まず、図５（ａ）に示すように透明または不透明な絶縁性基板１に下部導電材３としてアルミニウムを、上部導電材４としてモリブデンを使用して膜を堆積させる。

【００２９】

その後、図５（ｂ）に示すように、膜上にフォトレジスト３１を塗設し、特に図示しない画素電極と、接続パッドとの間において配線密度が低くなる部分にダミー導体パターン２９を形成させるパターンが設けられたフォトマスク３２を使用してフォトレジストの露光・現像を行う。

【００３０】

ついで、リン酸、硝酸、酢酸、またはこれらの混合された水溶液をエッチャントとして用いてエッチングを行い、配線２およびダミー配線パターン２９を形成する。ダミー配線パターン２９を配線密度が低い部分に配置することにより、モリブデンといった導電材料が不動態化しがちな領域においても、図５（ｃ）に示した良好なテーパ形状を有する配線を形成させることが可能となる。テーパ角度は、エッチャントの組成、エッチング条件を調節することにより２０°～７０°の範囲とすることができ、さらには、約２０°～約６０°とすることが好ましい。

【００３１】

その後、本発明においてはゲート絶縁膜、ゲート電極、ソース電極、ドレイン電極、および画素電極などを形成することにより、本発明の表示用アレイ基板１０が製造される。本発明においては、必要に応じてダミー導体パターン２９は、除去することもできるし、除去せずそのまま残しておくことも可能である。

【００３２】

図６は、図３に示したダミー導体パターン１９を設けてエッチングを行った場合に得られた図３に示す配線３３の形状を示した電子顕微鏡写真である。このとき、上部導電材４としてはモリブデンを用い、下部導電材３としてはアルミニウムを使用した。モリブデンの膜厚は、約５０ｎｍであり、エッチャントとしては、リン酸、硝酸、酢酸の混合水溶液を用いるウエット・エッチングを行った。図

６に示されるように、ダミー導体パターン２９を形成することにより、従来では、アンダーカットが発生しがちであった、配線部分においても良好なテーパ形状が形成されていることがわかる。

【００３３】

また、図７は、図４に示したダミー導体パターン２９を形成して、図６と同一の条件でエッチングを行った場合に得られた図４に示す配線３４の形状を示した図である。図７に示すように、ダミー導体パターン２９の密度を増加させても、良好なテーパ形状が得られているのが示されている。

【００３４】

図８は、ダミー導体パターン２９を配置した場合の基板上のダミー導体パターン２９の部分を含む配線のパターン密度（面積％）に対して、形成される配線のテーパ角度をプロットした図である。図８に示すように、エッチングにより得られる配線のテーパ角度は、配線のパターン密度が増加するにつれて小さくなり、よりなだらかなテーパが形成されていて、ダミー導体パターン２９を配置することにより上部導電材４が下部導電材３のエッチングに対して充分な選択比を付与することができることが示されている。

【００３５】

図９は、比較のため、図３および図４に示したと同一のパターンを有する表示用アレイ基板１０を使用して、ダミー導体パターン２９を全く形成させずに同一の条件でエッチングを行った場合に得られる配線の形状を示した電子顕微鏡写真である。図９に示されるように、上部導電材４として使用したモリブデンが不動態化し、下部導電材３であるアルミニウムのエッチングのみが進行してしまったため、配線には、大きなアンダーカットが発生しているのが示されている。

【００３６】

図１０は、図９に示した配線の切断線Ａ－Ａに沿った断面を示した電子顕微鏡写真を示す。図１０に示されるように、下側導電材３として用いるアルミニウムは、上側導電材４として用いるモリブデンよりもエッチングが進行して、その結果、大きなアンダーカットが発生しているのが示されている。

【００３７】

本発明は、上述したように逆スタガ型の薄膜トランジスタに適用するばかりではなく、アルミニウムと、アルミニウム以外の不動態化電流密度が知られているいかなる金属とから形成される配線を含むトップゲート型薄膜トランジスタにも適用することができる。

【００３８】

さらに本発明の表示用アレイデバイスは、ガラスといった透明絶縁性基板を使用した液晶ディスプレイ・デバイスに適用することも可能であるが、不透明な絶縁性基板を使用し、この絶縁性基板上に表示用アレイを形成し、無機および有機のエレクトロ・ルミネッセンス・デバイスとして用いることも可能である。

【００３９】

上述したように、本発明によれば、充分なエッチング速度および選択比でエッチングを行うことを可能とすると共に、アンダーカットを発生させることなく、層間ショートといった不都合による製造歩留まりの低下を生じさせることのない、表示用アレイ基板、表示用アレイ基板の製造方法および該表示用アレイ基板を用いた表示デバイスを提供することが可能となる。また、本発明によれば、大型、かつ高精細な表示デバイスを提供することを可能とする、表示用アレイ基板、表示用アレイ基板の製造方法および該表示用アレイ基板を用いた表示デバイスを提供することが可能となる。

【図面の簡単な説明】

【図１】

本発明の表示用アレイ基板を使用した液晶ディスプレイ・デバイスの実施の形態を示した図。

【図２】

本発明の表示用アレイ基板の上面図。

【図３】

本発明におけるダミー導体パターンを拡大して示した図。

【図４】

本発明における別のダミー導体パターンを拡大して示した図。

【図５】

本発明の表示用アレイ基板の製造方法を示した図。

【図６】

図３に示したダミー導体パターンを使用した場合の配線のパターン形状を示した電子顕微鏡写真。

【図７】

図４に示したダミー導体パターンを使用した場合の配線のパターン形状を示した電子顕微鏡写真。

【図８】

配線のテーパ角度と、配線のパターン密度との関係を示した図。

【図９】

ダミー導体パターンを使用せずにエッチングを行った場合の配線形状を示した電子顕微鏡写真。

【図１０】

図９に示した配線形状の断面形状を示した電子顕微鏡写真。

【図１１】

配線のテーパ形状を示した模式図。

【図１２】

エッチング・プロセス時に形成される電池により形成される電流を示した図。

【符号の説明】

１…絶縁性基板

２…配線

２ａ…膜

２ｂ…膜

３…下部導電材

４…上部導電材

５…フォトレジスト

１０…表示用アレイ基板

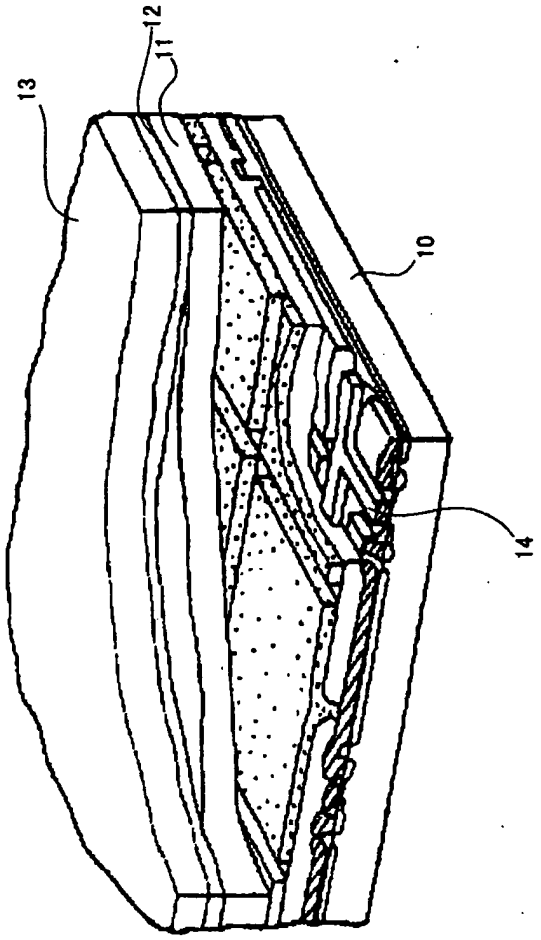
１１…液晶層

１２…透明電極

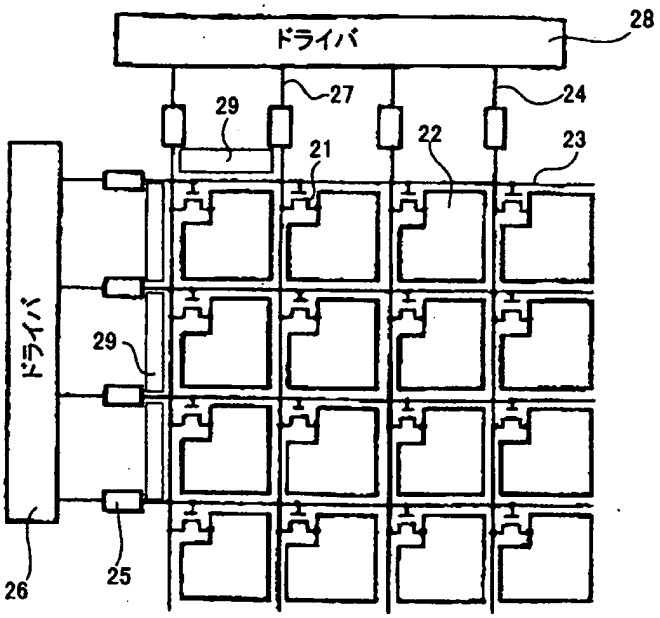
１３…ガラス基板
１４…配線
２１…薄膜トランジスタ
２２…画素電極
２３…走査線
２４…信号線
２５…走査線接続パッド
２６…ドライバ
２７…信号線接続パッド
２８…ドライバ
２９…ダミー導体パターン
３０…画素電極の端部
３１…フォトレジスト
３２…フォトマスク
３３…配線
３４…配線

【書類名】　図面

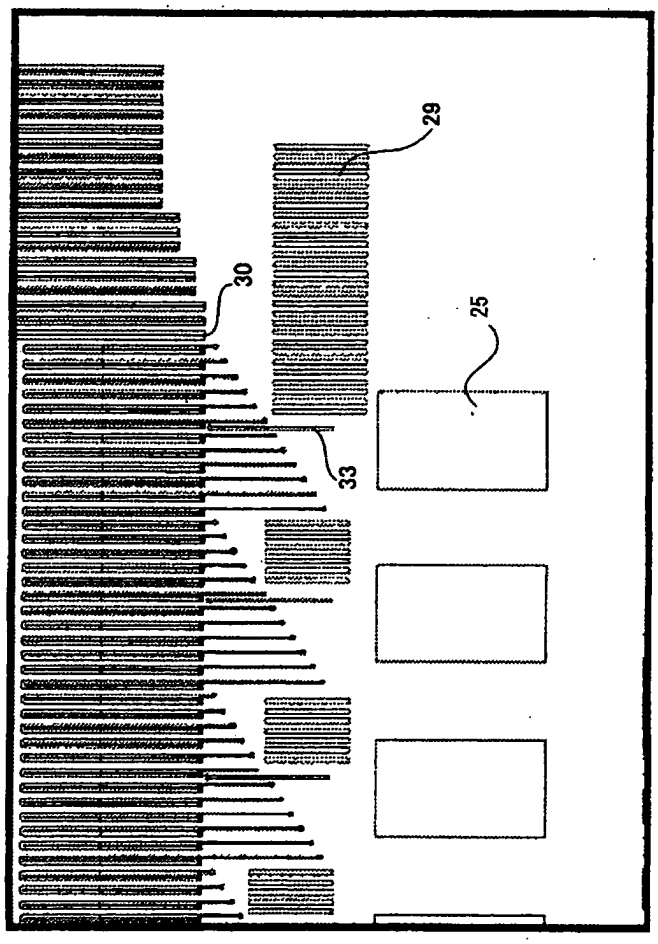
【図１】



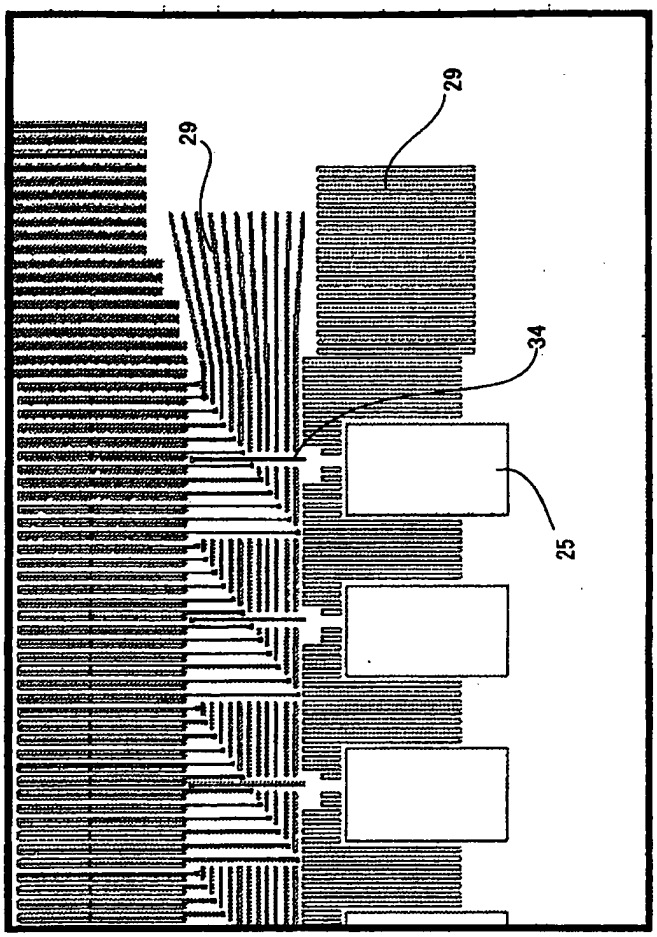
【図２】



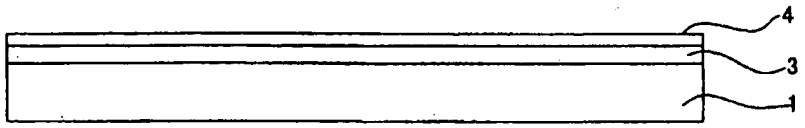
【図３】



【図４】



【図５】



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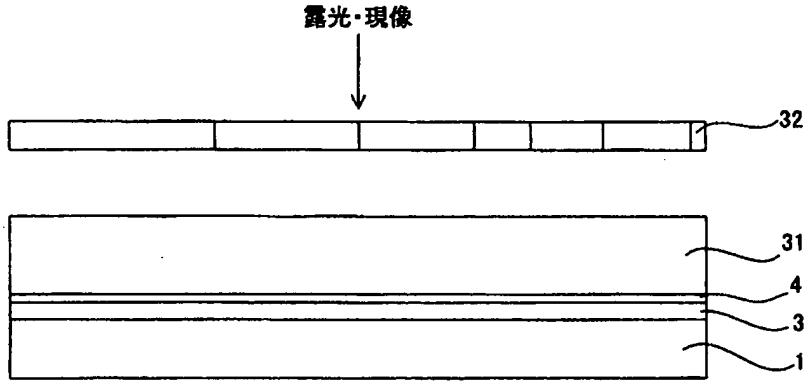
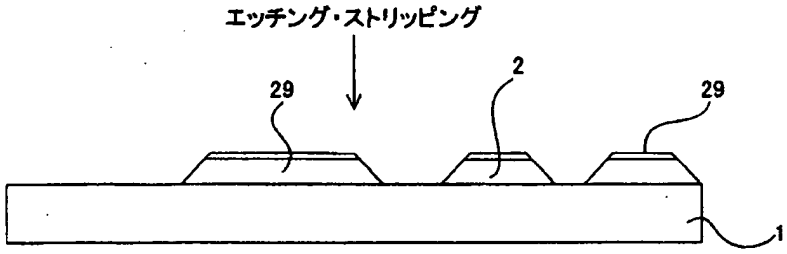
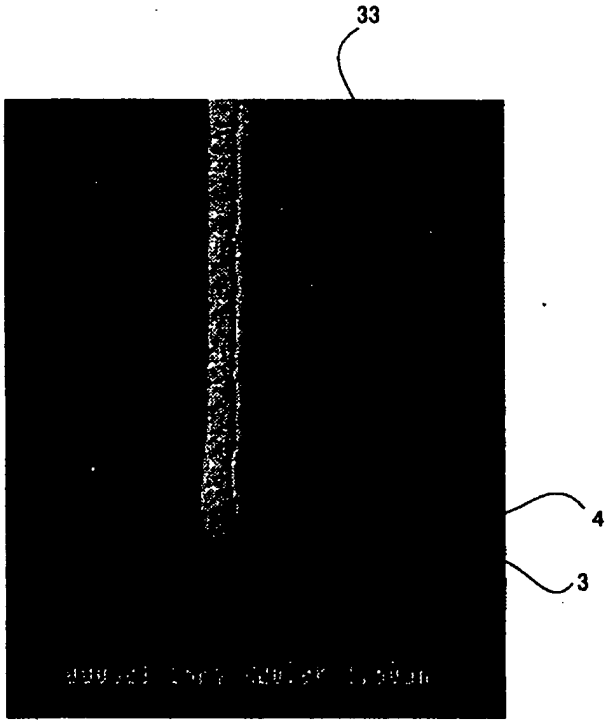


(b)

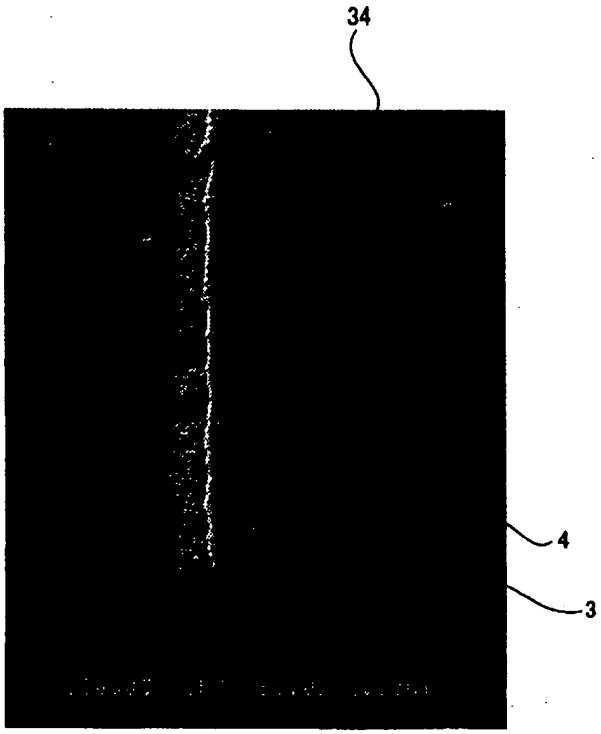


(c)

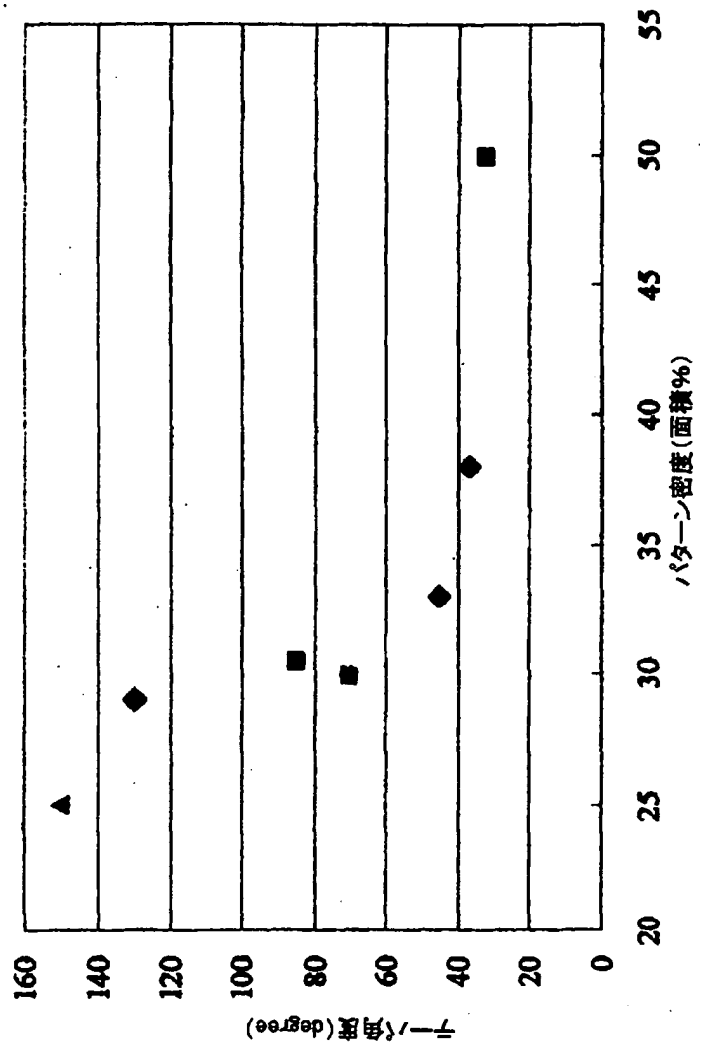
【図６】



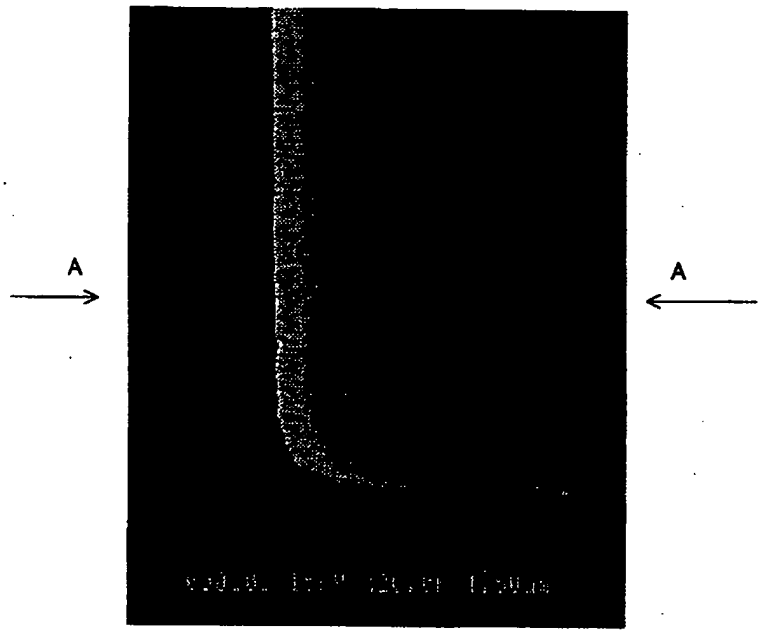
【図７】



【図８】

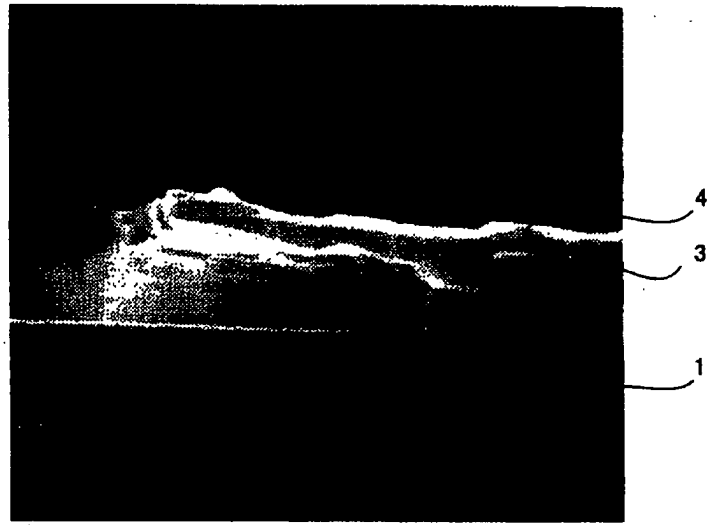

パターン密度(面積%)
20
25
30
35
40
45
50
55
テーパ角度(degree)
160
140
120
100
80
60
40
20
0

【図９】

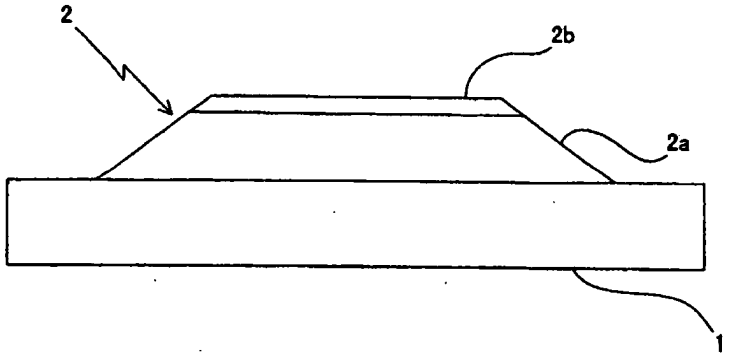


出証特２００１－３０４４０１６

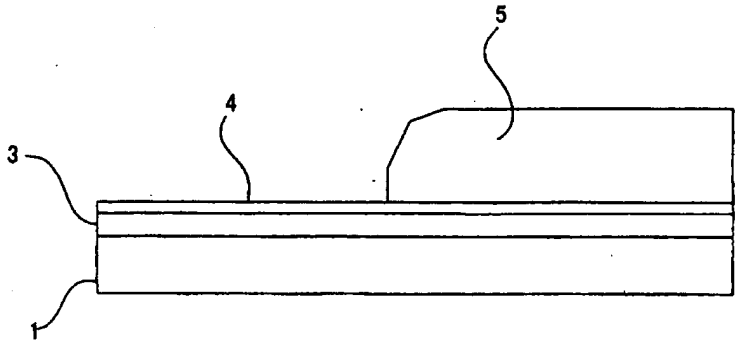
【図１０】



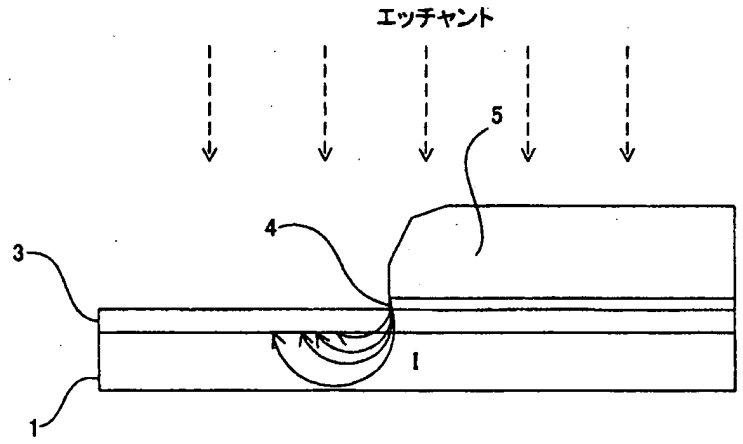
【図１１】



【図１２】



(a)



(b)

【書類名】　要約書

【要約】

【課題】　表示用アレイ基板、該表示用アレイ基板の製造方法、および該表示用アレイ基板を使用した表示デバイスを提供する。

【解決手段】　本発明は、絶縁性基板１上に形成された薄膜トランジスタアレイと、絶縁性基板１上に配置された複数の配線２３，２４と、該配線２３，２４の一端に配置されこれらの配線２３，２４にそれぞれ接続される接続パッド２５，２７と、画素電極２２とを含む表示用アレイ基板であって、接続パッド２５，２７の端部と画素電極２２の端部との間にダミー導体パターン２９が配置されている。

【選択図】　図２

認定・付加情報

特許出願の番号	特願２００１－０２９５８７
受付番号	５０１００１６４８６７
書類名	特許願
担当官	野口　耕作　　１６１０
作成日	平成１３年　３月２１日

＜認定情報・付加情報＞

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【氏名又は名称】　間山　進也

【選任した復代理人】

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認定・付加情報（続き）

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【氏名又は名称】　林　茂則

次頁無

特２００１－０２９５８７

出願人履歴情報

識別番号　〔３９０００９５３１〕

１．変更年月日　２０００年　５月１６日
［変更理由］　名称変更
住　所　アメリカ合衆国１０５０４、ニューヨーク州　アーモンク　（番地なし）
氏　名　インターナショナル・ビジネス・マシーンズ・コーポレーション

A 1X

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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO.
10/068,500	02/05/2002	Takatoshi Tsujimura	JP920000310US1	7252

32074 7590 05/29/2003

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
EVERHART, CARIDAD	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED. 05/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No.	Applicant(s)	
	10/068,500	TSUJIMURA ET AL.	
	Examiner	Art Unit	
	Carldad M. Everhart	2825	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1 136(a) In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U S C § 133)
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1 704(b)

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10 and 12-18* is/are rejected.

7)☒ Claim(s) *2 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are. a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance See 37 CFR 1 85(a)

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U S.C § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ .
4) ☐ Interview Summary (PTO-413) Paper No(s) ____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in publ c use or on sale in this country, more than one year prior to the date of application for patent in the United States

Claims 1 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Shirahashi, et al. ("Shirahashi")(US 5,285,301).

Shirahashi discloses an array of TFTs and method of forming the components of the array (col. 1, lines 19-20 and Fig. 15), comprising an insulating substrate(col. 3, lines 39-40), a plurality of wiring(col. 6, lines 10-20), pads(col. 13, lines 20-24), and dummy patterns between the pads and pixel electrodes and that are not connected to the lines (Fig. 15, in which ITO1 indicates pixel and Fig. 1 and Fig. 14, line which GL indicates lines and DGL indicates dummy lines).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3-9, 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirahashi, et al. in view of Song, et al ("Song")(US 6,163,356).

Shirahashi is silent with respect to an aluminum layer with a Mo layer on the aluminum layer. Shirahashi does disclose aluminum (col 12, lines 40-42).

Song discloses a bilayer of aluminum with a layer of chromium or molybdenum or tantalum on the aluminum to protect from etchants(col. 4, lines 38-50).

One of ordinary skill in the art would have been motivated to have provided the bilayer conductor taught by Song in the process and device taught by Shirahashi in order to protect from etchants such as those disclosed by Shsirahashi(col 12, ines 43-46).

Allowable Subject Matter

Claims 2 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not teach or suggest the area protected by the dummy metalization recited in claims 2 and 11.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caridad M. Everhart whose telephone number is 703-

308-3455. The examiner can normally be reached on Monday through Fridays 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

C. Everhart

C. Everhart
May 19, 2003

Notice of References Cited	Application/Control No 10/068,500	Applicant(s)/Patent Under Reexamination TSUJIMURA ET AL	
	Examiner Caridad M Everhart	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,163,356	12-2000	Song, et al	349/152
	B	US-5,285,301	02-1994	Shirahashi, et al	359/59
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action (See MPEP § 707 05(a))
Dates in MM-YYYY format are publication dates Classifications may be US or foreign

#9/A
Abell
9-9-03

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING SENT VIA BY FAX ON August 19, 2003 TO: COMMISSIONER FOR PATENTS, P.O. Box 1450, Alexandria, VA 22313-1450 ON:

Date of Deposit: August 29, 2003

Name of Person Faxing: Colleen J. Dow

Signature: Colleen J. Dow

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
In Re Application of: Takatoshi Tsujimura et al.	August 29, 2003 Examiner: Caridad Everhart
Serial No. 10/068,500 Filing Date: 02/05/2002	Group Art Unit: 2825
Title: Array Substrate for Display, Method of Manufacturing Array Substrate for Display and Display Device Using the Array Substrate	IBM Corporation 2070 Route 52 Dept. 18G, Bldg. 300-482 Hopewell Junction, N.Y. 12533

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In the claims:

1. (Currently Amended) An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

2. (Canceled)

3. (Original) The array substrate for display according to claim 1 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

4. (Original) The array substrate for display according to claim 3 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.

5. (Original) The array substrate for display according to claim 3 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

6. (Original) The array substrate for display according to claim 4 wherein the upper layer wiring

material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

7. (Original) The array substrate for display according to claim 5 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

8. (Original) The array substrate for display according to claim 4 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

9. (Original) The array substrate for display according to claim 5 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

10. (Currently Amended) A method for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array formed on the insulating substrate, each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

11. (Canceled)

10 12. (Original) The method for forming an array substrate for display according to claim 9 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

11 13. (Original) The method for forming an array substrate for display according to claim 12 wherein the lower layer wiring materials is selected from the group consisting of aluminum and aluminum alloys.

12 14. (Original) The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

13 15. (Original) The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

14 16. (Original) The method for forming an array substrate for display according to claim 15 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

15 17. (Original) The method for forming an array substrate for display according to claim 14 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

16 18. (Original) The method for forming an array substrate for display according to claim 15 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

OFFICIAL

Remarks:

Claims 1, 3-10 and 12 - 18 remain in the instant application. Subject matter from claims 2 and 11 were added to claims 1 and 10 respectively. The instant application is drawn to an apparatus and method relating to array substrates for displays.

The Applicants believe that there are no issues remaining in the instant matter. The Office Action indicated that claims 2 and 11 would be allowable if they were rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1 and 10, the originally presented independent claims, have been amended to include the subject matter of claims 2 and 11 respectively. Therefore, none of the art cited in the Office Action discloses teaches or claims the subject matter in independent claims 1 and 10. Further, as dependent claims 3 -9 and 12 - 18 ultimately depend on one of claim 1 and 10, none of the art cited discloses, teaches or claims the subject matter of claims 3 - 9 and 12 - 18.

Reconsideration and allowance of claims 1, 3 - 10 and 12 - 18 is respectfully requested.

Respectfully submitted,
Takatoshi Tsujimura et al.

By: _____
Tiffany L. Townsend, et al.
Attorney for Applicant
Registration No. 43,199
845-894-3668

AMENDMENT TRANSMITTAL LETTER (Large Entity) Applicant(s): Takatoshi Tsujimura et al.			Docket No. JP920000310US1
Serial No. 10/068,500	Filing Date 02/05/2002	Examiner Caridad Everhart	Group Art Unit 2825

Invention: **ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE**

FAX RECEIVED

AUG 2 9 2003

GROUP 2800

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT		RATE	ADDITIONAL FEE
TOTAL CLAIMS	18	-	20	=	0	x	$18.00	$0.00
INDEP. CLAIMS	2	-	3	=	0	x	$84.00	$0.00
Multiple Dependent Claims (check if applicable) ☐								$0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT								$0.00

OFFICIAL

☐ No additional fee is required for amendment.

☒ Please charge Deposit Account No. in the amount of

☐ A check in the amount of to cover the filing fee is enclosed.

☒ The Director is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 09-0458

- ☒ Any additional filing fees required under 37 C.F.R. 1.16.
- ☒ Any patent application processing fees under 37 CFR 1.17.

Signature

Dated: **August 29, 2003**

Tiffany L. Townsend, Registration No. 43,199
International Business Machines Corporation
2070 Route 52
Hopewell Junction, NY 12533
845-894-9665

I certify that this document and fee is being faxed, on 08/29/2003

Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature of Person Faxing Correspondence

Colleen J. Dew

Typed or Printed Name of Person Faxing Correspondence

cc:

P11LARGEREV08

File History Report

☐ Paper number _____ is missing from the United States Patent and Trademark Office's original copy of the file history. No additional information is available.

☒ The following page(s) **3 Of 8** of paper number **4** is/are missing from the United States Patent and Trademark Office's original copy of the file history. No additional information is available

☐ The following checked item(s) of paper number _____ is/are missing from the United States Patent and Trademark Office's original copy of the file history. No additional information is available

- ☐ **PTO 892**
- ☐ **PTO 948**
- ☐ **PTO 1449**
- ☐ **PTO 1474**
- ☐ **Assignment**

Additional comments

FACSIMILE TRANSMISSION TO USPTO

Caridad Everhart
703-872-9318 fax
703-872-9317 customer service

CERTIFICATION OF FACSIMILE TRANSMISSION:
I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO THE USPTO ON THE DATE SHOWN BELOW:

Date of Transmission: August 29, 2003

Name of Person Making Transmission: Colleen J. Dew

Signature: Colleen J. Dew

DOCUMENT FAXED: 8 PAGES ATTACHED; INCLUDING COVER

Re Applic of	Takatoshi Tsujimura et al.	
Docket No.	JP920000310US1	
Serial No.	10/068,500	
Filing Date	02/05/2002	
Attorney	Tiffany L. Townsend	

Attached: Amendment

INTERNATIONAL BUSINESS MACHINES CORPORATION

Intellectual Property Law
East Fishkill Facility
2070 Route 52
Hopewell Junction
New York 12533-6531

Fax: 845-892-6363
Phone: 845-894-3668

Notice of Allowability	Application No.	Applicant(s)
	10/068,500	TSUJIMURA ET AL.
	Examiner	Art Unit
	Caridad M Everhart	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 8-29-03*
2. ☒ The allowed claim(s) is/are *1,3-10 and 12-18*.
3. ☒ The drawings filed on *05 February 2002* are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3 ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

8. ☐ CORRECTED DRAWINGS must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☐ Notice of References Cited (PTO-892)
2☐ Notice of Informal Patent Application (FTO-152)
3☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
4☐ Interview Summary (PTO-413), Paper No.____.
5☐ Information Disclosure Statements (PTO-1449), Paper No. ____.
6☐ Examiner's Amendment/Comment
7☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8☐ Examiner's Statement of Reasons for Allowance
9☐ Other

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NOTICE OF ALLOWANCE AND FEE(S) DUE

32074 7590 10/01/2003

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
EVERHART, CARIDAD	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/01/2003

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/068,500	02/05/2002	Takatoshi Tsujimura	JP920000310US1	7252

TITLE OF INVENTION: ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

APPLN TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$300	$1630	01/02/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 10/03) Approved for use through 04/30/2004.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

32074 7590 10/01/2003

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,500	02/05/2002	Takatoshi Tsujimura	JP920000310US1	7252

TITLE OF INVENTION: ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$300	$1630	01/02/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
EVERHART, CARIDAD	2825	438-025000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ individual ☐ corporation or other private group entity ☐ government

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☐ Issue Fee
☐ Publication Fee
☐ Advance Order - # of Copies _____

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☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) (Date)

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address COMMISSIONER FOR PATENTS
P O Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,500	02/05/2002	Takatoshi Tsujimura	JP920000310US1	7252

32074 7590 10/01/2003

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
EVERHART, CARIDAD	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/01/2003

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 54 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 54 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (Rev. 10/03) Approved for use through 04/30/2004.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Address COMMISSIONER FOR PATENTS
P.O Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,500	02/05/2002	Takatoshi Tsujimura	JP920000310US1	7252

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
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2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
EVERHART, CARIDAD	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/01/2003

Notice of Fee Increase on October 1, 2003

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after October 1, 2003, then the amount due will be higher than that set forth in the "Notice of Allowance and Fee(s) Due" since there will be an increase in fees effective on October 1, 2003. See Revision of Patent Fees for Fiscal Year 2004; Final Rule, 68 Fed. Reg. 41532, 41533, 41534 (July 14, 2003).

The current fee schedule is accessible from (http://www.uspto.gov/main/howtofees.htm).

If the fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due" but not the correct amount in view of the fee increase, a "Notice of Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processing delays associated with mailing of a "Notice of Pay Balance of Issue Fee," if the response to the Notice of Allowance is to be filed on or after October 1, 2003 (or mailed with a certificate of mailing on or after October 1, 2003), the issue fee paid should be the fee that is required at the time the fee is paid. If the issue fee was previously paid, and the response to the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue fee now due, then the difference between the issue fee amount at the time the response is filed and the previously-paid issue fee should be paid. See Manual of Patent Examining Procedure, Section 1308.01 (Eighth Edition, August 2001).

Effective October 1, 2003, 37 CFR 1.18 is amended by revising paragraphs (a) through (c) to read as set forth below.

Section 1.18 Patent post allowance (including issue) fees.

(a) Issue fee for issuing each original or reissue patent, except a design or plant patent:
By a small entity (Sec. 1.27(a)) $665.00
By other than a small entity $1,330.00

(b) Issue fee for issuing a design patent:
By a small entity (Sec. 1.27(a)) $240.00
By other than a small entity: $480.00

(c) Issue fee for issuing a plant patent:
By a small entity (Sec. 1.27(a)) $320.00
By other than a small entity $640.00

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (Rev. 10/03) Approved for use through 04/30/2004.

[redacted]

PART B - FEE(S) TRANSMITTAL

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000

B4

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CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

32074 7590 10/01/2003

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$300	$1630	01/12/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
EVERHART, CARIDAD	2825	438-025000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

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1 Tiffany L. Townsend
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

International Business Machines Corporation Armonk, New York 10504

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

☒ Issue Fee
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☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 09-0458 (enclose an extra copy of this form). FT-352

Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature) Tiffany Townsend Date 10/20/03
Tiffany L. Townsend; Registration No. 43,199 10/20/2003

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

12/04/2003 JADD02 00000087 090458 10068500
01 FC:1501 1330.00 DA
02 FC:1504 300.00 DA

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.

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6689629

FIG. 1

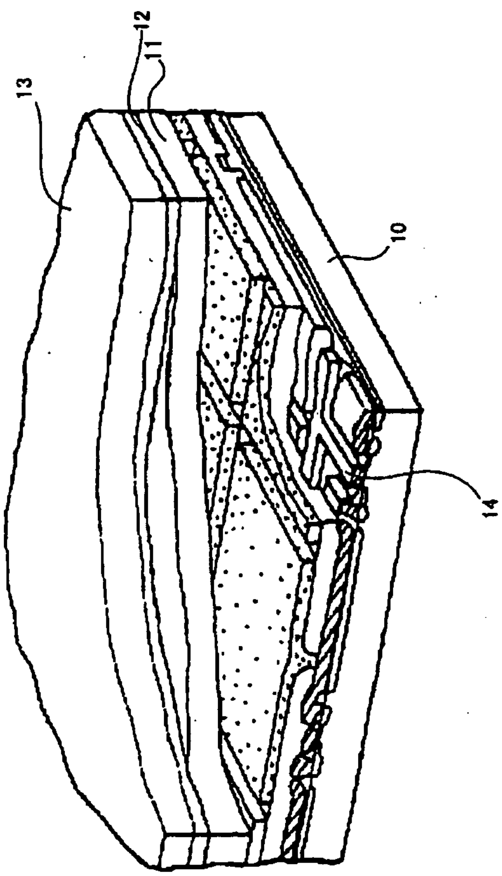
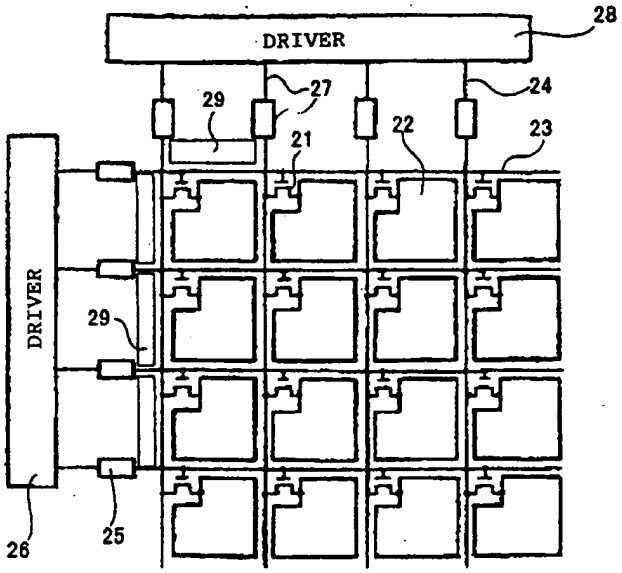
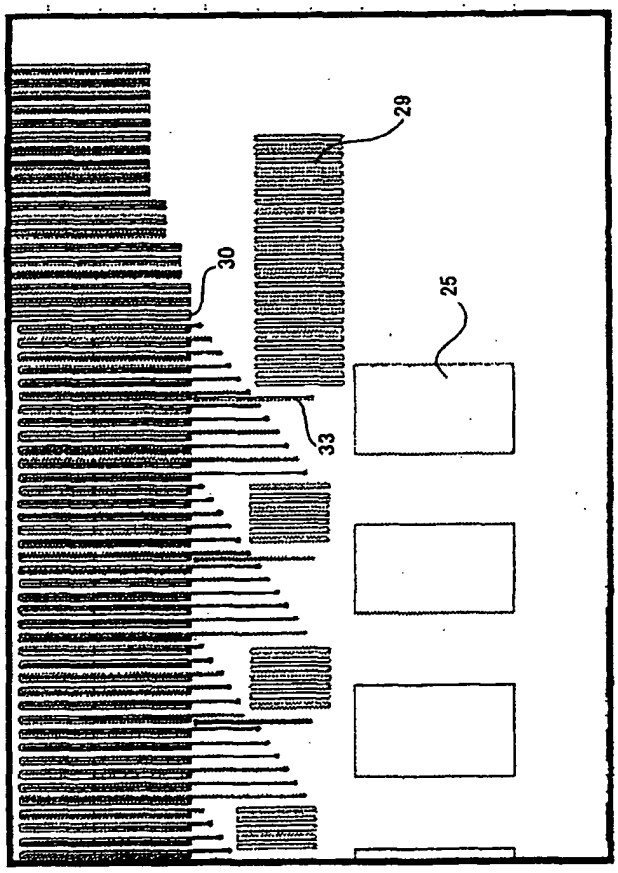


FIG. 2



2

FIG. 3



3

FIG. 4

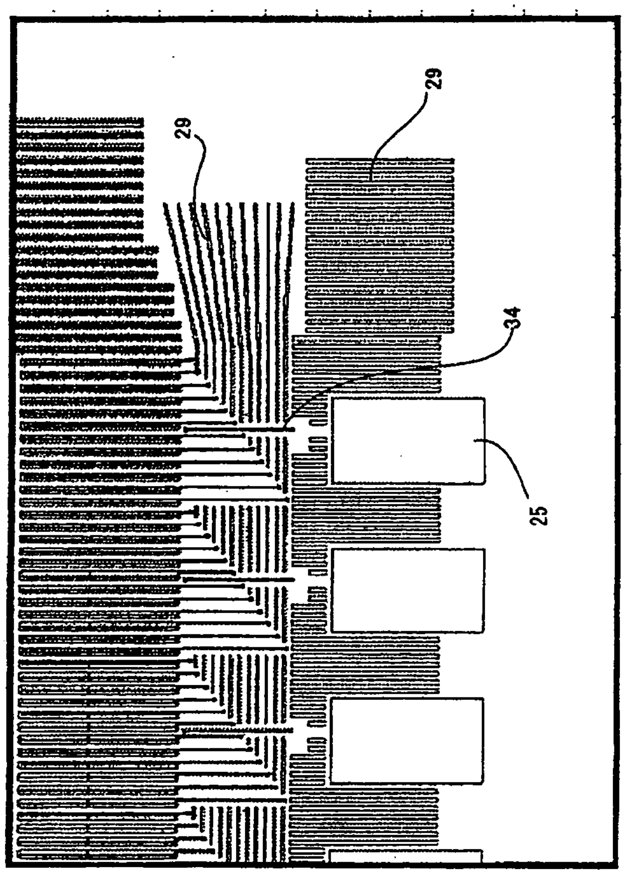
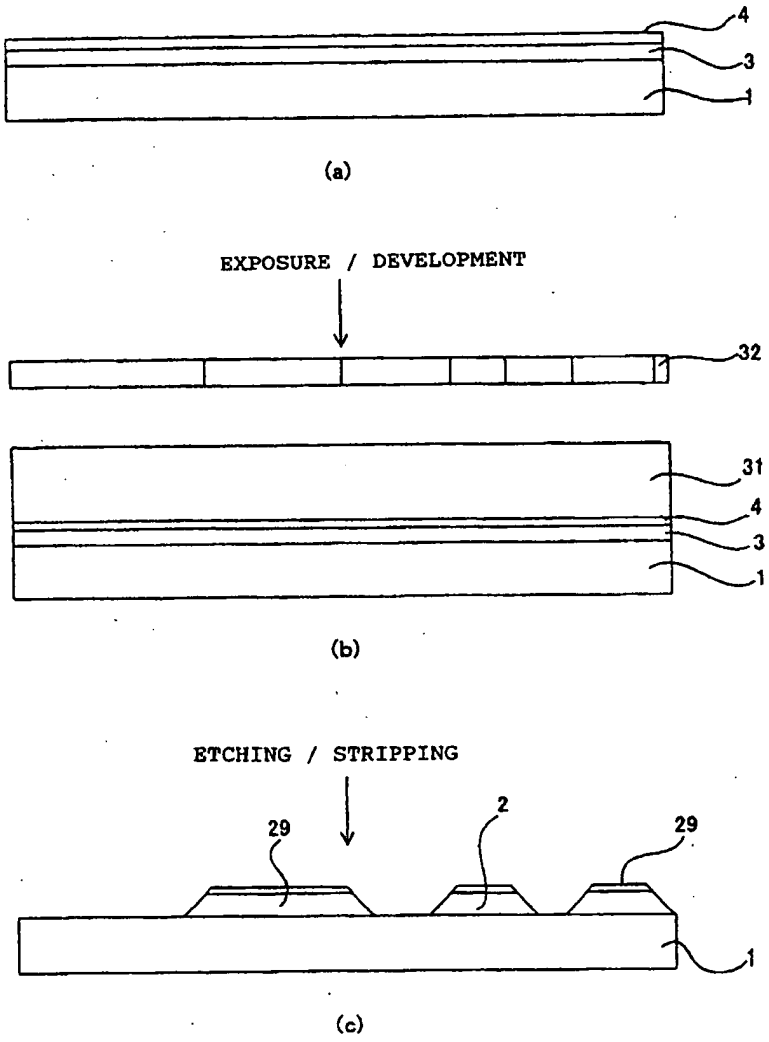
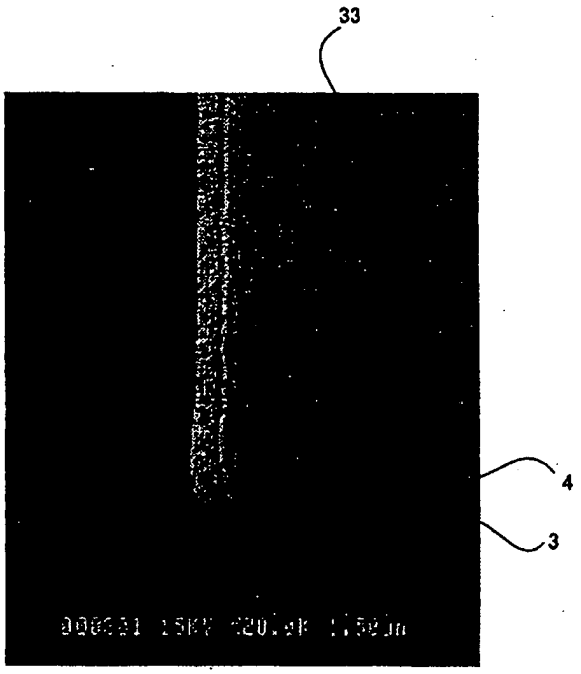


FIG. 5



5

FIG. 6



6

FIG. 7

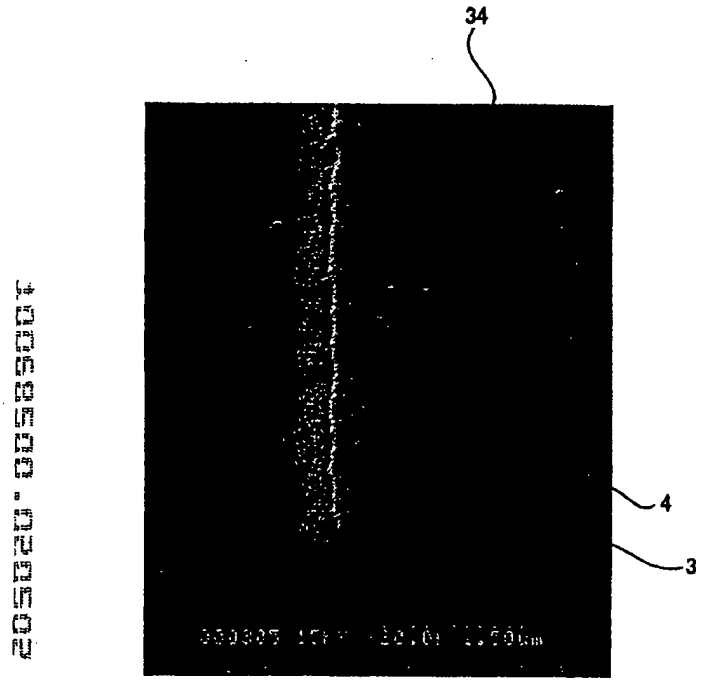
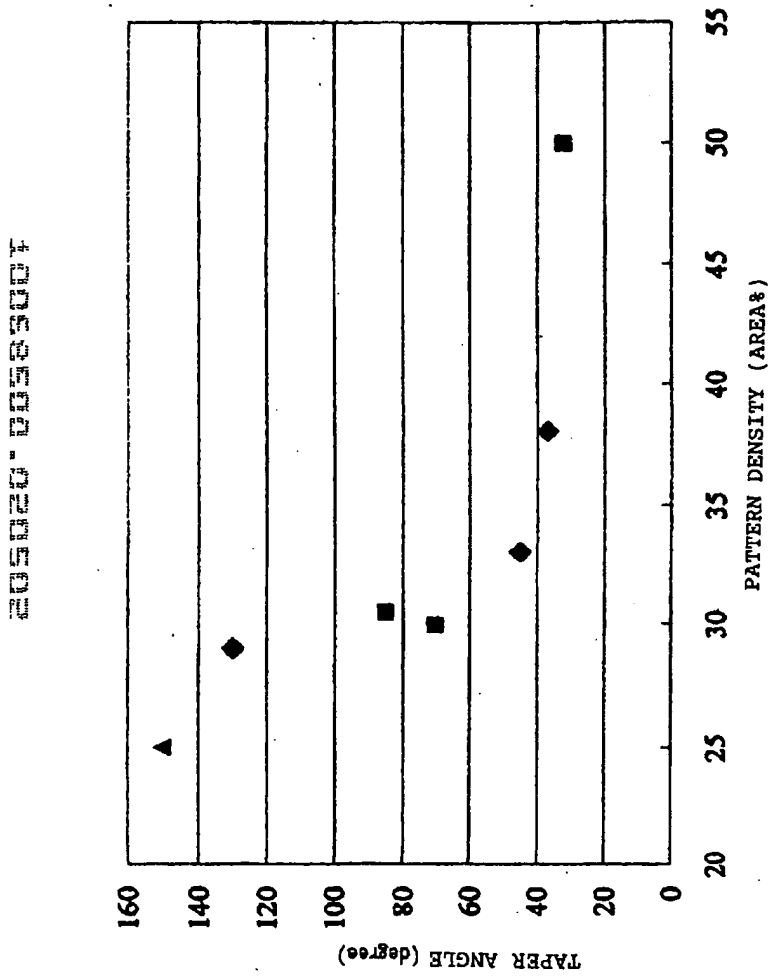


FIG. 8


TAPER ANGLE (degree)
160
140
120
100
80
60
40
20
0
PATTERN DENSITY (AREA%)
20
25
30
35
40
45
50
55

8

FIG. 9

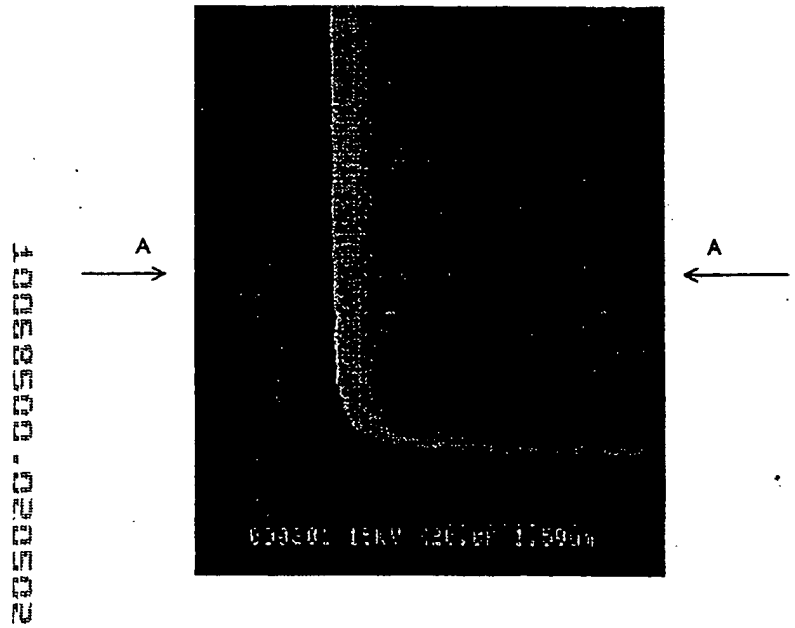


FIG. 10

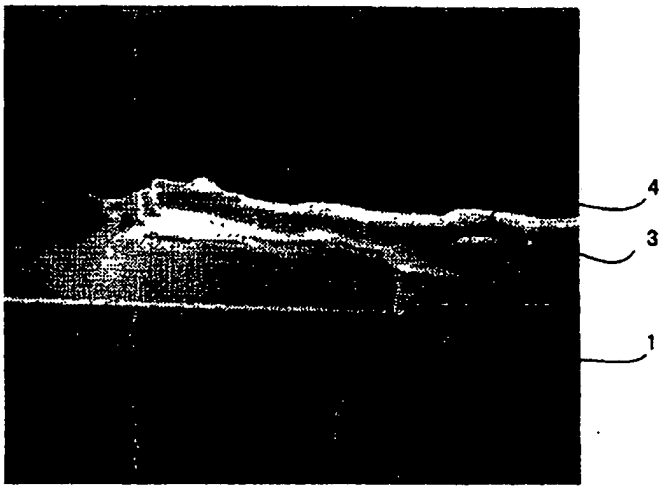
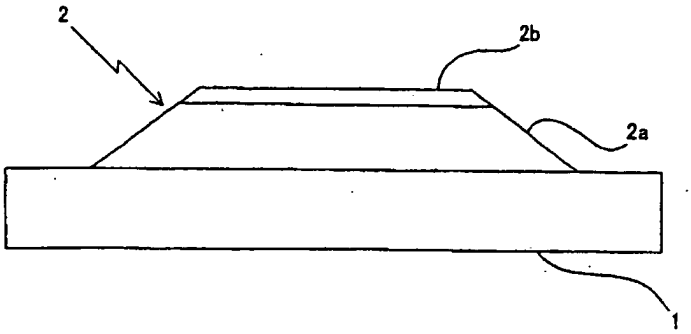
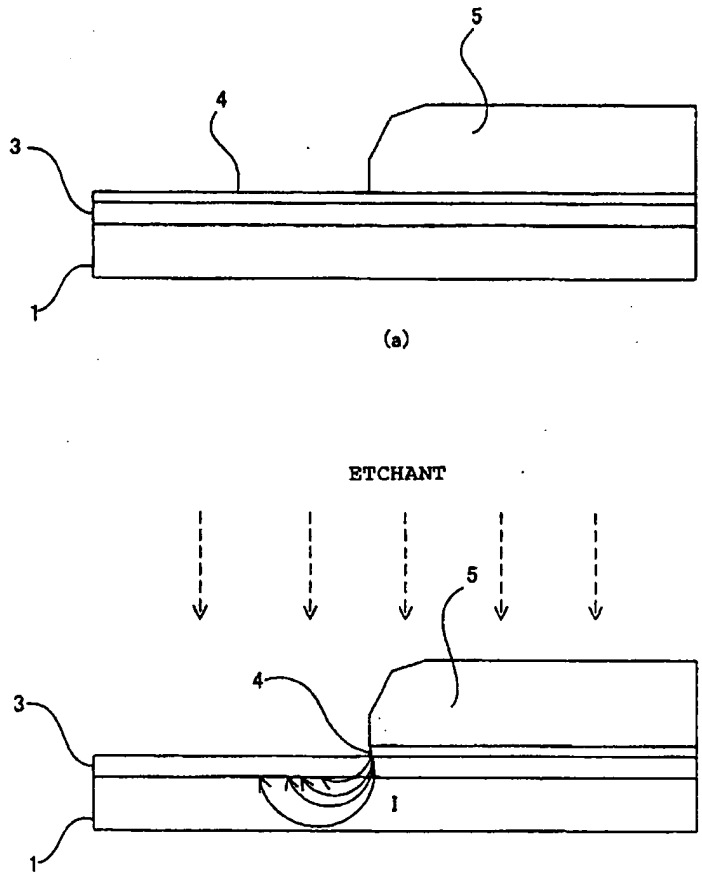


FIG. 11



10

FIG. 12



11

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ASSISTANT SECRETARY AND COMMISSIONER
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Washington, D.C. 20231

CHANGE OF ADDRESS/POWER OF ATTORNEY

FILE LOCATION 2FC1 SERIAL NUMBER 10068500 PATENT NUMBER

THE CORRESPONDENCE ADDRESS HAS BEEN CHANGED TO CUSTOMER # 32074

THE PRACTITIONERS OF RECORD HAVE BEEN CHANGED TO CUSTOMER # 32074

THE FEE ADDRESS HAS BEEN CHANGED TO CUSTOMER # 32074

ON 06/28/02 THE ADDRESS OF RECORD FOR CUSTOMER NUMBER 32074 IS:

INTERNATIONAL BUSINESS MACHINES CORPORAT
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION NY 12533

AND THE PRACTITIONERS OF RECORD FOR CUSTOMER NUMBER 32074 ARE:

26665	29894	30238	31316	32440	33086	33787	35791	36678	38252
38253	38371	43199	45008	45554					

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THIS FILE IS ASSIGNED TO GAU 2825.

PTO-FMD
TALBOT-1/97

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number: 10068500

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	18	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	18 minus 20=	* 0
INDEPENDENT CLAIMS	2 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	740

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 16	Minus	** 20	= —
Independent	* 2	Minus	*** 3	= —
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE	—	OR	TOTAL ADDIT. FEE	—

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 8/01) — Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

☆U.S. GPO 2001 482-124 / 59197

CLAIMS ONLY

SERIAL NO.	FILING DATE
10068500	
APPLICANT(S)	

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1	1					
2		1				
3		1				
4		1				
5		1				
6		1				
7		1				
8		1				
9		1				
10	1					
11		1				
12		1				
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TOTAL IND.	2					
TOTAL DEP.	16					
TOTAL CLAIMS	18					

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TOTAL CLAIMS						

* *MAY BE USED FOR ADDITIONAL CLAIMS OR ADMENDMENTS*

FORM PTO-2022 (1-96)

U.S.DEPARTMENT OF COMMERCE
Patent and Trademark Office

*U.S. Government Printing Office: 1998 - 433-214/70303

MPI Family Report (Family Bibliographic and Legal Status)

In the MPI Family report, all publication stages are collapsed into a single record, based on identical application data. The bibliographic information displayed in the collapsed record is taken from the latest publication.

Report Created Date: 2007-03-12

Name of Report:

Number of Families: 1

Comments:

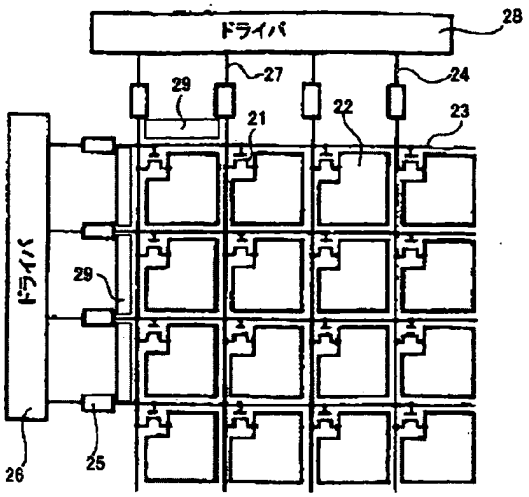
Table of Contents

Family1

4 records in the family, collapsed to 3 records.

JP2002244586A 20020830

(ENG) ARRAY SUBSTRATE FOR DISPLAY DEVICE, MANUFACTURING METHOD FOR THE ARRAY SUBSTRATE, AND DISPLAY DEVICE USING THE SAME SUBSTRATE



Assignee: IBM

Inventor(s): TSUJIMURA TAKATOSHI ; MAKITA ATSUYA ; ARAI TOSHIAKI

Application No: JP 2001029587 A

Filing Date: 20010206

Issue/Publication Date: 20020830

Abstract: (ENG) <sec>PROBLEM TO BE SOLVED: To provide an array substrate for display, the manufacturing method of the array substrate for display and a display device in which the array substrate for display is used.SOLUTION: This substrate is an array substrate for display in which a thin film transistor array which is formed on an insulating substrate 1, plural wirings 23, 24 which are arranged on the insulating substrate 1, connection pads 25, 27 which are arranged at one ends of the wirings 23, 24 and are connected respectively to these wirings 23, 24 and pixel electrodes 22 are included and, moreover, in the substrate, dummy conductive patterns 29 are arranged among end parts of the connection pads 25, 27 and end parts of the pixel electrodes 22.</sec>

Priority Data: JP 2001029587 20010206 A;

IPC (International Class): G09F00930; G02F0011345; G09F00900; H01L0213205; H05B03314; H05B03326

ECLA (European Class): G02F0011333; G02F0011345; H01L02712

Legal Status: There is no Legal Status information available for this patent

TW546788B 20030811

(ENG) Array substrate for display, method of manufacturing array substrate for display and display device using the array substrate

[no drawing available]

Assignee: IBM US

Inventor(s): TSUJIMURA TAKATOSHI JP ; MAKITA ATSUYA JP ; ARAI TOSHIAKI JP

Application No: TW 91101810 A

Filing Date: 20020201

Issue/Publication Date: 20030811

Abstract: Disclosed is to provide an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display. The present invention is an array substrate for display, which includes: a thin film transistor array formed on an insulating substrate 1; a plurality of wirings 23 and 24 arranged on the insulating substrate 1; connection pads 25 and 27 arranged on unilateral ends of the wirings 23 and 24 and respectively connected therewith; and pixel electrodes 22, wherein dummy conductive patterns 29 are arranged between the ends of the connection pads 25 and 27 and ends of the pixel electrodes 22.

Priority Data: JP 2001029587 20010206 A;

IPC (International Class): H01L02184; H01L02100; G02F0011333; G02F0011345

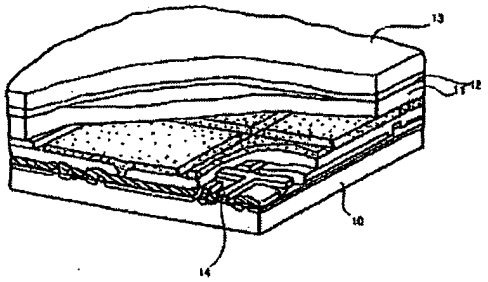
ECLA (European Class): G02F0011333; G02F0011345; H01L02712

Legal Status:

Date	+/-	Code	Description
20031204	(+)	GD4A	ISSUE OF PATENT CERTIFICATE FOR GRANTED INVENTION PATENT

US6689629B2 20040210

US2002106843A1 20020808



(ENG) Array substrate for display, method of manufacturing array substrate for display and display device using the array substrate

Assignee: IBM US

Inventor(s): TSUJIMURA TAKATOSHI JP ; MAKITA ATSUYA JP ; ARAI TOSHIAKI JP

Application No: US 6850002 A

Filing Date: 20020205

Issue/Publication Date: 20040210

Abstract: (ENG) Disclosed is to provide an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display. The present invention is an array substrate for display, which includes: a thin film transistor array formed on an insulating substrate 1; a plurality of wirings 23 and 24 arranged on the insulating substrate 1; connection pads 25 and 27 arranged on unilateral ends of the wirings 23 and 24 and respectively connected therewith; and pixel electrodes 22, wherein dummy conductive patterns 29 are arranged between the ends of the connection pads 25 and 27 and ends of the pixel electrodes 22.

Priority Data: JP 2001029587 20010206 A;

IPC (International Class): H01L02100

ECLA (European Class): G02F0011333; G02F0011345; H01L02712

US Class: 438025; 257072; 257748; 257E27111; 438073; 438149

Agent(s): Townsend Tiffany L.

Examiner Primary: Everhart, Caridad

Assignments Reported to USPTO:

Reel/Frame: 16926/0247 **Date Signed:** 20051208 **Date Recorded:** 20051221

Assignee: AU OPTRONICS CORPORATION NO. 1, LI-HSIN RD. 2, SCIENCE-BASED INDUSTRIAL PARK HSINCHU 300 TAIWAN

Assignor: INTERNATIONAL BUSINESS MACHINES CORPORATION

Corres. Addr: DANIEL R. MCCLURE 100 GALLERIA PARKWAY SUITE 1750 ATLANTA, GA 30339

Brief: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Legal Status:

Date	+/-	Code	Description
20051221		AS	ASSIGNMENT New owner name: AU OPTRONICS CORPORATION, TAIWAN; : ASSIGNMENT OF ASSIGNORS INTEREST;ASSIGNOR:INTERNATIONAL BUSINESS MACHINES CORPORATION;REEL/FRAME:016926/0247; Effective date: 20051208;

USPTO Maintenance Report					
Patent Bibliographic Data			03/12/2007 06:48 PM		
Patent Number:	6689629		Application Number:	10068500	
Issue Date:	02/10/2004		Filing Date:	02/05/2002	
Title:	ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE F				
Status:	4th year fee window opens: 02/12/2007			Entity:	Large
Window Opens:	02/12/2007	Surcharge Date:	08/13/2007	Expiration:	N/A
Fee Amt Due:	$900.00	Surchg Amt Due:	$0.00	Total Amt Due:	$900.00
Fee Code:	1551	MAINTENANCE FEE DUE AT 3.5 YEARS			
Surcharge Fee Code:					
Most recent events (up to 7):		No Maintenance History Found --- End of Maintenance History ---			
Address for fee purposes:	INTERNATIONAL BUSINESS MACHINES CORPORAT DEPT. 18G BLDG. 300-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533				

NOTE: All USPTO fees are subject to change. If you are making a payment by mail or fax, please visit this link or contact the Maintenance Fee Branch (571-272-6500) to confirm the amount due on the date payment is to be made. A maintenance fee payment can be timely made using the certificate of mailing or transmission procedure set forth in 37 CFR 1.8.

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants.	Civil Action No. 06-726 (JJF) Civil Action No. 07-357 (JJF) **CONSOLIDATED CASES**

AMENDED JOINT CLAIM CONSTRUCTION CHARTS

Pursuant to the Court's May 19, 2008 Stipulation and Order Modifying the Scheduling Order (D.I. 208), LG Display Co., Ltd. and LG Display America, Inc. ("LG Display"), Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA, Inc. ("CMO"), and AU Optronics Corporation and AU Optronics Corporation America ("AUO") submit their Joint Claim Construction Charts as follows:

I. Patents asserted by LG Display:

U.S. Patent No. 4,624,737	Exhibit A
U.S. Patent No. 5,019,002	Exhibit B
U.S. Patent No. 5,825,449	Exhibit C
U.S. Patent No. 6,664,569	Exhibit D
U.S. Patent No. 6,803,984	Exhibit E
U.S. Patent No. 5,905,274	Exhibit F
U.S. Patent No. 6,815,321	Exhibit G
U.S. Patent No. 7,176,489	Exhibit H
U.S. Patent No. 7,218,374	Exhibit I

II. Patents asserted by AUO:

U.S. Patent No. 5,748,266	Exhibit J
U.S. Patent No. 6,689,629	Exhibit K
U.S. Patent No. 6,734,944	Exhibit L
U.S. Patent No.6,778,160	Exhibit M
U.S. Patent No. 6,976,781	Exhibit N

U.S. Patent No.7,090,506	Exhibit O
U.S. Patent No. 7,101,069	Exhibit P
U.S. Patent No. 7,125,157	Exhibit Q

III. Patents asserted by CMO:

U.S. Patent No. 5,619,352	Exhibit R
U.S. Patent No. 6,008,786	Exhibit S
U.S. Patent No. 6,013,923	Exhibit T
U.S. Patent No. 6,134,092	Exhibit U
U.S. Patent No. 6,734,926	Exhibit V
U.S. Patent No. 7,280,179	Exhibit W

Each party has listed what it contends is intrinsic evidence to support its contentions. All parties reserve the right to contest whether any such evidence is intrinsic or extrinsic.

August 6, 2008

/s/ Richard D. Kirk

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Attorneys for AU Optronics Corporation and AU Optronics Corporation America

EXHIBIT K

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K
AU OPTRONICS USP 6,689,629

Claim Terms	Des.	Agreed Constructions
connection pads	L	conductive patterns on the substrate that electrically connect the plurality of wiring to circuits located external to the substrate

Disputed Constructions

Claim Terms	Des.	AUO Construction	LGD Construction
a layer of an insulating substrate, having an area	L	plain meaning Intrinsic Support Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 2:13-24, esp. 17-21; 3:11-28, esp. 11-14; 3:29-47, esp. 29-37; 4:33-41; 6:17 34, esp. 23-27, 30-34; claims 1, 9; Figures 1, 5a-5c, 11, 12a-12b; May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 3:37-44, esp. 39-40. Included is the intrinsic support for the disputed term: "area".	material deposited and patterned on a substrate, such as glass, that covers part of the array substrate surface Intrinsic Support 1:7-11; 1:21-2:63; 2:67- 3:6; 3:12-22; 3:26-28; 3:30-51; 3:60-4:23; 4:39-42; 4:55-5:26; 5:29-43; 5:46-6:6; 6:9-47; 6:59-67; 7:5-19; 7:24-27; 7:31-40; 7:50-62; Figs. 2-5, 8, 9, 10; App 10/068,500, 5/29/2003, Office Action, page 2-4.

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K
AU OPTRONICS USP 6,689,629

Claim Terms	Des.	AUO Construction	LGD Construction
area	A	a specified region Intrinsic Support 1:61-67, esp. 63-66; 2:51-62, esp. 51-54; 3:11-28, esp. 18-19; 3:29-47, esp. 38-39; 5:29-42, esp. 29-33, 38-42; 5:43-53; 5:54-60, esp. 54-57; 5:61-6:6, esp. 5:61-6:1, 6:4¬6; 6:35-47, esp. 35-40; claims 1, 9; Japanese Laid Open No. H10-90706, esp. at TR 0003, 0015, 0017, 0020, 0023, 0024, and Figure 5; May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 11:11-14; 11:54-58.	Indefinite or (see above)

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K
AU OPTRONICS USP 6,689,629

Claim Terms	Des.	AUO Construction	LGD Construction
a plurality of wiring arranged on the insulating substrate	L	two or more conductive paths disposed on the insulating substrate Intrinsic Support Abstract; 1:12-20, esp. 14-20; 1:28-30; 1:32-46, esp. 39-44; 2:13-24, esp. 17-21; 3:11-28, esp. 13-24; 3:29-47, esp. 32-47; 4:33-41, esp. 38-41; 5:29-42, esp. 29-33, 38-42; 6:17-34, esp. 23-27, 30-34; 6:35-47, esp. 35-40; claims 1, 2, 10; Figures 1, 3, 4, 5a-5c, 11, 12a-12b; Japanese Laid Open H10-90706, esp. ¶ 0009; Japanese Laid Open H10-240150, esp. ifif 0002, 0003, 0013May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 6:10-20. Included is the intrinsic support for the disputed term: "a layer of an insulating substrate, having an area".	portions of the layer that convey voltages or signals from the connection pads to the thin-film transistors in the pixel array Intrinsic Support 1:8-2:63; 2:66-3:6; 3:14-15; 3:22-29; 3:31-35; 3:42-48; 3:60-4:23; 4:39-42; 4:52-5:28; 5:34-43; 5:55-6:16; 6:24-47; 6:55-7:40; 7:50-62; Abstract; Figs. 2-11; App 10/068,500, 5/29/2003, Office Action, page 2-4.

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K
AU OPTRONICS USP 6,689,629

Claim Terms	Des.	AUO Construction	LGD Construction
dummy conductive patterns	L A	a metal pattern that does not conduct signals or current used in the operation of the display Intrinsic Support Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 1:46-59, esp. 49-54; 2:13-24, esp. 17-21; 3:11-28, esp. 17-22; 3:29-47, esp. 35-41; 3:66-4:2; 5:29-42, esp. 29-33, 38-42; 5:43-53; 6:14-17; 6:37-38; 6:52-55; claims 1, 9; Figures 2-4, 5a-5c. May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 6,163,356 (Song et al.) 7:31-63; 8:27-40; 8:41-67. U.S. Patent No. 5,285,301 (Shirahashi et al.) 6:10-18; 13:30-61, esp. 45-61; claims 3, 4; Figures 1, 14, 15.	portions of the layer that do not receive or convey voltages or signals Intrinsic Support 1:32-67; 2:25-63; 3:3-19; 3:21-29; 3:33-38; 4:34-42; 4:52-55; 5:11-54; 5:64-66; 6:24-38; 6:52-67; 7:15-35; 7:50-63; Abstract; Fig. 2-4.

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K
AU OPTRONICS USP 6,689,629

Claim Terms	Des.	AUO Construction	LGD Construction
dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes	L	dummy conductive patterns cover at least 30% of the region specified by where the dummy conductive patterns are formed; the dummy conductive patterns are situated between the connection pads and the pixel electrodes Intrinsic Support Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 2:13-24, esp. 17-21; 3:11-28, esp. 17-22; 3:29-47, esp. 35-41; 3:66-4:2; 5:29-42, esp. 29-33, 38-42; 5:43-53; 5:54-60, esp. 54-57; 5:61-6:6, esp. 5:61-6:1, 6:4-6; 6:7-17, esp. 9-12, 14-17; 6:17-34, esp. 23-27, 30-34; 6:35-47, esp. 35-40; claims 1, 9; Figures 2-4, 5a-5c. May 29, 2003 Office Action, esp. at 2-3. U.S. Patent No. 6,163,356 (Song et al.) 1:55-64; 7:31-63; 8:27-40; 8:41-67. U.S. Patent No. 5,285,301 (Shirahashi et al.) 6:10-18; 13:30-61, esp. 45-61; claims 3, 4; Figures 1, 14, 15. Included is the intrinsic support for disputed terms: "dummy conductive patterns," "a layer of an insulating substrate, having an area," "area," "pixel electrodes".	approximately 30% or more of the area of the layer is made of dummy conductive patterns that are located between the connection pads and an outer edge of the pixel electrodes in the pixel array Intrinsic Support 1:61-67; 3:3-6; 3:16-20; 3:35-40; 5:30-43; 5:46-6:17; 6:29-48; 7:8-18; 7:50-62; Figs. 2-5, 8, 11; App 10/068,500, 5/29/2003, Office Action.

JOINT CLAIM CONSTRUCTION STATEMENT - EXHIBIT K
AU OPTRONICS USP 6,689,629

Claim Terms	Des.	AUO Construction	LGD Construction
pixel electrode	A	an electrode for applying a driving voltage to a liquid crystal display element in a liquid crystal display Intrinsic Support 1:12-20, esp. 14-20; 4:33-41, esp. 38-41; 4:42-50, esp. 46-48; Figures 1-4; May 29, 2003 Office Action, esp. at 2. U.S. Patent No. 5,285,301 (Shirahashi et al.) 8:36-53, esp. 37-39; 9:48-56; Figure 13. U.S. Patent No. 6,163,356 (Song et al.) 1:61-64.	patterns of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device Intrinsic Support 1:12-21; 4:45-51; 6:48-52; Figs 2-5.
each wiring		each individual wiring in the plurality of wiring Intrinsic Support Abstract; 1:12-20, esp. 14-20; 1:32-46, esp. 39-44; 3:11-28, esp. 14-16; 3:29-47, esp. 33-34; 4:33-41, esp. 38-41; claims 1, 9; Figures 1-4, 5a-5c, 11, 12a-12b; Application for Patent, esp. at 14; May 29, 2003 Office Action, esp. at 2-3; August 29, 2003 Amendment, esp. at 3, 5. Included is the intrinsic support for the disputed term: "a plurality of wiring arranged on the insulating substrate".	Indefinite

CONFIDENTIAL ATTORNEYS EYES ONLY

SUBJECT TO PROTECTIVE ORDER

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG DISPLAY CO., LTD. Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al. Defendants.	Civil Action No. 06-726 (JJF) **CONSOLIDATED CASES**

REBUTTAL EXPERT REPORT OF DR. ARIS K. SILZARS ON VALIDITY OF AUO'S U.S. PATENT NO. 6,689,629

TABLE OF CONTENTS

I. OVERVIEW OF REBUTTAL OPINION

1. If called on as an expert witness in this matter, I anticipate that my testimony may concern the matters addressed below. My anticipated testimony includes my opinion regarding the validity of claims 7, 8, 15, and 16 of U.S. Patent No. 6,689,629 (the '629 patent), attached as Exhibit 1.

2. This report is provided in rebuttal to the expert report of Dr. Gary Rubloff, provided on February 27, 2009 (the "Rubloff report"), regarding his opinion that certain claims of the '629 patent are invalid. Here I address only the asserted claims of the '629 patent, i.e., claims 7, 8, 15, and 16. Should the Court wish to hear testimony regarding the validity of one or more unasserted claims, I reserve the right to address those matters at such time as the Court indicates its preference. I reserve the right to respond to any additional opinions relating to the background of the technology, validity, enforceability, or claim construction provided by any LGD expert.

3. In my opinion, the references relied upon by Dr. Rubloff in his expert report do not render the asserted claims of the '629 patent invalid, either individually or in combination. Specifically, in my opinion, claims 7, 8, 15, and 16 of the '629 patent are neither anticipated, nor rendered obvious, by any of the references relied upon by Dr. Rubloff.

4. In my opinion, Dr. Rubloff's assertions that the claims of the '629 patent are indefinite or not enabled are incorrect. Furthermore, I disagree with Dr. Rubloff's contention that the proper and only construction of the claimed "wiring" of the '629 patent is dual layer wiring.

5. Dr. Rubloff has identified several prior art references and asserts that these references anticipate the asserted claims of the '629 patent and/or render those claims obvious. As discussed

below, these references, alone or in combination, fail to disclose every limitation of the asserted claims.

6. The '629 patent, "Array Substrate for Display, Method of Manufacturing Array Substrate for Display and Display Device Using the Array Substrate," is an important innovation in manufacturing array substrates used in an LCD.

7. In an LCD substrate array, it is desired that the etching process form uniform metallization patterns. One such metallization pattern, wiring, can be formed with a desired, uniform tapered shape using an increased etching rate. '629 patent at 1:47-49. However, in areas where the wiring or metallization density is otherwise low, an increased etching rate can result in "undercut," i.e., where, in a multilayered structure, a lower layer of metallization is etched more or at a faster rate than the upper layer; this can cause circuit defects. '629 patent at 1:61-67, 2:50-63. The prior art discussed how to form the desired tapered shape, but failed to address how to evenly etch the substrate in areas where the metallization density is lowered. '629 patent at 2:1-12. The prior art also discussed how to avoid undercut around connection pads at the edge of the substrate, where the connection pads are located, but failed to address how to prevent "undercut of the signal lines in a region where the wiring density is apt to be lowered," such as between the TFT array and the connection pads. '629 patent at 1:47-67.

8. The invention of the '629 patent solves this problem by adding "dummy" conductive patterns of sufficient quantity and density into the area of the substrate where metallization density is low. '629 patent at 3:12-19. Because the dummy patterns are not needed for the operation of the circuit, they "are not in contact with any of the wiring" for the circuit. '629 patent at 8:18-19.

9. The wires connecting the connection pads to the TFT array are formed by etching one or more metal layers during manufacture of the array substrate. The placement of dummy conductive patterns as prescribed by the '629 patent is specifically to increase the metallization

density in areas of the substrate where the metallization density is otherwise low. '629 patent at 5:29-34. This increased density "reduc[es] concentration of electric current" during the etching process. '629 patent at 6:8-14. It is excessive localized electric current during etching that can cause "undercut" which can lead to defects, such as "an interlayer short circuit." '629 patent at 2:51-64. Thus, increasing the metallization density and reducing the localized electric current helps to avoid such defects.

10. The region of the substrate where the metallization or wiring density is low, and where the dummy conductive patterns are therefore located, are "between the pixel electrodes and the connection pads" in the TFT array. '629 patent at 6:30-34. As illustrated in Figure 2, dummy conductive patterns are located in the areas labeled 29. These areas are situated "between the pixel electrodes 22 and each scan line connection pad 25 and between the pixel electrodes 22 and each signal connection pad 27." '629 patent at 5:29-33 & Figure 2.

II. LEVEL OF ORDINARY SKILL IN THE ART

11. As stated in my report on Infringement of AUO's '266 and '629 Patents by LGD's Accused Products, it is my opinion that a person of ordinary skill in the art at the time of filing of the '629 patent would be a person with (i) at least a Bachelor's degree in chemical or electrical engineering, chemistry, or physics and (ii) having two or more years experience working with liquid crystal display fabrication processing, or the equivalent combined education and work experience.

III. ANALYSIS OF THE PRIOR ART

A. Legal Standards

12. I have been informed that a prior art reference anticipates a patent claim if the prior art reference discloses or includes every element of the patent claim, arranged as described in the claim. I have been informed that if even a single element is missing, the prior art reference does not anticipate the patent claim.

13. I have been informed that an element is inherently disclosed only if the missing descriptive matter is necessarily present in the thing described in the reference and would be so

recognized by persons of ordinary skill. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.

14. I have been informed that a patent claim is obvious if the differences between the prior art and the claim would have been obvious to a person of ordinary skill in the art at the time the patent was filed.

15. I have been informed that it is impermissible to use the claimed invention itself as a blueprint for piecing together elements in the art. In other words, it is impermissible to use hindsight reconstruction to pick and choose among disclosures in the prior art to reconstruct the claimed invention.

16. I have been informed that a reference that "teaches away" cannot render a patent claim obvious. I have also been informed that a reference teaches away if a person of ordinary skill in the art, upon reading the reference, would be led in a different direction from the path taken by the inventor of the patent claim. I have also been informed that a combination that would be inoperative teaches away from the combination.

17. I have been informed that a claim may be found invalid if it is determined that the written description fails to provide sufficient information to enable a person of ordinary skill in the art to practice the invention without undue experimentation. I understand that a patent need not teach, and preferably omits, what is well known in the art. I also understand that resort to material outside of the specification in order to satisfy the enablement requirement is permissible because it makes no sense to encumber the specification of a patent with all the knowledge of the past concerning how to make and use the claimed invention. I further understand that the fact that some experimentation is necessary does not preclude enablement, but that any required experimentation must be reasonable. Some trial and error is permissible. Further, I have been informed that enablement does not require the inventor to foresee every means of implementing an invention. Finally, I am informed that the specification need not necessarily describe how to make and use every possible variant of the claimed invention, for the artisan's knowledge of the prior art and routine experimentation can fill in any gaps, interpolate between embodiments, and even extrapolate beyond the disclosed embodiments.

18. I have been informed that an independent claim should not be interpreted such that it requires a limitation added by a dependent claim. Stated another way, limitations recited in dependent claims are not to be read into the independent claim from which they depend. Thus, a dependent claim must add a limitation to those recited in the independent claim.

19. I have been informed and understand that a term is indefinite if it is insolubly ambiguous. In other words, the definiteness of claim terms depends on whether the terms at issue can be given any reasonable meaning.

B. None of the References Cited by Dr. Rubloff Disclose the Problem or Solution Taught by the Asserted Claims of the '629 Patent.

20. Dr. Rubloff asserts that European Patent Publication No. 887695 (or related U.S. Patent No. 6,373,544) ("EP '695"), U.S. Patent No. 5,850,275 (or related Japanese Laid Open Patent Publication No. H09-211480) ("the "275 patent"), U.S. Patent No. 6,862,069 ("the '069 patent"), Japanese Laid Open Patent Publication No. H09-197415 ("JP '415"), and Japanese Laid Open Patent Publication No. H06-082811 ("JP '811"), attached as Exhibits 2-8, respectively, disclose, alone or in the combinations relied upon by Dr. Rubloff, every element of each of claims 7, 8, 15, and 16 of the '629 patent, as indicated in Exhibits 17, 22, 24, 26, and 28 of his report. I disagree, for the reasons discussed below.

1. <u>EP '695 is Directed to Creating a Uniform Surface for Polishing.</u>

21. In Dr. Rubloff's own words, "EP '695" discloses the use of polishing structures "for achieving a uniform polishing rate without thickening of the interlayer insulation film to be polished." Rubloff report at 20. More specifically, EP '695 relates to substrates for electro-optical devices such as a reflective liquid crystal panel substrate. EP '695 at 1:3-7.

22. In the formation of a reflective liquid crystal panel substrate, the chemical mechanical polishing (CMP) process is essential for subsequent deposition of a pixel electrode with a mirror surface as a reflective electrode on each pixel. EP '695 at 4:11-20. The CMP process uses a slurry (polishing liquid) which simultaneously prompts the chemical and mechanical removal of material. EP '695 at 4:11-20.

23. As each additional layer of material and structure is deposited and formed on the reflective liquid crystal substrate, the surface of the substrate as a whole will not be uniform. Specifically, there will typically be a difference in the thickness of the substrate in the pixel region and the thickness of the substrate in the sealing region as a whole will not be sufficiently flat to allow the CMP process to produce the desired result. EP '695 at 5:36-44. As a result, following the CMP process, the "periphery of the terminal pad 26 and the upper and lower centers of the sealing regions 27 are excessively polished, whereas the right and left centers of the sealing region 27 are insufficiently polished." EP '695 at 5:36-44.

24. "In a first means in the present invention for achieving the first object, in order to flatten the surface level of the unpolished interlayer insulation film as uniformly as possible, a dummy pattern for raising the level of an interlayer insulation film to be polished is formed on the entire exterior of the pixel region by using the previously formed wiring layer, instead of on the space in the pixel region." EP '695 at 9:15-42. That is, the substrate of EP '695 is characterized by a dummy pattern below the interlayer insulation film subjected to CMP polishing provided near at least a terminal pad formed at a non-pixel region on the substrate. EP '695 at 9:15-42.

25. Since the surface level of the interlayer insulation film to be polished is raised near the terminal pad in such a configuration, the surface level is substantially the same as the surface level of the interlayer insulation film to be polished in the pixel region, and thus the overall surface level is made more uniform. EP '695 at 9:43-10:2. The uniform surface, as a result, has a uniform polishing rate during CMP and the polished surface of the interlayer insulation film is flattened more than conventional surfaces. EP '695 at 9:43-10:2. As a result, the pixel region is satisfactorily flattened, control of the cell gap is improved in cell assembly using a counter substrate, and the etching time for the contact holes of the interlayer conductive portion etc., in the pixel region after polishing is easily determined. EP '695 at 9:43-10:2.

26. Dr. Rubloff also cites EP '695 for disclosure of wiring having as its lower layer wiring material of aluminum or aluminum alloy and having as its upper layer wiring material of molybdenum, chromium, tantalum, titanium and alloys thereof. Rubloff report at 26-28. As support, Dr. Rubloff cites "'EP 695, col. 16, ll. 20-22" where a "'quadrilateral structure composed of Ti/TiN/Al/TiN in that order from the bottom.'" Rubloff report at 26-28.

27. From the plain language of EP '695, neither aluminum nor an aluminum alloy is used as the lower layer of this quadrilateral structure; that material is titanium (Ti). In addition, the plain language indicates that none of molybdenum, chromium, tantalum, titanium or an alloy thereof is used as the upper layer wiring material. Instead, the upper layer material of EP '695 is TiN (titanium-nitride). Titanium-nitride is a compound constituted from titanium and nitrogen. It is not an alloy. Titanium-nitride is considered a ceramic and is known for its reflectivity and hardness. As such, in view of the nature of the EP '695 disclosure, TiN was undoubtedly selected as the upper layer of the quadrilateral structure of EP '695 based on its reflective and polishing characteristics.

28. Thus, EP '695 is directed to providing a uniform polishing surface. Most notably, nowhere in EP '695 is there a discussion of the problem of or the solution for "undercutting the wiring structure," which solution Dr. Rubloff asserts is an element of every claim of the '629 patent. Rubloff report at 78. Moreover, there is no discussion in EP '695 regarding selection of an upper layer wiring material such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant as required by the claims here at issue.

2. <u>The '275 Patent is Directed to the Provision of a Light Shield to Resolve Uneven Brightness.</u>

29. In Dr. Rubloff's own words, the "'275 patent addresses [] light leakage problem[s] by inserting light shield areas between terminal groups and outgoing line groups." Rubloff report at 30. Dr. Rubloff concedes that the '275 patent fails to disclose multilayer wiring structures. Rubloff report at 37-41.

30. More specifically, the '275 patent is directed to solving the problem of uneven brightness in a horizontal direction in an area near outgoing lines in a display without using any particular process or materials for light shielding in a liquid crystal display. '275 patent at 2:39-43. To create even brightness in the display, the '275 patent suggests placing strips of opaque material near the connection terminals and terminal wiring. '275 patent at 4:35-39.

31. The width of these light shielding strips is prescribed by the formula: "Width of strip = Width of terminal (or width of outgoing line) x (100 + Light transmittance of TCP [%])/100." '275 patent at 4:39-42. Notably, there is no discussion in the '275 patent regarding how closely to position the strips or a preferred density to be achieved. However, the '275 patent does warn that too

many light shielding patterns or too much light shielding material can cause portions of the nearby wiring to become conductive with the light shielding patterns such that the nearby wiring becomes defective. '275 patent at 50-58.

32. Thus, as with EP '695, the '275 patent fails to mention the problem of, or the solution for, "undercutting the wiring structure," which solution, along with a dual layer wiring structure, Dr. Rubloff asserts is an element of every claim of the '629 patent. Rubloff report at 78-79. Moreover, there is no discussion in the '275 patent regarding selection of an upper layer wiring material such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant as required by the claims here at issue.

3. The '069 Patent is Directed to the Regulation of Cell Gap in the Sealing Region.

33. In Dr. Rubloff's own words, the '069 patent describes patterns to "provide a more uniform cell gap in the liquid crystal display thereby avoiding non-uniform brightness issues." Rubloff report at 41. Dr. Rubloff concedes that the '069 patent fails to disclose multilayer wiring structures. Rubloff report at 48-52.

34. More specifically, the Abstract of the the'069 patent discusses forming patterns between gate links and data links which are coated with sealant such that the patterns between the links obtain the same height as a liquid crystal area to provide a uniform cell gap. According to the '069 patent at 38-41, the patterns are preferably formed to have the same height as the gate or data links and an equal distance from the gate or data links to either side so that the sealant can be coated on the gate link area with a desired height.

35. The '069 patent does not describe including patterns between adjacent sets of connection pads and the pixel electrodes, only between adjacent wires. The '069 patent never mentions a preferred density of the cell gap regulating structures in between the connection pads and the pixel electrodes. This is significant in that a person of ordinary skill in the art reading the '069 patent would be led on a path to include a density of these patterns consistent with the typical density of gap regulating structures, i.e., less than 1% of the overall substrate. At no point does the '069 patent mention the effect these patterns have on the formation of adjacent wiring, which wiring is admittedly single layer wiring. Rubloff report at 48-49.

36. The '069 patent fails to mention the problem of or the solution to "undercutting the wiring structure." Dr. Rubloff asserts that this solution, along with a dual layer wiring structure, is an element of every claim of the '629 patent. Dr. Rubloff's report at 78-79. Moreover, there is no discussion in the '069 patent regarding selection of an upper layer wiring material such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant as required by the claims at issue.

4. JP '415, like the '069 Patent, is Directed to the Regulation of Cell Gap in the Sealing Region.

37. In Dr. Rubloff's own words, "JP '415 addresses issues resulting from the non-uniformity of cell gap." Rubloff report at 53. Dr. Rubloff concedes that the '069 patent fails to disclose multilayer wiring structures. Rubloff report at 59-63.

38. There are considerable similarities between JP '415 and the '069 patent discussed above. However, one difference between JP '415 and the '069 patent is the placement of the gap regulating structures. According to JP '415, the gap regulating structures are not placed between adjacent wires as in the '069 patent, but at the corners of the LCD substrate, "excluding the areas passing said lead parts." JP '415 at [0009]. Thus, JP '415 teaches away from placing gap regulating structures between adjacent sets of connection pads and the pixel electrodes as required by every claim of the '629 patent.

39. The JP '415 fails to mention the problem of or the solution to "undercutting the wiring structure." Dr. Rubloff asserts that this solution, along with a dual layer wiring structure, is an element of every claim of the '629 patent. Rubloff report at 78-79. Moreover, there is no discussion in JP '415 regarding selection of an upper layer wiring material such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant as required by the claims here at issue.

5. JP '811, Like JP '415 and the '069 Patent, is Directed to the Regulation of Cell Gap in the Sealing Region.

40. In Dr. Rubloff's own words, "JP '811 also addresses the issue of cell gap uniformity to achieve a better quality display." Rubloff report at 64.

41. Like the '069 patent, JP '811 discusses placing gap regulating structures between adjacent wiring. JP '811 at [0022], [0025]. Also like the '069 patent, JP '811 fails to specify a density of these gap regulating structures to be formed between adjacent wires. The exaggerated, schematic drawings of JP '811 further fail to provide any teaching as to an ideal or desired density of gap regulating structures. Indeed, in a typical display, the density of gap regulating structures is less than 1% of the overall area of the substrate.

42. The JP '811 fails to mention the problem of or the solution to "undercutting the wiring structure." Dr. Rubloff asserts that this solution, along with a dual layer wiring structure, is an element of every claim of the '629 patent. Rubloff report at 78-79. Moreover, there is no discussion in JP '811 regarding selection of an upper layer wiring material such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant as required by the claims here at issue.

6. The Additional References Relied Upon by Dr. Rubloff Also Fail to Disclose the Required Elements of the Asserted Claims.

43. Dr. Rubloff cites to a number of additional references in his effort to invalidate the asserted claims of the '629 patent. However, none of these references provide the elements missing from Dr. Rubloff's primary references, discussed above.

44. For example, Dr. Rubloff cites U.S. Patent Nos. 5,285,301 and 6,163,356 (respectively, the '301 and '356 patent), attached as Exhibits 9 and 10, respectively. Dr. Rubloff relies on the '356 and '301 patents for their supposed disclosure of information relating to unasserted claims 1 and 9 (. . . the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patter[n]s are not in contact with any of the wiring). Rubloff report at 35-37, 46-48, 57-59, 69-71. Importantly, both the '301 and '356 patent were considered during prosecution of the '629 patent. '629 patent at Cover. The claims of the '629 patent was issued over the disclosures of the '301 and '356 patents. The reasons for this are apparent from their disclosures described below.

45. The '301 patent is directed to the provision of additional gate and data lines within the pixel array. These additional lines are provided with the intention of reducing the incidence of

line breakage at the edges of the pixel array. Such breakages are attributed to the fact that "the outermost scanning line [of the pixel array] is close to the end portion of a photoresist used for masking of anodic oxidation, [and] dirt is likely to adhere to the outermost scanning line when the photoresist is formed. Accordingly, the outermost scanning line is sometimes broken when the anodic oxide film is disposed on the scanning line." '301 patent at 1:40-60.

46. The '356 patent is directed to forming a false gate pad on the insulating layer over at least a portion of the periphery of a desired gate pad. The abstract of the '356 patent states that the false gate pad is intended to prevent etchant used during fabrication from penetrating into the periphery of the gate pad.

47. Dr. Rubloff also cites to JP 2000-47227 (JP '227), attached as Exhibit 11. JP '227, like many of the references relied upon by Dr. Rubloff, is directed to managing cell gap. In JP '227, the area of interest for gap regulating structures is at the corners of the LCD substrate, in the sealing region.

48. Finally, Dr. Rubloff's invalidity arguments also includes a few references to U.S. Patent No. 6,157,430 (the '430 patent), attached as Exhibit 12. Dr. Rubloff relies on the '430 patent for its supposed disclosure of matter relating to both asserted and unasserted claims.

49. The '430 patent describes a method for fabricating thin film transistors. It fails to disclose the use of dummy patterns or increased metallization density. Instead, the '430 patent discusses balancing the chemistry of the etching process to achieve the desired wiring formation.

50. Specifically, the '430 patent suggests, prior to etching the materials chosen to make-up the desired wiring, preparing the etching conditions for favorable etching by reviewing the compositions of phosphoric, acetic, and nitric acid and to form the etching face of the wiring material to a tapered shape. *See, e.g.*, '430 patent at 6:30-34, 8:38-42, 10:47-51, 12:23-27, 13:23-27, 14:27-31, 16:22-26, 18:21-27, 19:57-61. This advanced preparation further allows improved formation of a subsequent layer of film on the wiring. *See, e.g.*, '430 patent at 6:30-34, 8:38-42, 10:47-51, 12:23-27, 13:23-27, 14:27-31, 16:22-26, 18:21-27, 19:57-61.

51. Notably, this subsequent layer of film is chosen not for its solubility, but such that it has sufficient hardness to endure brush cleaning so as not to create short circuits or other defects. This subsequent layer is desirable because of the problems, typically shorts between wiring, that occur when firmly brush cleaning wiring materials made from soft metals such as Aluminum. The problems identified by the '629 patent, including undercut, are nowhere mentioned in the '430 patent.

52. Thus, the '430 patent relies upon modifications of the chemical conditions of the etching process, including the materials selected to form the wiring, to ensure wiring of a desired form is produced as is common when performing material plating or removal. This is distinctly different from the use of increased metallization density to aid in wiring formation. In my opinion, the '430 patent would lead a person of ordinary skill in the art in a different direction from the path recommended by the inventors of the '629 patent. Therefore, based on these teachings, it is my opinion that the '430 patent teaches away from the use of dummy patterns to achieve desired wiring shapes, preferring instead to adjust the chemistry of the process before etching takes place given the knowledge of the materials selected for the desired wiring.

7. Claims 1-6 and 9-14: Not Asserted.

53. I understand that claims 1-6 and 9-14 are not asserted. I have not been asked to analyze or offer an opinion as to the validity of claims 1-6 and 9-14 in view of the references relied upon by Dr. Rubloff.

8. Claims 7, 8, 15 and 16: The prior art does not disclose selecting an upper layer wiring material such that the upper layer wiring does not become insoluble in an acid or alkaline etchant.

54. Claims 7, 8, 15 and 16 include the limitation "wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant."

55. Dr. Rubloff argues that each reference, either alone or in combination, with one or more other references discloses, among the other required claim elements, a wiring structure having the same material for its upper layer material as that recited in the claims. Consequently, according to Dr. Rubloff, such a wiring structure, along with the presence of the other required elements,

would also inherently have the same property of not becoming insoluble in an acid or alkaline etchant. For at least the reasons stated below, I disagree with Dr. Rubloff's conclusions.

56. Dr. Rubloff relies on five primary references in his argument that claims 1-16 of the '629 patent are invalid: "EP '695," "the '275 patent," "the '069 patent," "JP '415," and "JP '811." In his own words, "EP '695" discloses the use of dummy patterns "for achieving a uniform polishing rate without thickening of the interlayer insulation film to be polished" (Dr. Rubloff's report at 20), the "'275 patent addresses [] light leakage problem[s] by inserting light shield areas between terminal groups and outgoing line groups" (Dr. Rubloff's report at 30), "the '069 patent" includes dummy patterns to "provide a more uniform cell gap in the liquid crystal display thereby avoiding non-uniform brightness issues" (Dr. Rubloff's report at 41), "JP '415 addresses issues resulting from the non-uniformity of cell gap" (Dr. Rubloff's report at 53), and "JP '811 also addresses the issue of cell gap uniformity to achieve a better quality display" (Dr. Rubloff's report at 64).

57. In other words, as noted above, not one of the references relied upon by Dr. Rubloff describes problems that can occur during the formation of multilayer wiring in general. Further, not a single reference relied upon by Dr. Rubloff describes the problem of an upper layer of metal in a multilayer wiring structure becoming insoluble during the formation of multilayer wiring. More specifically, not a single reference relied upon by Dr. Rubloff describes the problem of an upper layer of metal in a multilayer wiring structure becoming insoluble during the formation of multilayer wiring when such formation is conducted in an acid or alkaline etchant.

58. Dr. Rubloff has failed to identify a single reference which discloses, teaches or otherwise suggests the problem described by the '629 patent, let alone a reference that solves such a problem in a similar or the same manner. Therefore, Dr. Rubloff, as noted above, relies on the argument that the mere presence of wiring having the same materials as those prescribed by claims 7, 8, 15 and 16, along with dummy patterns designed for an admittedly completely different purpose, would also inherently have the same property of not becoming insoluble in an acid or alkaline etchant.

59. I have been informed that an element is inherently disclosed only if the missing descriptive matter is necessarily present in the thing described in the reference. More specifically, the mere fact that a certain thing may result from a given set of circumstances is not sufficient.

60. As a person of ordinary skill in the art of the '629 patent would readily recognize, the fabrication of array substrates is a complex process involving interactions between numerous components and aspects of the process. For example, the formation of wiring can be and is affected by many factors, including: how many layers of metals are used to form the wiring, the specific materials used for each layer of a multilayered wiring structure, the specific chemical composition of the etchant used to form the wiring, the temperature at which the etching process takes place, the etching method employed, e.g., wet or dry, dipping or spraying, whether the etching process includes agitation, the adhesion between the photoresist and the upper most layer of metallization, metallization density, as well as other factors. This is apparent from the '430 patent relied on by Dr. Rubloff. The '430 patent instructs a person of ordinary skill in the art that in order to create desired wiring patterns it is necessary to balance the chemical processes to be put into place based on the composition of the wiring and chemical composition of the etchants to be employed. In Dr. Rubloff's own words, "it is well known that different materials can provide different benefits as well as drawbacks." Rubloff report at 12. In any event, it is well-recognized that a change in any one of the many process factors will have an effect on the results of the etching or wiring formation process, such as the presence or absence of undercut.

61. Thus, even if we assume, for the sake of argument, that the references in question disclose a combination of elements the same as or similar to those recited in the asserted claims of the '629 patent, it does not necessarily follow that the upper layer wiring material does not become insoluble in an acid or alkaline etchant. The key, as described in the '629 patent, is avoiding the circumstances whereby the etching process enables the electrochemical conditions which can cause the upper layer material in a multilayer wiring structure to become insoluble. Such circumstances, as noted above, can be made to occur or avoided by numerous factors. Thus, while the disclosure of the references relied upon by Dr. Rubloff may result in a wiring top layer of a wiring structure that does not become insoluble in an acid or alkaline etchant, such is not necessarily the result.

62. Indeed I cannot find identification of single reference recognizing the problem identified in the '629 patent. Therefore it is difficult to see how a supposedly inherent characteristic that is not recognized by one of skill in the art could be regarded as part of the knowledge of such a person for purposes of determining obviousness. Furthermore, I understand that a retrospective view of inherency is not a substitute for some teaching or suggestion that supports the selection and use of

the various elements in the particular claimed combination. Indeed, that which may be inherent is not necessarily known, and obviousness by its plain meaning cannot be predicated on what is unknown.

63. For at least the reasons stated above, it is my opinion that the references relied upon by Dr. Rubloff, alone or in combination, fail to disclose an array substrate for display or a method for forming an array substrate for display "wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant" as required by claims 7, 8, 15 and 16.

D. The Claims of the '629 Patent are Definite.

70. In Section G. of his report, Dr. Rubloff asserts that the terms "area," "each wiring," and "the dummy patterns comprising at least about 30% of the area of the insulating substrate" in each of claims 1 and 9 are indefinite as insolubly ambiguous. Rubloff report at 77. For the reasons stated below and in my March 20, 2009 report on infringement of AUO's '266 and '629 patents by LGD's accused products. I disagree.

71. Addressing first Dr. Rubloff's argument that the term "area" is indefinite, I have been informed and understand that a term is indefinite if it is insolubly ambiguous. In other words, the definiteness of claim terms depends on whether the terms at issue can be given any reasonable meaning. The term "area" can easily be given a reasonable meaning. Plainly, the term "area" refers to a specified region. This is the plain meaning of the word "area." Furthermore, as used in the claims and specification of the '629 patent, the term area is expressly used to refer to a specified region. *See, e.g.*, '629 patent at 5:55-61 and claims 1 and 9 (describing area as the specified region where dummy patterns are located). I also note that Dr. Rubloff himself was able to discern the meaning of "area" throughout his report challenging the validity of the '629 patent. In fact, one of the references relied upon by Dr. Rubloff uses the very same term – area – in describing a dummy pattern density. '544 patent at 20:62-21:1.

72. In addition, it is important to note that a person of ordinary skill in the art would know that the portion of the array substrate that is located between the connection pads and the pixel electrodes is small. It typically covers significantly less than 10% of the surface of the substrate. Therefore, a person of ordinary skill in the art would understand that the "area" recited in the claims refers only to the a region where the dummy conductive patterns are placed. For at least these reasons, it is my opinion that the term "area" is not indefinite and the term should be interpreted as proposed by AUO to mean "a specified region."

73. Claim 1 requires "a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array." Thus, "each wiring" quite clearly refers to each wiring of the plurality of wiring. For example, if a plurality of wiring includes two wirings, then each wiring must have a first end and be in communication with at least one transistor in the thin film array. Thus the meaning of each wiring in claim 1 is evident from the plain language of the claim.

74. Claim 9 uses similar language. Specifically, claim 9 requires "each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array." Claim 9 is a method claim that parallels the language of claim 1. On at least this basis, the meaning of "each wiring" is clear and, under no circumstances, insolubly ambiguous.

75. Addressing Dr. Rubloff's assertion that the term "each wiring" in claim 9 is indefinite. I disagree. Considering the intrinsic record of the patent, which I understand to include the claims, specification and prosecution history, a person of ordinary skill in the art would clearly understand that the term "each wiring" in claim 9 refers to each individual wiring in the plurality of wiring. This is clear from the plain meaning of the term "wiring" and a review of claim 1 where language similar to that of claim 9 is used. A review of the prosecution history shows that "each wiring" refers to the individual wiring in the plurality of wiring of the array substrate. For example, original claim 10, which I understand forms a portion of issued claim 9, expressly shows that "each wiring" refers to the wires in the plurality of wiring to be formed on the insulating substrate. '629 patent File History, at 14 of the original application for patent, Claim 10, attached as Exhibit 14. The inadvertent omission of the language "forming a plurality of wiring on the insulating substrate" is evident in the applicants' response to office action dated August 29, 2003. '629 patent File History, Response to Office Action dated 08.29.2003, attached as Exhibit 15.

76. Dr. Rubloff asserts that the term "'the dummy patterns comprising at least about 30% of the area of the insulating substrate'" is insolubly ambiguous "because from the specification one cannot discern what area is taken into account to determine the 30%." Rubloff report at 77. Dr. Rubloff makes this argument in the face of his own assertions that the prior art he cites discloses this very feature. I find Dr. Rubloff's argument to be internally inconsistent and agree with AUO's proposed interpretation of this term.

77. A person of ordinary skill in the art need not turn to the specification to ascertain a reasonable meaning for the claim term "the dummy patterns comprising at least about 30% of the area of the insulating substrate." Claims 1 and 9 each specifically define where the dummy patterns are to be located stating that "the dummy conductive patterns [are] situated between the connection pads and the pixel electrodes such that the dummy patter[n]s are not in contact with any of the wiring." A person of ordinary skill in the art would readily recognize to what region of an LCD array substrate this language refers without having to turn to the specification of the '629 patent. However, should one turn to the specification, there they will find additional description of the region where the dummy patterns are to be located.

78. As discussed above, dummy conductive patterns are used in the '629 patent to eliminate known problems that occur during the etching process in those portions of the insulating substrate where the metallization density is low. The portions of the substrate where the metallization density is low, and where the dummy conductive patterns are therefore located, is "between the pixel electrodes and the connection pads" in the TFT array. '629 patent at 6:30-34. As illustrated in Figure 2, dummy conductive patterns (29) are situated "between the pixel electrodes 22 and each scan line connection pad 25 and between the pixel electrodes 22 and each signal connection pad 27." '629 patent at 5:29-33 & Figure 2. Dummy conductive patterns are formed in regions where the wiring density is low "so that the wiring density including the dummy conductive patterns 29 can be 30% or more on an area of a specified surface." '629 patent at 5:62-6:1.

79. I have been informed that AUO believes the term "dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters [sic] are not in contact with any of the wiring" means "dummy conductive patterns cover at least 30% of the region specified by where the dummy conductive patterns are formed; the dummy conductive patterns are situated between the connection pads and the pixel electrodes." I find this proposed interpretation to be the appropriate interpretation of this claim limitation and well supported by the claims and specification of the '629 patent.

80. Based on at least the above, each of the terms "area," "each wiring," and "the dummy patterns comprising at least about 30% of the area of the insulating substrate" can be given a reasonable meaning. Thus, each of these terms is not insolubly ambiguous and, therefore, not indefinite.

E. The Specification of the '629 Patent Enables the Full Scope of the Claims.

81. In section H. of his report, Dr. Rubloff asserts that a person of ordinary skill in the art, after reading the specification, could not practice the full scope of the claimed invention without undue experimentation. Rubloff report at 78. Specifically, Dr. Rubloff asserts that it is not possible to achieve the feature in claims 1 and 9 of "'dummy patterns comprising at least about 30% of the area of the insulating substrate'" without undue experimentation supposedly "because the written description does not properly describe to one of ordinary skill in the art how to determine the

percentage coverage that solves the problem of undercutting the wiring structure." Rubloff report at 78. I disagree.

82. In Dr. Rubloff's own words, "by the year 2000 the microelectronics processing community was well aware of pattern-dependence in chemical and physical processes. Furthermore, once the phenomenon was known – whether well understood or not from a mechanistic viewpoint – the use of additional dummy structures was a straightforward way to make the patterns more uniform and therefore process results more consistent. Essentially the dummy structures trick the process into a much more uniform pattern so that all features are transformed in largely similar fashion." Rubloff report at 15. In addition, Dr. Rubloff admits that "[t]he concept of pattern density adjustment has also been applied to the manufacturing of LCDs and TFT substrates." Rubloff report at 15. Thus, I find Dr. Rubloff's contention that a person of ordinary skill in the art, after reading the specification, could not practice the full scope of the claimed invention without undue experimentation to be incorrect and inconsistent with his assertions regarding the state of the art.

83. I would note that solving the problem of undercutting the wiring structure is not an express limitation of claims 1 and 9. However, if as Dr. Rubloff asserts, solving the problem of undercutting the wiring structure is a limitation of claims 1 and 9, then none of the references relied upon by Dr. Rubloff are relevant to any of the claims. On that basis alone, every claim of the '629 patent is valid over the art cited by Dr. Rubloff.

84. Assuming, for the sake of argument, that solving the problem of undercutting the wiring structure is a limitation of one or more claims, it is my opinion that the specification of the '629 patents teaches a person of ordinary skill in the art, without undue experimentation, how to use "dummy patterns comprising at least about 30% of the area of the insulating substrate" so as to reduce the occurrence of defects in the formation of the array substrate wiring.

85. First, Dr. Rubloff states that Figures 3 and 4 do not indicate the relative arrangement of the electrode line and the dummy lines. Presumably this is an attempt to suggest that the '629 fails to teach where the dummy patterns should be situated or what it means for the dummy conductive patterns to not be in contact with any of the wiring. Claims 1 and 9 themselves teach where the dummy patterns should be located with respect to the wiring, pixel electrodes and connection pads. In addition, Figure 3, along with its written description, plainly show one example

of the positioning of dummy conductive patterns (29) relative to the wiring (33), connection pads (25) and pixel electrodes (30) – as do Figures 2 and 4. Moreover, a person of ordinary skill in the art can ascertain without additional instruction whether one pattern is in contact with another pattern, be the patterns wiring, dummy conductive patterns, or something else.

86. Dr. Rubloff also asserts that "[t]here is no indication of whether to count some kind of overall area when dummy patterns are made of narrow lines instead of blanket coverage." Rubloff report at 78. The '629 patent states that the dummy conductive patterns can be formed as line-and-space patterns, as shown in Figure 3, or as land pattern completely covering a region where the dummy conductive pattern is formed. '629 patent at 5:43-54. In addition, the '629 patents states that, "as shown in Figure 4, the dummy conductive patterns may have any shape or pattern." '629 patent at 6:14-17. These teachings, in combination with the teachings regarding appropriate dummy conductive pattern placement, readily teach a person of ordinary skill in the art how to determine the percentage coverage of dummy conductive patterns in the specified area, regardless whether the dummy conductive patterns are made from narrow lines or the result of blanket coverage.

87. Dr. Rubloff also asserts that "[t]he description of Figure 8 is also unclear because it does not explain how the taper angle is measured and does not explain how pattern density (area %) is determined." Rubloff report at 78. The assertion that a person of ordinary skill in the art would not know how to measure the taper angle of wiring without undue experimentation to be incorrect. A person of ordinary skill in the art would recognize that the taper angle of wiring refers to the slope of one or more edges the wiring with respect to the substrate as illustrated in Figure 5(c), for example. This taper angle can be readily measured.

88. Regarding Dr. Rubloff's argument that Figure 8 "does not explain how pattern density (area %) is determined" without undue experimentation, such a calculation, as discussed above, is well described in the '629 patent claims, specification, figures and is well known by persons of ordinary skill in the art. Indeed, the "area" in which the dummy conductive patterns are situated is well defined by the figures, specification and claims of the '629 patent. That being the case, making a density (area %) calculation of the area coverage of those dummy patterns is well within the skill set of a person of ordinary skill in the art.

89. Dr. Rubloff's argument that "figures 6, 7, 9, and 10 are unclear if not illegible and the written description fails to provide sufficient specificity when describing how to make the device so that sufficient dummy patterns are present to achieve the tapered structure without resulting in the undercut of the wirings" (Rubloff report at 78) ignores the many other teachings of the '629 patent. Specifically, Figure 8 of the '629 patent, and its related written description, provide the necessary guidance to achieve a desired taper angle in wiring to be formed. In particular, Figure 8 provides the suggested pattern density to achieve a certain taper angle, e.g., a density of 30-35% can yield a wiring taper angle in the range of 50-70°. '629 patent at Fig. 8. Moreover, the written description plainly states that, for certain etching processes, "the taper angle of the wiring obtained by the etching is reduced as the pattern density is increased, and a more gentle taper angle is formed. Therefore, it is understood that the upper conductive material can impart a sufficient selective ration to the etching of the lower conductive material by arranging the dummy conductive patterns." '629 patent at 7:12-18.

90. Regarding Dr. Rubloff's discussion of the legibility of Figures 6, 7, 9, and 10, a person of ordinary skill in the art is knowledgeable about the appearance of wiring having a desired taper angle as well as that having undesirable defects such as undercut. A person of ordinary skill in the art in this field undertakes frequent inspections and tests to ensure that the production lines for which he is responsible are producing wiring of a desired form and that his processes are not generating wiring having undesirable defects, such as undercut. Thus, if dummy patterns were to be added to an existing process, a person of ordinary skill in the art would easily be able to compare the results he was getting before and after the introduction of dummy patterns to determine what effect, if any, the initial dummy conductive pattern design was having on an existing process. Just as easily, such a person could determine, through trial and error or reasonable experimentation, how to modify the location, shape, coverage, etc., of the dummy patterns to optimize the process to achieve the desired wiring formations. Finally, at a minimum, a person of ordinary skill in the art could, through knowledge of the prior art and routine experimentation could fill in any gaps, interpolate between embodiments, and extrapolate beyond the disclosed embodiments taught in the '629 patent.

F. The Wiring of the '629 Patent is Not Limited to Dual Layer Structures.

91. According to section I. of Dr. Rubloff's report, the "wiring" in the claims of the '629 patent should be interpreted to mean a two layer structure or the claims of the '629 are invalid for a

lack of written description. Rubloff report at 78-79. As an initial matter, I understand that claim construction is a legal matter solely within the province of the court, i.e., the judge will decide how the claims of the '629 patent should be interpreted. Furthermore, I understand that all briefs an arguments with respect to the proper interpretation of the terms of the '629 patent are already before and being considered by the court. That being said, I disagree with Dr. Rubloff's assertion.

92. According to Dr. Rubloff, one "other feature that has developed over the years during the manufacture TFT substrates and other semiconductor devices is the formation of what are known as 'dummy pattern.' . . . Dummy patterns generally have a non-electrical function and are provided to assist in the manufacturing process. More specifically, such dummy patterns are used to assure uniformity of all functional structures in the product." Rubloff report at 12-13. Dr. Rubloff also asserts that "it [was] clear by the year 2000 the microelectronics processing community was well aware of pattern-dependence in chemical and physical processes. Furthermore, once the phenomenon was known – whether well understood or not from a mechanistic viewpoint – the use of additional dummy structures was a straightforward way to make the patterns more uniform and therefore process results more uniform." Dr. Rubloff's report at 15. Thus, by Dr. Rubloff's own admission, certain uses of dummy patterns with single layer wiring was known as of the time of filing the application for the '629 patent.

93. Given the undisputed teachings of the '629 patent with respect to dual layer wiring and Dr. Rubloff's own admissions, it is my opinion that the written description of the '629 patent provides sufficient information to enable a person of ordinary skill in the art to practice the invention without undue experimentation, whether using single or multi-layer wiring. For at least the reasons stated above, I disagree that the claims of the '629 patent would be invalid for lack of enablement should the term wiring be interpreted to include single layer wiring.

94. Moreover, I understand that the claims of a patent are not necessarily limited to the specific embodiments it describes. Thus, if the '629 patent were to describe a particular embodiment, that does not mean the claims of the '629 patent are necessarily limited to those specific embodiments or the specific solutions disclosed.

95. Finally, I note that the claims of the '629 patent themselves require a different conclusion. Specifically, claims 1 and 9 are silent as to the number of layers required of the claimed

wiring. However, claims 2-8, which depend directly or indirectly from claims 1, and claims 10-16, which depend, directly or indirectly from claim 9, require wiring having at least a lower layer and an upper layer. Thus, the claims themselves teach that at least the wiring of claims 1 and 9 may be single or multi-layered. I understand that this interpretation is consistent with the rule that limitations stated in dependent claims are not to be read into the independent claim from which they depend.

Executed this 27th day of March, 2009 at San Francisco, California.

By: _____
Dr. Aris K. Silzars

Metalorganic chemical vapor deposition of TiN films for advanced metallization

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Titanium nitride (TiN) films are used extensively in advanced metallization schemes for ultralarge scale integrated applications. In the present experiments, physical properties of thin TiN films deposited using low pressure chemical vapor deposition from tetrakis-dimethyl-amino titanium and ammonia have been investigated. Deposited films were characterized by resistivity, stoichiometry and etch rates. It was found that bulk resistivity correlated to wet etch rates with high resistivity films having higher wet etch rates. High bulk resistivity films were unstable in atmosphere and Auger analysis showed higher relative oxygen content. It is concluded that high resistivity films are low density and thereby susceptible to *ex situ* contamination. Optimized films had bulk resistivity of 250 $\mu\Omega$ cm and wet etch rates comparable to reactively sputtered TiN.

Titanium nitride (TiN) has become an integral part of advanced metallization schemes for many ultralarge scale integrated (ULSI) applications. It is used as a diffusion barrier against junction spiking for Al contacts to Si, as a glue layer between tungsten (W) and intermetal level dielectrics, as well as a means of helping preserve the junction integrity during W chemical vapor deposition (CVD). Conventional physical deposition methods for TiN, such as sputtering, suffer from poor step coverage and the problem is exacerbated for sub-micron high aspect ratio contact/via holes required for ULSI applications. Angular collimation of sputtered atoms has recently been proposed as a means of improving bottom coverage.[1] However, there is no net increase in the flux of sputtered atoms reaching the walls of vertical contacts. Inadequate sidewall coverage in deep structures can lead to reliability problems due to poor functionality as a barrier or nucleation layer.

Deposition from metalorganic precursor offers an attractive route for low temperature deposition of TiN films with adequate feature coverage. Dialkylamino-derivatives of titanium [$Ti(NR_2)_4$] originally synthesized by Bradley[2] have been suggested for this purpose in the past.[3,4] This work presents metalorganic CVD (MOCVD) of TiN using tetrakis-dimethyl-amino titanium (TDMAT) and ammonia.

CVD depositions were carried out in a single-wafer cold-wall reactor. The source gas and ammonia, which was used as a reactive gas, were flowed into the CVD reactor through separate inlets. TDMAT is liquid at room temperature and has a vapor pressure of 1 Torr at 60 °C. Helium was used as a carrier gas to bubble through the TDMAT contained in a steel ampule at 50 °C. TiN films were deposited on Si and SiO_2 substrates. Depositions were performed over temperature and pressure ranges of 200–450 °C and 0.5–30 Torr, respectively. Film resistance and thickness were measured by using four-point probe and step profilometry, respectively. Wet etch rates in 1:1 $NH_4OH:H_2O_2$ at 21 °C were measured using resist masking and step profilometry. Thickness and impurity profiles were obtained from Auger and x-ray photoelectron spectroscopy (XPS) analysis.

The effect of process parameters on the bulk resistivity as well as the wet etch rate are shown in Figs. 1 and 2. Figure 1 shows the variation of resistivity and oxygen content in the films with the ammonia/TDMAT flow ratio at a deposition temperature of 350 °C and pressure of 0.5 Torr. The data shows that films with higher resistivity also have high oxygen content, and furthermore that resistivity and oxygen content decreased at higher ammonia to TDMAT ratios. We have reported previously[5] that the resistivity of the films deposited at lower ammonia to TDMAT ratio continuously increased with time in the atmosphere whereas, at higher ammonia flows, the films exhibited stable resistivity.

The effect of process pressure on the bulk resistivity as well as wet etch rate in 1:1 $NH_4OH:H_2O_2$ solution of TiN films is shown in Fig. 2. The lowest resistivity of 250 $\mu\Omega$ cm was obtained at 25 Torr. Interestingly, resistivity is also more stable for films deposited at higher pressures[5] and these films have the lowest etch rate. Assuming that

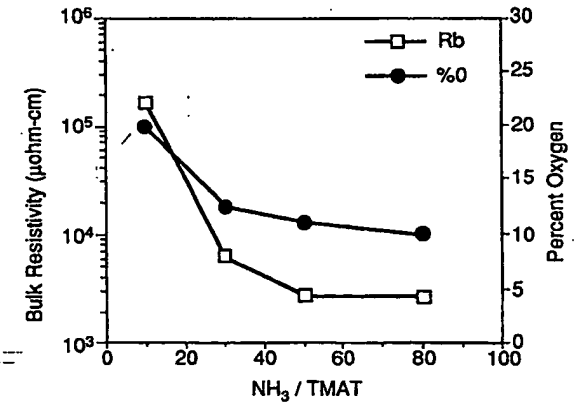

FIG. 1. Bulk resistivity and oxygen content of TiN films for various ammonia to TDMAT flow ratios at a deposition temperature of 350 °C and pressure 0.5 Torr. Oxygen content was determined from Auger analysis.

 0003-6951/93/030240-03$06.00

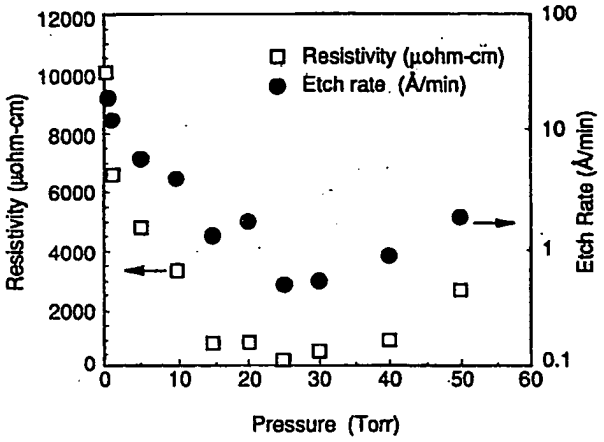

FIG. 2. Bulk resistivity and wet etch rate of TiN films deposited under various process pressures.

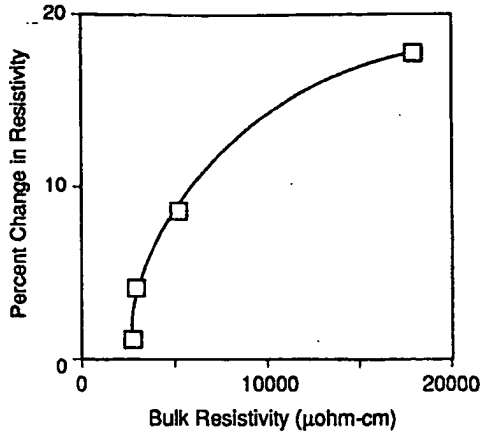

FIG. 4. Percent rise in resistivity after 15 h vs *as*-deposited resistivity of TiN films deposited under various process conditions.

the etch rate depends only on the density of the films, the correlation between the etch rate and bulk resistivity as shown in Fig. 2 indicates that denser films were obtained at higher process pressures. Auger profiles of the films deposited at two different pressures are shown in Figs. 3(a) and 3(b). The film deposited at lower pressure with high resistivity (Fig. 2) showed substantial oxygen incorporation while the optimized low resistivity films deposited at 25 Torr had oxygen levels lower than the detection limit. Thus the relationship between oxygen content and resistivity is similar to that shown in Fig. 1.

Figure 2 shows that wet etch rate rises with the resistivity. In fact, over the entire range of each of the process parameters investigated, higher wet etch rates were associated with high bulk resistivity. Assuming, as noted above, that higher wet etch rates indicate lower density films, it can be surmised that the less dense films are susceptible to *ex situ* oxygen incorporation which in turn causes the rise in resistivity. Figure 4 shows the relative rise of resistivity as a function of the *as*-deposited film resistivity. Clearly, films with lower *as*-deposited resistivity are more stable in atmosphere.

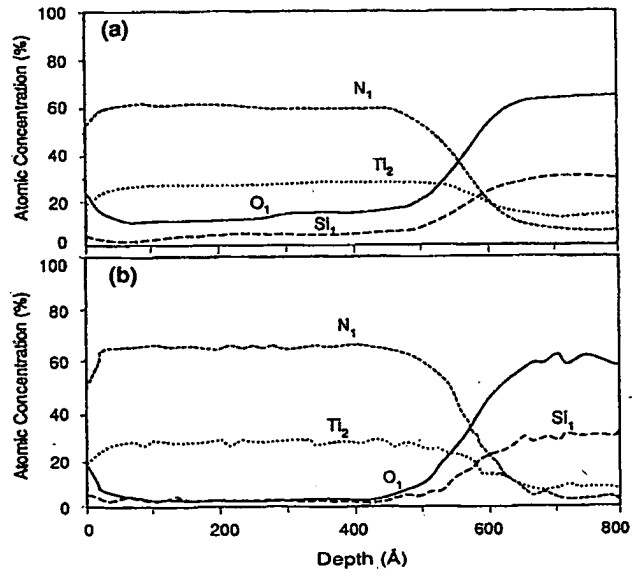

FIG. 3. Auger profiles of TiN films deposited at 300 °C on SiO_2/Si substrate at (a) 0.5 Torr and (b) 20 Torr, respectively.

From the data above, it appears that TiN deposition from TDMAT and ammonia can be divided into two regimes. The first regime comprises process conditions where the films are highly resistive, porous and susceptible to *ex situ* contamination. In the second regime, films are low resistivity, dense and stable in atmosphere. Given that the low resistivity films are produced at high pressures and high ammonia flows, it can be surmised that optimized conditions are those that promote gas phase reactions between ammonia and TDMAT. On the other hand, low TDMAT/ammonia ratios and pressures slow the gas phase reactions and lead to low density film growth. In any case, gas phase reactions are expected to be significant as TDMAT and ammonia react spontaneously at temperatures as low as 40 °C.[5] In the present investigations, deposition rate was almost temperature independent with a low activation energy of 0.02 eV, indicating that substrate thermal energy did not contribute significantly to the reaction.

In conclusion, CVD of TiN films obtained from the reaction between TDMAT and ammonia was studied. The bulk resistivity of deposited TiN films was a function of process temperature, process pressure and ammonia to TDMAT flow ratio. A direct correlation between the wet etch rate and resistivity was observed. Lower resistivity and wet etch rate were obtained at higher deposition temperature, ammonia flow and pressure. Moreover, changes in resistivity of the films monitored over a period of time showed that the high resistivity films were unstable in atmosphere and the stability could be enhanced by depositing denser films at higher ammonia flows as well as process pressures. The presence of oxygen in the films accounted for the high resistivity and it is believed that the oxygen was incorporated *ex situ*.

We would like to thank M. Tuttle for fruitful discussions.

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LG Display Co., Ltd. v.
AU Optronics Corp.

Trial
June 2, 2009

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IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG DISPLAY CO., LTD,) Volume 1
Plaintiff,)
v.)
AU OPTRONICS CORPORATION,)
AU OPTRONICS CORPORATION)
AMERICA, CHI MEI)
OPTOELECTRONICS)
CORPORATION, and CHI MEI)
OPTOELECTRONICS, USA,)
INC.,)
Defendants.)

Tuesday, June 2, 2009
9:00 a.m.
Courtroom 4B
844 King Street
Wilmington, Delaware

BEFORE: THE HONORABLE JOSEPH J. FARNAN, JR.
United States District Court Judge

APPEARANCES:

BAYARD
BY: RICHARD D. KIRK, ESQ.
BY: STEPHEN B. BRAUERMAN, ESQ.
-and-
McKENNA, LONG & ALDRIDGE, LLP
BY: GASPARE J. BONO, ESQ.
BY: CASS W. CHRISTENSON, ESQ.
BY: LORA BRZEZYNSKI, ESQ.
BY: TYLER GOODWYN, ESQ.
Counsel for the Plaintiff

APPEARANCES CONTINUED:

YOUNG, CONAWAY, STARGATT & TAYLOR, LLP
BY: KAREN L. PASCALE, ESQ.
BY: JOHN SHAW, ESQ.
-and-
WILSON, SONSINI, GOODRICH & ROSATI
BY: RON E. SHULMAN, ESQ. ESQ.
BY: JULIE HOLLOWAY, ESQ.
BY: CRAIG TYLER, ESQ.
BY: GREGORY WALLACE, ESQ.
Counsel for the Defendants

THE COURT: All right. Be seated, please. Good morning.

Ready to proceed.

MR. BONO: Good morning, Your Honor.

THE COURT: Good morning. Are you ready to proceed?

MR. BONO: Plaintiffs are ready to proceed, Your Honor.

Two housekeeping matters. We would like to invoke the rule on witnesses so that if any person is going to be a witness in this trial, we ask that they be excluded from the courtroom. We ask that that rule be applied to the entire trial and even though we're splitting up into two weeks that if there is any witness that is going to testify either this week or the second week of trial that they be excluded from these proceedings.

MR. SHULMAN: Your Honor, we have no problem with the sequestration rule, but as Your Honor will recall from the final pretrial conference this is not a single trial, this is two trials.

In fact, we requested that our damages expert testify at the end of the second case and Your Honor said no, we're having two trials. So I agreed the sequestration rule should apply to fact witnesses in this case until they're dismissed. It certainly doesn't apply to experts and doesn't apply to people that are testifying in some other trial.

THE COURT: I'll grant the application for sequestration between the parties in this case. Expert witnesses are excluded.

And I'll ask counsel to enforce the order by instructing fact witnesses who will be testifying in the case between present parties to exit the courtroom and to honor the sequestration.

MR. SHULMAN: So it applies to both trials or one trial?

THE COURT: Well, when I said between the parties that are present now, that's only the two of you, LG and AUO.

MR. SHULMAN: Very well.

MR. BONO: Just so there is no

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connected to the display module and the first flexible printed circuit board and that could be either of the second FPC boards that we identified at this point. Wherein the first flexible printed circuit has a first alignment mark and the second flexible printed circuit board has a second alignment mark overlapped and aligned to the first alignment mark.

And in both cases both of the second FPC we can identify readily alignment marks that are used to position and align the two boards during soldering.

Q: Okay. And you have just been handed an exhibit AUO-P-1499.

Just examine that for a second.

MS. HOLLOWAY: And, Your Honor, we intend to label AUO 332 with the annotations as AUO 1575 and offer that exhibit into evidence.

BY MS. HOLLOWAY:

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MS. HOLLOWAY: Okay. And Your Honor, we offer AUO-P-1499 into evidence.

THE COURT: Admitted.

MS. HOLLOWAY: Okay. Your Honor, we label the annotated photograph AUO 332 as Exhibit AUO 1575. And we would like to offer that into evidence.

THE COURT: It's admitted.

MS. HOLLOWAY: Okay. We're done with this witness for the moment. Pass the witness to LG.

MR. BONO: Your Honor, could we just have a short recess to switch exhibits?

THE COURT: Sure. Just let the clerk know when you're ready.

THE CLERK: All rise.

(Whereupon a short recess was taken.)

THE CLERK: All rise.

THE COURT: All right. Be seated, please.

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MS. HOLLOWAY: Your Honor, I have a couple of exhibits to address before Mr. Tyler begins. I think I misspoke on the record.

I identified the list of overdriving chips that were analyzed by Dr. Silzars as 1533. That's actually AUO 1553.

And in addition, there was a presentation that he spoke about, the overdriving circuit presentation, AUO 1538. We'd like to offer that into evidence.

THE COURT: All right. This will be admitted.

MR. GOODWYN: Good afternoon, Your Honor. Tyler Goodwyn with LG Display.

CROSS-EXAMINATION

BY MR. GOODWYN:

Q: Good afternoon, Dr. Silzars.

A: Good afternoon.

Q: Earlier today, you — there's a large board beside you — I think you identified the accused area for the '629 patent as being the large triangular region that's in blue bounded by the edge of the display, the edge of

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the — I think what you called the wiring or the fan out and the pad.
Is that correct?
A: Yes.
Q: Is that the same area that's described in the '629 patent?
A: The '629 patent describes a plurality of wiring and it describes dummy patterns. There is not a drawing in the '629 patent that corresponds to this overall analysis area that we've indicated.
The '629 patent depicts the structures that are somewhat different in how they're drawn.
Q: The '629 patent, in fact, describes protecting the wirings, which you've identified as the plurality of wiring; is that correct?
A: Yes.
Q: And in fact, the area where the dummy patterns exist in the '629 patent is actually within what you've identified as the plurality of wiring; is that correct?
A: No. I don't believe that's

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correct.
Q: Can I have the '629 patent? I believe it was a deposition, Exhibit 5.
Now, Dr. Silzars, do you recognize what I've put on the screen as Figure 3 from the '629 patent as you have annotated that figure at your deposition?
A: Yes, I do.
Q: And you've identified in Figure 3 four different areas for Claim 1; is that right?
A: Yes.
Q: And the area that you've defined is the area bounded by where the dummy patterns are formed; is that correct?
A: That is correct.
Q: And, in fact, Number 29 is a single dummy pattern; is that right?
A: I believe 29 is identified as a dummy pattern in the patent. Yes.
Q: And the lines or the rectangles 25, those correspond to what you identified as the connection pads?
A: I don't see an identification on that figure, but I could check in the patent.

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Q: Well, number 25, it's turned sideways, but right there just above the large rectangles highlighted in yellow.
A: Yes.
Q: You understand that the rectangle here is designed or intended to designate a connection pad?
A: I will check that to see if that's what the patent says, so we're not making a guess. Yes.
Patent on page — on Column 4, Line 53 says connection pads 25.
Q: And do you understand that these dummy patterns are between the connection pads and the array in this space identified in Figure 3?
A: Well —
Q: There's a connection pad 25, and there are three of them shown in Figure 3; is that correct?
A: Yes.
Q: And then to the left-hand side of Figure 3, designated by number 30 is the array; is that correct?

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A: I believe so, but let me check that in the patent. Thirty is identified an end of an pixel electrode.
Q: So if that were the end of the pixel electrode, would the area between what's been designated as 30 and what's been designated as 25 be the area between the connection pads and the pixel array?
A: I think — I think any of the space that is occupied between a connection pad and the array is where the dummy patterns are located. And I think that would be consistent with what I've shown here.
Q: My question was: Is the region between what's been designated as number 30, and there's a pattern on the left-hand side of Figure 3, and the three rectangles, the top one being designated 25, is the region between them an area between the connection pads and the array?
A: What I would identify would be if we were to draw a vertical line that goes up the edge of 30, you would have to draw a vertical line that goes up the left — left side of 25 or

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anywhere along 25. Then that would be where I would consider between that entire —

Q: Okay.

A: Entire section going top to bottom.

Q: This whole area?

A: All the way to the top and all the way to the bottom.

Q: Okay. Now, you identified the pattern or whatever it is, it's designated as 29, as an area. And that's also what you identified as a dummy pattern; is that right?

A: That's right.

Q: So you define, as explained in the patent, that, in your opinion, the area is defined as where the dummy patterns are located; is that right?

A: Yes.

Q: And I believe you also explained at your deposition that the — you only needed to have one of the areas identified in Figure 3 to have a density greater than 30 percent to meet the Claim 1 limitations; is that right?

A: Yes.

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Q: So that if the — if three of the areas, for example, were at 10 percent and one of the areas was at 50 percent, in your opinion, that would meet the limitations of Claim 1; is that right?

A: I think the question that we have to sort of deal with here is somewhat artificial, because if we're just constructing a hypothetical structure, then that may or may not be adequate.

It's — there's a purpose to doing this. And it's not just arbitrarily creating areas and then deciding whether they meet the claim elements or not.

I think if the — if the area that is about 30 percent is germane to what the claim says of the patent, then that may be perfectly adequate. I think the claim needs to be read in context, not to take out an element, and I think basically try to misrepresent it.

Q: Let me refer you to your deposition testimony. And you — I believe it was May 1st of this year.

I asked you a question with

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respect to this figure: "Must all of the areas exceed 30 percent individually?"

Your answer was: "I don't know. I believe that Claim 1 requires that."

Then I asked: "Must all of them exceed 30 percent collectively?

And your answer was: "I don't believe Claim 1 requires it, either."

"Question: It only requires one of them to meet the 30-percent requirement?"

Your answer: "Yes."

A: And I stand by that testimony.

Q: Now, if I could ask you to look at Claim 1 of the patent. Claim 1 says dummy conductive patterns.

Do you believe that dummy conductive patterns means more than one pattern?

A: It's — the word is plural, so I would expect it to mean more than one. Yes.

Q: In fact, it says —

A: I can't think of a case where there would only be one.

Q: Okay.

A: So in all other cases we looked

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at, there are many.

Q: Well, it says the dummy conductive patterns comprising at least 30 percent of the area. You said one pattern could be the entire area.

Is that correct?

A: In the language of the claim, I think we need them to be in plural.

Q: So what you had highlighted in Figure 1 during your deposition then was incorrect; is that —

A: I did not say in my deposition about one dummy pattern.

Q: No. The claim calls 29 a pattern; 29, the entire region is a pattern.

A: Consisting of many dummy patterns.

Q: Oh, let's look at what the patent says.

If I understand correctly, and I'll try to find it for you, Dr. Silzars, the patent refers to pattern 29 as potentially a single pattern as being made up of line and space patterns. So it's still one pattern that has the dashes.

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So 29 is one pattern.
A: If I look in Column 6, it says the dummy conductive patterns plural 29.
Q: Okay. Well, if we look in Column 5, it says Figure 3 is an enlarged view showing a portion where the dummy conductive pattern 29 is formed in the embodiment of the array substrate 10 for display of the present invention shown in Figure 2.
For the record, that begins around Line 43. Then it says Figure 3 shows the dummy conductive pattern 29 formed as a line and space pattern between the connection pad 25 and the end 30. So what's been identified as a line of space pattern is a single pattern, and therefore, the area of Claim 1 needs to include more than just that dummy pattern, doesn't it?
A: Well, I think we're not talking so much technical terminology as interpretation of English language right now. Because if you — if I use your current interpretation strictly, then I don't know what I would call one pattern. If I have a — we have seen on some of our GDS files where a single, we might call a line is

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referred to as a dummy pattern. And if it has to be one or more lines, I think all of that is a dummy pattern. A dummy pattern, it does not specify how many lines it has to have. It could be one line.
Q: But the claim also refers to an area, and the area includes more than one pattern. And the area would not be bound by a single pattern, but would include more than a single pattern, wouldn't it?
A: This is where I think we're having a semantics argument rather than a technical argument. Because that would from a technical standpoint make no sense whatsoever.
Q: Well, if I could look at Figure 4 from the same deposition exhibit. And perhaps it doesn't make sense, Dr. Silzars, but here you've identified six different areas; is that correct, in Figure 4, during your deposition?
A: I'm not sure what you're pointing to when you say six different areas.
Q: You have area of Claim 1 (1), area of Claim 1 (2), area of Claim 1 (3), area of Claim 1 (4), and I apologize, it's actually

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five, five different areas.
A: Yes.
Q: And you have outlined them in red?
A: Yes.
Q: And you have outlined them based on where you found dummy patterns?
A: That's correct.
Q: And in your opinion, you could take any one of those patterns and randomly subdivide it, couldn't you?
A: I don't think I said randomly. I said if it's a regular pattern and it repeats itself, and the lines and spaces are the same, then we could subdivide it and get the same result. That's different than saying randomly subdivided.
Q: Again, at your deposition do you recall me asking you whether or not any of those areas could be subdivided, your answer was — I'm sorry, this was page 182, beginning on line three:
"Could any of those areas be subdivided?
"ANSWER: Yes, I believe they

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could.
"QUESTION: How would you determine how you could subdivide them into different areas?
"ANSWER: Given this particular drawing and this particular configuration, if we simply want to subdivide them, I could almost do it randomly because this pattern is quite even, so given that I have drawn — identified the area being the periphery of these dummy patterns, I could begin to subdivide them without changing the percentage of coverage so in this case the subdivision would not affect the outcome."
A: I think it's correct because you absolutely must read the entire quote rather than take out only the word randomly. I very specifically said that it's a regular pattern, that it's a repeating pattern. And if it's a regular and repeating pattern, then one can subdivide.
Q: And you could subdivide if it was a regular and repeating pattern, you could then subdivide the pattern randomly?

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A: You could choose the area where you pick as long as you encompass enough area to make it sensible to do a calculation of the percentage of coverage. And that would be two or more lines. If you select one line, that's not going to be sufficient to do an area of calculation, but if I select — if the pattern repeats, if it's a regular pattern of nice uniform lines, then I can take three or four of them and I can get a percentage calculation of the area that's being covered by the metal.

Q: Well, the patent doesn't talk about protecting just one or two lines, does it, it talks about protecting all the lines?

A: I was now telling you what could be done with a regular pattern. And I think beyond that, then we should look at the claim and interpret the claim terms properly.

Q: Well, you've defined area by where you find a pattern as opposed to defining the area first and then determining whether or not that area contains dummy patterns that comprise 30 percent of the total area, haven't I?

A: In the particular example that was

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shown in the patent, that was the appropriate selection to make, because it specifically tells us in the patent where we should look.

I did not invent those areas. I took the areas that were identified by the inventors and I simply pointed out to you that that's the area of the dummy patterns.

Q: The patent describes these as dummy patterns. The patent does not say that's an area, does it?

A: It has to be the area that pertains to the dummy patterns. It can't be any area we choose because then the patent makes no sense whatsoever.

Q: Doesn't the patent define the area as — in the claim as being between the pads and the array?

A: Yes, it does.

Q: And then it simply says that the dummy patterns need to comprise 30 percent of the space between the dummy pads and the array?

A: The claim element that I believe to which you are right now referring says dummy conductive patterns, the dummy patterns

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comprising at least about 30 percent of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patterns are not in contact with any of the wiring. That's the entire claim language that I think is pertinent here.

Q: You're interpreting the dummy patterns and the area to be coextensive, to be the same?

A: Yes.

Q: Would you agree that there is no specific teaching in the '629 patent that explains that the dummy patterns and the area of Claim 1 should be coextensive?

A: I believe if we look at the figures, using the figures that you've just had up there, and if we look at these figures, if the area were taken as some arbitrary area much larger than the area where the dummy patterns exist, then the 30 percent area that's taught by the patent would clearly not be met.

So it would be an obvious incorrect interpretation of the inventor's

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intentions if we take a figure that very clearly shows the intent that the 30 percent coverage needs to be in the area where the patterns are and assign an arbitrarily larger area and thereby not be in keeping with what the patent is teaching.

Q: The patent teaches how to protect all of the wires; isn't that correct?

A: It is specifically teaching how to protect the wiring, yes.

Q: You mentioned earlier during your direct testimony that the important area was the — essentially the last line of the fan out, the outer most wire, or the outer most one or two wires, I'm interpreting from your comments just a moment or two ago. Is that correct?

A: The outer most wiring plural, not just one or two. It may be easily ten or twenty as you can see on here. The wiring is very dense and the fact could extend well into that area so it would not be just one or two, it could easily be in the tens or twenties, we're talking about lots of wiring there in a very short distance.

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Q: You're coming to that conclusion not based on your review of the patent but based on your review of LGD's accused display products, aren't you?
A: No, I'm coming to that conclusion based on an understanding of etching processes.
Q: Can you show me in the patent where it describes that the outer most wires are the most important?
A: That — I may be able to show you if I search through the patent, but that is a conclusion based on an understanding of how this process will work, not that it is particularly — we do not have this particular configuration shown in the patent because it didn't exist at the time.
Q: Because the patent was disclosing wires where the density was not as high as in the accused products and they showed — the patent showed providing dummy patterns between each and every wire?
A: That may be one example, but it's not an exclusive example.
Q: That's the only example provided,

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isn't it?
A: I don't see that for — in Figure 4. I see dummy patterns all grouped together, not between wires.
Q: Well, you understand that not all of the pads are shown in Figure 4; right, all the connection pads? It's just a portion of the connection pads.
A: I do understand that. Yes.
Q: But between each and every connection pad shown and the area bounded by the connection pads and the array between each and every gate wire, if that's what's shown in Figure 4, they're dummy patterns; is that right?
A: What I see in Figure 4 are two classes, in effect, of dummy patterns. They are the ones that we identified to the right that we had that are the regular lines. And then we have some in Figure 4 to the left that come down and then seem to either terminate, or you — yeah. I can't tell if they terminate or not at that point or if they go on — go on up.
Q: Okay.
A: But it's — I don't believe that

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from Figure 4 I could draw the conclusion that there is a line between every — every wiring. A dummy pattern.
Q: Well, let's look at Figure 3 from the '629 patent. Again, we have the pads that are numbered 25.
A: That's still Figure 4.
Q: I'm sorry. I meant to have Figure 3.
Thank you, Dr. Silzars. All right.
Figure 3, we have three and perhaps the top part of another pad or connection pad shown. We have a dummy pattern numbered 29 and then three more dummy patterns.
And if the line — assuming they are — gate lines are 33, would you agree that each of what appear to be gate lines in Figure 3 has a dummy pattern between that and the adjacent gate line?
A: I am checking to see exactly what the patent says is 33. If you spot it first and can point me to it, I would appreciate that as well.

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Q: I seem to be having the same trouble you're having, Dr. Silzars. And we have looked at it with respect to Figure 4.
A: Oh, I see way at the bottom of Column 6 it says — well, near the bottom line, 56, it says Figure 6 is an electron microscope shape of the wiring 33 shown in Figure 3, which was obtained.
Now, unfortunately that doesn't tell us what specifically we have other than the wiring. So I presume if this is actually wiring, this would be — the gate would be the connection to the gate.
Q: So if we assume — if we go back to Figure 3, please.
A: It may — it may not be only the gate wiring, but at least it's the examples we have used for wiring are the gate wiring. So I think with that qualification, that the inventors may not have been that specific. But in terms of saying that it's gate wiring.
Q: Well, and I believe we discussed at your deposition that the wirings could potentially be the gate or the source; is that

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right?
A: Yes.
Q: Okay. But if we were to assume that 33 represents the gate wiring, would you agree that there is a conductive pattern, a dummy conductive pattern between each adjacent gate line?
A: What — what we can't quite see here is that, as we've seen in the actual construction, there's this very, very large fan out where the patterns are coming in and then they spread toward the TFT.
I — you know, this is an earlier invention. The density of the pixels was not so great.
I would not be able to tell you, just looking at this drawing, what the other lines are that are in the vicinity of 33 that are going horizontally, whether those are also active wiring or whether they are not.
Q: Well, if they were active wiring, wouldn't you expect them to be more than one pad, one connection pad? Wouldn't you expect one connection pad to be associated with one

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gate line?
A: That is generally what we would expect. But, also, I have to look there and say that then why is 33 not connecting to the gate pad? If it's as simple as saying it's just a pad, why didn't they, the inventors, draw the line all the way up there and go ahead and connect it?
So I — I don't think there's a big problem in interpretation, but it's just not clear from the figure right now exactly what — how we should interpret that.
Q: The patent figure is unclear?
A: Pardon?
Q: The patent figure is unclear?
A: Well, from that specific element, only from the element of saying you — I mean, it says 33 is wiring. And you're asking me to add the additional interpretation should that be associated with that singular pad. And I don't know that the patent says that.
So for that particular aspect, I can't tell you just by looking at that figure.
Q: Okay. Now, in this figure, would

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you expect the dummy pattern numbered 29 to have an impact on the etching of the wire 20 gate lines away?
A: Are you asking me to assume that the other dummy patterns don't exist?
Q: No, with all the other dummy patterns. Assuming — assume that that pattern continues for all of the gate lines.
A: Yes.
Q: Would the top most, what you've identified as area of Claim 1, that has been highlighted with item number 29, would that dummy pattern impact the etching of a gate line 20 lines away?
A: Twenty lines being off the bottom of the screen?
Q: Yes.
A: There's clearly some distance at which there will not be an impact. That if we place — if you have two metallization patterns that are separated by a large distance, compared to any of the size of the structures, then, indeed, there may not be any relationship.
Q: In fact, it depends on the density

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of the entire area where the wires and dummy patterns are, doesn't it?
A: That is right. In general it always depends on the density of the wires, the amount of coverage, what's in the vicinity. So in general, that answer is yes.
Q: Now, do you understand that AUO has proposed a construction for area to be a specified region?
A: I think I would need to verify that, but I don't have a reason to doubt that, as I sit here.
Q: Okay. Would you agree that a specified region doesn't provide any guidance as to determining the bounds of the area?
A: Well, I think if it's taken in the context of an application, then it has considerable meaning and can be precisely identified as I have already tried to do.
Q: Well, the way you've done it is to make the area and the dummy patterns co-extensive. So you've essentially defined a specified region to be the region where the dummy patterns are located, provided they're

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between the connection pads and the array?
A: And that's based — I base my interpretation on the teaching of the patent, and the figures and what the patent says as that being the only correct interpretation.
Q: Well, I believe you also testified earlier that in the accused product that's on the board, where there are these large wide patterns in the demonstrative — and I apologize. I don't remember what the exhibit number was for that.
The area that you identified as region of dummy patterns. You acknowledged that those patterns, those actually carried different voltages and signals during the operation of the display; is that right?
A: Some of them are connected, others are not.
Q: Well, when you say some of them are connected, connected to what?
A: I found some that are connected to ground. I found some that are connected to voltages. And I found some that are not connected.

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Q: Dr. Silzars, earlier you had a panel that you had shown to show what a glass panel is, but you had removed all the driving circuitry; is that right?
A: That's correct.
Q: But the way the signals get on to a display such as this one, they would come in through driving circuitry, in fact, you're probably familiar with the TCONS and in through the driving boards, but this has to provide — since there is only connections on one side, this has to provide the connections for both the source drivers and the gate drivers, doesn't it?
A: Yes, it does.
Q: In fact, the gate drivers are over here on this little piece of film over here; right?
A: Yes.
Q: And these are integrated circuits?
A: Yes.
Q: And integrated circuits actually require voltages to operate, don't they?
A: They do.
Q: They need something like Vcc to provide a reference voltage?
A: That's correct.
Q: And they need ground to also provide a reference voltage?
A: They do.

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MR. GOODWYN: May I approach, Your Honor?
THE COURT: Yes, you may.
BY MR. GOODWYN:
Q: We have another demonstrative that I believe is the same product, if not, pretty close. I hope I don't break this.
MR. SHULMAN: That was an expensive exhibit.
MR. GOODWYN: I definitely hope I don't break it.
BY MR. GOODWYN:

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Now, I believe this is one of the products that you've accused of infringing the '629 patent?

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A: Well, I think you're reading of that file number, which is not possible from memory or otherwise to relate, makes it essentially impossible to relate it to anything as I sit here.

Certainly we created a demonstrative and I analyzed all of the GDS files that went into that creation, so I'm comfortable in providing an opinion on that.

But the GDS file as you know is a multilayer document that contains many different kinds of information. And you're asking me to accept a layer or a portion of a layer that has some notations on it without the ability to analyze the rest of the GDS file, and to look at how it is in context and to provide an opinion, and I don't believe I can do that.

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MS. HOLLOWAY: Objection, Your Honor. If he wants to question him on someone's testimony, he can put it in front of him.

BY MR. GOODWYN:

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Q: Right. In fact, all of those signals are necessary for the operation of the display?

A: Yes, they are.

Q: Now, I'll put on here another chart for you. What I've put up on the screen, Dr. Silzars, is a portion from the joint claim construction statement that was filed in this case. And it provides the claim term or one of the claim terms for the '629 patent, and that's dummy conductive patterns.

And it has both AUO's proposed construction and LG Display's proposed construction. AUO's proposed construction for dummy conductive patterns is a metal pattern that does not conduct signals or current used in the operation of the display.

Is that right?

A: That is what I read there.

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Q: And LG Display's proposed construction is portions of the layer that do not receive or convey voltages or signals.

Is that correct?

A: Yes.

Q: And would you agree that there's at least some matching between those constructions? That AUO and LG Display both agree that a dummy conductive pattern does not carry a signal during the operation of the display?

A: Well, what I look at in analyzing this is that the patent is very clear on what is meant by wiring. And the wiring is the connection to the TFT array as I explained earlier in my direct testimony.

And the patent explains that other conductive patterns that are not the wiring are the dummy patterns. So I believe in that sense they — the AUO construction may be too constrictive.

Q: Well, my question was simple. AUO's and LG Display's proposed construction at least agree in the context of they both exclude

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dummy conductive patterns from carrying signals during operation of the display; is that correct?

A: That is a construction as I see on the — on the projector.

Q: The main difference perhaps is that LG Display's construction also would exclude signals during testing prior to operation of the display; is that right?

A: I am not sure how you're distinguishing testing from operation.

Q: Well, would you consider an operation or testing of the display before the display is completed, the manufacturing to be operation of the display?

A: You mean testing without being able to put any kind of an image on?

Q: Perhaps.

A: Just resistive components? I think that could be a distinction that could be made between the two constructions. Yes.

Q: Okay. Now, Dr. Silzars, you filed a declaration in this case, didn't you, during claim construction?

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A: I believe I did. Yes.
Q: Is that your declaration?
A: That looks like the first page of it, yes.
Q: Is that your signature?
A: Yes, it is.
Q: Let's look at what you said in your declaration about dummy conductive patterns during the claim construction process. The first in Paragraph 10 you said, dummy conductive patterns in question are referred to as "dummy" conductive patterns because they perform no function in the operation of the display. Is that right?
A: Yes.
Q: Was that your position at the time you signed this declaration?
A: That was my position at that time.
Q: Okay. And Paragraph 12, you say it again, The dummy conductive patterns perform no function in the operation of the display. In fact, for this reason, according to the claim language, a dummy conductive pattern is not connected to any of the wiring that is used to

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convey signals between the transistor array and the system.
And then in 15, Second, the dummy conductive patterns are not connected to any of the wiring that communicate with the TFT or other components used to operate the display.
Is that right?
A: In the first quote, Line 12, it specifically says not connected to any of the wiring that is used to convey signals between the transistor array and the system. That is consistent with my position today.
Q: And in 15 — well, in 15, you say communicate with the wiring or other component used to operate the display. You would agree, wouldn't you, that the driver chips are components used to operate the display?
A: Yes, I would.
Q: And wouldn't you agree that all of what you called dummy patterns that line on glass patterns are used to drive and are connected to the driver chip for the operation of the display?
A: And in — I think in further

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review of the patent language since I made that declaration, it is my opinion that the patent is very clear and did not require that additional interpretation —
Q: Based on your —
A: — that the dummy pattern —
Q: Excuse me.
A: Excuse me. That the plurality of wiring very clearly states that it communicates with the transistors in the thin film array and that other patterns are intended to be the conductive dummy patterns.
And that the structure, I think, also could — to go back to what is intending in using this structure, that this structure is used to create a wiring pattern that is uniform and does not have defects in it. And that the wiring structure is what guides the design of these patterns, and that they can incidentally be used for other functions later.
Q: Let's look back at your declaration again. In Paragraph 8, you say, The facts stated herein are based on my expert knowledge and my review of U.S. Patent Number

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6,689,629.
You reviewed the patent before signing this declaration, didn't you?
A: I sure did.
Q: And you said that the dummy conductive patterns in question referred to dummy patterns because they perform no function in the operation of the display. That's a clear statement, is it not?
A: Yes, it is.
Q: When did you first start reviewing the mask files of LG Display?
A: I do not have a specific date that I can give you.
Q: Was it before or after you signed this declaration?
A: I don't know.
Q: When did you first learn that the patterns that you have accused of being dummy patterns carry signals?
A: It would have been during the time when I was reviewing the GDS files.
Q: Did you know that those patterns carried signals before you reviewed the

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LIST OF REFERENCES CITED IN THE REQUEST

(use as many sheets as necessary)

Sheet 1 of 1

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Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	BA	EP 0 887 695 A2	12-30-1998	Seiko Epson Corporation		
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the application number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

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Examiner Signature		Date Considered	

DC:50680289.1

APPENDIX CC1

U.S. PATENT NO. 6, 689, 629 - HIRABAYASHI

As detailed below European Patent Application 0887695 to Hirabayashi discloses each and every element of claims 1-5, 7-13, and 15-16.

CLAIM 1	PRIOR ART DISCLOSURE – HIRABAYASHI
An array substrate for display, comprising:	Hirabayashi discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1.
a layer of an insulating substrate, having an area;	Hirabayashi discloses that in the liquid crystal panel substrate the switching elements may be fabricated on the main surface of an insulating substrate, such as a glass substrate. *See e.g.*, Hirabayashi, col. 31, ll. 16-20. The insulating substrate of Hirabayashi includes various areas that can meet this limitation, including for example, the dummy sealing region or a portion thereof, the pad region or portion thereof, the peripheral circuit region or a portion thereof, or any combination of these areas. *See e.g.*, Hirabayashi, Figs. 1 and 4-6.
a thin film transistor array formed on the insulating substrate;	Hirabayashi discloses forming switching elements, for example thin film transistor, on the substrate. *See e.g.*, Hirabayashi,, col. 31, ll. 16-23.
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Hirabayashi discloses a plurality of wiring, where each wiring is in communication with at least one of the transistors in the thin film array in order for the display device to function. *See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin.
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Hirabayashi discloses connection or terminal pads that connect to the opposite end of the plurality of wirings. *See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18.
pixel electrodes, and	Hirabayashi discloses a pixel region. *See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7.
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the	Hirabayashi discloses dummy patterns that are located between the connection pads and the pixel electrodes and are not in contact with any of the wirings. *See e.g.*, Hirabayashi, Figs. 1, 4-6, shown in hatch pattern; col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54. The dummy conductive patterns comprise well over 30% of various selected areas.

wiring.	
CLAIM 2	
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.	Hirabayashi discloses that the wiring can comprise a multilayer structure of Ti/TiN/Al/TiN in that order from the bottom. *See e.g.*, Hirabayashi, col. 16, ll. 19-22.
CLAIM 3	
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.	Hirabayashi discloses that the wiring can comprise a multilayer of Ti/TiN/Al/TiN. Focusing on two of the layers, Hirabayashi teaches of a lower layer of Al and an upper layer of TiN. *See e.g.*, Hirabayashi, col. 16, ll. 19-22.
CLAIM 4	
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Hirabayashi discloses that the wiring can comprise a multilayer of Ti/TiN/Al/TiN. Focusing on two of the layers, Hirabayashi teaches of a lower layer of Al and an upper layer of TiN. *See e.g.*, Hirabayashi, col. 16, ll. 19-22.
CLAIM 5	
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Hirabayashi discloses that the wiring can comprise a multilayer of Ti/TiN/Al/TiN. Focusing on two of the layers, Hirabayashi teaches of a lower layer of Al and an upper layer of TiN. *See e.g.*, Hirabayashi, col. 16, ll. 19-22.
CLAIM 7	
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Hirabayashi discloses that the wiring can comprise a multilayer of Ti/TiN/Al/TiN. The upper layer of TiN would inherently meet this limitation. *See e.g.*, Hirabayashi, col. 16, ll. 19-22; see also Ex. N at 240-241.
CLAIM 8	
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Hirabayashi discloses that the wiring can comprise a multilayer of Ti/TiN/Al/TiN. The upper layer of TiN would inherently meet this limitation. *See e.g.*, Hirabayashi, col. 16, ll. 19-22; see also Ex. N at 240-241.
CLAIM 9	
A meted for forming an array substrate for display, comprising:	Hirabayashi discloses an array substrate for a liquid crystal display and method of forming an array

	substrate. *See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1.
forming a layer of an insulating substrate, having an area;	Hirabayashi discloses that in the liquid crystal panel substrate the switching elements may be fabricated on the main surface of an insulating substrate, such as a glass substrate. *See e.g.*, Hirabayashi, col. 31, ll. 16-20. The insulating substrate of Hirabayashi includes various areas that can meet this limitation, including for example, the dummy sealing region or a portion thereof, the pad region or portion thereof, the peripheral circuit region or a portion thereof, or any combination of these areas. *See e.g.*, Hirabayashi, Figs. 1 and 4-6.
forming a thin film transistor array formed on the insulating substrate;	Hirabayashi discloses forming switching elements, for example thin film transistor, on the substrate. *See e.g.*, Hirabayashi,, col. 31, ll. 16-23.
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Hirabayashi discloses a plurality of wiring, where each wiring is in communication with at least one of the transistors in the thin film array in order for the display device to function. *See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin.
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Hirabayashi discloses connection or terminal pads that connect to the opposite end of the plurality of wirings. *See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18.
forming pixel electrodes, and	Hirabayashi discloses a pixel region. *See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7.
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Hirabayashi discloses dummy patterns that are located between the connection pads and the pixel electrodes and are not in contact with any of the wirings. *See e.g.*, Hirabayashi, Figs. 1, 4-6, shown in hatch pattern; col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54. The dummy conductive patterns comprise well over 30% of various selected areas.
CLAIM 10	
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.	Hirabayashi discloses that the wiring can comprise a multilayer structure of Ti/TiN/Al/TiN in that order from the bottom. *See e.g.*, Hirabayashi, col. 16, ll. 19-22.

CLAIM 11	
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.	Hirabayashi discloses that the wiring can comprise a multilayer of Ti/TiN/Al/TiN. Focusing on two of the layers, Hirabayashi teaches of a lower layer of Al and an upper layer of TiN. *See e.g.*, Hirabayashi, col. 16, ll. 19-22.
CLAIM 12	
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Hirabayashi discloses that the wiring can comprise a multilayer of Ti/TiN/Al/TiN. Focusing on two of the layers, Hirabayashi teaches of a lower layer of Al and an upper layer of TiN. *See e.g.*, Hirabayashi, col. 16, ll. 19-22.
CLAIM 13	
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Hirabayashi discloses that the wiring can comprise a multilayer of Ti/TiN/Al/TiN. Focusing on two of the layers, Hirabayashi teaches of a lower layer of Al and an upper layer of TiN. *See e.g.*, Hirabayashi, col. 16, ll. 19-22.
CLAIM 15	
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Hirabayashi discloses that the wiring can comprise a multilayer of Ti/TiN/Al/TiN. The upper layer of TiN would inherently meet this limitation. *See e.g.*, Hirabayashi, col. 16, ll. 19-22; see also Ex. N at 240-241.
CLAIM 16	
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Hirabayashi discloses that the wiring can comprise a multilayer of Ti/TiN/Al/TiN. The upper layer of TiN would inherently meet this limitation. *See e.g.*, Hirabayashi, col. 16, ll. 19-22; see also Ex. N at 240-241.

APPENDIX CC2

U.S. PATENT NO. 6, 689, 629 - HIRABAYASHI IN VIEW OF SONG

As detailed below European Patent Application 0887695 to Hirabayashi in view of U.S. Patent No. 6,163,356 to Song renders obvious claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – HIRABAYASHI	PRIOR ART DISCLOSURE – SONG
An array substrate for display, comprising:	Hirabayashi discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1.	
a layer of an insulating substrate, having an area;	Hirabayashi discloses that in the liquid crystal panel substrate the switching elements may be fabricated on the main surface of an insulating substrate, such as a glass substrate. *See e.g.*, Hirabayashi, col. 31, ll. 16-20. The insulating substrate of Hirabayashi includes various areas that can meet this limitation, including for example, the dummy sealing region or a portion thereof, the pad region or portion thereof, the peripheral circuit region or a portion thereof, or any combination of these areas. *See e.g.*, Hirabayashi, Figs. 1 and 4-6.	
a thin film transistor array formed on the insulating substrate;	Hirabayashi discloses forming switching elements, for example thin film transistor, on the substrate. *See e.g.*, Hirabayashi,, col. 31, ll. 16-23.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Hirabayashi discloses a plurality of wiring, where each wiring is in communication with at least one of the transistors in the thin film array in order for the display device to function. *See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin.	

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Hirabayashi discloses connection or terminal pads that connect to the opposite end of the plurality of wirings. *See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18.	
pixel electrodes, and	Hirabayashi discloses a pixel region. *See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Hirabayashi discloses dummy patterns that are located between the connection pads and the pixel electrodes and are not in contact with any of the wirings. *See e.g.*, Hirabayashi, Figs. 1, 4-6, shown in hatch pattern; col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54. The dummy conductive patterns comprise well over 30% of various selected areas.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 9		
A meted [sic] for forming	Hirabayashi discloses an array	

an array substrate for display, comprising:	substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1.	
forming a layer of an insulating substrate, having an area;	Hirabayashi discloses that in the liquid crystal panel substrate the switching elements may be fabricated on the main surface of an insulating substrate, such as a glass substrate. *See e.g.*, Hirabayashi, col. 31, ll. 16-20. The insulating substrate of Hirabayashi includes various areas that can meet this limitation, including for example, the dummy sealing region or a portion thereof, the pad region or portion thereof, the peripheral circuit region or a portion thereof, or any combination of these areas. *See e.g.*, Hirabayashi, Figs. 1 and 4-6.	
forming a thin film transistor array formed on the insulating substrate;	Hirabayashi discloses forming switching elements, for example thin film transistor, on the substrate. *See e.g.*, Hirabayashi,, col. 31, ll. 16-23.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Hirabayashi discloses a plurality of wiring, where each wiring is in communication with at least one of the transistors in the thin film array in order for the display device to function. *See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Hirabayashi discloses connection or terminal pads that connect to the opposite end of the plurality of wirings. *See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18.	
Forming pixel electrodes, and	Hirabayashi discloses a pixel region. *See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7.	

forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Hirabayashi discloses dummy patterns that are located between the connection pads and the pixel electrodes and are not in contact with any of the wirings. *See e.g.*, Hirabayashi, Figs. 1, 4-6, shown in hatch pattern; col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54. The dummy conductive patterns comprise well over 30% of various selected areas.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or

wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

APPENDIX CC3

U.S. PATENT NO. 6, 689, 629 - HIRABAYASHI IN VIEW OF THE '629 APA

As detailed below European Patent Application 0887695 to Hirabayashi in view of the '629 Admitted Prior Art renders obvious claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – HIRABAYASHI	PRIOR ART DISCLOSURE – THE '629 APA
An array substrate for display, comprising:	Hirabayashi discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1.	
a layer of an insulating substrate, having an area;	Hirabayashi discloses that in the liquid crystal panel substrate the switching elements may be fabricated on the main surface of an insulating substrate, such as a glass substrate. *See e.g.*, Hirabayashi, col. 31, ll. 16-20. The insulating substrate of Hirabayashi includes various areas that can meet this limitation, including for example, the dummy sealing region or a portion thereof, the pad region or portion thereof, the peripheral circuit region or a portion thereof, or any combination of these areas. *See e.g.*, Hirabayashi, Figs. 1 and 4-6.	
a thin film transistor array formed on the insulating substrate;	Hirabayashi discloses forming switching elements, for example thin film transistor, on the substrate. *See e.g.*, Hirabayashi,, col. 31, ll. 16-23.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Hirabayashi discloses a plurality of wiring, where each wiring is in communication with at least one of the transistors in the thin film array in order for the display device to function. *See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin.	

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Hirabayashi discloses connection or terminal pads that connect to the opposite end of the plurality of wirings. *See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18.	
pixel electrodes, and	Hirabayashi discloses a pixel region. *See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Hirabayashi discloses dummy patterns that are located between the connection pads and the pixel electrodes and are not in contact with any of the wirings. *See e.g.*, Hirabayashi, Figs. 1, 4-6, shown in hatch pattern; col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54. The dummy conductive patterns comprise well over 30% of various selected areas.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the

		'629 patent, col. 1, ll. 26-39.

CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Hirabayashi discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1.	
forming a layer of an insulating substrate, having an area;	Hirabayashi discloses that in the liquid crystal panel substrate the switching elements may be fabricated on the main surface of an insulating substrate, such as a glass substrate. *See e.g.*, Hirabayashi, col. 31, ll. 16-20. The insulating substrate of Hirabayashi includes various areas that can meet this limitation, including for example, the dummy sealing region or a portion thereof, the pad region or portion thereof, the peripheral circuit region or a portion thereof, or any combination of these areas. *See e.g.*, Hirabayashi, Figs. 1 and 4-6.	
forming a thin film transistor array formed on the insulating substrate;	Hirabayashi discloses forming switching elements, for example thin film transistor, on the substrate. *See e.g.*, Hirabayashi,, col. 31, ll. 16-23.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Hirabayashi discloses a plurality of wiring, where each wiring is in communication with at least one of the transistors in the thin film array in order for the display device to function. *See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Hirabayashi discloses connection or terminal pads that connect to the opposite end of the plurality of wirings. *See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18.	

Forming pixel electrodes, and	Hirabayashi discloses a pixel region. *See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Hirabayashi discloses dummy patterns that are located between the connection pads and the pixel electrodes and are not in contact with any of the wirings. *See e.g.*, Hirabayashi, Figs. 1, 4-6, shown in hatch pattern; col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54. The dummy conductive patterns comprise well over 30% of various selected areas.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 13		
The method for forming an		The '629 APA discloses a

array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

APPENDIX CC4

U.S. PATENT NO. 6, 689, 629 - HIRABAYASHI IN VIEW OF KUBOTA

As detailed below European Patent Application 0887695 to Hirabayashi in view of U.S. Patent No. 6,157,430 to Kubota renders obvious claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – HIRABAYASHI	PRIOR ART DISCLOSURE – KUBOTA
An array substrate for display, comprising:	Hirabayashi discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1.	
a layer of an insulating substrate, having an area;	Hirabayashi discloses that in the liquid crystal panel substrate the switching elements may be fabricated on the main surface of an insulating substrate, such as a glass substrate. *See e.g.*, Hirabayashi, col. 31, ll. 16-20. The insulating substrate of Hirabayashi includes various areas that can meet this limitation, including for example, the dummy sealing region or a portion thereof, the pad region or portion thereof, the peripheral circuit region or a portion thereof, or any combination of these areas. *See e.g.*, Hirabayashi, Figs. 1 and 4-6.	
a thin film transistor array formed on the insulating substrate;	Hirabayashi discloses forming switching elements, for example thin film transistor, on the substrate. *See e.g.*, Hirabayashi,, col. 31, ll. 16-23.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Hirabayashi discloses a plurality of wiring, where each wiring is in communication with at least one of the transistors in the thin film array in order for the display device to function. *See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin.	

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Hirabayashi discloses connection or terminal pads that connect to the opposite end of the plurality of wirings. *See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18.	
pixel electrodes, and	Hirabayashi discloses a pixel region. *See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Hirabayashi discloses dummy patterns that are located between the connection pads and the pixel electrodes and are not in contact with any of the wirings. *See e.g.*, Hirabayashi, Figs. 1, 4-6, shown in hatch pattern; col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54. The dummy conductive patterns comprise well over 30% of various selected areas.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 8		

The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Hirabayashi discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1.	
forming a layer of an insulating substrate, having an area;	Hirabayashi discloses that in the liquid crystal panel substrate the switching elements may be fabricated on the main surface of an insulating substrate, such as a glass substrate. *See e.g.*, Hirabayashi, col. 31, ll. 16-20. The insulating substrate of Hirabayashi includes various areas that can meet this limitation, including for example, the dummy sealing region or a portion thereof, the pad region or portion thereof, the peripheral circuit region or a portion thereof, or any combination of these areas. *See e.g.*, Hirabayashi, Figs. 1 and 4-6.	
forming a thin film transistor array formed on the insulating substrate;	Hirabayashi discloses forming switching elements, for example thin film transistor, on the substrate. *See e.g.*, Hirabayashi,, col. 31, ll. 16-23.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Hirabayashi discloses a plurality of wiring, where each wiring is in communication with at least one of the transistors in the thin film array in order for the display	

	device to function. *See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Hirabayashi discloses connection or terminal pads that connect to the opposite end of the plurality of wirings. *See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18.	
Forming pixel electrodes, and	Hirabayashi discloses a pixel region. *See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Hirabayashi discloses dummy patterns that are located between the connection pads and the pixel electrodes and are not in contact with any of the wirings. *See e.g.*, Hirabayashi, Figs. 1, 4-6, shown in hatch pattern; col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54. The dummy conductive patterns comprise well over 30% of various selected areas.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or

		alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 14		
The method for forming an array substrate for display according to claim 13, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g.,

		Kubota, col. 4, ll. 39-55.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

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APPENDIX CC5

U.S. PATENT NO. 6, 689, 629 - WATANABE '275

U.S. Patent No. 5,850,275 To Watanabe anticipates claims 1-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – WATANABE '275
An array substrate for display, comprising:	Watanabe '275 discloses a liquid crystal panel 11 including a display portion 14. See, e.g., Watanabe '275 col 3, lines 22-23; Figs 1, 3-4.
a layer of an insulating substrate, having an area;	Watanabe '275 discloses a TFT glass substrate 21 having an area, for example portion G. See, e.g., Watanabe '275, col 3, lines 27-30; Figs. 1-4.
a thin film transistor array formed on the insulating substrate;	Watanabe '275 discloses a glass substrate 21 including thin film transistors. See, e.g., Watanabe '275, col. 3:37-44; Fig 1-4.
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.
pixel electrodes, and	Watanabe '275 discloses a plurality of transparent pixel electrodes 22 that are formed in a matrix on the TFT substrate. See, e.g., Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4.
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Watanabe '275 discloses that a light shield area 20 is located between the terminals 23 and the matrix of pixel electrodes 22. See, e.g., Watanabe '275, Figs 1-2, and 6. The light shield area has a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area. See, e.g., Watanabe '275, col 4, lines 28-30; Fig. 2. The specification also states that the light shield area 20 should be as large as possible. See, e.g., Watanabe '275, col 4, lines 28-30. Further, the light shield area is not in contact with the outgoing lines 24. See, e.g., Watanabe '275, col. 3:28-35; Figs 2 and 6.
CLAIM 2	
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.	Watanabe '275 discloses that the materials for the wiring can include molybdenum and aluminum. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 3	

The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.	Watanabe '275 discloses that the materials for the wiring can include aluminum. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 4	
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Watanabe '275 discloses that the materials for the wiring can include molybdenum. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 5	
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Watanabe '275 discloses that the materials for the wiring can include molybdenum. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 6	
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.	Watanabe '275 discloses that the materials for the wiring can include molybdenum. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 7	
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Watanabe '275 discloses that the materials for the wiring can include molybdenum, which inherently meet this limitation. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 8	
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Watanabe '275 discloses that the materials for the wiring can include molybdenum, which inherently meet this limitation. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 9	
A meted for forming an array substrate for display, comprising:	Watanabe '275 discloses a liquid crystal panel 11 including a display portion 14. See, e.g., Watanabe '275 col 3, lines 22-23; Figs 1, 3-4.
forming a layer of an insulating substrate, having an area;	Watanabe '275 discloses a TFT glass substrate 21 having an area, for example portion G. See, e.g., Watanabe '275, col 3, lines 27-30; Figs. 1-4.
forming a thin film transistor array formed on the insulating substrate;	Watanabe '275 discloses a glass substrate 21 including thin film transistors. See, e.g., Watanabe '275, col.

	3:37-44; Fig 1-4.
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.
forming pixel electrodes, and	Watanabe '275 discloses a plurality of transparent pixel electrodes 22 that are formed in a matrix on the TFT substrate. See, e.g., Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4.
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Watanabe '275 discloses that a light shield area 20 is located between the terminals 23 and the matrix of pixel electrodes 22. See, e.g., Watanabe '275, Figs 1-2, and 6. The light shield area has a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area. See, e.g., Watanabe '275, col 4, lines 28-30; Fig. 2. The specification also states that the light shield area 20 should be as large as possible. See, e.g., Watanabe '275, col 4, lines 28-30. Further, the light shield area is not in contact with the outgoing lines 24. See, e.g., Watanabe '275, col. 3:28-35; Figs 2 and 6.
CLAIM 10	
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.	Watanabe '275 discloses that the materials for the wiring can include molybdenum and aluminum. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 11	
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.	Watanabe '275 discloses that the materials for the wiring can include aluminum. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 12	
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Watanabe '275 discloses that the materials for the wiring can include molybdenum. See, e.g., Watanabe '275, col 4, lines 24-28.

CLAIM 13	
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Watanabe '275 discloses that the materials for the wiring can include molybdenum. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 14	
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.	Watanabe '275 discloses that the materials for the wiring can include molybdenum. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 15	
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Watanabe '275 discloses that the materials for the wiring can include molybdenum, which inherently meet this limitation. See, e.g., Watanabe '275, col 4, lines 24-28.
CLAIM 16	
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Watanabe '275 discloses that the materials for the wiring can include molybdenum, which inherently meet this limitation. See, e.g., Watanabe '275, col 4, lines 24-28.

APPENDIX CC6

U.S. PATENT NO. 6, 689, 629 - WATANABE '275 IN VIEW OF SONG

U.S. Patent No. 5,850,275 To Watanabe in view of U.S. Patent No. 6,163,356 to Song renders obvious claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – WATANABE	PRIOR ART DISCLOSURE – SONG
An array substrate for display, comprising:	Watanabe '275 discloses a liquid crystal panel 11 including a display portion 14. See, e.g., Watanabe '275 col 3, lines 22-23; Figs 1, 3-4.	
a layer of an insulating substrate, having an area;	Watanabe '275 discloses a TFT glass substrate 21 having an area, for example portion G. See, e.g., Watanabe '275, col 3, lines 27-30; Figs. 1-4.	
a thin film transistor array formed on the insulating substrate;	Watanabe '275 discloses a glass substrate 21 including thin film transistors. See, e.g., Watanabe '275, col. 3:37-44; Fig 1-4.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
pixel electrodes, and	Watanabe '275 discloses a plurality of transparent pixel electrodes 22 that are formed in a matrix on the TFT substrate. See, e.g., Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the	Watanabe '275 discloses that a light shield area 20 is located between the terminals 23 and the matrix of pixel electrodes 22.	

insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	See, e.g., Watanabe '275, Figs 1-2, and 6. The light shield area has a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area. See, e.g., Watanabe '275, col 4, lines 28-30; Fig. 2. The specification also states that the light shield area 20 should be as large as possible. See, e.g., Watanabe '275, col 4, lines 28-30. Further, the light shield area is not in contact with the outgoing lines 24. See, e.g., Watanabe '275, col. 3:28-35; Figs 2 and 6.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer		Song discloses a dual layer wiring including aluminum with chromium,

wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Watanabe '275 discloses a liquid crystal panel 11 including a display portion 14. See, e.g., Watanabe '275 col 3, lines 22-23; Figs 1, 3-4.	
forming a layer of an insulating substrate, having an area;	Watanabe '275 discloses a TFT glass substrate 21 having an area, for example portion G. See, e.g., Watanabe '275, col 3, lines 27-30; Figs. 1-4.	
forming a thin film transistor array formed on the insulating substrate;	Watanabe '275 discloses a glass substrate 21 including thin film transistors. See, e.g., Watanabe '275, col. 3:37-44; Fig 1-4.	

each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
Forming pixel electrodes, and	Watanabe '275 discloses a plurality of transparent pixel electrodes 22 that are formed in a matrix on the TFT substrate. See, e.g., Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Watanabe '275 discloses that a light shield area 20 is located between the terminals 23 and the matrix of pixel electrodes 22. See, e.g., Watanabe '275, Figs 1-2, and 6. The light shield area has a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area. See, e.g., Watanabe '275, col 4, lines 28-30; Fig. 2. The specification also states that the light shield area 20 should be as large as possible. See, e.g., Watanabe '275, col 4, lines 28-30. Further, the light shield area is not in contact with the outgoing lines 24. See, e.g., Watanabe '275, col. 3:28-35; Figs 2 and 6.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

materials.		
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or

wiring material does not become insoluble in an acid or alkaline etchant.		antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

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APPENDIX CC7

U.S. PATENT NO. 6, 689, 629 - WATANABE '275 IN VIEW OF THE '629 APA

U.S. Patent No. 5,850,275 To Watanabe in view of the '629 Admitted Prior Art renders obvious claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – WATANABE	PRIOR ART DISCLOSURE – THE '629 APA
An array substrate for display, comprising:	Watanabe '275 discloses a liquid crystal panel 11 including a display portion 14. See, e.g., Watanabe '275 col 3, lines 22-23; Figs 1, 3-4.	
a layer of an insulating substrate, having an area;	Watanabe '275 discloses a TFT glass substrate 21 having an area, for example portion G. See, e.g., Watanabe '275, col 3, lines 27-30; Figs. 1-4.	
a thin film transistor array formed on the insulating substrate;	Watanabe '275 discloses a glass substrate 21 including thin film transistors. See, e.g., Watanabe '275, col. 3:37-44; Fig 1-4.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
pixel electrodes, and	Watanabe '275 discloses a plurality of transparent pixel electrodes 22 that are formed in a matrix on the TFT substrate. See, e.g., Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4.	
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the	Watanabe '275 discloses that a light shield area 20 is located between the terminals 23 and the matrix of pixel electrodes 22.	

insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	See, e.g., Watanabe '275, Figs 1-2, and 6. The light shield area has a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area. See, e.g., Watanabe '275, col 4, lines 28-30; Fig. 2. The specification also states that the light shield area 20 should be as large as possible. See, e.g., Watanabe '275, col 4, lines 28-30. Further, the light shield area is not in contact with the outgoing lines 24. See, e.g., Watanabe '275, col. 3:28-35; Figs 2 and 6.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 5		
The array substrate for		The '629 APA discloses a

display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Watanabe '275 discloses a liquid crystal panel 11 including a display portion 14. See, e.g., Watanabe '275 col 3, lines 22-23; Figs 1, 3-4.	
forming a layer of an insulating substrate, having an area;	Watanabe '275 discloses a TFT glass substrate 21 having an area, for example portion G. See, e.g., Watanabe '275, col 3, lines 27-30; Figs. 1-4.	

forming a thin film transistor array formed on the insulating substrate;	Watanabe '275 discloses a glass substrate 21 including thin film transistors. See, e.g., Watanabe '275, col. 3:37-44; Fig 1-4.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
forming pixel electrodes, and	Watanabe '275 discloses a plurality of transparent pixel electrodes 22 that are formed in a matrix on the TFT substrate. See, e.g., Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Watanabe '275 discloses that a light shield area 20 is located between the terminals 23 and the matrix of pixel electrodes 22. See, e.g., Watanabe '275, Figs 1-2, and 6. The light shield area has a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area. See, e.g., Watanabe '275, col 4, lines 28-30; Fig. 2. The specification also states that the light shield area 20 should be as large as possible. See, e.g., Watanabe '275, col 4, lines 28-30. Further, the light shield area is not in contact with the outgoing lines 24. See, e.g., Watanabe '275, col. 3:28-35; Figs 2 and 6.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9,		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer

wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 15		

The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

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APPENDIX CC8

U.S. PATENT NO. 6, 689, 629 - WATANABE '275 IN VIEW OF KUBOTA

U.S. Patent No. 5,850,275 To Watanabe in view of U.S. Patent No. 6,157,430 to Kubota renders obvious claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – WATANABE	PRIOR ART DISCLOSURE – KUBOTA
An array substrate for display, comprising:	Watanabe '275 discloses a liquid crystal panel 11 including a display portion 14. See, e.g., Watanabe '275 col 3, lines 22-23; Figs 1, 3-4.	
a layer of an insulating substrate, having an area;	Watanabe '275 discloses a TFT glass substrate 21 having an area, for example portion G. See, e.g., Watanabe '275, col 3, lines 27-30; Figs. 1-4.	
a thin film transistor array formed on the insulating substrate;	Watanabe '275 discloses a glass substrate 21 including thin film transistors. See, e.g., Watanabe '275, col. 3:37-44; Fig 1-4.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
pixel electrodes, and	Watanabe '275 discloses a plurality of transparent pixel electrodes 22 that are formed in a matrix on the TFT substrate. See, e.g., Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the	Watanabe '275 discloses that a light shield area 20 is located between the terminals 23 and the matrix of pixel electrodes 22.	

insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	See, e.g., Watanabe '275, Figs 1-2, and 6. The light shield area has a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area. See, e.g., Watanabe '275, col 4, lines 28-30; Fig. 2. The specification also states that the light shield area 20 should be as large as possible. See, e.g., Watanabe '275, col 4, lines 28-30. Further, the light shield area is not in contact with the outgoing lines 24. See, e.g., Watanabe '275, col. 3:28-35; Figs 2 and 6.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 8		

The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Watanabe '275 discloses a liquid crystal panel 11 including a display portion 14. See, e.g., Watanabe '275 col 3, lines 22-23; Figs 1, 3-4.	
forming a layer of an insulating substrate, having an area;	Watanabe '275 discloses a TFT glass substrate 21 having an area, for example portion G. See, e.g., Watanabe '275, col 3, lines 27-30; Figs. 1-4.	
forming a thin film transistor array formed on the insulating substrate;	Watanabe '275 discloses a glass substrate 21 including thin film transistors. See, e.g., Watanabe '275, col. 3:37-44; Fig 1-4.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Watanabe '275 discloses outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22. See, e.g., Watanabe '275, col. 3:37-44; Figs 1-2.	
forming pixel electrodes, and	Watanabe '275 discloses a plurality of transparent pixel electrodes 22 that are formed in a matrix on the TFT substrate. See, e.g., Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4.	
forming dummy conductive patterns, the dummy patterns comprising at least	Watanabe '275 discloses that a light shield area 20 is located between the terminals 23 and the	

about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	matrix of pixel electrodes 22. See, e.g., Watanabe '275, Figs 1-2, and 6. The light shield area has a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area. See, e.g., Watanabe '275, col 4, lines 28-30; Fig. 2. The specification also states that the light shield area 20 should be as large as possible. See, e.g., Watanabe '275, col 4, lines 28-30. Further, the light shield area is not in contact with the outgoing lines 24. See, e.g., Watanabe '275, col. 3:28-35; Figs 2 and 6.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a

from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of

or alkaline etchant.		chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

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APPENDIX CC9

U.S. PATENT NO. 6, 689,629 - KWAK

U.S. Patent No. 6,862,069 to Kwak et al anticipates Claims 1-2 and 9-10 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE - KWAK '069
An array substrate for display, comprising:	Kwak discloses a liquid crystal display panel includes a display part 10. See, e.g., Kwak, col. 1, ll. 34-36, Fig. 1.
a layer of an insulating substrate, having an area;	Kwak discloses a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15. See, e.g., Kwak, col. 2, ll. 6-9, 20-23, Figs 1 and 3.
a thin film transistor array formed on the insulating substrate;	Kwak discloses that at each crossover point of the gate lines and data lines there is a thin film transistor. See, e.g., Kwak at col. 1, ll. 43-45, Fig. 1.
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Kwak discloses gate links 15 and data links 33 is formed on transparent substrate 20 that connect to TFTs at the crossover points. See, e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12.
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Kwak discloses gate pads 14 and data pad 32 that contact the gate links 15 and data links 33. See, e.g., Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9.
pixel electrodes, and	Kwak discloses a pixel electrode is connected to the TFT to drive the liquid crystal cell. See, e.g., Kwak at col. 1, ll. 45-46.
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Kwak discloses dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10. See, e.g., Kwak at Figs 7 and 9. Kwak further discloses that the distance between the gate links in the convention art was 100 μm, but Kwak '069 teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus covering at least 30% of the area. See, e.g., Kwak at col. 4, ll. 28-41. Further, the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33. See, e.g., Kwak at Figs 7-12.

CLAIM 2	
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.	Kwak discloses the gate links and data links comprise multiple layers of conductive materials such as metal layer 16 and 34, amorphous silicon 24 , and n+ layer 26. See, e.g., Kwak at col. 4, ll. 21-25.
CLAIM 9	
A meted for forming an array substrate for display, comprising:	Kwak discloses a liquid crystal display panel includes a display part 10. See, e.g., Kwak, col. 1, ll. 34-36, Fig. 1.
forming a layer of an insulating substrate, having an area;	Kwak discloses a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15. See, e.g., Kwak, col. 2, ll. 6-9, 20-23, Figs 1 and 3.
forming a thin film transistor array formed on the insulating substrate;	Kwak discloses that at each crossover point of the gate lines and data lines there is a thin film transistor. See, e.g., Kwak at col. 1, ll. 43-45, Fig. 1.
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Kwak discloses gate links 15 and data links 33 is formed on transparent substrate 20 that connect to TFTs at the crossover points. See, e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12.
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Kwak discloses gate pads 14 and data pad 32 that contact the gate links 15 and data links 33. See, e.g., Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9.
forming pixel electrodes, and	Kwak discloses a pixel electrode is connected to the TFT to drive the liquid crystal cell. See, e.g., Kwak at col. 1, ll. 45-46.
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Kwak discloses dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10. See, e.g., Kwak at Figs 7 and 9. Kwak further discloses that the distance between the gate links in the convention art was 100 μm, but Kwak '069 teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus covering at least 30% of the area. See, e.g., Kwak at col. 4, ll. 28-41. Further, the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33. See, e.g., Kwak at Figs 7-12.
CLAIM 10	
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings	Kwak discloses the gate links and data links comprise multiple layers of conductive materials such as metal layer 16 and 34, amorphous silicon 24 , and n+ layer

comprises at least an upper layer and a lower layer of conductive materials.	26. See, e.g., Kwak at col. 4, ll. 21-25.

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APPENDIX CC10

U.S. PATENT NO. 6, 689,629 - KWAK IN VIEW OF SONG

U.S. Patent No. 6,862,069 to Kwak in view of U.S. Patent No. 6,163,356 to Song renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – KWAK	PRIOR ART DISCLOSURE – SONG
An array substrate for display, comprising:	Kwak discloses a liquid crystal display panel includes a display part 10. See, e.g., Kwak, col. 1, ll. 34-36, Fig. 1.	
a layer of an insulating substrate, having an area;	Kwak discloses a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15. See, e.g., Kwak, col. 2, ll. 6-9, 20-23, Figs 1 and 3.	
a thin film transistor array formed on the insulating substrate;	Kwak discloses that at each crossover point of the gate lines and data lines there is a thin film transistor. See, e.g., Kwak at col. 1, ll. 43-45, Fig. 1.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Kwak discloses gate links 15 and data links 33 is formed on transparent substrate 20 that connect to TFTs at the crossover points. See, e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Kwak discloses gate pads 14 and data pad 32 that contact the gate links 15 and data links 33. See, e.g., Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9.	
pixel electrodes, and	Kwak discloses a pixel electrode is connected to the TFT to drive the liquid crystal cell. See, e.g., Kwak at col. 1, ll. 45-46.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the	Kwak discloses dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10. See, e.g.,	

dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Kwak at Figs 7 and 9. Kwak further discloses that the distance between the gate links in the convention art was 100 μm, but Kwak '069 teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus covering at least 30% of the area. See, e.g., Kwak at col. 4, ll. 28-41. Further, the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33. See, e.g., Kwak at Figs 7-12.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or

from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Kwak discloses a liquid crystal display panel includes a display part 10. See, e.g., Kwak, col. 1, ll. 34-36, Fig. 1.	
forming a layer of an insulating substrate, having an area;	Kwak discloses a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15. See, e.g., Kwak, col. 2, ll. 6-9, 20-23, Figs 1 and 3.	
forming a thin film transistor array formed on the insulating substrate;	Kwak discloses that at each crossover point of the gate lines and data lines there is a thin film transistor. See, e.g., Kwak at col. 1, ll. 43-45, Fig. 1.	

each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Kwak discloses gate links 15 and data links 33 is formed on transparent substrate 20 that connect to TFTs at the crossover points. See, e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Kwak discloses gate pads 14 and data pad 32 that contact the gate links 15 and data links 33. See, e.g., Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9.	
Forming pixel electrodes, and	Kwak discloses a pixel electrode is connected to the TFT to drive the liquid crystal cell. See, e.g., Kwak at col. 1, ll. 45-46.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Kwak discloses dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10. See, e.g., Kwak at Figs 7 and 9. Kwak further discloses that the distance between the gate links in the convention art was 100 μm, but Kwak '069 teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus covering at least 30% of the area. See, e.g., Kwak at col. 4, ll. 28-41. Further, the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33. See, e.g., Kwak at Figs 7-12.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll.

or alkaline etchant.		5-18.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

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APPENDIX CC11

U.S. PATENT NO. 6, 689,629 - KWAK IN VIEW OF THE '629 APA

U.S. Patent No. 6,862,069 to Kwak in view of the '629 Admitted Prior Art renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – KWAK	PRIOR ART DISCLOSURE – THE '629 APA
An array substrate for display, comprising:	Kwak discloses a liquid crystal display panel includes a display part 10. See, e.g., Kwak, col. 1, ll. 34-36, Fig. 1.	
a layer of an insulating substrate, having an area;	Kwak discloses a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15. See, e.g., Kwak, col. 2, ll. 6-9, 20-23, Figs 1 and 3.	
a thin film transistor array formed on the insulating substrate;	Kwak discloses that at each crossover point of the gate lines and data lines there is a thin film transistor. See, e.g., Kwak at col. 1, ll. 43-45, Fig. 1.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Kwak discloses gate links 15 and data links 33 is formed on transparent substrate 20 that connect to TFTs at the crossover points. See, e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Kwak discloses gate pads 14 and data pad 32 that contact the gate links 15 and data links 33. See, e.g., Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9.	
pixel electrodes, and	Kwak discloses a pixel electrode is connected to the TFT to drive the liquid crystal cell. See, e.g., Kwak at col. 1, ll. 45-46.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the	Kwak discloses dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10. See, e.g.,	

dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Kwak at Figs 7 and 9. Kwak further discloses that the distance between the gate links in the convention art was 100 μm, but Kwak '069 teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus covering at least 30% of the area. See, e.g., Kwak at col. 4, ll. 28-41. Further, the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33. See, e.g., Kwak at Figs 7-12.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 5		
The array substrate for display according to claim		The '629 APA discloses a lower layer wiring material of

3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Kwak discloses a liquid crystal display panel includes a display part 10. See, e.g., Kwak, col. 1, ll. 34-36, Fig. 1.	
forming a layer of an insulating substrate, having an area;	Kwak discloses a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15. See, e.g., Kwak, col. 2, ll. 6-9, 20-23, Figs 1 and 3.	

forming a thin film transistor array formed on the insulating substrate;	Kwak discloses that at each crossover point of the gate lines and data lines there is a thin film transistor. See, e.g., Kwak at col. 1, ll. 43-45, Fig. 1.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Kwak discloses gate links 15 and data links 33 is formed on transparent substrate 20 that connect to TFTs at the crossover points. See, e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Kwak discloses gate pads 14 and data pad 32 that contact the gate links 15 and data links 33. See, e.g., Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9.	
Forming pixel electrodes, and	Kwak discloses a pixel electrode is connected to the TFT to drive the liquid crystal cell. See, e.g., Kwak at col. 1, ll. 45-46.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Kwak discloses dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10. See, e.g., Kwak at Figs 7 and 9. Kwak further discloses that the distance between the gate links in the convention art was 100 μm, but Kwak '069 teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus covering at least 30% of the area. See, e.g., Kwak at col. 4, ll. 28-41. Further, the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33. See, e.g., Kwak at Figs 7-12.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder

wirings comprises at least an upper layer and a lower layer of conductive materials.		to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 15		
The method for forming an array substrate for display		The '629 APA discloses a lower layer wiring material of

according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

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APPENDIX CC12

U.S. PATENT NO. 6, 689,629 - KWAK IN VIEW OF KUBOTA

U.S. Patent No. 6,862,069 to Kwak in view of U.S. Patent No. 6,157,430 to Kubota renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – KWAK	PRIOR ART DISCLOSURE – KUBOTA
An array substrate for display, comprising:	Kwak discloses a liquid crystal display panel includes a display part 10. See, e.g., Kwak, col. 1, ll. 34-36, Fig. 1.	
a layer of an insulating substrate, having an area;	Kwak discloses a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15. See, e.g., Kwak, col. 2, ll. 6-9, 20-23, Figs 1 and 3.	
a thin film transistor array formed on the insulating substrate;	Kwak discloses that at each crossover point of the gate lines and data lines there is a thin film transistor. See, e.g., Kwak at col. 1, ll. 43-45, Fig. 1.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Kwak discloses gate links 15 and data links 33 is formed on transparent substrate 20 that connect to TFTs at the crossover points. See, e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Kwak discloses gate pads 14 and data pad 32 that contact the gate links 15 and data links 33. See, e.g., Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9.	
pixel electrodes, and	Kwak discloses a pixel electrode is connected to the TFT to drive the liquid crystal cell. See, e.g., Kwak at col. 1, ll. 45-46.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the	Kwak discloses dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10. See, e.g.,	

insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Kwak at Figs 7 and 9. Kwak further discloses that the distance between the gate links in the convention art was 100 μm, but Kwak '069 teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus covering at least 30% of the area. See, e.g., Kwak at col. 4, ll. 28-41. Further, the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33. See, e.g., Kwak at Figs 7-12.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 9		
A meted for forming an array substrate for display, comprising:	Kwak discloses a liquid crystal display panel includes a display part 10. See, e.g., Kwak, col. 1, ll. 34-36, Fig. 1.	
forming a layer of an insulating substrate, having an area;	Kwak discloses a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15. See, e.g., Kwak, col. 2, ll. 6-9, 20-23, Figs 1 and 3.	
forming a thin film transistor array formed on the insulating substrate;	Kwak discloses that at each crossover point of the gate lines and data lines there is a thin film transistor. See, e.g., Kwak at col. 1, ll. 43-45, Fig. 1.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Kwak discloses gate links 15 and data links 33 is formed on transparent substrate 20 that connect to TFTs at the crossover points. See, e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Kwak discloses gate pads 14 and data pad 32 that contact the gate links 15 and data links 33. See, e.g., Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9.	
Forming pixel electrodes, and	Kwak discloses a pixel electrode is connected to the TFT to drive the liquid crystal cell. See, e.g., Kwak at col. 1, ll. 45-46.	
forming dummy conductive patterns, the dummy	Kwak discloses dummy patterns 36 and 38 are located between	

patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	gate pads 14 and data pads 32 and the display part 10. See, e.g., Kwak at Figs 7 and 9. Kwak further discloses that the distance between the gate links in the convention art was 100 μm, but Kwak '069 teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus covering at least 30% of the area. See, e.g., Kwak at col. 4, ll. 28-41. Further, the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33. See, e.g., Kwak at Figs 7-12.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a

from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

APPENDIX CC13

U.S. PATENT NO. 6, 689, 629 - YOSHINORI

Japanese Pub. No. H10-333151 to Yoshinori et al. anticipates Claims 1-5, 7-13, and 15-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – YOSHINORI
An array substrate for display, comprising:	Yoshinori discloses an array substrate 1 including a display area 2. See, e.g., Yoshinori, Abstract, Figs 1-3.
a layer of an insulating substrate, having an area;	Yoshinori discloses an array substrate 1, including an area. See, e.g., Yoshinori, Abstract, Figs 1-3.
a thin film transistor array formed on the insulating substrate;	Yoshinori discloses an array of TFTs is formed on the array substrate 1 in the display area 2. See, e.g., Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7.
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Yoshinori discloses scan and signal wiring that connect to the scan and signal electrodes 6 and 9. See, e.g., Yoshinori, ¶ 20, Figs 1-3.
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Yoshinori discloses connection pads 3 and 4 that connect to the scan and signal wiring. See, e.g., Yoshinori, ¶ 20, Figs 1-3.
pixel electrodes, and	Yoshinori discloses pixels electrodes 10. See, e.g., Yoshinori, Abstract, Figs 1-3.
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Yoshinori discloses equal-interval projection steps 5 are located between the connection pads 3 and 4 and the pixel electrodes 10. Yoshinori teaches, for example, the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area. See, e.g., Yoshinori, ¶ 20. Further, the projection steps or dummy patterns of Yoshinori do not contact the scan and signal wirings. See, e.g., Yoshinori, Figs 1-3.
CLAIM 2	
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.	Yoshinori discloses the signal electrode 9 comprises a bilayer of titanium/aluminum or can be a monolayer or multilayer film of conductive metal. See, e.g., Yoshinori, ¶ 20.
CLAIM 3	
The array substrate for display according to claim 2 wherein the lower	Yoshinori discloses the signal electrode 9 comprises a bilayer of titanium/aluminum or can be a monolayer or

layer wiring material is selected from the group consisting of aluminum and aluminum alloys.	multilayer film of conductive metal. See, e.g., Yoshinori, ¶ 20.
CLAIM 4	
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Yoshinori discloses the signal electrode 9 comprises a bilayer of titanium/aluminum or can be a monolayer or multilayer film of conductive metal. See, e.g., Yoshinori, ¶ 20.
CLAIM 5	
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Yoshinori discloses the signal electrode 9 comprises a bilayer of titanium/aluminum or can be a monolayer or multilayer film of conductive metal. See, e.g., Yoshinori, ¶ 20.
CLAIM 7	
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Yoshinori discloses the signal electrode 9 comprises a bilayer including titanium, which would inherently meet this limitation. See, e.g., Yoshinori, ¶ 20.
CLAIM 8	
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Yoshinori discloses the signal electrode 9 comprises a bilayer including titanium, which would inherently meet this limitation. See, e.g., Yoshinori, ¶ 20.
CLAIM 9	
A meted for forming an array substrate for display, comprising:	Yoshinori discloses an array substrate 1 including a display area 2. See, e.g., Yoshinori, Abstract, Figs 1-3.
forming a layer of an insulating substrate, having an area;	Yoshinori discloses an array substrate 1, including an area. See, e.g., Yoshinori, Abstract, Figs 1-3.
forming a thin film transistor array formed on the insulating substrate;	Yoshinori discloses an array of TFTs is formed on the array substrate 1 in the display area 2. See, e.g., Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7.
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Yoshinori discloses scan and signal wiring that connect to the scan and signal electrodes 6 and 9. See, e.g., Yoshinori, ¶ 20, Figs 1-3.

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Yoshinori discloses connection pads 3 and 4 that connect to the scan and signal wiring. See, e.g., Yoshinori, ¶ 20, Figs 1-3.
forming pixel electrodes, and	Yoshinori discloses pixels electrodes 10. See, e.g., Yoshinori, Abstract, Figs 1-3.
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Yoshinori discloses equal-interval projection steps 5 are located between the connection pads 3 and 4 and the pixel electrodes 10. Yoshinori teaches, for example, the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area. See, e.g., Yoshinori, ¶ 20. Further, the projection steps or dummy patterns of Yoshinori do not contact the scan and signal wirings. See, e.g., Yoshinori, Figs 1-3.
CLAIM 10	
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.	Yoshinori discloses the signal electrode 9 comprises a bilayer of titanium/aluminum or can be a monolayer or multilayer film of conductive metal. See, e.g., Yoshinori, ¶ 20.
CLAIM 11	
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.	Yoshinori discloses the signal electrode 9 comprises a bilayer of titanium/aluminum or can be a monolayer or multilayer film of conductive metal. See, e.g., Yoshinori, ¶ 20.
CLAIM 12	
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Yoshinori discloses the signal electrode 9 comprises a bilayer of titanium/aluminum or can be a monolayer or multilayer film of conductive metal. See, e.g., Yoshinori, ¶ 20.

CLAIM 13	
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Yoshinori discloses the signal electrode 9 comprises a bilayer of titanium/aluminum or can be a monolayer or multilayer film of conductive metal. See, e.g., Yoshinori, ¶ 20.
CLAIM 15	
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Yoshinori discloses the signal electrode 9 comprises a bilayer including titanium, which would inherently meet this limitation. See, e.g., Yoshinori, ¶ 20.
CLAIM 16	
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Yoshinori discloses the signal electrode 9 comprises a bilayer including titanium, which would inherently meet this limitation. See, e.g., Yoshinori, ¶ 20.

APPENDIX CC14

U.S. PATENT NO. 6, 689, 629 - YOSHINORI IN VIEW OF SONG

Japanese Pub. No. H10-333151 to Yoshinori et al. in view of U.S. Patent No. 6,163,356 to Song renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – YOSHINORI	PRIOR ART DISCLOSURE – SONG
An array substrate for display, comprising:	Yoshinori discloses an array substrate 1 including a display area 2. See, e.g., Yoshinori, Abstract, Figs 1-3.	
a layer of an insulating substrate, having an area;	Yoshinori discloses an array substrate 1, including an area. See, e.g., Yoshinori, Abstract, Figs 1-3.	
a thin film transistor array formed on the insulating substrate;	Yoshinori discloses an array of TFTs is formed on the array substrate 1 in the display area 2. See, e.g., Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Yoshinori discloses scan and signal wiring that connect to the scan and signal electrodes 6 and 9. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Yoshinori discloses connection pads 3 and 4 that connect to the scan and signal wiring. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
pixel electrodes, and	Yoshinori discloses pixels electrodes 10. See, e.g., Yoshinori, Abstract, Figs 1-3.	
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in	Yoshinori discloses equal-interval projection steps 5 are located between the connection pads 3 and 4 and the pixel electrodes 10. Yoshinori teaches, for example, the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area. See, e.g., Yoshinori, ¶ 20. Further,	

contact with any of the wiring.	the projection steps or dummy patterns of Yoshinori do not contact the scan and signal wirings. See, e.g., Yoshinori, Figs 1-3.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g.,

molybdenum and alloys thereof.		Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Yoshinori discloses an array substrate 1 including a display area 2. See, e.g., Yoshinori, Abstract, Figs 1-3.	
forming a layer of an insulating substrate, having an area;	Yoshinori discloses an array substrate 1, including an area. See, e.g., Yoshinori, Abstract, Figs 1-3.	
forming a thin film transistor array formed on the insulating substrate;	Yoshinori discloses an array of TFTs is formed on the array substrate 1 in the display area 2. See, e.g., Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Yoshinori discloses scan and signal wiring that connect to the scan and signal electrodes 6 and 9. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Yoshinori discloses connection pads 3 and 4 that connect to the scan and signal wiring. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
Forming pixel electrodes, and	Yoshinori discloses pixels electrodes 10. See, e.g., Yoshinori, Abstract, Figs 1-3.	

forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Yoshinori discloses equal-interval projection steps 5 are located between the connection pads 3 and 4 and the pixel electrodes 10. Yoshinori teaches, for example, the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area. See, e.g., Yoshinori, ¶ 20. Further, the projection steps or dummy patterns of Yoshinori do not contact the scan and signal wirings. See, e.g., Yoshinori, Figs 1-3.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 13		
The method for forming an		Song discloses a dual layer

array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

APPENDIX CC15

U.S. PATENT NO. 6, 689, 629 - YOSHINORI IN VIEW OF '629 APA

Japanese Pub. No. H10-333151 to Yoshinori et al. in view the '629 Admitted Prior Art renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – YOSHINORI	PRIOR ART DISCLOSURE – THE '629 APA
An array substrate for display, comprising:	Yoshinori discloses an array substrate 1 including a display area 2. See, e.g., Yoshinori, Abstract, Figs 1-3.	
a layer of an insulating substrate, having an area;	Yoshinori discloses an array substrate 1, including an area. See, e.g., Yoshinori, Abstract, Figs 1-3.	
a thin film transistor array formed on the insulating substrate;	Yoshinori discloses an array of TFTs is formed on the array substrate 1 in the display area 2. See, e.g., Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Yoshinori discloses scan and signal wiring that connect to the scan and signal electrodes 6 and 9. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Yoshinori discloses connection pads 3 and 4 that connect to the scan and signal wiring. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
pixel electrodes, and	Yoshinori discloses pixels electrodes 10. See, e.g., Yoshinori, Abstract, Figs 1-3.	

Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Yoshinori discloses equal-interval projection steps 5 are located between the connection pads 3 and 4 and the pixel electrodes 10. Yoshinori teaches, for example, the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area. See, e.g., Yoshinori, ¶ 20. Further, the projection steps or dummy patterns of Yoshinori do not contact the scan and signal wirings. See, e.g., Yoshinori, Figs 1-3.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 5		
The array substrate for display according to claim		The '629 APA discloses a lower layer wiring material of

3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Yoshinori discloses an array substrate 1 including a display area 2. See, e.g., Yoshinori, Abstract, Figs 1-3.	
forming a layer of an insulating substrate, having an area;	Yoshinori discloses an array substrate 1, including an area. See, e.g., Yoshinori, Abstract, Figs 1-3.	
forming a thin film transistor array formed on the insulating substrate;	Yoshinori discloses an array of TFTs is formed on the array substrate 1 in the display area 2.	

	See, e.g., Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Yoshinori discloses scan and signal wiring that connect to the scan and signal electrodes 6 and 9. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Yoshinori discloses connection pads 3 and 4 that connect to the scan and signal wiring. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
Forming pixel electrodes, and	Yoshinori discloses pixels electrodes 10. See, e.g., Yoshinori, Abstract, Figs 1-3.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Yoshinori discloses equal-interval projection steps 5 are located between the connection pads 3 and 4 and the pixel electrodes 10. Yoshinori teaches, for example, the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area. See, e.g., Yoshinori, ¶ 20. Further, the projection steps or dummy patterns of Yoshinori do not contact the scan and signal wirings. See, e.g., Yoshinori, Figs 1-3.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium,

from the group consisting of aluminum and aluminum alloys.		tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 16		
The method for forming an array substrate for display according to claim 13		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer

wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

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APPENDIX CC16

U.S. PATENT NO. 6, 689, 629 - YOSHINORI IN VIEW OF KUBOTA

Japanese Pub. No. H10-333151 to Yoshinori et al. in view of U.S. Patent No. 6,157,430 to Kubota renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – YOSHINORI	PRIOR ART DISCLOSURE – KUBOTA
An array substrate for display, comprising:	Yoshinori discloses an array substrate 1 including a display area 2. See, e.g., Yoshinori, Abstract, Figs 1-3.	
a layer of an insulating substrate, having an area;	Yoshinori discloses an array substrate 1, including an area. See, e.g., Yoshinori, Abstract, Figs 1-3.	
a thin film transistor array formed on the insulating substrate;	Yoshinori discloses an array of TFTs is formed on the array substrate 1 in the display area 2. See, e.g., Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Yoshinori discloses scan and signal wiring that connect to the scan and signal electrodes 6 and 9. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Yoshinori discloses connection pads 3 and 4 that connect to the scan and signal wiring. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
pixel electrodes, and	Yoshinori discloses pixels electrodes 10. See, e.g., Yoshinori, Abstract, Figs 1-3.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in	Yoshinori discloses equal-interval projection steps 5 are located between the connection pads 3 and 4 and the pixel electrodes 10. Yoshinori teaches, for example, the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area. See, e.g., Yoshinori, ¶ 20. Further,	

contact with any of the wiring.	the projection steps or dummy patterns of Yoshinori do not contact the scan and signal wirings. See, e.g., Yoshinori, Figs 1-3.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium,		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of

tantalum, titanium and alloys thereof.		chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 9		
A meted for forming an array substrate for display, comprising:	Yoshinori discloses an array substrate 1 including a display area 2. See, e.g., Yoshinori, Abstract, Figs 1-3.	
forming a layer of an insulating substrate, having an area;	Yoshinori discloses an array substrate 1, including an area. See, e.g., Yoshinori, Abstract,	

	Figs 1-3.	
forming a thin film transistor array formed on the insulating substrate;	Yoshinori discloses an array of TFTs is formed on the array substrate 1 in the display area 2. See, e.g., Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Yoshinori discloses scan and signal wiring that connect to the scan and signal electrodes 6 and 9. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Yoshinori discloses connection pads 3 and 4 that connect to the scan and signal wiring. See, e.g., Yoshinori, ¶ 20, Figs 1-3.	
Forming pixel electrodes, and	Yoshinori discloses pixels electrodes 10. See, e.g., Yoshinori, Abstract, Figs 1-3.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Yoshinori discloses equal-interval projection steps 5 are located between the connection pads 3 and 4 and the pixel electrodes 10. Yoshinori teaches, for example, the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area. See, e.g., Yoshinori, ¶ 20. Further, the projection steps or dummy patterns of Yoshinori do not contact the scan and signal wirings. See, e.g., Yoshinori, Figs 1-3.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 15		

The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

APPENDIX CC17

U.S. PATENT NO. 6, 689, 629 - TOMOYUKI

Japanese Pub. No. 2000-098909 to Tomoyuki anticipates Claims 1 and 9 of the '629 patent.

Claim 1	**PRIOR ART DISCLOSURE - TOMOYUKI '909**
An array substrate for display, comprising:	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.
a layer of an insulating substrate, having an area;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.
a thin film transistor array formed on the insulating substrate;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Tomoyuki discloses TFT array substrate including wiring, drain lines DLs and gate lines GLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Tomoyuki discloses that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.
pixel electrodes, and	Tomoyuki discloses pixel electrodes 12. See, e.g., Tomoyuki, Figs 1, 5-6.
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Tomoyuki discloses dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figures 1, 5-6. Further, the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel electrode. See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6. The dummy film 5 and 5a would comprise at least 30% of the area or a specified region.
CLAIM 9	
A meted for forming an array substrate for display, comprising:	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.
forming a layer of an insulating substrate, having an area;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.

forming a thin film transistor array formed on the insulating substrate;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Tomoyuki discloses TFT array substrate including wiring, drain lines DLs and gate lines GLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Tomoyuki discloses that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.
forming pixel electrodes, and	Tomoyuki discloses pixel electrodes 12. See, e.g., Tomoyuki, Figs 1, 5-6.
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Tomoyuki discloses dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figures 1, 5-6. Further, the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel electrode. See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6. The dummy film 5 and 5a would comprise at least 30% of the area or a specified region.

APPENDIX CC18

U.S. PATENT NO. 6, 689, 629 - TOMOYUKI IN VIEW OF SONG

Japanese Pub. No. 2000-098909 to Tomoyuki in view of U.S. Patent No. 6,163,356 to Song renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE - TOMOYUKI '909	PRIOR ART DISCLOSURE – SONG
An array substrate for display, comprising:	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
a layer of an insulating substrate, having an area;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
a thin film transistor array formed on the insulating substrate;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Tomoyuki discloses TFT array substrate including wiring, drain lines DLs and gate lines GLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Tomoyuki discloses that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
pixel electrodes, and	Tomoyuki discloses pixel electrodes 12. See, e.g., Tomoyuki, Figs 1, 5-6.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in	Tomoyuki discloses dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figures 1, 5-6. Further, the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel	

contact with any of the wiring.	electrode. See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6. The dummy film 5 and 5a would comprise at least 30% of the area or a specified region.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g.,

molybdenum and alloys thereof.		Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 9		
A meted for forming an array substrate for display, comprising:	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
forming a layer of an insulating substrate, having an area;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
forming a thin film transistor array formed on the insulating substrate;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Tomoyuki discloses TFT array substrate including wiring, drain lines DLs and gate lines GLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Tomoyuki discloses that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
Forming pixel electrodes, and	Tomoyuki discloses pixel electrodes 12. See, e.g., Tomoyuki, Figs 1, 5-6.	
forming dummy conductive	Tomoyuki discloses dummy film	

patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figures 1, 5-6. Further, the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel electrode. See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6. The dummy film 5 and 5a would comprise at least 30% of the area or a specified region.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 13		
The method for forming an array substrate for display		Song discloses a dual layer wiring including aluminum

according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

APPENDIX CC19

U.S. PATENT NO. 6, 689, 629 - TOMOYUKI IN VIEW OF THE '629 APA

Japanese Pub. No. 2000-098909 to Tomoyuki in view of the '629 Admitted Prior Art renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE - TOMOYUKI '909	PRIOR ART DISCLOSURE – THE '629 APA
An array substrate for display, comprising:	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
a layer of an insulating substrate, having an area;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
a thin film transistor array formed on the insulating substrate;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Tomoyuki discloses TFT array substrate including wiring, drain lines DLs and gate lines GLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Tomoyuki discloses that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
pixel electrodes, and	Tomoyuki discloses pixel electrodes 12. See, e.g., Tomoyuki, Figs 1, 5-6.	
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in	Tomoyuki discloses dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figures 1, 5-6. Further, the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel	

contact with any of the wiring.	electrode. See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6. The dummy film 5 and 5a would comprise at least 30% of the area or a specified region.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer

wiring material is selected from the group consisting of molybdenum and alloys thereof.		wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
forming a layer of an insulating substrate, having an area;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
forming a thin film transistor array formed on the insulating substrate;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Tomoyuki discloses TFT array substrate including wiring, drain lines DLs and gate lines GLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of	Tomoyuki discloses that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki,	