production cost can be reduced because no photomask is used. Productivity may be increased by simplifying manufacturing processes."

(3) Comparison

From the well-known documents 1 to 3, an invention of a liquid crystal display, herein after referred to as well-known invention, is found to be well-known before the present application was filed, which liquid crystal comprises a first substrate, and a second substrate facing the first substrate, a columnar spacer for regulating a cell gap between the both substrates which spacer is made from a photosensitive resin only in non-display area of either or both of the first and second substrates , and liquid crystal held in the gap.

The difference between the present invention and the well-known invention is that the present amended invention specifies that the columnar spacer has a hardness (DH) of from 26 to 30, whereas the well-known invention does not have such a specification.

(4) Judgment

(i) In the present specification, the followings are described:

"[0015] As a material for forming the spacers 18, a photosensitive resin is used, particularly the one which gives a spacer having a dynamic hardness defined below of from 26 to 30.

$DH = K \times Pmax/hmax^2$

wherein DH is a dynamic hardness in Kgf/mm, Pmax is a maximum load in kgf, hmax is maximum of total of elastic deformation and plastic deformation in mm, and K is determined from deformation of an instrument-specific indentator. The above formula was derived by conducting dynamic hardness measurement. ...

[0016] The spacer 18 having a DH of from 26 to 30 is neither too soft nor too hard. A spacer with a DH smaller than 26 may allow large change in cell gap when an external force is applied to a liquid crystal display. A spacer with a DH larger than 26 may cause bubbles to form in liquid crystal when a liquid crystal display is cooled to a low

temperature."

The appellant argued in the response of July 31, 2002, that the constant, K, is known as described in section 0014 of Japanese Patent Application Laid-Open No.11-34206, hereinafter referred to as Reference document 1, sections 0016 and 0017 of Japanese Patent Application Laid-Open No.11-296908. In the section 0014 of the Reference document 1, it is described that the dynamic hardness (DH) is defined by the following equation:

$DH = 3.8584 \times P/D^2$

Even if the constant, K, is widely known to be 3.8584, the present amended claim neither defines nor describes K. The description, "a hardness value (DH) of from 26 to 30", alone does not define hardness of the spacer clearly. The aforesaid difference is therefore considered nothing more than a hardness that achieves little change in cell gap caused by an external force applied to a liquid crystal display and no bubble formation at a low temperature, as described in the present specification, section 0016.

(ii) In the reference 1 cited in the decision of the rejection, it is described that, by setting a range of K value, which defines a hardness of a spacer, of from 500 kgf/mm^2 to 1500 kgf/mm^2, a cell gap is well maintained and thereby bubble formation is prevented when temperature of a liquid crystalline display lowers. There is a similar description in the cited reference 2, Japanese Patent Application Laid-Open No.5-80343.

(iii) The K value in the invention of Reference 1 and the DH value in the present invention are determined in different manners. However, the invention of Reference 1 and the present invention commonly intend to prevent bubble formation at a low temperature in a liquid crystal display and to avoid too soft spacers.

Although the spacer used in the liquid crystal display described in Reference 1 is spherical, there is no reason that the technology concerning the spherical spacer cannot be applied to a liquid crystal

display using columnar spacers.

Therefore, a person skilled in the art could easily set a hardness of the columnar spacer in the well-known liquid crystal display to such a degree that a cell gap is not changed a lot and no bubbles are formed at a low temperature as described in Reference 1. The present invention merely expressed the hardness in DH value derived from a parameter different from those for the K value described in Reference 1. To specify the hardness range of from 26 to 30 is mere optimization easily made by a skilled person.

The effect of the present invention is predictable from the reference 1 and aforesaid well-known documents 1 to 3.

As the present amended invention could have been easily made by a person skilled in the art by applying the invention described in Reference 1 to the well-known invention, it is not independently patentable under the Patent Low Art.29(2).

(5) Conclusion

As stated above, the present amendment violates the Patent Low Art. 126(4) applied mutatis mutandis in the Patent Low Art.17^{bis}(5) and therefore is declined under the Patent Low Section 53(1).

3. The present invention

(1) Since the amendment submitted on July 11, 2003 was declined as described above, the present inventions are those amended claims of from 1 to 10 on July 31, 2002, with claim 1, hereinafter referred to as the present invention, being as shown below:

Claim 1. A liquid crystal display comprising:

first and second substrates facing each other,

spacers for regulating a cell gap between the both substrates, said spacers being made from a photosensitive resin and disposed in a non-display region of either or both of the first and the second substrates and having a hardness (DH) of from 26 to 30,and

liquid crystal sandwiched between the first and the second

substrates."

(2) Inventions described in the cited documents

In the document 1 cited in the decision of rejection, Japanese Patent Application Laid-Open No.6-273774, the well-known document 1, Japanese Patent Application Laid-Open No.8-286194, the well-known document 2:Japanese Patent Application Laid-Open No.1-134336, and the well-known document 3,Japanese Patent Application Laid-Open No.9-127513, the invention stated in 2.(2) above is described.

(3) Comparison and Judgment

Compared with the present amended invention, the present invention lacks the limitations that the spacer is disposed only in a non-display region and that the spacer has a columnar shape.

Accordingly, for the almost same reasons as those concerning the present amended invention, a person skilled in the art could easily made the present invention by applying the invention described in the cited document 1 to the well-known inventions.

(4) Closing

As stated above, the present invention could be easily made by a person with skilled in the art based on the invention described in the cited document 1 and well-known technologies and therefore cannot be patented under the Japanese Patent Low Art.29(2).

The appeal examination is closed with the aforesaid conclusion.

January 10, 2006

Trial examiner-in-chief	Yoshinori Hirai
Trial examiner	Yoshito Inazumi
Trial examiner	Toshimitsu Suzuki

Teaching based on the Administrative Case Litigation Law Art.46

A low suit against this trial decision can be filed in 30 days,

or 30 days plus additional period, if granted, from the date of transmittal of the trial decision with the director of the Japanese Patent Office as a defendant.

[Class of appeal decision] P18 .121-Z (G02F)

Additional period of 90 days are granted for filing the action against the trial decision.

Our Comments

(i) Before giving our comments, we would like to mention that criterion for inventive step is severer than before. One reason for this is the IP high court established on April 1, 2005, as a special branch of the Tokyo High Court for intellectual property cases. The court tends to employ severer criterion than the Japanese Patent Office which then follows the court, so as not their appeal decision to be overturned by the court.

To illustrate this, an example may be useful.

Suppose an invention which is a combination of the limitation A with B, A+B. The limitation A is disclosed in document 1 and B in document 2. Both documents 1 and 2 relate to the same technical field.

In order for the invention A+B to be held nonobvious, there should be something which prevents a skilled person from combining A with B, for example, description in the document 1 that B adversely affects A.

Previously, criterion was that there must be some suggestion or motivation either in the documents or in the knowledge generally available to a skilled person to combine teachings of the documents.

(ii) The severer criterion is seen in the present decision, (4) Judgment, (iii):

> There is no reason that the technology concerning a spherical spacer disclosed in the reference 1 cannot be applied to a columnar spacer.

The above judgment was made though none of the references suggests combining the columnar spacer with the dynamic hardness.

This severer criterion is current big issue in the Japanese patent practice.

(iii) You may rebut the decision by arguing an unexpected advantages of the combination of the columnar spacer with the Dynamic Hardness. In the appeal brief, we argued that the present DH value simulates actual pressure applied to the columnar spacer better than the K value

described in the cited document 1 which is derived theoretically. However, it is rejected in the appeal decision.

(iv) Under these circumstances, estimated winning rate of the low suit is very low and therefore filing a low suit against the decision is not recommended.

(v) The other things to note

It is allowed to cite a document which has not been cited in examination process, if the document is used to show well-known technology at the time of the filing of an application in question.

Regarding (4) Judgment, (i), the 3rd paragraph, the K value was deleted from the original claim 1 in response to the first office action, rejecting claim 1 for the reason that definitions of K, Pmax, and hmax are unclear. In the response, the applicant argued that these parameters are known at the time of the filing of the present application, citing Japanese Patent Application Laid-open No.11-34206, and No.11-296908.

審決

不服２００３－１３３４０

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平成１１年特許願第１２２９２３号「液晶表示装置」拒絶査定不服審判事件〔平成１２年１１月２４日出願公開、特開２０００－３２１５８０〕について、次のとおり審決する。

結　論

本件審判の請求は、成り立たない。

理　由

１　手続の経緯

本願は、平成１１年４月２８日の出願であって、平成１５年４月７日付で拒絶査定がなされ、これに対し、平成１５年７月１１日付で拒絶査定に対する審判請求がなされるとともに同日付で特許法第１７条の２第１項第３号の規定による手続補正がなされたものである。

２．平成１５年７月１１日付の手続補正についての補正却下の決定
［補正却下の決定の結論］
平成１５年７月１１日付の手続補正を却下する。
［理由］
（１）補正の内容
本件補正は、特許請求の範囲の請求項１を、
「【請求項１】対向させて配設された第１基板及び第２基板と、
該第１基板と第２基板のいずれか一方又は双方の非表示領域にのみ配設され、該両基板の間のセルギャップを規制する感光性樹脂から成り、硬さ値（ＤＨ）が２６～３０である柱状のスペーサーと、
前記第１基板と第２基板の間に介在させられる液晶と
を含む液晶表示装置。」
とする補正を含むものである。

上記補正は、スペーサの形状及び配置を、さらに具体的に限定しようとするものであり、特許請求の範囲の減縮を目的とするものに該当するので、本件補正後の請求項１に記載された発明（以下、「本願補正発明」という。）が特許出願の際独立して特許を受けることができるものであるかについて検討する。

（２）刊行物記載の発明
原査定の拒絶理由に引用したこの出願前公知の刊行物１：特開平６－２７３７７４号公報には、下記の事項が記載されている。
「【０００４】【発明が解決しようとする課題】
本発明は、上記問題点を解決するためになされたものであり、プラスチックスペーサーを高硬度・高弾性率とすることによりギャップ制御を容易にし、単位面積当りのスペーサー散布個数の低減を図り、表示品質を向上させることができる液晶表示素子用スペーサーおよびそれを用いた液晶表示素子を提供することを目的とする。・・・
【００１９】まず、スペーサーの硬度を規定するＫ値について説明する。・・・
【００２４】このＫ値は球体の硬さを普遍的かつ定量的に表すものである。このＫ値を用いることにより、スペーサーの好適な硬さを定量的、かつ一義的に表すことが可能となる。・・・
【００２６】Ｋ値が１５００ｋｇｆ／ｍｍ^{2}を超えるスペーサーでは硬すぎて、液晶表示素子を作製する際に液晶配向制御膜面に傷を付けるおそれがあり、さらに作製された液晶表示素子において、温度が低下した際に液晶の収縮に対してスペーサーの圧縮変形が生じ難くいため液晶セル中に減圧に起因

する気泡が発生する。
【００２７】K値が５００ｋｇｆ／ｍｍ^{2}未満のスペーサーでは硬度が不充分であり、基板のギャップコントロールが困難となるおそれがある。そのため、スペーサーの単位面積当りの散布個数を多くする必要があり、表示のコントラストが低下するおそれがある。」

技術水準を示す文献である特開平８－２８６１９４号公報（以下、「周知文献１」という。）には、下記の事項が記載されている。
「【００４５】（スペサーの形成）合成例２で調製した感光性樹脂組成物（水分散塗料）を用い、・・・均一な膜厚５　５μｍを有する感光性樹脂組成物膜が得られた。次に、遮光部の一部分のみを１２μｍ径の光で露光するパターンを有するホトマスクを通して、上記感光性樹脂組成物膜に、３６５ｎｍの紫外線を１５０ｍＪ／ｃｍ^{2}の強度で照射した。感光性樹脂組成物膜を濃度２．４重量％のテトラメチルアンモニウムヒドロキシド水溶液で現像したところ、遮光部の一部分のみに感光性樹脂組成物のスペーサーがパターニングされた。スペーサーがパターニングされたカラーフィルター基板を純水で洗浄した後、更に感光性樹脂組成物からなるスペーサーを１８０℃で２時間加熱硬化した。その結果、圧縮強度が高くかつ弾性のある高さ５μｍの樹脂製スペーサーが得られた。・・・
【００４６】（液晶表示装置の組立）以上のようにして得られた樹脂製スペーサーを有するカラーフィルター基板を用い、電極基板用の透明導電膜を形成した後、両基板間にＴＦＴ用液晶組成物であるＬＩＸＯＮ５００５（商品名、チッソ（株）製）を充填してＴＦＴ液晶表示装置を組み立てたところ、セルギャップのバラツキが少なく、その結果表示ムラ、色ムラ、干渉縞などのない表示装置が得られた。またこのＴＦＴ液晶表示装置は、有効表示部分にスペーサーがないため、コントラストの低下、光抜け、スペーサー界面での配向欠陥による画質低下等のない良質な画質を表示した。図１は、上記のようにして得られた液晶表示装置の部分拡大縦断面図である。液晶表示装置１１は、図５に示したスペーサーを有するカラーフィルター基板５ａと、カラーフィルターを有しない他の電極基板１２とをスペーサー１０を介して一定の間隔に保ち、両基板間に液晶材料１３を充填したものである。」
また、スペーサーを付与したカラーフィルター基板の部分拡大断面図である図５には、遮光部８上に柱状スペーサー１０が形成されたものが見て取れる。

上記によれば、周知文献１には、
「圧縮強度が高くかつ弾性のある感光性樹脂組成物からなる柱状スペーサーを有するカラーフィルター基板５ａと、カラーフィルターを有しない他の電極基板１２とを前記柱状スペーサー１０を介して一定の間隔に保ち、両基板

間に液晶材料１３を充填した、有効表示部分にスペーサーがない液晶表示装置。」の発明が記載されている。

同じく技術水準を示す文献である特開平１－１３４３３６号公報（以下、「周知文献２」という。）には、下記の事項が記載されている。
「（１）１組の電極付基板と、前記電極付基板上に形成された配向膜と、スペーサとから構成され、前記スペーサが少なくとも一方の前記電極付基板上に形成された前記配向膜上に固定され、前記スペーサが島状に配置されることを特徴とした液晶表示装置。」（特許請求の範囲請求項１）、
「スペーサ１１は所定の数を自在に形成でき、スペーサの所定の押圧力に見合うだけの所定数のスペーサを形成できる。・・・以上のように配向膜上の画素部以外にスペーサを形成することができ、・・・画質を向上させるという効果を有する。」（４頁左上欄１９行～同頁右上欄９行）
また、第１図（ａ）～（ｄ）及びこれに関する明細書の記載（３頁左下欄１行～同頁右下欄１７行）から、電極付基板２の配向膜上に感光性ポリイミド３を塗布し、所定パターンで露光した後、露光されない部分を除去することによりスペーサ５が形成されることが見て取れ、第１図及び第３図には、スペーサが柱状であることが、また第５図には、１組の電極付基板間に液晶が介在する液晶表示装置の断面図が見て取れる。

上記によれば、周知文献２には、
「１組の電極付基板と、感光性ポリイミドからなる柱状のスペーサと、前記１組の電極付基板間に介在する液晶とから構成され、前記スペーサが少なくとも一方の前記電極付基板上の画素部以外に形成された液晶表示装置。」の発明が記載されている。

同じく技術水準を示す文献である特開平９－１２７５１３号公報（以下、「周知文献３」という。）には、下記の事項が記載されている。
「【請求項１】第１の電極及び第１の遮光手段を有する第１の電極基板と、
第２の電極及び第２の遮光手段を有し前記第１の電極基板に間隙を隔てて対向する第２の電極基板と、
感光性樹脂からなり前記第１の遮光手段及び前記第２の遮光手段の交差位置に設けられ前記間隙を一定に保持する柱状の間隙保持手段と、
前記間隙に挟持される液晶組成物と、を具備する事を特徴とする液晶表示素子。」、
「【００７２】
【発明の効果】以上説明したように本発明によれば、電極基板上に設けられるマスクとして、感光性樹脂を露光し現像することにより、コストの上昇を招くことも無く、容易かつ短時間で、非画像形成部にのみ設けられる柱状スペ

ーサにて、両電極基板間の間隙を均一に保持でき、従来両電極基板間にスペーサを設ける事により生じいていたコントラストの低下や、表示むらを生じることがなく、表示品位を向上出来、しかもフォトマスクを使わないのでコストを低減出来、更に製造工程の簡素化により生産性の向上を図れる。」

（３）対比

上記周知文献１～３からは、「対向させて配設された第１基板及び第２基板と、該第１基板と第２基板のいずれか一方又は双方の非表示領域にのみ配設され、該両基板の間のセルギャップを規制する感光性樹脂から成る柱状のスペーサーと、前記第１基板と第２基板の間に介在させられる液晶とを含む液晶表示装置」が、本願出願前周知（以下、「周知発明」という。）であることが分かる。

そこで、本願補正発明と周知発明とを対比すると、両者は、上記の点で一致し、次の点で相違する。

相違点：

柱状のスペーサーについて、本願補正発明では、「硬さ値（ＤＨ）が２６～３０である」と規定しているのに対して、周知発明では、このような規定がない点。

（４）判断

(ア) 本願補正明細書には、

「【００１５】スペーサー１８を形成する材質には感光性樹脂が用いられ、その中でも形成したスペーサー１８が次の条件を満たす感光性樹脂が用いられる。すなわち、スペーサー１８は、次式

$DH = K \times Pmax / hmax^2$

ＤＨ：硬さ値（Ｋｇｆ／ｍｍ^2）

Ｐｍａｘ：最大荷重（Ｋｇｆ）

ｈｍａｘ：弾性変形量及び塑性変形量を合計した最大変位量（ｍｍ）

により求めた硬さ値（ＤＨ）が２６～３０となる感光性樹脂が選定される。ここで、定数Ｋは、装置固有の圧子の変位量より求めた値である。また、この式は、ダイナミック硬度試験を行うことより導いたものである。・・・

【００１６】硬さ値（ＤＨ）が２６～３０の範囲にあるスペーサー１８は、硬くも柔らかくもなく、硬さ値（ＤＨ）が２６未満のときは、液晶表示装置の外部から力が加えられた際のセルギャップの変化量が大きく、画質が変化し易く問題となる。また、硬さ値（ＤＨ）が３０を越えるときは、液晶表示装置が低温冷却されたときなどに、液晶中に低温気泡が発生することとなり、不都合となる。」と記載されている。

また、請求人は、上記定数Ｋについて、平成１４年７月３１日付の意見書

において、特開平１１－３４２０６号公報（以下、「参考文献１」という。）の段落番号００１４や特開平１１－２９６９０８号公報の段落番号００１６，００１７に記載されているように公知の技術内容である旨主張している。そして、上記参考文献１の段落番号００１４には、ダイナミック硬度ＤＨは、ＤＨ＝３．８５８４×Ｐ／Ｄ^{2}の式で定義されると記載されている。

仮に、本願補正発明の硬さ値（ＤＨ）を求めるための定数Ｋが上記のとおり３．８５８４であることが広く知られていたとしても、本願補正発明には定数Ｋが定義づけられているわけでも記載されているわけでもないから、本願補正発明の「硬さ値（ＤＨ）が２６～３０」との記載だけでは、スペーサの硬さが明確に規定されることにはならないから、上記相違点が示すのは、本願補正明細書の【００１６】に記載されているように、『液晶表示装置の外部から力が加えられた際のセルギャップの変化量が大きくなく、液晶表示装置が低温冷却されたときなどに、液晶中に低温気泡が発生することがない』という程度の意味と理解される。

（イ）これに対し、原査定の拒絶理由に引用した上記刊行物１には、スペーサーの硬度を規定するＫ値を所定の範囲（５００ｋｇｆ／ｍｍ^{2}～１５００ｋｇｆ／ｍｍ^{2}）とすることによって、基板のギャップコントロールを良好にし、液晶表示装置の温度が低下した際に気泡が発生するのを防止する（前掲の【００２６】、【００２７】参照。）と記載されている。（同じく、原査定の拒絶理由に引用した刊行物：特開平５－８０３４３号公報にも、同様の記載がある。）

（ウ）上記刊行物１のＫ値と本願補正発明の硬さ値（ＤＨ）とでは、測定方法が異なるとしても、両者とも、液晶表示装置作製後の、低温気泡の発生を問題にしており、また柔らかすぎる点も問題視されているのであるから、課題が共通している。

そして、刊行物１記載の液晶表示装置のスペーサが球状のものであるとしても、それに関する技術を柱状スペーサを用いた液晶表示装置に適用できない理由はない。

してみると、従来周知の液晶表示装置における柱状スペーサの硬度を、刊行物１に記載されたような、セルギャップの変化量が大きくならず、低温気泡が発生することのない程度のものとすることは当業者が容易に想到し得たものであって、本願補正発明は、その硬度を刊行物１記載のＫ値とは異なるパラメータから導き出された硬さ値（ＤＨ）で表わしたにすぎないものであるから、その数値範囲を２６～３０と規定することは、当業者が適宜設定し得る程度のことにすぎない。

そして、本願補正発明によってもたらされる効果は、刊行物１記載の事項及び上記周知文献１～３から予測し得る程度のものである。

したがって、本願補正発明は、刊行物１に記載された発明を周知発明に適用することにより当業者が容易に発明をすることができたものであるから、特許法第２９条第２項の規定により、特許出願の際独立して特許を受けることができないものである。

（５）むすび

以上のとおり、本件補正は、特許法第１７条の２第５項において準用する同法第１２６条第４項の規定に違反するものであるから、特許法第１５９条第１項で準用する特許法第５３条第１項の規定により却下されるべきものである。

３．本願発明について

（１）本願発明

平成１５年７月１１日付の手続補正は上記のとおり却下されたので、本願の請求項に係る発明は、平成１４年７月３１日付手続補正書によって補正された明細書及び図面の記載からみて、その特許請求の範囲の請求項１～１０に記載された事項によって特定されるものであるところ、請求項１に係る発明は次のとおりのものである。

「【請求項１】　対向させて配設された第１基板及び第２基板と、該第１基板と第２基板のいずれか一方又は双方の非表示領域に配設され、該両基板の間のセルギャップを規制する感光性樹脂から成り、硬さ値（ＤＨ）が２６～３０であるスペーサーと、前記第１基板と第２基板の間に介在させられる液晶とを含む液晶表示装置。」（以下、「本願発明」という。）

（２）引用例記載の発明

原査定の拒絶の理由に引用したこの出願前公知の刊行物１：特開平６－２７３７７４号公報、並びに、周知文献１：特開平８－２８６１９４号公報、周知文献２：特開平１－１３４３３６号公報及び周知文献３：特開平９－１２７５１３号公報には、上記２．（２）刊行物記載の発明に摘記した事項がそれぞれ記載されている。

（３）対比・判断

本願発明は、本願補正発明に比べて、スペーサの配置を非表示領域のみに限定し、スペーサの形状を柱状とした点を欠くものである。

したがって、本願発明は、上記スペーサの配置と形状に関する部分を除き、上記本願補正発明に対するとほぼ同様の理由により、刊行物１に記載された発明を周知発明に適用することにより当業者が容易に想到し得たものである。

（４）むすび

以上のとおり、本願発明は、刊行物１に記載された発明及び周知技術に基づいて当業者が容易に発明をすることができたものであるから、特許法第２９条第２項の規定により特許を受けることができない。

よって、結論のとおり審決する。

平成１８年　１月１０日

審判長　特許庁審判官　平井　良憲
特許庁審判官　稲積　義登
特許庁審判官　鈴木　俊光

（行政事件訴訟法第４６条に基づく教示）

この審決に対する訴えは、この審決の謄本の送達があった日から３０日（附加期間がある場合は、その日数を附加します。）以内に、特許庁長官を被告として、提起することができます。

〔審決分類〕Ｐ１８　１２１－Ｚ　（Ｇ０２Ｆ）

出訴期間として９０日を附加する。

上記はファイルに記録されている事項と相違ないことを認証する。
認証日　平成18年 1月19日　審判書記官　児玉　輝子

【書類名】　刊行物等提出書
【提出日】　平成17年12月19日
【あて先】　特許庁長官　殿
【事件の表示】
　【出願番号】　平成11年特許願第122923号
　【出願公開番号】　特開2000-321580
【提出者】
　【住所又は居所】　省略
　【氏名又は名称】　省略
【提出する刊行物等】　刊行物１：特開平９－１４６０９７号公報　刊行物２：特開平１１－１５３８１６号公報　刊行物３：特開平１１－２４２２１１号公報
【提出の理由】　（１）特願平１１－１２２９２３号（特開２０００－３２１５８０号公報）の手続補正書（平成１５年７月１１日提出）による補正後の請求項１～４に記載の各発明は、上記刊行物１～３に記載された発明であり、請求項６に記載の発明は、上記刊行物３に記載された発明であるため、特許法第２９条第１項第３号、若しくは特許法第２９条の２の規定に該当し、拒絶されるべきものである。　本願発明は、本願の詳細な説明の記載が、当業者がその実施をすることができる程度に明確かつ十分に記載したものではないため、特許法第３６条第４項第１号の規定に該当し、拒絶されるべきものである。　本願発明は、本願の特許請求の範囲の記載が、特許を受けようとする発明が明確ではないため、特許法第３６条第６項第２号の規定に該当し、拒絶されるべきものである。　以下、これらの理由について説明する。　（２）本願発明の特徴　本願の請求項１～８には、以下の通り記載されている。〔請求項１〕　対向させて配設された第１基板及び第２基板と、　該第１基板と第２基板のいずれか一方又は双方の非表示領域にのみ配設され、該両基板の間のセルギャップを規制する感光性樹脂から成り、硬さ値（ＤＨ）が２６～３０である柱状のスペーサーと、　前記第１基板と第２基板の間に介在させられる液晶とを含む液晶表示装置。〔請求項２〕　対向させて配設された第１基板及び第２基板と、　該第１基板と第２基板のいずれか一方又は双方の非表示領域にのみ配設され、該両基板の間のセルギャップを規制する感光性樹脂から成り、塑性変形硬さ（ＨＶ）が３８～４６である柱状のスペーサーと、　前記第１基板と第２基板の間に介在させられる液晶とを含む液晶表示装置。〔請求項３〕　対向させて配設された第１基板及び第２基板と、　該第１基板と第２基板のいずれか一方又は双方の非表示領域にのみ配設され、該両基板の間のセルギャップを規制する感光性樹脂から成り、硬さ値（ＤＨ）が２６～３０であり、且つ塑性変形硬さ（ＨＶ）が３８～４６である柱状のスペーサーと、　前記第１基板と第２基板の間に介在させられる液晶とを含む液晶表示装置。〔請求項４〕前記スペーサーの弾性係数が１００～５００ｋｇ／ｍｍ▲２▼である請求項１～３のいずれか１項記載の液晶表示装置。〔請求項５〕前記スペーサーの線膨張係数が前記液晶の単位面積当たりの体積膨張係数と等しい請求項１～４のいずれか１項記載の液晶表示装置。〔請求項６〕　前記スペーサーが、次式　柱占有率＝（柱下底面積×柱密度／絵素面積）×１００　柱密度＝全柱数／全絵素数で現される柱占有率が０．０５～０．８６％である、請求項１

～５のいずれか１項記載の液晶表示装置。〔請求項７〕　前記スペーサーの、両基板と平行をなす面の形状が矩形、三角形、または多角形であり、上底の一辺と下底の一辺との比が５０～９０％、または該面が円形、楕円、または長円形であり、上底の直径もしくは長径と下底の直径もしくは長径との比が５０～９０％である、請求項１～６のいずれか１項記載の液晶表示装置。〔請求項８〕　前記スペーサーの上底の一辺の長さ又は直径もしくは長径は、該スペーサの最大高に０．９をかけた位置における下底と水平な面の一辺の長さ又は直径もしくは長径である請求項７に記載の液晶表示装置。　本願発明は、本願の明細書段落（０００９）に記載のように、配設位置が一定しない球状スペーサー等の課題を解決するとともに、低温発泡の発生を抑制することができ、しかも局所荷重に対して耐性のある光感光性樹脂材料から成るスペーサーを備えた液晶表示装置の提供を課題としてなされたものである。　本願の明細書段落（００４２）には、「本発明に係る液晶表示装置のスペーサーは、感光性樹脂により所定の適切な箇所に形成され、しかも所定の硬さ値や塑性変形硬さなどの物性値あるいは形態を備えて構成されている。このため、局所荷重に対して容易に押しつぶされて破壊してしまうことはなく、元の状態に回復して、セルギャップをほぼ一定に支持することができる。また、低温発泡に対しては、液晶表示装置が低温に曝されたとしても、セルギャップ内の液晶の収縮に伴い、外部圧力などによりスペーサーも収縮するため、セルギャップ内に真空部ができることはなく、低温発泡が生じることはない。」旨の効果が示されている。　（３）本願の請求項１～４、６に記載の発明が特許法第２９条第１項第３号、若しくは特許法第２９条の２の規定に該当する理由　本願の請求項１では、対向させて配設された第１基板及び第２基板と、該第１基板と第２基板のいずれか一方又は双方の非表示領域にのみ配設され、該両基板の間のセルギャップを規制する感光性樹脂から成り、硬さ値（ＤＨ）が２６～３０である柱状のスペーサーと、第１基板と第２基板の間に介在させられる液晶とを含む液晶表示装置である旨が規定されている。　本願の明細書段落（００３３）、（００３４）以下に記載の実施例では、柱状のスペーサーを構成する方法として、「ガラス基板を用いて、従来の製法によりアレイ基板を作成した。このアレイ基板に柱状スペーサーを形成するのにあたり、その下地として、ＳｉＮｘから成るパッシベーション膜を、画素電極を除いて被着した。そのパッシベーション膜の上に感光性樹脂層をＪＮＰＣ－４３（ＪＳＲ社製）を用いて、膜厚５．５μｍで均一に塗布し、１２０℃で３分間、プレベークした。　次いで、スペーサーの柱占有率が０．１９％で、配設位置が非表示領域になるように設定されたフォトマスクを用い、光源としてフィルター無し（ブロードバンド）のものを用い、エネルギー３００ｍＪで露光した。そして、現像液として０．２％ＴＭＡＨ水溶液（東京応化製）を用い、現像温度は室温で、現像時間６０秒で現像した。その後、焼成温度２３０℃で焼成時間として２０分間、焼成して、スペーサーを形成した。」旨が記載されている。　一方、刊行物１の明細書段落（００６２）～（００７４）、（００８２）及び図４（ａ）、（ｂ）には、２つのガラス基板１、２が対向配置されており、この２つのガラス基板１、２の間隔を規制している柱状のスペーサ１５

を備える変形例１の液晶表示装置が開示されている。　刊行物１の明細書段落（００８２）には、この変形例１の液晶表示装置等においてスペーサ１５を構成する方法として、「変形例１の液晶表示装置と同様な構成で、スペーサ１５…を有する液晶表示装置を実際に作製した。この液晶表示装置の作製においては、次の手順で厚さ１．５μｍのスペーサ１５…を形成した。まず、感光性アクリル樹脂（日本合成ゴム社製－品番ＪＮＰＣ）をスピンコート法で１．５μｍの厚さに形成し、８０℃で３分間焼成する。続いて、フォトマスクを用いて露光および現像し、さらに２００℃で６０分間本焼成を行う。」旨が記載されている。　さらに、刊行物１の明細書段落（００９０）～（００９４）及び図８（ａ）、（ｂ）には、複数画素毎に非画素領域にのみ柱状のスペーサ１５を設けた液晶表示装置が開示されている。そして、刊行物１の明細書段落（００９３）に記載のように、図８（ａ）、（ｂ）に示す液晶表示装置では、柱状のスペーサー１５は、変形例１での手順と同様に形成されるので、上記感光性アクリル樹脂等を用いて構成され得る。　よって、刊行物１には、スペーサーの硬さ値（ＤＨ）が２６～３０の範囲であること以外の本願の請求項１に記載の発明に係る構成、すなわち、対向させて配設された第１基板及び第２基板と、該第１基板と第２基板のいずれか一方又は双方の非表示領域にのみ配設され、該両基板の間のセルギャップを規制する感光性樹脂から成る柱状のスペーサーと、第１基板と第２基板の間に介在させられる液晶とを含む液晶表示装置が明確に開示されている。　ここで、刊行物１に記載の柱状のスペーサ１５は、本願の実施例と同様に感光性アクリル樹脂（日本合成ゴム社製－品番ＪＮＰＣ）を用いて構成され得るため、硬さ値（ＤＨ）が２６～３０の範囲にあるはずである。すなわち、刊行物１には、硬さ値（ＤＨ）が２６～３０の範囲にある柱状のスペーサーも開示されている。　従って、本願の請求項１に記載の発明は、刊行物１に記載された発明であるため、特許法第２９条第１項第３号により拒絶されるべきである。　なお、本願の明細書段落（００２９）には、「感光性樹脂の焼成条件を制御することにより、目的とする物性を得るようにしてもよい。」旨が記載されている。しかしながら、仮に、柱状のスペーサーを構成する際に膜厚や焼成条件等によりスペーサーの硬さ値（ＤＨ）が異なり、硬さ値（ＤＨ）が２６～３０の範囲外になることがあり得るとしても、本願の詳細な説明には、膜厚をどの範囲にすればよいのか、若しくは柱状のスペーサーの焼成条件をどの範囲とすればよいのか等については具体的に記載されておらず、この場合、本願の詳細な説明の記載が当業者にとって本願の請求項１に記載の発明を実施することができないものとなる。　一方、刊行物２の明細書段落（００２４）以下に記載の第１の実施形態では、第１、第２の基板１、２が対向配置されており、この第１、第２の基板１、２の間隔を規制している柱状のスペーサーであるギャップ材６を備える強誘電性液晶パネル１０が開示されている。　刊行物２の明細書段落（００３５）～（００３７）には、この強誘電性液晶パネル１０におけるギャップ材６を構成する方法として、「第１の基板１の電極形成面に、各第１の透明電極４を被覆するように、アクリル系のネガ型感光樹脂（例えばＪＮＰＣ－４３：日本合成ゴム社製）をスピンナ法を用いて５５０～６５０ｒｐｍの回転数

で塗布し、８０℃の温度で約１分間炉内でプリベークする。それによって、厚さが約１．７μｍの感光樹脂膜を形成する。　その後、多数の十字状のギャップ材６の配置に対応するパターンを形成したフォトマスクを位置合わせして、第１の基板１上の感光樹脂膜に重ね合わせ、露光機で波長が３６０ｎｍの光によって露光する。　その後、この第１の基板１を現像液（例えば、ＭＦ－３１２：シプレイマイクロジャパン（株）製）の中に入れ、感光樹脂膜の光に照射されなかった部分を落とす。さらに、この第１の基板１を１９０℃～２００℃の窒素雰囲気中の炉内に１時間投入し、ポストベイクを施す。このようにして、図５に示すような多数の十字状のギャップ材６を、第１の基板１上に固定して容易に形成することができる。」旨が記載されている。　よって、刊行物２には、スペーサーの硬さ値（ＤＨ）が２６～３０の範囲であること、並びにスペーサーが非画素領域にのみ配置されていることを除く本願の請求項１に記載の発明に係る構成が開示されている。　ここで、刊行物２に記載のギャップ材６は、本願の実施例と同様のアクリル系のネガ型感光樹脂（ＪＮＰＣ－４３：日本合成ゴム社製）を用いて構成され得るため、硬さ値（ＤＨ）が２６～３０の範囲にあるはずである。すなわち、刊行物２には、硬さ値（ＤＨ）が２６～３０の範囲にある柱状のスペーサーも開示されている。　さらに、柱状のスペーサーが第１基板と第２基板のいずれか一方又は双方の非表示領域にのみ配設する構成は、上記刊行物１に記載のように、本願出願前に周知の技術的事項にすぎない。　現行の特許・実用新案審査基準第ＩＩ部第３章特許法第２９条の２「２．３他の出願の当初明細書等に記載された発明または考案」においては、引用例の当初明細書に記載された発明または考案とは、当初明細書に記載されている事項だけでなく、記載されているに等しい事項から把握される発明または考案をいうとされており、「記載されているに等しい事項」とは、記載されている事項から引用例の出願時における周知技術を参酌することにより導き出されるものをいうものとするとされている。　すなわち、本願の請求項１に記載の発明は、刊行物２に記載の強誘電性液晶パネル１０において、ギャップ材６を非画素領域にのみ配置する周知の技術的事項が付加されたものにすぎない。　従って、本願の請求項１に記載の発明は、刊行物２に記載されているに等しいものであるので、特許法第２９条の２により拒絶されるべきである。　他方、刊行物３の明細書段落（００９０）以下に記載の実施例９には、ガラス基板１、２が対向配置されており、この２つのガラス基板１、２の間隔を規制している柱状スペーサ７を備える液晶表示装置が開示されている。この液晶表示装置では、柱状スペーサ７は、絵素領域４０を囲むように、すなわち非画素領域であるブラックマトリックス４１部分にのみ配置されている。　さらに、刊行物３の明細書段落（００９０）には、柱状スペーサ７を構成する方法として、「コーニング社製７０５９ガラス基板１の上にＩＴＯからなる厚み１００ｎｍの透明電極３を形成し、この上に膜厚が５μｍになるようにＪＮＰＣ－４３（ＪＳＲ社製）をスピンコート法で塗布した。ホットプレート上で８０℃／３分間加熱した後、図１６（ａ）および（ｂ）に示すように柱状スペーサ７の長さの一辺がｄｓであり、隣の柱状スペーサとの間隔Ｄが表１のように異なるマスクパターンを用いて、マスク

越しにコンタクト露光を６０秒行った。露光時の照度は３６５ｎｍで１０ｍＷ／ｃｍ▲２▼であった。これを現像液ＣＤ（１５％希釈、２５℃）で１５０秒現像し、純水シャワーで１２０秒間リンスを行った後、２００℃の循環オーブンで１時間ポストベークを行い柱状スペーサ７を形成した。」旨が記載されている。　よって、刊行物３には、スペーサーの硬さ値（ＤＨ）が２６～３０の範囲であること以外の本願の請求項１に記載の発明に係る構成が明確に開示されている。　ここで、刊行物３に記載の柱状スペーサ７は、本願の実施例と同様のＪＮＰＣ－４３（ＪＳＲ社製）を用いて構成され得るため、硬さ値（ＤＨ）が２６～３０の範囲にあるはずである。すなわち、刊行物３には、硬さ値（ＤＨ）が２６～３０の範囲にある柱状のスペーサーも開示されている。従って、本願の請求項１に記載の発明は、刊行物３にも記載されているので、特許法第２９条の２により拒絶されるべきである。

本願の請求項２では、スペーサーの塑性変形硬さ（ＨＶ）が３８～４６である旨が限定されており、本願の請求項３では、スペーサーの硬さ値（ＤＨ）が２６～３０であり、且つ塑性変形硬さ（ＨＶ）が３８～４６である旨が限定されており、本願の請求項４では、スペーサーの弾性係数が１００～５００ｋｇ／ｍｍ▲２▼である旨が限定されている。　しかしながら、刊行物１～３に記載のスペーサーは、本願の実施例と同様のＪＮＰＣ、若しくはＪＮＰＣ－４３（ＪＳＲ社製）を用いて構成され得るため、硬さ値（ＤＨ）が２６～３０であり、塑性変形硬さ（ＨＶ）が３８～４６であり、弾性係数が１００～５００ｋｇ／ｍｍ▲２▼であるはずである。すなわち、刊行物１～３には、硬さ値（ＤＨ）が２６～３０であり、塑性変形硬さ（ＨＶ）が３８～４６であり、もしくは弾性係数が１００～５００ｋｇ／ｍｍ▲２▼であるスペーサーが開示されている。　従って、本願の請求項２～４に記載の各発明は、刊行物１に記載された発明であるため、特許法第２９条第１項第３号により、若しくは刊行物２、３に記載されているので、特許法第２９条の２により拒絶されるべきである。　なお、仮に、柱状のスペーサーを構成する際に膜厚や焼成条件等によりスペーサーの硬さ値（ＤＨ）、塑性変形硬さ（ＨＶ）や弾性係数が異なり、本願の請求項２～４に記載の範囲外になることがあり得るとしても、上述のように、本願の詳細な説明には、膜厚をどの範囲にすればよいのか、若しくは柱状のスペーサーの焼成条件をどの範囲とすればよいのか等については具体的に記載されておらず、この場合、本願の詳細な説明の記載が当業者にとって本願の請求項２～４に記載の発明を実施することができないものとなる。　本願の請求項６では、以下の式で示されるスペーサーの柱占有率が０．０５～０．８６％である旨が限定されている。柱占有率＝（柱下底面積×柱密度／絵素面積）×１００　柱密度＝全柱数／全絵素数　他方、刊行物３の明細書段落（００３３）には、「柱状スペーサを複数有し、互いに隣接する該柱状スペーサの間隔をＤ、該柱状スペーサの断面形状が四角形の場合、該四角形の一辺の長さをｄｓとし、該柱状スペーサの断面形状が円形の場合、該円形の直径をｄｓとしたとき、長さの比ｙ（＝Ｄ／ｄｓ）が、０．１≦ｙ≦４．４９ｅ▲－０．０６０７ｄｓ▼＋１．５の関係にあることが好ましい。」旨が記載されている。　ここで、刊行物１に記載の長さの比ｙ（＝Ｄ／ｄｓ）が、０．１≦ｙ

≦４．４９ｅ▲－０．０６０７ｄｓ▼＋１．５の関係にある場合には、スペーサーの柱占有率は０．０５～０．８６％の範囲に属するはずである。　従って、本願の請求項６に記載の発明は、刊行物３に記載されているので、特許法第２９条の２により拒絶されるべきである。　（４）本願の発明の詳細な説明の記載が、特許法第３６条第４項第１号の規定に該当する理由、若しくは本願の特許請求の範囲の記載が、特許法第３６条第６項第２号の規定に該当する理由　本願の請求項４では、スペーサーの弾性係数が１００～５００ｋｇ／ｍｍ▲２▼である旨が限定されている。本願の明細書段落（００２７）には、スペーサの弾性係数が１００～５００ｋｇ／ｍｍ▲２▼の範囲である場合に、「局所荷重に対してスペーサー１８が容易に破壊されることはなく、また、温度低下に伴う液晶２０の収縮によりセルギャップ１６の間隔が収縮して、スペーサー１８が圧縮力を受けても、スペーサー１８は十分に収縮するため、低温発泡が生じることはない。」旨の効果が記載されているが、本願の具体的な実施例では弾性係数が評価されておらず、このような効果は、具体的な実施例により裏付けられていない。　本願の請求項５では、スペーサーの線膨張係数が液晶の単位面積あたりの体積膨張係数と等しい旨が限定されている。　本願の明細書段落（００２８）には、「スペーサー１８の線膨張係数が液晶２０の単位面積当たりの体積膨張係数より極めて大きい場合、液晶表示装置１０が高温に曝されたとき、スペーサー１８が膨張してセルギャップ１６内に真空の空間が生じる恐れがある。一方、スペーサー１８の線膨張係数が液晶２０の単位面積当たりの体積膨張係数より極めて小さい場合、液晶表示装置１０が低温に曝されたとき、スペーサー１８以上に液晶２０が収縮するため、低温発泡が生じる恐れがある。そこで、スペーサー１８の線膨張係数は液晶２０の単位面積当たりの体積膨張係数とほぼ等しいか、近似する値であることが好ましい。」旨が記載されているが、本願の具体的な実施例では体積膨張係数が評価されておらず、このような効果は、具体的な実施例により裏付けられていない。　本願の請求項６では、スペーサーの柱占有率が０．０５～０．８６％である旨が限定されている。　本願の明細書段落（００２３）には、「柱占有率の範囲が０．０５～０．８６％であるとき、柱状スペーサー１８は局所荷重に対して押しつぶされることなく充分に耐えることができる。また、低温に曝された場合においても、液晶の収縮に伴いセルギャップ１６内に生じる負圧に応じて、スペーサー１８は圧縮されて縮む結果、セルギャップ１６内に低温発泡が生じることはない。」旨が記載されているが、本願の具体的な実施例では柱占有率が記載されておらず、このような効果は、具体的な実施例により裏付けられていない。　本願の請求項７では、スペーサーの、両基板と平行をなす面の形状が矩形、三角形、または多角形であり、上底の一辺と下底の一辺との比が５０～９０％、または該面が円形、楕円、または長円形であり、上底の直径もしくは長径と下底の直径もしくは長径との比が５０～９０％である旨が限定されている。　本願の明細書段落（００２４）には、「柱状スペーサー１８の基板と平行をなす面の形状が矩形を成す場合、スペーサー１８の上底の一辺と下底の一辺との比が５０～９０％であり、又は、同じくその面の形成が円形を成す場合、スペーサー１８の上底の直径と下底の

直径との比が５０～９０％であるのが好ましい。スペーサー１８の一辺又は直径の比が５０～９０％の範囲内であれば、以下の不具合・問題を最小限にとどめることができる。すなわち、その比が５０％未満であると、液晶表示装置における開口率を極端に失ってしまうこととなり、またその比が９０％を越えると、柱を形成する工程で柱の形状が逆テーパーになりやすく、以降のセル工程で柱がくずれるなどの不具合を生じて、好ましくない。」旨が記載されている。　しかしながら、上底の一辺と下底の一辺との比が５０％未満であると、上底の一辺または下底の一辺のいずれかが極端に短くなるが、このことが液晶表示装置における開口率を極端に失うとは一概に言えない。すなわち、液晶表示装置における開口率は、上底の一辺と下底の一辺との比ではなく、柱状スペーサーの縦断面形状の総面積等に依存するはずである。他方、上底の一辺と下底の一辺との比が９０％を超えると、上底の一辺と下底の一辺とがほぼ等しくなるが、この場合、逆テーパー状のテーパーの傾斜が小さくなるはずであり、以降のセル工程で柱がむしろくずれ難くなるはずである。さらに、本願の具体的な実施例では柱状スペーサーの上底の一辺と下底の一辺との比が記載されておらず、上底の一辺と下底の一辺との比が５０～９０％である場合にこのような効果が得られることは、本願の具体的な実施例で裏付けられてもいない。　また、本願の明細書段落（００２６）及び図２（ｂ）において、上底の寸法方法について定義されており、具体的には、「スペーサーの断面拡大写真を用い、スペーサー１８の上底４４に接線４６を引き、次いで、接線４６と同方向の下底４８の一辺の長さＤを測定する。次に、スペーサー１８の下底４８（基板２２）と上底４４の接線４６との間の間隔（高さ）Ｈを測定する。そして、この高さＨに１未満の一定の定数Ｃ、たとえば０．９をかけた寸法を基板２２からの上底の高さ（Ｃ×Ｈ）として、その位置に基板２２と平行な線Ｘを引き、その線Ｘとスペーサー１８の輪郭（側面）５０との交わった点と点との間隔を上底の寸法とした。」旨が記載されている。　この記載によれば、スペーサー１８の高さＨに定数Ｃをかけた位置における寸法を上底の寸法とする旨が示されているが、定数Ｃの範囲については何ら記載されていない。よって、定数Ｃの範囲が不明であり、それによって上底の寸法が、柱状スペーサーのどの位置における寸法であるのかが不明であり、本願の請求項７に記載の発明は明確ではない。　本願の請求項７に記載の発明に従属している本願の請求項８では、スペーサーの上底の一辺の長さ又は直径もしくは長径は、該スペーサの最大高に０．９をかけた位置における下底と水平な面の一辺の長さ又は直径もしくは長径である旨が限定されている。　しかしながら、この場合にも、上述のように、上底の一辺と下底の一辺との比が５０％未満であると、液晶表示装置における開口率を極端に失うとは一概に言えず、上底の一辺と下底の一辺との比が９０％を超えると、逆テーパー状のテーパーの傾斜が小さくなるはずであり、以降のセル工程で柱がむしろくずれ難くなるはずであり、本願の上記効果が得られるものではない。　よって、本願発明は、本願の発明の詳細な説明の記載が、当業者がその実施をすることができる程度に明確かつ十分に記載したものではないため、特許法第３６条第４項第１号の規定に該当し、あるいは本願の特許請求の範囲の記載が、特許を受

けようとする発明が明確ではないため、特許法第３６条第６項第２号の規定に該当し拒絶されるべきものである。

Japanese Patent Application No.11-122923

Claims

1.A liquid crystal display comprising:

first and second substrates facing each other,

columnar spacers for regulating a cell gap between the both substrates, said spacers being made from a photosensitive resin and disposed solely in a non-display region of either or both of the first and the second substrates, and having a hardness (DH) of from 26 to 30,and

liquid crystal sandwiched between the first and the second substrates.

2.A liquid crystal display comprising:

first and second substrates facing each other,

columnar spacers for regulating a cell gap between the both substrates, said spacers being made from a photosensitive resin and disposed solely in a non-display region of either or both of the first and the second substrates, and having a hardness value of plastic deformation (HV) of from 38 to 46,and

liquid crystal sandwiched between the first and the second substrates.

3.A liquid crystal display comprising:

first and second substrates facing each other,

columnar spacers for regulating a cell gap between the both substrates, said spacers being made from a photosensitive resin and disposed solely in a non-display region of either or both of the first and the second substrates, and having a hardness (DH) of from 26 to 30 and a hardness value of plastic deformation (HV) of from 38 to 46,and

liquid crystal sandwiched between the first and the second substrates.

4. The liquid crystal display according to any one of claims 1 to 3, wherein said spacers have an elastic coefficient of from 100 to 500 kg/mm^2.

5. The liquid crystal display according to any one of claims 1 to 4, wherein said spacers have a linear expansion coefficient which is equal to a coefficient of volume expansion per unit area of said liquid crystal.

6. The liquid crystal display according to any one of claims 1 to 5, wherein said spacers have a column occupancy ratio of from 0.05 to 0.86%, said column occupancy ratio defined by the following formula,

column occupancy ratio = (column base area x column density/ pixel area) x 100

wherein the column density is defied by the following formula,

column density = total number of columns/ total number of pixels.

7. The liquid crystal display according to any one of claims 1 to 6, wherein said spacers have a cross-section, in a direction parallel to the both substrates,

in the form of a rectangle, triangle, or polygon with a ratio of a side length of a upper cross-section to that of a lower cross-section ranging from 50 to 90 %, or

in the form of a circle, ellipsoid, or prolate ellipsoid with a ratio of a length of diameter or major axis of a upper cross-section to that of a lower cross-section ranging from 50 to 90 %.

8. The liquid crystal display according to claim 7, wherein the length of the side, diameter, or major axis of the upper cross-section is a length of a side, diameter, or major axis of a cross-section at a height of 0.9 time a maximum height of the spacer.

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	1/1343			1/1343		
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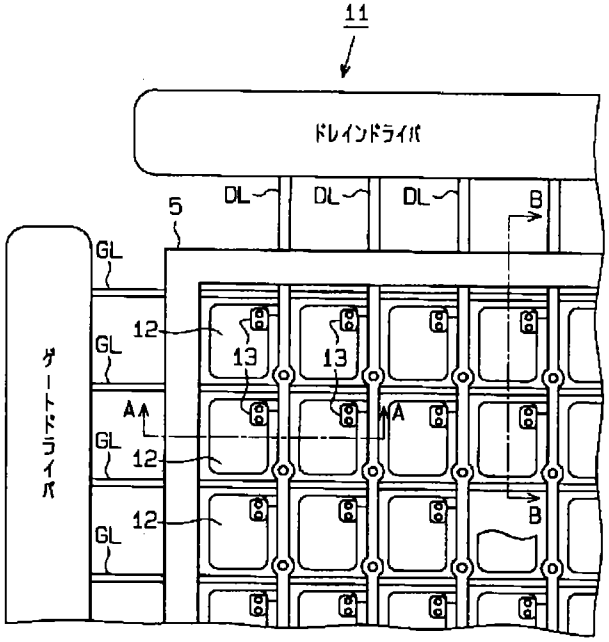
(54)【発明の名称】　膜材がパターン形成された固体装置及びパターン形成方法

(57)【要約】
【課題】例えば薄膜電極が基板表面にパターン形成された液晶表示装置にあって、ブラシスクラバ等による基板洗浄に伴う薄膜電極の損傷を防止する。
【解決手段】ポリシリコン形ＴＦＴ方式アクティブマトリックス液晶表示装置を構成するＴＦＴアレイ側基板１１の透明絶縁基板上にはＩＴＯにて形成される画素電極２２がマトリックス状に設けられている。また、アレイ側基板１１の透明絶縁基板上には、ブラシスクラバ等による基板洗浄の際に画素電極２２が損傷することを防止するために、画素電極２２群の外周を囲むように同画素電極２２より膜厚の薄いダミー膜５が設けられる。



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【特許請求の範囲】

【請求項１】表面に適宜の膜材がパターン形成された状態でブラシ洗浄される固体装置において、
当該装置の同一表面において前記膜材の外周を囲むようにパターン形成されたダミー膜を備えることを特徴とする膜材がパターン形成された固体装置。

【請求項２】前記ダミー膜は、その膜厚が前記膜材の膜厚よりも薄くパターン形成されたものである請求項１記載の膜材がパターン形成された固体装置。

【請求項３】前記ダミー膜は、その膜厚が装置外周に向かうにしたがって順次薄くなる勾配を有して若しくは階段状にパターン形成されたものである請求項１または２記載の膜材がパターン形成された固体装置。

【請求項４】前記ダミー膜は、前記膜材と同一材料にてパターン形成されたものである請求項１～３のいずれかに記載の膜材がパターン形成された固体装置。

【請求項５】前記ダミー膜は、前記膜材と異なる材料にてパターン形成されたものである請求項１～３のいずれかに記載の膜材がパターン形成された固体装置。

【請求項６】前記固体装置は液晶表示装置の液晶駆動用半導体素子が設けられる透明絶縁基板であり、前記膜材は同透明絶縁基板の表面に上にパターン形成された画素透明電極である請求項１～５のいずれかに記載の膜材がパターン形成された固体装置。

【請求項７】固体装置の表面に膜材をパターン形成する方法において、
少なくとも前記固体装置の最外周にパターン形成される膜材の膜厚をそれ以外の部分にパターン形成される膜材の膜厚よりも薄くすることを特徴とするパターン形成方法。

【請求項８】固体装置の表面に膜材を着膜する工程と、該着膜した膜材の膜厚がその端部ほど薄くなるようにプラズマ反応圧力を高めたプラズマドライエッチングにて同膜材をエッチングする工程と、
を備えるパターン形成方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、例えば透明電極がパターン形成された液晶表示装置など、膜材がパターン形成された固体装置、及びパターン形成方法に関する。

【０００２】

【従来の技術】従来、表示装置、例えばポリシリコン形ＴＦＴ（Thin Film Transistor：薄膜トランジスタ）方式アクティブマトリックス液晶表示装置等においては、その画素電極としてＩＴＯ（Indium Tin Oxide）等の透明薄膜電極が使用されている。この透明薄膜電極はポリシリコン形ＴＦＴをガラス基板等の上に形成した後にパターニングして形成される。そして、特に歩留まりの向上を図るものに対しては、その後の製造工程に移る前にブラシスクラバ等による基板洗浄が行われている。

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【０００３】ここで、図１０～図１２を参照して、上記ブラシスクラバを用いた基板洗浄の概要を説明する。図１０に上記液晶表示装置のＴＦＴアレイ側基板１の部分平面構造を示し、図１１には同図１０のＸ－Ｘ線に沿った断面構造を示す。なお、図１１に示す断面構造においてＴＦＴ等、画素電極以外の液晶駆動にかかる部分の図示は省略する。

【０００４】図１０に示すＴＦＴアレイ側基板１において、ドレインドライバに接続されるドレイン線ＤＬとゲートドライバに接続されるゲート線ＧＬとの交点近傍に液晶表示装置を構成する各表示画素の画素電極２がパターン形成されている。この画素電極２はＴＦＴアレイ側基板１のほぼ全面において所定画素数分、マトリックス状に形成されているが、図１０においてはその一部分のみを示す。

【０００５】また、画素電極２は上述のＩＴＯからなり、コンタクトホール３を介してＴＦＴのソース電極（図示略）に接続されている。また同画素電極２は、図１１に示されように、ＴＦＴアレイ側基板１を構成する透明絶縁基板（ガラス基板等）１ａ上に形成されている。

【０００６】次に、図１２に示す平面図に基づき、ブラシスクラバを使用したＴＦＴアレイ側基板１の洗浄態様を説明する。基板洗浄に際しては同図１２に示されるように、ＴＦＴアレイ側基板１を所定の回転台（図示略）に載置し、同回転台を回転させた状態で同じく回転させたブラシスクラバのブラシ部４を当該基板１の表面に当接させる。そして、同図１２の矢印Ｙ方向にブラシ部４を移動させながら同基板１の表面全体を洗浄する。なおこのとき、薬液を用いた化学的洗浄と併用されることも多い。

【０００７】

【発明が解決しようとする課題】ところで、上述したようなＩＴＯ等の画素電極２がその最上部にパターン形成されたＴＦＴアレイ側基板１をブラシスクラバを使用して洗浄する場合にあっては、図１３に示されるように、画素電極２のうちの上記回転するブラシスクラバのブラシ４ａに最初に当接する電極がその機械的な力によって損傷してしまうことがある。このように基板１の洗浄工程において画素電極２が損傷を被ると、それは画素欠陥となり、ひいては液晶表示装置としての製品歩留りを低下させる要因ともなる。

【０００８】なお、こうした液晶表示装置に限らず、半導体装置等を含めてその表面に膜材がパターン形成され、その後上記ブラシスクラバ等によって表面洗浄される固体装置にあっては、こうした実情も概ね共通したものとなっている。

【０００９】本発明は上記実情に鑑みてなされたものであり、その目的とするところは、ブラシスクラバ等による洗浄に対してその表面にパターン形成された膜材を好

適に保護し、ひいては製品歩留りを向上させることのできる膜材がパターン形成された固体装置及びパターン形成方法を提供することにある。

【００１０】

【課題を解決するための手段】上記の目的を達成するために、請求項１に記載の発明では、表面に適宜の膜材がパターン形成された状態でブラシ洗浄される固体装置において、当該装置の同一表面において前記膜材の外周を囲むようにパターン形成されたダミー膜を備えることをその要旨とする。

【００１１】同構成においては、固体装置の同一表面において前記膜材の外周を囲むようにパターン形成されたダミー膜が備えられる。そのため、固体装置を例えばブラシスクラバ等を使用してブラシ洗浄する場合、ブラシスクラバのブラシは前記パターン形成された膜材と当接する前にまずダミー膜に当接する。そのため、回転するブラシスクラバのブラシの機械的な力によって前記膜材が損傷すことは防止される。

【００１２】また請求項２に記載の発明では、請求項１記載の膜材がパターン形成された固体装置において、前記ダミー膜は、その膜厚が前記膜材の膜厚よりも薄くパターン形成されたものであることをその要旨とする。

【００１３】同構成においては、固体装置を例えばブラシスクラバ等を使用してブラシ洗浄する場合、ブラシスクラバのブラシは、まず膜材の膜厚よりも薄くパターン形成されたダミー膜に乗り上げ段差を小さくしてから同膜材に乗り上がるようになる。そのため、回転するブラシスクラバのブラシの機械的な力によって前記膜材が損傷することは好適に防止される。

【００１４】また請求項３に記載の発明では、請求項１または２記載の膜材がパターン形成された固体装置において、前記ダミー膜は、その膜厚が装置外周に向かうにしたがって順次薄くなる勾配を有して若しくは階段状にパターン形成されたものであることをその要旨とする。

【００１５】同構成においては、固体装置を例えばブラシスクラバ等を使用してブラシ洗浄する場合、ブラシスクラバのブラシはダミー膜の勾配若しくは階段に沿って好適に前記膜材に乗り上がるようになる。そのため、回転するブラシスクラバのブラシの機械的な力によって前記膜材が損傷することは好適に防止される。

【００１６】また請求項４に記載の発明では、請求項１～３のいずれかに記載の膜材がパターン形成された固体装置において、前記ダミー膜は、前記膜材と同一材料にてパターン形成されたものであることをその要旨とする。

【００１７】同構成によれば、ダミー膜を形成するための別途マスク等は不要となり、その製造工程が簡略化される。また請求項５に記載の発明では、請求項１～３のいずれかに記載の膜材がパターン形成された固体装置において、前記ダミー膜は、前記膜材と異なる材料にてパターン形成されたものであることをその要旨とする。

【００１８】同構成によれば、ダミー膜の設計等の自由度が高まる。また請求項６に記載の発明では、請求項１～５のいずれかに記載の膜材がパターン形成された固体装置において、前記固体装置は液晶表示装置の液晶駆動用半導体素子が設けられる透明絶縁基板であり、前記膜材は同透明絶縁基板の表面に上にパターン形成された画素透明電極であることをその要旨とする。

【００１９】同構成によれば、液晶表示装置にあって、透明絶縁基板表面のブラシ洗浄に伴う画素透明電極の損傷は好適に防止される。また請求項７に記載の発明では、固体装置の表面に膜材をパターン形成する方法において、少なくとも前記固体装置の最外周にパターン形成される膜材の膜厚をそれ以外の部分にパターン形成される膜材の膜厚よりも薄くすることをその要旨とする。

【００２０】同形成方法においては、膜材の段差が緩和されるため、ブラシ洗浄に伴う同膜材の損傷も好適に防止される。また請求項８に記載の発明では、パターン形成方法において、固体装置の表面に膜材を着膜する工程と、該着膜した膜材の膜厚がその端部ほど薄くなるようにプラズマ反応圧力を高めたプラズマドライエッチングにて同膜材をエッチングする工程と、を備えることをその要旨とする。

【００２１】同形成方法においては、膜材の段差が緩和されるため、ブラシ洗浄に伴う同膜材の損傷も好適に防止されるとともに、製造工数を増やすことなく勾配を有する膜材を得ることができる。

【００２２】

【発明の実施の形態】［第１の実施の形態］以下、本発明にかかる膜材がパターン形成された固体装置をポリシリコン形ＴＦＴ方式アクティブマトリックス液晶表示装置に適用した第１の実施の形態について図１～図４に基づき詳細に説明する。

【００２３】図１は、本実施の形態にかかる固体装置（液晶表示装置）のＴＦＴアレイ側基板１１の部分平面構造を示すものである。また、図２（ａ）は、この図１のＡ－Ａ線に沿った断面構造、図２（ｂ）は同じく図１のＢ－Ｂ線に沿った断面構造をそれぞれ示すものである。

【００２４】図１に示すＴＦＴアレイ側基板１１において、ドレインドライバに接続されるドレイン線ＤＬとゲートドライバに接続されるゲート線ＧＬとの交点近傍に液晶表示装置を構成する各表示画素の画素電極１２がパターン形成されている。この画素電極１２はＴＦＴアレイ側基板１１のほぼ全面において所定画素数分、マトリックス状に形成されているが、図１においてはその一部分のみを示す。

【００２５】また、画素電極１２は上述のＩＴＯからなり、コンタクトホール１３を介してＴＦＴのソース電極（図示略）に接続されている。また同画素電極１２は、

図２に示されように、ＴＦＴアレイ側基板１１を構成する透明絶縁基板（ガラス基板等）１１ａ上に形成されている。

【００２６】ここで本実施の形態にかかる液晶表示装置にあっては、図１に示されるように、マトリックス状に設けられた画素電極１２の外周を連続して囲むようにして、ダミー膜５が設けられている（図１にはその一部のみ示される）。また、図２（ａ）及び（ｂ）に示されるように、同ダミー膜５の膜厚は、画素電極１２の膜厚よりも薄く形成されている。このダミー膜５は、前記ブラシスクラバ（図１２、図１３）を使用してアレイ側基板１１を洗浄する際に、同ブラシスクラバのブラシ４ａによって画素電極１２が損傷すことを防止するために設けられている。

【００２７】すなわち、本第１の実施の形態においては、図３に示されるように、前記ブラシ４ａが画素電極１２と当接する際、同ブラシ４ａは、まずダミー膜５に乗り上がり、画素電極１２との段差が小さくなった状態で同画素電極１２に乗り上がる。そのため、回転するブラシ４ａの機械的な力によって画素電極１２自体が損傷することは防止されるようになる。

【００２８】なお、このダミー膜５は画素電極１２と同様にＩＴＯにて形成されてもよいし、その他の材質にて、例えばＡｌ（アルミニウム）、Ｃｒ（クロム）等にて形成されてもよい。

【００２９】次に、図４を参照して、上記ダミー膜５及び画素電極１２の形成方法を説明する。これら膜材のパターン形成に際しては、まず図４（ａ）に示すように、透明絶縁基板１１ａ上にダミー膜５となる薄膜５Ａを成膜する。次に、図４（ｂ）に示すように所定のレジストパターン６を形成し、続いて図４（ｃ）に示すように薄膜５Ａをエッチングする。その後、レジストパターン６を剥離することで、透明絶縁基板１１ａ上に薄膜ダミー配線５が形成される。

【００３０】次に、図４（ｄ）に示すように、透明絶縁基板１１ａ上に上記画素電極１２となるＩＴＯ膜１２Ａを成膜し、その上に所定のレジストパターン６ａを形成する。続いて、この成膜したＩＴＯ膜２Ａをエッチングし、レジストパターン６ａを剥離すると、図４（ｅ）に示されるように、画素電極１２及びダミー膜５が透明絶縁基板１１ａ上に形成されるようになる。

【００３１】以上説明したように、本第１の実施の形態によれば、以下のような効果を得ることができる。

（１）本第１の実施の形態では、液晶表示装置のＴＦＴアレイ側基板１１の透明絶縁基板１１ａ上において、画素電極１２の周囲を連続して囲んで、且つその膜厚が同画素電極１２の膜厚より薄く形成されるダミー膜５が設けられる。そのため、ブラシスクラバを使用して前記基板１１を洗浄する場合にあっても、ブラシスクラバのブラシ４ａが画素電極１２と当接する際、ブラシ４ａはいきなり画素電極１２の側面に衝突せずに、まずダミー膜５に乗り上げて、画素電極１２の段差が小さくなってから同画素電極１２に乗り上げるようになる。そのため、同ブラシ４ａの機械的な力によって画素電極１２が損傷すことが防止され、ひいては液晶表示装置としての生産歩留りが向上されるようになる。

【００３２】なお、上記ダミー膜５の形状は、図１に示したような画素電極１２の外周を連続して囲む形状に限られない。他に例えば、図５に示すように、画素電極１２の形状に対応して切断された形状となるダミー膜５ａの集合として同画素電極１２の外周を囲む形状としてもよい。このダミー膜として要は、透明絶縁基板１１ａ上において画素電極１２より同基板端側にあって画素電極１２の周囲を囲むように設けられるとともに、その膜厚が画素電極１２の膜厚より薄く形成されるものであればよい。

【００３３】また、上述のようにダミー膜５は画素電極１２と同様にＩＴＯにて形成されてもよいし、その他の材質にて、例えばＡｌ（アルミニウム）、Ｃｒ（クロム）等にて形成されてもよいが、ＩＴＯにて形成される場合は、画素電極１２をパターン形成する工程において一括してダミー膜５をパターン形成することができる。すなわち、ダミー膜５を形成するための別途マスク等は一切不要であり、その製造工数、製造コストを低く抑えることが可能となる。一方、ダミー膜５をＩＴＯ以外の材質にて形成する場合は、同ダミー膜５の設計等の自由度が高まる。

［第２の実施の形態］次に、本発明にかかる膜材がパターン形成された固体装置を同じくポリシリコン形ＴＦＴ方式アクティブマトリックス液晶表示装置に適用した第２の実施の形態について図６～図９に基づき詳細に説明する。

【００３４】図６は本実施の形態にかかる固体装置（液晶表示装置）のＴＦＴアレイ側基板２１の部分平面構造を示すものである。図７（ａ）は、この図６のＣ－Ｃ線に沿った断面構造、図７（ｂ）は、同じく図６のＤ－Ｄ線に沿った断面構造をそれぞれ示すものである。

【００３５】ここでは第１の実施の形態との相違点を中心に説明する。本第２の実施の形態の前記第１の実施の形態との相違点は、図６に示されるように、マトリックス状に設けられた画素電極２２の外周を囲むダミー膜として、同画素電極２２を２重に囲むダミー電極２２ａ，２２ｂが設けられている点にある（図６にはその一部のみ示される）。また、これらダミー電極２２ａ，２２ｂの平面形状は画素電極２２と同一に形成されるとともに、その膜厚は画素電極２２の膜厚に比べて薄く形成される。さらに、図７（ａ），（ｂ）に示されるように、同ダミー電極２２ａ，２２ｂの表面は、その膜厚が画素電極２２からアレイ側基板２１端部に向けて、すなわち図７（ａ）及び（ｂ）においてはその右側から左側に向

けて薄くなるように勾配を有して形成されている。なお、このダミー電極２２ａ，２２ｂは画素電極２２と同様にＩＴＯにて形成される。

【００３６】そのため、本第２の実施の形態においては、上述したようなブラシスクラバを用いた基板２１の洗浄の際、図８に示されるように、そのブラシ４ａは、ダミー電極２２ａからダミー電極２２ｂの表面の傾斜に沿うようにして画素電極２２上に乗り上げるようになる。このため、本第２の実施の形態によっても、回転するブラシ４ａの機械的な力によって画素電極２２が損傷すことは好適に防止されるようになる。

【００３７】次に、図９を参照して、上記ダミー配線２２ａ，２２ｂ及び画素電極２２の形成方法を説明する。これら膜材のパターン形成に際しては、まず図９（ａ）に示すように、透明絶縁基板２１ａ上にダミー電極２２ａ，２２ｂ及び画素電極２２となるＩＴＯ膜２２Ａを成膜する。次に、図９（ｂ）に示すように、透明絶縁基板２１ａの端部に形成されるＩＴＯ膜２２Ａの膜厚が、その中央部に形成されるＩＴＯ膜２２Ａに対して徐々に薄くなるように同ＩＴＯ膜２２Ａの表面をエッチングする。

【００３８】このエッチング方法としては、例えばプラズマを用いたドライエッチング法において、反応圧力を通常の圧力（約１８ｍＴｏｒｒ）より高く、例えば２０ｍＴｏｒｒとする方法が有効である。すなわちここでは、上記エッチングにかかるプラズマ反応圧力を高くすると、基板端ほど深く、いわばアンバランスにエッチングされることを積極的に利用する。

【００３９】続いて、図９（ｃ）に示すように、このエッチングされたＩＴＯ膜２２Ａ上に所定のレジストパターン６ｂを形成する。そしてＩＴＯ膜２２Ａをエッチングし、レジストパターン６ｂを剥離すると、図９（ｄ）に示されるように、画素電極２２及びダミー電極２２ａ，２２ｂが透明絶縁基板２１ａ上に形成されるようになる。

【００４０】以上説明したように、本第２の実施の形態によれば、以下のような効果を得ることができる。

（１）本第２の実施の形態では、ダミー電極２２ａ，２２ｂの膜厚が透明絶縁基板２１ａの外側に向かうにしたがい薄くなるように形成される。そのため同基板２１ａを例えばブラシスクラバを使用して洗浄する場合であれ、ブラシスクラバのブラシ４ａが画素電極２２と当接する際、同ブラシ４ａは好適に画素電極２２に乗り上がるようになる。そのため、回転するブラシスクラバのブラシ４ａの機械的な力によって画素電極２２が損傷することは好適に防止される。

【００４１】（２）本第２の実施の形態では、ダミー電極２２ａ，２２ｂが画素電極２２と同質のＩＴＯによってパターン形成される。そのため、画素電極２２をパターン形成する工程において一括してダミー電極２２ａ，２２ｂをパターン形成することができる。すなわち、ダミー電極２２ａ，２２ｂを形成するための別途マスク等は一切不要であり、その製造工数、製造コストを低く抑えることが可能となる。

【００４２】（３）本第２の実施の形態では、ダミー電極２２ａ，２２ｂの表面の傾斜を、画素電極２２の形成も含めたＩＴＯのエッチング工程において、プラズマ反応圧力を積極的に高めることにより形成した。すなわち、それらダミー電極２２ａ，２２ｂの表面の傾斜すら、何ら別途の工程を追加することなく形成することができる。

【００４３】なお、上記第２の実施の形態は以下のようにその構成を変更して実施することもできる。

・上記第２の実施の形態においては、画素電極２２のダミー膜として、同画素電極２２の外周を２重に囲むようにその膜厚に勾配を有するダミー電極２２ａ，２２ｂを形成する例を示したが、これに限定されない。この膜厚に勾配を有するダミー電極は画素電極２２の外周を１重に囲むように形成されるものであってもよい。

【００４４】・上記第２の実施の形態においては、画素電極２２のダミー膜として、その平面形状が画素電極２２と同一に形成されるダミー電極２２ａ，２２ｂを形成する例を示したが、これに限定されない。他に例えば、薄膜ダミー配線２２ａ，２２ｂの平面形状は２画素分の面積を有する平面形状としてもよいし、あるいは３画素分、４画素分の面積を有する平面形状としてもよい。また逆に、１画素分の面積よりも面積が小さくなる形状としてもよい。要は、画素電極２２と同一面積である必要はない。また、画素電極２２を含めてダミー電極２２ａ，２２ｂの材質がＩＴＯである必要はなく、構造的にはそれら画素電極２２及びダミー電極２２ａ，２２ｂが同一材料である必要もない。

【００４５】その他、先の第１の実施の形態も含めて、前記各実施の形態では、ダミー膜として形成される膜材（ダミー膜５やダミー電極２２ａ，２２ｂ）がいずれも画素電極（１２，２２）よりも膜厚が薄く形成される場合について例示したが、その限りでもない。すなわち、画素電極をそのブラシによる洗浄に伴う損傷から保護することができればダミー膜自体は損傷されてもよく、例えば画素電極と同一の膜厚にするなど、必ずしも画素電極より薄い膜厚とする必要はない。また、特にダミー膜が金属膜（Ａｌ等）にて形成され下地との密着性が良い場合にも、必ずしも画素電極より薄い膜厚とする必要はない。

【００４６】また、第１の実施の形態のダミー膜５にも、第２の実施の形態に示したダミー電極２２ａ，２２ｂのような勾配を設けてもよい。また、これらダミー膜５及びダミー電極２２ａ，２２ｂに勾配を設ける代わりに、それらの膜厚が装置外周に向かうにしたがって階段状に順次薄くなるように形成されるものとしてもよい。

なお、この膜厚が階段状に順次薄くなる態様は、複数のダミー膜によって階段状とされるものであってもよいし、単一のダミー膜上においても階段状とされものであってもよい。

【００４７】また、前記各実施の形態では、固体装置の最外周にパターン形成される膜材をダミー膜（ダミー膜５やダミー電極２２ａ）として形成する例を示したがその限りでもない。同膜材はダミー膜としてではなく、他に例えば電極等として形成されるものであってもよい。

【００４８】また、上記各実施の形態においては、本発明にかかる膜材がパターン形成された固体装置をポリシリコン形ＴＦＴ方式アクティブマトリックス液晶表示装置に適用した例を示したが、これに限定されない。他に例えば、同固体装置をアモルファスシリコン形ＴＦＴアクティブマトリクス液晶表示装置に適用してもよいし、パッシブマトリクス液晶表示装置に適用してもよい。さらに液晶表示装置に限定されず、例えば太陽電池セル等、薄膜電極が基板上にパターン形成されるものであれば同様にこの発明を適用することができる。そしてさらには、これら薄膜電極がパターン形成されるものに限らず、ＬＳＩ等の半導体装置にあっても、電極その他の膜材が基板表面にパターン形成され、その状態で前記ブラシスクラバ等による洗浄が行われる固体装置でさえあれば、やはり同様に本発明を適用することはできる。

【００４９】

【発明の効果】請求項１の発明によれば、固体装置を例えばブラシスクラバ等を使用してブラシ洗浄する場合、ブラシスクラバのブラシは前記パターン形成された膜材と当接する前にまずダミー膜に当接する。そのため、回転するブラシスクラバのブラシの機械的な力によって同膜材が損傷すことは防止される。

【００５０】請求項２の発明によれば、同様にブラシ洗浄する場合、ブラシスクラバのブラシは、まず膜材の膜厚よりも薄くパターン形成されたダミー膜に乗り上げ段差を小さくしてから同膜材に乗り上がるようになる。そのため、回転するブラシスクラバのブラシの機械的な力によって同膜材が損傷すことは好適に防止される。請求項３の発明によれば、同様にブラシ洗浄する場合、ブラシスクラバのブラシはダミー膜の勾配若しくは階段に沿って好適に膜材に乗り上がるようになる。そのため、回転するブラシスクラバのブラシの機械的な力によって同膜材が損傷することは好適に防止される。

【００５１】請求項４の発明によれば、前記ダミー膜の製造工程が簡略化される。請求項５の発明によれば、前記ダミー膜の設計等の自由度が高まる。請求項６の発明によれば、液晶表示装置にあって、透明絶縁基板表面のブラシ洗浄に伴う画素透明電極の損傷は好適に防止される。

【００５２】請求項７の発明によれば、膜材の段差が緩和されるため、ブラシ洗浄に伴う同膜材の損傷も好適に防止される。請求項８の発明によれば、膜材の段差が緩和されるため、ブラシ洗浄に伴う同膜材の損傷も好適に防止されるとともに、製造工数を増やすことなく勾配を有する膜材を得ることができる。

【図面の簡単な説明】

【図１】この発明にかかる固体装置の第１の実施の形態を示す部分平面図。

【図２】図１のＡ－Ａ線及びＢ－Ｂ線に沿った部分断面図。

【図３】第１の実施の形態の固体装置に対する洗浄の態様を示す部分断面図。

【図４】第１の実施の形態の固体装置の製造手順を示す断面図。

【図５】第１の実施の形態の他の実施の態様を示す部分平面図。

【図６】この発明にかかる固体装置の第２の実施の形態を示す部分平面図。

【図７】図６のＣ－Ｃ線及びＤ－Ｄ線に沿った部分断面図。

【図８】第２の実施の形態の固体装置に対する洗浄の態様を示す部分断面図。

【図９】第２の実施の形態の固体装置の製造手順を示す断面図。

【図１０】従来の固体装置（液晶表示装置）の平面構造を示す部分平面図。

【図１１】図１０のＸ－Ｘ線に沿った部分断面図。

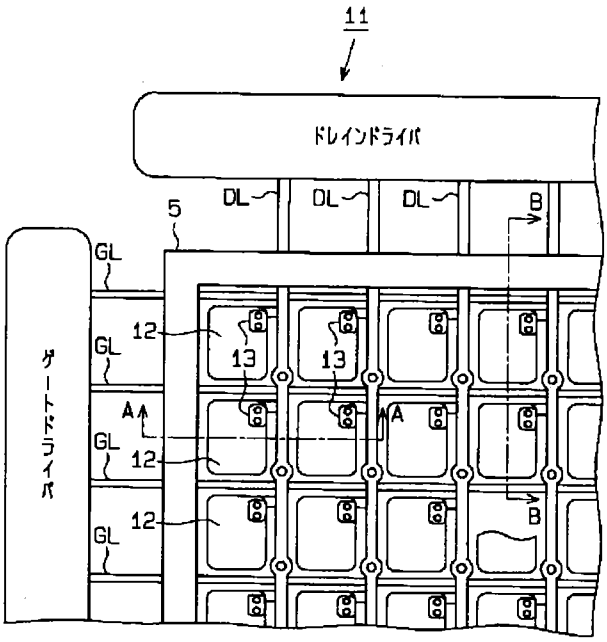
【図１２】ブラシスクラバによる基板洗浄態様を示す平面図。

【図１３】従来の固体装置に対する洗浄の態様を示す部分断面図。

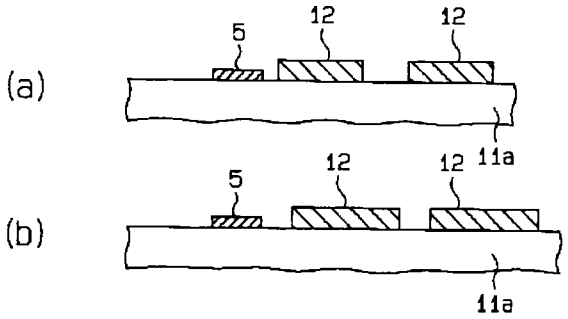
【符号の説明】

４ａ…ブラシスクラバのブラシ、５…ダミー膜、６，６ａ，６ｂ…レジスト膜、１１，２１…ＴＦＴアレイ側基板、１１ａ，２１ａ…透明絶縁基板、１２，２２…画素電極（ＩＴＯ薄膜電極）、２２ａ，２２ｂ…ダミー電極。

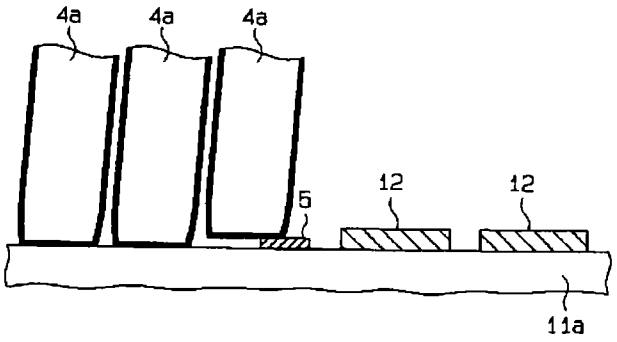
【図１】



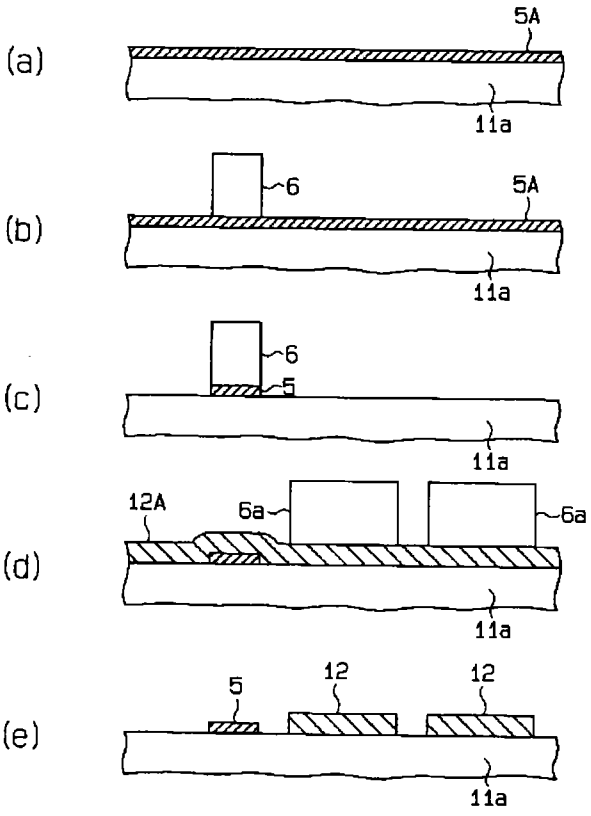
【図２】



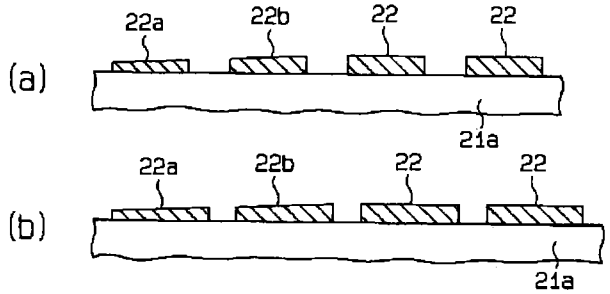
【図３】



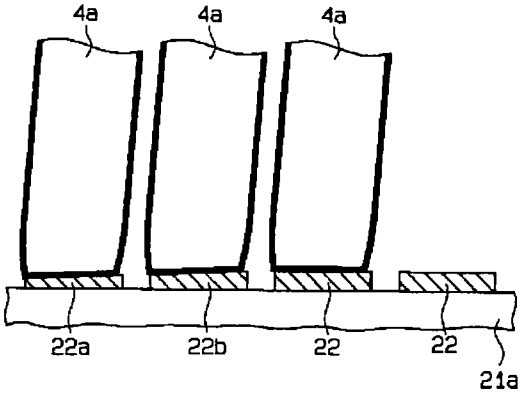
【図４】



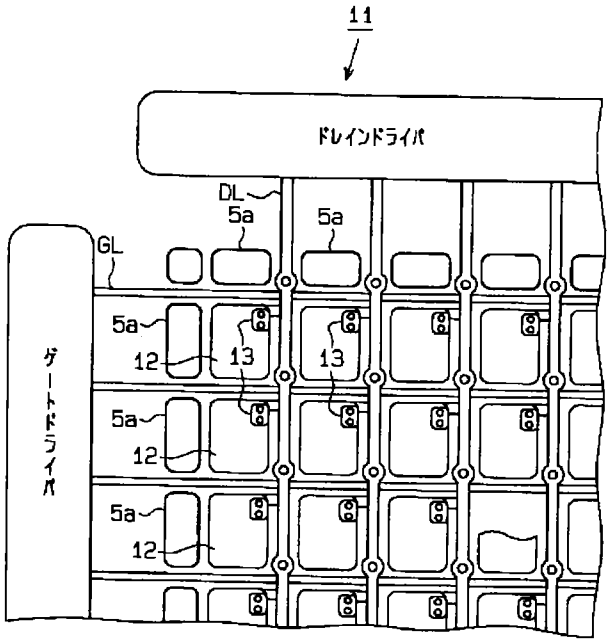
【図７】



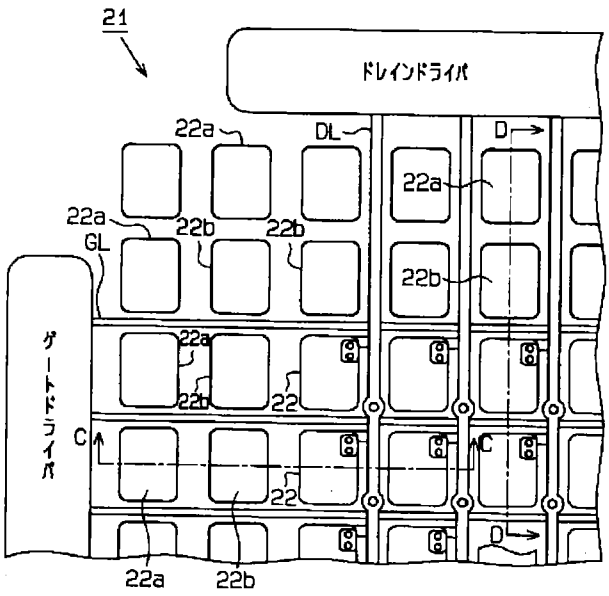
【図８】



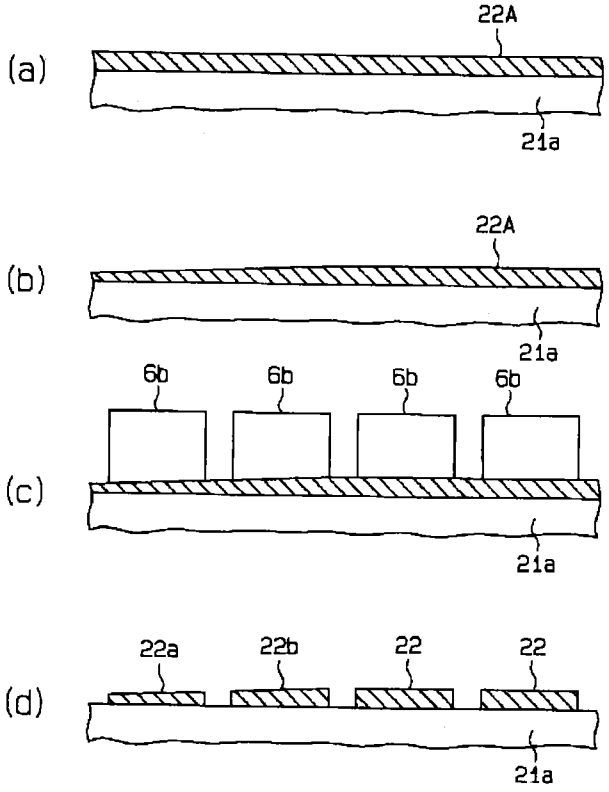
【図５】



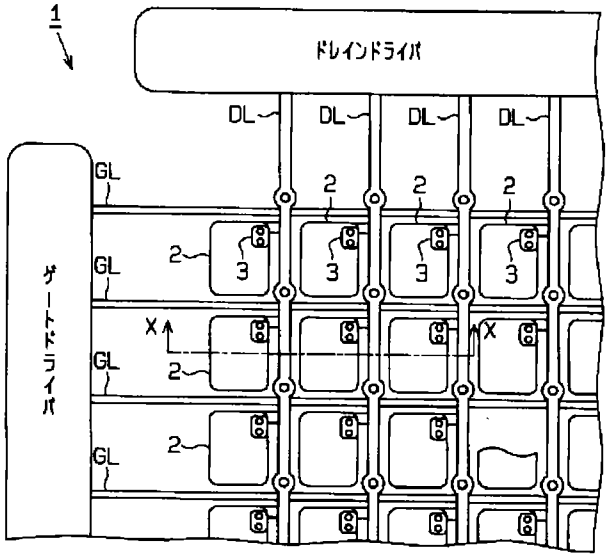
【図６】



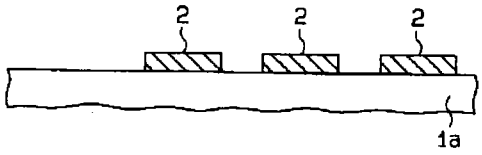
【図９】



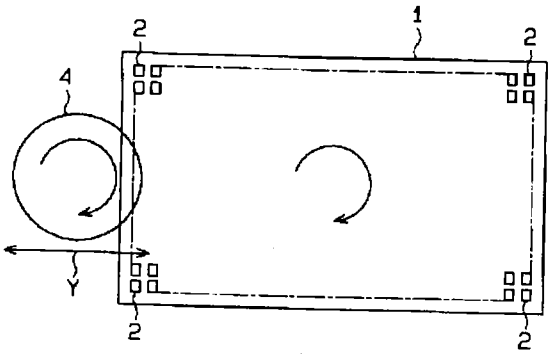
【図１０】



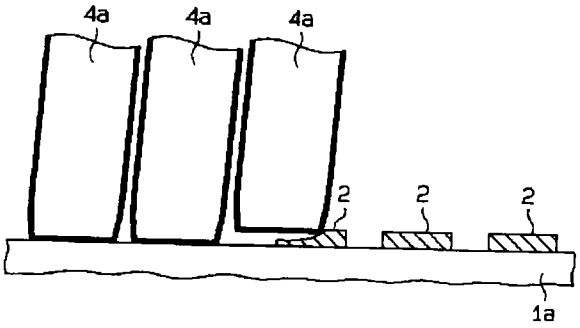
【図１１】



【図１２】



【図１３】



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審査請求　未請求　請求項の数 1　(全5頁)

⑤4発明の名称　半導体装置の製造方法

⑳特　願　平1−9209
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明　細　書

1．発明の名称

半導体装置の製造方法

2．特許請求の範囲

1．半導体基板上に金属膜を形成する工程と、この金属膜上に所望の配線パターンのフォトレジスト膜パターン及びダミーのフォトレジスト膜パターンを形成する工程と、これらフォトレジスト膜パターン及びダミーパターンをマスクにして前記金属膜を反応性イオンエッチング法によりエッチングする工程とを含み、前記ダミーパターンにより前記フォトレジスト膜パターンの面積密度を増大させた状態で前記エッチングを行うことを特徴とする半導体装置の製造方法。

3．発明の詳細な説明

〔産業上の利用分野〕

本発明は半導体の製造方法に関し、特にアルミニウム膜等の金属膜で構成される配線パターンの形成方法に関する。

〔従来の技術〕

従来、アルミニウム膜等の金属膜で構成される配線パターン形成は、全面に形成した金属膜上に所望のパターンのフォトレジスト膜を形成し、このフォトレジスト膜をマスクとして反応性イオンエッチングにより金属膜を選択エッチングすることで形成していた。

従来の技術の一例を第3図(a)及び(b)の縦断面図を用いて説明する。

先ず、第3図(a)のように、半導体基板1上の酸化膜2上にアルミニウム膜3を形成し、この上に所望のパターンを有するフォトレジスト膜7を形成する。

次いで、同図(b)のように、このフォトレジスト膜7をマスクにして反応性イオンエッチングを行い、前記アルミニウム膜3を選択エッチングし、配線パターンを形成する。

その後、フォトレジスト膜7を除去することでアルミニウム配線パターンが完成される。

〔発明が解決しようとする課題〕

上述した従来の方法では、エッチングにより得

られるアルミニウム膜3の形状は、フォトレジスト膜7のパターン密度（ウェハの面積に対してフォトレジスト膜が占める面積の割合）に大きく影響され、パターン密度が小さくなるほどサイドエッチングやアンダーカットが生じやすくなる。これはアルミニウム膜の反応性イオンエッチングでは、エッチング中に側壁に反応生成物が堆積することにより異方性が保たれるが、この堆積にはフォトレジスト膜からの反応物が大きく寄与しているためである。

このため、第3図（b）のように、形成されるアルミニウム膜3はサイドエッチングやアンダーカットにより、フォトレジスト膜7の幅寸法よりも小さくなり、所要の配線パターンを得ることが難しいものとなる。

サイドエッチングやアンダーカットが生じ易いパターン密度はエッチング条件により異なるが、ほぼ25%以下の場合である。

したがって、第4図に示すように、同一のウェハ上でフォトレジスト膜7のパターン密度が場所

により著しく異なる場合には、パターン密度が小さい（例えば20%）領域Aでのアルミニウム膜3が、パターン密度が大きい（例えば60%）領域Bのアルミニウム膜3よりもアンダーカットやサイドエッチングにより細幅に形成され、均一な配線パターンを得ることができなくなる。

この結果、半導体素子の歩留りの低下，信頼性の低下をまねき、また素子の微細化に不利になるという問題が生じている。

本発明は所望の配線幅でかつウェハ上において均一な高精度の配線パターンを容易に得ることを可能にした半導体装置の製造方法を提供することを目的とする。

〔課題を解決するための手段〕

本発明の半導体装置の製造方法は、半導体基板上に金属膜を形成する工程と、この金属膜上に所望の配線パターンのフォトレジスト膜パターン及びダミーのフォトレジスト膜パターンを形成する工程と、これらフォトレジスト膜パターン及びダミーパターンをマスクにして金属膜を反応性イオ

ンエッチング法によりエッチングする工程とを含んでおり、このダミーパターンにより配線パターンを形成するためのフォトレジスト膜パターンの面積密度を増大させた状態でエッチングを行う。

〔作用〕

上述した製造方法では、フォトレジスト膜のパターンの密度をダミーパターンにより増大させ、エッチングに際してのサイドエッチングやアンダーカットを抑制し、高精度の配線パターンの製造を実現する。

〔実施例〕

次に、本発明を図面を参照して説明する。

第1図（a）乃至（d）は本発明の第1実施例を製造工程順に示す縦断面図である。ここでは、配線パターンをアルミニウム膜で形成する例について説明する。

先ず、第1図（a）のように、半導体基板1の表面に成長させたシリコン酸化膜2上の全面にアルミニウム膜3を形成し、かつこの上にフォトレジスト膜4をパターン形成している。ここで、フ

ォトレジスト膜4は配線パターンの形成に必要とされるパターン4aに加えて、本来不要とされる部分にもダミーパターン4bを形成している。

このダミーパターン4bは任意に形成することが可能であるが、このダミーパターン4bにより形成されるアルミニウムパターンを後に除去する必要がある場合は、その除去が容易なように、本来のパターン4aから適切に離しておくことが必要である。例えば3μm程度以上離しておげば充分である。

このダミーパターン4bを設けることにより、本来のパターン4aのパターン密度が10%の場合にも、パターン全体の密度を60%に増大することが可能となる。

次いで、同図（b）のように、前記各フォトレジスト膜のパターン4a，4bをマスクにして反応性イオンエッチングを施し、アルミニウム膜3で配線パターン3a及びダミー配線パターン3bを形成する。このとき、上述のようにフォトレジスト膜4のパターン密度が充分に大きいため、配

線パターン３ａ及びダミー配線パターン３ｂにおけるアンダーカットやサイドエッチングは抑制され、パターン４ａ，４ｂと殆ど等しい幅寸法に形成される。

その後、フォトレジストのパターン４ａ，４ｂを除去し、更にダミー配線パターン３ｂをも除去する場合は、同図（ｃ）のように、本来の配線パターン３ａの上部および側面を新たにフォトレジスト膜５で完全に覆う。一方、ダミー配線パターン３ｂはそのまま露出させておき、フォトレジスト膜５をマスクとしてエッチングすることにより、ダミー配線パターン３ｂのみを除去する。これは湿式エッチングにより容易に行える。

次いでフォトレジスト膜５を除去すれば、同図（ｄ）のように、所望の配線パターン３ａを得ることができる。

なお、アルミニウム膜の反応性イオンエッチングにおけるアルミニウム膜とシリコン酸化膜のエッチングレートの選択比はきわめて高く、通常100程度は得られる。このため、ダミー配線パターン３ｂの部分での下地シリコン酸化膜２の凹凸が生じることは殆どない。

なお、ダミー配線パターン３ｂは必ずしも除去する必要はなく、この場合には、第１図（ｃ）及び（ｄ）の工程は不要となる。

第２図（ａ）乃至（ｃ）は本発明の第２実施例を製造工程順に示す縦断面図である。この実施例では、所望とする配線パターンがウェハ上において密度が異なる場合について説明する。

先ず、第２図（ａ）のように、半導体基板１上のシリコン酸化膜２上にアルミニウム膜３を形成し、かつこの上にフォトレジスト膜６をパターン形成している。このフォトレジスト膜６のパターンは、本来必要とされるパターン６ａの密度は場所により密度が異なり、領域Ａでは20%，領域Ｂでは60%である。このため領域Ａでは、パターン密度が領域Ｂと略等しくなるように、領域Ａのパターンと同様なダミーパターン６ｂを設けている。

そして、これらパターン６ａとダミーパターン６ｂをマスクにしてアルミニウム膜３の反応性イ

オンエッチングを施せば、同図（ｂ）のように、領域Ａ，Ｂのいずれにおいても本来の配線パターン３ａを均一な形状にエッチングすることが可能となる。勿論、ダミー配線パターン３ｂも均一にエッチング形成される。

なお、この場合もダミー配線パターン３ｂは必ずしも除去する必要はないが、除去する必要がある場合は、第１実施例１と同様な方法で除去すればよく、この結果同図（ｃ）のように、領域Ａ，Ｂの夫々に所要密度の配線パターン３ａを形成することができる。

〔発明の効果〕

以上説明したように本発明は、フォトレジスト膜のパターンの密度が小さい領域にダミーパターンを配設してパターン密度を所定以上にすることにより、金属膜のエッチングに際してのサイドエッチングやアンダーカットを抑制し、高精度の配線パターンを容易に得ることができる効果がある。

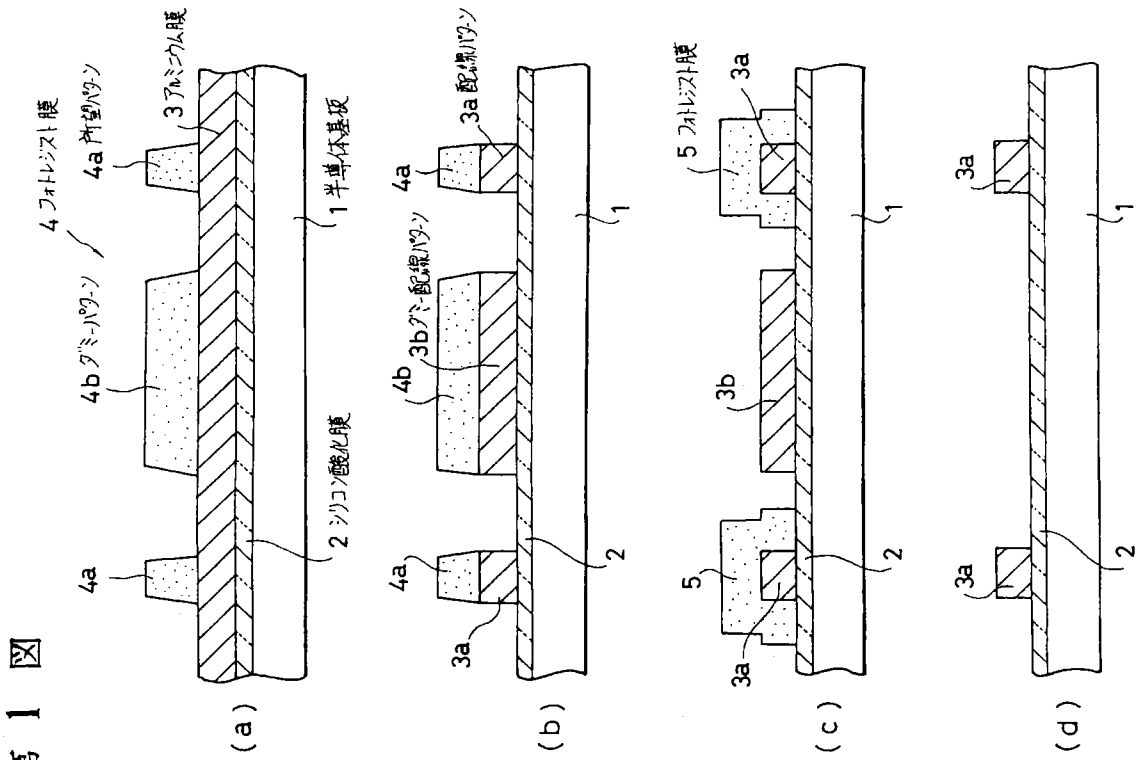
４．図面の簡単な説明

第１図（ａ）乃至（ｄ）は本発明の製造方法の第１実施例を工程順に示す縦断面図、第２図（ａ）乃至（ｃ）は本発明の製造方法の第２実施例を工程順に示す縦断面図、第３図（ａ）及び（ｂ）は従来の製造方法の一例を工程順に示す縦断面図、第４図は従来の製造方法における不具合を説明するための縦断面図である。

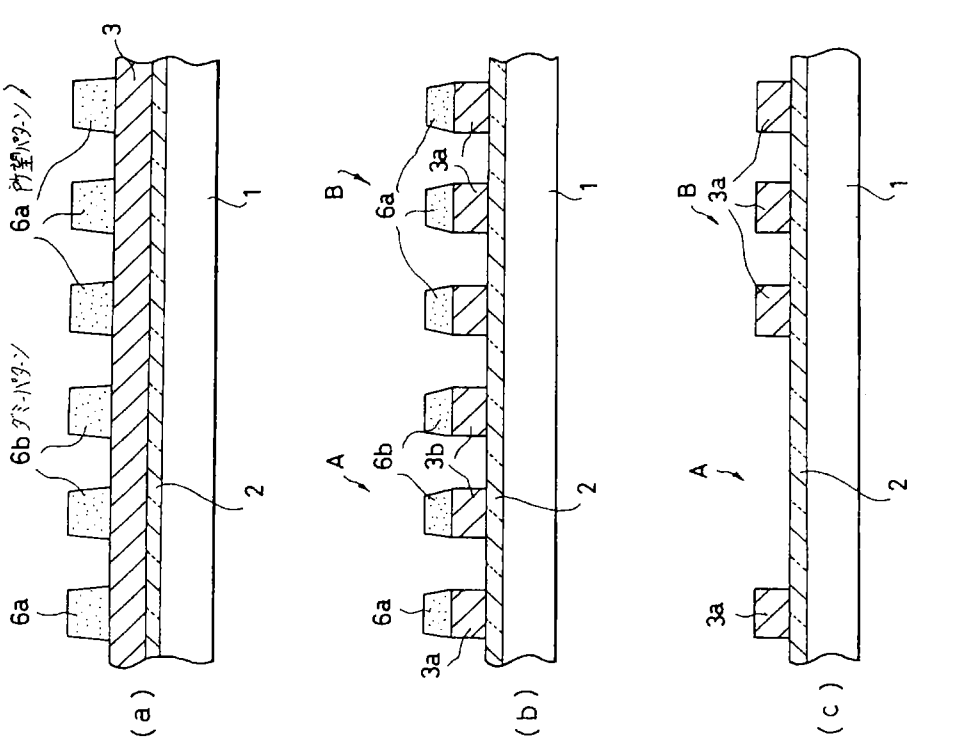
１…半導体基板、２…シリコン酸化膜、３…アルミニウム膜、３ａ…配線パターン、３ｂ…ダミー配線パターン、４…フォトレジスト膜、４ａ…パターン、４ｂ…ダミーパターン、５…フォトレジスト膜、６…フォトレジスト膜、６ａ…パターン、６ｂ…ダミーパターン、７…フォトレジスト膜。

代理人　弁理士　鈴　木　章

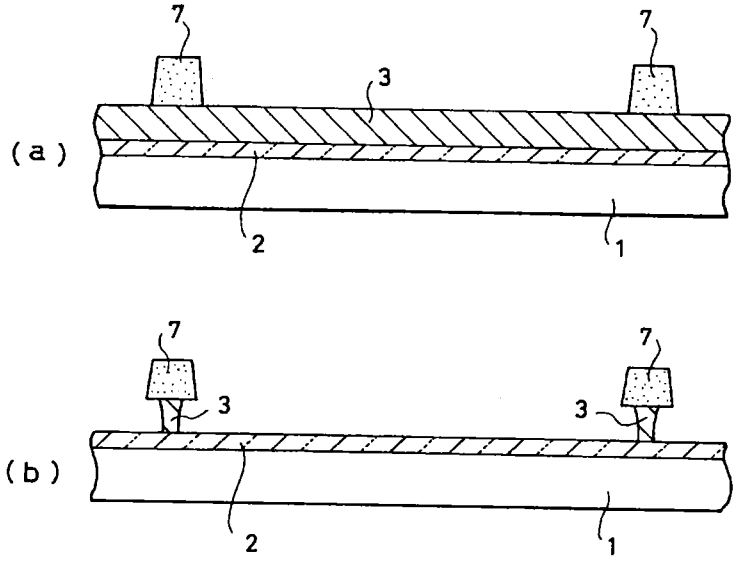
第 1 図


4 フォトレジスト膜
4a
4b ダミーパターン
3 アルミニウム膜
4a 所望パターン
2 シリコン酸化膜
1 半導体基板
(a)
4a
3a
4b
3b ダミー配線パターン
3a 配線パターン
(b)
5
3a
3b
5 フォトレジスト膜
(c)
3a
(d)

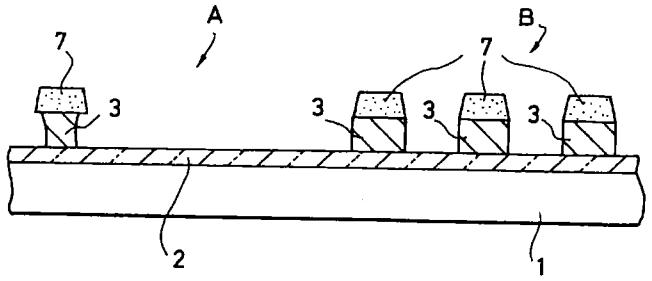
第 2 図


A 領域
B 領域
6 フォトレジスト
6a 所望パターン
6b ダミーパターン
3
1
2
(a)
6a
3a
6b
3b
(b)
(c)

第 3 図



第 4 図



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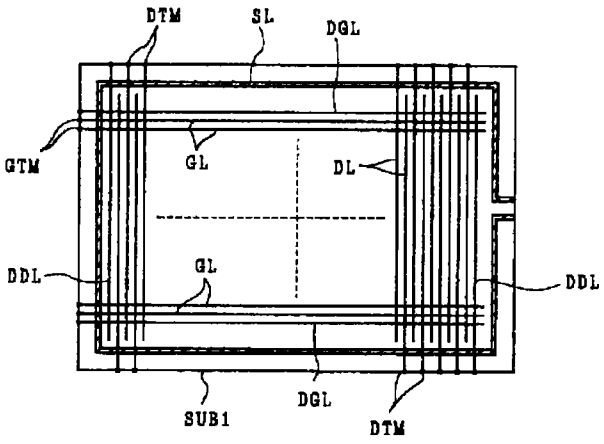
最終頁に続く

(54)【発明の名称】　液晶表示装置

(57)【要約】
【目的】最外側の信号線が断線するのを防止する。
【構成】最外側の走査信号線ＧＬの外側にダミー線ＤＧＬを設け、最外側の映像信号線ＤＬの外側にダミー線ＤＤＬを設け、走査信号線ＧＬ上に陽極酸化膜を設ける。

図１



ＧＬ：走査信号線
ＤＧＬ：ダミー線
ＤＤＬ：ダミー線

1

【特許請求の範囲】

【請求項１】薄膜トランジスタと画素電極とを画素の一構成要素としたアクティブ・マトリクス方式の液晶表示装置において、最外側の信号線の外側にダミー線を設けたことを特徴とする液晶表示装置。

【請求項２】上記信号線が走査信号線であり、上記走査信号線上に陽極酸化膜が設けられたことを特徴とする請求項１に記載の液晶表示装置。

【請求項３】上記信号線が映像信号線であることを特徴とする請求項１に記載の液晶表示装置。

【請求項４】最外側の画素の外側にダミー画素を設け、上記ダミー画素を遮光膜でマスクしたことを特徴とする請求項１に記載の液晶表示装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】この発明は液晶表示装置、特に薄膜トランジスタ等を使用したアクティブ・マトリクス方式の液晶表示装置に関する。

【０００２】

【従来の技術】アクティブ・マトリクス方式の液晶表示装置は、マトリクス状に配列された複数の画素電極のそれぞれに対応して非線形素子（スイッチング素子）を設けたものである。各画素における液晶は理論的には常時駆動（デューティ比１．０）されているので、時分割駆動方式を採用している、いわゆる単純マトリクス方式と比べてアクティブ方式はコントラストが良く、特にカラー液晶表示装置では欠かせない技術となりつつある。スイッチング素子として代表的なものとしては薄膜トランジスタ（ＴＦＴ）がある。

【０００３】従来のアクティブ・マトリクス方式の液晶表示装置においては、最外側の走査信号線、映像信号線に信号を印加している。

【０００４】なお、薄膜トランジスタを使用したアクティブ・マトリクス方式の液晶表示装置は、たとえば「冗長構成を採用した１２．５型アクティブ・マトリクス方式カラー液晶ディスプレイ」、日経エレクトロニクス、頁１９３～２１０、１９８６年１２月１５日、日経マグロウヒル社発行、で知られている。

【０００５】

【発明が解決しようとする課題】しかし、このような液晶表示装置においては、最外側の走査信号線、映像信号線以外の走査信号線、映像信号線は両側に走査信号線、映像信号線が存在するのに対して、最外側の走査信号線、映像信号線は片側にのみ走査信号線、映像信号線が存在するから、走査信号線、映像信号線を形成する際に、最外側の走査信号線、映像信号線は他の走査信号線、映像信号線と比較してホトレジストの形成条件、エッチング条件等が相違するので、最外側の走査信号線、映像信号線が断線することがある。また、特開昭５８－１９７１０６号公報、特開昭６３－１６４号公報に示されるように、アルミニウムまたはアルミニウムを主成分とする材料からなる走査信号線上にアルミニウムの陽極酸化膜を設けたときには、陽極酸化の際に最外側の走査信号線部における電界が不均一になり、また最外側の走査信号線は陽極酸化のマスキングに使用するホトレジストの端部に近いから、最外側の走査信号線にホトレジストの形成の際に汚れが付きやすいので、走査信号線上に陽極酸化膜を設けるときに、最外側の走査信号線が断線することがある。

2

【０００６】この発明は上述の課題を解決するためになされたもので、最外側の信号線が断線することがない液晶表示装置を提供することを目的とする。

【０００７】

【課題を解決するための手段】この目的を達成するため、この発明においては、薄膜トランジスタと画素電極とを画素の一構成要素としたアクティブ・マトリクス方式の液晶表示装置において、最外側の信号線の外側にダミー線を設ける。

【０００８】この場合、上記信号線を走査信号線とし、上記走査信号線上に陽極酸化膜を設けてもよい。

【０００９】また、上記信号線を映像信号線としてもよい。

【００１０】また、最外側の画素の外側にダミー画素を設け、上記ダミー画素を遮光膜でマスクしてもよい。

【００１１】

【作用】この液晶表示装置においては、最外側の信号線もそれ以外の信号線と同様に両側に線が存在するから、信号線を形成する際に、最外側の信号線と他の信号線とはホトレジストの形成条件、エッチング条件等が同一になる。

【００１２】また、信号線を走査信号線とし、走査信号線上に陽極酸化膜を設けたときには、陽極酸化の際に最外側の走査信号線部における電界が不均一になることがなく、またホトレジスト形成の際に最外側の信号線に汚れが付きにくい。

【００１３】

【実施例】以下、この発明の構成について、アクティブ・マトリクス方式のカラー液晶表示装置にこの発明を適用した実施例とともに説明する。

【００１４】なお、実施例を説明するための全図において、同一機能を有するものは同一符号を付け、その繰り返しの説明は省略する。

【００１５】図２はこの発明が適用されるアクティブ・マトリクス方式カラー液晶表示装置の一画素とその周辺を示す平面図、図３は図２の３－３切断線における断面と表示パネルのシール部付近の断面を示す図、図４は図２の４－４切断線における断面図である。また、図７（要部平面図）には図２に示す画素を複数配置したときの平面図を示す。

【００１６】（画素配置）図２に示すように、各画素は

隣接する２本の走査信号線（ゲート信号線または水平信号線）ＧＬと、隣接する２本の映像信号線（ドレイン信号線または垂直信号線）ＤＬとの交差領域内（４本の信号線で囲まれた領域内）に配置されている。各画素は薄膜トランジスタＴＦＴ、透明画素電極ＩＴＯ１および保持容量素子Ｃaddを含む。走査信号線ＧＬは列方向に延在し、行方向に複数本配置されている。映像信号線ＤＬは行方向に延在し、列方向に複数本配置されている。

【００１７】（表示部断面全体構造）図３に示すように、液晶ＬＣを基準に下部透明ガラス基板ＳＵＢ１側には薄膜トランジスタＴＦＴおよび透明画素電極ＩＴＯ１が形成され、上部透明ガラス基板ＳＵＢ２側にはカラーフィルタＦＩＬ、遮光用ブラックマトリクスパターンを形成する遮光膜ＢＭが形成されている。下部透明ガラス基板ＳＵＢ１はたとえば１．１㎜程度の厚さで構成されている。また、透明ガラス基板ＳＵＢ１、ＳＵＢ２の両面にはディップ処理等によって形成された酸化シリコン膜ＳＩＯが設けられている。このため、透明ガラス基板ＳＵＢ１、ＳＵＢ２の表面に鋭い傷があったとしても、鋭い傷を酸化シリコン膜ＳＩＯで覆うことができるので、走査信号線ＧＬ、カラーフィルタＦＩＬが損傷するのを有効に防止することができる。

【００１８】図３の中央部は一画素部分の断面を示しているが、左側は透明ガラス基板ＳＵＢ１、ＳＵＢ２の左側縁部分で外部引出配線の存在する部分の断面を示しており、右側は透明ガラス基板ＳＵＢ１、ＳＵＢ２の右側縁部分で外部引出配線の存在しない部分の断面を示している。

【００１９】図３の左側、右側のそれぞれに示すシール材ＳＬは液晶ＬＣを封止するように構成されており、液晶封入口（図示せず）を除く透明ガラス基板ＳＵＢ１、ＳＵＢ２の縁周囲全体に沿って形成されている。シール材ＳＬはたとえばエポキシ樹脂で形成されている。

【００２０】上部透明ガラス基板ＳＵＢ２側の共通透明画素電極ＩＴＯ２は、少なくとも一個所において、銀ペースト材ＳＩＬによって下部透明ガラス基板ＳＵＢ１側に形成された外部引出配線に接続されている。この外部引出配線はゲート電極ＧＴ、ソース電極ＳＤ１、ドレイン電極ＳＤ２のそれぞれと同一製造工程で形成される。

【００２１】配向膜ＯＲＩ１、ＯＲＩ２、透明画素電極ＩＴＯ１、共通透明画素電極ＩＴＯ２、保護膜ＰＳＶ１、ＰＳＶ２、絶縁膜ＧＩのそれぞれの層は、シール材ＳＬの内側に形成される。偏光板ＰＯＬ１、ＰＯＬ２はそれぞれ下部透明ガラス基板ＳＵＢ１、上部透明ガラス基板ＳＵＢ２の外側の表面に形成されている。

【００２２】液晶ＬＣは液晶分子の向きを設定する下部配向膜ＯＲＩ１と上部配向膜ＯＲＩ２との間に封入され、シール部ＳＬによってシールされている。

【００２３】下部配向膜ＯＲＩ１は下部透明ガラス基板ＳＵＢ１側の保護膜ＰＳＶ１の上部に形成される。

【００２４】上部透明ガラス基板ＳＵＢ２の内側（液晶ＬＣ側）の表面には、遮光膜ＢＭ、カラーフィルタＦＩＬ、保護膜ＰＳＶ２、共通透明画素電極ＩＴＯ２（ＣＯＭ）および上部配向膜ＯＲＩ２が順次積層して設けられている。

【００２５】この液晶表示装置は下部透明ガラス基板ＳＵＢ１側、上部透明ガラス基板ＳＵＢ２側のそれぞれの層を別々に形成し、その後上下透明ガラス基板ＳＵＢ１、ＳＵＢ２を重ね合わせ、両者間に液晶ＬＣを封入することによって組み立てられる。

【００２６】（薄膜トランジスタＴＦＴ）薄膜トランジスタＴＦＴは、ゲート電極ＧＴに正のバイアスを印加すると、ソース－ドレイン間のチャネル抵抗が小さくなり、バイアスを零にすると、チャネル抵抗は大きくなるように動作する。

【００２７】各画素の薄膜トランジスタＴＦＴは、画素内において２つ(複数)に分割され、薄膜トランジスタ（分割薄膜トランジスタ）ＴＦＴ１およびＴＦＴ２で構成されている。薄膜トランジスタＴＦＴ１、ＴＦＴ２のそれぞれは実質的に同一サイズ（チャネル長、幅が同じ）で構成されている。この分割された薄膜トランジスタＴＦＴ１、ＴＦＴ２のそれぞれは、主にゲート電極ＧＴ、ゲート絶縁膜ＧＩ、ｉ型（真性、intrinsic、導電型決定不純物がドープされていない）非晶質シリコン（Ｓｉ）からなるｉ型半導体層ＡＳ、一対のソース電極ＳＤ１、ドレイン電極ＳＤ２で構成されている。なお、ソース・ドレインは本来その間のバイアス極性によって決まり、この液晶表示装置の回路ではその極性は動作中反転するので、ソース・ドレインは動作中入れ替わると理解されたい。しかし、以下の説明でも、便宜上一方をソース、他方をドレインと固定して表現する。

【００２８】（ゲート電極ＧＴ）ゲート電極ＧＴは図８（図２の第２導電膜ｇ２およびｉ型半導体層ＡＳのみを描いた平面図）に詳細に示すように、走査信号線ＧＬから垂直方向（図２および図８において上方向）に突出する形状で構成されている（Ｔ字形状に分岐されている）。ゲート電極ＧＴは薄膜トランジスタＴＦＴ１、ＴＦＴ２のそれぞれの形成領域まで突出するように構成されている。薄膜トランジスタＴＦＴ１、ＴＦＴ２のそれぞれのゲート電極ＧＴは、一体に（共通ゲート電極として）構成されており、走査信号線ＧＬに連続して形成されている。ゲート電極ＧＴは、単層の第２導電膜ｇ２で構成する。第２導電膜ｇ２はたとえばスパッタで形成されたアルミニウム膜を用い、１０００～５５００Å程度の膜厚で形成する。また、ゲート電極ＧＴ上にはアルミニウムの陽極酸化膜ＡＯＦが設けられている。

【００２９】このゲート電極ＧＴは図２、図３および図８に示されているように、ｉ型半導体層ＡＳを完全に覆うよう（下方からみて）それより大き目に形成される。したがって、下部透明ガラス基板ＳＵＢ１の下方に蛍光

灯等のバックライトＢＬを取り付けた場合、この不透明なアルミニウムからなるゲート電極ＧＴが影となって、ｉ型半導体層ＡＳにはバックライト光が当たらず、光照射による導電現象すなわち薄膜トランジスタＴＦＴのオフ特性劣化は起きにくくなる。なお、ゲート電極ＧＴの本来の大きさは、ソース電極ＳＤ１とドレイン電極ＳＤ２との間をまたがるに最低限必要な（ゲート電極ＧＴとソース電極ＳＤ１、ドレイン電極ＳＤ２との位置合わせ余裕分も含めて）幅を持ち、チャネル幅Ｗを決めるその奥行き長さはソース電極ＳＤ１とドレイン電極ＳＤ２との間の距離（チャネル長）Ｌとの比、すなわち相互コンダクタンスgmを決定するファクタＷ／Ｌをいくつにするかによって決められる。

【００３０】この液晶表示装置におけるゲート電極ＧＴの大きさはもちろん、上述した本来の大きさよりも大きくされる。

【００３１】（走査信号線ＧＬ）走査信号線ＧＬは第２導電膜ｇ２で構成されている。この走査信号線ＧＬの第２導電膜ｇ２はゲート電極ＧＴの第２導電膜ｇ２と同一製造工程で形成され、かつ一体に構成されている。また、走査信号線ＧＬ上にはアルミニウムの陽極酸化膜ＡＯＦが設けられている。

【００３２】（ダミー線ＤＧＬ、ＤＤＬ）図１に示すように、最外側の走査信号線ＧＬの外側にダミー線ＤＧＬが設けられており、また最外側の映像信号線ＤＬの外側にダミー線ＤＤＬが設けられている。

【００３３】このように、最外側の走査信号線ＧＬ、映像信号線ＤＬの外側にダミー線ＤＧＬ、ＤＤＬが設けられているから、最外側の走査信号線ＧＬ、映像信号線ＤＬもそれ以外の走査信号線ＧＬ、映像信号線ＤＬと同様に、両側に線ＧＬ、ＤＧＬ、線ＤＬ、ＤＤＬが存在する。このため、走査信号線ＧＬ、映像信号線ＤＬを形成する際に、最外側の走査信号線ＧＬ、映像信号線ＤＬと他の走査信号線ＧＬ、映像信号線ＤＬとはホトレジストの形成条件、エッチング条件等が同一になるから、最外側の走査信号線ＧＬ、映像信号線ＤＬが断線することがない。また、走査信号線ＧＬ上に陽極酸化膜ＡＯＦを設けるための陽極酸化の際に、最外側の走査信号線ＧＬ部における電界が不均一になることがなく、また陽極酸化のマスキングに使用するホトレジスト形成の際に、最外側の走査信号線ＧＬに汚れが付きにくいから、走査信号線ＧＬ上に陽極酸化膜ＡＯＦを設けるときに、最外側の走査信号線ＧＬが断線することがない。

【００３４】なお、走査信号線ＧＬ、映像信号線ＤＬを形成する際、走査信号線ＧＬ上に陽極酸化膜ＡＯＦを設ける際に、ダミー線ＤＧＬ、ＤＤＬが断線することはあるが、ダミー線ＤＧＬ、ＤＤＬが断線したとしても、液晶表示装置の表示品質には影響を与えない。また、ダミー線ＤＧＬ、ＤＤＬはパネル枠または遮光膜ＢＭのよってマスクされている。

【００３５】（絶縁膜ＧＩ）絶縁膜ＧＩは薄膜トランジスタＴＦＴ１、ＴＦＴ２のそれぞれのゲート絶縁膜として使用される。絶縁膜ＧＩはゲート電極ＧＴおよび走査信号線ＧＬの上層に形成されている。絶縁膜ＧＩはたとえばプラズマＣＶＤで形成された窒化シリコン膜を用い、３０００Å程度の膜厚で形成する。

【００３６】（ｉ型半導体層ＡＳ）ｉ型半導体層ＡＳは、図８に示すように、複数に分割された薄膜トランジスタＴＦＴ１、ＴＦＴ２のそれぞれのチャネル形成領域として使用される。ｉ型半導体層ＡＳは非晶質シリコン膜または多結晶シリコン膜で形成し、約１８００Å程度の膜厚で形成する。

【００３７】このｉ型半導体層ＡＳは、供給ガスの成分を変えてSi_3N_4からなるゲート絶縁膜として使用される絶縁膜ＧＩの形成に連続して、同じプラズマＣＶＤ装置で、しかもそのプラズマＣＶＤ装置から外部に露出することなく形成される。また、オーミックコンタクト用のリン（Ｐ）をドープしたＮ(＋)型半導体層ｄ０（図３）も同様に連続して約４００Åの厚さに形成される。しかる後、下部透明ガラス基板ＳＵＢ１はＣＶＤ装置から外に取り出され、写真処理技術によりＮ(＋)型半導体層ｄ０およびｉ型半導体層ＡＳは図２、図３および図８に示すように独立した島状にパターニングされる。

【００３８】ｉ型半導体層ＡＳは、図２および図８に詳細に示すように、走査信号線ＧＬと映像信号線ＤＬとの交差部（クロスオーバ部）の両者間にも設けられている。この交差部のｉ型半導体層ＡＳは交差部における走査信号線ＧＬと映像信号線ＤＬとの短絡を低減するように構成されている。

【００３９】（ソース電極ＳＤ１、ドレイン電極ＳＤ２）複数に分割された薄膜トランジスタＴＦＴ１、ＴＦＴ２のそれぞれのソース電極ＳＤ１とドレイン電極ＳＤ２とは、図２、図３および図９（図２の第１～第３導電膜ｄ１～ｄ３のみを描いた平面図）で詳細に示すように、ｉ型半導体層ＡＳ上にそれぞれ離隔して設けられている。

【００４０】ソース電極ＳＤ１、ドレイン電極ＳＤ２のそれぞれは、Ｎ(＋)型半導体層ｄ０に接触する下層側から、第１導電膜ｄ１、第２導電膜ｄ２、第３導電膜ｄ３を順次重ね合わせて構成されている。ソース電極ＳＤ１の第１導電膜ｄ１、第２導電膜ｄ２および第３導電膜ｄ３は、ドレイン電極ＳＤ２の第１導電膜ｄ１、第２導電膜ｄ２および第３導電膜ｄ３と同一製造工程で形成される。

【００４１】第１導電膜ｄ１はスパッタで形成したクロム膜を用い、５００～１０００Åの膜厚（この液晶表示装置では、６００Å程度の膜厚）で形成する。クロム膜は膜厚を厚く形成するとストレスが大きくなるので、２０００Å程度の膜厚を越えない範囲で形成する。クロム膜はＮ(＋)型半導体層ｄ０との接触が良好である。クロ

ム膜は後述する第２導電膜ｄ２のアルミニウムがN(＋)型半導体層ｄ０に拡散することを防止するいわゆるバリア層を構成する。第１導電膜ｄ１としては、クロム膜の他に高融点金属（Ｍｏ、Ｔｉ、Ｔａ、Ｗ）膜、高融点金属シリサイド（$MoSi_2$、$TiSi_2$、$TaSi_2$、WSi_2）膜で形成してもよい。

【００４２】第１導電膜ｄ１を写真処理でパターニングした後、同じ写真処理用マスクを用いて、あるいは第１導電膜ｄ１をマスクとして、N(＋)型半導体層ｄ０が除去される。つまり、ｉ型半導体層ＡＳ上に残っていたN(＋)型半導体層ｄ０は第１導電膜ｄ１以外の部分がセルフアラインで除去される。このとき、N(＋)型半導体層ｄ０はその厚さ分は全て除去されるようエッチされるので、ｉ型半導体層ＡＳも若干その表面部分でエッチされるが、その程度はエッチ時間で制御すればよい。

【００４３】しかる後、第２導電膜ｄ２がアルミニウムのスパッタリングで３０００～５５００Åの膜厚（この液晶表示装置では、３５００Å程度の膜厚）に形成される。アルミニウム膜はクロム膜に比べてストレスが小さく、厚い膜厚に形成することが可能で、ソース電極ＳＤ１、ドレイン電極ＳＤ２および映像信号線ＤＬの抵抗値を低減するように構成されている。第２導電膜ｄ２としてはアルミニウム膜の他にシリコンや銅（Ｃｕ）を添加物として含有させたアルミニウム膜で形成してもよい。

【００４４】第２導電膜ｄ２の写真処理技術によるパターニング後、第３導電膜ｄ３が形成される。この第３導電膜ｄ３はスパッタリングで形成された透明導電膜（Indium-Tin-Oxide　ＩＴＯ：ネサ膜）からなり、１０００～２０００Åの膜厚（この液晶表示装置では、１２００Å程度の膜厚）で形成される。この第３導電膜ｄ３はソース電極ＳＤ１、ドレイン電極ＳＤ２および映像信号線ＤＬを構成するとともに、透明画素電極ＩＴＯ１を構成するようになっている。

【００４５】ソース電極ＳＤ１の第１導電膜ｄ１、ドレイン電極ＳＤ２の第１導電膜ｄ１のそれぞれは、上層の第２導電膜ｄ２および第３導電膜ｄ３に比べて内側に（チャネル領域内に）大きく入り込んでいる。つまり、これらの部分における第１導電膜ｄ１は第２導電膜ｄ２、第３導電膜ｄ３とは無関係に薄膜トランジスタＴＦＴのチャネル長Ｌを規定できるように構成されている。

【００４６】ソース電極ＳＤ１は透明画素電極ＩＴＯ１に接続されている。ソース電極ＳＤ１は、ｉ型半導体層ＡＳの段差形状（第１導電膜ｇ１の膜厚、N(＋)型半導体層ｄ０の膜厚およびｉ型半導体層ＡＳの膜厚を加算した膜厚に相当する段差）に沿って構成されている。具体的には、ソース電極ＳＤ１は、ｉ型半導体層ＡＳの段差形状に沿って形成された第１導電膜ｄ１と、この第１導電膜ｄ１の上部にそれに比べて透明画素電極ＩＴＯ１と接続される側を小さいサイズで形成した第２導電膜ｄ２とで、この第２導電膜ｄ２から露出する第１導電膜ｄ１に接続された第３導電膜ｄ３とで構成されている。ソース電極ＳＤ１の第２導電膜ｄ２は第１導電膜ｄ１のクロム膜がストレスの増大から厚く形成できず、ｉ型半導体層ＡＳの段差形状を乗り越えられないので、このｉ型半導体層ＡＳを乗り越えるために構成されている。つまり、第２導電膜ｄ２は厚く形成することでステップカバレッジを向上している。第２導電膜ｄ２は厚く形成できるので、ソース電極ＳＤ１の抵抗値（ドレイン電極ＳＤ２や映像信号線ＤＬについても同様）の低減に大きく寄与している。第３導電膜ｄ３は第２導電膜ｄ２のｉ型半導体層ＡＳに起因する段差形状を乗り越えることができないので、第２導電膜ｄ２のサイズを小さくすることで、露出する第１導電膜ｄ１に接続するように構成されている。第１導電膜ｄ１と第３導電膜ｄ３とは接着性が良好であるばかりか、両者間の接続部の段差形状が小さいので、ソース電極ＳＤ１と透明画素電極ＩＴＯ１とを確実に接続することができる。

【００４７】（透明画素電極ＩＴＯ１）透明画素電極ＩＴＯ１は液晶表示部の画素電極の一方を構成する。

【００４８】透明画素電極ＩＴＯ１は薄膜トランジスタＴＦＴ１のソース電極ＳＤ１および薄膜トランジスタＴＦＴ２のソース電極ＳＤ１に接続されている。このため、薄膜トランジスタＴＦＴ１、ＴＦＴ２のうちの１つたとえば薄膜トランジスタＴＦＴ１に欠陥が発生したときには、製造工程においてレーザ光等によって、薄膜トランジスタＴＦＴ１と映像信号線ＤＬとを切り離すとともに、薄膜トランジスタＴＦＴ１と透明画素電極ＩＴＯ１とを切り離せば、点欠陥、線欠陥にはならず、しかも２つの薄膜トランジスタＴＦＴ１、ＴＦＴ２に同時に欠陥が発生することはほとんどないから、点欠陥が発生する確率を極めて小さくすることができる。

【００４９】（保護膜ＰＳＶ１）薄膜トランジスタＴＦＴおよび透明画素電極ＩＴＯ１上には保護膜ＰＳＶ１が設けられている。保護膜ＰＳＶ１は主に薄膜トランジスタＴＦＴを湿気等から保護するために形成されており、透明性が高くしかも耐湿性の良いものを使用する。保護膜ＰＳＶ１はたとえばプラズマＣＶＤ装置で形成した酸化シリコン膜や窒化シリコン膜で形成されており、８０００Å程度の膜厚で形成する。

【００５０】（ゲート端子ＧＴＭ、ドレイン端子ＤＴＭ）図５に示すように、ゲート端子ＧＴＭは第１導電膜ｇ１と第３導電膜ｄ３とで構成されている。

【００５１】また、図６に示すように、ドレイン端子ＤＴＭは第１導電膜ｇ１と第３導電膜ｄ３とで構成されている。

【００５２】第１導電膜ｇ１はたとえばスパッタで形成されたクロム（Ｃｒ）膜を用い、１０００Å程度の膜厚で形成する。

【００５３】（遮光膜ＢＭ）上部透明ガラス基板ＳＵＢ２側には、外部光（図３では上方からの光）がチャネル

形成領域として使用されるｉ型半導体層ＡＳに入射されないように、遮光膜ＢＭが設けられ、遮光膜ＢＭは図１０のハッチングに示すようなパターンとされている。なお、図１０は図２におけるＩＴＯ膜からなる第３導電膜ｄ３、カラーフィルタＦＩＬおよび遮光膜ＢＭのみを描いた平面図である。遮光膜ＢＭは光に対する遮蔽性が高いたとえばアルミニウム膜やクロム膜等で形成されており、この液晶表示装置ではクロム膜がスパッタリングで１３００Å程度の膜厚に形成される。

【００５４】したがって、薄膜トランジスタＴＦＴ１、ＴＦＴ２のｉ型半導体層ＡＳは上下にある遮光膜ＢＭおよび大き目のゲート電極ＧＴによってサンドイッチにされ、その部分は外部の自然光やバックライト光が当たらなくなる。遮光膜ＢＭは図１０のハッチング部分で示すように、画素の周囲に形成され、つまり遮光膜ＢＭは格子状に形成され（ブラックマトリクス）、この格子で１画素の有効表示領域が仕切られている。したがって、各画素の輪郭が遮光膜ＢＭによってはっきりとし、コントラストが向上する。つまり、遮光膜ＢＭはｉ型半導体層ＡＳに対する遮光とブラックマトリクスとの２つの機能をもつ。

【００５５】また、透明画素電極ＩＴＯ１のラビング方向の根本側のエッジ部に対向する部分（図２右下部分）が遮光膜ＢＭによって遮光されているから、上記部分にドメインが発生したとしても、ドメインが見えないので、表示特性が劣化することはない。

【００５６】なお、バックライトを上部透明ガラス基板ＳＵＢ２側に取り付け、下部透明ガラス基板ＳＵＢ１を観察側（外部露出側）とすることもできる。

【００５７】（共通透明画素電極ＩＴＯ２）共通透明画素電極ＩＴＯ２は、下部透明ガラス基板ＳＵＢ１側に画素ごとに設けられた透明画素電極ＩＴＯ１に対向し、液晶ＬＣの光学的な状態は各画素電極ＩＴＯ１と共通透明画素電極ＩＴＯ２との間の電位差（電界）に応答して変化する。この共通透明画素電極ＩＴＯ２にはコモン電圧Ｖcomが印加されるように構成されている。コモン電圧Ｖcomは映像信号線ＤＬに印加されるロウレベルの駆動電圧Ｖｄminとハイレベルの駆動電圧Ｖｄmaxとの中間電位である。

【００５８】（カラーフィルタＦＩＬ）カラーフィルタＦＩＬはアクリル樹脂等の樹脂材料で形成される染色基材に染料を着色して構成されている。カラーフィルタＦＩＬは画素に対向する位置にストライプ状に形成され（図１１）、染め分けられている（図１１は図７の第３導電膜層ｄ３、遮光膜ＢＭおよびカラーフィルタＦＩＬのみを描いたもので、Ｂ、Ｒ、Ｇの各カラーフィルターＦＩＬはそれぞれ、４５°、１３５°、クロスのハッチを施してある）。カラーフィルタＦＩＬは図１０に示すように透明画素電極ＩＴＯ１の全てを覆うように大き目に形成され、遮光膜ＢＭはカラーフィルタＦＩＬおよび透明画素電極ＩＴＯ１のエッジ部分と重なるよう透明画素電極ＩＴＯ１の周縁部より内側に形成されている。

【００５９】カラーフィルタＦＩＬは次のように形成することができる。まず、上部透明ガラス基板ＳＵＢ２の表面に染色基材を形成し、フォトリソグラフィ技術で赤色フィルタ形成領域以外の染色基材を除去する。この後、染色基材を赤色染料で染め、固着処理を施し、赤色フィルタＲを形成する。つぎに、同様な工程を施すことによって、緑色フィルタＧ、青色フィルタＢを順次形成する。

【００６０】（保護膜ＰＳＶ２）保護膜ＰＳＶ２はカラーフィルタＦＩＬを異なる色に染め分けた染料が液晶ＬＣに漏れることを防止するために設けられている。保護膜ＰＳＶ２はたとえばアクリル樹脂、エポキシ樹脂等の透明樹脂材料で形成されている。

【００６１】（表示装置全体等価回路）表示マトリクス部の等価回路とその周辺回路の結線図を図１２に示す。同図は回路図ではあるが、実際の幾何学的配置に対応して描かれている。ＡＲは複数の画素を二次元状に配列したマトリクス・アレイである。

【００６２】図中、Ｘは映像信号線ＤＬを意味し、添字Ｇ、ＢおよびＲがそれぞれ緑、青および赤画素に対応して付加されている。Ｙは走査信号線ＧＬを意味し、添字１，２，３，…，endは走査タイミングの順序に従って付加されている。

【００６３】映像信号線Ｘ（添字省略）は交互に上側（または奇数）映像信号駆動回路Ｈｅ、下側（または偶数）映像信号駆動回路Ｈｏに接続されている。

【００６４】ＳＵＰは１つの電圧源から複数の分圧した安定化された電圧源を得るための電源回路やホスト（上位演算処理装置）からのＣＲＴ（陰極線管）用の情報をＴＦＴ液晶表示装置用の情報に交換する回路を含む回路である。

【００６５】（保持容量素子Ｃaddの構造）透明画素電極ＩＴＯ１は、薄膜トランジスタＴＦＴと接続される端部と反対側の端部において、隣りの走査信号線ＧＬと重なるように形成されている。この重ね合わせは、図４からも明らかなように、透明画素電極ＩＴＯ１を一方の電極ＰＬ２とし、隣りの走査信号線ＧＬを他方の電極ＰＬ１とする保持容量素子（静電容量素子）Ｃaddを構成する。この保持容量素子Ｃaddの誘電体膜は、薄膜トランジスタＴＦＴのゲート絶縁膜として使用される絶縁膜ＧＩおよび陽極酸化膜ＡＯＦで構成されている。

【００６６】保持容量素子Ｃaddは、図８からも明らかなように、走査信号線ＧＬの第２導電膜ｇ２の幅を広げた部分に形成されている。なお、映像信号線ＤＬと交差する部分の第２導電膜ｇ２は映像信号線ＤＬとの短絡の確率を小さくするため細くされている。

【００６７】保持容量素子Ｃaddを構成するために重ね合わされる透明画素電極ＩＴＯ１と電極ＰＬ１との間の

一部には、ソース電極ＳＤ１と同様に、段差形状を乗り越える際に透明画素電極ＩＴＯ１が断線しないように、第１導電膜ｄ１および第２導電膜ｄ２で構成された島領域が設けられている。この島領域は、透明画素電極ＩＴＯ１の面積（開口率）を低下しないように、できる限り小さく構成する。（保持容量素子Ｃaddの等価回路とその動作）図２に示される画素の等価回路を図１３に示す。図１３において、Ｃgsは薄膜トランジスタＴＦＴのゲート電極ＧＴとソース電極ＳＤ１との間に形成される寄生容量である。寄生容量Ｃgsの誘電体膜は絶縁膜ＧＩである。Ｃpixは透明画素電極ＩＴＯ１（ＰＩＸ）と共通透明画素電極ＩＴＯ２（ＣＯＭ）との間に形成される液晶容量である。液晶容量Ｃpixの誘電体膜は液晶ＬＣ、保護膜ＰＳＶ１および配向膜ＯＲＩ１、ＯＲＩ２である。Ｖlcは中点電位である。

【００６８】保持容量素子Ｃaddは、薄膜トランジスタＴＦＴがスイッチングするとき、中点電位（画素電極電位）Ｖlcに対するゲート電位変化ΔＶgの影響を低減するように働く。この様子を式で表すと、次式のようになる。

【００６９】

$$\Delta Vlc = \{Cgs/(Cgs+Cadd+Cpix)\} \times \Delta Vg$$

ここで、ΔＶlcはΔＶgによる中点電位の変化分を表わす。この変化分ΔＶlcは液晶ＬＣに加わる直流成分の原因となるが、保持容量Ｃaddを大きくすればする程、その値を小さくすることができる。また、保持容量素子Ｃaddは放電時間を長くする作用もあり、薄膜トランジスタＴＦＴがオフした後の映像情報を長く蓄積する。液晶ＬＣに印加される直流成分の低減は、液晶ＬＣの寿命を向上し、液晶表示画面の切り替え時に前の画像が残るいわゆる焼き付きを低減することができる。

【００７０】前述したように、ゲート電極ＧＴはｉ型半導体層ＡＳを完全に覆うよう大きくされている分、ソース電極ＳＤ１、ドレイン電極ＳＤ２とのオーバラップ面積が増え、したがって寄生容量Ｃgsが大きくなり、中点電位Ｖlcはゲート（走査）信号Ｖgの影響を受け易くなるという逆効果が生じる。しかし、保持容量素子Ｃaddを設けることによりこのデメリットも解消することができる。

【００７１】保持容量素子Ｃaddの保持容量は、画素の書込特性から、液晶容量Ｃpixに対して４～８倍（$4 \cdot Cpix < Cadd < 8 \cdot Cpix$）、寄生容量Ｃgsに対して８～３２倍（$8 \cdot Cgs < Cadd < 32 \cdot Cgs$）程度の値に設定する。

【００７２】（保持容量素子Ｃadd電極線の結線方法）保持容量電極線としてのみ使用される初段の走査信号線ＧＬ（Y_0）は、図１２に示すように、共通透明画素電極ＩＴＯ２（Ｖcom）に接続する。共通透明画素電極ＩＴＯ２は、図３に示すように、液晶表示装置の周縁部において銀ペースト材ＳＬによって外部引出配線に接続されている。しかも、この外部引出配線の一部の導電膜（ｇ１およびｇ２）は走査信号線ＧＬと同一製造工程で構成されている。この結果、最終段の保持容量電極線ＧＬは、共通透明画素電極ＩＴＯ２に簡単に接続することができる。

【００７３】初段の保持容量電極線Y_0は最終段の走査信号線Ｙendに接続、Ｖcom以外の直流電位点（交流接地点）に接続するかまたは垂直走路回路Ｖから１つ余分に走査パルスY_0を受けるように接続してもよい。

【００７４】つぎに、この発明に係る液晶表示装置の製造方法について説明する。まず、７０５９ガラス（商品名）からなる下部透明ガラス基板ＳＵＢ１の両面に酸化シリコン膜ＳｉＯをディップ処理により設けたのち、５００℃、６０分間のベークを行なう。つぎに、下部透明ガラス基板ＳＵＢ１上に膜厚が１１００Åのクロムからなる第１導電膜ｇ１をスパッタリングにより設ける。つぎに、エッチング液として硝酸第２セリウムアンモニウム溶液を使用した写真蝕刻技術で第１導電膜ｇ１を選択的にエッチングすることによって、ゲート端子ＧＴＭおよびドレイン端子ＤＴＭを形成するとともに、図１４に示すように、ゲート端子ＧＴＭを接続する陽極酸化バスラインＡＯＢ、陽極酸化バスラインＡＯＢに接続された陽極酸化パッドＡＯＰを形成する。つぎに、レジストを剥離液Ｓ５０２（商品名）で除去したのち、O_2アッシャーを１分間行なう。つぎに、膜厚が２６００Åのアルミニウム－パラジウム、アルミニウム－シリコン、アルミニウム－シリコン－チタン、アルミニウム－シリコン－銅等からなる第２導電膜ｇ２をスパッタリングにより設ける。つぎに、エッチング液としてリン酸と硝酸と酢酸との混酸を使用した写真蝕刻技術で第２導電膜ｇ２を選択的にエッチングすることにより、走査信号線ＧＬ、ダミー線ＤＧＬ、ゲート電極ＧＴおよび保持容量素子Ｃaddの電極ＰＬ１を形成する。つぎに、ドライエッチング装置にSF_6ガスを導入して、シリコン等の残渣を除去したのち、レジストを除去する。つぎに、陽極酸化用のホトレジストＲＳＴを設ける。つぎに、３％酒石酸をアンモニアによりｐＨ７．０±０．５に調整した溶液をエチレングリコール液で１：９に稀釈した液からなる陽極酸化液中に下部透明ガラス基板ＳＵＢ１の陽極酸化すべき部分を浸漬し、陽極酸化パッドＡＯＰに陽極酸化電圧を印加することにより、第２導電膜ｇ２を陽極酸化して、走査信号線ＧＬ上、ダミー線ＤＧＬ上およびゲート電極ＧＴ上に陽極酸化膜ＡＯＦを設ける。つぎに、プラズマＣＶＤ装置にアンモニアガス、シランガス、窒素ガスを導入して、膜厚が３５００Åの窒化シリコン膜を設け、プラズマＣＶＤ装置にシランガス、水素ガスを導入して、膜厚が２１００Åのｉ型非晶質シリコン膜を設けたのち、プラズマＣＶＤ装置に水素ガス、ホスフィンガスを導入して、膜厚が３００ÅのＮ(＋)型非晶質シリコン膜を設ける。つぎに、ドライエッチングガスとしてＳ

F_6、CCl_4を使用した写真蝕刻技術でN(＋)型非晶質シリコン膜、ｉ型非晶質シリコン膜を選択的にエッチングすることにより、ｉ型半導体層ＡＳを形成する。つぎに、レジストを除去したのち、ドライエッチングガスとしてSF_6を使用した写真蝕刻技術で、窒化シリコン膜を選択的にエッチングすることによって、絶縁膜ＧＩを形成する。つぎに、レジストを除去したのち、膜厚が６００Åのクロムからなる第１導電膜ｄ１をスパッタリングにより設ける。つぎに、写真蝕刻技術で第１導電膜ｄ１を選択的にエッチングすることにより、映像信号線ＤＬ、ダミー線ＤＤＬ、ソース電極ＳＤ１、ドレイン電極ＳＤ２の第１層を形成する。つぎに、レジストを除去する前に、ドライエッチング装置にCCl_4、SF_6を導入して、N(＋)型非晶質シリコン膜を選択的にエッチングすることにより、N(＋)型半導体層ｄ０を形成する。つぎに、レジストを除去したのち、O_2アッシャーを１分間行なう。つぎに、膜厚が３５００Åのアルミニウムーパラジウム、アルミニウムーシリコン、アルミニウムーシリコンーチタン、アルミニウムーシリコンー銅等からなる第２導電膜ｄ２をスパッタリングにより設ける。つぎに、写真蝕刻技術で第２導電膜ｄ２を選択的にエッチングすることにより、映像信号線ＤＬ、ダミー線ＤＤＬ、ソース電極ＳＤ１、ドレイン電極ＳＤ２の第２層を形成する。つぎに、レジストを除去したのち、O_2アッシャーを１分間行なう。つぎに、膜厚が１２００ÅのＩＴＯ膜からなる第３導電膜ｄ３をスパッタリングにより設ける。つぎに、エッチング液として塩酸と硝酸との混酸を使用した写真蝕刻技術で第３導電膜ｄ３を選択的にエッチングすることにより、映像信号線ＤＬ、ダミー線ＤＤＬ、ソース電極ＳＤ１、ドレイン電極ＳＤ２の第３層、ゲート端子ＧＴＭ、ドレイン端子ＤＴＭの最上層および透明画素電極ＩＴＯ１を形成する。つぎに、レジストを除去したのち、プラズマＣＶＤ装置にアンモニアガス、シランガス、窒素ガスを導入して、膜厚が１μｍの窒化シリコン膜を設ける。つぎに、ドライエッチングガスとしてSF_6を使用した写真蝕刻技術で窒化シリコン膜を選択的にエッチングすることによって、保護膜ＰＳＶ１を形成する。

【００７５】図１５はこの発明に係る他のアクティブ・マトリックス方式カラー液晶表示装置の画素部の四隅を示す概略図である。この液晶表示装置においては、最外側の走査信号線ＧＬの外側に設けられたダミー線ＤＧＬのダミー端子ＤＧＴＭの電位はアース電位とされており、最外側の映像信号線ＤＬの外側に設けられたダミー線ＤＤＬのダミー端子ＤＤＴＭはコモン電圧Ｖcomに接続されている。また、画素の外側にはダミー透明画素電極ＤＩＴＯ１、ダミー薄膜トランジスタＤＴＦＴ等を有するダミー画素が形成されており、ダミー画素のダミー薄膜トランジスタＤＴＦＴのゲート電極、ドレイン電極は走査信号線ＧＬ、映像信号線ＤＬ、ダミー線ＤＧＬ、ＤＤＬに接続されている。また、遮光膜ＢＭ（図１５においては遮光膜ＢＭ部に斜線を施している）によってダミー画素がマスクされている。

【００７６】このように、ダミー線ＤＧＬの電位はアース電位とされているから、ダミー薄膜トランジスタＤＴＦＴがオンになることがないので、映像信号線ＤＬに映像信号が印加されたとしても、ダミー透明画素電極ＤＩＴＯ１部の液晶ＬＣに電圧が印加されることがない。また、ダミー線ＤＤＬはコモン電圧Ｖcomに接続されているから、走査信号線ＧＬに走査信号が印加され、ダミー薄膜トランジスタＤＴＦＴがオンになったとしても、ダミー透明画素電極ＤＩＴＯ１部の液晶ＬＣに電圧が印加されることがない。また、遮光膜ＢＭによってダミー画素がマスクされているから、仮にダミー透明画素電極ＤＩＴＯ１に映像信号が印加されて、ダミー画素が点灯したとしても、その光は遮光膜ＢＭによって遮光される。

【００７７】以上、本発明者によってなされた発明を、前記実施例に基づき具体的に説明したが、この発明は、前記実施例に限定されるものではなく、その要旨を逸脱しない範囲において種々変更可能であることは勿論である。

【００７８】たとえば、上述実施例においては、ゲート電極形成→ゲート絶縁膜形成→半導体層形成→ソース・ドレイン電極形成の逆スタガ構造を示したが、上下関係または作る順番がそれと逆のスタガ構造でもこの発明は有効である。また、上述実施例においては、ダミー線ＤＧＬ、ＤＤＬを１本設けたが、ダミー線ＤＧＬ、ＤＤＬを２本以上設けてもよい。また、上述実施例においては、走査信号線ＧＬ上にアルミニウムの陽極酸化膜ＡＯＦを設けた場合について説明したが、走査信号線上にタンタル、チタン等の陽極酸化膜を設けた場合にもこの発明を適用することができる。

【００７９】

【発明の効果】以上説明したように、この発明に係る液晶表示装置においては、信号線を形成する際に、最外側の信号線と他の信号線とはホトレジストの形成条件、エッチング条件等が同一になるから、最外側の信号線が断線することがない。

【００８０】また、信号線を走査信号線とし、走査信号線上に陽極酸化膜を設けたときには、陽極酸化の際に最外側の走査信号線部における電界が不均一になることがなく、またホトレジスト形成の際に最外側の走査信号線に汚れが付きにくいから、最外側の走査信号線が断線することがない。

【００８１】このように、この発明の効果は顕著である。

【図面の簡単な説明】

【図１】図２に示す液晶表示装置の一部概略断面図である。

【図２】この発明が適用されるアクティブ・マトリック

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ス方式のカラー液晶表示装置の液晶表示部の一画素を示す要部平面図である。

【図３】図２の３－３切断線で切った部分とシール部周辺部の断面図である。

【図４】図２の４－４切断線における断面図である。

【図５】図２に示す液晶表示装置のゲート端子部を示す断面図である。

【図６】図２に示す液晶表示装置のドレイン端子部を示す断面図である。

【図７】図２に示す画素を複数配置した液晶表示部の要部平面図である。

【図８】図２に示す画素の所定の層のみを描いた平面図である。

【図９】図２に示す画素の所定の層のみを描いた平面図である。

【図１０】図２に示す画素の所定の層のみを描いた平面図である。

【図１１】図７に示す画素電極層、遮光膜およびカラーフィルタ層のみを描いた要部平面図である。

【図１２】アクティブ・マトリックス方式のカラー液晶表示装置の液晶表示部を示す等価回路図である。

【図１３】図２に示す画素の等価回路図である。

【図１４】図２に示す液晶表示装置の製造方法の説明図である。

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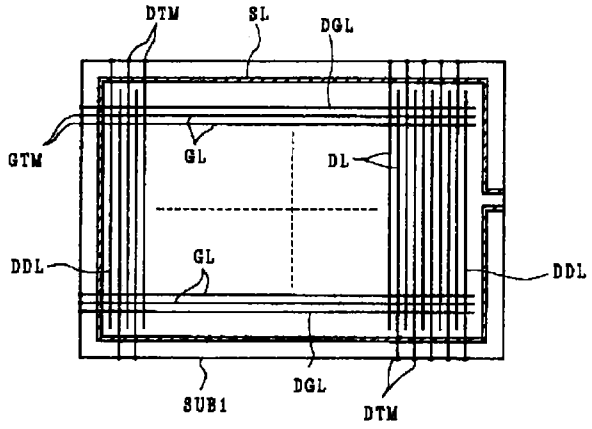
＊【図１５】この発明に係る他のアクティブ・マトリックス方式カラー液晶表示装置の画素部の四隅を示す概略図である。

【符号の説明】

ＳＵＢ…透明ガラス基板
ＧＬ…走査信号線
ＤＬ…映像信号線
ＧＩ…絶縁膜
ＧＴ…ゲート電極
ＡＳ…ｉ型半導体層
ＳＤ…ソース電極またはドレイン電極
ＰＳＶ…保護膜
ＢＭ…遮光膜
ＬＣ…液晶
ＴＦＴ…薄膜トランジスタ
ＩＴＯ…透明画素電極
ｇ、ｄ…導電膜
Ｃadd…保持容量素子
Ｃgs…寄生容量
Ｃpix…液晶容量
ＡＯＦ…陽極酸化膜
ＤＧＬ…ダミー線
ＤＤＬ…ダミー線

【図１】

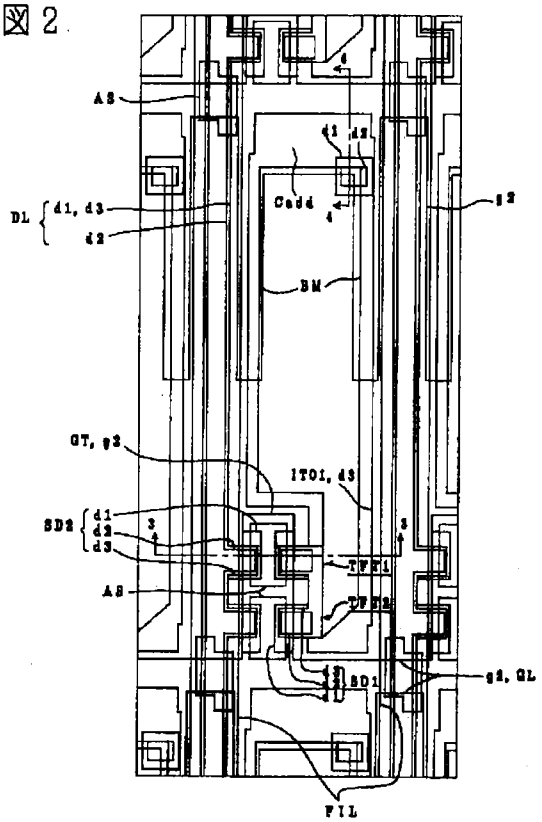
図１



ＧＬ：走査信号線
ＤＧＬ：ダミー線
ＤＤＬ：ダミー線

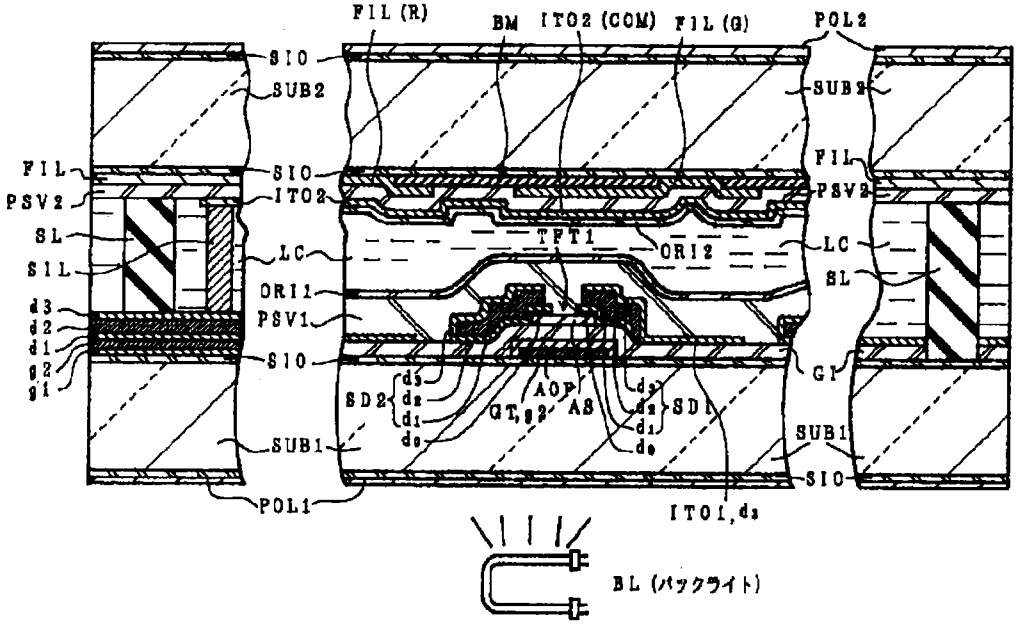
【図２】

図２



【図３】

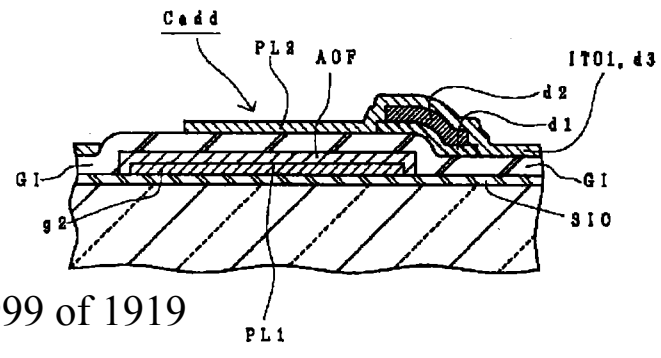
図３



POL1, POL2…偏光板
SUB２…上部ガラス基板
ＦＩＬ…カラーフィルタ
ＰＳＶ２…カラーフィルタの保護膜
ＩＴＯ２…共通透明画素電極
ＯＲＩ２…上部配向膜
Ｌ　Ｃ　…液晶
ＯＲＩ１…下部配向膜
Ｂ　Ｍ　…ブラックマトリックス
ＰＳＶ１…ＴＦＴの保護膜
ＩＴＯ１（層ｄ３）…透明画素電極
Ｓ　Ｄ　…ソース・ドレイン電極（層ｄ１～ｄ３）
Ａ　Ｓ　…ｉ型半導体層
Ｇ　Ｉ　…ゲート絶縁膜
Ｇ　Ｔ　…ゲート電極（層ｇ１，ｇ２）
ＳＵＢ１…下部ガラス基板
Ｂ　Ｌ　…バックライト
ＳＩＯ…酸化シリコン膜

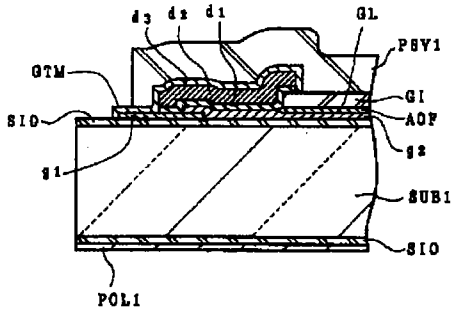
【図４】

図４



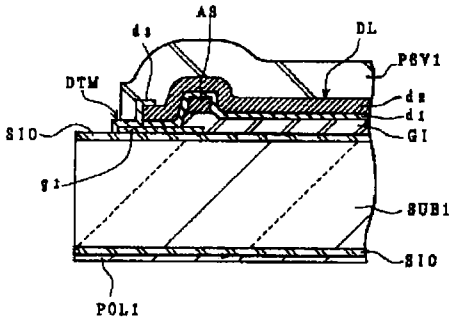
【図５】

図５



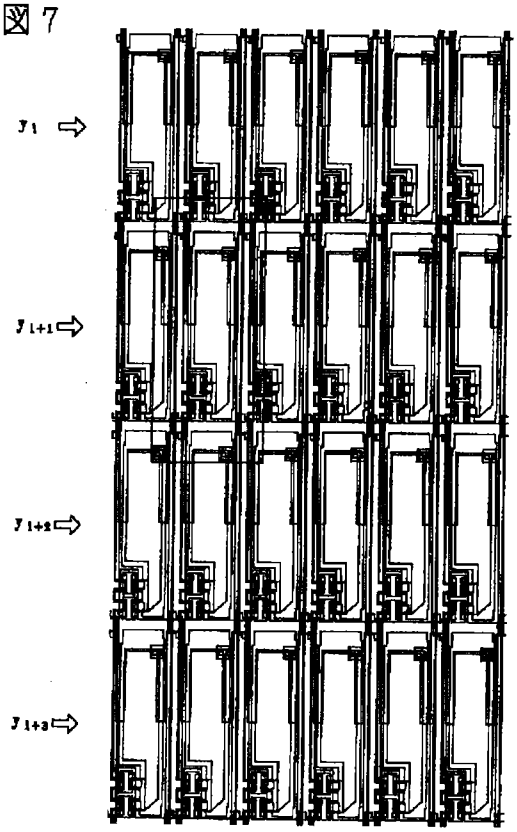
【図6】

図6



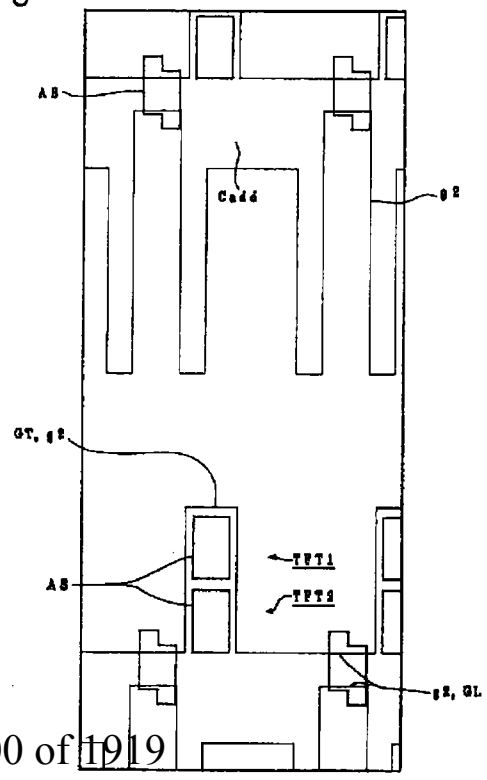
【図7】

図7



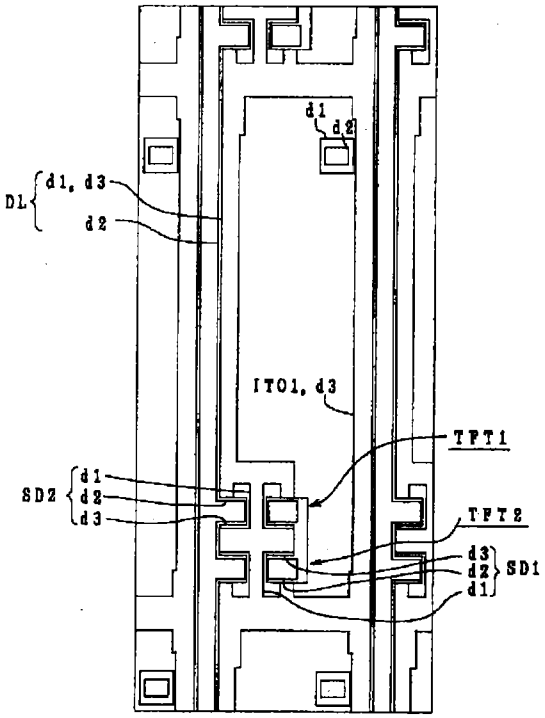
【図8】

図8



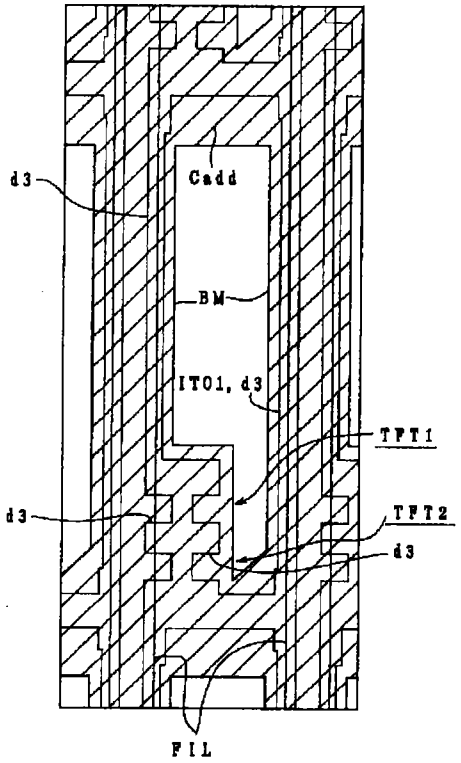
【図9】

図9



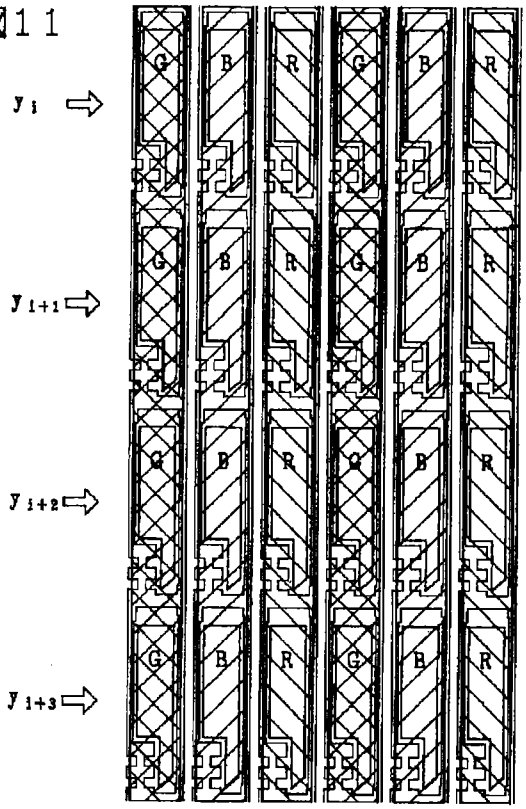
【図１０】

図１０



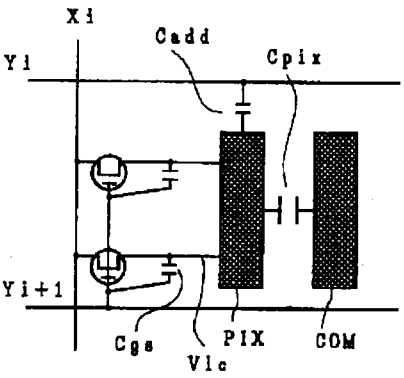
【図１１】

図１１



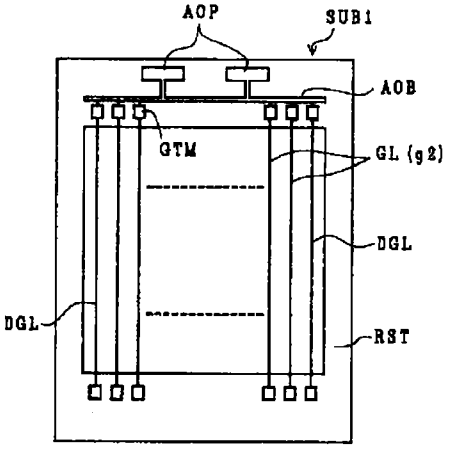
【図１３】

図１３



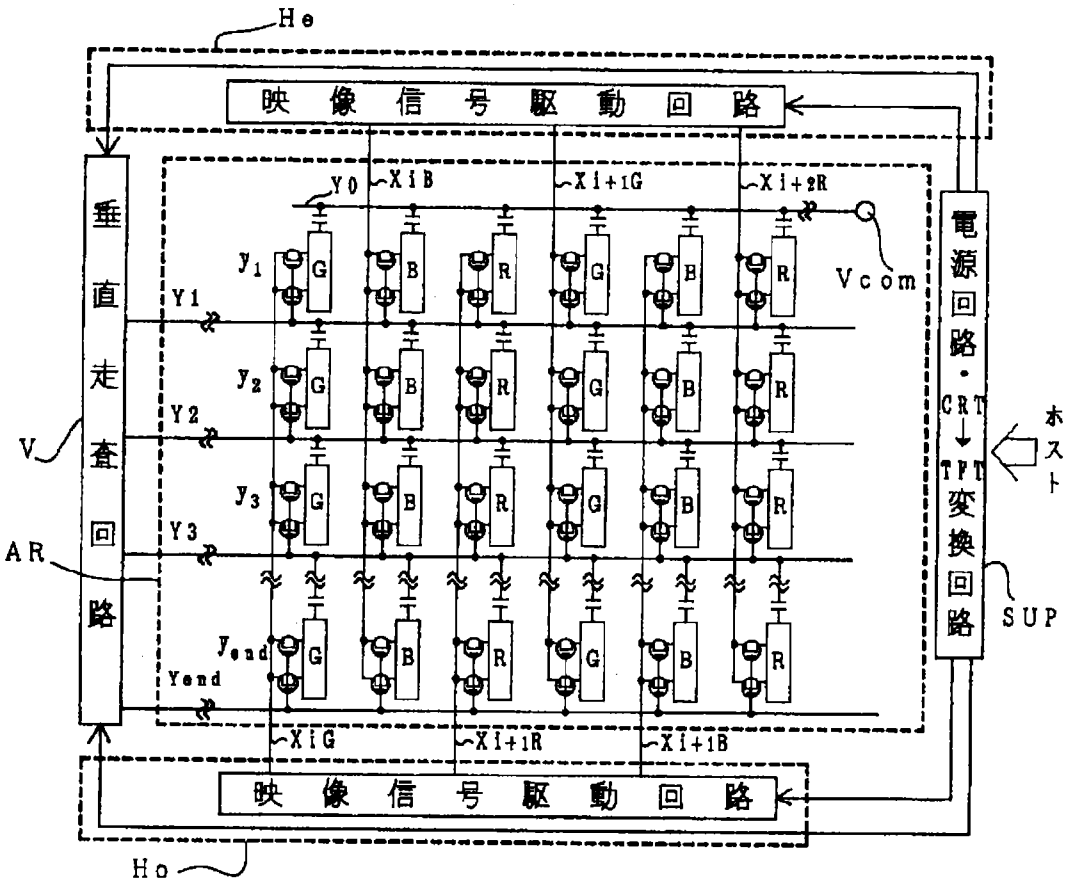
【図１４】

図１４



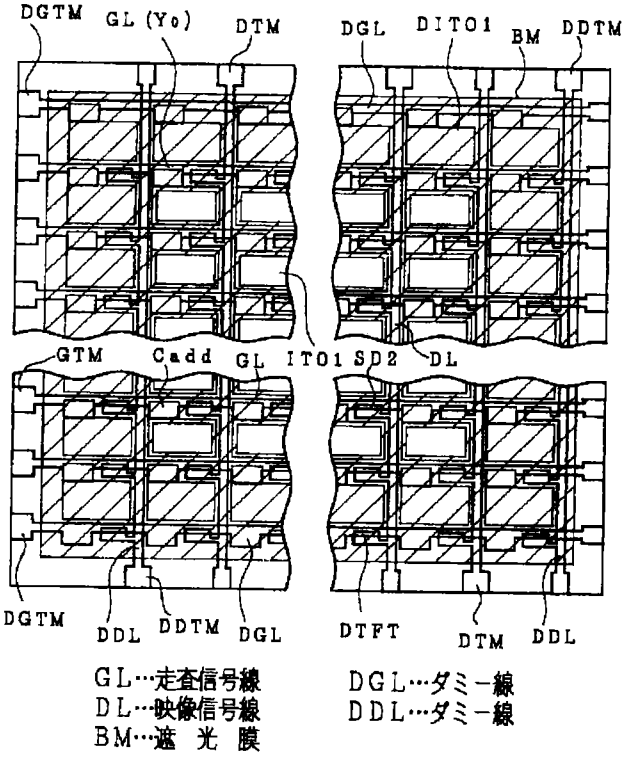
【図１２】

図１２


He
映像信号駆動回路
垂直走査回路
V
AR
Y0
XiB
Xi+1G
Xi+2R
Vcom
y1
y2
y3
yend
Y1
Y2
Y3
Yend
G
B
R
XiG
Xi+1R
Xi+1B
電源回路・CRT→TFT変換回路
ホスト
SUP
映像信号駆動回路
Ho

【図１５】

図１５



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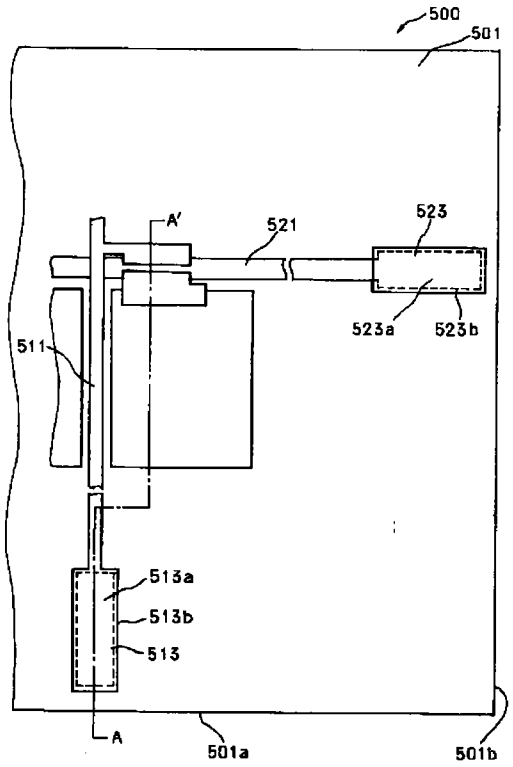
最終頁に続く

(54)【発明の名称】　表示装置用アレイ基板

(57)【要約】
【課題】　この発明は、信号線と走査線との層間ショート等による製造歩留まりの低下を抑えることができる表示装置用アレイ基板を提供することを目的としている。
【解決手段】　本発明は、絶縁基板(501)上に配列された複数本の走査線(521)と、走査線(521)の少なくとも一端に配置される走査線接続パッド(523)と、走査線(521)上に絶縁膜を介して略直交する複数本の信号線(511)と、信号線(511)の一端に配置される信号線接続パッド(513)とを備えた表示装置用アレイ基板であって、信号線接続パッド(513)は走査線と同一材料から成る信号線接続パッド部(513a)を含み、且つ信号線(511)の他端側には信号線(511)と離間し走査線(521)と同一材料から成るダミー信号線接続パッド部(533)を含む。



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【特許請求の範囲】

【請求項１】　絶縁基板上に配列された複数本の走査線と、前記走査線の少なくとも一端に配置される走査線接続パッドと、前記走査線上に絶縁膜を介して略直交する複数本の信号線と、前記信号線の一端に配置される信号線接続パッドとを備えた表示装置用アレイ基板において、

前記信号線接続パッドは前記走査線と同一材料から成る信号線接続パッド部を含み、

且つ前記信号線の他端側には前記信号線と離間し前記走査線と同一材料から成るダミー信号線接続パッド部を含むことを特徴とする表示装置用アレイ基板。

【請求項２】　請求項１記載の前記走査線、前記信号線接続パッド部及び前記ダミー信号線接続パッド部は同一工程にてパターニングされて成ることを特徴とする表示装置用アレイ基板。

【請求項３】　請求項２記載のパターニングがケミカル・ドライ・エッチングによることを特徴とする表示装置用アレイ基板。

【請求項４】　請求項１記載の前記ダミー信号線接続パッド部は除去されることを特徴とする表示装置用アレイ基板。

【請求項５】　絶縁基板上に配列された複数本の信号線と、前記信号線の少なくとも一端に配置される信号線接続パッドと、前記信号線上に絶縁膜を介して略直交する複数本の走査線と、前記走査線の一端に配置される走査線接続パッドとを備えた表示装置用アレイ基板において、

前記走査線接続パッドは前記信号線と同一材料から成る走査線接続パッド部を含み、

且つ前記走査線の他端側には前記走査線と離間し前記信号線と同一材料から成るダミー走査線接続パッド部を含むことを特徴とする表示装置用アレイ基板。

【請求項６】　請求項５記載の前記信号線、前記走査線接続パッド部及び前記ダミー走査線接続パッド部は同一工程にてパターニングされて成ることを特徴とする表示装置用アレイ基板。

【請求項７】　請求項６記載のパターニングがケミカル・ドライ・エッチングによることを特徴とする表示装置用アレイ基板。

【請求項８】　請求項５記載の前記ダミー走査線接続パッド部は除去されることを特徴とする表示装置用アレイ基板。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、平面表示装置等に用いられる表示装置用アレイ基板に関する。

【０００２】

【従来の技術】近年、小型、軽量、低消費電力を志向して、液晶表示装置に代表されるフラットパネルディスプレイの開発が進められている。例えば、液晶表示装置は、絶縁基板上に複数本の信号線及び走査線が絶縁膜を介してマトリクス状に配線され、各交点近傍にスイッチ素子を介して画素電極が配置されて成るマトリクスアレイ基板と、絶縁基板上に透明電極材料から成る対向電極が配置されて成る対向基板と、これら基板間に狭持される液晶材料から成る液晶層とを含む。信号線や走査線は、それぞれ表示領域外に引き出され、外部回路等との電気的接続を行うための接続パッドに導かれ接続される。

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【０００３】

【発明が解決しようとする課題】ところで、近年では、平面表示装置の低廉化を達成するために、一大判基板に多数のアレイ基板を作り込む多面取りが成される。このため、基板がより一層大型化されており、このため基板各所で均一なエッチングを行うことが困難となってきている。特に、ドライエッチングでは、十分なエッチングレートを確保しつつ、基板各所で均一な放電状態を維持することが非常に難しく、エッチング条件のマージンが小さくなっている。

【０００４】また、近年では、平面表示装置の高精細化を達成するため、走査線や信号線の微細化あるいはその本数が増大する傾向にある。このため、例えば、走査線をエッチングしパターニングするに際し、基板外周近傍と中央付近とでは、単位面積当たりに存在する金属薄膜等の被パターニング薄膜の面積が大幅に異なる。このため、単位面積当たりに存在する被パターニング薄膜の面積が少ない基板外周近傍では、エッチング終了寸前では、被パターニング薄膜に供給されるエッチングガスが他の領域に比べて多く、オーバーエッチングされ易く、このためテーパー角度が垂直に近くなる。これにより、走査線と信号線とが層間ショートし、製造歩留まりが低下するという問題が生じる。

【０００５】この発明は、上記した技術課題に対処して成されたものであって、走査線あるいは信号線のパターン形状を基板各所で均一にでき、また信号線と走査線との層間ショート等による製造歩留まりの低下を抑えることができる表示装置用アレイ基板を提供することを目的としている。

【０００６】

【課題を解決するための手段】請求項１記載の発明は、絶縁基板上に配列された複数本の走査線と、前記走査線の少なくとも一端に配置される走査線接続パッドと、前記走査線上に絶縁膜を介して略直交する複数本の信号線と、前記信号線の一端に配置される信号線接続パッドとを備えた表示装置用アレイ基板において、前記信号線接続パッドは前記走査線と同一材料から成る信号線接続パッド部を含み、且つ前記信号線の他端側には前記信号線と離間し前記走査線と同一材料から成るダミー信号線接続パッド部を含むことを特徴とする表示装置用アレイ基

板にある。

【０００７】請求項２記載の発明は、請求項１記載の前記走査線、前記信号線接続パッド部及び前記ダミー信号線接続パッド部は同一工程にてパターニングされて成ることを特徴とする表示装置用アレイ基板にある。

【０００８】請求項３記載の発明は、請求項２記載のパターニングがケミカル・ドライ・エッチングによることを特徴とする表示装置用アレイ基板にある。請求項４記載の発明は、請求項１記載の前記ダミー信号線接続パッド部は除去されることを特徴とする表示装置用アレイ基板にある。

【０００９】請求項５記載の発明は、絶縁基板上に配列された複数本の信号線と、前記信号線の少なくとも一端に配置される信号線接続パッドと、前記信号線上に絶縁膜を介して略直交する複数本の走査線と、前記走査線の一端に配置される走査線接続パッドとを備えた表示装置用アレイ基板において、前記走査線接続パッドは前記信号線と同一材料から成る走査線接続パッド部を含み、且つ前記走査線の他端側には前記走査線と離間し前記信号線と同一材料から成るダミー走査線接続パッド部を含むことを特徴とする表示装置用アレイ基板にある。

【００１０】請求項６記載の発明は、請求項５記載の前記信号線、前記走査線接続パッド部及び前記ダミー走査線接続パッド部は同一工程にてパターニングされて成ることを特徴とする表示装置用アレイ基板にある。

【００１１】請求項７記載の発明は、請求項６記載のパターニングがケミカル・ドライ・エッチングによることを特徴とする表示装置用アレイ基板にある。請求項８記載の発明は、請求項５記載の前記ダミー走査線接続パッド部は除去されることを特徴とする表示装置用アレイ基板にある。

【００１２】

【発明の実施の形態】以下、本発明の一実施例の液晶表示装置について、図面を参照して詳細に説明する。図１は、本発明の一実施例の液晶表示装置の概略斜視図であり、この液晶表示装置(1) は、アレイ基板(500) と対向基板(800) とが液晶層(700) （図３参照）を介して対向配置されて成る液晶パネル(3) を含む。

【００１３】アレイ基板(500) の一端辺(501a)側に信号線(511) （図２参照）は引き出され、８個のＸ－ＴＡＢ(901-1),…,(901-8)を介して回路基板(911) に電気的に接続されている。また、アレイ基板(500) の一端辺(501a)と直交する他の一端辺(501b)側に走査線(521) （図２参照）は引き出され、２個のＹ－ＴＡＢ(903-1),(903-2) を介して回路基板(921) に電気的に接続されている。

【００１４】図２乃至３を参照して、この実施例のアレイ基板(500) について更に詳細に説明する。このアレイ基板(500) は、０．７㎜厚のガラスから成る絶縁基板(501) 上にモリブデンータングステン（Ｍｏ－Ｗ）合金から成る互いに略平行な６００本の走査線(521) を含む。この走査線(521) は、絶縁基板(501) の一端辺(501b)側に、シール領域(601) （図５参照）を介して延在され、走査線接続パッド(523) を構成する走査線(521) と一体の第１走査線接続パッド部(523) に導かれる。また、この走査線(521) と同一材料、同一工程にて、後述する信号線接続パッド(513)の一部を成す第１信号線接続パッド部(513a)が配置されている。

【００１５】走査線(521) 上には、窒化膜から成るゲート絶縁膜(571) を介して、アルミニウム（Ａｌ）から成る走査線(521) と略直交する（８００×３）本の信号線(511) が配置される。この信号線(511) は、絶縁基板(501) の一端辺(501a)側に、シール材が配されるシール領域(601) （図５参照）を介して延在され、第１信号線接続パッド部(513a)上に信号線(511) と一体の第２信号線接続パッド部(513b)を構成し、第１信号線接続パッド部(513a)と第２信号線接続パッド部(513b)との積層構造で信号線接続パッド(513) は構成されている。また、この信号線(511) と同一材料、同一工程にて、走査線接続パッド(523) の一部を成す第１走査線接続パッド部(523a)上に第２走査線接続パッド部(523b)が配置され、信号線接続パッド(513) と同様に第１走査線接続パッド部(523a)と第２走査線接続パッド部(523b)との積層構造で走査線接続パッド(523) は構成されている。

【００１６】これら信号線(511) や走査線(521) としては、Ａｌ、Ａｌ合金、Ｍｏ－Ｔａ合金、Ｍｏ－Ｗ合金等の低抵抗金属材料が好適に用いられ、更にはＡｌとこのＡｌを被覆する金属層等の複数の金属層の積層構造であってもかまわない。

【００１７】シール領域(601) （図５参照）内における信号線(511) と走査線(521) との交差部近傍には、走査線(511) をゲート電極とし、信号線(521) にドレイン電極が接続された逆スタガ構造でチャネルストッパを備えたＴＦＴ(531) が配置されている。各ＴＦＴ(531) のソース電極にＩＴＯから成る画素電極(541) が接続され、これら画素電極(541) によって表示領域が形成される。このＴＦＴ(531) は、半導体層(581) としてアモルファスシリコン（ａ－Ｓｉ：Ｈ）薄膜が用いられて成るもので、半導体層としてはポリシリコン（ｐ－Ｓｉ）や化合物半導体等が用いられるものであってもかまわない。

【００１８】ところで、このようなアレイ基板(500) は、図５に示されるアレイ基板原板(100) から切り取ることにより作成することができる。このアレイ基板原板(100) は、図４に示す如く、ガラスから成る大判絶縁基板(101) 上に所望の膜厚のＭｏ－Ｗ合金がパターニングされて成る互いに略平行な６００本の走査線(521) 、この走査線(521) の一端に接続される走査線接続パッド(523) を構成する第１走査線接続パッド部(523a)、最外端の第６００番目の走査線(521) の図中下側に配置された信号線接続パッド(513) を構成する第１信号線接続パッ

ド部(513a)、最外端の第１番目の走査線(521) の図中上側に配置されたダミー信号線接続パッド(533) を含む。

【００１９】これら走査線(521) 、第１走査線接続パッド部(523a)、第１信号線接続パッド部(513a)及びダミー信号線接続パッド(533) は、例えばＭｏ－Ｗ合金上にフォトレジストが配置され、所望形状に露光した後、ＣＦ４とO2 との混合ガスを用いたケミカル・ドライ・エッチンク（ＣＤＥ）により図４に示す形状にパターニングされる。ウエット・エッチングによりパターニングすることもできるが、パターニング性、薬液管理等を考えると、ドライ・エッチンクの方が望ましい。また、ここでは、ＣＦ４とO2 との混合ガスを用いたが、金属材料に応じて各種変更することは言うまでもない。

【００２０】このように、最外端の第６００番目の走査線(521) の図中下側及び第１番目の走査線(521) の図中上側に、それぞれ第１信号線接続パッド部(513a)及びダミー信号線接続パッド(533) を配置するようにしたので、第６００番目の走査線(521) 近傍や第１番目の走査線(521) 近傍での被パターニング薄膜であるＭｏ－Ｗ合金パターン密度を略等しくすることができる。このようにして、単位面積当たりに存在するＭｏ－Ｗ合金の面積が均一であれば、エッチング終了寸前でも、Ｍｏ－Ｗ合金に供給されるエッチングガスは各所で略等しくなる。また、単位面積当たりに存在するフォトレジストも各所で略均一であるため、フォトレジストのエッチングについても各所で均一にO2 が消費されるため、Ｍｏ－Ｗ合金に影響するＣＦ４とO2 との混合比も各所で均一となる。

【００２１】これらの理由から、基板各所でのエッチング状態を略等しくすることができ、各走査線(521) のパターン形状を均一にでき、またテーパー角度を均一にでき、信号線(511) との交差部におけるクロス・ショート等の発生を防止することができる。

【００２２】また、アレイ基板原板(100) は、図５に示すように、大判絶縁基板(101) 上にシール材が配されるシール領域(601) を越えて延在され走査線(521) と略直交する信号線(511) 、この信号線(511) の一端側に配置される信号線接続パッド(513) を構成する第２信号線接続パッド部(513b)、更に走査線接続パッド(523) を構成する第１走査線接続パッド部(523a)（図２参照）上に配置される第２走査線接続パッド部(523b)を含む。

【００２３】シール領域(601) の内側領域は上述したアレイ基板(500) と同様であるので、ここでの説明は省略する。このようなアレイ基板原板(100) から、図中ＢＢ’線に沿って切断することにより、上述したアレイ基板(500) を得ることができる。

【００２４】以上説明したように、この実施例によれば、アレイ基板原板(100) は、最外端の第６００番目の走査線(521) の図中下側及び第１番目の走査線(521) の図中上側に、それぞれ第１信号線接続パッド部(513a)及びダミー信号線接続パッド(533) を含むように構成し、被パターニング薄膜の単位面積当たりの密度を均一化したので、第６００番目の走査線(521) や第１番目の走査線(521) のエッチング状態を他の走査線(521) のエッチング状態と略等しくすることができる。このため、基板が大判であっても、エッチング条件のマージンが大きくとれ、また基板各所で均一なエッチングが可能となる。これにより各走査線(521) のテーパー角度を均一にでき、信号線(511) との交差部におけるクロス・ショート等の発生を防止することができる。

【００２５】また、ダミー信号線接続パッド(533) は信号線(511) と平面的に離間すると共に電気的に接続されない、即ちシール領域(601) とダミー信号線接続パッド(533) との間には信号線(511) は配置されないため、不要な狭配線ピッチ部がなく、このため配線間ショートが増大することもない。

【００２６】更に、この実施例によれば、信号線(511) パターニング用のマスクのみを変更し、第１信号線接続パッド部(513a)と信号線(511) とを電気的に接続せず、ダミー信号線接続パッド(533) と信号線(511) とを電気的に接続する構成とし、図５中ＣＣ’線に沿って切断することで、電極引出位置が異なる他の仕様のアレイ基板を容易に形成することができる。

【００２７】この実施例では、大判の絶縁基板から一アレイ基板を切り取る場合を説明したが、多数枚のアレイ基板を搾取する場合も同様である。また、この実施例では、ダミー信号線接続パッド(533) は第１走査線接続パッド部(523a)及び第１信号線接続パッド部(513a)と同一工程でパターニングされて成るＭｏ－Ｗ合金のみで構成したが、信号線接続パッド(513) と同様に積層構造としてもかまわない。このような構成により、信号線(511) のパターン形状を各所で均一化できる。

【００２８】更に、この実施例では、走査線上に絶縁膜を介して信号線が配置される場合を例にとり説明したが、信号線上に絶縁膜を介して走査線が配置される場合であってもかまわない。例えば、スタガ構造のＴＦＴを用いたアレイ基板であれば、このような構成が有利であるが、この場合は、例えば信号線パターニング時に信号線形成材料により信号線の両端に信号線接続パッド及びダミー信号線接続パッドを配しておくことで、信号線のパターン形状を均一化でき、またテーパー角度を均一にできるので、その上に絶縁膜を介して配置される走査線との交差部におけるクロス・ショート等の発生を防止することができる。

【００２９】

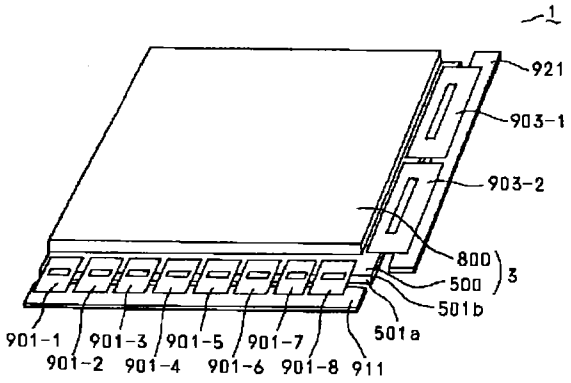
【発明の効果】本発明の表示装置用アレイ基板によれば、走査線あるいは信号線のパターニング性が各所で均一にでき、これにより信号線と走査線との層間ショート等による製造歩留まりの低下を抑える。

【図面の簡単な説明】

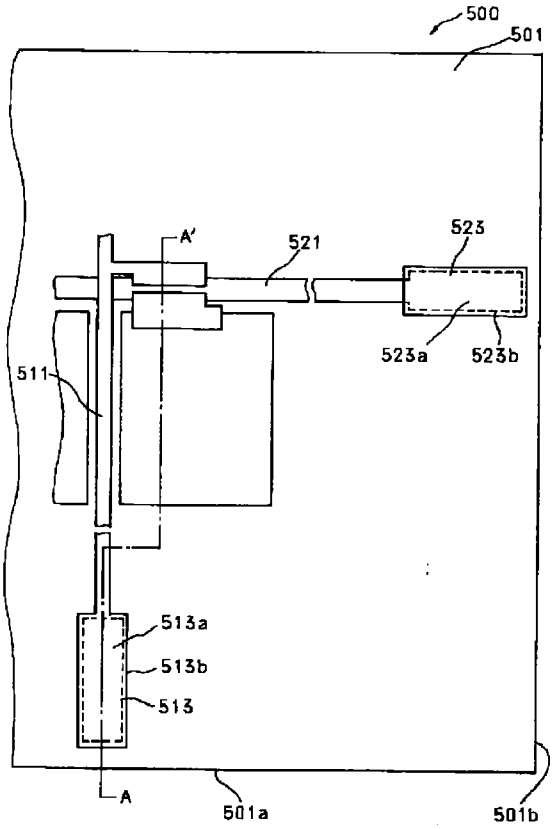
【図１】図１は、本発明の一実施例の液晶表示装置の概略斜視図である。
【図２】図２は、図１におけるアレイ基板の一部概略斜視図である。
【図３】図３は、図２におけるＡＡ’線に沿って切断した液晶表示装置の概略断面図である。
【図４】図４は、図１のアレイ基板を得るためのアレイ基板原板の一部概略正面図である。
【図５】図５は、図１のアレイ基板を得るためのアレイ基板原板の一部概略正面図である。
【符号の説明】

＊(1)…液晶表示装置
(100)…アレイ基板原板
(500)…アレイ基板
(511)…信号線
(513)…信号線接続パッド
(521)…走査線
(523)…走査線接続パッド
(533)…ダミー信号線接続パッド
(700)…液晶層
(800)…対向基板

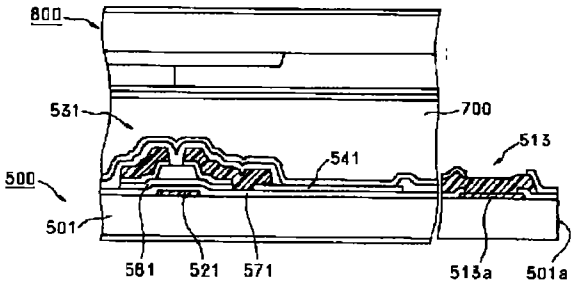
【図１】



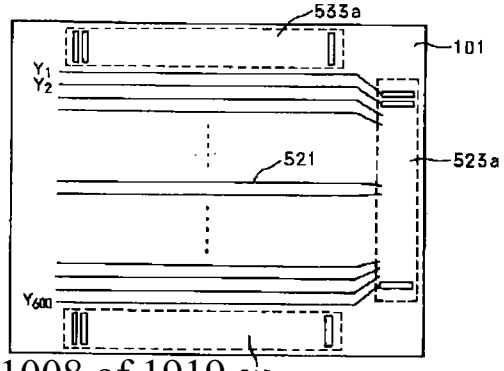
【図２】



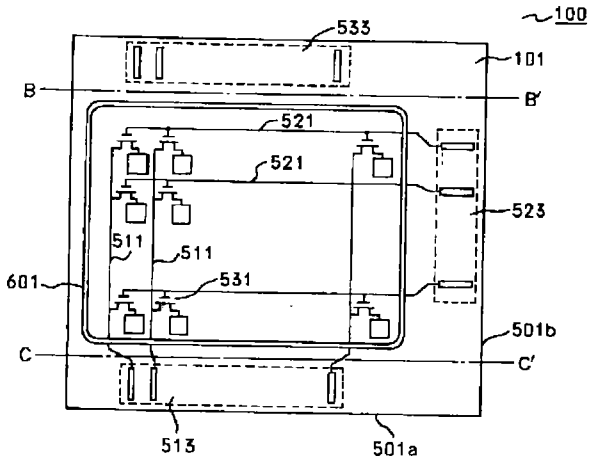
【図３】



【図４】



【図５】



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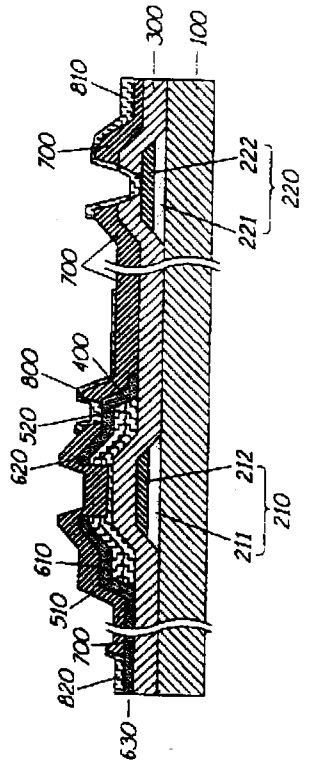
(54)【発明の名称】　配線用組成物、この組成物を用いた金属配線およびその製造方法、この配線を用いた表示装置およびその製造方法

(57)【要約】
【課題】　低抵抗を有しかつ厚さに応じて応力の調節が可能な薄膜トランジスタの配線を提供する。
【解決手段】　モリブデンまたはモリブデンータングステン組成物を用いて配線をする際に接触孔を形成するとき、保護膜およびゲート絶縁層の側面部エッチングを遅延させる高分子膜を形成するかCF_4+O_2を用いてモリブデン合金膜がエッチングされないようにし、SF_6+HCl(+He)またはSF_6+Cl_2(+He)を用いて接触孔のフレームが緩やかな傾斜を有するように形成する。また、モリブデンまたはモリブデンータングステン合金膜をマスクにして非晶質シリコン層をエッチングするとき、ハロゲン化水素気体とCF_4、CHF_3、$CHClF_2$、CH_3FおよびC_2F_6のうち、少なくとも一つの気体を用いる。



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【特許請求の範囲】

【請求項１】　同一のエッチング条件においてテーパ形状に加工でき、テーパ角度が２０～７０°の範囲である二重導電膜からなる表示装置用配線。

【請求項２】　前記導電膜は１５μΩcm以下の低い比抵抗を有する下部導電膜とパッド用物質からなる上部導電膜からなる請求項１に記載の表示装置用配線。

【請求項３】　前記下部導電膜はアルミニウムまたはアルミニウム合金からなり、前記上部導電膜は原子百分率０．０１％～２０％未満のタングステンと、残りのモリブデンおよび必須不純物からなるモリブデンータングステン合金からなる請求項２に記載の配線。

【請求項４】　前記エッチング条件が湿式である場合、エッチング液はアルミニウムまたはアルミニウム合金をエッチングするに用いられるエッチング液である$CH_3COOH/HNO_3/H_3PO_4/H_2O$であり、前記$HNO_3$の濃度は８～１４％である請求項３に記載の表示装置用配線。

【請求項５】　基板の上部に下部導電膜を積層する段階と、

前記下部導電膜の上部に同一のエッチング条件に対し前記下部導電膜のエッチング比よりエッチング比が７０～１００オングストローム／sec程度大きい上部導電膜を積層する段階と、

前記エッチング条件を用いて前記上部導電膜および下部導電膜を同時にエッチングする段階とを含む表示装置用配線の製造方法。

【請求項６】　前記下部導電膜は１５μΩcm以下の低い比抵抗を有し、前記上部導電膜はパッド用物質である請求項５に記載の表示装置用配線の製造方法。

【請求項７】　前記下部導電膜はアルミニウムまたはアルミニウム合金からなり、前記上部導電膜は原子百分率０．０１％～２０％未満のタングステンと、残りのモリブデンおよび必須不純物からなるモリブデン合金である請求項６に記載の表示装置用配線の製造方法。

【請求項８】　前記エッチング条件が湿式である場合、エッチング液は前記アルミニウムまたはアルミニウム合金をエッチングするに用いられるエッチング液である$CH_3COOH/HNO_3/H_3PO_4/H_2O$であり、前記$HNO_3$の濃度は８～１４％である請求項７に記載の表示装置用配線の製造方法。

【請求項９】　モリブデンまたはモリブデンータングステン合金の単一膜からなる表示装置用配線。

【請求項１０】　前記モリブデンまたはモリブデンータングステン合金の単一膜の下部にクロム膜をさらに含む請求項９に記載の表示装置用配線。

【請求項１１】　前記モリブデンータングステン合金は原子百分率０．０１％～２０％未満のタングステンと、残りのモリブデンおよび必須不純物からなる請求項９に記載の表示装置用配線。

【請求項１２】　基板上に原子百分率０．０１％～２０％未満のタングステンと、残りのモリブデンおよび必須不純物からなるモリブデン合金膜を積層する段階と、

エッチング液を用いて前記モリブデン合金膜をパターニングしてゲート線、ゲートパッドおよびゲート電極を含むゲートパターンを形成する段階と、

前記基板上にゲート絶縁膜を積層する段階と、

前記ゲート絶縁膜上部にドーピングしない非晶質シリコン層およびドーピングされた非晶質シリコン層を形成する段階と、

データ線、ソース／ドレイン電極およびデータ線と連結されているデータパッドを含むデータパターンを形成する段階と、

前記データパターンをマスクにして前記ドーピングされた非晶質シリコン層をエッチングする段階と、

保護膜を積層する段階と、

前記保護膜を前記ゲート絶縁膜と共にパターニングして前記ドレイン電極、データパッドおよびゲートパッドの一部が露出されるようにする段階と、

透明な導電膜を積層する段階と、

前記透明な導電膜をエッチングして前記ゲートパッドと接続されるゲート導電膜および前記ドレイン電極と接続される画素電極を形成する段階とを含む表示装置用薄膜トランジスタ基板の製造方法。

【請求項１３】　前記モリブデン合金膜の下部にアルミニウムまたはアルミニウム合金からなる導電膜を積層する段階をさらに含み、前記モリブデン合金膜をパターニングするとき前記エッチング液を用いて前記導電膜と共にパターニングする請求項１２に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項１４】　アルミニウム合金膜はアルミニウと原子百分率５％以下の希土類金属または転移金属からなる請求項１３に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項１５】　前記エッチング液は$CH_3COOH/HNO_3/H_3PO_4/H_2O$であり、前記$HNO_3$は８～１４％の範囲で含有される請求項１４に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項１６】　前記データパターンはクロム、モリブデンまたはタングステンとモリブデンおよび必須不純物からなるモリブデン合金膜の単一膜またはこれらを組合わせた多重膜で形成される請求項１５に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項１７】　前記データパターンを前記クロムからなる下部膜と原子百分率０．０１％～２５％未満のタングステンと、残りのモリブデンおよび必須不純物からなるモリブデンータングステン合金からなる上部膜からなる二重導電膜で形成する場合、前記二重導電膜をエッチングするエッチング液はHNO_3：$(NH_4)_2Ce(NO_3)_6$：H_2Oである請求項１６に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項１８】　前記HNO_3濃度は４～１０％であり、前記$(NH_4)_2Ce(NO_3)_6$濃度は１０～１５％である請求項１７に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項１９】　前記データパターンがモリブデンまたはモリブデンータングステン合金を含み、前記データパターンをマスクにして前記ドーピングされた非晶質シリコン層をハロゲン化水素とCF_4、CHF_3、$CHClF_2$、CH_3およびC_2F_6のうち、少なくとも一つを用いて乾式エッチングする請求項１６に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項２０】　前記データパターンはモリブデンまたはモリブデンータングステン合金で形成し、前記ドレイン電極、データパッドおよび前記ゲートパッドの一部が露出されるようにする段階は、

前記保護膜上部にホトレジスト膜を塗布し、前記ゲートパッド、データパッドおよびドレイン電極に対応する位置に開口部を有する前記ホトレジストパターンを形成する段階と、

前記ホトレジストと前記ゲート絶縁層および前記保護膜のエッチング選択比が１：１ないし１：１．５であるエッチング条件において前記データパッドおよびドレイン電極を露出させる段階と、

前記データパターンと前記ゲート絶縁層および前記保護膜とのエッチング選択比が１：１５以上であるエッチング条件において前記ゲートパッドを露出させる段階とを含む請求項１６に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項２１】　前記データパッドおよびドレイン電極を露出させる段階はSF_6+HClまたはSF_6+Cl_2ガスを用い、前記ゲートパッドを露出させる段階はCF_4/O_2ガスを用いる請求項２０に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項２２】　前記データパターンはモリブデンまたはモリブデンータングステン合金で形成し、前記ドレイン電極、データパッドおよび前記ゲートパッドの一部が露出されるようにする段階は、

前記保護膜上部にホトレジスト膜を塗布し、前記ゲートパッド、データパッドおよびドレイン電極に対応する位置に開口部を有する前記ホトレジストパターンを形成する段階と、

前記データパッドおよびドレイン電極を露出させる段階と、

四フッ化炭素(CF_4)と水素(H_2)または塩化水素(HCl)を混合したガスをプラズマ状態で用いて前記基板上部に高分子膜を形成する段階と、

前記データパターンと前記ゲート絶縁層および前記保護膜とのエッチング選択比が１：１５以上であるエッチング条件において前記ゲートパッドを露出させる段階とを含む請求項１６に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項２３】　前記ゲートパッドを露出させる段階はCF_4/O_2ガスを用い、前記データパッドおよびドレイン電極を露出させる段階はSF_6+HCl、SF_6+Cl_2または前記CF_4/O_2ガスを用いる請求項２２に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項２４】　前記データパターンはモリブデンまたはモリブデンータングステン合金で形成し、前記ドレイン電極、データパッドおよび前記ゲートパッドの一部が露出されるようにする段階は、

前記保護膜上部にホトレジスト膜を塗布し、前記ゲートパッド、データパッドおよびドレイン電極に対応する位置に開口部を有する前記ホトレジストパターンを形成する段階と、

前記ホトレジストパターンをマスクにして前記データパッド、ドレイン電極およびゲートパッドをCF_4+O_2ガスを用いて露出させるエッチング段階とを含む請求項１６に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項２５】　前記エッチング段階においてCF_4に対するO_2ガスの比率を１０：４以下とする請求項２４に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項２６】　基板上に原子百分率０．０１％～２０％未満のタングステンと、残りのモリブデンおよび必須不純物からなるモリブデン合金膜を積層する段階と、

エッチング液を用いて前記モリブデン合金膜を第１マスクにパターニングしてゲート線、ゲート線に連結されたゲートパッドおよびゲート線に連結されたゲート電極からなるゲートパターンを形成する段階と、

前記基板上にゲート絶縁膜、ドーピングされない非晶質シリコン層、ドーピングされた非晶質シリコン層および金属膜を順に積層する段階と、

第２マスクを用いて前記金属膜およびドーピングされた非晶質シリコン層およびドーピングされない非晶質シリコン層の一部を連続的にエッチングする段階と、

前記基板上部に透明導電膜を蒸着し第３マスクを用いて前記金属膜の上部に開口部を有する画素電極を形成する段階と、

前記画素電極をマスクにして前記金属膜およびドーピングされた非晶質シリコン層をエッチングしてコンタクト層、データ線およびソース／ドレイン電極を含むデータパターンを形成する段階と、

前記基板上部に保護膜を積層する段階と、

第４マスクを用いて前記ゲートパッド上部に前記ゲート絶縁膜と前記保護膜をホトエッチングする段階とを含む表示装置用薄膜トランジスタ基板の製造方法。

【請求項２７】　前記モリブデン合金膜の下部にアルミニウムまたはアルミニウム合金からなる導電膜を積層する段階をさらに含み、前記モリブデン合金膜をパターニングするとき、前記エッチング液を用いて前記導電膜と共にパターニングする請求項２６に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項２８】　アルミニウム合金膜はアルミニウと原子百分率５％以下の希土類金属または転移金属からなる請求項２７に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項２９】　前記エッチング液は$CH_3COOH/HNO_3/H_3PO_4/H_2O$であり、前記$HNO_3$は８～１４％の範囲で含有される請求項２８に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項３０】　前記データパターンはクロム、モリブデンまたはタングステンとモリブデンおよび必須不純物からなるモリブデン合金膜の単一膜またはこれらを組合わせた多重膜で形成する請求項３０に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項３１】　前記データパターンを前記クロムからなる下部膜と原子百分率０．０１％～２５％未満のタングステンと、残りのモリブデンおよび必須不純物からなるモリブデン－タングステン合金の上部膜からなる二重導電膜で形成する場合、前記二重導電膜をエッチングするエッチング液はHNO_3：$(NH_4)_2Ce(NO_3)_6$：H_2Oである請求項３０に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項３２】　前記HNO_3の濃度は４～１０％であり、前記$(NH_4)_2Ce(NO_3)_6$の濃度は１０～１５％である請求項３１に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項３３】　前記データパターンはモリブデンまたはモリブデン－タングステン合金を含み、前記データパターンをマスクに露出された前記ドーピングされた非晶質シリコン層をハロゲン化水素とCF_4、CHF_3、$CHClF_2$、CH_3およびC_2F_6のうち、少なくとも一つを用いて乾式エッチングする請求項３０に記載の表示装置用薄膜トランジスタ基板の製造方法。

【請求項３４】　透明な絶縁基板と、
前記基板上に形成されており、原子百分率０．０１％～２０％未満のタングステンと、残りのモリブデンおよび必須不純物からなるモリブデン合金膜のゲート線、ゲート電極およびゲートパッドを含むゲートパターン、
前記ゲートパターンを覆うゲート絶縁膜と、
前記ゲート絶縁膜上部に形成されている非晶質シリコン層と、
前記非晶質シリコン層上部に形成されており、データ線、ソース／ドレイン電極およびデータパッドを含むデータパターンと、
前記ドレイン電極と連結されている画素電極とを含む表示装置用薄膜トランジスタ基板。

【請求項３５】　前記モリブデン合金膜の下部にアルミニウムまたはアルミニウム合金からなる導電膜をさらに含む請求項３４に記載の表示装置用薄膜トランジスタ基板。

【請求項３６】　前記アルミニウム合金はアルミニウムと原子百分率５％以下の希土類金属または転移金属からなる請求項３５に記載の表示装置用薄膜トランジスタ基板。

【請求項３７】　前記データパターンはクロム、モリブデンまたはタングステンと、残りのモリブデンおよび必須不純物からなるモリブデン合金膜の単一膜またはこれらの組合せである多重膜からなる請求項３６に記載の表示装置用薄膜トランジスタ基板。

【請求項３８】　前記データパターンを前記モリブデンまたはモリブデン合金膜の単一膜で形成する場合に前記基板の大きさは３７０＊４７０mm^2以上である請求項３７に記載の表示装置用薄膜トランジスタ基板。

【請求項３９】　前記データパターンの厚さは０．３～２．０μm範囲である請求項３８に記載の表示装置用薄膜トランジスタ基板。

【請求項４０】　前記データ線の幅は３．０～１０．０μm範囲である請求項３８に記載の表示装置用薄膜トランジスタ基板。

【請求項４１】　ハロゲン化水素とCF_4、CHF_3、$CHClF_2$、CH_3およびC_2F_6のうち、少なくとも一つを含む非晶質シリコン層の乾式エッチング用気体。

【請求項４２】　基板上部にドーピングされた非晶質シリコン層を形成する段階と、
前記ドーピングされた非晶質シリコン層上にモリブデンまたはモリブデン－タングステン合金膜で第１および第２電極を形成する段階と、
前記第１および第２電極をマスクにして前記ドーピングされた非晶質シリコンをハロゲン化水素気体とCF_4、CHF_3、$CHClF_2$、CH_3FおよびC_2F_6のうち、少なくとも一つの気体を用いて乾式エッチングする段階とを含む表示装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術の分野】本発明は配線用組成物、この組成物を用いた金属配線およびその製造方法、この配線を用いた表示装置およびその製造方法に関する。

【０００２】

【従来の技術】一般に、半導体装置または表示装置の配線は信号が伝達される手段に用いられるので、信号の遅延および短絡を抑制するのが求められる。短絡を防止する方法としては、配線を多層に形成する方法があるが、多層の配線を形成するため、互いに異なるエッチング液が必要であるばかりでなく、数回のエッチング工程が必要になる。

【０００３】信号遅延を防止する方法としては、低抵抗を有するアルミニウム(Al)またはアルミニウム合金(Al alloy)などのような物質を用いるのが一般的である。しかしながら、アルミニウムまたはアルミニウム合金を用いる場合には陽極酸化工程を付加してアルミニウムの弱い物理的な特性を補完する必要がある。また、液晶表示

装置でのように、パッド部においてＩＴＯ(indium tin oxide)を用いてアルミニウムを補完する場合、アルミニウムまたはアルミニウム合金とＩＴＯの接触特性が不良で他の金属を介在しなければならないという問題点を有している。

【０００４】一方、液晶表示装置用配線は液晶表示装置の高精細化が進行されるに従って配線の数が増加するので、配線の幅は狭くなる。しかしながら、配線は一定の程度以下の抵抗値を確保しなければならないので、配線の厚さは増加することになる。このとき、配線の厚さが増加するほど配線の応力は液晶表示装置用基板に印加され、基板の大きさが大きくなるに従ってこの応力は増加することになる。

【０００５】

【発明の目的】本発明は前記従来の問題点を解決するためのものであって、その目的は、低抵抗を有しかつ厚さに応じて応力の調節が可能な配線を提供することにある。

【０００６】また、本発明の目的は、容易に形成できる二重配線を提供し、これを用いて表示装置の製造工程が簡単でかつ製品の特性を向上させることにある。

【０００７】また、本発明の目的は、導電膜または金属配線を露出させる接触孔のフレームの傾斜角を緩やかにし接触孔の下部の導電膜のエッチングを防止することにある。

【０００８】

【課題を解決するための手段】本発明に従う配線は同一のエッチング条件においてテーパ形状に加工でき、テーパ角度が２０～７０°の範囲である二重導電膜であるか、同一のエッチング条件において下部導電膜のエッチング比より上部導電膜のエッチング比が７０～１００オングストローム／sec程度大きい二重導電膜からなる。ここで、エッチング方法が湿式エッチングである場合、同一のエッチング条件とは、同一のエッチング液を用いることである。

【０００９】かかる導電膜は１５μΩcm以下の低い比抵抗を有する下部導電膜とパッド用物質からなる上部導電膜からなる。ここで、パッド用物質とは、パッドとして用いられる特性を有する物質である。その特性については実施の形態において説明する。

【００１０】ここで、導電膜のうち、一つはアルミニウムまたはアルミニウム合金が用いられ、導電膜がアルミニウム合金である場合には含有された転移金属または希土類金属が５％以下であることが好ましい。

【００１１】他の導電膜としては、原子百分率０．０１％～２０％未満のタングステンWと残りのモリブデン(Ｍｏ)および必須不純物からなるモリブデン組成物または合金が用いられる。モリブデン合金においてタングステンの組成比は原子百分率９％～１１％であることが好

【００１２】湿式エッチングの際、エッチング液はアルミニウムまたはアルミニウム合金をエッチングするに用いられるエッチング液であり、例えば、$CH_3COOH/HNO_3/H_3PO_4/H_2O$を挙げられ、このとき、$HNO_3$の濃度は８～１４％であることが好ましい。

【００１３】かかる二重導電膜の配線は表示装置において走査信号を印加するゲート線またはデータ信号を印加するデータ線に用いられる。かかる本発明に従う配線の製造方法は、１基板の上部に下部導電膜を積層し下部導電膜の上部に同一のエッチング条件において下部導電膜のエッチング比よりエッチング比が７０～１００オングストローム/sec程度大きい上部導電膜を積層する。次に、上部導電膜および下部導電膜を同時にエッチングして配線を完成する。

【００１４】かかる二重導電膜からなる配線の製造方法は、表示装置の製造方法において走査信号を印加するゲート線またはデータ信号を印加するデータ線の製造方法でも適用できる。このとき、配線は外部から信号が伝達されるパッドを有し、下部導電膜がパッド用物質で形成されている場合、パッドにおいては上部導電膜を除去することが好ましい。ここで、モリブデン組成物は比抵抗が１２～１４μΩcm程度に小さく、パッドに使用可能であるので、単一膜配線に用いられる。この配線は２０～７０°、より好ましくは、４０～５０°程度のプロファイルを有する。従って、かかる配線は表示装置のゲート線またはデータ線に用いられる。

【００１５】前述したように、かかるモリブデンータングステン配線を用いて液晶表示装置を製作できる。本発明に従う液晶表示装置用薄膜トランジスタ基板の製造方法においては、基板上に原子百分率０．０１％～２０％未満のタングステンと残りのモリブデンおよび必須不純物からなるモリブデン合金を積層しエッチング液を用いてモリブデン合金膜をパターニングしてゲート線、ゲートパッドおよびゲート電極を含むゲート配線を形成する。ここで、モリブデン合金膜の下部にアルミニウムまたはアルミニウム合金からなる導電膜を積層することができ、モリブデン合金膜をパターニングするとき、導電膜と共にパターニングする。アルミニウム合金である場合、含有された転移金属または希土類金属が５％以下であることが好ましい。湿式エッチングの際、エッチング液はアルミニウムまたはアルミニウム合金をエッチングするに用いられるエッチング液であって、例えば、$CH_3COOH/HNO_3/H_3PO_4/H_2O$を挙げられ、このとき、$HNO_3$の濃度は８～１４％であることが好ましい。

【００１６】また、かかる本発明に従う薄膜トランジスタ基板の製造方法においてデータ線、データパッドおよびソース／ドレイン電極を含むデータ配線はモリブデンータングステン合金、クロムまたはモリブデンの単一膜またはこれらを組合わせた２重膜で形成する。このとき、アルミニウムまたはアルミニウム合金を上部膜で形

成する場合、パッドにおいてはアルミニウム膜またはアルミニウム合金膜を除去することが好ましい。

【００１７】このデータ線、データパッドおよびソース／ドレイン電極を下部膜はクロム膜、上部膜はモリブデンータングステン合金膜で形成する場合、同一のエッチング液で上部膜と下部膜とを同一にエッチングしてテーパ形状に加工する。ここで、エッチング液はクロムをエッチングするに用いられるエッチング液であって、例えば、$HNO_3/(HN_4)_2Ce(NO_3)_6/H_2O$を挙げられ、このとき、$HNO_3$の濃度は４～１０％、$(HN_4)_2Ce(NO_3)_6$の濃度は１０～１５％であることが好ましい。このとき、モリブデンまたはモリブデン合金の配線はその厚さを厚く形成しても基板が歪まないように応力を調節できるので、高精細大画面基板に適合である。

【００１８】また、本発明に従う半導体装置の製造方法においては金属膜または金属配線上の絶縁膜にホトレジストをパターニングし、これをマスクにして絶縁膜をエッチングして金属膜上に二つ以上の接触孔を形成する。このとき、絶縁膜の厚さが異なるため、厚さが薄い側の接触孔の下方の金属膜がエッチングされるのを防止し、緩やかな傾斜角でエッチングするため、２段階または３段階過程に分けて接触孔を形成する。

【００１９】２段階で形成する方法においては、まずホトレジストと絶縁膜に対しエッチング選択比１：１ないし１：１．５であるエッチング条件において部分エッチングを行なうが、このとき、絶縁膜の厚さが薄い側は絶縁膜および金属膜の一部がエッチングされる。次いで、絶縁膜と金属膜とのエッチング選択比が１：１５以上であるエッチング条件において残りの絶縁膜をエッチングする。

【００２０】３段階で形成する方法においては、まず絶縁膜の厚さが薄い側の金属膜が露出されるまでエッチングした後、エッチングの際露出された表面に高分子膜を形成する。次に、絶縁層と金属膜とのエッチング選択比が１５：１以上であるエッチング条件において残りの絶縁膜をエッチングする。ここで、高分子膜は最後の段階において絶縁膜が側面にエッチングされるのを防止する。

【００２１】かかる方法は第１金属膜、第１絶縁膜、第２金属膜、第２絶縁膜が連続に形成されている構造で適用できる。すなわち、第２絶縁膜下部の第２金属膜を露出させる第１接触孔と第２および第１絶縁膜下部の第１金属膜を露出させる第２接触孔を同時に形成するとき適用できる。

【００２２】また、かかる方法は半導体装置の配線を外部と連結するためのパッドを露出させる接触孔を形成するとき適用でき、特に、薄膜トランジスタ基板においてゲートパッドとデータパッドとをそれぞれ露出させる接触孔を同時に形成するとき適用できる。

【００２３】特に、金属膜はモリブデン膜またはモリブデンータングステン合金膜であり、絶縁膜は窒化シリコン膜であり、プラズマ乾式エッチングを用いて絶縁膜をエッチングする場合、２段階または３段階のエッチング方法のうち、最後の段階で用いる気体としてモリブデン膜またはモリブデンータングステン合金膜のエッチングを最小化できるCF_4+O_2が好ましい。また、２段階のエッチング方法において最初の段階で用いる気体としては、初期プロファイルを良好にできる$SF_6+HCl(+He)$または$SF_6+Cl_2(+He)$が適切である。CF_4に対するO_2の比率を4/10以下とする場合、１回のエッチング段階でモリブデン膜またはモリブデンータングステン合金膜のゲートパッドおよびデータパッドを同時に露出させることができる。

【００２４】また、このデータ配線は非晶質シリコン薄膜トランジスタ基板に適用でき、このとき、非晶質シリコン層と共にドーピングされた非晶質シリコン層が用いられる。このドーピングされた非晶質シリコンはデータ配線をマスクにして乾式エッチングされる。しかしながら、モリブデンまたはモリブデン合金は非晶質シリコン層をエッチングするための乾式エッチング用気体によりエッチングされやすいため、この過程においてデータ配線に対するエッチング比が１００オングストローム/min以下の乾式エッチング用気体を選択しなければならないし、ハロゲン化水素気体とCF_4、CHF_3、$CHClF_2$、CH_3FおよびC_2F_2のうち、少なくとも一つの気体がこれに適合である。

【００２５】

【発明の実施の形態】以下、本発明の実施の形態を本発明の属する技術分野における当業者が容易に実施することができる程度に詳細に説明する。半導体装置、特に表示装置の配線としては、１５μΩcm以下の低い比抵抗を有するアルミニウム、アルミニウム合金、モリブデン、銅などのような物質が適合である。一方、配線は外部から信号を受けるか、外部に信号を伝達するためのパッドを有していなければならない。パッドの露出の際、よく酸化されるといけないし、製造過程においても容易に短絡が発生しなければならない。アルミニウムとアルミニウム合金は比抵抗が非常に低いが、よく酸化され製造過程においても容易に短絡が発生するため、パッド用物質としては適合でない。一方、クロム、タンタル、チタン、モリブデンおよびその合金などのような物質はパッド用としては適合であるが、アルミニウムに比べ比抵抗が大きい。従って、配線をつくるときには二つの特性すべてを満たす金属を用いるか、低抵抗導電膜を用い、パッド用導電膜を用いて抵抗が低くかつパッドに用いられることにする。

【００２６】また、配線を二重にする場合同一のエッチング条件、特に湿式エッチングである場合、一つのエッチング液を用いて同時にエッチングするが緩やかな傾斜角を有するテーパ形態に加工する。このため、同一のエ

ッチング液に対して２０～７０°未満の範囲においてテーパ角度を有するか、上部導電膜のエッチング比が下部導電膜のエッチング比に比べ７０～１００オングストローム／sec程度大きいことが好ましい。また、単一膜で配線を形成する場合にも２０～７０°未満の範囲でテーパ角度を有することが好ましい。

【００２７】かかる過程において、本発明の実施の形態に従う配線用合金として原子百分率０．０１％～２０％未満のタングステンと残りのモリブデンおよび必須不純物からなるモリブデン合金を開発した。ここで、タングステンの組成比は、好ましくは原子百分率５％～１５％、より好ましくは９％～１１％である。

【００２８】図１ないし図３は、本発明の実施の形態に従うモリブデンータングステン合金(MoW)の特性を示すグラフである。図１は、本発明の実施の形態に従うモリブデンータングステン合金の蒸着特性を示すものであり、横軸はタングステン含有量を原子百分率で示し、縦軸は単位電力当り蒸着される厚さを示すものである。図１からわかるように、タングステン含有量が原子百分率２０atomic％以下である場合、単位電力当り蒸着されるモリブデンータングステン合金膜の厚さは１．２０～１．４０オングストローム/Wの範囲である。図２は本発明の実施の形態に従うモリブデンータングステン合金の比抵抗特性を示すものであり、横軸はタングステン含有量を原子百分率で示し、縦軸はそれに従う比抵抗を示すものである。図２からわかるように、原子百分率２０％以下のタングステンを含有するモリブデンータングステン合金の比抵抗Ｒは１２．０～１４．０μΩcmである。このように、原子百分率２０％以下のタングステンを含有するモリブデンータングステン合金は１５μΩcm以下の低い比抵抗を有し、パッド用物質としての性質を有しているので、単一膜配線に用いられる。また、アルミニウムやその合金などのように、二重配線に用いられる。特に、表示装置の信号線、この中でも液晶表示装置のゲート線またはデータ線に用いられる。図３は本発明の実施の形態に従うモリブデンータングステン合金のエッチング比特性を示すものであり、横軸はタングステン含有量を原子百分率で示し、縦軸はアルミニウムエッチング液に対し単位時間当りエッチングされる程度を示す。すなわち、モリブデンータングステン合金薄膜がアルミニウム合金のエッチング液(HNO_3：H_3PO_4：CH_3COOH：H_2O)に対し単位時間当りエッチングされる程度をタングステン(W)の含有量に従い示すものである。図３からわかるように、タングステンの含有量が０％である場合にはエッチング比が２５０オングストローム/sec程度に非常に大きく現われるが、タングステンの含有量が５％である場合にはエッチング比が１００オングストローム/sec程度に現われる。そして、タングステンの含有量が１５～２０％の間では５０オングストローム/sec以下に低下することがわかる。

【００２９】一方、比抵抗が非常に低いアルミニウムまたはその合金はHNO_3（８～１４％）：H_3PO_4：CH_3COOH：H_2Oからなるアルミニウムエッチング液に対し４０～８０オングストローム／sec程度のエッチング比を有するので、この程度のエッチング比より７０～１００オングストローム／sec程度が大きいエッチング比を有するモリブデンータングステン合金膜をアルミニウムまたはアルミニウム合金膜の上部に形成すると緩やかなテーパ角を有する二重膜配線を得られる。

【００３０】図４は本発明の実施の形態に従うモリブデンータングステン合金膜のアルミニウムエッチング液に対するエッチングプロファイルを示すものである。基板１上部に原子百分率１０％のタングステンが含有されるタングステンーモリブデン合金膜２を３０００オングストローム程度の厚さで蒸着した後、アルミニウム合金エッチング液を用いてエッチングすると２０～２５°の角を有する緩やかなプロファイルが形成される。

【００３１】一方、図３からわかるように、タングステンの組成比を調節してモリブデンータングステン合金膜のエッチング比を１００オングストローム/sec未満に低めることができるので、３０～９０°範囲のテーパ角を有する単一膜を形成することができる。従って、モリブデンータングステン合金からなる単一膜でも表示装置用、特に液晶表示装置のゲート線またはデータ線に用いられる。

【００３２】図５ないし図８はアルミニウム合金とモリブデンータングステン合金の二重膜をアルミニウム合金のエッチング液を用いてエッチングした場合、二重膜プロファイルを示すものである。基板１上部にアルミニウムまたはアルミニウム合金膜３を２０００オングストローム程度の厚さで蒸着し、その上にモリブデンータングステン合金膜２を１０００オングストローム程度の厚さで蒸着した後、アルミニウムエッチング液を用いてアルミニウム合金膜３およびモリブデンータングステン合金膜２を連続的にエッチングした。ここで、アルミニウムエッチング液としてはHNO_3：H_3PO_4：CH_3COOH：H_2Oを用い、好ましくは窒酸が８～１４％程度含有されている。ここで、アルミニウム合金はアルミニウムを基本物質とし、ここにＴｉ，Ｃｒ，Ｎｉ，Ｃｕ，Ｚｒ，Ｎｂ，Ｍｏ，Ｐｄ，Ｈｆ，Ｔａ，Wなどの転移元素(transi-tion metal)またはＮｄ，Ｇｄ，Ｄｙ，Ｅｒなどの希土類金属(rare earth metal)が結合された合金であって、含有された転移元素または希土類金属は原子百分率５％以下である。

【００３３】図５はモリブデンータングステン合金膜においてタングステンの含有率が５％である場合であって、３０～４０°のプロファイルを示しており、タングステンの含有率が１０％である図６の場合には４０～５０°のプロファイルを示している。タングステンの含有率が１５％になると、図７でのように、プロファイルが

８０～９０°になり、タングステンの含有率が２０％になると、図８でのように、９０°のプロファイルを示す。

【００３４】また、本発明の実施の形態においてアルミニウム合金とモリブデン－タングステン合金の二重膜をアルミニウムエッチング液を用いてエッチングする場合には、エッチング後に斑が現われない。

【００３５】このように、アルミニウム合金と原子百分率２０％以下のタングステンが含有されたモリブデン－タングステン合金からなる二重膜をアルミニウム合金エッチング液を用いてエッチングする場合、３０～９０°範囲においてテーパ角度が形成され、タングステン含有量が増加するに従ってテーパ角度が大きくなる。また、図６からわかるように、タングステン含有量が９％～１１％である場合に最も好ましいテーパ角度（４０～５０°）が形成される。

【００３６】以下、かかる配線を用いた液晶表示装置用薄膜トランジスタ基板について詳細に説明する。まず、図９～図１１を参照して本発明の第１の実施の形態に従う薄膜トランジスタ基板の構造について説明する。ここで、図１１は、図９におけるＸ－Ｘ'線の断面図である。基板１００上にゲート線２００およびその分枝であるゲート電極２１０、ゲート線２００の端部に形成されているゲートパッド２２０からなるゲートパターンが形成されている。ゲート電極２１０およびゲートパッド２２０はそれぞれ下層のアルミニウム膜またはアルミニウム合金膜２１１、２２１と上層の原子百分率０．０１％～２０％未満のタングステンと、残りのモリブデンからなるモリブデン－タングステン合金膜２１２、２２２からなり、ゲート線２００もアルミニウム膜またはアルミニウム合金膜とモリブデン－タングステン合金膜の二重膜からなる。ここで、ゲートパッド２２０は外部からの走査信号をゲート線２００に伝達する。

【００３７】ゲートパターン２００、２１０、２２０上にはゲート絶縁層３００が形成されており、このゲート絶縁層３００はゲートパッド２２０の上層であるモリブデン－タングステン合金膜２２２を露出させる接触孔７２０を有している。ゲート電極２１０上部のゲート絶縁層３００上には水素化非晶質シリコン(a-Si：H)層４００およびn⁺高濃度不純物でドーピングされた水素化非晶質シリコン層５１０、５２０がゲート電極２１０を中心に両側に形成されている。

【００３８】ゲート絶縁層３００上にはさらにデータ線６００が形成されており、その一端にはデータパッド６３０が形成されて外部からの画像信号を伝達する。データ線６００の分枝であるソース電極６１０が一方がドーピングされた非晶質シリコン層５１０上に形成されており、ソース電極６１０の向かい側に位置するドーピングされた非晶質シリコン層５２０上にはドレイン電極６２０が形成されている。ここで、データ線６００、ソースおよびドレイン電極６１０、６２０、データパッド６３０を含むデータパターンはモリブデン膜またはモリブデン－タングステン合金膜からなる。一方、図１０においてはゲートパッド２２０付近のゲート絶縁層３００上にはゲート補助パッド部６４０がさらに形成されている。

【００３９】データパターン６００、６１０、６２０、６３０およびこのデータパターンで覆われない非晶質シリコン層５００上には保護膜７００が形成されており、この保護膜７００にはゲートパッド２２０の上層モリブデン－タングステン合金膜２２２、ドレイン電極６２０およびデータパッド６３０を露出させる接触孔７２０、７１０、７３０がそれぞれ形成されている。一方、図１０においてはゲート補助パッド部６４０上部に保護膜７００の接触孔７４０が形成されている。

【００４０】最後に、保護膜７００上には接触孔７１０を通じてドレイン電極６２０と連結されており、ＩＴＯからなる画素電極８００が形成されており、接触孔７２０を通じて露出されたゲートパッド２２０と接続されて外部からの走査信号をゲート線２００に伝達するゲートパッド用ＩＴＯ電極８１０、接触孔７３０を通じてデータパッド６３０と接続されて外部からのデータ信号をデータ線６００に伝達するデータパッド用ＩＴＯ電極８２０が形成されている。一方、図１０において、ゲートパッド用ＩＴＯ電極８１０はゲート補助パッド部６４０まで延長されて接触孔７４０を通じて連結されている。

【００４１】図９および図１０からみるように、外部からの信号が実質的に直接印加されてパッドになる部分はゲートパッド用ＩＴＯ電極８１０とデータパッド用ＩＴＯ電極８２０である。以下、図９～図１１に示す構造の薄膜トランジスタ基板を製造する方法について図１２～図１５までを参照して説明する。この実施の形態においては５枚のマスクを用いた製造方法である。図１２に示すように、透明な絶縁基板１００上にアルミニウム膜またはアルミニウム合金膜とモリブデン－タングステン合金膜０．１～０．５μm、０．０２～０．１５μmの厚さで順に積層し第１マスクを用いてホトエッチングしてゲート線２００、ゲート電極２１０およびゲートパッド２２０を含み二重膜からなるゲートパターンを形成する。すなわち、図１２に示すように、ゲート電極２１０は下方のアルミニウムまたはアルミニウム合金膜２１１と、上方のモリブデン－タングステン合金膜２１２からなり、ゲートパッド２２０は下方のアルミニウムまたはアルミニウム合金膜２２１と、上方のモリブデン－タングステン合金膜２２２からなり、図１２に図示していないがゲート線２１０も二重膜からなる。ここで、アルミニウム合金膜はアルミニウムと５％以下の希土類金属または転移金属からなる。モリブデン－タングステン合金膜は原子百分率０．０１％以上２０％未満のタングステン(W)と、残りのモリブデン(Ｍｏ)からなり、タングステン含有率は原子百分率９～１１％であることが好まし

い。また、アルミニウムエッチング液、例えば、CH_3COOH／HNO_3／H_3PO_4／H_2Oなどを用い、HNO_3の含量は好ましくは８～１４％の範囲である。

【００４２】また、ゲートパターンはアルミニウム、アルミニウム合金およびタングステンーモリブデン合金のうち、一つの物質を蒸着して単一膜で形成することができる。

【００４３】図１３に示すように、窒化シリコンからなるゲート絶縁層３００、水素化非晶質シリコン層４００およびＮ形高濃度不純物でドーピングされた水素化非晶質シリコン層５００をそれぞれ０．２～１．０μm、０．１～０．３μm、０．０１５～０．１５μmの厚さで順に積層した後、ドーピングされた非晶質シリコン層５００および非晶質シリコン層４００を第２マスクを用いてホトエッチングする。

【００４４】図１４に示すように、モリブデンまたはタングステンを含むモリブデンータングステン合金膜を０．３～２．０μmの厚さで積層した後、第３マスクを用いてエッチングしてデータ線６００を、ソース電極６１０、ドレイン電極６２０およびデータパッド６３０を含むデータパターンを形成する。データパターンはクロム、モリブデンまたはモリブデン合金のうち、一つの単一膜またはこれらを組合わせた二重膜で形成することができる。また、抵抗を低めるため、アルミニウム膜またはアルミニウム合金膜をさらに形成することができる。

【００４５】しかしながら、表示装置用基板の大きさが大きくなり高精細化されるに従って配線数が増加するので、配線幅は狭くならなければならないが、一定の程度以下の抵抗値を確保しなければならないので、配線の厚さは増加させることが好ましい。従って、配線になる金属膜は厚さを増加しても金属膜が有する応力により基板が歪まないようにする物性を有するのが好ましい。かかる特性を有する金属膜としてはモリブデン膜またはモリブデンータングステン合金膜が適合である。詳しくは後述する実験例１において説明する。

【００４６】また、データパターンを下部膜はクロム膜、上部膜はモリブデンータングステン合金膜で形成する場合、同一のエッチング条件において上部膜と下部膜とを順にエッチングしてテーパ状に加工する。詳しくは後述する実験例２ないし４において説明する。ここで、エッチング液はクロムをエッチングするに用いられるエッチング液であって、例えば、HNO_3／$(NH_4)_2Ce(NO_3)_6$／H_2Oを挙げられ、このとき、HNO_3の濃度は４～１０％、$(NH_4)_2Ce(NO_3)_6$の濃度は１０～１５％であることが好ましい。

【００４７】次いで、データパターン６００、６１０、６２０、６３０をマスクにして露出されているドーピングされた非晶質シリコン層５００をプラズマ乾式エッチングしてゲート電極２１０を中心に両側に分離させる一方、両側にエッチングされた非晶質シリコン層５１０、５２０の間の非晶質シリコン層４００を露出させる。

【００４８】しかしながら、ドーピングされた非晶質シリコン層５００をエッチングするための乾式エッチング用気体はモリブデンータングステン合金膜を容易にエッチングさせるので、モリブデンータングステン合金膜のエッチング比が１００オングストローム/min以下になるように気体を選択しなければならない。ハロゲン化水素気体とCF_4、CHF_3、$CHClF_2$、CH_3FおよびC_2F_6のうち、少なくとも一つの気体がこれに適合し、非晶質シリコン層４００の表面を安定化するために水素(H_2)プラズマ工程を選択的にさらに行なうことができる。この特性については実験例５ないし７において詳細に説明する。

【００４９】図１５に示すように、保護膜７００を０．１～１．０μmの厚さで積層した後、第４マスクを用いて絶縁膜３００と共にホトエッチングし、ゲートパッド２２０上層のモリブデンータングステン合金膜２２２、ドレイン電極６２０およびデータパッド６３０を露出させる接触孔７２０、７１０、７３０を形成する。データパターンを形成するとき、ゲート補助パッド部６４０をさらに形成し、保護膜７００の接触孔７４０をさらに形成し図１０のような構造で形成することができる。

【００５０】ここで、接触孔を形成する過程について詳細に説明する。第４マスクを用いる写真工程においては接触孔７２０、７１０、７３０、７４０に対応する位置に開口部を有するホトレジストを保護膜７００の上部に形成し、これをマスクにしてプラズマ乾式エッチング方法で保護膜７００およびゲート絶縁層３００の窒化シリコン膜をエッチングする。

【００５１】接触孔７２０、７１０、７３０、７４０のフレームの傾斜を緩やかにするためには保護膜７００およびゲート絶縁層３００だけではなく、これを覆っているホトレジスト９００もエッチングしなければならない。このため、プラズマ乾式エッチング方法においては酸素量を増加させるか高周波電源においてSF_6＋HCl(＋He)またはSF_6＋Cl_2(＋He)を用いられる。しかしながら、保護膜７００およびゲート絶縁層３００の窒化シリコンとホトレジスト９００に対し２５００～３０００オングストローム／min程度のエッチング比を有するSF_6＋HCl(＋He)またはSF_6＋Cl_2(＋He)を用いる場合、このガスは窒化シリコン膜下部のゲートパッド２２０およびデータパターン６２０、６３０、６４０のモリブデン膜またはモリブデンータングステン合金膜に対し２０００オングストローム／min程度のエッチング比を有するので、選択的なエッチングが容易でなくて露出される窒化シリコン膜だけではなく、その下部のモリブデン膜またはモリブデンータングステン合金膜もエッチングし易い。

【００５２】特に、エッチングされる膜の厚さの差異により接触孔７１０、７３０、７４０の下部のモリブデンータングステン合金膜が過度にエッチングされる。すなわち、ゲートパッド２２０の上部にはゲート絶縁層３０

０と保護膜９００があるがデータパターン６２０、６３０、６４０の上部には保護膜９００のみがあるため、まずデータパターン６２０、６３０、６４０のモリブデンータングステン合金膜が露出される。

【００５３】これを解決するためには、モリブデン膜またはモリブデンータングステン合金膜がエッチングされない条件を適用しなければならないし、このためにはモリブデン膜またはモリブデンータングステン合金膜に対し４００オングストローム／min以下のエッチング比を有する乾式エッチング用ガスであるCF_4+O_2を用いられる。CF_4+O_2に対するホトレジスト９００のエッチング比は１０００オングストローム／min以下であり、窒化シリコン膜のエッチング比は６０００～１００００オングストローム／minであるので、経時変化に従ってホトレジスト９００の下部において窒化シリコン膜の側面部がエッチングされる量が増加してアンダーカットが発生し、このため、窒化シリコンのエッチングプロファイルを悪くなる。しかしながら、CF_4+O_2だけでエッチングしてもエッチング時間を縮小することにより、エッチングプロファイルを改善できる。このとき、CF_4とO_2との比率は、１０：４以下とすることが好ましい。

【００５４】一方、これをより改善するための方法として２段階または３段階のエッチングを行なうことができる。図１６（ａ）・（ｂ）及び図１７（ａ）・（ｂ）は、２段階のエッチング工程を行なった場合であり、図１８（ａ）から図１８（ｃ）まで、図１９（ａ）から図１９（ｃ）まで、図２０（ａ）から図２０（ｃ）、図２１（ａ）～図２１（ｃ）までは、３段階のエッチング工程を行なった場合である。図１６（ａ）・（ｂ）、図１８（ａ）から図１８（ｃ）までおよび図２０（ａ）から図２０（ｃ）までは、ゲートパッド２２０を覆う保護膜７００およびゲート絶縁層３００をエッチングして接触孔７１０、７３０、７４０を形成する工程を示す断面図であり、図１７（ａ）・（ｂ）、図１９（ａ）から図１９（ｃ）まで及び図２１（ａ）から図２１（ｃ）までは、データパターン６２０、６３０、６４０を覆う保護膜７００をエッチングして接触孔７２０を形成する工程を示す断面図である。まず、開口部を有するホトレジスト９００を保護膜７００の上部に形成する。次いで、ホトレジスト９００と保護膜７００およびゲート絶縁層３００の窒化シリコン膜のエッチング選択比がほぼ１：１．５であるエッチング用ガスを用いてデータパターン６２０、６３０、６４０のモリブデンータングステン合金膜が露出されるまでエッチングする（図１６（ａ）・図１７（ａ）参照）。かかるエッチング用ガスは前述した$SF_6+HCl(+He)$または$SF_6+Cl_2(+He)$が好ましい。このとき、データパターン６２０、６３０、６４０のモリブデンータングステン合金膜もSF_6+HClまたはSF_6+Cl_2に対し２０００オングストローム/min程度のエッチング比を有するので一部がエッチングされ得る。このようにすると、接触孔７１０、７２０、７３０、７４０のフレームの傾斜角は３０～８０°程度になる。

【００５５】次に、図１６（ｂ）および図１７（ｂ）からみるように、残っているゲートパッド２２０上部のゲート絶縁膜３００を窒化シリコンとモリブデンータングステン合金のエッチング選択比がほぼ１５：１以上である気体条件を適用して乾式エッチングする。このとき、窒化シリコン膜７００、３００の側面部も一部エッチングされる。ホトレジストは多少エッチングしてもかかる気体の例としては前述したCF_4+O_2を挙げられる。

【００５６】次に、３段階で接触孔を形成する方法について説明する。３段階で形成する方法においては、途中に高分子膜を全面に形成する過程をたどるが、ここでは次のような二つの方法が可能である。まず、図１８（ａ）から図１８（ｃ）および図１９（ａ）から図１９（ｃ）を参照して３段階で接触孔を形成する方法について説明する。第１段階においては図１８（ａ）および図１９（ａ）からみてもわかるように、$SF_6+HCl(+He)$または$SF_6+Cl_2(+He)$のガスを用いてホトレジスト９００と窒化シリコン膜７００、３００を順にエッチングする。このとき、エッチング工程はデータパターン６２０、６３０、６４０のモリブデンータングステン合金膜が完全に露出されるまで行なう。このとき、モリブデンータングステン合金膜の一部がエッチングされ得るが、これはゲートパッド２２０の上部に残留するゲート絶縁層３００の厚さを最小化して第３段階においてゲート絶縁層３００のエッチングのために適用する時間を最小化するためである。次に、第２段階においては図１８（ｂ）および図１９（ｂ）からみるように、四フッ化炭素(CF_4)と水素(H_2)または塩化水素(HCl)を混合するガスをプラズマ状態で反応させて露出されたホトレジスト９００および窒化シリコン膜７００、３００の表面上部に高分子(polymer)膜１０００を形成する。かかる高分子膜１０００は乾式エッチングを行なう場合、保護膜７００およびゲート絶縁層３００の側面部がエッチングされるのを減少させる役割をする。第３段階においては、図１８（ｃ）および図１９（ｃ）からみるように、モリブデン膜またはモリブデンータングステン合金膜６２０、６３０、６４０と窒化シリコン膜３００、７００とのエッチング選択比が１：１５以上の高い条件を有する乾式エッチング用ガス条件を適用してゲートパッド２２０上部の残っている窒化シリコン膜３００をエッチングして接触孔を完成する。このとき、用いる気体としてはホトレジスト９００がよくエッチングしなくてもCF_4+O_2が適切で、窒化シリコン膜７００、３００の側面部もエッチングされる。しかしながら、この気体のモリブデンータングステン合金膜のエッチング比は３００オングストローム／min程度であるので、ゲートパッド２２０が露出されるまでエッチングしてもデータパターン６２０、６３０、６４０のモリブデンータングステン合金膜はほ

とんどエッチングされない。また、高分子膜１０００が形成されているため、ゲートパッド２２０上部のゲート絶縁層３００の平面部に比べゲート絶縁層３００および保護膜７００の側面部のエッチング速度がさらに小さくなるので、接触孔７１０、７２０、７３０、７４０の側面部は緩やかな傾斜角を有するプロファイルが形成される。ここで、保護膜７００とゲート絶縁層３００のエッチング比がCF_4+O_2条件において異なるように現われるが、これは同一の窒化シリコンであっても形成する過程において膜の特性を異にして形成するためである。

【００５７】第２方法としては、モリブデン膜またはモリブデンータングステン合金膜と窒化シリコン膜とのエッチング選択比が１：１５以上に高い条件を有するプラズマ乾式エッチングを行なう途中に高分子膜を形成する段階をさらに含んで３回の工程を行なうのである。まず、図２０（ａ）および図２１（ａ）からみるように、CF_4+O_2ガスを用いてデータパターン６２０、６３０、６４０のモリブデンータングステン合金膜が露出されるまでエッチングして接触孔７１０、７３０、７４０を形成する。次いで、第２段階においては前述した方法と同様に、四フッ化炭素(CF_4)と水素(H_2)または塩化水素(HCl)を混合するガスをプラズマ状態で反応させて露出されたホトレジスト９００および窒化シリコン膜７００、３００表面の上部に高分子膜１０００を形成する（図２０（ｂ）および図２１（ｂ）参照）。かかる高分子膜１０００は同様に、窒化シリコン膜７００、３００が側面にエッチングされるのを遅延させる役割をする。また、ホトレジスト９００はイオンが側面部に向くのを妨害するため、側面部のエッチングが遅延される効果を高める。第３段階においては、第１段階と同一に行い接触孔を完成する（図２０（ｃ）および図２１（ｃ）参照）。かかる第２方法においては乾式エッチング用ガスを一つの条件に適用するため、第１方法より工程適用が簡単である。

【００５８】また、第１方法においては、$SF_6+HCl(+He)$または$SF_6+Cl_2(+He)$のガスを用いて第１段階のエッチング工程においてホトレジスト９００と窒化シリコン膜７００、３００を同様の程度にエッチングするため、保護膜７００の側面部に形成された高分子膜１０００が乾式エッチング気体の衝突で直接露出される。しかしながら、第２方法の第１段階のエッチング工程においては、CF_4+O_2ガスはホトレジスト９００に対し１０００オングストローム／min以下のエッチング比を有するので、図２１（ｃ）に示すように、保護膜７００はホトレジスト９００の下部においてアンダーカットが発生する。これに従い、図１７Ｃに示すように、第３段階工程においてCF_4+O_2ガスを用いて窒化シリコン膜７００、３００をエッチングするとき、ホトレジスト９００は保護膜７００の側面部に形成された高分子膜１０００がエッチング気体に直接露出されるのを防止する。このため、第２方法においては、ホトレジスト９００は保護膜７００の側面部がエッチングされるのを防止する効果を高めることができる。

【００５９】前述したプラズマエッチング方法において、モリブデンータングステン合金膜がエッチングされるのを最大限防止するため、CF_4に対するO_2の比率は４／１０以下とすることが好ましい。また、CF_4に対するO_2の比率が４／１０以下である場合には１段階で接触孔７１０、７２０、７３０、７４０を同時に形成することができる。かかる方法は表示装置の製造方法において金属膜上の絶縁膜の厚さが異なるため、厚さが薄い側の接触孔の下方の金属膜がエッチングされるのを防止し、接触孔の側面を緩やかな傾斜角でエッチングするための工程においてはすべて可能である。例えば、第１金属膜、第１絶縁膜、第２金属膜および第２絶縁膜が連続形成されている構造において、第２絶縁膜下部の第２金属膜を露出させる第１接触孔と第２および第１絶縁膜下部の第１金属膜を露出させる第２接触孔を同時に形成するとき適用できる。つまり、ホトレジストと絶縁膜に対し１ないし１．５倍のエッチング比を有するエッチング条件で絶縁膜の側面部が傾斜されるようにエッチングし、絶縁膜と金属膜とのエッチング選択比が１５：１以上であるエッチング条件で接触孔を完成する。このとき、高分子膜を形成する工程を追加して絶縁膜が側面にエッチングされるのを防止する。このとき、データパッド６３０を二重膜で形成しアルミニウム膜またはアルミニウム合金膜を上部膜で形成する場合、以後に形成されるＩＴＯとの接触を防止するため、アルミニウム膜またはアルミニウム合金膜を除去することにする。

【００６０】最後に、図１１に示すように、０．０３～０．２μmの厚さでＩＴＯを積層し第５マスクを用いて乾式エッチングし、接触孔７１０、７３０を通じてそれぞれドレイン電極６２０およびデータパッド６３０と接続される画素電極８００およびデータパッド用ＩＴＯ電極８２０、そして接触孔７２０を通じてゲートパッド２２０と接続されるゲートパッド用ＩＴＯ電極８１０からなるＩＴＯパターンを形成する。ここで、図１０でのように、ゲート補助パッド部６４０と接触孔７４０を追加する場合、ゲートパッド用ＩＴＯ電極８１０をゲート補助パッド部６４０まで延長されるように形成する。もし、ゲートパッド２２０の上層をアルミニウム膜またはアルミニウム合金膜を用いるとゲートパッド用ＩＴＯ電極８１０が直接接触して酸化反応が起こるため、ゲートパッドが不良になりやすいが、これはゲートパッド２２０の上層としてモリブデン合金膜を用いるとよい。

【００６１】次に、図２２および図２３を参照して本発明の第２の実施の形態に従う薄膜トランジスタ基板の構造について説明する。図２３は、図２２においてXIX－XIX'線の断面図であり、図９から図１１と同一符号は同様の機能を示す。基板１００上にゲート線２００および

その分枝であるゲート電極２１０、そしてゲート線２００の端部に形成されているゲートパッド２２０からなるゲートパターンが形成されている。ゲートパターンはモリブデンータングステン合金の単一膜からなり、ゲートパッド２２０は外部からの走査信号をゲート線２００に伝達する。

【００６２】ゲートパターン２００、２１０、２２０上にはゲート絶縁層３００が形成されており、このゲート絶縁層３００はゲートパッド２２０上部を露出させる接触孔７２０を有している。ゲート絶縁層３００上には水素化非晶質シリコン層４００が形成されている。水素化非晶質シリコン層４００はゲート電極２１０に該当する位置に形成されて薄膜トランジスタの活性層に機能しており、延長されて縦に長く形成されている。

【００６３】非晶質シリコン層４００上にはｎ形不純物が高濃度でドーピングされた水素化非晶質シリコン層５１０、５２０が形成されている。その上にはモリブデンータングステン合金膜からなるデータパターン６１０、６２０が形成されており、ドーピングされた非晶質シリコン層５１０、５２０とデータパターン６１０、６２０は同一形状に形成されている。これら二つの層はそれぞれゲート電極２１０に対し二つの部分（５１０、６１０：５２０、６２０）に分けられており、非晶質シリコン層４００の形状に沿い形成されている。

【００６４】データパターン６１０、６２０上にはＩＴＯなどの透明な導電物質からなる透明な導電層８３０、８４０が形成されており、この中で、一部８３０はデータパターンおよびドーピングされた非晶質シリコン層５１０のパターンに従い形成されており、他の一部８４０はデータパターン６２０を覆い画素の中央部分に延長されて画素電極になる。

【００６５】最後に、ＩＴＯパターン８３０、８４０およびＩＴＯパターンで覆われないゲート絶縁層３００上には保護膜７００が形成されており、この保護膜７００にはゲートパッド２２０および透明な導電層８３０の端部を露出させる接触孔７２０、７３０がそれぞれ形成されている。

【００６６】以下、添付図面を参照して図２２および図２３に示す薄膜トランジスタ基板の製造方法について詳細に説明する。図２４（ａ）から図２４（ｃ）は、図２２および図２３に示す薄膜トランジスタ基板の製造方法をその工程順序に従い示す断面図であり、４枚のマスクを用いた製造方法である。図２４（ａ）に示すように、透明な絶縁基板１００上に０．１～２．０μｍの厚さでモリブデンータングステン合金膜を積層し第１マスクを用いて写真工程を行いゲート線２００、ゲート電極２１０およびゲートパッド２２０を含むゲートパターンを形成する。ここで、モリブデンータングステン合金膜は原子百分率０．０１％以上２０％未満のタングステン(Ｗ)と残りのモリブデン(Ｍｏ)からなり、タングステン含有率は原子百分率９～１１％であることが好ましい。また、アルミニウムエッチング液、例えばCH_3COOH／HNO_3／H_3PO_4／H_2Oなどを用い、HNO_3の含量は好ましくは８～１４％の範囲である。また、ゲートパターンはモリブデンータングステン合金膜にアルミニウム膜またはアルミニウム合金を追加して二重膜で形成することができ、これらのうち、一つの物質を蒸着して単一膜で形成することができる。ここで、アルミニウム合金膜を用いる場合、アルミニウム合金膜はアルミニウムと５％以下の希土類金属または転移金属からなる。

【００６７】次に、窒化シリコンからなる０．２～１．０μｍの厚さでゲート絶縁層３００、０．１～０．３μｍの厚さで水素化非晶質シリコン層４００、０．０１５～０．１５μｍの厚さでＮ形高濃度不純物でドーピングされた水素化非晶質シリコン層５００および厚さ０．３～２．０μｍでモリブデンまたはモリブデンータングステン合金６００を順に積層し、第２マスクを用いて図２４（ｂ）に示すように、モリブデンータングステン合金膜６００、ドーピングされた非晶質シリコン層５００および非晶質シリコン層４００を順にパターニングする。モリブデンまたはモリブデンータングステン合金膜６００の代わりに、クロム、モリブデンまたはモリブデン合金のうち、一つの単一膜またはこれらを組み合わせた二重膜で形成することができる。また、抵抗を低めるためにアルミニウム膜またはアルミニウム合金膜を追加することができる。ここで、モリブデンータングステン合金膜６００の代わりに、下部膜はクロム膜、上部膜はモリブデンータングステン合金膜で形成する場合、同一のエッチング条件で上部膜と下部膜とを順にエッチングしてテーパ形状に加工することができる。このとき、前述したエッチング条件が湿式エッチングであると、エッチング液はクロムをエッチングするに用いられるエッチング液であって、例えば、HNO_3／$(NH_4)_2Ce(NO_3)_6$／H_2Oを挙げられ、このとき、HNO_3の濃度は４～１０％、$(NH_4)_2Ce(NO_3)_6$の濃度は１０～１５％であることが好ましい。

【００６８】次に、図２４（ｃ）に示すように、透明な導電物質であるＩＴＯを０．０３～０．２μｍの厚さで積層した後、第３マスクを用いて透明な導電層８３０、８４０を写真工程でパターニングする。その後、透明な導電層８３０、８４０をマスクにして露出されたモリブデンータングステン合金膜６００およびドーピングされた非晶質シリコン層５００をそれぞれ湿式および乾式エッチングしてデータパターン６１０、６２０およびコンタクト層としてドーピングされた非晶質シリコン層５１０、５２０を形成する。このとき、データパターン６１０、６２０が透明な導電層８３０、８４０により覆われているため、エッチングするための気体としては必ずハロゲン化水素とCF_4、CHF_3、$CHClF_2$、CH_3FおよびC_2F_6を用いなくてもよい。

【００６９】図２３に示すように、保護膜７００を０．

１～１．０μｍの厚さで積層した後、第４マスクを用いてゲート絶縁層３００と共にホトエッチングし、ゲートパッド２２０およびデータパターン６１０の端部に対応する透明な導電層８３０上部を露出させる接触孔７２０、７３０を形成する。

【００７０】以下、実験例１ないし実験例７について詳細に説明する。

実験例１

実験例１はモリブデン膜またはモリブデンータングステン合金膜の蒸着特性に関するものである。実験例１においては原子百分率１０at％のタングステンを含むモリブデンータングステン合金を基板１００の上部に蒸着した。このとき、蒸着温度は１５０℃程度である。図２５はモリブデンータングステン合金の蒸着圧力と応力との関係を示すグラフである。図２５に示すように、モリブデンータングステン合金膜の応力は蒸着圧力２～７mtorrの変化に従い圧縮力－３．０＊10^9程度から引張力６．０＊10^9まで変化する。従って、モリブデンータングステン合金膜の蒸着の際基板が歪まないようにモリブデンータングステン合金膜の応力を調節できるので、モリブデンータングステン合金膜の金属配線は大画面および高精細の液晶表示装置に使用の際にさらに有利である。このように、モリブデンータングステン合金膜を液晶表示装置の配線に用いると、小さい基板に適用でき、３７０＊４７０mm^2以上の大きさを有する基板にも適用できる。また、配線の厚さは０．３～２．０μｍ程度の範囲で、配線の幅は３．０～１０．０μｍ程度の範囲で形成することが好ましい。

【００７１】実験例２ないし実験例４はクロムとモリブデンまたはモリブデンータングステン合金膜を含む構造のエッチング比およびエッチングプロファイルに関するものである。

実験例２

実験例２においてはモリブデン膜またはモリブデンータングステン合金膜のエッチング比を測定した。図２６はタングステン(W)の含有量に従うクロムエッチング液HNO_3／$(NH_4)_2Ce(NO_3)_6$／H_2Oに対するモリブデンータングステン合金のエッチング比の特性を示すものである。同図からわかるように、タングステン含有量が０％であるとエッチング比は２５０オングストローム/sec程度に非常に大きく現れるが、タングステン含有量が１０％であるとエッチング比は１００オングストローム/sec程度に現れる。また、タングステン含有量が１５～２５％である場合には８０～４０オングストローム/sec程度に低下することがわかる。一方、クロムはHNO_3（４～１０％）：$(NH_4)_2Ce(NO_3)_6$（１０～１５％）：H_2Oからなるクロムエッチング液に対し４０～６０オングストローム/sec程度のエッチング比を有するので、これより大きいエッチング比を有するモリブデンータングステン合金膜をクロム膜の上部に形成すると緩やかな傾斜角を有する二重膜配線を得られる。

【００７２】実験例３

図２７は、下部のクロム膜と上部のモリブデンータングステン合金膜とからなる二重膜の断面図であり、基板１０００の上部にクロム膜２０００を２０００オングストローム、モリブデンータングステン合金膜３０００を８００オングストローム程度の厚さで順に蒸着した後、クロムをエッチングするに用いられるエッチング液であるHNO_3／$(NH_4)_2Ce(NO_3)_6$／H_2Oでエッチングした。このとき、タングステン含有率は２０％である。図２７に示すように、２０°程度の傾斜角を有するエッチングプロファイルが形成されている。

【００７３】実験例４

実験例４においては基板１０００の上部にクロム膜２０００を１５００オングストローム、モリブデンータングステン合金膜３０００を５００オングストローム程度の厚さで順に蒸着した後、エッチングした。その以外の条件は実験例１と同一である。図２８は本発明の実験例４に従うクロム膜とモリブデンータングステン合金膜のエッチングプロファイルを示す断面図である。実験例４においては図２８に示すように、１２～１５°程度の傾斜角を有するエッチングプロファイルが形成されている。かかる実験例からみるとき、データパターンまたはゲートパターンをモリブデンータングステン合金膜とクロム膜との二重膜を適用する場合、１回の工程を通じて緩やかな傾斜角を有するテーパ加工が可能でかつ低抵抗であるため、大画面の表示装置において有利である。

【００７４】次に、データパターン６１０、６２０をマスクにしてドーピングされた非晶質シリコン層５００をエッチングする工程について実験例５ないし７において詳細に説明する。図１５を参照して説明すると、基板１００に蒸着されているゲート電極２１０のうち、下部に形成されているアルミニウム合金膜２２１の厚さは２５００オングストローム程度であり、その上に形成されているモリブデンータングステン合金膜２２２の厚さは５００オングストローム程度である。また、ゲート絶縁膜３００は４５００オングストローム、非晶質シリコン層４００は２０００オングストローム、ドーピングされた非晶質シリコン層５００は５００オングストローム、データパターン６１０、６２０は４０００オングストロームおよび保護膜７００は３０００オングストローム程度の厚さを有する。ここで、データパターン６１０、６２０はタングステンを含むモリブデン合金またはモリブデンで形成する。

実験例５

実験例５においてはプラズマ乾式エッチング方法を通じてドーピングされた非晶質シリコン層５００をエッチングし、乾式エッチング用気体としては$HCl+SF_6$またはCl_2+SF_6を用いた。図２９は本発明の第１の実施の形態に従う薄膜トランジスタの製造方法のうち、実験例５にお

いて乾式エッチング用気体に対するＭｏＷのエッチング比を示す表である。　同図に示すように、乾式エッチング用気体としてHCl＋SF_6を用いる場合、２００～６１０オングストローム／min程度のエッチング比でデータパターン６１０、６２０のモリブデン合金が多量にエッチングされ、Cl_2＋SF_6を用いる場合には１５０～３２０オングストローム／min程度のエッチング比が現われた。

【００７５】実験例６

図３０は本発明の実験例６に従う薄膜トランジスタの製造方法を示す断面図である。同図に示すように、ホトレジスト９００をマスクにして湿式エッチング方法を通じてモリブデン合金からなる金属層をパターニングしてデータパターン６１０、６２０を形成した。次いで、データパターン６１０、６２０がエッチングされるのを防止するため、ホトレジスト９００を除去しない状態において、これをマスクにしてドーピングされた非晶質シリコン層５００をエッチングし、乾式エッチング用気体としてはHCl＋SF_6を用いた。従って、ソース／ドレイン電極６１０、６２０はエッチングされなかった。一方、乾式エッチングで硬化しているホトレジスト９００を除去するため、アシング(ashing)工程をさらに行い、非晶質シリコン層４００表面をよくするために水素プラズマ工程を選択的に行なった。図３１は、本発明の実験例６に従う薄膜トランジスタの特性を示すグラフであって、アシング工程のみを行なう場合と、アシング工程および水素プラズマ工程を行なった場合とについてそれぞれ薄膜トランジスタの特性を測定した結果である。Ｙ軸はソースードレイン間の電流(Ａ)をログで示すものであり、Ｘ軸はゲート電圧(Ｖｇ)である。アシング工程のみを行なった場合と、アシング工程および水素プラズマ工程いずれもを行なった場合とを比較すると、アシング工程で用いられる酸素気体により非晶質シリコン層４００の表面が酸化されるため、薄膜トランジスタの特性が劣化された。また、水素プラズマ工程をさらに行なうことにより、非晶質シリコン層４００表面の酸化を除去でき、オフ電流が低くなることがわかる。

【００７６】実験例７

実験例７においては乾式エッチング用気体HCl＋CF_4を用いてドーピングされた非結晶シリコン層５００を乾式エッチングし、データパターン６１０、６２０上部にホトレジストを形成しない状態で行なった。また、アシング工程および水素プラズマ工程は行なわなかった。図３２は乾式エッチング用気体に対するＭｏＷのエッチング比を示す表である。図３２に示すように、乾式エッチング用気体としてHCl＋CF_4を用いる場合、１５～８０オングストローム／min程度のエッチングでデータパターン６１０、６２０のモリブデン合金がエッチングされた。かかる結果を実験例５と比較すると、HCl＋SF_6またはCl_2＋SF_6を用いる場合より非常に少ない量がエッチングされることがわかる。図３３は本発明の実験例７に従う薄膜トランジスタの特性を示すグラフである。図面において、Ｙ軸の左側はソースードレイン間の電流(Ａ)であり、右側は素子の特性傾きであり、Ｘ軸はゲート電圧(Ｖｇ)である。図３３に示すように、アシング工程および水素プラズマ工程を省略してもソースードレイン間のオン／オフ電流特性は良好に測定された。また、ドーピングされた非晶質シリコン層をその上のモリブデンまたはモリブデンータングステン合金をマスクにしてエッチングするすべての半導体装置の製造方法においてハロゲン化水素気体とCF_4、CHF_3、$CHClF_2$、CH_3FおよびC_2F_6のうち、少なくとも一つの気体を用いられる。

【００７７】

【発明の効果】以上のように、本発明に従う表示装置の製造方法においてはモリブデン合金は１５Ωcm以下の低抵抗を有し、テーパの加工の際アルミニウムエッチング液およびクロムエッチング液を用いられるので、アルミニウムおよびクロムと共に表示装置または半導体装置の配線に用いるに非常に容易である。また、モリブデン膜またはモリブデンータングステン合金膜は蒸着圧力に従い膜の応力を変化させて基板が歪まない条件で厚く形成することができるので、高精細および大画面の表示装置用配線に適合である。そして、接触孔を形成するとき保護膜およびゲート絶縁層の側面部のエッチングを遅延させる高分子膜を形成するかCF_4＋O_2を用いてモリブデン合金膜がエッチングされないようにし、SF_6＋HCl(＋He)またはSF_6＋Cl_2(＋He)を用いて接触孔のフレームが緩やかな傾斜を有するように形成できる。また、モリブデンまたはモリブデンータングステン合金膜をマスクにして非結晶シリコン層をエッチングするとき、ハロゲン化水素気体とCF_4、CHF_3、$CHClF_2$、CH_3FおよびC_2F_6のうち、少なくとも一つの気体を用いて良好な薄膜トランジスタの特性を得た。そして、水素プラズマ工程を通じて薄膜トランジスタの特性が向上される。

【図面の簡単な説明】

【図１】　本発明の一実施の形態として示したモリブデン合金(ＭｏＷ)膜の特性を示すグラフである。

【図２】　本発明の一実施の形態として示したモリブデン合金(ＭｏＷ)膜の特性を示すグラフである。

【図３】　本発明の一実施の形態として示したモリブデン合金(ＭｏＷ)膜の特性を示すグラフである。

【図４】　本発明に従うモリブデン合金(ＭｏＷ)膜のエッチングプロファイルを示す断面図である。

【図５】　本発明の一実施の形態として示したモリブデン合金(ＭｏＷ)とアルミニウム合金(Al alloy)からなる二重膜のエッチングプロファイルを示す断面図である。

【図６】　本発明の一実施の形態として示したモリブデン合金(ＭｏＷ)とアルミニウム合金(Al alloy)からなる二重膜のエッチングプロファイルを示す断面図である。

【図７】　本発明の一実施の形態として示したモリブデン合金(ＭｏＷ)とアルミニウム合金(Al alloy)からなる

二重膜のエッチングプロファイルを示す断面図である。

【図８】　本発明の一実施の形態として示したモリブデン合金(ＭｏW)とアルミニウム合金(Al alloy)からなる二重膜のエッチングプロファイルを示す断面図である。

【図９】　本発明の一実施の形態として示した薄膜トランジスタ基板の構造を示す平面図である。

【図１０】　本発明の一実施の形態として示した薄膜トランジスタ基板の構造を示す平面図である。

【図１１】　図９においてＸ－Ｘ’線に沿い切断した断面図である。

【図１２】　本発明の一実施の形態として示した薄膜トランジスタ基板の製造方法を示す断面図である。

【図１３】　本発明の一実施の形態として示した薄膜トランジスタ基板の製造方法を示す断面図である。

【図１４】　本発明の一実施の形態として示した薄膜トランジスタ基板の製造方法を示す断面図である。

【図１５】　本発明の一実施の形態として示した薄膜トランジスタ基板の製造方法を示す断面図である。

【図１６】　本発明の一実施の形態として示した薄膜トランジスタ基板の上部に接触孔を形成する工程を詳細に示す断面図である。

【図１７】　本発明の一実施の形態として示した薄膜トランジスタ基板の上部に接触孔を形成する工程を詳細に示す断面図である。

【図１８】　本発明の一実施の形態として示した薄膜トランジスタ基板の上部に接触孔を形成する工程を詳細に示す断面図である。

【図１９】　本発明の一実施の形態として示した薄膜トランジスタ基板の上部に接触孔を形成する工程を詳細に示す断面図である。

【図２０】　本発明の一実施の形態として示した薄膜トランジスタ基板の上部に接触孔を形成する工程を詳細に示す断面図である。

【図２１】　本発明の一実施の形態として示した薄膜トランジスタ基板の上部に接触孔を形成する工程を詳細に示す断面図である。

【図２２】　本発明の第２の実施の形態として示した薄膜トランジスタ基板の構造を示す平面図である。

【図２３】　図２２においてＸＩＸ－ＸＩＸ’線に沿い切断した断面図である。

【図２４】　本発明の第２の実施の形態として示した薄膜トランジスタ基板の製造方法を示す断面図である。　＊

＊【図２５】　本発明の実験例１に従うモリブデンータングステン合金に対する蒸着圧力と応力との関係を示すグラフである。

【図２６】　本発明の実験例２に従うモリブデンータングステン合金膜のエッチング比を示すグラフである。

【図２７】　本発明の実験例３に従う薄膜トランジスタの製造方法においてデータパターンを二重膜で形成する場合のエッチングプロファイルを示す断面図である。

【図２８】　本発明の実験例４に従う薄膜トランジスタの製造方法においてデータパターンを二重膜で形成する場合のエッチングプロファイルを示す断面図である。

【図２９】　本発明の実施の形態に従う薄膜トランジスタの製造方法のうち、実験例５において乾式エッチング用気体に対するＭｏWのエッチング比を示す図表である。

【図３０】　本発明の実験例６に従う薄膜トランジスタの製造方法を示す断面図である。

【図３１】　本発明の実験例７に従う薄膜トランジスタの特性を示すグラフである。

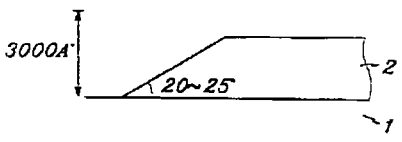
【図３２】　本発明の第１の実施の形態として示した薄膜トランジスタの製造方法のうち、実験例７において乾式エッチング用気体に対するＭｏWのエッチング比を示す図表である。

【図３３】　本発明の実験例７に従う薄膜トランジスタの特性を示すグラフである。

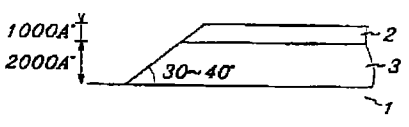
【符号の説明】

１　基板
２　モリブデンータングステン合金膜
３　アルミニウム合金膜
１００　基板
２００　ゲート線
２１０　ゲート電極
２２０　ゲートパッド
３００　ゲート絶縁層
４００、５００、５１０、５２０　非晶質シリコン層
６００　モリブデンータングステン合金
６４０　ゲート補助パッド
７００　保護膜
７４０　接触孔
８１０　ＩＴＯ電極
８３０　透明な導電層

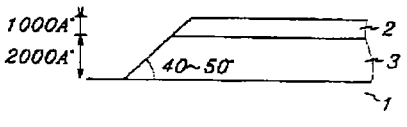
【図４】



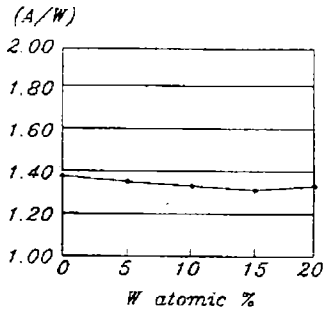
【図５】



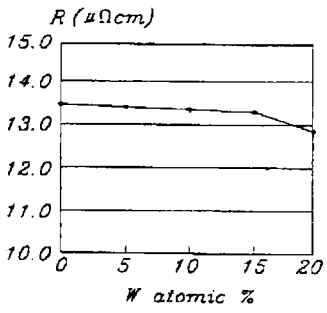
【図６】



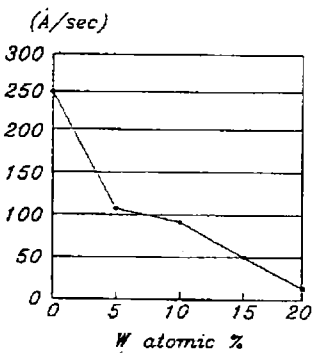
【図１】



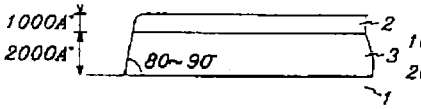
【図２】



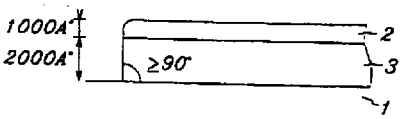
【図３】



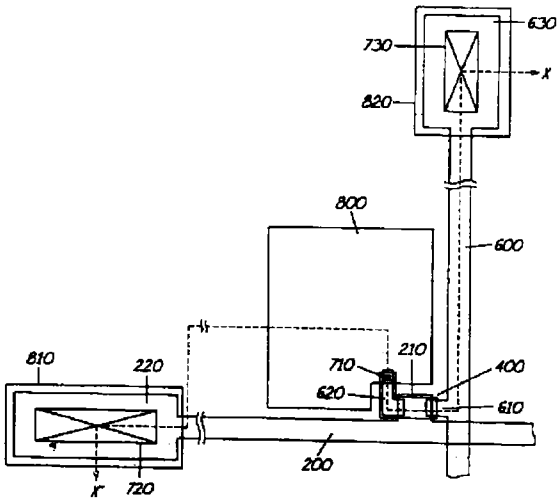
【図７】



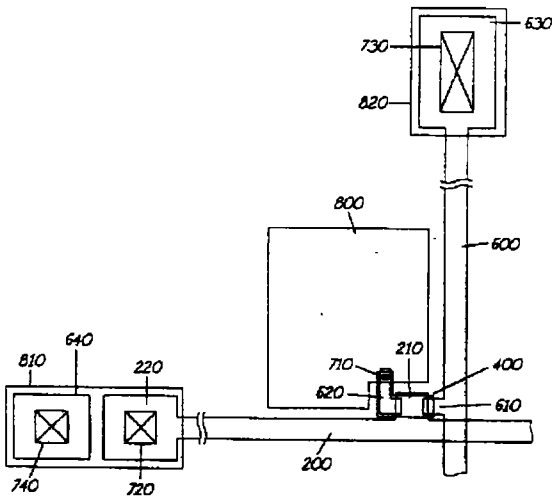
【図８】



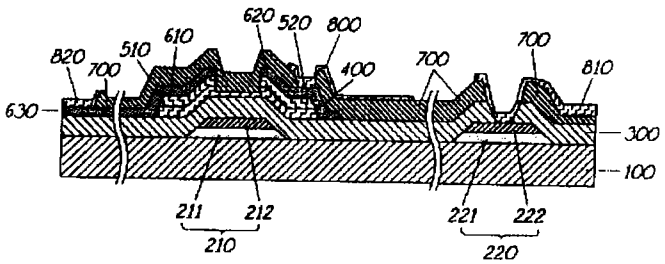
【図９】



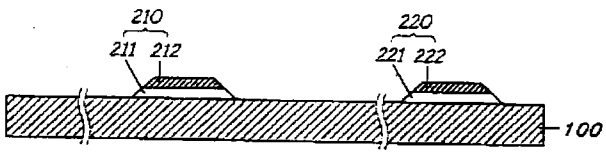
【図１０】



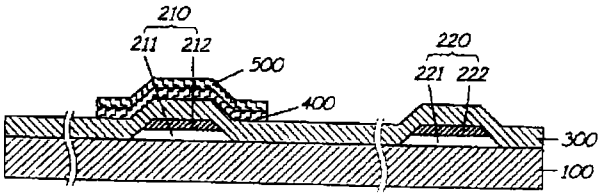
【図１１】



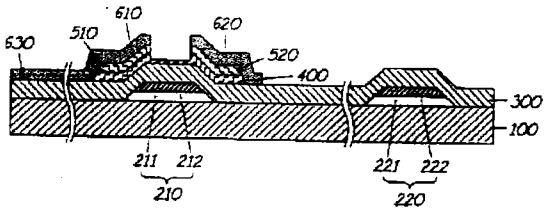
【図１２】



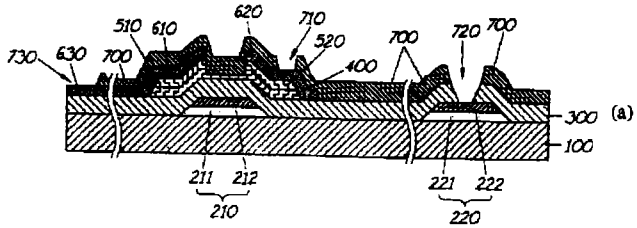
【図１３】



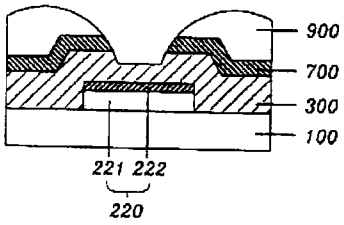
【図１４】



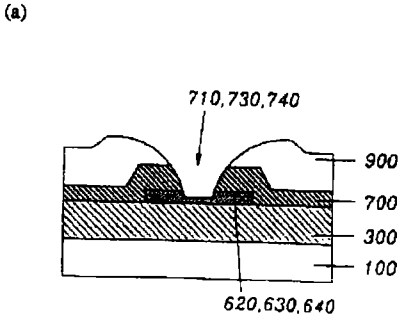
【図１５】

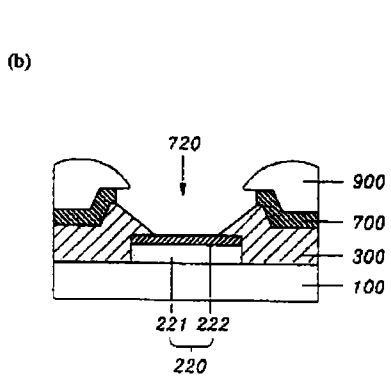


【図１６】

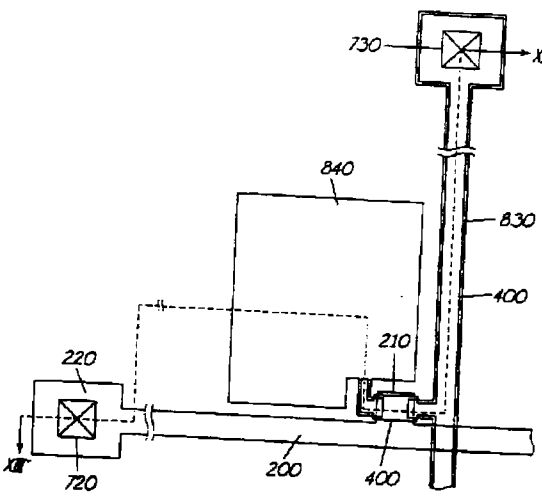


【図１７】

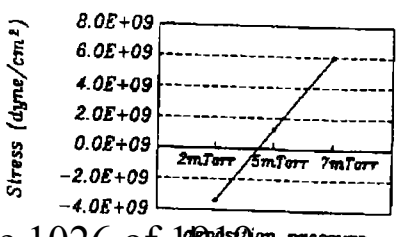




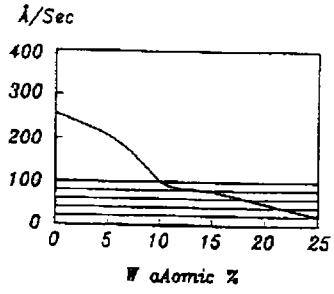
【図２２】



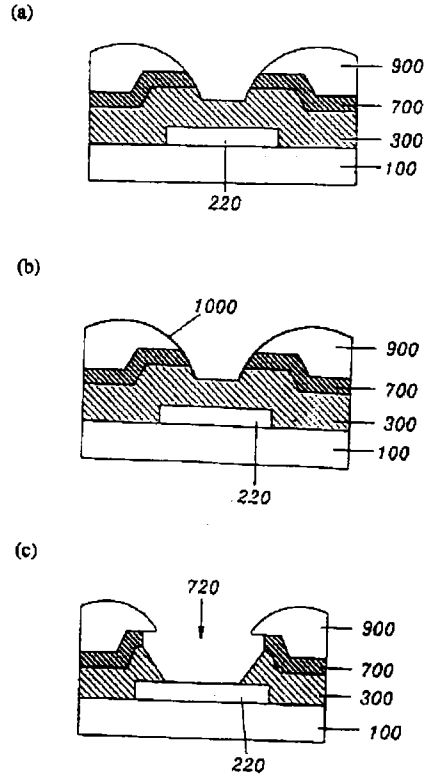
【図２５】



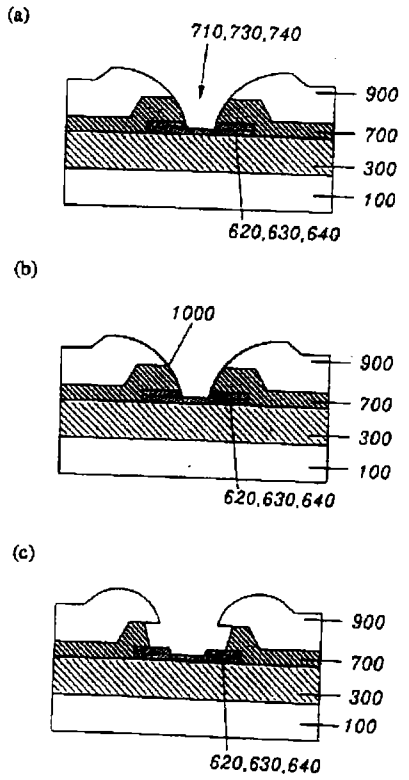
【図２６】



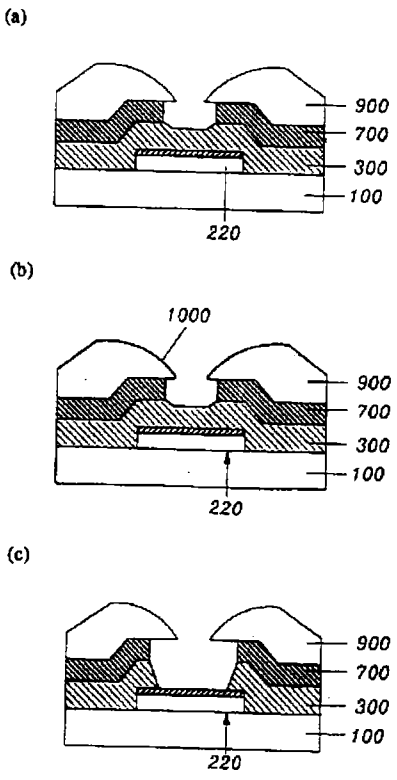
【図１８】



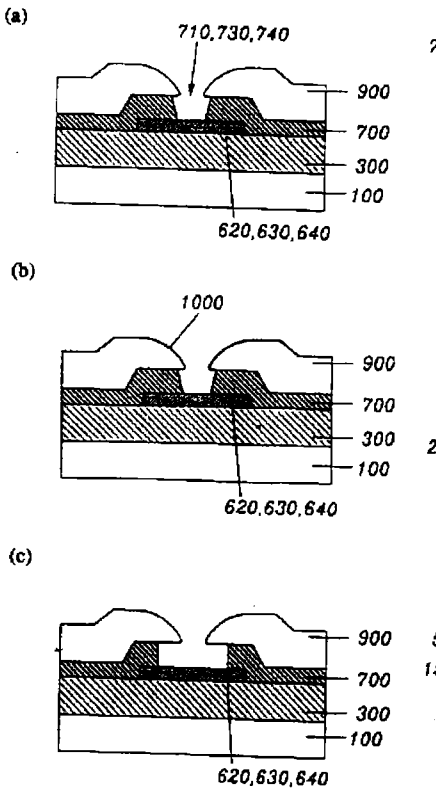
【図１９】



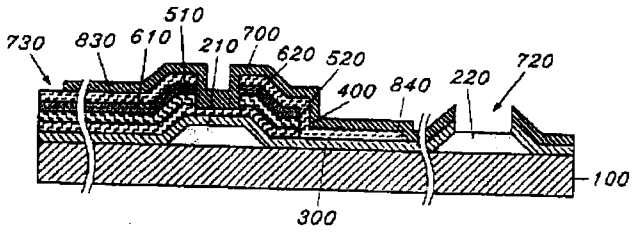
【図２０】



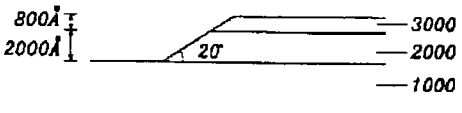
【図２１】



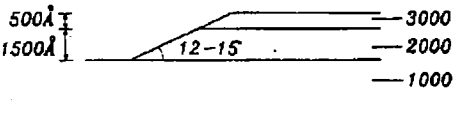
【図２３】



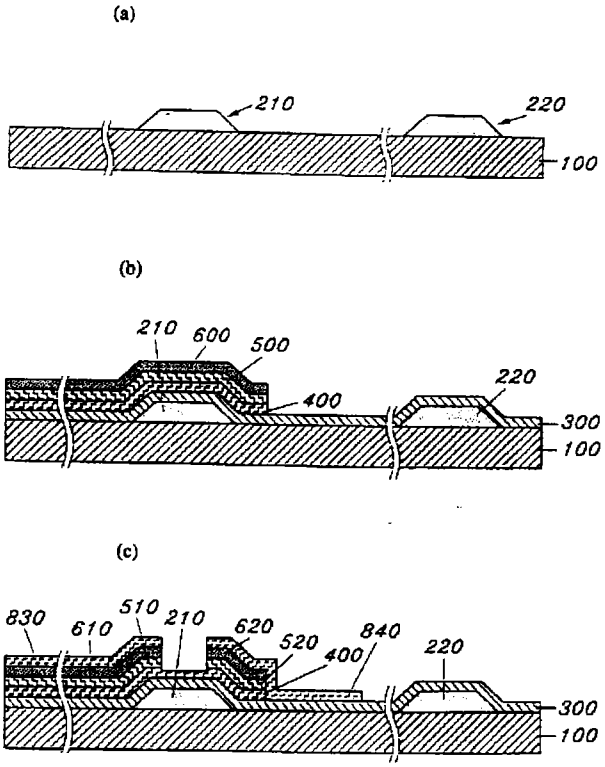
【図２７】



【図２８】



【図２４】



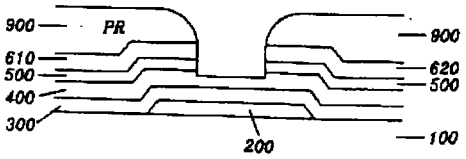
【図２９】

MoW content (atm%)	Cl2+SF6	HCl+SF6
0%	200Å/min	150Å/min
0% – 10%	243Å/min	261Å/min
10% – 20%	592Å/min	280Å/min
20% – 30%	604Å/min	313Å/min

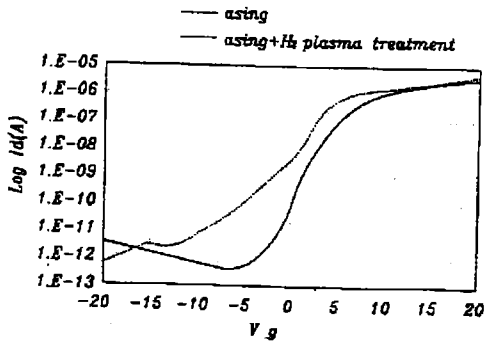
【図３２】

MoW content (atm%)	HCL+CF4
0%	17Å/min
0% –10%	20Å/min
10% –20%	80Å/min
20% –30%	50Å/min

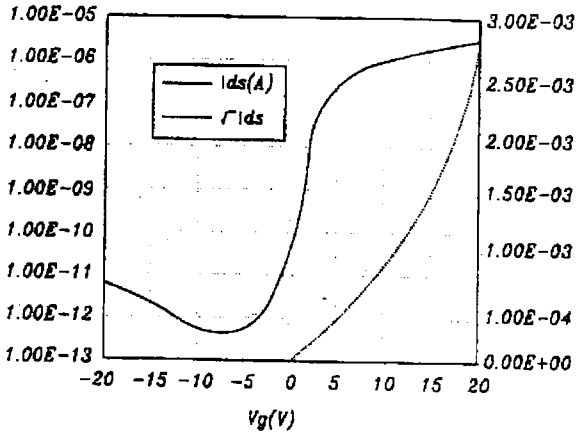
【図３０】



【図３１】



【図３３】



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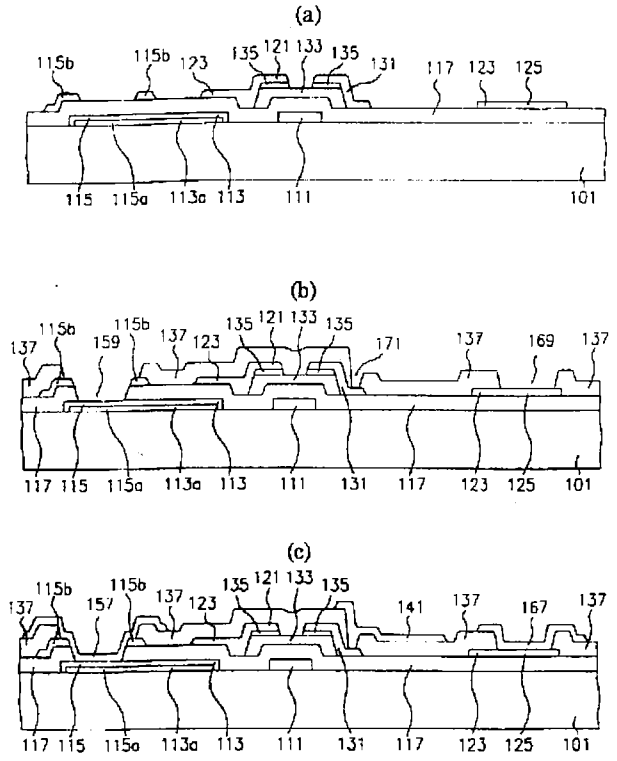
(54)【発明の名称】　液晶表示装置及びその製造方法

(57)【要約】

【課題】　本発明は、エッチャントの浸透からゲートパッドを保護することができる液晶表示装置及びその製造方法を提供することを目的とする。

【解決手段】　基板１０１、ゲート配線１１３、ゲート配線から分岐した少なくとも一つのゲート電極１１１、ゲート配線の端部に配置されるゲートパッド１１５を形成する段階とを含む。そして、ゲート配線と基板を覆うようにゲート絶縁層１１７を形成して、ゲートパッドの少なくとも外周部の前記ゲート絶縁層上にダミーゲートパッド１１５ｂを形成する。前記ダミーゲートパッドは液晶表示装置の製造過程の中に用いられるエッチャントがゲートパッドの外周部から浸透することを防止する。



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【特許請求の範囲】

【請求項１】　基板上にゲート配線、前記ゲート配線から分岐する少なくとも一つのゲート電極、そして、前記ゲート配線の端部に位置されている外周部を有するゲートパッドを形成する段階と、

前記ゲート配線、前記ゲート電極及び前記ゲートパッドが形成された前記基板上にゲート絶縁層を形成する段階と、

前記ゲートパッドの外周部の少なくとも一部分を覆う前記ゲート絶縁層上に第１ダミーゲートパッドを形成する段階とを含むことを特徴とする液晶表示装置の製造方法。

【請求項２】　前記第１ダミーゲートパッドをマスクとして前記ゲート絶縁層をエッチングして前記ゲートパッドの一部を露出させてゲートパッドコンタクトホールを形成する段階を含むことを特徴とする請求項１記載の液晶表示装置の製造方法。

【請求項３】　前記ゲートパッド上に前記ゲートパッドコンタクトホールを通じて前記ゲートパッドと接触するゲートパッド連結端子を形成する段階を含むことを特徴とする請求項２記載の液晶表示装置の製造方法。

【請求項４】　前記第１ダミーゲートパッドは、半導体物質から成ることを特徴とする請求項１記載の液晶表示装置の製造方法。

【請求項５】　前記第１ダミーゲートパッドは、導電物質から成ることを特徴とする請求項１記載の液晶表示装置の製造方法。

【請求項６】　前記第１ダミーゲートパッド上に第２ダミーゲートパッドを形成する段階を含むことを特徴とする請求項１記載の液晶表示装置の製造方法。

【請求項７】　半導体物質から前記第１ダミーゲートパッドを形成し、導電物質から前記第２ダミーゲートパッドを形成することを特徴とする請求項６記載の液晶表示装置の製造方法。

【請求項８】　前記第１ダミーゲートパッドは、半導体物質をパターニングして形成し、前記ゲート電極上に半導体層を形成する段階を含むことを特徴とする請求項１記載の液晶表示装置の製造方法。

【請求項９】　第１導電物質をパターニングして前記ゲート電極の一方の上の前記半導体層の第１部分上にドレイン電極を形成し、前記ゲート電極の他方上の前記半導体層の第２部分上にソース電極を形成する段階と、

前記基板上に保護層を形成する段階と、

前記保護層を選択的にエッチングして前記ドレイン電極の一部を露出させるドレインコンタクトホールを形成し、前記ゲートパッド上に形成された前記ゲート絶縁層の一部と前記第１ゲートパッドの一部を露出させるゲートパッドコンタクトホールを形成する段階と、

前記第１ダミーゲートパッドをマスクとして前記ゲート絶縁層を選択的にエッチングして前記ゲートパッドコンタクトホールが完全に露出されるように形成する段階と、

第２導電物質をパターニングして前記ゲートパッドコンタクトホールを通じて前記ゲートパッドに接触するゲートパッド連結端子を形成し、前記ドレインコンタクトホールを通じて前記ドレイン電極に接触する画素電極を形成する段階を含むことを特徴とする請求項８記載の液晶表示装置の製造方法。

【請求項１０】　前記第１導電物質をパターニングして前記ソースに連結されるソース配線と前記ソース配線の端部分にソースパッドとを形成し、

前記保護層を選択的にエッチングして前記ソースパッドの一部分を露出させるソースパッドコンタクトホールを形成し、

前記第２導電物質をパターニングして前記ソースパッドコンタクトホールを通じて前記ソースパッドに接触するソースパッド連結端子を形成することを特徴とする請求項９記載の液晶表示装置の製造方法。

【請求項１１】　前記第１導電物質をパターニングして前記第１ダミーゲートパッドに第２ダミーゲートパッドを形成し、

前記保護層を選択的にエッチングして前記第２ダミーゲートパッドの一部を露出させ、前記ゲートパッド上に前記ゲートコンタクトホールを形成することを特徴とする請求項９記載の液晶表示装置の製造方法。

【請求項１２】　前記第１導電物質をパターニングする段階で、前記ゲートパッドコンタクトホールが傾斜された階段形状の構造を有するように前記第２ダミーゲートパッドを形成することを特徴とする請求項１１記載の液晶表示装置の製造方法。

【請求項１３】　前記傾斜された側壁の構造が階段の形状を有することを特徴とする請求項１２記載の液晶表示装置の製造方法。

【請求項１４】　前記保護層、前記第１ダミーゲートパッド及び前記ゲート絶縁層に階段形状の前記ゲートパッドコンタクトホールを形成することを特徴とする請求項９記載の液晶表示装置の製造方法。

【請求項１５】　前記保護層の選択的エッチング段階と前記ゲート絶縁層の選択的エッチング段階は、連続的に一段階で行われることを特徴とする請求項９記載の液晶表示装置の製造方法。

【請求項１６】　半導体物質をパターニングして前記ゲート電極上に半導体層を形成する段階と、

前記第１ダミーゲートパッドを形成する段階で前記第１導電物質をパターニングして前記第１ダミーゲートパッドを形成し、前記ゲート電極の一方上の前記半導体層上にドレイン電極を形成し、前記ゲート電極の他方上の前記半導体層上にソース電極を形成する段階を含むことを特徴とする請求項１記載の液晶表示装置の製造方法。

【請求項１７】　前記基板上に保護層を形成する段階

と、
前記保護層を選択的にエッチングして前記ドレイン電極を露出させるドレインコンタクトホールを形成し、前記ゲートパッド上に前記ゲート絶縁層の一部と前記第１ダミーゲートパッドの一部を露出させるゲートコンタクトホールの一部を形成する段階と、
前記第１ダミーゲートパッドをマスクとして前記ゲート絶縁層を選択的にエッチングして前記ゲートコンタクトホールが完全に露出されるように形成する段階と、
第２導電物質をパターニングして前記ゲートパッドコンタクトホールを通じて前記ゲートパッドに接触するゲートパッド連結端子を形成し、前記ドレインコンタクトホールを通じて前記ドレイン電極に接触する画素電極を形成する段階とを含むことを特徴とする請求項１６記載の液晶表示装置の製造方法。
【請求項１８】　前記第１ダミーゲートパッドを形成する段階で、前記第１導電物質をパターニングして前記ソースに連結されるソース配線を形成し、前記ソースパッドを前記ソース配線の端部分に形成し、
前記保護層を選択的にエッチングする段階で、前記ソースパッドの一部を露出させるソースコンタクトホールを加えて形成し、
前記第２導電物質をパターニングする段階で、前記ソースパッドコンタクトホールを通じて前記ソースパッドに接触されるソースパッド連結端子を形成することを特徴とする請求項１７記載の液晶表示装置の製造方法。
【請求項１９】　前記ゲート配線を形成する段階で、
前記基板上に第１導電物質をパターニングして低抵抗ゲート配線と前記低抵抗ゲート配線の端部分に低抵抗ゲートパッドを形成し、
第２導電物質をパターニングして前記低抵抗ゲート配線の少なくとも一部上にゲート配線と、前記ゲート配線で分岐された少なくとも一つのゲート電極と、そして前記ゲート配線の端部分に位置して前記低抵抗ゲートパッドの少なくとも一部を覆うゲートパッドを形成する段階を含むことを特徴とする請求項１記載の液晶表示装置の製造方法。
【請求項２０】　前記第１導電物質はアルミニウムを含むことを特徴とする請求項１９記載の液晶表示装置の製造方法。
【請求項２１】　前記第２導電物質はクローム、モリブデン、タンタル、そして、アンチモンの中の少なくとも一つを含むことを特徴とする請求項１９記載の液晶表示装置の製造方法。
【請求項２２】　基板と、
前記基板上に形成されたゲート配線と、
前記基板上の前記ゲート配線から分岐する少なくとも一つのゲート電極と、
前記基板上で前記ゲート配線の端部に形成された外周部と、
前記基板上の前記ゲート配線、前記ゲート電極及び前記ゲートパッドを覆うゲート絶縁層と、
前記ゲートパッドの外周部の少なくとも一部分上の前記ゲート絶縁層上に形成された第１ダミーゲートパッドとを備える液晶表示装置。
【請求項２３】　前記ゲート絶縁層及び前記第１ダミーゲートパッドには前記ゲートパッドの一部を露出させるゲートパッドコンタクトホールを形成することを特徴とする請求項２２記載の液晶表示装置。
【請求項２４】　前記ゲートパッドコンタクトホールを通じて前記ゲートパッドと接触する前記ゲートパッド上に形成されたゲートパッド連結端子を加えて含むことを特徴とする請求項２３記載の液晶表示装置。
【請求項２５】　前記第１ダミーゲートパッドは、半導体物質を含むことを特徴とする請求項２２記載の液晶表示装置。
【請求項２６】　前記第１ダミーゲートパッドは、導電物質を含むことを特徴とする請求項２２記載の液晶表示装置。
【請求項２７】　前記第１ダミーゲートパッド上に形成された第２ダミーゲートパッドを加えて含むことを特徴とする請求項２２記載の液晶表示装置。
【請求項２８】　前記第１ダミーゲートパッドは半導体物質を含み、
前記第２ダミーゲートパッドは導電物質を含むことを特徴とする請求項２７記載の液晶表示装置。
【請求項２９】　前記ゲート電極上の前記ゲート絶縁層上の一部分に形成された半導体層と、
前記ゲート電極の一方上の前記半導体層の第１部分上に形成されたドレイン電極と、
前記ゲート電極の他方上の前記半導体層の第２部分上に形成されたソース電極と、
前記基板上に形成され、前記ドレイン電極を露出させるドレインコンタクトホールが形成された保護層と、
前記保護層、前記第１ダミーゲートパッド及び前記ゲート絶縁層には前記ゲートパッドの一部を露出させるゲートパッドコンタクトホールを形成し、
前記ゲートパッドコンタクトホールを通じて前記ゲートパッドに連結するゲートパッド連結端子と、
前記ドレインコンタクトホールを通じて前記ドレイン電極に連結する画素電極とを含むことを特徴とする請求項２２記載の液晶表示装置。
【請求項３０】　前記ゲート絶縁層上に形成され、前記ソース電極に連結されるように形成されたソース配線と、
前記ソース配電の端部分に形成されたソースパッドと、
前記保護層をエッチングして前記ソースパッドの一部を露出させるソースパッドコンタクトホールと、
前記ソースパッドコンタクトホールを通じて前記ソースパッドに接触されるソースパッド連結端子とを含むこと

を特徴とする請求項２９記載の液晶表示装置。

【請求項３１】　前記第１ダミーゲートパッド上に形成された第２ダミーゲートパッドと、

前記保護層、前記第１ダミーゲートパッド、前記第２ダミーゲートパッド及び前記ゲート絶縁層に前記ゲートパッドコンタクトホールを形成する段階を含むことを特徴とする請求項２９記載の液晶表示装置。

【請求項３２】　前記第１及び第２ダミーゲートパッドに傾斜された側壁を有するゲートパッドコンタクトホールを形成することを特徴とする請求項３１記載の液晶表示装置。

【請求項３３】　傾斜される側壁が階段構造を有することを特徴とする請求項３２記載の液晶表示装置。

【請求項３４】　前記保護層、前記第１ダミーゲートパッド及び前記ゲート絶縁層に階段構造の側壁を有するゲートパッドコンタクトホールを形成することを特徴とする請求項２９記載の液晶表示装置。

【請求項３５】　前記ゲート配線及び前記ゲートパッドは前記基板上に形成された低抵抗性の第１導電物質と、前記第１導電物質の少なくとも一部上に形成された第２導電物質とを含むことを特徴とする請求項２２記載の液晶表示装置。

【請求項３６】　前記第１導電物質はアルミニウムを含むことを特徴とする請求項３５記載の液晶表示装置。

【請求項３７】　前記第２導電物質はクローム、モリブデン、タンタル、又はアンチモンの中の一つを含むことを特徴とする請求項３５記載の液晶表示装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、液晶表示装置（以下に“AMLCD”と略する）及びその製造方法に関する。特に、本発明は、薄膜トランジスタ（ＴＦＴ）、該薄膜トランジスタに連結された画素電極とを含んで製造工程を単純化させた液晶表示装置の製造方法およびその液晶表示装置に関する。

【０００２】

【従来の技術】今まで画像情報を画面に示す画面表示装置の中、ブラウン管表示装置（Cathode Ray Tube; CRT）が多く用いられている。しかし、最近には薄型及び軽量という長点のためにいずれの場所でも容易に使用が出来る薄膜型の平板表示装置と代替されつつある。特に、液晶表示装置は、表示解像度が他の平板装置より優れており、動画像を具現する際にその品質がブラウン管に比べることが出来る程に反応速度が早いため、最も活発な研究開発が行われている。

【０００３】液晶表示装置の駆動原理は、液晶の光学的異方性と分極性質を利用したことである。液晶分子は細長く、方向性及び分極性を有している。このような性質を利用して液晶分子に人為的に電磁気場を印加することで配列方向を調節することが出来る。液晶分子の配向方向と、液晶の光学的異方性とを用いて光を透過、又は遮断することが出来る。

【０００４】現在には、行列方式で配列された薄膜トランジスタと、画素電極とを含むアクティブマトリクス液晶表示装置は、優れた画質の特性と自然色を提供するので、最も注目されている製品である。

【０００５】従来の液晶表示装置の構造は、次の如くである。従来の液晶表示装置は、様々な素子が設けられた二つのパネルが対向し、その間に液晶層が介されている形状である。一般にカラーフィルターパネルと呼ばれる第１パネルには、色を現す複数個の素子が構成されている。

【０００６】前記カラーフィルターパネルには、第２パネルの画素の位置に合わせて赤（Ｒ）、緑（Ｇ）、青（Ｂ）のカラーフィルターが順次に配列されている。前記カラーフィルターの間には、細いブラックマトリクスが形成されている。それは、他のカラーフィルター間の境界を明確に区分し、混合色が発生することを防止する。又、前記カラーフィルター上に共通電極が形成されている。前記共通電極は、前記液晶に電気場を印加するための一方の電極としての役割をする。

【０００７】従来の液晶表示装置の他方の前記第２パネルは、スイッチ素子と、前記液晶に電界を印加するための導電性の配線とを含む。前記第２パネルをアクティブパネルと称する。前記アクティブパネルには、透明基板上に前記画素の位置に合わせて複数の画素電極が形成されている。前記画素電極は、前記カラーフィルターパネル上に形成されている共通電極と対向して、液晶に電気場を印加する他方の電極としての役割をする。

【０００８】前記複数の画素電極の水平配列方向に沿って複数の信号配線が形成されており、垂直配列方向に沿っては、複数のデータ配線が形成されている。前記各々の画素電極の一部には、前記画素に電気場信号を印加する前記薄膜トランジスタが形成されている。前記薄膜トランジスタのゲート電極は、信号配線の一つに対応するように連結されており、ソース電極はデータ配線の一つに対応するように連結されている。前記信号配線を“ゲート配線”とも称し、前記データ配線を“ソース配線”とも称する。前記薄膜トランジスタのドレイン電極は、前記画素電極に連結されている。又、前記ゲート配線及び前記ソース配線の端部には、外部から印加される信号を受け取るための終端端子（Terminal）、又はパッドが形成されている。

【０００９】外部ソースから電気信号が前記ゲートパッドに印加される際、信号は前記ゲート配線を通じて前記ゲート電極に印加される。ソース配線は前記ソースパッドに外部から印加された画像情報をソース電極に印加する。ゲート電極はソース電極からの画像情報をドレイン電極に印加するかないかを調節する。従って、前記ゲート電極に印加される信号を調節することによって、前記

ドレイン電極へのデータ信号の印加が決定される。従って、前記薄膜トランジスタの前記ドレイン電極に連結されている前記画素電極にデータ信号を選択的に印加することが出来る。即ち、各々の前記薄膜トランジスタは、対応する画素電極を駆動させるためのスイッチとしての役割をする。

【００１０】前述した第１、第２のパネルは、所定の間隔（セルギャップ；Cell Gap）を隔てて対向されており、前記両パネル間のセルギャップに液晶物質が注入されている。各々のパネルの外側部にはパネルからの光を選択的に透過させるための偏光板が形成されている。これで液晶表示装置の重要要素である液晶パネルが完成される。

【００１１】前記液晶パネルの製造工程は複雑であり、多数の製造工程が要求される。特に、薄膜トランジスタを含むアクティブパネルを製造するには、いろいろな工程が要求される。このように複雑な製造工程によって製品の性能が決定されるため、可能な限り工程が簡単であれば、不良が発生する確率が少なくなる。さらに、前記アクティブパネルには、液晶表示装置の性能を決定する重要な素子が多く形成されているため、前記アクティブパネルの製造工程を単純化させることが良い製品を生産する重要な役割をする。

【００１２】図１は、従来の液晶表示装置のアクティブパネルの一部を示し、図２（ａ）～図３（ｃ）は、図１のII－II線に沿った従来のアクティブパネルの製造方法を説明するための断面図である。

【００１３】図１、図２（ａ）に示すように、透明ガラス基板１にアルミニウム合金を蒸着し、フォトリソグラフィー法(Photo-Lithography；写真食刻法）で各々所定の形状を有するようにパターニングしてゲート電極１１、ゲート配線１３、ゲートパッド１５、ソースパッド２５及び短絡配線４５を形成する。前記ゲート電極１１はマトリクス状で配列された画素の一つの隅部に対応するように位置されている。前記ゲート配線１３は、前記行方向に配列されたゲート電極１１と連結されている。前記ゲートパッド１５は前記ゲート配線１３の端部に形成されている。又、前記ソースパッド２５は、前記ゲート配線１３が形成されているソース配線２３の端部に形成されている。前記短絡配線４５は全ての前記ゲートパッド１５及び前記ソースパッド２５とに連結されている。

【００１４】しかし、アルミニウムを含む金属物質の表面には、ヒロック(Hillock）と呼ばれる角が形成されて近接する層の間にショートを発生させる。このようなヒロックの形成を防止するためには陽極酸化工程で陽極酸化層１９を形成する。前記短絡配線４５を利用してアルミニウムを含む前記データ電極１１、前記ゲート配線１３、前記ゲートパッド１５及び前記ソースパッド２５を陽極酸化する時、電極として活用する。しかし、前記陽極酸化層１９は、電流をよく通さない性質がある。もし、外部の電気的信号を受け取るゲートパッド１５及びソースパッド２５の表面に陽極酸化層１９が形成されたとすれば、電気的信号が良好に印加されることは出来なくなる。このような問題点を解決するために図２（ｂ）に示すように、ゲートパッド１５及びソースパッド２５の表面には陽極酸化層を形成しないようにする。

【００１５】そして、図２（ｃ）に示すように、前記基板１上に酸化シリコン、又は窒化シリコンを蒸着しパターニングして、ゲート絶縁層１７を形成する。前記ゲート絶縁層１７上に純粋アモルファスシリコンのような真性半導体物質と、不純物が添加されたアモルファスシリコンのような不純物半導体物質を連続に蒸着し、フォトリソグラフィー法でパターニングして半導体層３３及び不純物半導体層３５を形成する。

【００１６】そして、図２（ｄ）に示すように、前記ゲート絶縁層１７をフォトリソグラフィー法でパターニングして、前記ゲートパッド１５部分上に第１ゲートコンタクトホール５１を、前記ソースパッド２５部分上には第１ソースコンタクトホール６１を形成する。前記第１コンタクトホール５１及び６１は、前記ゲート絶縁層１７を貫いて形成されており、陽極酸化層１９が形成されてないゲートパッド１５及びソースパッド２５の部分を露出させる。

【００１７】そして、図３（ａ）に示すように、前記半導体層３３の一方上にクローム、又はクローム合金のような金属物質を蒸着しパターニングして、ソース電極２１を形成し、前記半導体層３３の他方上にドレイン電極３１を形成する。ここで、前記不純物半導体層３５と前記ソース電極２１との間、又前記不純物半導体層３５と前記ドレイン電極３１との間は、オーミック接触をなしている。しかし、前記ソース電極２１と前記ドレイン電極３１との間に前記不純物半導体層３５が連結し形成されていれば、ソース電極２１とドレイン電極３１とは常に導通する状態となり、スイッチとしての役割は出来なくなる。従って、ソース電極２１とドレイン電極３１間にある前記不純物半導体層３５は、例えば、エッチング法のような方法で除去しなければならない。

【００１８】又、図１に示すように、前記ソース電極２１に連結するように前記列配列方向で延長するソース配線２３が図３（ａ）に示すように形成されている。前記ソース配線２３は、前記ゲート配線１３とほぼ直交するように位置されている。そして、前記ソース配線２３の端部には、前記ソースパッド２５を連結させるために前記第１ソースコンタクトホール６１を覆うソースパッド中間電極６５が形成されている。又、前記ゲートパッド１５にも前記第１ゲートパッドコンタクトホール５１を覆うゲートパッド中間電極５５が形成されている。

【００１９】そして、図３（ｂ）に示すように、酸化シリコン又は、窒化シリコン等の絶縁物質を基板全面に蒸

着して保護層３７を形成する。そして、フォトリソグラフィー法でパターニングして前記ゲートパッド１５部分に第２ゲートコンタクトホール５３を、前記ソースパッド２５部分に第２ソースコンタクトホール６３を、そしてドレイン電極３１部分にはドレインコンタクトホール７１を形成する。前記第２ゲートコンタクトホール５３はゲートパッド中間電極５５の一部を、第２ソースコンタクトホール６３は前記ソースパッド中間電極６５の一部を、そして、ドレインコンタクトホール７１はドレイン電極３１の一部を各々露出させる。

【００２０】前記ゲートパッド１５とソースパッド２５を連結する前記短絡配線４５は、最終に完成された前記液晶表示装置では必要ない。従って、前記短絡配線４５において前記ゲートパッド１５と前記ソースパッド２５とを互いに連結する部分を除去し、又は必要によっては短絡配線４５の全部を除去することもできる。この際、エッチング法を用いて除去する（図示せず）。

【００２１】そして、図３（ｃ）に示すように、ITO(Indium Tin Oxide)を蒸着しパターニングして、画素電極４１、ゲートパッド連結端子５７、又ソースパッド連結端子６７を形成する。前記画素電極４１は、前記ドレインコンタクトホール７１を通じて前記ドレイン電極３１に連結されている。前記ゲートパッド連結端子５７は、前記第２ゲートコンタクトホール５３を通じて前記ゲートパッド中間電極５５に連結されている。前記ソースパッド連結端子６７は、前記第２ソースコンタクトホール６３を通じて前記ソースパッド中間電極６５に連結されている。

【００２２】以上の製造工程は、一回の陽極酸化処理工程と少なくとも７～８回のマスク工程が要求される製造工程である。この際、一回のマスク工程だけでも減らすことが出来れば、製造費用及び製造時間が節減され、製造歩留まりが向上される。従って、マスク工程の回数を減らすために陽極酸化工程を使用せずにマスク工程の１～２段階を減らした製造工程が次の如く開発された。

【００２３】図４は、従来の液晶表示装置の一部を示す図であり、図５（ａ）～図６（ｃ）は、パターニング工程を単純化した方法を説明するための図４のIV－IV線に沿った断面図である。

【００２４】図５（ａ）に示すように、透明基板１上にアルミニウム、又はアルミニウム合金のような物質を蒸着して、フォトリソグラフィー法でパターニングして低抵抗ゲート配線１３a及び低抵抗ゲートパッド１５aを形成する。前記低抵抗ゲート配線１３aは、行列配列方式で設計された画素電極４１の間に位置され、前記低抵抗ゲートパッド１５aは、前記低抵抗ゲート配線１３aの端部分に形成されている。

【００２５】前述したようにアルミニウムを使用する層は、表面にヒロックが発生しやすい。従って、クローム(Cr)、モリブデン(Mo)、タンタル(Ta)、又はアンチモン（Sb）のような金属物質を蒸着しパターニングして、前記低抵抗ゲート配線13a上にゲート配線１３と、前記低抵抗ゲートパッド１５ａ上にゲートパッド１５を各々形成する。そして、図５（ｂ）に示すように、前記ゲート配線１３から分岐するゲート電極１１が形成される。前記ゲート電極１１は画素の隅部に形成される（図４を参照されたい）。図５（ｂ）にはクローム、モリブデン、タンタル、又はアンチモンのような金属物質が前記アルミニウム層を完全に覆う形態を示すが、前記アルミニウムの一部だけを覆うように形成することも出来る。

【００２６】図５（ｃ）に示すように、前記基板１上に酸化シリコン、又は窒化シリコンのような絶縁物質を蒸着して絶縁層１７を形成する。前記ゲート絶縁層１７上に純粋アモルファスシリコンのような真性半導体物質を、不純物が添加されたアモルファスシリコンのような不純物半導体物質とを各々連続に蒸着しパターニングして、半導体層３３及び不純物半導体層３５を形成する。

【００２７】図６（ａ）に示すように、クローム、又はクローム合金のような金属物質を蒸着しパターニングしてソース電極２１、ドレイン電極３１、ソース配線２３及びソースパッド２５を形成する。前記ソース電極２１は、前記半導体層３３及び前記不純物半導体層３５を介して前記ゲート電極１１の一方の一部と重畳されるように形成されている。前記ドレイン電極３１は、前記半導体層３３及び不純物半導体層３５を介して前記ゲート電極１１の他方の一部と重畳されるように形成されている。この際、前記ソース電極２１と前記不純物半導体層３５との間、そして、前記ドレイン電極３１と前記不純物半導体層３５との間は、オーミック接触をなしている。又、前記ソース電極２１と前記ドレイン電極３１とをマスクとして前記不純物半導体層３５を選択的にエッチングし、前記ソース電極２１と前記ドレイン電極３１の間に残っている前記不純物半導体層３５を除去する。図４及び図６（ａ）に示すように、前記ソースパッド２３は、列配列方向に配列されて前記ソース電極２１と連結されており、前記ソースパッド２５は前記ソース配線２３の端部に形成されている。

【００２８】図６（ｂ）に示すように、前記ソース電極２１及び前記ドレイン電極３１を有する前記基板１上に酸化シリコン、又は窒化シリコンのような絶縁物質を蒸着して保護層３７を形成する。前記保護層３７及び前記絶縁層１７の一部分をパターニングしてドレインコンタクトホール７１、ゲートパッドコンタクトホール５９、そしてソースパッドコンタクトホール６９を形成する。前記ドレインコンタクトホール７１はドレイン電極３１の一部を露出させ、前記ゲートパッドコンタクトホール５９はゲートパッド１５を露出させ、前記ソースパッドコンタクトホール６９はソースパッド２５を露出させる。

【００２９】図６（ｃ）に示すように、前記保護層３７上にITO(Indium Tin Oxide) のような透明導電物質を蒸着しパターニングして、画素電極４１、ゲートパッド連結端子５７、そしてソースパッド連結端子６７を形成する。前記画素電極４１は、前記ドレインコンタクトホール７１を通じて前記ドレイン電極３１に連結されている。前記ゲートパッド連結端子５７は、前記ゲートパッドコンタクトホール５９を通じて前記ゲートパッド１５に連結されている。又、前記ソースパッド連結端子６７は、前記ソースパッドコンタクトホール６９を通じて前記ソースパッド２５に連結されている。

【００３０】上述の問題点を解決するための陽極酸化する製造方法及び陽極酸化しない製造方法について、図７（ａ）～７（ｂ）及び図８を参照して各々説明する。図７（ａ）～７（ｂ）は、図１のV－V線に沿った断面図であり、図８は、図４のVI－VI線に沿った断面図である。

【００３１】陽極酸化法を使用する製造方法において、陽極酸化層は、比較的に耐化学性が強い物質で構成されるので、アクティブ基板の形成に使用されるエッチャントによく反応しない。図７（ａ）を参照して前記ゲート絶縁層１７の製造工程において、前記半導体層３３、前記不純物半導体層３５及び前記ゲートパッドコンタクトホール５１、前記ゲートパッド１５の外縁部に陽極酸化層１９が形成されて前記ゲートパッド１５を覆う前記ゲート絶縁層１７の製造工程でエッチング液が浸透することを防止する。そして、図７（ｂ）に示すように、ゲートパッド中間電極５５を形成する時、ゲートパッド中間電極５５は、前記ゲートパッド１５の周辺領域を覆い、前記ゲートパッド１５を保護している。しかし、前記陽極酸化法を使用すると、多くのマスク工程が要求されてマスク整列時に誤差が発生しやすい。

【００３２】次に陽極酸化しない製造方法では、陽極酸化する製造方法に比べ使用されるマスクの回数が少ないため、マスクの整列時に発生する誤差が少なくなり、又製造に所要される時間を短縮することができる。しかし、半導体層及び不純物半導体層、又はソース電極及びドレイン電極を形成する時に、前記ゲートパッド１５を覆うゲート絶縁層１７の形成段階を通じてエッチャントが前記ゲートパッド１５をアンダーカットして前記ゲートパッド１５に不良を発生させる（図８）。

【００３３】

【発明が解決しようとする課題】本発明は、エッチャントの浸透からゲートパッドを保護することができる液晶表示装置及びその製造方法を提供することを目的とする。

【００３４】又、本発明は、ゲートパッドをエッチャントの浸透から保護し、同じにゲートパッド部の接触抵抗を減少させることができる液晶表示装置及びそのの製造方法を提供することを他の目的とする。

【問題を解決するための手段】本発明による液晶表示装置の製造方法は、基板上にゲート配線、前記ゲート配線から分岐する少なくとも一つのゲート電極、そして前記ゲート配線の端部に配置されている外周部を有するゲートパッドを形成する段階と；前記基板上に前記ゲート配線、前記ゲート電極、前記ゲートパッドにゲート絶縁層を形成する段階と；そして前記ゲートパッドの外周部の少なくとも一部分を覆う前記ゲート絶縁層上に第１ダミーゲートパッドを形成する段階とを含む。

【００３６】本発明による液晶表示装置は、基板と；前記基板上に形成されているゲート配線と；前記基板上の前記ゲート配線から分岐する少なくとも一つのゲート電極と；前記基板上の前記ゲート配線の端部に配置された外周部を有するゲートパッドと；前記ゲート配線、前記ゲート電極及び前記ゲートパッドの前記基板上に形成されたゲート絶縁層と；前記ゲートパッドの外周部の少なくとも一部分上の前記ゲート絶縁層上に形成された第１ダミーゲートパッドと；から構成される。

【００３７】好ましくは、前記第１ダミーゲートパッドは、半導体物質から成る。

【００３８】好ましくは、前記第１ダミーゲートパッドは、導電物質から成る。

【００３９】好ましくは、前記第１ダミーゲートパッド上に第２ダミーゲートパッドを形成する段階を含む。

【００４０】好ましくは、半導体物質から前記第１ダミーゲートパッドを形成し、導電物質から前記第２ダミーゲートパッドを形成する。

【００４１】好ましくは、前記第１ダミーゲートパッドは、半導体物質をパターニングして形成し、前記ゲート電極上に半導体層を形成する段階を含む。

【００４２】好ましくは、前記第１ダミーゲートパッドをマスクとして前記ゲート絶縁層を選択的にエッチングして前記ゲートパッドコンタクトホールが完全に露出されるように形成する段階を含む。

【００４３】好ましくは、第１導電物質をパターニングして前記第１ダミーゲートパッドに第２ダミーゲートパッドを形成し、前記保護層を選択的にエッチングして前記第２ダミーゲートパッドの一部を露出させ、前記ゲートパッド上に前記ゲートコンタクトホールを形成する段階を含む。

【００４４】好ましくは、前記第１導電物質をパターニングする段階で、前記ゲートパッドコンタクトホールが傾斜された階段形状の構造を有するように前記第２ダミーゲートパッドを形成する。

【００４５】好ましくは、前記傾斜された側壁の構造が階段の形状を有する。

【００４６】好ましくは、前記保護層、前記第１ダミーゲートパッド及び前記ゲート絶縁層に階段形状の前記ゲートパッドコンタクトホールを形成する。

【００４７】好ましくは、前記保護層の選択的エッチン

グ段階と前記ゲート絶縁層の選択的エッチング段階は、連続的に一段階で行われる。

【００４８】好ましくは、半導体物質をパターニングして前記ゲート電極上に半導体層を形成する段階と、前記第１ダミーゲートパッドを形成する段階で前記第１導電物質をパターニングして前記第１ダミーゲートパッドを形成し、前記ゲート電極の一方上の前記半導体層上にドレイン電極を形成し、前記ゲート電極の他方上の前記半導体層上にソース電極を形成する段階を含む。

【００４９】好ましくは、前記基板上に保護層を形成する段階と、前記保護層を選択的にエッチングして前記ドレイン電極を露出させるドレインコンタクトホールを形成し、前記ゲートパッド上に前記ゲート絶縁層の一部と前記第１ダミーゲートパッドの一部を露出させるゲートコンタクトホールの一部を形成する段階と、前記第１ダミーゲートパッドをマスクとして前記ゲート絶縁層を選択的にエッチングして前記ゲートコンタクトホールが完全に露出されるように形成する段階と、第２導電物質をパターニングして前記ゲートパッドコンタクトホールを通じて前記ゲートパッドに接触するゲートパッド連結端子を形成し、前記ドレインコンタクトホールを通じて前記ドレイン電極に接触する画素電極を形成する段階とを含む。

【００５０】好ましくは、前記第１ダミーゲートパッドを形成する段階で、前記第１導電物質をパターニングして前記ソースに連結されるソース配線を形成し、前記ソースパッドを前記ソース配線の端部分に形成し、前記保護層を選択的にエッチングする段階で、前記ソースパッドの一部を露出させるソースコンタクトホールを加えて形成し、前記第２導電物質をパターニングする段階で、前記ソースパッドコンタクトホールを通じて前記ソースパッドに接触されるソースパッド連結端子を形成する。

【００５１】好ましくは、前記ゲート配線を形成する段階で、前記基板上に第１導電物質をパターニングして低抵抗ゲート配線と前記低抵抗ゲート配線の端部分に低抵抗ゲートパッドを形成し、第２導電物質をパターニングして前記低抵抗ゲート配線の少なくとも一部上にゲート配線と、前記ゲート配線で分岐された少なくとも一つのゲート電極と、そして前記ゲート配線の端部分に位置して前記低抵抗ゲートパッドの少なくとも一部を覆うゲートパッドを形成する段階を含む。

【００５２】好ましくは、前記第１導電物質はアルミニウムを含む。

【００５３】好ましくは、前記第２導電物質はクローム、モリブデン、タンタル、そして、アンチモンの中の少なくとも一つを含む。

【００５４】

【発明の実施の形態】本発明では液晶表示装置の製造工程を単純化させるために、陽極酸化法を使用しない。そして、エッチャントの浸透からゲートパッド、又はソースパッドを保護するためには、次の如き方法を用いた。

【００５５】基板上にアルミニウムを含む第１導電物質を蒸着しパターニングして、ゲート配線、ゲート電極及びゲートパッドを形成する。第１絶縁物質を用いて前記ゲート配線、ゲート電極及び前記ゲートパッドを覆うゲート絶縁層を形成する。前記ゲート絶縁層上に真性半導体物質及び不純物が添加された不純物半導体物質を連続蒸着しパターニングして、前記ゲート電極を覆う半導体層及び不純物半導体層を各々形成する。ここで、前記ゲートパッドの外周部、又は端部上にダミー半導体層及びダミー不純物半導体層をダミーゲートパッドで形成する。そして、クロームを含む第２導電物質を用いてソース電極、ドレイン電極、ソース配線及びソースパッドを形成する。この際、前記ダミー半導体ゲートパッドに加えて第２導電層からなるダミーゲートパッドを前記ゲートパッドの端部、又は外周部を囲むように形成される。そして、前記ソース電極、前記ドレイン電極、前記ソース配線、前記ソースパッド及び前記ダミーゲートパッド上に保護層として第２絶縁層を形成する。前記保護層上にドレインコンタクトホール、ゲートパッドコンタクトホール、そしてソースパッドコンタクトホールを形成する。前記保護層上に透明導電物質を蒸着しパターニングして、前記ドレインコンタクトホールを通じて前記ドレイン電極に連結される画素電極を形成し、前記ゲートパッドコンタクトホールを通じて前記ゲートパッドに連結されるゲートパッド連結端子を形成し、前記ソースパッドコンタクトホールを通じて前記ソースパッドに連結されるソースパッド連結端子を形成する。前記ダミー半導体ゲートパッド及び／又は、前記ダミー導電ゲートパッドは、前記ゲートパッドにエッチング保護層としての役割をする。

【００５６】本発明について、以下に具体的に説明する。

【００５７】発明の実施の形態１．図９は、本発明の実施の形態による液晶表示装置を示す平面図であり、図１０（ａ）～図１１（ｃ）は、図９のVIII－VIII線に沿った断面図である。本実施の形態では、半導体物質を用いてダミーゲートパッドを製造する工程について説明する。

【００５８】図１０（ａ）に示すように透明ガラス基板１０１上にアルミニウムを蒸着しフォトリソグラフィ法でパターニングして、低抵抗ゲート配線１１３ａ及び低抵抗ゲートパッド１１５ａを形成する。前記低抵抗ゲート配線１１３ａは後に形成するゲート配線１１３に位置され、前記低抵抗ゲートパッド１１５ａは後に形成されるゲートパッド１１５に位置される。

【００５９】図１０（ｂ）に示すように、前記低抵抗ゲート配線１１３ａ及び前記低抵抗ゲートパッド１１５ａ上にクローム（Ｃｒ）、モリブデン（Ｍｏ）、タンタル（Ｔａ）、又はアンチモン（Ｓｂ）のような金属を蒸着

しパターニングして、ゲート電極１１１、ゲート配線１１３及びゲートパッド１１５を形成する。前記ゲート電極１１１は、対応する画素電極１４１の一隅部に配置されている。前記ゲート配線１１３は、前記複数のゲート電極１１１を連結するために一方向で配置され、前記低抵抗ゲート配線１１３ａを覆っている。この際、前記ゲート配線１１３は、前記低抵抗ゲート配線１１３ａを完全に覆うように形成することもでき、又は前記低抵抗ゲート配線１１３ａを部分的に覆うように形成することも出来る。前記ゲートパッド１１５は、前記ゲート配線１１３の端部に形成され、前記ゲート配線１１３が前記低抵抗ゲート配線１１３ａを覆う方法と類似な方法で前記低抵抗ゲートパッド１１５ａを覆う。

【００６０】図１０（ｃ）に示すように、前記基板１０１上に酸化シリコン、又は窒化シリコンを蒸着してゲート絶縁層１１７を形成する。前記ゲート絶縁層１１７上に純粋アモルファスシリコンのような真性半導体物質と不純物が添加されたアモルファスシリコンのような半導体物質を連続蒸着しパターニングして、前記ゲート電極１１１を覆う半導体層１３３及び不純物半導体層１３５を形成する。又、前記ゲート絶縁層１１７の形成段階において、前記半導体層１３３及び不純物半導体層１３５からなるダミーゲートパッド１１５ｂが前記ゲートパッド１１５の外周部を囲んで形成される。前記ダミーゲートパッド１１５ｂは、前記ゲートパッド１１５に対してエッチング保護層としての役割をする。

【００６１】図１１（ａ）に示すように、前記半導体層１３３及び前記不純物半導体層１３５を含む前記基板上にクローム、又はクローム合金を蒸着しパターニングして、ソース電極１２１、ドレイン電極１３１、ソース配線１２３及びソースパッド１２５を形成する。前記ソース電極１２１は、前記ゲート電極１１１の一方の部分と重畳されるように、前記ドレイン電極１３１は、前記ゲート電極１１１の他方の部分と重畳されるように前記半導体層１３３及び不純物半導体層１３５を介して各々形成されている。前記ソース電極１２１と前記不純物半導体層１３５，そして前記ドレイン電極１３１と前記不純物半導体層１３５は、各々オーミックコンタクトをなしている。前記ソース電極１２１及び前記ドレイン電極１３１をマスクとして前記不純物半導体層１３５を選択的にエッチングして前記ソース電極１２１と前記ドレイン電極１３１の間に存在する前記不純物半導体層１３５を完全に除去する。この際、このエッチング処理方法で前記ゲートパッド１１５の外周部を囲む前記ダミーゲートパッド１１５ｂを形成するために使用された前記不純物半導体物質が除去され、前記ダミーゲートパッド１１５ｂは真性半導体物質からなる前記半導体層１３３だけを有しているようになる。図９に示すように、前記ソース配線１２３は、列方向に延長され、前記ソース電極１２１に連結されている。前記ソースパッド１２５は、前記ソース配線１２３の端部に形成されている。

【００６２】図１１（ｂ）に示すように、前記ソース電極１２１を含む前記基板１０１上に酸化シリコン、又は窒化シリコンのような絶縁物質を蒸着しパターニングして保護層１３７を形成する。前記保護層１３７は、前記ドレイン電極１３１上に形成されているドレインコンタクトホール１７１を含み、前記ゲートパッド１１５上に形成されているゲートパッドコンタクトホール１５９を含む。前記ゲートパッドコンタクトホール１５９を通じて前記ダミーゲートパッド１１５ｂの一部分が露出される。前記ダミーゲートパッド１１５ｂをマスクとして前記ゲートパッド１１５を覆う前記ゲート絶縁層１１７の一部を連続にエッチングし除去し、前記ゲートパッドコンタクトホール１５９を通じて前記ゲートパッド１１５の一部分を露出させる。前記ソースパッド１２５上にはソースパッドコンタクトホール１６９が形成される。

【００６３】窒化シリコンのような同一物質から前記ゲート絶縁層１１７及び前記保護層１３７を形成することによって、前記連続エッチング過程の間にこれらの膜を選択的にエッチングすることが出来、この際、前記ダミーゲートパッド１１５ｂはマスクとしての役割をする。さらに、前記保護層１３７，前記ダミーゲートパッド１１５ｂ及び前記ゲート絶縁層１１７は、前記ゲートパッドコンタクトホール１５９のために段差形状の側壁構造を示す。

【００６４】図１１（ｃ）に示すように、前記保護層１３７上にITO(Indium Tin Oxide)のような透明導電物質を蒸着しパターニングして画素電極１４１、ゲートパッド連結端子１５７及びソースパッド連結端子１６７を形成する。前記画素電極１４１は、前記ドレインコンタクトホール１７１を通じて前記ドレイン電極１３１に連結されている。前記ゲートパッド連結端子１５７は、前記ゲートパッドコンタクトホール１５９を通じて前記ダミーゲートパッド１１５ｂ及び前記ゲートパッド１１５に連結されている。前記ソースパッド連結端子１６７は、前記ソースパッドコンタクトホール１６９を通じて前記ソースパッド１２５に連結されている。

【００６５】本実施の形態において、真性半導体物質を含む前記半導体層１３３は、前記ゲートパッド１１５の外周部を覆うゲート絶縁層１１７の段差された部分を囲む。その結果、前記半導体物質は、ゲート絶縁層１１７の弱い部分を通じてエッチャントが浸透することを防止する。

【００６６】発明の実施の形態２．図１２（ａ）～図１３（ｃ）は、本発明の他の実施の形態による液晶表示装置の製造方法を説明するために図９のIX－IX線に沿った断面図である。本実施の形態では、ソース電極又はドレイン電極を形成するクロームのような金属物質を用いてダミーゲートパッドを形成する工程について説明する。

【００６７】図１２（ａ）に示すように、透明ガラス基

板１０１上にアルミニウムを蒸着し、フォトリソグラフィ法でパターニングして低抵抗ゲート配線１１３ａ及び低抵抗ゲートパッド１１５ａを形成する。前記低抵抗ゲート配線１１３ａは、追後に形成されるゲート配線１１３に位置される。そして、前記低抵抗ゲートパッド１１５ａは、追後に形成されるゲートパッド１１５に位置される。

【００６８】図１２（ｂ）に示すように、前記低抵抗ゲート配線１１３ａ及び前記低抵抗ゲートパッド１１５ａ上にクローム（Ｃｒ）、モリブデン（Ｍｏ）、タンタル（Ｔａ）、又はアンチモン（Ｓｂ）のような金属を蒸着しパターニングして、ゲート電極１１１、ゲート配線１１３及びゲートパッド１１５を形成する。複数の前記ゲート電極１１１は、行配列方式の対応する画素の一隅部に形成されている。前記ゲート配線１１３は、複数の前記ゲート電極１１１に連結されるように垂直方向で延長し、前記低抵抗ゲート配線１１３ａを完全に、又は部分的に覆うように形成されている。前記ゲートパッド１１５は前記ゲート配線１１３ａの端部に形成され、前記ゲート配線１１３が前記低抵抗配線１１３ａを覆う方法と類似な方法で前記低抵抗ゲートパッド１１５ａを覆う。

【００６９】図１２（ｃ）に示すように、前記ゲート電極１１１、前記ゲート配線１１３及び前記ゲートパッド１１５を含む前記基板１０１上に酸化シリコン、又は窒化シリコンを蒸着してゲート絶縁層１１７を形成する。そして、前記ゲート絶縁層１１７上に純粋アモルファスシリコンのような真性半導体物質及びアモルファスシリコンのような不純物が添加された不純物半導体物質の順に蒸着しパターニングして、前記ゲート電極１１１を覆う半導体層１３３及び不純物半導体層１３５を形成する。

【００７０】図１３（ａ）に示すように、前記基板１０１上にクローム、又はクローム合金を蒸着しパターニングして、ソース電極１２１、ドレイン電極１３１、ソース配線１２３、ソースパッド１２５及びダミーゲートパッド１１６ｂを形成する。前記半導体層１３３及び不純物半導体層１３５を介し、前記ソース電極１２１は前記ゲート電極１１１の一方の部分と重畳されており、前記ドレイン電極１３１は前記ゲート電極１１１の他方の部分と重畳されている。ここで、前記ソース電極１２１と前記不純物半導体層１３５、そして前記ドレイン電極１３１と不純物半導体層１３５の間は、オーミックコンタクトをなしている。前記ソース電極１２１及び前記ドレイン電極１３１をマスクとして前記ソース電極１２１と前記ドレイン電極１３１の間に存在する前記不純物半導体層１３５を選択的にエッチングして完全に除去する。図９に示すように前記ソース配線１２３は、一方向で延長され、複数の前記ソース電極１２１に連結されている。前記ソースパッド１２５は、前記ソース配線１２３の端部に形成される。

【００７１】前記ダミーゲートパッド１１６ｂは、前記ゲート絶縁層１１７の段差された部分を覆っており、前記ゲートパッド１１５の外周部を囲んでいる。前記ダミーゲートパッド１１６ｂは、前記ゲートパッド１１５のエッチング保護層としての役割をする。

【００７２】図１３（ｂ）に示すように、前記ソース電極１２１が形成された前記基板１０１上に酸化シリコン、又は窒化シリコンのような絶縁物質を蒸着して保護層１３７を形成する。前記保護層１３７をパターニングして前記ドレイン電極１３１部分にはドレインコンタクトホール１７１を形成し、前記ゲートパッド１１５上には前記ダミーゲートパッド１１６ｂの一定部分を露出させるゲートパッドコンタクトホール１５９を形成する。前記ダミーゲートパッド１１６ｂをマスクとしてエッチングを連続進行して前記ゲートパッド１１５を覆っている前記ゲート絶縁層１１７をエッチングし、前記ゲートコンタクトホール１５９を通じて前記ゲートパッド１１５の一部を露出させる。そして、前記ソースパッド１２５の近傍にソースパッドコンタクトホール１６９が形成される。

【００７３】窒化シリコンのような物質で前記ゲート絶縁層１１７及び前記保護層１３７を形成することによって、連続エッチング工程の間にこのような膜を選択的にエッチングすることができ、この際、前記ダミーゲートパッド１１６ｂはマスクとしての役割をする。又、前記保護層１３７、前記ダミーゲートパッド１１６ｂ及び前記ゲート絶縁層１１７は前記ゲートパッドコンタクトホール１５９のために段差形状の側壁構造をなしている。

【００７４】図１３（ｃ）に示すように、前記保護層１３７上にITO（Ｉｎｄｉｕｍ　Ｔｉｎ　Ｏｘｉｄｅ）のような透明導電物質を蒸着しパターニングし、画素電極１４１、ゲートパッド連結端子１５７及びソースパッド連結端子１６７を形成する。前記画素電極１４１は、前記ドレインコンタクトホール１７１を通じてドレイン電極１３１に連結されている。前記ゲートパッド連結端子１５７は、前記ゲートパッドコンタクトホール１５９を通じて前記ダミーゲートパッド１１６ｂ及び前記ゲートパッド１１５に連結されている。前記ソースパッド連結端子１６７は、前記ソースパッドコンタクトホール１６９を通じて前記ソースパッド１２５に連結されている。

【００７５】本実施の形態では、前記ソース電極１２１を形成するためにクロームを含む金属で前記ゲートパッド１１５を覆うゲート絶縁層１１７の段差された部分を囲む。その結果、前記ゲート絶縁層１１７の弱い部分（段差された部分）を通じてエッチャントが浸透することを防止する。更に、前記ダミーゲートパッド１１６ｂは前記ゲートパッド１１５及び前記ゲートパッド連結端子１５７に電気的に連結されているため、前記ゲートパッド１１５の接触抵抗が低くなる。

【００７６】発明の実施の形態３．又、図１４（ａ）～

図１５（ｃ）は、本発明の他の実施の形態による液晶表示装置の製造方法を説明するための図９のX－X線に沿った断面図である。本実施の形態では、ダミーゲートパッドを半導体物質と、クロームを含むソース電極物質で形成する方法について説明する。

【００７７】図１４（ａ）に示すように、透明ガラス基板１０１上にアルミニウムを蒸着し、フォトリソグラフィ法でパターニングして、低抵抗ゲート配線１１３ａ及び低抵抗ゲートパッド１１５ａを形成する。前記低抵抗ゲート配線１１３ａは、追後形成されるゲート配線１１３に位置されている。そして、前記低抵抗ゲートパッド１１５ａは、追後に形成されるゲートパッド１１５に位置されている。

【００７８】図１４（ｂ）に示すように、前記基板１０１上にクローム（Ｃｒ）、モリブデン（Ｍｏ）、タンタル（Ｔａ）、又はアンチモン（Ｓｂ）のような金属を蒸着しパターニングして、ゲート電極１１１、ゲート配線１１３及びゲートパッド１１５を形成する。図９に示すように、前記ゲート電極１１１は、行列配列の対応する画素の一隅部に形成されている。前記ゲート配線１１３は、前記ゲート電極１１１に連結され水平方向で延長され、前記低抵抗ゲート配線１１３ａを覆っている。前記ゲート配線１１３は、前記低抵抗ゲート配線１１３ａを完全に、又は部分的に覆うことが出来る。前記ゲートパッド１１５は、前記ゲート配線１１３の端部分に形成されており、前記低抵抗ゲートパッド１１５ａは前記低抵抗ゲート配線１１３ａを覆う前記ゲート配線１１３を形成する方法と類似な方法で覆っている。

【００７９】図１４（ｃ）に示すように、前記基板１０１上に酸化シリコン、又は窒化シリコン等を蒸着してゲート絶縁層１１７を形成する。前記ゲート絶縁層１１７上に純粋アモルファスシリコンのような真性半導体物質及び不純物が添加されたアモルファスシリコンのような不純物半導体物質を連続に蒸着しパターニングして、半導体層１３３及び不純物半導体層１３５を各々形成する。そして、第１ダミーゲートパッド１１９ａは、前記ゲートパッド１１５を覆う前記ゲート絶縁層１１７の段差された部分の近くの前記ゲートパッド１１５を囲んで形成される。前記第１ダミーゲートパッド１１９ａは、前記半導体層１３３及び前記不純物半導体層１３５から構成されている。

【００８０】図１５（ａ）に示すように、前記半導体層１３３及び前記不純物半導体層１３５を含む前記基板１０１上にクローム、又はクローム合金を蒸着しパターニングして、ソース電極１２１、ドレイン電極１３１、ソース配線１２３、ソースパッド１２５及び第２ダミーゲートパッド１１９ｂを形成する。前記半導体層１３３と前記不純物半導体層１３５を介して前記ソース電極１２１は前記ゲート電極１１１の一方の一部に重畳されており、前記ドレイン電極１３１は前記ゲート電極１１１の他方の一部に重畳されている。前記ソース電極１２１と前記不純物半導体層１３５との間、又前記ドレイン電極１３１と前記不純物半導体層１３５との間はオーミックコンタクトをなしている。前記ソース電極１２１及び前記ドレイン電極１３１をマスクとして前記ソース電極１２１とドレイン電極１３１との間に存在する前記不純物半導体層１３５の一部分をエッチングして完全に除去する。同時に、前記第２ダミーゲートパッド１１９ｂをマスクとして前記ゲートパッド１１５を囲む第１ダミーゲートパッド１１９ａを形成する不純物半導体物質を除去する。図９に示すように前記ソース配線１２３は、前記ソース電極１２１に列配列方向に連結するために延長されている。前記ソース配線１２３の端部分にソースパッド１２５が形成されている。そして、第２ダミーゲートパッド１１９ｂは、半導体物質からなる前記第１ダミーゲートパッド１１９ａを覆う。その結果、本実施の形態では半導体物質、そしてクロームのような金属からなる２層構造を有するダミーゲートパッドが形成される。前記第１ダミーゲートパッド１１９ａと第２ダミーゲートパッド１１９ｂは、前記ゲートパッド１１５に対してエッチング保護層としての役割をする。

【００８１】図１５（ｂ）に示すように、前記基板１０１上に酸化シリコン、又は窒化シリコンのような絶縁物質を蒸着して保護層１３７を形成し、パターニングして前記ドレイン電極１３１上にドレインコンタクトホール１７１を形成する。前記ゲートバット１１５部分に前記第１ダミーゲートパッド１１９aと前記第２ダミーゲートパッド１１９ｂの一部分を露出させるようにゲートパッドコンタクトホール１５９が形成される。この際、前記第１ダミーゲートパッド１１９aをマスクとして連続エッチングして前記ゲートパッド１１５を覆っている前記ゲート絶縁層１１７をエッチングし、前記ゲートパッドコンタクトホール１５９を通じて前記ゲートパッド１１５を露出させる。前記ソースパッド１２５上にはソースパッドコンタクトホール１６９が形成される窒化シリコンのような同じ物質で前記ゲート絶縁層１１７及び保護層１３７を形成することによって連続エッチング工程の際、このような膜を選択的にエッチングすることが出来、この際、前記第１ダミーゲートパッド１１９ａはマスクとしての役割をする。又、前記保護層１３７、第１ダミーゲートパッド１１９ａ、第２ダミーゲートパッド１１９ｂ、そして前記ゲート絶縁層１１７は前記ゲートパッドコンタクトホール１５９のために階段形状の側壁構造を形成する。

【００８２】図１５（ｃ）に示すように、前記保護層１３７上にITO（Ｉｎｄｉｕｍ　Ｔｉｎ　Ｏｘｉｄｅ）のような透明導電物質を蒸着しパターニングして画素電極１４１、ゲートパッド連結端子１５７、そしてソースパッド連結端子１６７を形成する。前記画素電極１４１は前記ドレインコンタクトホール１７１を通じて前記ドレ

イン電極１３１に連結されている。前記ゲートパッド連結端子１５７は前記ゲートパッドコンタクトホール１５９を通じて前記第１ダミーゲートパッド１１９ａ、前記第２ダミーゲートパッド１１９ｂ、そしてゲートパッド１１５に連結されている。前記ソースパッド連結端子１６７は前記ソースパッドコンタクトホール１６９を通じて前記ソースパッド１２５に連結されている。

【００８３】本実施の形態では、真性半導体物質を含む半導体層１３３物質とクローム金属を含むソース電極物質が前記ゲートパッド１１５を覆う前記ゲート絶縁層１１７上の周囲に形成される。その結果、前記ゲート絶縁層１１７の弱い部分（段差された部分）を通じてエッチャントが浸透することを効果的に防止することができる。

【００８４】以上の実施の形態を通じて前記ゲートパッド１１５の外周部を囲んで覆う前記ダミーゲートパッドを形成するための様々な方法について説明した。図１６（ａ）～図１６（ｃ）は、本発明の実施の形態による前記ダミーゲートパッド１１５ｂの他の形状を示す。

【００８５】図１６（ａ）に示すように、前記ダミーゲートパッド１１５ｂは前記ゲートパッド１１５を完全に囲んで覆っている。図１６（ｂ）や図１６（ｃ）に示すように、前記ダミーゲートパッド１１５ｂは前記ゲートパッド１１５の一部分、又は外周部が覆われていないように前記ゲートパッド１１５とゲート配線１１３の一致する部分の一部だけを覆うことにすることも出来る。このような前記ダミーゲートパッドの様々な構成について、前記ダミーゲートパッド１１５ｂと関連して説明したが、これらの構成は本発明の他の構造で説明される前記ダミーゲートパッドにも適用される。

【００８６】

【発明の効果】本発明は、エッチャントの浸透によってゲートパッドに不良が発生することを防止することができる。本発明において、ゲート絶縁層の形成後、ゲート絶縁層の段差された部分を通じてエッチャントが浸透することを防止するために、少なくとも一つの半導体物質、又は金属からなるダミーゲートパッドが前記ゲートパッドの外周部上に形成されている。

【００８７】本発明の実施の形態１において、ソース電極を形成する間にゲートパッドの外周部、又は外端部を覆うゲート絶縁層上にダミーゲートパッドを形成する。その結果、ゲートパッドを覆うゲート絶縁層の段差された部分を通じてエッチャントが浸透することを防止する。さらに、ダミーゲートパッドが金属物質からなるため、前記ゲートパッドと連結されて、ゲートパッドの接触抵抗を低くすることが出来る。従って、ゲートパッドを保護し、そしてゲートパッド及び、配線の抵抗を低くして水平輝度不良も防止する。

【００８８】本発明の実施の形態２において、半導体物質で第１ダミーゲートパッドを形成し、ソース電極の形成に使用する同じ金属物質で第１ダミーゲートパッドを覆う第２ダミーゲートパッドを形成することもある。この場合は、異なる製造工程の間にダミーゲートパッドが形成されるため、他の製造段階で発生するエッチャントの浸透を防止する。又、金属物質を含む第２ダミーゲートパッドによってゲートパッド部分で接触抵抗を低くして輝度不良防止する。さらに、第１ダミーゲートパッドと、第２ダミーゲートパッドとが異なる大きさで形成することによってゲートコンタクトホールで緩慢な傾斜を形成してITOで形成するゲートパッド連結端子の部分浸蝕も防止する。

【図面の簡単な説明】

【図１】　陽極酸化によって形成された従来の液晶表示装置を示す断面図。

【図２】　陽極酸化を使用した従来の液晶表示装置の製造方法を説明するための図１のII－II線に沿った断面図。

【図３】　陽極酸化を使用した従来の液晶表示装置の製造方法を説明するための図１のII－II線に沿った断面図（続き）。

【図４】　陽極酸化を使用せずに形成された従来の液晶表示装置を示す断面図。

【図５】　陽極酸化を使用せずに従来の液晶表示装置の製造方法を説明するための図４のIV－IV線に沿った断面図。

【図６】　陽極酸化を使用せずに従来の液晶表示装置の製造方法を説明するための図４のIV－IV線に沿った断面図（続き）。

【図７】　ゲート絶縁層及びその段差された部分を通したエッチャントの浸透を説明するための図１のV－V線に沿った断面図。

【図８】　ゲート絶縁層及びその段差された部分を通したエッチャントの浸透を説明するための図４のVI－VI線に沿った断面図。

【図９】　本発明の実施の形態による液晶表示装置を示す平面図。

【図１０】　本発明の実施の形態１による液晶表示装置の製造方法を示すための図９のVIII－VIII線に沿った断面図。

【図１１】　本発明の実施の形態１による液晶表示装置の製造方法を示すための図９のVIII－VIII線に沿った断面図（続き）。

【図１２】　本発明の他の実施の形態による液晶表示装置の製造方法を示すための図９のIX－IX線に沿った断面図。

【図１３】　本発明の他の実施の形態による液晶表示装置の製造方法を示すための図９のIX－IX線に沿った断面図（続き）。

【図１４】　本発明の他の実施の形態による液晶表示装置の製造方法を示すための図９のX－X線に沿った断面

図。

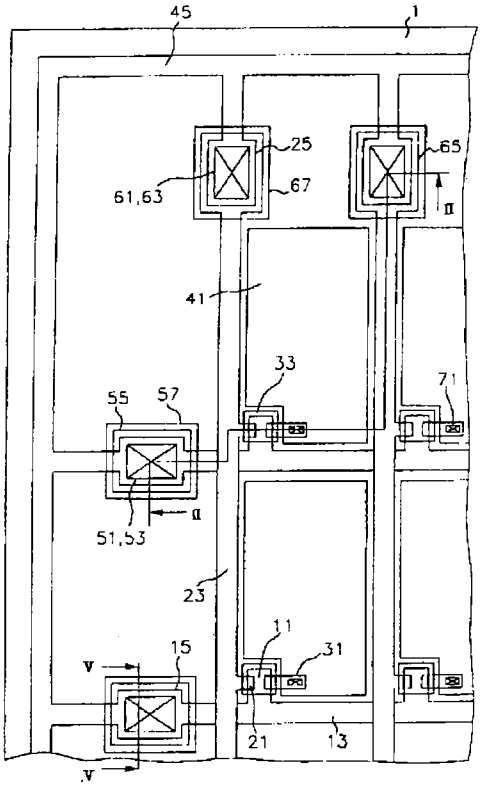
【図１５】　本発明の他の実施の形態による液晶表示装置の製造方法を示すための図９のX－X線に沿った断面図（続き）。

【図１６】　本発明による液晶表示装置において、様々なゲートパッド部を示す図。

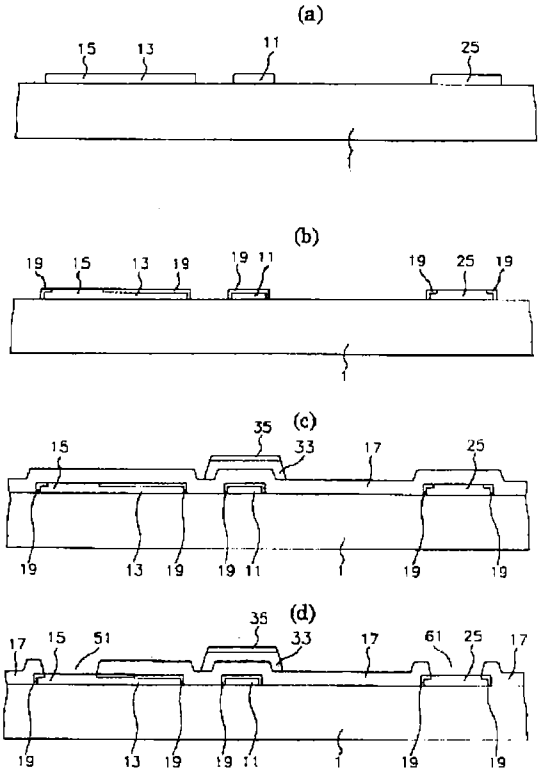
【符号の簡単な説明】

１、１０１	基板
１１、１１１	ゲート電極
１３、１１３	ゲート配線
１５、１１５	ゲートパッド
１３ａ、１１３ａ	低抵抗ゲート配線
１５ａ、１１５ａ	低抵抗ゲートパッド
１１５ｂ	ダミーゲートパッド
１７、１１７	ゲート絶縁層
１９	陽極酸化層
１１９ａ	第１ダミーゲートパッド
１１９ｂ	第２ダミーゲートパッド
２１、１２１	ソース電極
＊２３、１２３	ソース配線
２５、１２５	ソースパッド
３１、１３１	ドレイン電極
３３、１３３	半導体層
３５、１３５	不純物半導体層
３７、１３７	保護層
４１、１４１	画素電極
４５	短絡配線
５１	第１ゲートパッドコンタクトホール
５３	第２ゲートコンタクトホール
５５	ゲートパッド中間電極
５７、１５７	ゲートパッド連結端子
５９、１５９	ゲートパッドコンタクトホール
６１	第１ソースコンタクトホール
６３	第２ソースコンタクトホール
６５	ソースパッド中間電極
６７、１６７	ソースパッド連結端子
６９、１６９	ソースパッドコンタクトホール
＊７１、１７１	ドレインコンタクトホール

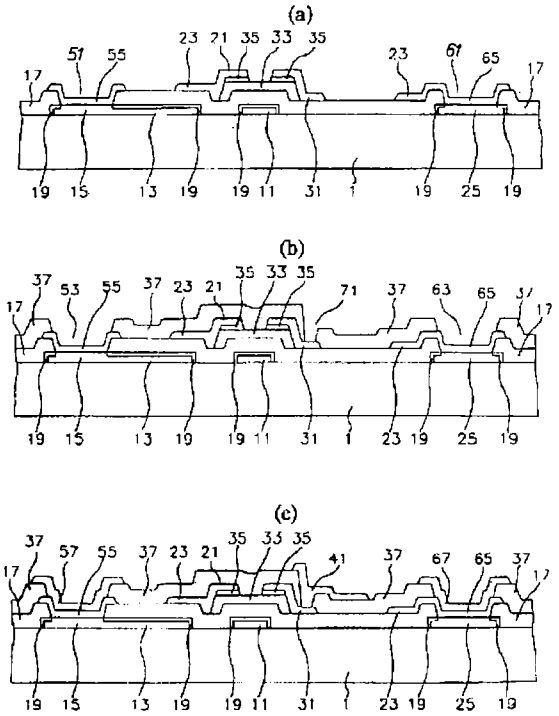
【図１】



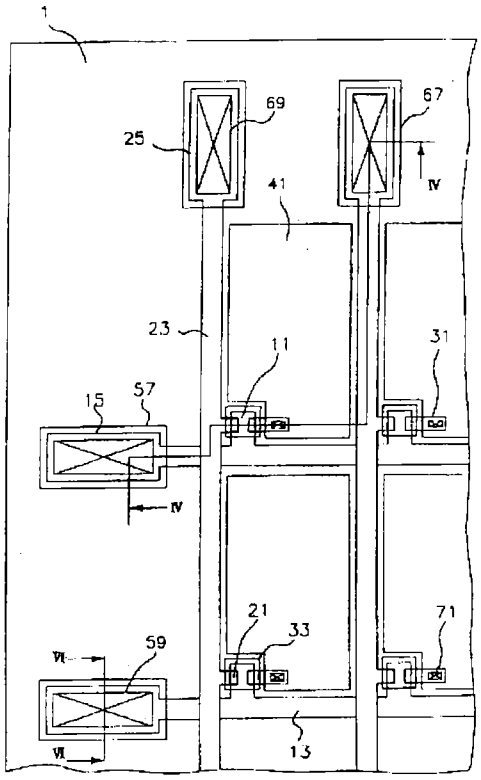
【図２】



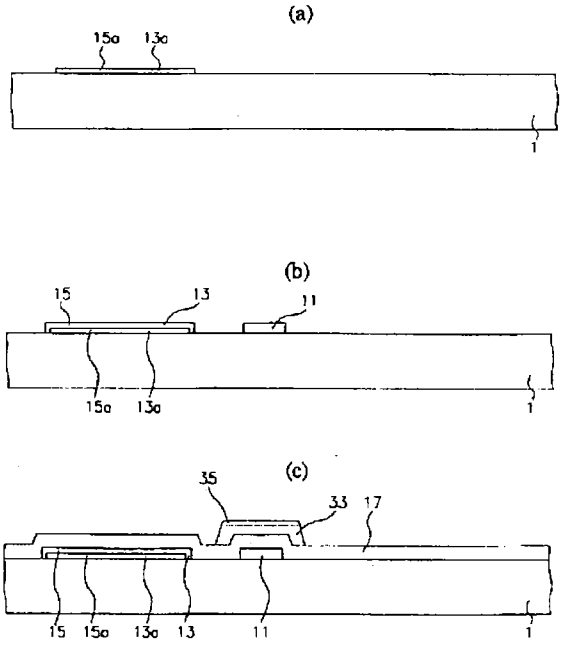
【図３】



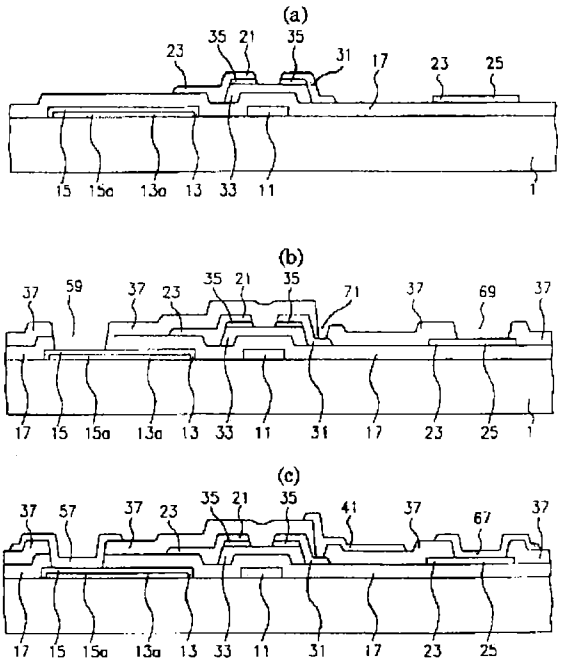
【図４】



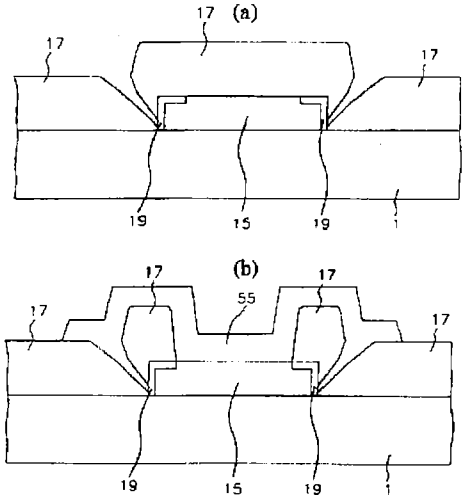
【図５】



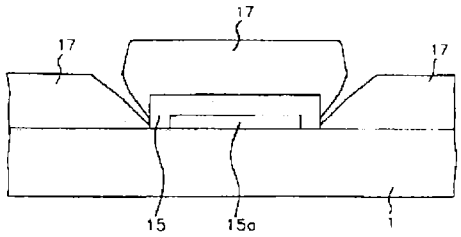
【図６】



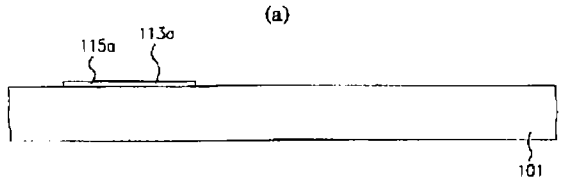
【図７】


(a)
17
19
15
1
(b)
55

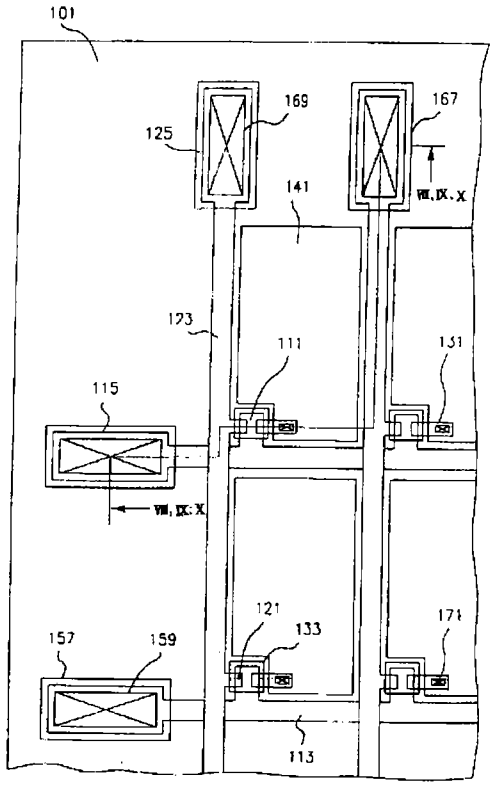
【図８】


17
15
15a
1

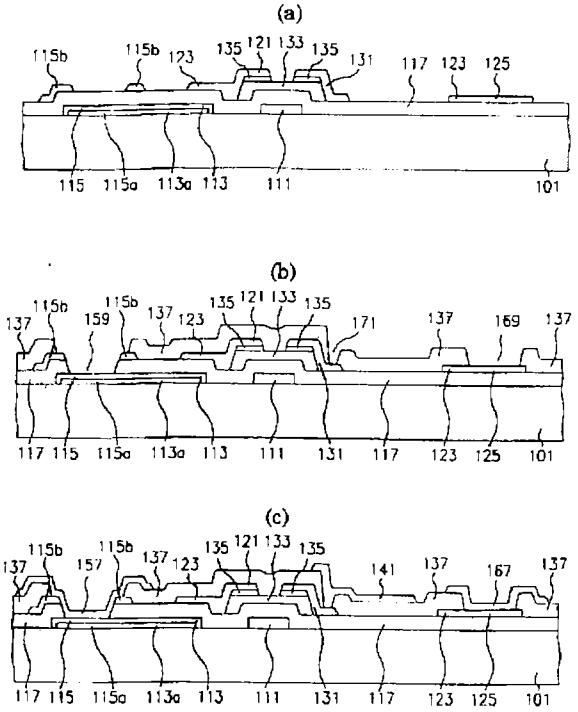
【図１０】


(a)
115a
113a
101
(b)
115
113
111
(c)
115b (133)
135
133
117

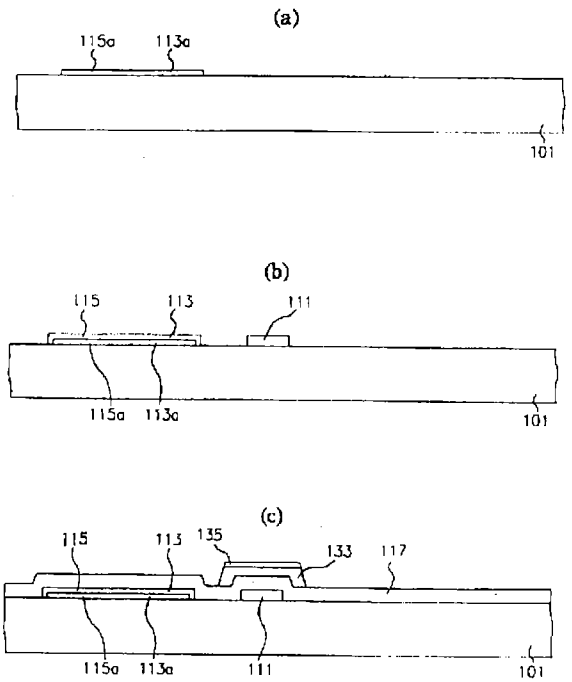
【図９】


101
125
169
167
141
123
111
131
115
121
133
171
157
159
113

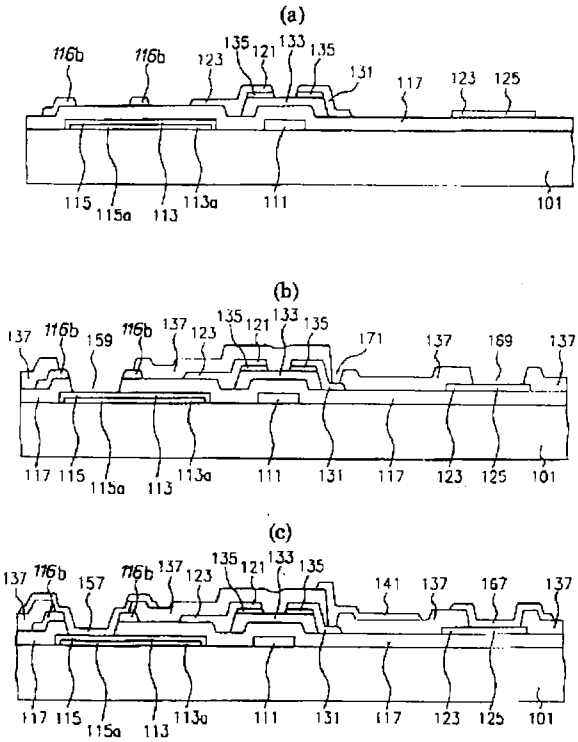
【図１１】



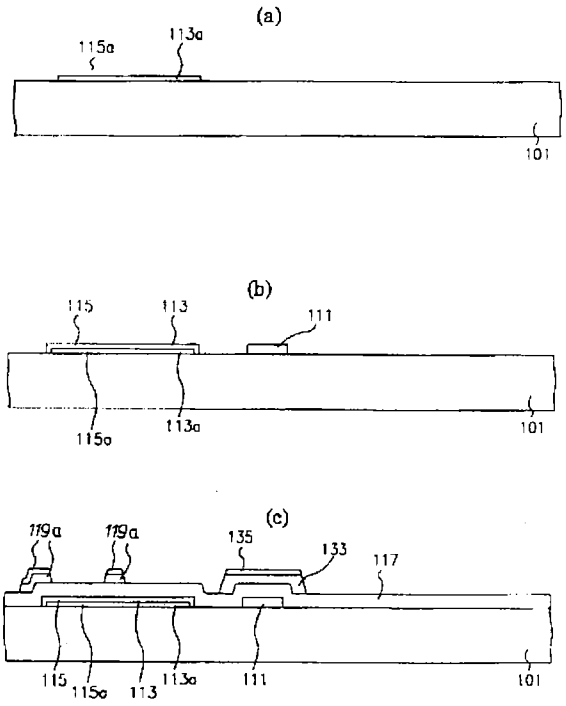
【図１２】



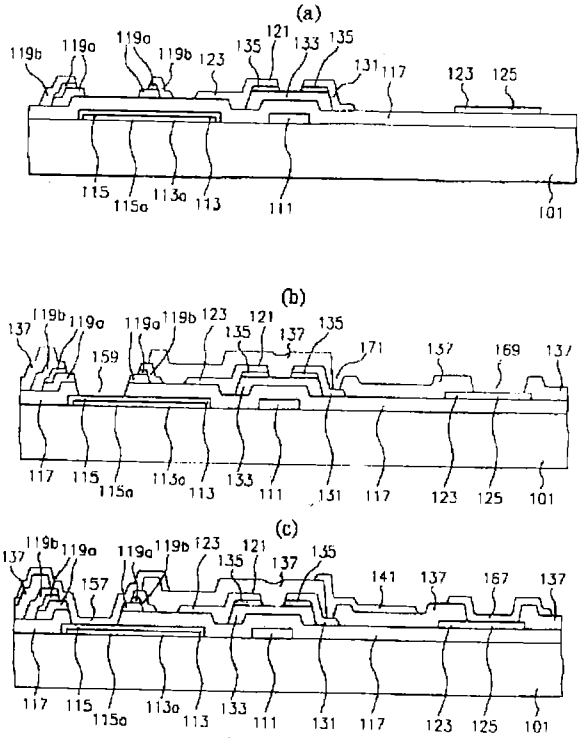
【図１３】



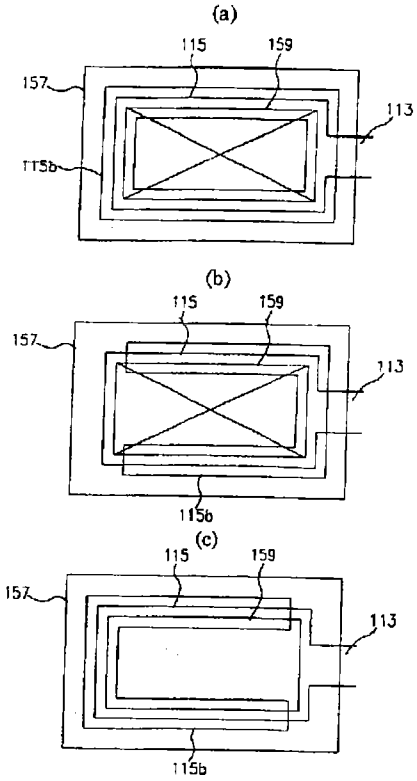
【図１４】



【図１５】



【図１６】



フロントページの続き

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究団地ＬＣＤ研究所内

Electronic Acknowledgement Receipt

EFS ID:	7992631
Application Number:	90009697
International Application Number:	
Confirmation Number:	5947
Title of Invention:	ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE
First Named Inventor/Applicant Name:	6689629
Customer Number:	24504
Filer:	Daniel R. McClure/Gina Silverio
Filer Authorized By:	Daniel R. McClure
Attorney Docket Number:	7773.0084
Receipt Date:	12-JUL-2010
Filing Date:	16-MAR-2010
Time Stamp:	12:52:42
Application Type:	Reexam (Third Party)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	01186168.PDF	111394 812163185 1f648102f2202a93b2d3454296a627e	no	3

Warnings:	
Information:	

2	Information Disclosure Statement (IDS) Filed (SB/08)	01185961.PDF	892679 5c4771cf7a0f6132f725174e157600bbeaf5014d	no	5
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
3	Foreign Reference	01186167.PDF	946286 540cbbd6df8ff2d3e85b5c0b8c6d75af2a3043f8	no	19
Warnings:					
Information:					
4	Foreign Reference	01186165.PDF	500670 15170ca3516a2a39f4593d1c6b1b8f3f74d1e58c	no	9
Warnings:					
Information:					
5	Foreign Reference	01186166.PDF	1090702 5323657c8475fd5b3a0456709bf3adb769bf4384	no	22
Warnings:					
Information:					
6	NPL Documents	01186169.PDF	2137014 e6ac65fc2f79add7cdef9a082ed1b7066c5e746f	no	45
Warnings:					
Information:					
7	Foreign Reference	01186173.PDF	615527 5637648ffb7c3582e8e38e277f6c5a7f296747a6	no	9
Warnings:					
Information:					
8	Foreign Reference	01186174.PDF	172822 ad702ceac6e047c822d2ebb1ca6fff6f348affa1	no	5
Warnings:					
Information:					
9	Foreign Reference	01186177.PDF	994870 02828b9b9df66032be18eec7adc76aec1e9a5088	no	14
Warnings:					
Information:					

10	Foreign Reference	01186178.PDF	406148 2046ad9af6cf3f25dd655607a3e5ead2689d696c	no	6
Warnings:					
Information:					
11	Foreign Reference	01186179.PDF	1640007 ed2caa003c3a7d10dcede92ed1cf32ef820a097c	no	20
Warnings:					
Information:					
12	Foreign Reference	01186181.PDF	1283908 d56ab82b38113ce202da1187ac8cf7b1465336b5	no	17
Warnings:					
Information:					
		Total Files Size (in bytes):	10792027		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re *Inter Partes* Reexamination Application of:

U.S. Patent No. 6,689,629

Confirmation No.: 5947

Group Art Unit: 3992

Control No.: 90/009,697

Examiner:

Filed: March 16, 2010

TKHR Ref: 250129-1080

For: Array Substrate for Display, Method of Manufacturing Array Substrate for Display and Display Device Using the Array Substrate

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

This information disclosure statement is filed in accordance with 37 C.F.R. §§ 1.56, 1.97, and 1.98, and specifically:

☒ under 37 CFR 1.97(b), or
(within Three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)

☐ under 37 CFR 1.97(c) together with either a:
- ☐ Statement Under 37 C.F.R. 1.97(e), or
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(After the CFR 1.97(b) time period, but before the final office action or notice of allowance, whichever occurs first)

☐ under 37 CFR 1.97(d) together with a:
- ☐ Statement under 37 CFR 1.97(e), and
- ☐ a $180.00 petition fee set forth in 37 CFR 1.17(p).

(Filed after final office action or notice of allowance, whichever occurs first, but before payment of the issue fee)

☐ Enclosed is a check in the amount of $.

☐ Payment by credit card.

☐ Please charge $ to deposit account .

☒ At any time during the pendency of this application, please charge any fees required to Deposit Account pursuant to 37 CFR 1.25. The Commissioner is hereby requested to credit any overpayment to Deposit Account No. 20-0778.

☒ Applicant(s) submit herewith *Form PTO SB/08A-08B-08a - Information Disclosure Statement by Applicant* together with copies (where required) of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may or may not be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56. As required by 37 C.F.R. §1.98(a), a legible copy of each document is provided.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form SB/08A-08B-08a, as presently understood by the individual(s) designated in 37 CFR 1.56(c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on the form PTO SB/08A-08B-08a and is enclosed herewith.

The following rights are reserved by the Applicant(s): the right to establish the patentability of the claimed invention over any of the listed documents should they be applied as reference, and/or the right to prove that some of these documents may not be prior art, and/or the right to prove that some of these documents may not be enabling for the teachings they purport to offer.

This statement should not be construed as a representation that an exhaustive search has been made, or that information more material to the examination of the present application does not exist. Any statements or identifications regarding the relevance of any portion(s) of cited references should not be construed as a representation that the most relevant portion(s) have been identified, and the absence of such statements or identifications should not be construed as representations that there are no relevant portion(s). The Examiner is specifically requested not to rely solely on the materials submitted herewith. The Examiner is requested to conduct an independent and thorough review of the documents, and to form independent opinions as to their significance.

The references cited in the accompanying SB08A became known to the Patent Owner (either through citation in corresponding non-U.S. applications or otherwise) after the issuance of the underlying patent. It is requested that the information disclosed herein be made of record in this application and that the Examiner initial and return a copy of the enclosed PTO SB/08A-08B-08a to indicate the documents have been considered.

Respectfully Submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

/Daniel R. McClure/

By: _____

Daniel R. McClure, Reg. No. 38,962

600 Galleria Parkway, S.E.
Suite 1500
Atlanta, Georgia 30339-5994
Phone: (770) 933-9500
Fax: (770) 951-0933

CERTIFICATE OF SERVICE

I hereby certify that the foregoing **INFORMATION DISCLOSURE STATEMENT** was served upon the following:

Song K. Jung
McKenna Long & Aldridge LLP
1900 K St., N.W.
Washington, DC 20006

by depositing a true and correct copy of the same with the U.S. Postal Service (via First Class mail service) with full postage prepaid.

July 12, 2010
Date

/Daniel R. McClure/
Daniel R. McClure, Reg. No. 38,962

Litigation Search Report CRU 3999

Reexam Control No. 90/009,697

TO: TUAN H. NGUYEN	From: MANUEL SALDANA
Location: CRU	Location: CRU 3999
Art Unit: 3992	MDW 7C55
Date: 12/28/10	Phone: (571) 272-7740
	MANUEL.SALDANA@uspto.gov

Search Notes

Litigation was found for US Patent Number: **6,689,629**
DOCKET 1:07CV357 (NOT CLOSED).
DOCKET 1:07CV137 (CLOSED 05/30/07).

1) I performed a KeyCite Search in Westlaw, which retrieves all history on the patent including any litigation.

2) I performed a search on the patent in Lexis CourtLink for any open dockets or closed cases.

3) I performed a search in Lexis in the Federal Courts and Administrative Materials databases for any cases found.

4) I performed a search in Lexis in the IP Journal and Periodicals database for any articles on the patent.

5) I performed a search in Lexis in the news databases for any articles about the patent or any articles about litigation on this patent.

Date of Printing: Dec 28, 2010

KEYCITE

H US PAT 6689629 ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE, Assignee: International Business Machines (Feb 10, 2004)

History

Direct History

=> 1 **ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE,** US PAT 6689629, 2004 WL 247094 (U.S. PTO Utility Feb 10, 2004) (NO. 10/068500)

Construed and Ruled Infringed by

H 2 LG Display Co., Ltd. v. AU Optronics Corp., 686 F.Supp.2d 429, 2010 Markman 545921 (D.Del. Feb 16, 2010) (NO. CIV.A. 06-726-JJF, CIV.A. 07-357-JJF) (Markman Order Version)

AND Ruled Infringed by

H 3 LG Display Co., Ltd. v. AU Optronics Corp., 722 F.Supp.2d 466 (D.Del. Jul 08, 2010) (NO. CIV.A. 06-726-JJF, CIV.A. 07-357-JJF)

H 4 LIQUID-CRYSTAL DISPLAY, LIQUID-CRYSTAL CONTROL CIRCUIT, FLICKER INHIBITION METHOD, AND LIQUID-CRYSTAL DRIVING METHOD, US PAT 6778160, 2004 WL 1839025 (U.S. PTO Utility Aug 17, 2004) (NO. 09/760131)

Construed and Ruled Infringed by

H 5 LG Display Co., Ltd. v. AU Optronics Corp., 686 F.Supp.2d 429, 2010 Markman 545921 (D.Del. Feb 16, 2010) (NO. CIV.A. 06-726-JJF, CIV.A. 07-357-JJF) (Markman Order Version)

AND Ruled Infringed by

H 6 LG Display Co., Ltd. v. AU Optronics Corp., 722 F.Supp.2d 466 (D.Del. Jul 08, 2010) (NO. CIV.A. 06-726-JJF, CIV.A. 07-357-JJF)

H 7 SIGNAL TRANSMISSION DEVICE HAVING FLEXIBLE PRINTED CIRCUIT BOARDS, US PAT 7090506, 2006 WL 2358291 (U.S. PTO Utility Aug 15, 2006) (NO. 10/921462)

Construed and Ruled Infringed by

H 8 LG Display Co., Ltd. v. AU Optronics Corp., 686 F.Supp.2d 429, 2010 Markman 545921 (D.Del. Feb 16, 2010) (NO. CIV.A. 06-726-JJF, CIV.A. 07-357-JJF) (Markman Order Version)

AND Ruled Infringed by

H 9 LG Display Co., Ltd. v. AU Optronics Corp., 722 F.Supp.2d 466 (D.Del. Jul 08, 2010) (NO. CIV.A. 06-726-JJF, CIV.A. 07-357-JJF)

10 BACKLIGHT UNIT AND LIQUID CRYSTAL DISPLAY UTILIZING THE SAME, US PAT 7125157, 2006 WL 3011617 (U.S. PTO Utility Oct 24, 2006) (NO. 10/902914)

Construed and Ruled Infringed by

11 LG Display Co., Ltd. v. AU Optronics Corp., 686 F.Supp.2d 429, 2010 Markman 545921 (D.Del. Feb 16, 2010) (NO. CIV.A. 06-726-JJF, CIV.A. 07-357-JJF) (Markman Order Version)

AND Ruled Infringed by

12 LG Display Co., Ltd. v. AU Optronics Corp., 722 F.Supp.2d 466 (D.Del. Jul 08, 2010) (NO. CIV.A. 06-726-JJF, CIV.A. 07-357-JJF)

Related References

13 ELECTRICAL BATTERY, US PAT 600457, 1898 WL 29085 (U.S. PTO Utility Mar 08, 1898) (NO. 609969)

Construed by

14 LG Philips LCD Co., Ltd. v. Tatung Co. of America, 2005 WL 6219893, 2005 Markman 6219893 (C.D.Cal. May 05, 2005) (NO. CV 02-6775 CBM(JTLX))

15 PROCESS FOR PRODUCING THIN-FILM TRANSISTOR, US PAT 4624737, 1986 WL 520398 (U.S. PTO Utility Nov 25, 1986) (NO. 06/743092)

Construed by

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92 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants. CHI MEI OPTOELECTRONICS CORPORATION and Chi Mei Optoelectronics USA, Inc., Plaintiffs, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 3242282 (Trial Motion, Memorandum and Affidavit) (D.Del. May 8, 2009) **Chi Mei Optoelectronics Corporation's Memorandum of Points and Authorities in Support of Its Motion for Partial Summary Judgment Finding Non-Infringement of U.S. Patent No. 7,218,374 By Certain Cmo Pr** (NO. 106CV00726)

93 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3242283 (Trial Motion, Memorandum and Affidavit) (D.Del. May 8, 2009) **AUO's Opening Brief in Support of Its Motion for Summary Judgment of Invalidity of All of Claims of LGD's "737 Patent** (NO. 106CV00726)

94 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3242284 (Trial Motion, Memorandum and Affidavit) (D.Del. May 12, 2009) **Plaintiff LG Display Company Ltd.'s Reply Breif in Support of Its Motion to Strike or Preclude Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA, Inc. From Asserting an Advice of Cou** (NO. 106CV00726)

95 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3242285 (Trial Motion, Memorandum and Affidavit) (D.Del. May 12, 2009) **LG Display Co., Ltd.'s Reply Brief in Support of Its Motion to Compel Auo to Provide Knowledgeable Witnesses on Key Inducement and Damages Deposition Topics** (NO. 106CV00726)

96 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORAION, et al., Defendants., 2009 WL 3242286 (Trial Motion, Memorandum and Affidavit) (D.Del. May 13, 2009) **LG Display Co., Ltd.'s Opposition to AUO's Motion to Supplement Briefing of Its Motion to Preclude LG Display's Reliance On Invalidating Prior Art** (NO. 106CV00726)

97 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; CHI, MEI Optoelectronics Corporation; and CHI MEI Optoelectronics USA, Inc., Defendants., 2009 WL 3242287 (Trial Motion, Memorandum and Affidavit) (D.Del. May 21, 2009) **AUO's Opening Brief in Support of its Motion for Summary Judgment of Invalidity on all Claims of LGD's "274, "321 and "489 Patents** (NO. 106CV00726)

98 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3242288 (Trial Motion, Memorandum and Affidavit) (D.Del. May 21, 2009) **Au Optronics' Motion in Limine No. 1 to Exclude any Opinion Testimony by LG Display's Technical Experts Regarding any Devices or Processess that they have not Analyzed** (NO. 106CV00726)

99 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245830 (Trial Motion, Memorandum and Affidavit) (D.Del. May 21, 2009) **Au Optronicss' Motion in Limine No.2 to Preclude Any Reference to the Prior Cpt Litigations** (NO. 106CV00726)

100 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245831 (Trial Motion, Memorandum and Affidavit) (D.Del. May 21, 2009) **Au Optronics' Motion in Limine No.3 to Preclude Any Testimony from the Prior CPT Litigations, Including Reliance by Experts on the Prior Testimony of Expert Michael Keeley in the California CPT Litiga** (NO. 106CV00726)

101 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245832 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **AU Optronics' Motion in Limine No. 4 to Preclude Any Testimony from the Prior CPT Litigations, Including Reliance By Experts on the Prior Testimony of Dr. Holmberg, Mr. Castleberry, and Mr. Ho Lee in** (NO. 106CV00726)

102 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Cor-

poration America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245833 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **Au Optronics' Motion in Limine No.5 to Preclude Lg Display from Introducing Any Evidence Regarding Yield Percentage and to Preclude Mr. Cobb from Offering Any Opinions Based Upon Yield Improvements** (NO. 106CV00726)

103 LG DISPLAY COMPANY, LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245834 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **LG Display Co., Ltd.'s Motion in Limine No. 1 to Preclude Joyce Pan and James Chen from Testifying at Trial because They Were not Timely Identified by AU Optronics Corporation** (NO. 106CV00726)

104 LG DISPLAY COMPANY, LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245835 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **Lg Display Co., Ltd.'s Motion in Limine No. 2 to Preclude Auo's Experts from Asserting Prior Art Against Lg Display's Patents that They Did not Address in Their Expert Reports** (NO. 106CV00726)

105 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORP., et al., Defendants., 2009 WL 3245836 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **LG Display Co., Ltd's Motion Inlimine No. 4 to Preclude the Introduction of Testimony from the Depostion of Third Party Catalyst Sales, Inc. Prior to Appearance At the Deposition By All Counsel** (NO. 106CV00726)

106 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245837 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **Lg Display Co., Ltd.'s Motion in Limine No. 3 to Preclude Auo from Offering Evidence Regarding Advice of Counsel** (NO. 106CV00726)

107 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245838 (Trial Motion, Memorandum and Affidavit) (D.Del. May 28, 2009) **Lg Display Co., Ltd.'s Opposition to Auo's ""Addendum" to Its Motion Limine No. 7** (NO. 106CV00726)

108 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245839 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 5, 2009) **Auo's Opposition to Lgd's Motion in Limine to Preclude Auo from Introducing Live Testimony from Mr. Kuang-Tao (""Surf") Sung or Other Evidence Allegedly Showing Dates of Conception and Reduction to P** (NO. 106CV00726)

109 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245840 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 5, 2009) **Addendum to AUO's Motion in Limine No. 7 (D.I. 1266), Regarding Additional Untimely Prior Art Documents (LGD 2170033-2170457, Produced by LGD on May 26, 2009)** (NO. 106CV00726)

110 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245841 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 8,

2009) **Au Optronics' Response to Lg Display Co. Ltd.'s Motion in Limine No.5 to Preclude Introduction of Evidence or Opinion Testimony Concerning Electro-Static Discharge Repairs and Repair Costs** (NO. 106CV00726)

111 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245842 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 8, 2009) **Au Optronics' Response to Lg Display Co. Ltd.'s Motion in Limine No. 3** (NO. 106CV00726)

112 LG DISPLAY COMPANY, LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245843 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Motion in Limine No.5 to Preclude Auo from Introducing Evidence or Opinion Testimony Concerning Purported Electro-Static Discharge Repairs and Repair Costs** (NO. 106CV00726)

113 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245844 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Memorandum in Opposition to Auo's Motion in Limine No. 5** (NO. 106CV00726)

114 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORP., et al., Defendants., 2009 WL 3245845 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **Lg Display Co., Ltd.'s Opposition to Au Optronics Corporation's Motion in Limine No.6 to Preclude Lgd from Relying On Certain Defenses and Evidence that Lgd Failed to Disclose During Discovery** (NO. 106CV00726)

115 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245846 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Memorandum in Opposition to Auo's Motion in Limine No. 4 to Preclude Any Testimony from the Prior CPT Litigations, Including Reliance By Experts On the Prior Testimony of Dr. Ho** (NO. 106CV00726)

116 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245847 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Memorandum in Opposition to Auo's Motion in Limine No. 1** (NO. 106CV00726)

117 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245848 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **Lg Display Co., Ltd.'s Memorandum in Opposition to Auo's Motion in Limine No. 2 to Preclude Any Reference to the Prior Cpt Litigations** (NO. 106CV00726)

118 LG DISPLAY COMPANY, LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245849 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Motion in Limine to Preclude AU Optronics Corporation from Introducing Live Testimony from Mr. Kuang-Tao (""Surf") Sung or Other Evidence Allegedly Showing Dates of Conception** (NO. 106CV00726)

119 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2010 WL 2833076 (Trial Motion, Memorandum and Affidavit) (D.Del. May 10, 2010) **Memorandum of Law in Support of Anvik Corporation's Motion for Limited Intervention to Obtain Cop-**

ies of Evidence (NO. 106CV00726)

120 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2010 WL 2833077 (Trial Motion, Memorandum and Affidavit) (D.Del. May 27, 2010) **LG Display Co., Ltd.'s Opposition to Anvik Corporation's Motion for Limited Intervention to Obtain Copies of Evidence** (NO. 106CV00726)

121 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2010 WL 2833078 (Trial Motion, Memorandum and Affidavit) (D.Del. May 27, 2010) **Auo's Answering Brief in Opposition to Anvik Corporation's Motion for Limited Intervention to Obtain Copies of Evidence** (NO. 106CV00726)

122 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2010 WL 2833079 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 7, 2010) **Reply Memorandum of Law in Support of Anvik Corporation's Motion for Limited Intervention to Obtain Copies of Evidence** (NO. 106CV00726)

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123 John D. Villasenor, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6877461 (Court-filed Expert Resume) (D.Del. Aug. 12, 2008) **Expert Resume of John D. V** (NO. 106CV00726)

124 Pochi Yeh, curriculum vitae filed in LG. Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6889166 (Court-filed Expert Resume) (D.Del. Aug. 12, 2008) **Expert Resume of Pochi Yeh** (NO. 106CV00726)

125 Miltiadis K. Hatalis, curriculum vitae filed in LG,Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6889167 (Court-filed Expert Resume) (D.Del. Aug. 12, 2008) **Expert Resume of Miltiadis K. Hatalis** (NO. 106CV00726)

126 David A. Eccles, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6877462 (Court-filed Expert Resume) (D.Del. Sep. 4, 2008) **Expert Resume of David A. Eccles** (NO. 106CV00726)

127 Allan R. Kmetz, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6877463 (Court-filed Expert Resume) (D.Del. Sep. 4, 2008) **Expert Resume of Allan R. Kmetz** (NO. 106CV00726)

128 George M. Pharr, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6882352 (Court-filed Expert Resume) (D.Del. Sep. 4, 2008) **Expert Resume of George M. Pharr** (NO. 106CV00726)

D.Del. Trial Filings

129 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159025 (Trial Filing) (D.Del. Jul. 29, 2008) **Claim Construction Chart** (NO. 06CV00726)

130 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159026 (Trial Filing) (D.Del. Jul. 29, 2008) **Claim Construction Chart** (NO. 06CV00726)

131 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159027 (Trial Filing) (D.Del. Jul. 29, 2008) **Claim Construction Chart** (NO. 06CV00726)

132 LG PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008

WL 6159028 (Trial Filing) (D.Del. Jul. 29, 2008) **Claim Construction Chart** (NO. 06CV00726)

133 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159029 (Trial Filing) (D.Del. Jul. 29, 2008) **Claim Construction Chart** (NO. 06CV00726)

134 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159030 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

135 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159031 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

136 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159032 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

137 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159033 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

138 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159034 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

139 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159035 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

140 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159036 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

141 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159037 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

142 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159038 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

143 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159039 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

144 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159040 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

145 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159041 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

146 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159042 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

147 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159043 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

148 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159044 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

149 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159045 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

150 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159046 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit B LG Display USP 5,019,002** (NO. 06CV00726)

151 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159047 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit C LG Display USP 5,825,449** (NO. 06CV00726)

152 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159048 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit D LG Display USP 6,664,569** (NO. 06CV00726)

153 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159049 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit E LG Display USP 6,803,984** (NO. 06CV00726)

154 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159050 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit F LG Display USP 5,905,274** (NO. 06CV00726)

155 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159051 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit G LG Display USP 6,815,321** (NO. 06CV00726)

156 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159052 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit H LG Display USP 7,176,489** (NO. 06CV00726)

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157 LG.PHILIPS LCD CO. LTD. v. CHI MEI OPTOELECTRONICS CORPORATION ET AL, NO. 1:06cv00726 (Docket) (D.Del. Dec. 1, 2006)

158 AU OPTRONICS CORPORATION v. LG.PHILIPS LCD CO. LTD. ET AL, NO. 1:07cv00357 (Docket) (D.Del. Jun. 6, 2007)

Expert Court Documents (U.S.A.)

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159 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680917 (Expert Report and Affidavit) (D.Del. Aug. 10, 2008) **Declaration of Dr. Pochi Yeh** (NO. 06-726, JJF)

160 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680918 (Expert Report and Affidavit) (D.Del. Aug. 10, 2008) **Declaration of Dr. John D. Villasenor in Support of Cmo's Opening Brief on Claim Construction** (NO. 06-726, JJF)

161 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680919 (Expert Report and Affidavit) (D.Del. Aug. 11, 2008) **Declaration of Dr. Miltiadis Hatalis in Support of Defendants Chi Mei Optoelectronics' Proposed Claim Constructions** (NO. 06-726, JJF)

162 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680921 (Expert Report and Affidavit) (D.Del. Aug. 29, 2008) **Declaration of Dr. George M. Pharr** (NO. 06-726, JJF)

163 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680920 (Expert Report and Affidavit) (D.Del. Sep. 4, 2008) **Declaration of David Eccles** (NO. 06-726, JJF)

164 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680922 (Expert Report and Affidavit) (D.Del. Sep. 4, 2008) **Declaration of Dr. Allan R. Kmetz** (NO. 06-726, JJF)

165 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680923 (Expert Report and Affidavit) (D.Del. Sep. 4, 2008) **Declaration of Dr. Pochi Yeh in Support of Responsive Brief** (NO. 06-726, JJF)

166 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics Usa, Inc., Defendants; Au Optronics Corporation, Plaintiff, v. LG Display Co., Ltd. and LG Display America, Inc., Defendants; LG Philips L, 2008 WL 8096469 (Expert Report and Affidavit) (D.Del. Sep. 4, 2008) **Declaration of Aris K. Silzars in Support of Auo's Response to Lgd's Claim Construction Briefing on Auo's Patents** (NO. 06-726-JJF, 07-357-JJF)

167 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants; Au Optronics Corporation, Plaintiff, v. LG Display Co., Ltd. and LG Display America, Inc., Defendants., 2008 WL 7505544 (Expert Report and Affidavit) (D.Del. Oct. 31, 2008) **Supplemental Declaration of Aris K. Silzars in Support of Au Optronics' Reply Brief in Support of Its Motion to Compel LGD to Produce Complete GDS Files** (NO. 06-726-JJF, 07-357-JJF)

168 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants; Au Optronics Corporation, Plaintiff, v. LG Display Co., Ltd. and LG Display America, Inc., Defendants., 2008 WL 8096470 (Expert Report and Affidavit) (D.Del. Nov. 19, 2008) **Declaration of Aris K. Silzars in Support of Auo's Motion to Compel LGD to Produce Technical Documents** (NO. 06-726-JJF, 07-357-JJF)

169 LG DISPLAY CO., LTD., v. AU OPTRONICS CORPORATION and Au Optronics Corporation America et al., 2009 WL 5850939 (Expert Report and Affidavit) (D.Del. Feb. 27, 2009) **Report of Expert Tsu-Jae King Liu, Ph.D. Regarding Invalidity of United States Patent Number 5,019,002** (NO. 06CV00726)

170 LG DISPLAY CO., LTD., v. AU OPTRONICS CORPORATION and Au Optronics Corporation AMerica., 2009 WL 5850940 (Expert Report and Affidavit) (D.Del. Feb. 27, 2009) **Report of Expert Regarding Invalidity of United States Patent Number 7,218,374 of Lawrence Tannas, Jr.** (NO. 06CV00726)

171 LG DISPLAY CO., LTD., v. AU OPTRONICS CORPORATION and Au Optronics Corporation America., 2009 WL 5850941 (Expert Report and Affidavit) (D.Del. Feb. 27, 2009) **Report of Expert Webster Howard, Ph.D. Regarding Invalidity of United States Patent Numbers 5,905,274, 6,815,321, and 7,176,489** (NO. 06CV00726)

172 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2009 WL 6869995 (Expert Report and Affidavit) (D.Del. Feb. 27, 2009) **Report of Expert Tsu-Jae King Liu, Ph.D. Regarding Invalidity of United States Patent Number 5,825,449** (NO.

06CV00726)

173 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2010 WL 3740722 (Expert Report and Affidavit) (D.Del. Aug. 9, 2010) **Declaration of Dr. Aris K. Silzars in Support of Au Optronics Corporation's Reply Brief in Support of Its Motion for Permanent Injunction** (NO. 06-726-JJF, 07-357-JJF, 08-355-JJF)

174 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2010 WL 3740723 (Expert Report and Affidavit) (D.Del. Sep. 8, 2010) **Amended Declaration of Jonathan D. Putnam in Support of AU Optronics Corporation's Reply Brief in Support of its Motion for Permanent Injunction** (NO. 06-726-JJF, 07-357-JJF, 08-355-JJF)

D.Del. Trial Motions, Memoranda And Affidavits

175 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002378 (Trial Motion, Memorandum and Affidavit) (D.Del. Aug. 11, 2008) **Memorandum In Support of Defendants Chi Mei Optoelectronics' Proposed Claim Constructions** (NO. 106CV00726)

176 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2008 WL 6002380 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Auo's Response To Lgd's Claim Construction Briefing On Auo's Patents** (NO. 106CV00726)

177 LG DISPLAY CO., Ltd., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; CHI, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2008 WL 6002381 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Auo's Responsive Claim Construction Brief for Lg Display's Patents** (NO. 106CV00726)

178 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002382 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Response of Plaintiff Lg Display Co., Ltd. To Auo's Opening Claim Construction Brief** (NO. 106CV00726)

179 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002383 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Response of Plaintiff Lg Display Co., Ltd. To Cmo's Opening Claim Construction Brief** (NO. 106CV00726)

180 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002384 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Chi Mei Optoelectronics' Answering Memorandum Regarding Proposed Claim Constructions** (NO. 106CV00726)

181 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al.,

Defendants., 2008 WL 6002385 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 10, 2008) **Plaintiff LG Display Co., Ltd.'s Brief in Support of its Motion to Strike AU Optronics Corporation's Claim Construction Briefs** (NO. 106CV00726)

182 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6137427 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 10, 2008) **Plaintiff Lg Display Co., Ltd.'s Brief in Support of Its Motion to Strike Chi Mei Optoelectronics Corporation's Claim Construction Briefs** (NO. 06-726, JJF)

183 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendats., 2009 WL 1347872 (Trial Motion, Memorandum and Affidavit) (D.Del. Jan. 20, 2009) **Plaintiff Lg Display's Opening Brief in Support of its Motion to Compel Au Optronics Corporation and Chi Mei Optoelectronics Corporation to Provide Knowledgeable Deposition Witnesses and for Entry of** (NO. 106CV00726)

184 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 1347876 (Trial Motion, Memorandum and Affidavit) (D.Del. Feb. 6, 2009) **Defendant Au Optronics Corporation's Answering Brief in Opposition to Plaintiff Lg Display Co., Ltd.'s Motion to Compel Auo to Provide Knowledgeable Deposition Witnesses and for Entry of Protective Or** (NO. 106CV00726)

185 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi Mei Optoelectronics Corporation, and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 1347859 (Trial Motion, Memorandum and Affidavit) (D.Del. Feb. 17, 2009) **Defendant AU Optronics Corporation's Corrected Answering Brief in Opposition to Plaintiff's Motion to Strike Advice of Counsel Defense or in the Alternative, to Compel Production of Documents, Witness** (NO. 106CV00726)

186 LG DISPLAY CO., LTD., Plaintiff, v. AU OPIRONICS CORPORATION; AU Optronics Corporation America; Chi Mei Optoelectronics Corporation, and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 1347866 (Trial Motion, Memorandum and Affidavit) (D.Del. Feb. 17, 2009) **Defendant AU Optronics Corporation's Answering Brief in Opposition to Plaintiff Lg Display Co., Ltd.'s Motion to Compel Additional Correlation Charts, Technical Documents, and Damages Discovery** (NO. 106CV00726)

187 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants. CHI MEI OPTOELECTRONICS CORPORATION and Chi Mei Optoelectronics USA, Inc., Plaintiffs, v. LG DISPLAY CO., LTD. and Lg Display America, Inc., Defendants., 2009 WL 3242276 (Trial Motion, Memorandum and Affidavit) (D.Del. May 8, 2009) **Chi Mei Optoelectronics' Motion in Limine No. 3 to Exclude Evidence of LG Display Settlement Agreements** (NO. 106CV00726)

188 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants. CHI MEI OPTOELECTRONICS CORPORATION and CHI Mei Optoelectronics USA, Inc., Plaintiffs, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 3242277 (Trial Motion, Memorandum and Affidavit) (D.Del. May 8, 2009) **Chi Mei Optoelectronics' Motion in Limine No. 4 to Exclude Testimony By Lgd's Expert Witness**

Arthur Cobb Due to Failure to Comply with the Requirements of FRCP 26 (NO. 106CV00726)

189 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTONICS CORPORATION, et al., Defendants. CHI MEI OPTOELECTRONICS CORPORATION and Chi Mei Optoelectronics USA, Inc., Plaintiffs, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 3242278 (Trial Motion, Memorandum and Affidavit) (D.Del. May 8, 2009) **Chi Mei Optoelectronics' Motion in Limine No. 5 to Preclude Lg Display from Presenting Evidence or Argument Regarding the Supplemental Expert Report of Dr. Elliott Schlam and to Strike the Report** (NO. 106CV00726)

190 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants. CHI MEI OPTOELECTRONICS CORPORATION and Chi Mei Optoelectronics USA, Inc., Plaintiffs, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 3242279 (Trial Motion, Memorandum and Affidavit) (D.Del. May 8, 2009) **Chi Mei Optoelectronics' Motion in Limine No.6 to Preclude Lg Display Form Presenting Evidence or Argument Regarding the Rebuttal Expert Reports of Dr. Elliott Schlam and to Strike the Reports** (NO. 106CV00726)

191 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants. CHI MEI OPTOELECTRONICS CORPORATION and Chi Mei Optoelectronics USA, Inc., Plaintiffs, v. LG DISPLAY CO., Ltd. and Lg Display America, Inc., Defendants., 2009 WL 3242281 (Trial Motion, Memorandum and Affidavit) (D.Del. May 8, 2009) **Chi Mei Optoelectronics' Memorandum of Points and Authorities in Support of Motion for Partial Summary Judgment Finding Non-Infringement of U.S. Patent 6,803,984 By Chi Mei Optoelectronics' Fab V** (NO. 106CV00726)

192 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORAION, et al., Defendants., 2009 WL 3242286 (Trial Motion, Memorandum and Affidavit) (D.Del. May 13, 2009) **LG Display Co., Ltd.'s Opposition to AUO's Motion to Supplement Briefing of Its Motion to Preclude LG Display's Reliance On Invalidating Prior Art** (NO. 106CV00726)

193 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; CHI, MEI Optoelectronics Corporation; and CHI MEI Optoelectronics USA, Inc., Defendants., 2009 WL 3242287 (Trial Motion, Memorandum and Affidavit) (D.Del. May 21, 2009) **AUO's Opening Brief in Support of its Motion for Summary Judgment of Invalidity on all Claims of LGD's "274, "321 and "489 Patents** (NO. 106CV00726)

194 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3242288 (Trial Motion, Memorandum and Affidavit) (D.Del. May 21, 2009) **Au Optronics' Motion in Limine No. 1 to Exclude any Opinion Testimony by LG Display's Technical Experts Regarding any Devices or Processess that they have not Analyzed** (NO. 106CV00726)

195 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245831 (Trial Motion, Memorandum and Affidavit) (D.Del. May 21, 2009) **Au Optronics' Motion in Limine No.3 to Preclude Any Testimony from the Prior CPT Litigations, Including Reliance by Experts on the Prior Testimony of Expert Michael**

Keeley in the California CPT Litiga (NO. 106CV00726)

196 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245832 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **AU Optronics' Motion in Limine No. 4 to Preclude Any Testimony from the Prior CPT Litigations, Including Reliance By Experts on the Prior Testimony of Dr. Holmberg, Mr. Castleberry, and Mr. Ho Lee in** (NO. 106CV00726)

197 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245833 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **Au Optronics' Motion in Limine No.5 to Preclude Lg Display from Introducing Any Evidence Regarding Yield Percentage and to Preclude Mr. Cobb from Offering Any Opinions Based Upon Yield Improvements** (NO. 106CV00726)

198 LG DISPLAY COMPANY, LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245835 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **Lg Display Co., Ltd.'s Motion in Limine No. 2 to Preclude Auo's Experts from Asserting Prior Art Against Lg Display's Patents that They Did not Address in Their Expert Reports** (NO. 106CV00726)

199 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245841 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 8, 2009) **Au Optronics' Response to Lg Display Co. Ltd.'s Motion in Limine No.5 to Preclude Introduction of Evidence or Opinion Testimony Concerning Electro-Static Discharge Repairs and Repair Costs** (NO. 106CV00726)

200 LG DISPLAY COMPANY, LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245843 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Motion in Limine No.5 to Preclude Auo from Introducing Evidence or Opinion Testimony Concerning Purported Electro-Static Discharge Repairs and Repair Costs** (NO. 106CV00726)

201 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245844 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Memorandum in Opposition to Auo's Motion in Limine No. 5** (NO. 106CV00726)

202 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245847 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Memorandum in Opposition to Auo's Motion in Limine No. 1** (NO. 106CV00726)

203 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245848 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **Lg Display Co., Ltd.'s Memorandum in Opposition to Auo's Motion in Limine No. 2 to Preclude Any Reference to the Prior Cpt Litigations** (NO. 106CV00726)

D.Del.

204 John D. Villasenor, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6877461 (Court-filed Expert Resume) (D.Del. Aug. 12, 2008) **Expert Resume of John D. V** (NO. 106CV00726)

205 Pochi Yeh, curriculum vitae filed in LG. Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6889166 (Court-filed Expert Resume) (D.Del. Aug. 12, 2008) **Expert Resume of Pochi Yeh** (NO. 106CV00726)

206 Miltiadis K. Hatalis, curriculum vitae filed in LG,Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6889167 (Court-filed Expert Resume) (D.Del. Aug. 12, 2008) **Expert Resume of Miltiadis K. Hatalis** (NO. 106CV00726)

207 David A. Eccles, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6877462 (Court-filed Expert Resume) (D.Del. Sep. 4, 2008) **Expert Resume of David A. Eccles** (NO. 106CV00726)

208 Allan R. Kmetz, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6877463 (Court-filed Expert Resume) (D.Del. Sep. 4, 2008) **Expert Resume of Allan R. Kmetz** (NO. 106CV00726)

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D.Del.

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212 ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY, INCLUDES DUMMY CONDUCTIVE PATTERNS ARRANGED BETWEEN CONNECTION PADS AND PIXEL ELECTRODES, Derwent World Patents Legal 2002-674166

Assignments

213 Action: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS). Number of Pages: 008, (DATE RECORDED: May 18, 2007)

214 Action: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS). Number of Pages: 017, (DATE RECORDED: Dec 21, 2005)

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.. Request for Re-Examination, (OG DATE: May 25, 2010)

Docket Summaries

216 AU OPTRONICS CORPORATION v. LG.PHILIPS LCD CO. LTD. ET AL, (D.DEL. Jun 06,

2007) (NO. 1:07CV00357), (35 USC 271 PATENT INFRINGEMENT)

217 AU OPTRONICS CORPORATION v. LG.PHILIPS LCD CO., LTD., (W.D.WIS. Mar 08, 2007) (NO. 3:07C00137), (PROPERTY RIGHTS; PATENT)

Prior Art (Coverage Begins 1976)

C 218 LIQUID CRYSTAL DISPLAY DEVICE HAVING PERIPHERAL DUMMY LINES, US PAT 5285301Assignee: Hitachi, Ltd., (U.S. PTO Utility 1994)

C 219 LIQUID CRYSTAL DISPLAY WITH ENHANCED GATE PAD PROTECTION AND METHOD OF MANUFACTURING THE SAME, US PAT 6163356Assignee: LG Electronics, (U.S. PTO Utility 2000)

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Items 1 to 2 of 2

	Patent	Class	Subclass	Description	Court (All)	Docket Number	Filed	Date Retrieved
☐	6,689,629	438	25	AU Optronics Corporation v. Lg.philips LCD Co Ltd et al	US-DIS-DED	1:07cv357	6/6/2007	12/4/2010
☐	6,689,629	438	25	AU Optronics Corporation v. Lg.philips LCD Co, Ltd	US-DIS-WIWD	1:07cv137	3/8/2007	11/5/2009

Items 1 to 2 of 2

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US District Court Civil Docket

U.S. District - Delaware
(Wilmington)

1:07cv357

Au Optronics Corporation v. Lg.Philips Lcd Co Ltd et al

Date Filed:	**06/06/2007**	**Class Code:**	
Assigned To:	**Judge Leonard P Stark**	**Closed:**	**No**
Referred To:		**Statute:**	**35:271**
Nature of suit:	**Patent (830)**	**Jury Demand:**	**Defendant**
Cause:	**Patent Infringement**	**Demand Amount:**	**$0**
Lead Docket:	**1:06-cv-00726-LPS**	**NOS Description:**	**Patent**
Other Docket:	**1:06-cv-00726-LPS** **1:08-cv-00355-LPS** **1:10-cv-00706**		
Jurisdiction:	**Federal Question**		

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Date	#	Proceeding Text
06/06/2007	49	Record of case transferred in from District of Wisconsin(Western); Case Number in Other District: 07-C-137. Copy of Docket Sheet and original file with documents numbered 1-49 attached. (Attachments: # 1 DI #1# 2 DI #2# 3 Exhibit A to DI #2# 4 Exhibit B to DI #2# 5 Exhibit C to DI #2# 6 DI #3# 7 DI #4# 8 DI #5# 9 DI #6# 10 DI #7# 11 DI #8# 12 DI #9# 13 DI #10# 14 DI #11# 15 DI #12# 16 DI #13# 17 DI #14# 18 DI #15# 19 DI #16# 20 DI #17# 21 DI #18# 22 DI #19# 23 DI #20# 24 DI #21# 25 DI #22# 26 DI #23# 27 DI #24- SEALED DOCUMENT# 28 DI #25# 29 DI #26# 30 DI #27# 31 DI #28# 32 DI #29# 33 Exhibit A to DI #29# 34 Exhibit B to DI #29# 35 Exhibit C to DI #29# 36 Exhibit D to DI #29# 37 Exhibit E to DI #29# 38 DI #30# 39 DI #31# 40 DI #32- SEALED DOCUMENT# 41 DI #33# 42 DI #34# 43 DI #35# 44 DI #36# 45 DI #37# 46 DI #38# 47 DI #39# 48 Exhibit A to DI #39# 49 DI #40# 50 DI #41# 51 DI #42# 52 DI #43# 53 DI #44# 54 DI #45# 55 DI #46# 56 Exhibit A to DI #46# 57 Exhibit B to DI #46# 58 DI #47# 59 DI #48# 60 DI #49)(ead) (Entered: 06/08/2007)
06/06/2007	--	Order granting Motion To Transfer matter to U.S. District Court for the District of Delaware, signed by Judge Shabaz on 5/30/07 in U.S.D.C., Wisconsin(Western) - DI # in other district: 49. (ead) (Entered: 06/08/2007)
06/06/2007	50	COMPLAINT filed against LG.Philips LCD Co. Ltd., LG.Philips LCD America - - filed by AU Optronics Corporation. (Filed in USDC/WD/WI on 3/8/07 as DI #2)(Attachments: # 1 Civil Cover Sheet)(ead) (Entered: 06/08/2007)
06/06/2007	51	MOTION to Dismiss for Improper Venue - filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 3/29/07 as DI #6) (ead) (Entered: 06/08/2007)
06/06/2007	52	OPENING BRIEF in Support re 51 MOTION to Dismiss for Improper Venue filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 3/29/07 as DI #7) (ead) (Entered: 06/08/2007)
06/06/2007	53	AFFIDAVIT of Dong Hoon Han- filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 3/29/07 as DI #8) (ead) (Entered: 06/08/2007)
06/06/2007	54	ANSWERING BRIEF in Opposition re 51 MOTION to Dismiss for Improper Venue filed by AU Optronics Corporation. (Filed in USDC/WD/WI on 4/18/07 as DI #27) (ead) (Entered: 06/08/2007)
06/06/2007	55	REPLY BRIEF re 51 MOTION to Dismiss for Improper Venue filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 4/30/07 as DI #31)(ead) (Entered: 06/08/2007)
06/06/2007	56	REPLY BRIEF re 51 MOTION to Dismiss for Improper Venue filed by LG.Philips LCD America. CORRECTED (Filed in USDC/WD/WI on 5/3/07 as DI #36) (ead) (Entered: 06/08/2007)
06/06/2007	57	MOTION to Compel LG.Philips LCD America to Respond to Requests for Production and Interrogatories and for Other Relief - filed by AU Optronics Corporation. (Filed in USDC/WD/WI on 5/18/07 as DI #41) (ead) (Entered: 06/08/2007)
06/06/2007	58	OPENING BRIEF in Support re 57 MOTION to Compel filed by AU Optronics Corporation. (Filed in USDC/WD/WI on 5/18/07 as DI #42) (ead) (Entered: 06/08/2007)
06/06/2007	59	AFFIDAVIT of James R. Troupis re 57 MOTION to Compel filed by AU Optronics Corporation. (Filed in USDC/WD/WI on 5/18/07 as DI #43) (ead) (Entered: 06/08/2007)
06/06/2007	60	AFFIDAVIT of David W. Panneck re 57 MOTION to Compel filed by AU Optronics Corporation. (Attachments: # 1 Notice of Filing of Papaer Documents- Exhibits A-G) (Filed in USDC/WD/WI on 5/18/07 as DI #44)(ead) (Entered: 06/08/2007)
06/06/2007	61	ANSWERING BRIEF in Opposition re 57 MOTION to Compel filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 5/22/07 as DI #45) (ead) (Entered: 06/08/2007)
06/06/2007	62	AFFIDAVIT of Nicole Talbott Settle re 61 Answering Brief in Opposition filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 5/22/07 as DI #46) (ead) (Entered: 06/08/2007)
06/06/2007	63	NOTICE of filing the following document(s) in paper format: Exhibits A-T to Declaration of David W. Panneck (DI #28 Filed in USDC/WD/WI on 4/18/07)). Original document(s) on file in Clerk's Office. Notice filed by AU Optronics Corporation. (ead) (Entered: 06/08/2007)
06/06/2007	64	NOTICE of filing the following document(s) in paper format: Exhibits A-W to Declaration of Paul Barbato. (DI #38 Filed in USDC/WD/WI on 5/7/07) Original document(s) on file in Clerk's Office. Notice filed by AU Optronics Corporation. (ead) (Entered: 06/08/2007)
06/06/2007	65	NOTICE of filing the following document(s) in paper format: Exhibits A-G to Declaration of David W. Panneck. (Filed as DI #44 in USDC/WD/WI on 5/18/07) Original document(s) on file in Clerk's Office. Notice filed by AU Optronics Corporation (ead) (Entered: 06/08/2007)
06/08/2007	66	Local Counsel Letter sent to James D. Peterson.Notice of Compliance deadline set for 7/12/2007. (ead) (Entered: 06/08/2007)
06/08/2007	67	Local Counsel Letter sent to James P. Troupis. Notice of Compliance deadline set for 7/12/2007. (ead) (Entered: 06/08/2007)
06/08/2007	68	Report to the Commissioner of Patents and Trademarks for Patent/Trademark Number(s) 6,689,629; 6,976,781; 6,778,160; (ead) (Entered: 06/08/2007)

06/08/2007	69	SEALED AFFIDAVIT of R. Tyler Goodwyn in Support of LG.Philips LCD Co. Ltd's Motion to Transfer to the District of Delaware filed by LG.Philips LCD Co. Ltd. (Filed in USDC/WD/WI on 4/16/07 as DI #24) (ead) (Entered: 06/08/2007)
06/08/2007	70	SEALED AFFIDAVIT of Dong Hoon Han in Support of LG.Philips LCD America's Motion to Dismiss re 51 MOTION to Dismiss for Improper Venue filed by LG.Philips LCD America. (ead) (Entered: 06/08/2007)
06/08/2007	71	NOTICE of Appearance by Richard D. Kirk on behalf of LG.Philips LCD Co. Ltd., LG.Philips LCD America (Kirk, Richard) (Entered: 06/08/2007)
06/11/2007	72	ANSWER to Complaint with Jury Demand, COUNTERCLAIM against AU Optronics Corporation by LG.Philips LCD America. (Attachments: # 1 Certificate of Service)(Kirk, Richard) (Entered: 06/11/2007)
06/11/2007	73	ANSWER to Complaint with Jury Demand, COUNTERCLAIM against AU Optronics Corporation America, Chi Mei Optoelectronics Corporation, CHI MEI OPTOELECTRONICS USA, INC., AU Optronics Corporation by LG.Philips LCD Co. Ltd.. (Attachments: # 1 Exhibit A# 2 Exhibit B# 3 Exhibit C# 4 Certificate of Service)(Kirk, Richard) (Entered: 06/11/2007)
06/12/2007	74	PRAECIPE filed by Richard D. Kirk on behalf of LG.Philips LCD Co. Ltd. requesting Clerk to issue Summonses (Attachments: # 1 Certifidate of Service)(Kirk, Richard) (Entered: 06/12/2007)
06/12/2007	--	Summons Issued as to AU Optronics Corporation America on 6/12/2007; CHI MEI OPTOELECTRONICS USA, INC. on 6/12/2007. (eew) (Entered: 06/12/2007)
06/13/2007	--	Summons Issued as to Chi Mei Optoelectronics Corporation on 6/13/2007. (eew) (Entered: 06/13/2007)
06/14/2007	75	Return of Service Executed by LG.Philips LCD Co. Ltd.. CHI MEI OPTOELECTRONICS USA, INC. served on 6/12/2007, answer due 7/2/2007. (Kirk, Richard) (Entered: 06/14/2007)
06/14/2007	76	NOTICE OF SERVICE OF ANSWER TO COMPLAINT WITH COUNTERCLAIMS ON DEFENDANT CHI MEI OPTOELECTRONICS CORPORATION PURSUANT TO 10 DEL.C. SECTION 3104 by LG.Philips LCD Co. Ltd. (Kirk, Richard) (Entered: 06/14/2007)
06/14/2007	77	NOTICE OF SERVICE OF ANSWER TO COMPLAINT WITH COUNTERCLAIMS ON DEFENDANT AU OPTRONICS CORPORATION AMERICA A/K/A AU OPTRONICS AMERICA, INC. PURSUANT TO 10 DEL.C.SECTION 3104 by LG.Philips LCD Co. Ltd. (Kirk, Richard) (Entered: 06/14/2007)
06/18/2007	78	NOTICE of Appearance by Ashley Blake Stitzer on behalf of LG.Philips LCD Co. Ltd., LG.Philips LCD America (Stitzer, Ashley) (Entered: 06/18/2007)
06/18/2007	79	NOTICE OF SERVICE of LG. PHILIPS LCD'S OBJECTIONS TO AU OPTRONICS CORPORATION'S SECOND SET OF INTERROGATORIES (NO. 17) by LG.Philips LCD Co. Ltd..(Stitzer, Ashley) (Entered: 06/18/2007)
06/21/2007	80	ANSWER to Counterclaim, COUNTERCLAIM against LG.Philips LCD Co. Ltd. by AU Optronics Corporation America.(Pascale, Karen) (Entered: 06/21/2007)
06/21/2007	81	ANSWER to Counterclaim of LG.Philips LCD Co., LTD. , COUNTERCLAIM against LG.Philips LCD Co. Ltd. by AU Optronics Corporation. (Attachments: # 1 Exhibit A-C)(Pascale, Karen) (Entered: 06/21/2007)
06/21/2007	82	ANSWER to Counterclaim of LG.Philips LCD America, Inc. , COUNTERCLAIM against LG.Philips LCD America by AU Optronics Corporation. (Attachments: # 1 Exhibit A-C)(Pascale, Karen) (Entered: 06/21/2007)
06/26/2007	83	Joint MOTION to Consolidate Cases - filed by AU Optronics Corporation America, AU Optronics Corporation, LG.Philips LCD Co. Ltd., LG.Philips LCD America. (Attachments: # 1 Text of Proposed Order Of Consolidation# 2 Certificate of Compliance Local Rule 7.1.1 Statement)(Pascale, Karen) (Entered: 06/26/2007)
06/26/2007	84	NOTICE of Joint Motion To Consolidate by AU Optronics Corporation America, AU Optronics Corporation, LG.Philips LCD Co. Ltd., LG.Philips LCD America re 83 MOTION to Consolidate Cases (Pascale, Karen) (Entered: 06/26/2007)
06/26/2007	85	Joint STATEMENT re 83 MOTION to Consolidate Cases, 84 Notice (Other) Following Transfer Pursuant To Local Rule 81.2 by AU Optronics Corporation, LG.Philips LCD Co. Ltd., LG.Philips LCD America. (Pascale, Karen) (Entered: 06/26/2007)
06/29/2007	86	NOTICE OF SERVICE of LG.PHILIPS LCD CO., LTD.'S OBJECTIONS TO AU OPTRONICS CORPORATION'S SECOND SET OF DOCUMENTS REQUESTS (NOS. 143-152) by LG.Philips LCD Co. Ltd..(Stitzer, Ashley) (Entered: 06/29/2007)
07/02/2007	87	ANSWER to Counterclaim, COUNTERCLAIM CHI MEI OPTOELECTRONICS USA, INC.'S ANSWER, AFFIRMATIVE DEFENSES AND COUNTERCLAIMS TO THE COUNTERCLAIMS OF LG. PHILIPS LCD CO., LTD. against LG.Philips LCD Co. Ltd. by CHI MEI OPTOELECTRONICS USA, INC..(Rovner, Philip) (Entered: 07/02/2007)
07/03/2007	88	MOTION for Pro Hac Vice Appearance of Attorney M. Craig Tyler, Brian D. Range and Julie M. Holloway - filed by AU Optronics Corporation America, AU Optronics Corporation. (Pascale, Karen) (Entered: 07/03/2007)
07/05/2007	89	MOTION to Dismiss for Lack of Jurisdiction Over the Person, MOTION to Dismiss for Insufficiency of Service of Process - filed by Chi Mei Optoelectronics Corporation. (Rovner, Philip) (Entered: 07/05/2007)
07/05/2007	--	Set Briefing Schedule: re 89 MOTION to Dismiss for Lack of Jurisdiction Over the Person MOTION to Dismiss for Insufficiency of Service of Process. Answering Brief due 7/23/2007. (lec) (Entered: 07/06/2007)
07/06/2007	90	Joint MOTION to Consolidate Cases - filed by LG. Philips LCD America, Inc., AU Optronics Corporation America, AU Optronics Corporation, LG.Philips LCD Co. Ltd.. (Pascale, Karen) (Entered: 07/06/2007)
07/06/2007	91	Joint NOTICE of Motion (Re-Notice) and Withdrawal of Motion by LG. Philips LCD America, Inc., AU Optronics Corporation America, AU Optronics Corporation, LG.Philips LCD Co. Ltd. re 92 Joint MOTION to Consolidate Cases, 90 MOTION to Consolidate Cases (Pascale, Karen) (Entered: 07/06/2007)

07/10/2007	92	Amended ANSWER to Counterclaim of LG. Philips LCD Co. Ltd. , COUNTERCLAIM against LG.Philips LCD Co. Ltd. by AU Optronics Corporation America.(Pascale, Karen) (Entered: 07/10/2007)
07/10/2007	93	Amended ANSWER to Counterclaim of LG.Philips LCD Co. Ltd. , COUNTERCLAIM against LG.Philips LCD Co. Ltd. by AU Optronics Corporation. (Attachments: # 1 Exhibit A - C)(Pascale, Karen) (Entered: 07/10/2007)
07/10/2007	--	SO ORDERED D.I. 88 MOTION for Pro Hac Vice Appearance of Attorney M. Craig Tyler, Brian D. Range and Julie M. Holloway filed by AU Optronics Corporation, AU Optronics Corporation America. Signed by Judge Joseph J. Farnan, Jr. on 7/10/2007. (lec) (Entered: 07/10/2007)
07/11/2007	--	ORAL ORDER re 57 MOTION to Compel filed by AU Optronics Corporation. This motion will be decided after a decision has been rendered on the pending Motion to Consolidate. Therefore, the Notice for the Motion Day Hearing of July 13, 2007 is cancelled. Ordered by Judge Joseph Farnan this 11th day of July, 2007. (dlk) (Entered: 07/11/2007)
07/11/2007	94	ANSWER to Counterclaim filed by AU Optronics Corporation by LG.Philips LCD America.(Kirk, Richard) (Entered: 07/11/2007)
07/12/2007	95	NOTICE of Withdrawal of Motion to Compel LG.Philips LCD America to Respond to Requests for Production and Interrogatories and for Other Relief by AU Optronics Corporation re 57 MOTION to Compel (Pascale, Karen) (Entered: 07/12/2007)
07/16/2007	96	Disclosure Statement pursuant to Rule 7.1 filed by AU Optronics Corporation, AU Optronics Corporation America. (Pascale, Karen) (Entered: 07/16/2007)
07/19/2007	97	Disclosure Statement pursuant to Rule 7.1 filed by Chi Mei Optoelectronics Corporation identifying CHI MEI CORPORATION as Corporate Parent. (Rovner, Philip) (Entered: 07/19/2007)
07/19/2007	98	Disclosure Statement pursuant to Rule 7.1 filed by CHI MEI OPTOELECTRONICS USA, INC. identifying CMO JAPAN CO., LTD. as Corporate Parent. (Rovner, Philip) (Entered: 07/19/2007)
07/19/2007	99	ANSWERING BRIEF in Opposition re 89 MOTION to Dismiss for Lack of Jurisdiction Over the Person MOTION to Dismiss for Insufficiency of Service of Process filed by LG.Philips LCD America, LG.Philips LCD Co. Ltd..Reply Brief due date per Local Rules is 7/30/2007. (Attachments: # 1 Certificate of Service)(Stitzer, Ashley) (Entered: 07/19/2007)
07/19/2007	100	ORDER GRANTING D.I. 90 Motion to Consolidate Cases. This case is consolidated into Civil Action No. 06-726-GMS. All future filings shall be captioned and filed only in the consolidated lead case. Signed by Judge Joseph J. Farnan, Jr. on 07/19/2007. (dlk) (Entered: 07/23/2007)
07/19/2007	--	Case associated with lead case: Create association to 1:06-cv-00726-GMS. (dlk) (Entered: 07/23/2007)
07/23/2007	--	Case reassigned to Judge Gregory M. Sleet. Please include the initials of the Judge (GMS) after the case number on all documents filed. (Please note all future filings shall still be captioned and filed only in the consolidated lead case 1:06-cv-00726) (rjb) (Entered: 07/23/2007)
07/23/2007	101	ANSWER to Counterclaim of defendant Chi Mei Optoelectronics USA, Inc. by LG.Philips LCD America. (Attachments: # 1 certificate of service)(Kirk, Richard) (Entered: 07/23/2007)
07/24/2007	102	ANSWER to Counterclaim OF AU OPTRONICS CORPORATION AMERICA , COUNTERCLAIM against AU Optronics Corporation America by LG.Philips LCD Co. Ltd.. (Attachments: # 1 Exhibit A)(Kirk, Richard) (Entered: 07/24/2007)
07/24/2007	103	ANSWER to Counterclaim OF AU OPTRONICS CORPORATION , COUNTERCLAIM against AU Optronics Corporation by LG.Philips LCD Co. Ltd.. (Attachments: # 1 Exhibit A)(Kirk, Richard) (Entered: 07/24/2007)
09/28/2007	104	NOTICE of AU Optronics Corporation's Reply to LG.Philips LCD Co., Ltd's Additional Counterclaims by AU Optronics Corporation re 138 Answer to Counterclaim (Pascale, Karen) (Entered: 09/28/2007)
12/14/2007	--	Case reassigned to Judge Joseph J. Farnan, Jr. Please include the initials of the Judge (JJF) after the case number on all documents filed. (rjb) (Entered: 12/14/2007)
03/13/2008	--	CORRECTING ENTRY: Amended the party name for plaintiff and counterclaim plaintiff LG. Philips LCD Co., LTD to LG Display Co., Ltd., per DI # 161 ;and amended defendant and counterclaim plaintiff LG. Philips LCD America, Inc. to LG Display America, Inc., per DI # 161 . Also confirmed with counsel as to how the amended caption to read. (nms) (Entered: 03/13/2008)
03/28/2008	105	NOTICE of Service of AU Optronics Corporation's First Set of Requests for Production of Documents and Things to LG Display Co., Ltd., Nos. 1-110; AU Optronics Corporation's Second Set of Requests for Production of Documents to LG Display Co., Ltd. (Nos. 111-208); AU Optronics Corporation's First Set of Interrogatories to LG Display Co., Ltd. (Nos. 1-13), AU Optronics Corporation's Second Set of Interrogatories to LG Display Co., Ltd. (Nos. 14-23), and AU Optronics Corporation's Notice of Rule 30(b)(6) Deposition of Plaintiff LG Display Co. Ltd. by Au Optronics Corporation, AU Optronics Corporation America, AU Optronics Corporation re (1 in 1:06-cv-00726-JJF) Complaint, (Keller, Karen) (Entered: 03/28/2008)
04/16/2008	106	TRANSCRIPT of Status Telephone Conference held on 2/14/2008 before Judge Farnan. Court Reporter: Dale C. Hawkins (Hawkins Reporting). (Transcript on file in Clerk's Office) (nms) (Entered: 04/16/2008)
04/25/2008	107	NOTICE OF SERVICE of Defendant AU Optronics Corporation's Objections and Responses to Plaintiff LG Display Co., Ltd.'s First Set of Interrogatories (Nos. 1-19); and Defendant AU Optronics Corporation's Objections and Responses to Plaintiff LG Display Co., Ltd.'s First Set of Requests for the Production of Documents and Things (Nos. 1-83) by AU Optronics Corporation.(Pascale, Karen) (Entered: 04/25/2008)
05/01/2008	108	Letter to The Honorable Mary Pat Thynge from Karen L. Pascale regarding production of license agreements - re (191 in 1:06-cv-00726-JJF) Letter. (Pascale, Karen) (Entered: 05/01/2008)

06/23/2008	109	NOTICE OF SERVICE of LG Display Co., Ltd.'s Objections and Responses to Attachment A to AU Optronics Corporation's Notice of Rule 30(b)(6) Deposition by LG Display Co., Ltd.. (Attachments: # 1 Certificate of Service)(Kirk, Richard) (Entered: 06/23/2008)
07/17/2008	110	NOTICE OF SERVICE of AU Optronics Corporations Responses and Objections to Plaintiff LG Display Co., Ltd.s Second Set of Interrogatories (Nos. 20-29); and AU Optronics Corporations Supplemental Objections and Responses to Plaintiff LG Display Co., Ltd.s First Set of Interrogatories (Nos. 1-19) by AU Optronics Corporation.(Pascale, Karen) (Entered: 07/17/2008)
07/30/2008	--	ORAL ORDER: LG Display Co., Ltd. shall file a response to the July 30, 2008 letter (D.I. 364 in 06-726) by Chi Mei Optoelectronics Corp. no later than 9:00 a.m. on July 31, 2008. Ordered by Judge Joseph J. Farnan, Jr. on 7/30/2008. (dlk) (Entered: 07/30/2008)
09/08/2008	--	ORAL ORDER: The September 12, 2008 Motion Day Hearing is CANCELLED regarding MOTION to Consolidate Cases filed by LG Display Co., Ltd., MOTION for Leave to File Second Amended Answer to AU Optronics Corporation's Amended Counterclaims and Additional Counterclaims filed by LG Display Co., Ltd., and the MOTION to Consolidate Cases DEFENDANT CHI MEI OPTOELECTRONICS CORPORATION'S M OTION TO CONSOLIDATE AND TO EXTEND DISCOVERY LIMITS filed by Chi Mei Optoelectronics Corporation. The motions will be decided on the papers submitted. Ordered by Judge Joseph J. Farnan, Jr. on 09/08/2008. (dlk) (Entered: 09/08/2008)
09/08/2008	--	ORAL ORDER: The September 12, 2008 Motion Day Hearing is CANCELLED regarding the CHI MEI OPTOELECTRONICS CORPORATION'S MOTION TO LIMIT THE NUMBER OF PATENTS-IN-SUIT AND STAY THE REMAINDER filed by Chi Mei Optoelectronics Corporation. A decision is deferred pending possible oral argument. Ordered by Judge Joseph J. Farnan, Jr. on 9/8/08. (dlk) (Entered: 09/08/2008)
09/08/2008	--	ORAL ORDER: The September 12, 2008 Motion Day Hearing is CANCELLED regarding Motion to Compel Chi Mei Optoelectronics Corporation to Provide Discovery filed by LG Display Co., Ltd., PLAINTIFFS CHI MEI OPTOELECTRONICS' MOTION TO COMPEL DEFENDANTS LG DISPLAY TO RESPOND TO INTERROGATORIES filed by Chi Mei Optoelectronics USA Inc.(D.I. 98 in 08-cv-00355-JJF), Chi Mei Optoelectronics Corporation, and DEFENDANTS CHI MEI OPTOELECTRONICS' MOTION TO COMPEL PLAINTIFFS LG DISPLAY TO PRODUCE DOCUMENTS RESPONSIVE TO DOCUMENT REQUEST NO. 98 filed by Chi Mei Optoelectronics Corporation. The Court will decide these motions on the papers submitted. Ordered by Judge Joseph J. Farnan, Jr. on 9/8/08. (dlk) (Entered: 09/08/2008)
11/20/2008	111	MOTION for Leave to File A First Amended Answer and Joinder In CMO's Motion For Leave To File A First Amended Answer - filed by AU Optronics Corporation America, AU Optronics Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Local Rule 7.1.1 Statement)(Lundgren, Andrew) (Entered: 11/20/2008)
11/20/2008	112	NOTICE OF MOTION by AU Optronics Corporation America, AU Optronics Corporation re 111 MOTION for Leave to File ; Requesting the following Motion Day: December 19, 2008 (Lundgren, Andrew) Modified on 11/25/2008 (nms). (Entered: 11/20/2008)
12/04/2008	113	Amended NOTICE of [AUO's Amended Notice of Subpoena And Deposition to Centric Technical Sales on December 17, 2008] by AU Optronics Corporation America, AU Optronics Corporation re (234 in 1:06-cv-00726-JJF) Notice of Service (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	114	Amended NOTICE of Subpoena And Deposition to Bell Microproducts, Inc. on December 16, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (230 in 1:06-cv-00726-JJF) Notice of Service (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	115	Amended NOTICE of Subpoena And Deposition to Axis Group, Inc. on December 17, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (229 in 1:06-cv-00726-JJF) Notice of Service (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	116	Amended NOTICE of Subpoena And Deposition to Avnet, Inc on December 16, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (228 in 1:06-cv-00726-JJF) Notice of Service (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	117	Amended NOTICE of Subpoena And Deposition to Philips Electronics N.A., Inc. on December 17, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (344 in 1:06-cv-00726-JJF) Notice (Other) (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	118	Amended NOTICE of Subpoena And Deposition to LG Electronics Alabama, Inc. on December 15, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (341 in 1:06-cv-00726-JJF) Notice (Other) (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	119	Amended NOTICE of Subpoena And Deposition to LG Electronics USA, Inc. on December 15, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (342 in 1:06-cv-00726-JJF) Notice (Other) (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	120	Amended NOTICE of Subpoena And Deposition to LG Infocomm, Inc. on December 15, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (340 in 1:06-cv-00726-JJF) Notice (Other) (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	121	Amended NOTICE of Subpoena And Deposition to LG International (America), Inc. on December 15, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (357 in 1:06-cv-00726-JJF) Notice (Other) (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	122	Amended NOTICE of Subpoena And Deposition to Catalyst Sales, Inc. on December 16, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (233 in 1:06-cv-00726-JJF) Notice of Service (Pascale, Karen) (Entered: 12/04/2008)

12/08/2008	--	ORAL ORDER: The Court has reviewed the parties numerous email submissions regarding discovery disputes; therefore, Counsel shall appear for the December 19, 2008 Motion Day Hearing at 10:00 AM in Courtroom 4B before Judge Joseph J. Farnan, Jr. regarding these disputes. The non-prevailing party will be assessed all fees and costs associated with these disputes. Ordered by Judge Joseph J. Farnan, Jr. on 12/8/2008. (dlk) (Entered: 12/08/2008)
12/08/2008	--	CORRECTING ENTRY: The 12/8/2008 Oral Order has been corrected to note that the non-prevailing party will be assessed fees and costs associated with email discovery dispute. Associated Cases: 1:07-cv-00357-JJF, 1:06-cv-00726-JJF(dlk) (Entered: 12/08/2008)
12/12/2008	123	NOTICE of [AUO's Notice of Withdrawal of Amended Notice of Subpoena and Deposition of Philips Electronics N.A., Inc.] by AU Optronics Corporation America, AU Optronics Corporation re (117 in 1:07-cv-00357-JJF, 731 in 1:06-cv-00726-JJF) Notice (Other) (Lundgren, Andrew) (Entered: 12/12/2008)
12/22/2008	--	ORAL ORDER: The Court GRANTS parties Motions To Consolidate (D.I. 298 in 1:06-cv-00726-JJF, D.I. 89 in 1:08-cv-00355-JJF) and (D.I. 295 in 1:06-cv-00726-JJF). Accordingly, all future filings shall be made and captioned under C.A. No. 06-726 only.. Ordered by Judge Joseph J. Farnan, Jr. on 12/19/2008. Associated Cases: 1:06-cv-00726-JJF, 1:07-cv-00357-JJF, 1:08-cv-00355-JJF(dlk) (Entered: 12/22/2008)
12/22/2008	--	Case associated with lead case: Create association to 1:06-cv-00726-JJF. Associated Cases: 1:07-cv-00357-JJF, 1:08-cv-00355-JJF(dlk) (Entered: 12/22/2008)
01/23/2009	--	ORAL ORDER: LG's "motion" regarding 30(b)(6) depos per Mr. Kirk's January 16, 2009 e-mail request is DENIED. CMO's e-mail request for 30(b)(6) deposition, per Mr. Rovner's January 21, 2009 e-mail is GRANTED.. Signed by Judge Joseph J. Farnan, Jr. on 1/22/2009. Associated Cases: 1:06-cv-00726-JJF, 1:07-cv-00357-JJF, 1:08-cv-00355-JJF(dlk) (Entered: 01/23/2009)
02/27/2009	124	Joint Stipulation of Authenticity As To Certain Documents by CHI MEI OPTOELECTRONICS USA, INC., Chi Mei Optoelectronics Corporation, Au Optronics Corporation, AU Optronics Corporation America, LG Display Co. Ltd., LG Display America Inc.. (Pascale, Karen) Modified on 3/3/2009 (nms). (Entered: 02/27/2009)
03/03/2009	--	SO ORDERED, re (124 in 1:07-cv-00357-JJF, 1019 in 1:06-cv-00726-JJF, 106 in 1:08-cv-00355-JJF) Joint Stipulation of Authenticity as to Certain Documents, filed by LG Display America Inc., LG Display Co. Ltd., CHI MEI OPTOELECTRONICS USA, INC., AU Optronics Corporation America, Au Optronics Corporation, Chi Mei Optoelectronics Corporation. Signed by Judge Joseph J. Farnan, Jr. on 3/3/2009. Associated Cases: 1:06-cv-00726-JJF, 1:07-cv-00357-JJF, 1:08-cv-00355-JJF(nms) (Entered: 03/03/2009)
03/09/2009	125	NOTICE OF SERVICE of Expert Report of Jonathan D. Putnam by Au Optronics Corporation, AU Optronics Corporation America.(Pascale, Karen) (Entered: 03/09/2009)
03/09/2009	126	NOTICE OF SERVICE of Expert Report of Dr. Aris K. Silzars on Infringement of AUO's Asserted '781, '160, '157, '506 and '069 Patents by LGD's Accused Products by Au Optronics Corporation, AU Optronics Corporation America, AU Optronics Corporation.(Pascale, Karen) (Entered: 03/09/2009)
03/09/2009	127	NOTICE OF SERVICE of Report of Expert Abbie Gregg Regarding Invalidity of United States Patent Number 6,803,984; Report of Expert Webster Howard, Ph.D. Regarding Invalidity of United States Patent Number 4,624,737; Report of Expert Lawrence Tannas, Jr. Regarding Invalidity of United States Patent Number 7,218,374; Report of Expert Webster Howard, Ph.D. Regarding Invalidity of United States Patent Numbers 5,905,274, 6,815,321, and 7,176,489; Report of Expert Tsu-Jae King Liu, Ph.D. Regarding Invalidity of United States Patent Number 5,019,002; Report of Expert Tsu-Jae King Liu, Ph.D. Regarding Invalidity of United States Patent Number 6,664,569; and Report of Expert Tsu-Jae King Liu, Ph.D. Regarding Invalidity of United States Patent Number 5,825,449 by Au Optronics Corporation, AU Optronics Corporation America, AU Optronics Corporation.(Pascale, Karen) (Entered: 03/09/2009)
05/10/2009	128	Official Transcript of Pretrial Conference held on 05-07-09 before Judge Joseph J. Farnan, Jr. Court Reporter/Transcriber Leonard A. Dibbs. Transcript may be viewed at the court public terminal or purchased through the Court Reporter/Transcriber before the deadline for Release of Transcript Restriction. After that date it may be obtained through PACER (Redaction Request due 6/1/2009., Redacted Transcript Deadline set for 6/10/2009., Release of Transcript Restriction set for 8/10/2009.). (lad) (Entered: 05/10/2009)
05/12/2009	129	MEMORANDUM ORDER Setting Bench Trial between LG and AUO for 6/2/2009 09:30 AM in Courtroom 4B before Judge Joseph J. Farnan, Jr. A second Pretrial Conference is set for 5/20/2009 01:30 PM in Courtroom 4B before Judge Joseph J. Farnan, Jr. (See Order for details). Signed by Judge Joseph J. Farnan, Jr. on 5/12/2009. Associated Cases: 1:06-cv-00726-JJF, 1:07-cv-00357-JJF(dlk) (Entered: 05/12/2009)
05/21/2009	130	Official Transcript of Final Pretrial Conference held on 05-20-09 before Judge Joseph J. Farnan, Jr. Court Reporter/Transcriber Leonard A. Dibbs. Transcript may be viewed at the court public terminal or purchased through the Court Reporter/Transcriber before the deadline for Release of Transcript Restriction. After that date it may be obtained through PACER (Redaction Request due 6/11/2009., Redacted Transcript Deadline set for 6/22/2009., Release of Transcript Restriction set for 8/19/2009.). (lad) (Entered: 05/21/2009)
05/22/2009	131	REDACTED VERSION of (1266 in 1:06-cv-00726-JJF) SEALED MOTION in Limine No. 7 To Preclude LGD's Reliance On Certain Prior Art Products And Foreign Language References by AU Optronics Corporation. (Attachments: # 1 Text of Proposed Order)(Pascale, Karen) (Entered: 05/22/2009)
07/20/2009	--	CORRECTING ENTRY: Official Transcripts of 10 day Bench Trial held in June 2009 (DI 132 thru 141) removed from member case CA 07-357 JJF. For information regarding these transcripts, SEE LEAD CASE CA 06-726 JJF, DI 1366 thru 1375. (rbe) (Entered: 07/20/2009)
06/03/2010	133	NOTICE of Appearance by Colm F. Connolly on behalf of LG Display America Inc., LG Display America, Inc., LG Display America, Inc. (Connolly, Colm) (Entered: 06/03/2010)
06/04/2010	134	MOTION for Pro Hac Vice Appearance of Attorney Kell M. Damsgaard, Thomas B. Kenworthy, and Collin W.

		Park - filed by LG Display America Inc., LG Display Co. Ltd., LG Display America, Inc., LG Display Co., Ltd., LG Display America, Inc.. (Connolly, Colm) (Entered: 06/04/2010)
06/07/2010	135	MOTION for Pro Hac Vice Appearance of Attorney John D. Zele - filed by LG Display America Inc., LG Display Co. Ltd., LG Display America, Inc., LG Display Co., Ltd., LG Display America, Inc.. (Connolly, Colm) (Entered: 06/07/2010)
06/14/2010	--	CORRECTING ENTRY: D.I. 132 was removed from the docket as it was corrected by D.I. 133. (nms) (Entered: 06/14/2010)
07/16/2010	136	PROPOSED Final Judgment ORDER, by AU Optronics Corporation America, Au Optronics Corporation. (Lundgren, Andrew) Modified on 7/19/2010 (nms). (Entered: 07/16/2010)
07/16/2010	137	Letter to The Honorable Joseph J. Farnan, Jr. from Andrew A. Lundgren regarding Proposed Final Judgment Order. (Lundgren, Andrew) Modified on 7/19/2010 (nms). (Entered: 07/16/2010)
08/18/2010	--	Case reassigned to Judge Leonard P. Stark. Please include the initials of the Judge (LPS) after the case number on all documents filed. (rpg) (Entered: 08/18/2010)
09/22/2010	--	SO ORDERED, re (1597 in 1:06-cv-00726-LPS) MOTION for Pro Hac Vice Appearance of Attorney John V. Gorman filed by LG Display Co., Ltd., LG Display America, Inc. Signed by Judge Leonard P. Stark on 9/22/2010. Associated Cases: 1:06-cv-00726-LPS, 1:07-cv-00357-LPS, 1:08-cv-00355-LPS(rpg) (Entered: 09/22/2010)
11/02/2010	138	ORAL ORDER: IT IS ORDERED that counsel are to provide the Court with a joint status report on or before November 9, 2010. ORDERED by Judge Leonard P. Stark on 11/2/10.Associated Cases: 1:06-cv-00726-LPS, 1:07-cv-00357-LPS, 1:08-cv-00355-LPS(ntl) (Entered: 11/02/2010)
11/09/2010	139	Joint STATUS REPORT by LG Display America Inc., LG Display Co. Ltd., LG Display America, Inc., LG Display Co., Ltd., LG Display America, Inc.. (Connolly, Colm) (Entered: 11/09/2010)

US District Court Civil Docket

U.S. District - Wisconsin Western
(Madison)

1:07cv137

Au Optronics Corporation v. Lg.Philips Lcd Co, Ltd

This case was retrieved from the court on Thursday, November 05, 2009

Date Filed:	**03/08/2007**	**Class Code:**	**TERM 05/30/2007**
Assigned To:	**Judge John C Shabaz**	**Closed:**	**Yes**
Referred To:	**Magistrate Judge Crocker**	**Statute:**	
Nature of suit:	**Patent (830)**	**Jury Demand:**	**Yes**
Cause:	**PROPERTY RIGHTS; Patent**	**Demand Amount:**	**$0**
Lead Docket:	**none**	**NOS Description:**	**Patent**
Other Docket:	**None**		
Jurisdiction:	**Federal Question**		

Litigants	Attorneys
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Defendant

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Washington , DC 20006-1108
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Date	#	Proceeding Text
03/08/2007	--	NORTC - FEE PAID.
03/08/2007	1	JS-44
03/08/2007	2	COMPLAINT - SUMMONS ISSUED.
03/08/2007	3	DISCLOSURE OF CORP. AFFIL. & FINAN. INT. BY PLTF.
03/15/2007	4	SUMMONS
03/29/2007	5	NOTICE OF APPEARANCE BY JAMES PETERSON, BRADY WILLIAMSON, GASPARE BONO AND TYLER GOODWYN FOR DEFTS.
03/29/2007	6	MOTION TO DISMISS BY DEFTS.
03/29/2007	7	BRIEF IN SUPPORT OF DEFTS. MOTION TO DISMISS.
03/29/2007	8	AFFIDAVIT OF DONG HOON HAN.
03/29/2007	9	MOTION TO ADMIT GASPARE J. BONO PRO HAC VICE.
03/29/2007	10	MOTION TO ADMIT TYLER GOODWYN PRO HAC VICE.
03/29/2007	11	AFFIDAVIT OF JAMES D. PETERSON IN SUPPORT OF MOTION TO ADMIT GASPARE J. BONO PRO HAC VICE.
03/29/2007	12	AFFIDAVIT OF JAMES D. PETERSON IN SUPPORT OF MOTION TO ADMIT TYLER GOODWYN PRO HAC VICE.
04/02/2007	13	ORDER ADMITTING GASPARE BONO PRO HAC VICE.
04/02/2007	14	ORDER ADMITTING R. TYLER GOODWYN PRO HAC VICE.
04/03/2007	15	MOTION TO ADMIT ATTYS. M.TYLER, B.RANGE, B.DIETZEL, J.CHEN, R.SHULMAN AND S.BAIK PRO HAC VICE.
04/03/2007	16	AFFIDAVIT OF JAMES R. TROUPIS.
04/03/2007	17	DISCLOSURE OF CORP. AFFIL. & FINAN. INT. BY DEFT. LG.PHILIPS LTD.
04/03/2007	18	DISCLOSURE OF CORP. AFFIL. & FINAN. INT. BY DEFT. LG.PHILIPS AMERICA.
04/04/2007	19	ORDER ADMITTING M.TYLER, B.RANGE, B.DIETZEL, J.CHEN, R.SHULMAN AND S.BAIK PRO HAC VICE.
04/16/2007	20	PPTC REPORT BY PLTF.
04/16/2007	21	PPTC REPORT BY DEFTS.
04/16/2007	22	MOTION BY DEFTS. TO TRANSFER TO DISTRICT OF DELAWARE.
04/16/2007	23	BRIEF IN SUPPORT OF DEFTS. MOTION TO TRANSFER TO DISTRICT OF DELAWARE.
04/16/2007	24	AFFIDAVIT OF R.TYLER GOODWYN.
04/17/2007	25	EXHIBIT 1 TO AFFIDAVIT OF DONG HOON HAN FILED 3/29/07.
04/17/2007	26	WAIVER OF SERVICE OF SUMMONS BY DEFT. LG.PHILIPS LTD.
04/18/2007	27	BRIEF IN OPPOSITION BY PLTF. TO DEFTS. MOTION TO DISMISS.
04/18/2007	28	AFFIDAVIT OF DAVID W. PANNECK.
04/18/2007	29	AFFIDAVIT OF MICHAEL LESTINA.
04/19/2007	30	PTC ORDER - AMENDMENTS TO PLEADINGS DUE 5/15/07; DISPOSITIVE MOTIONS DUE 7/30/07.
04/30/2007	31	BRIEF IN REPLY IN SUPPORT OF DEFTS. MOTION TO DISMISS.
04/30/2007	32	AFFIDAVIT OF DONG HOON HAN (SUPPLEMENTAL).
05/02/2007	33	MOTION BY PLTF. TO ADMIT JAMES C. YOON AND JULIE HOLLOWAY PRO HAC VICE.
05/02/2007	34	AFFIDAVIT OF JAMES R. TROUPIS.
05/03/2007	35	ORDER ADMITTING JAMES YOON AND JULIE HOLLOWAY PRO HAC VICE.
05/03/2007	36	BRIEF IN REPLY (CORRECTED) IN SUPPORT OF DEFT. LG PHILIPS LCD AMERICA MOTION TO DISMISS.
05/07/2007	37	BRIEF IN OPPOSITION BY PLTF. TO DEFTS. MOTION TO TRANSFER TO DISTRICT OF DELAWARE.
05/07/2007	38	AFFIDAVIT OF PAUL BARBATO.

05/07/2007	39	AFFIDAVIT OF ARIS K. SILZARS.
05/17/2007	40	BRIEF IN REPLY IN SUPPORT OF DEFTS. MOTION TO TRANSFER TO DISTRICT OF DELAWARE.
05/18/2007	41	MOTION BY PLTF. TO COMPEL DEFT. LG PHILIPS LCD AMERICA TO RESPOND TO REQ. FOR PROD. OF INTERROGS.
05/18/2007	42	BRIEF IN SUPPORT OF PLTF. MOTION TO COMPEL.
05/18/2007	43	AFFIDAVIT OF JAMES R. TROUPIS.
05/18/2007	44	AFFIDAVIT (2ND) OF DAVID W. PANNECK.
05/22/2007	45	BRIEF IN OPPOSITION BY DEFTS. TO PLTF. MOTION TO COMPEL.
05/22/2007	46	AFFIDAVIT OF NICOLE TALBOTT SETTLE.
05/23/2007	--	TELE. MOTION HEARING SET ON #41 FOR 5/30/07, 8:30 AM.
05/24/2007	--	RECD. PROPOSED PROTECTIVE ORDER; FORWARDED TO CHAMBERS.
05/29/2007	47	JOINT RULE 26 REPORT.
05/30/2007	48	PROTECTIVE ORDER
05/30/2007	49	ORDER TRANSFERRING CASE TO DISTRICT OF DELAWARE.
06/01/2007	--	RECORD SENT TO DISTRICT OF DELAWARE.
07/21/2008	--	Further docketing is in CM/ECF at pacer.wiwd.uscourts.gov

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,697	03/16/2010	6689629	7773.0084	5947

24504 7590 01/06/2011

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
600 GALLERIA PARKWAY, S.E.
STE 1500
ATLANTA, GA 30339-5994

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 01/06/2011

Please find below and/or attached an Office communication concerning this application or proceeding.

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(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

SONG K. JUNG

MCKENNA LONG AND ALDRIDGE LLP

1900 K STREET, NW

WASHINGTON, DC 20006

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,697*.

PATENT NO. *6689629*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	Control No. 90/009,697	Patent Under Reexamination 6689629	
	Examiner TUAN H. NGUYEN	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a☒ Responsive to the communication(s) filed on *16 March 2010* . b☐ This action is made FINAL.
c☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire _____ month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☒ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☒ Claims *1-16* are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims _____ are patentable and/or confirmed.
4. ☒ Claims *1-16* are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a)☐ approved (7b)☐ disapproved.
8. ☒ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   1☐ been received.
   2☐ not been received.
   3☒ been filed in Application No. *10/068,500* .
   4☐ been filed in reexamination Control No. _____.
   5☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

DETAILED ACTION

Reexamination

Summary of Proceedings

A Request pursuant to 37 CFR 1.510 for ex parte reexamination of the US Patent Number 6,689,629 (the '629 patent) issued to Tsujimura et al. was filed on March 16, 2010 by the Third party Requester. An Order granting ex parte reexamination of the base patent was mailed on April 22, 2010. The Order stated that there was a substantial new question of patentability affecting claims 1-16 of the '629 patent.

Status of claims

The following is the status of the claims with respect to the Request:

Claims 1-16 are reexamined in view of the following prior art submitted by the third party requesters. Of these, claims 1, and 9 are independent claims.

References cited by the Requester

1. U.S. Patent No. 6,163,356 to Song et al. (hereinafter "Song").
2. U.S. Patent No. 5,850,275 to Watanabe et al. (hereinafter "Watanabe '275").
3. U.S. Patent No. 6,862,069 to Kwak et al. (hereinafter "Kwak").
4. U.S. Patent No. 5,995,189 to Zhang (hereinafter "Zhang").
5. U.S. Patent No. 6,157,430 to Kubota et al. (hereinafter Kubota).
6. EP 0 887 695 A2 to Hirabayashi (hereinafter "Hirabayashi").

7. JP 10-333151 to Yamamoto et al. (hereinafter "Yamamoto").

8. JP 10-82909 to Harada et al. (hereinafter"Harada").

9. JP 6-82811 to Watanabe et al. (hereinafter "Watanabe").

10. JP 9:197415 to Miyashita et al. (hereinafter "Miyashita").

11. JP Pub. No. 2000-098909 to Tomoyuki (hereinafter Tomoyuki).

Claim Rejections - Relevant statutes

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Detailed Analysis

Claims 1-5, 7-13, 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirabayashi.

Regarding claims 1, 9:

Hirabayashi, Fig. 1, col.1:1-7 discloses an array substrate for a liquid crystal display and method of forming an array substrate comprising the steps of forming a layer of insulating substrate having an area; forming a thin film transistor array on the insulating substrate (col. 31:16-23); a plurality of wiring 7 arranged on the insulating substrate in communication with at least one of the transistors in the thin film array; each connection pads 26 contacting the opposite end of the plurality of wiring (Fig. 2, Fig. 5, Lin, Fig. 10, Col. 14:16-20); pixel electrodes 20 (Fig. 1, col. 4:6-7), and forming dummy conductive patterns that are located between connection pads 26 and the pixel electrodes 20, and are not in contact with any of the wirings (Fig. 1, 4-6 shown in hatch pattern, col. 11:35-42, paragraph bridging col. 11-12, col. 12:35-42, col. 18:52-54). The dummy conductive patterns comprise well over 30% of various selected areas.

Regarding claims 2-5, 10-13:

Hirabayashi, col. 16:19-22 discloses that the wiring can comprise at least an upper layer and a lower layer of conductive materials wherein the lower layer is of aluminum and the upper layer is of titanium nitride.

Regarding claims 7-8, 15-16:

Hirabayashi teaches the use titanium nitride which is the same material for forming the upper wiring; therefore, it inherently does not become insoluble in an acid or alkaline etchant.

Claims 2-8, 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi in view of the '626 APA.

Hirabayashi discloses substantially the claimed array substrate for a liquid crystal display and method of forming an array substrate as noted above accept the use of two-layer structure of aluminum as a lower conductive material, and a material such as molybdenum, chromium, tantalum, titanium as an upper conductive material for wiring.

The '626 APA, col. 1:26-39 discloses a lower layer wiring material of aluminum and an upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have formed wiring having upper layer selected from the group consisting of molybdenum, chromium, tantalum, titanium over lower aluminum layer as suggested by the '626 APA in Hirabayashi since the harder to be oxidized material from the upper layer would protect the aluminum from oxidation.

Claims 1-5, 7-13, 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang.

Regarding claims 1-5, 7-13, 15-16: The proposed rejections **are adopted** as proposed. The Examiner incorporates by reference the detailed explanation of the manner of applying the Applicant admitted prior art as recited in claim chart CC-21 of the Request.

Other References Submitted by the Requester

Other references submitted by Requester, for example, Kwak, Song, Kubota, Yamamoto, Harada, Watanabe '811, Miyashita, and Tomoyuki are relevant; however, additional rejections based on them would be redundant and unnecessary at this time.

CONCLUSION

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that ex parte reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in ex parte reexamination proceedings are provided for in 37 CFR 1.550(c).

Amendment in Reexamination Proceedings

Patent owner is notified that any proposed amendment to the specification and/or claims in this reexamination proceeding must comply with 37 CFR 1.530(d)-(j), must be formally presented pursuant to 37 CFR 1.52(a) and (b), and must contain any fees required by 37 CFR 1.20(c). See MPEP § 2250(IV) for examples to assist in the preparation of proper proposed amendments in reexamination proceedings.

Submissions

In order to insure full consideration of any amendments, affidavits or declarations or other documents as evidence of patentability, such documents must be submitted in response to the first Office action on the merits (which does not result in a close of prosecution). Submissions after the second Office action on the merits, which is intended to be a final action, will be governed by the requirements of 37 CFR 1.116, after final rejection and by 37 CFR 41.33 after appeal, which will be strictly enforced.

Notice Regarding Certain Reexamination Issue

The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 6,689,629 throughout the course of this reexamination proceeding. The requester is also reminded of the ability to similarly appraise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

Notice Re Patent Owner's Correspondence Address

Effective May 16, 2007, 37 CFR 1.33(c) has been revised to provide that:

The patent owner's correspondence address for all communications in an *ex parte* reexamination or an *inter partes* reexamination is designated-as the correspondence address of the patent. *Revisions and Technical Corrections Affecting Requirements for Ex Parte and Inter Partes Reexamination*, 72 FR 18892 (April 16, 2007)(Final Rule)

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of this revision to 37 CFR 1.33(c), automatically changed to that of the patent file as of the effective date.

This change is effective for any reexamination proceeding which is pending before the Office as of May 16, 2007, including the present reexamination proceeding, and to any reexamination proceeding which is filed after that date. Parties are to take this change into account when filing papers, and direct communications accordingly.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of change of Correspondence Address in the reexamination proceeding and/or the patent

(depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone numbers for reexamination inquiries:

Reexamination and Amendment practice

(571) 272-7703

Central Reexam Unit (CRU)

(571) 272-7705

Reexamination Facsimile Transmission No.

(571) 272-9900

All correspondence relating to this *ex parte* reexamination proceeding should be directed:

By Mail to: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Registered users of EFS-Web may alternatively submit such correspondence via the electronic filing system EFS-Web, at https://sportal.uspto.gov/authenticate/authenticateuserlocalepf.html. EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are "soft scanned" (i.e., electronically uploaded) directly into the official file for the reexamination proceeding, which offers parties the opportunity to review the content of their submissions after the "soft scanning" process is complete.

Any inquiry concerning this communication should be directed to Tuan Nguyen at telephone number 571-272-1694

Signed:

Tuan H. Nguyen
Primary Examiner
Central Reexamination Unit
Art Unit 3992

Conferees:

Sue Lao

Minh Nguyen

FEB 26 2010

CENTRAL REEXAMINATION UNIT

PTO/SB/08a/b (05-03)
Approved for use through 05/31/2003. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449/PTO

LIST OF REFERENCES CITED IN THE REQUEST

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Control Number	90/009,614
Filing Date	February 26, 2010
First Named Inventor	Tsujimura et al.
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	7773.084.60

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	6,163,356	12-19-2000	In-Duk Song et al.	
	AB	5,850,275	12-15-1998	Makoto Watanabe et al.	
	AC	6,862,069	03-01-2005	Dong Yeung Kwak et al.	
	AD	5,995,189	11-30-1999	Hongyong Zhang	
	AE	6,157,430	12-05-2000	Takeshi Kubota et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	BA	EP 0 887 695 A2	12-30-1998	Seiko Epson Corporation		
	BB	JP 10-333151 (with English translation)	12-18-1998	Matsushita Denki Sangyo K.K.		
	BC	JP 10-82909 (with English translation)	03-31-1998	Dainippon Printing Co., Ltd.		
	BD	JP 6-82811 (with English translation)	03-25-1994	Toshiba Corp.		
	BE	JP 9-197415 (with English translation)	07-31-1997	Casio Computer Co., Ltd.		

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the application number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature	/Tuan Nguyen/ (12/27/2010)	Date Considered	

DC:50680289.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /TN/

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	90009697
Filing Date	2010-03-16
First Named Inventor	Tsujimura
Art Unit	3992
Examiner Name	
Attorney Docket Number	250129-1080

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2000098909	JP	A	2000-04-07	Sanyo Electric Co. Ltd.		☐
	2	02-189922	JP	A	1990-07-25	NEC Corp.		☐
	3	05-061072	JP	A	1993-03-12	Hitachi Ltd.		☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /TN/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	90009697
	Filing Date	2010-03-16
	First Named Inventor	Tsujimura
	Art Unit	3992
	Examiner Name	
	Attorney Docket Number	250129-1080

	4	10-090706	JP	A	1998-04-10	Toshiba Corp.		☐
	5	10-240150	JP	A	1998-09-11	Samsung Electron Co. Ltd.		☐
	6	10-282528	JP	A	1998-10-23	LG Electron Inc.		☐
	7	11-242211	JP	A	1999-09-07	Sharp Corp, Sony Corp.		☐
	8	11-153816	JP	A	1999-06-08	Citizen Watch Co. Ltd.		☐
	9	09-146097	JP	A	1997-06-06	Sharp Corp., UK Government		☐

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	Japanese Language Office Action dated December 26, 2008 and English translation of Office Action.	☐
	2	Japanese Language Office Action dated May 12, 2009 and English translation of Office Action.	☐
	3	Japanese Language Appeal Decision dated January19, 2006 and English translation of Appeal Decision.	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	90009697
	Filing Date	2010-03-16
	First Named Inventor	Tsujimura
	Art Unit	3992
	Examiner Name	
	Attorney Docket Number	250129-1080

EXAMINER SIGNATURE			
Examiner Signature	/Tuan Nguyen/ (12/27/2010)	Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /TN/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90009697	6689629
	Examiner	Art Unit
	TUAN H NGUYEN	3992

SEARCHED			
Class	Subclass	Date	Examiner
None		12/17/10	TN

SEARCH NOTES		
Search Notes	Date	Examiner
Reviewed of patented file's prosecution history	4/16/10	TN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Reexamination	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90009697	6689629
	Certificate Date	Certificate Number

Requester Correspondence Address: ☐ Patent Owner ☒ Third Party
SONG K. JUNG MCKENNA LONG AND ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006

LITIGATION REVIEW ☒	TN (examiner initials)	01/03/2011 (date)
Case Name		Director Initials
Open 1:07cv357 Au Optronics Corp. v. Lg. Philips Lcd Co Ltd et al		
Closed 1:07cv137 Au Optronics Corp. v. Lg. Philips Lcd Co. Lt		

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	NUMBER
1. None	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:		90/009,697
Filing Date	:	03-16-2010
Applicant	:	Takatoshi Tsujimura et al. 66/89629
Assignee	:	AU Optronics Corp.
Art Unit	:	3992
Examiner	:	NGUYEN, TUAN H

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

REVOCATION OF POWER OF ATTORNEY
WITH NEW POWER OF ATTORNEY
AND
CHANGE OF CORRESPONDENCE ADDRESS

Dear Sir:

The undersigned hereby revokes any and all previous powers of attorney in the above-identified application.

The undersigned hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Justin I. King, Registration No. 50,464, and
Practitioners associated with the Customer Number: 65358

The undersigned also requests that all future communications with respect thereto from the Patent and Trademark Office be directed to address associated with the above Customer Number.

Please also change the attorney docket Number of this matter to

I am the
☐ Applicant/Inventor
☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.

SIGNATURE of Applicant or Assignee of Record			
Signature	Kai Ti Chen		
Name	Kai-Ti Chen	Date	2011. 2. 23

Note: Signature of all the inventors or assignees of record of the entire interest or their representative(s) are required.

PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Takatoshi Tsujimura et al.

Application No./Patent No.: 90/009,697 Filed/Issue Date: 03-16-2010

Titled: ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

AU OPTRONICS CORPORATION , a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy therefore is attached.

OR

B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

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The document was recorded in the United States Patent and Trademark Office at
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2. From: TSUJIMURA, TAKATOSHI et al. To: INTERNATIONAL BUSINESS MACHINES CO

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Justin King/ 02/23/2011

Signature Date

Justin King Attorney on record

Printed or Typed Name Title

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	9500821
Application Number:	90009697
International Application Number:	
Confirmation Number:	5947
Title of Invention:	ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE
First Named Inventor/Applicant Name:	6689629
Customer Number:	24504
Filer:	Anthony King/Justin King
Filer Authorized By:	Anthony King
Attorney Docket Number:	7773.0084
Receipt Date:	23-FEB-2011
Filing Date:	16-MAR-2010
Time Stamp:	11:33:42
Application Type:	Reexam (Third Party)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA.pdf	144024 9ae1e9c8cd4ecaeebcf638471b85eb80bb94d095	no	1

Warnings:	
Information:	

2	Power of Attorney	sb0096.pdf	427313 ac221b702e1bbefea9a7321132d034899a7918d5	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	571337

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

CONFIRMATION NO. 5947

Bib Data Sheet

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
90/009,697	03/16/2010 RULE	438	3992	7773.0084

APPLICANTS

6689629, Residence Not Provided;
INTERNATIONAL BUSINESS MACHINES CORPORATION, ARMONK, NY;
SONG K. JUNG (3RD PTY REQ.), WASHINGTON, DC;
MCKENNA LONG & ALDRIDGE, LLP, WASHINGTON, DC

**** CONTINUING DATA ***************************

This application is a REX of 10/068,500 02/05/2002 PAT 6,689,629

**** FOREIGN APPLICATIONS *********************

JAPAN 2001-029587 02/06/2001

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed	☐ yes ☐ no				
35 USC 119 (a-d) conditions met	☐ yes ☐ no ☐ Met after Allowance			16	2
Verified and Acknowledged	Examiner's Signature Initials				

ADDRESS
65358

TITLE
ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

FILING FEE RECEIVED		
2520	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
90/009,697	03/16/2010	6689629	7773.0084

CONFIRMATION NO. 5947

POWER OF ATTORNEY NOTICE

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NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/23/2011.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/rbell/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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90/009,697	03/16/2010	6689629	7773.0084

CONFIRMATION NO. 5947

POA ACCEPTANCE LETTER

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Date Mailed: 03/01/2011

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/23/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/rbell/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

Appl No.:	**90/009,697**
Applicant:	**Takatoshi Tsujimura**
Filing Date:	**03-16-2010**
Art Unit:	**3992**
Examiner:	**Nguyen, Tuan H.**
Attorney Docket No.:	**67507-008Re-exam**

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ATTN: Central Reexamination Unit
P.O. Box 1450
Alexandria, Virginia 22313-1450

RESPONSE TO OFFICE ACTION
IN EX PARTE REEXAMINATION

Sir:

This paper responds to the Office Action dated January 06, 2011. Please amend the above–identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

What is claimed is:

1. (Original) An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;

connection pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

2. (Original) The array substrate for display according to claim 1 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

3. (Original) The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.

4. (Original) The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

5. (Original) The array substrate for display according to claim 3 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

6. (Original) The array substrate for display according to claim 5 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

7. (Original) The array substrate for display according to claim 4 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

8. (Original) The array substrate for display according to claim 5 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

9. (Original) A meted for forming an array substrate for display, comprising: forming a layer of an insulating substrate, having an area; forming a thin film transistor array formed on the insulating substrate, each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;

forming connection pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

10. (Original) The method for forming an array substrate for display according to claim 9 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

11. (Original) The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring materials is selected from the group consisting of aluminum and aluminum alloys.

12. (Original) The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

13. (Original) The method for forming an array substrate for display according to claim 11 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and allays thereof.

14. (Original) The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

15. (Original) The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

16. (Original) The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

REMARKS/ARGUMENTS

This is a full and timely response to the outstanding non-final Office Action mailed January 6, 2011. The Examiner is thanked for the thorough reexamination of the present application. Upon entry of this response, claims 1-16 are pending in the present application. Claims 1 and 9 have been amended to address minor typographical errors. In response to the rejections set forth in the Office Action, the owners of U.S. Patent No. 6,689,629 (hereinafter "Patentees") respectfully request consideration of the following remarks contained herein.

Claim Status Summary

Claims 1-5, 7-13, and 15-16 are rejected under 35 U.S.C. §102(b), as being anticipated by Hirabayashi.

Claims 1-5, 7-13, and 15-16 are rejected under 35 U.S.C. §102(b), as being anticipated by Zhang.

Claims 2-8 and 10-16 are rejected under 35 U.S.C. §103(a), as being unpatentable over Hirabayashi in view of the '626 APA.

35 U.S.C. §102(b)

Claims 1-5, 7-13, and 15-16 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by *Hirabayashi* (EP Patent No. 0887695). Claims 1-5, 7-13, and 15-16 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by *Zhang* (U.S. Patent No. 5,995,189). For at least the reasons set forth below, Patentees traverse these rejections.

The 35 U.S.C. §102(b) states the following:

"A person shall be entitled to a patent unless

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States"

As indicated in MPEP 2131, to anticipate a claim, the cited reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631 (MPEP § 2131). As can be gleaned from the cited case law, the requirement is that each element must be either expressly or inherently described.

A. Claims 1-5, 7, and 8 are Patentable over *Hirabayashi*

Patentees respectfully submit that independent claim 1 is patentable over *Hirabayashi* for at least the reason that *Hirabayashi* fails to disclose, teach, or suggest the features emphasized below in claim 1. The claim 1 recites the following limitations:

> "An array substrate for display, comprising:
>
> a layer of an insulating substrate, having an area;
>
> a thin film transistor array formed on the insulating substrate;
>
> a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;
>
> ***connection pads, each connection pad contacting the first end of at most one of the plurality of wirings***;
>
> pixel electrodes, and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring."

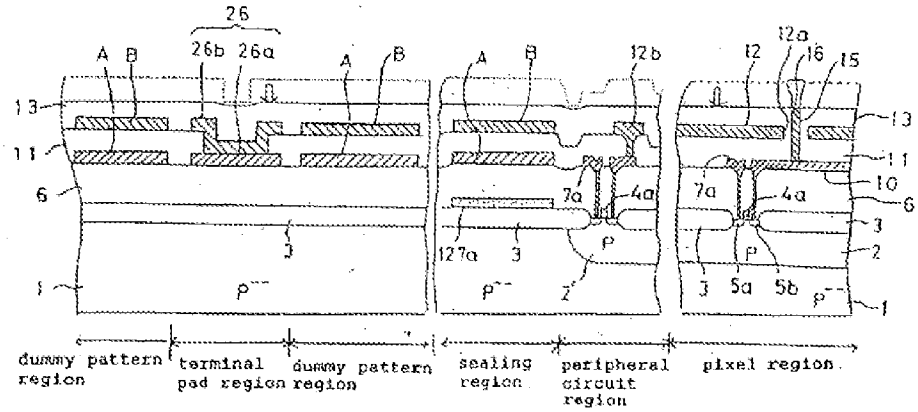
Patentee respectfully submits that Hirabayashi does not disclose the recited structural arrangement for the connection pads. The claim 1 recites that "a plurality of

wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array", and the claim 1 further recites that "connections pads, each connection pad contacting the first end of at most one of the plurality of wirings". In particular, Patentee respectfully submits that Hirabayashi does not discloses the recited "connections pads, each connection pad contacting the first end of **at most one** of the plurality of wirings".

For the connection pads in claim 1, the Office cites the terminal pad 26 depicted in various figures of the *Hirabayashi* reference. The Office alleged that "*Hirabayashi . . . discloses . . . each connection pads 26 contacting the opposite end of the plurality of wiring (Fig. 2, Fig. 5, Lin, Fig. 10, Col. 14:16-20) . . . .*" (Office Action, page 4, center paragraph, lines 4-7). Patentee respectfully disagrees.

Hirabayashi discloses an electro-optical device substrate. Hirabayashi's figure 2 discloses a connection pad 26 with a padding structure. Hirabayashi's figure 6 discloses that the connection pad 26 contacts lines L/Lin. Hirabayashi's figure 5 further disclose that the lines L/Lin were connected to the data line driver 21 (column 20, lines 41-55) not to any of transistor of the thin film array. Hirabayashi discloses that the data line driver 21 supplies signals to the image signal sampling circuit 24 (Hirabayashi, column 14, lines 16-22).

Patentees respectfully submit that the "each connection pad 26 contacting the opposite end of the plurality of wirings" explicated stated by the Office is not the recited limitation of "connection pads, each connection pad contacting the first end of ***at most <u>one</u>*** of the plurality of wirings". FIG. 2 of the *Hirabayashi* reference is reproduced below:



In the related text describing FIG. 2, *Hirabayashi* teaches that the reflective liquid crystal panel substrate 131 includes a plurality of terminal pads 26 arranged along the bottom end and adhesively connected to a flexible tape wiring with an anisotropic conductive film therebetween. A data line driver circuit(X driver) 21 lying between the terminal pad array 26 and the bottom side of the sealing region 127 supplies sampling signals to the image signal sampling circuit 24. (*Hirabayashi*, col. 14, lines 16-22). *Hirabayashi*, however, fails to disclose that the terminal pads 26 are in contact with the first end of at most ***one*** of the plurality of wirings. Reference is made to FIG. 6 below, which depicts how the terminal pad 26 is interconnected to other components:

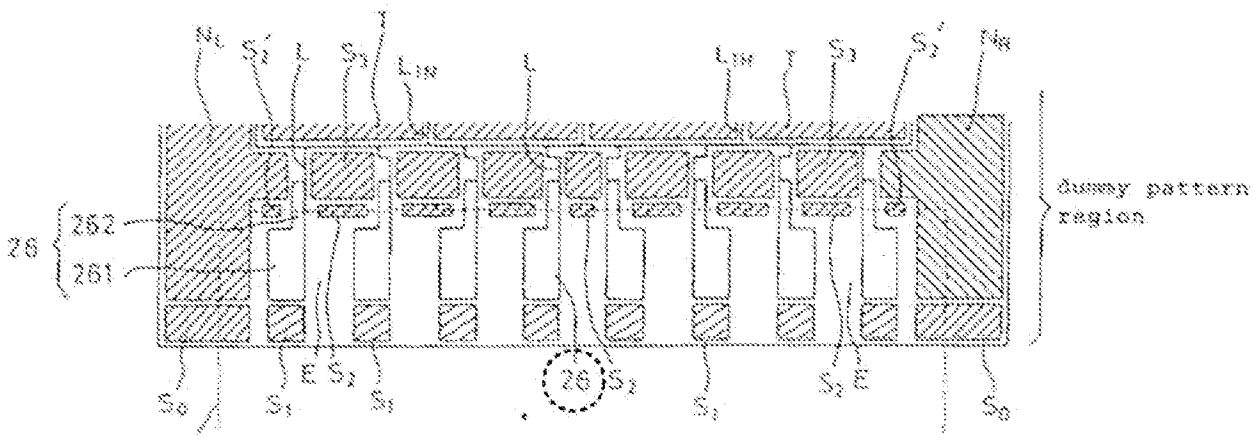
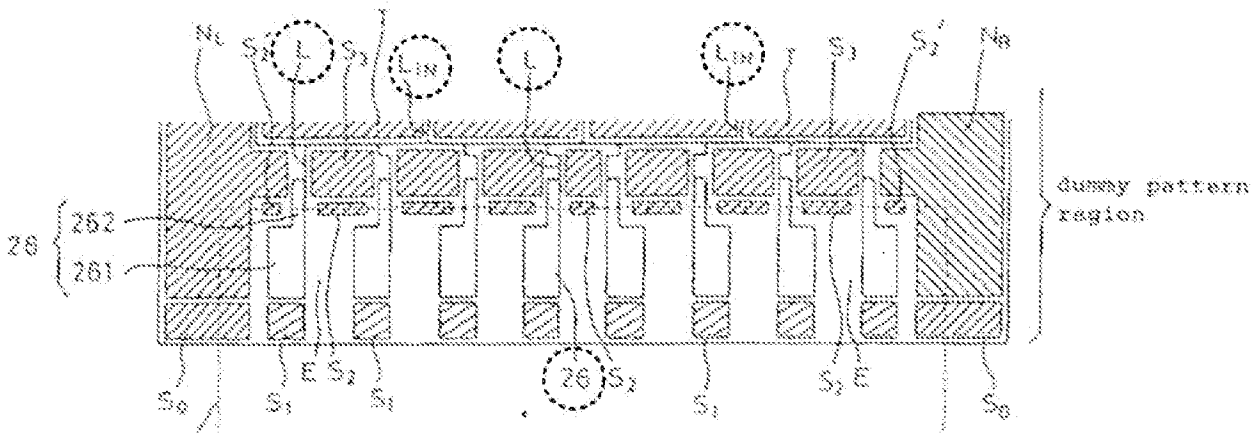


FIG. 6 provides a partial plan view near the terminal pads in the reflective liquid crystal panel substrate in Embodiment 1. As depicted above, the terminal pad 26 is not

in contact with <u>at most one</u> of the plurality of wirings, as required in claim 1. Rather, as clearly depicted in the marked-up figure below, the terminal pad 26 is in contact with a <u>plurality</u> of wirings (*e.g.*, wirings L and wirings L_{IN}).



This is further supported in the related text for FIG. 6, where Hirabayashi, column 20, lines 41-55, explicitly teaches the following: As shown in Fig. 6, there are two types of wirings extending from the region of the input terminal pads 26 to the interior of the substrate, that is, **<u>wirings LIN</u>** for inputting signals (DXIN (data signals), power source Vddx and Vssx, clock signals and inverted clock signals) to the data line driver circuit 21, and wirings for inputting signals (DYIN (data signals), power source Vddy and Vssy, clock signals and inverted clock signals) to the gate line driver circuits 22R and 22L and the precharging/testing circuit 23. Hence the **<u>wirings L</u>** *<u>extracted from the input terminal pads 26</u>* towards the column direction (vertical direction in the drawing) **<u>are divided into the wirings LIN</u>** directed to the data line driver circuit 21 **<u>and the other wirings</u>** in the wiring region in the line direction (transverse direction in the drawing). Thus, the input terminal pads 26, a plurality of isolated rectangular divisional dummy patterns S1 to S3 formed between the input wirings, and isolated rectangular interwiring dummy patterns T, formed between the wirings LIN for input to the data line driver circuit 21, lie in the interposed region Y between the region of the input terminal pads 26 and the data line driver circuit 21. In Fig. 6, the number of the shown input terminal pads 26 is reduced.

Patentee t thus respectfully submits that, as shown in the Hirabayashi's figure 6, Hirabayashi does not disclose the connections pad 26 contacting the first end of **at most one** of the plurality of wirings as recited in the claim 1. In fact, Hirabayashi's figure 6 shows that each connection pad 26 connects to a plurality of wirings Lin which go to the data line driver 21. Since Hirabayashi's wirings Lin are connected to the data line driver 21, Hirabayashi's wirings Lin do not connect to any of the transistor of the thin film array. Therefore, Hirabayashi not only fails disclosing the connection pad contacting the first end of at most one of the plurality of wirings, Hirabayashi also fails discloses recited wirings that connection pad should be contacting to.

Hence, Patentee respectfully submits that Hirabayashi does not disclose or teach that the recited limitation of "connections pads, each connection pad contacting the first end of at most one of the plurality of wirings". And for the reason discussed above, Patentee respectfully submits that the cited reference Hirabayashi does not disclose every recited limitation in the claim 1 as required under 35 USC 102(b); hence, Patentee respectfully requests the Office to withdraw the rejection over claim 1 accordingly, and to issue favorable re-consideration.

Claims 2-5 and 7-8 depend on claim 1; thus they incorporate every recited limitation in claim 1. For the same reasons stated above, Applicant respectfully requests the Office to withdraw the rejection over the claims 2-5 and 7-8, and to issue favorable re-consideration.

B. Claims 9-13, 15, and 16 are Patentable over *Hirabayashi*

Patentees respectfully submit that independent claim 9 is patentable over *Hirabayashi* for at least the reason that *Hirabayashi* fails to disclose, teach, or suggest the features emphasized below in claim 9. Claim 9 recites the following limitations:

"A method for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array formed on the insulating substrate, each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;

forming connection pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring."

The claim 9 was rejected along with the claim 1. As claim 9 recites a similar limitation relating to the connection pads where each connection pad contacts the first end of at most one of the plurality of wirings, Patentees submit that claim 9 is patentable over *Hirabayashi* for reasons similar to those discussed above in connection with claim 1. Dependent claims 10-13, 15, and 16 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

C. Claims 1-5, 7, and 8 are Patentable Over *Zhang*

Claims 1-5, 7-13, and 15-16 are rejected under 35 U.S.C. §102(b), as being anticipated by Zhang. Patentees respectfully submit that independent claim 1 is patentable over *Zhang* for at least the reason that *Zhang* fails to disclose, teach, or suggest the features emphasized below in claim 1. Claim 1 recites the following limitations:

"An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;

connection pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring."

The Office incorporates by the reference the claim chart provided in Appendix CC21 of the Ex Parte Request by Third Party Requester. For the connection pads in claim 1, the Office adopts the Requester's position that these structural components are disclosed by *Zhang* in col. 1, lines 45-47; col. 6, lines 51-60, FIGs. 1 and 16-17. In the Request, the Requester asserted that "*Zhang discloses that the signal lines 2 and scan lines 3 also connect to extension terminals 6.*" (Ex Parte Request by Third Party submitted February 26, 2010, Appendix CC21). The adopted rejection seems to equal the extension terminal 6 to the recited connections pads. Patentees respectfully disagree with the rejection, and Patentee respectfully submits that the disclosed extension terminal 6 is not the recited connections pads.

FIG. 1 in *Zhang* is a front view showing the outline of an element substrate of an active matrix type liquid-crystal display device, while FIG. 16-17 provide a top view showing a liquid crystal display in accordance with conventional examples. *Zhang,* Column 6, lines 51-60, teaches the following in connection with FIG. 1:On the right and bottom sides of the paper surface, the signal lines 105 and the scanning lines 106 extend to the exterior of the sealing material formation region 107 so as to be connected to a control circuit outside of the panel, or the like. Furthermore, an external terminal 108 is disposed on the element substrate 101, and the external terminal 108 is connected with

the signal line drive circuit 103 and the scanning line drive circuit 104 through wirings 109, respectively.

As set forth in the passage above, *Zhang* teaches that signal lines 105 and scanning lines 106 extend to the exterior of the sealing material formation region 107. There is no mention, however, of connection pads in the figure, and it is not clear from the Requester's claim chart where connection pads are disclosed in this passage. Even assuming, for the sake of argument, that the external terminal 108 in FIG. 1 could be construed as "connection pads," *Zhang's* FIG. 1 fails to show the external terminal 108 contacting the first end of at most one of the plurality of wirings, as required in claim 1.

In fact, the adopted rejection appears to rely on a totally different section of *Zhang* to allegedly disclose this connection to the first end of at most one of a plurality of wirings. Specifically, the adopted rejection relies on col. 1, lines 45-47 found in the Background section where *Zhang* describes a conventional active matrix liquid crystal panel in connection with FIG. 16. Col. 1, lines 45-47 states the following: The ends of those wirings form extension terminals 6 as they are, and the extension terminals 6 are connected with a peripheral drive circuit not shown.

In the passage above, *Zhang* teaches that the extension terminals 6, which the adopted rejection apparently equates to the connection pads of claim 1, are connected to the ends of wirings. Based on the combination of this passage and the passage cited above (col. 6, lines 51-60), the adopted rejection contends that *Zhang* teaches "connection pads, each connection pad contacting the first end of at most one of the plurality of wirings." Patentees respectfully disagree with this rejection.

As is well established in the law, the Office must consider the claims as a whole. *Net MoneyIN, Inc. v. Verisign, Inc. et al.*, CAFC No. 07-1565; October 20, 2008 (Fed. Cir. 2008) (the hallmark of anticipation is prior invention, the prior art reference - in order to anticipate under 35 U.S.C. § 102 - must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements

"arranged as in the claim." *Connell v. Sears*, Roebuck & Co., 722 F.2d 1542, 1548 (Fed. Cir. 1983)). "The identical invention must be shown in as complete detail as is contained in the … claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

In the instant adopted rejection, Patentees respectfully submits that not only the FIG. 16 fails discloses the extension terminal 6 in the structure of connection pad, the adopted rejection also improperly combines the teachings related to two completely different configurations (a conventional liquid crystal display and the new liquid crystal display structure disclosed by *Zhang*). Patentee respectfully submits that Zhang only discloses the extension terminal 6 as the end tip of the wiring; Zhang does not explicitly disclose any padding structure. Patentees further respectfully submits that in the Summary of the Invention section, *Zhang* emphasizes that "[t]he present invention has been made to eliminate the above problems with the conventional devices." (Emphasis added; col. 3, lines 17-18). The adopted rejection appears to rely on two unrelated teachings within a single reference to disclose every feature recited in claim 1. As set forth in Appendix CC21 of the Request, the Requester relies on a combination of FIGS. 1 and 16-17 to allegedly disclose a majority of the features recited in claim 1, as shown in Requester's claim chart below:

CLAIM 1	PRIOR ART DISCLOSURE – ZHANG
An array substrate for display, comprising:	Zhang discloses a liquid crystal display device. See, e.g., Zhang, Title, Figs. 1 and 16-17.
a layer of an insulating substrate, having an area;	Zhang discloses a substrate 1 made of glass or quartz, including an area. See, e.g., Zhang, 1:35-36, Figs. 1 and 16-17.
a thin film transistor array formed on the insulating substrate;	Zhang discloses scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines. See, e.g., Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17.
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Zhang discloses scan lines 2 and signal lines 3 and are connected to the TFTs. See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17.
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Zhang discloses that the signal lines 2 and scan lines 3 also connect to extension terminals 6. See, e.g., Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17.
pixel elecurodes, and	Zhang discloses a pixel section 12. See, e.g., Zhang, Figs. 1 and 16-17.
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Zhang discloses dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals. See, e.g., Zhang, Figs. 4, 8 and 16. Further, the dummy wirings are not in contact with the wiring. Zhang also discloses that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, 10:7-17. Thus, the dummy patterns would comprise at least 30% of the area.

The Board has held that the reference must "*clearly and unequivocally* disclose the claimed compound or direct those skilled in the art to the compound without any need for *picking, choosing, and combining various combining various disclosures*" (*In re Arkley*, 455 F.2d 586, 587, 172 U.S.P.Q. 524,526). Patentees respectfully submit that *Zhang* fails disclosing each of the elements as arranged in claim 1.

Accordingly, Patentees respectfully submit that independent claim 1 is patentable over *Zhang* for at least the reason that *Zhang* fails to disclose, teach, or suggest the highlighted features in claim 1 above. Patentees submit that dependent claims 2-5, 7, and 8 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

D. Claims 9-13, 15, and 16 are Patentable Over *Zhang*

Patentees respectfully submit that independent claim 9 is patentable over *Zhang* for at least the reason that *Zhang* fails to disclose, teach, or suggest the features emphasized below in claim 9.

Claim 9 recites:

"A method for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array formed on the insulating substrate, each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;

forming connection pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring."

As claim 9 recites a similar limitation relating to the connection pads where each connection pad contacts the first end of at most one of the plurality of wirings, Patentees submit that claim 9 is patentable over *Zhang* for reasons similar to those discussed above in connection with claim 1. Dependent claims 10-13, 15, and 16 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

35 U.S.C. §103(a)

Claims 2-8 and 10-16 are rejected under 35 U.S.C. §103(a), as being unpatentable over Hirabayashi in view of the '626 APA. Applicant respectfully disagrees for the reasons discussed below.

The 35 U.S.C. §103(a) states the following:

> "(a) A patent may not be obtained though the invention is not identically disclosed or described as set for the in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be nagatived by the manner in which the invention was made."

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

For a proper rejection of the claim under 35 U.S.C. §103, the cited combination of references must disclose, teach, or suggest all elements / features of the claim at issue. See, e.g., *In re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

Claims 2-8 and 10-16 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over *Hirabayashi* in view of *'629 APA*. Patentees respectfully submit that independent claim 1 (from which claims 2-8 depend) and independent 9 (from which claims 10-16 depend) are patentable over *Hirabayashi* in view of *'629 APA* as *'629 APA* fails to address the deficiencies expressed above in connection with *Hirabayashi*. Dependent claims 2-8 and 10-16 are therefore allowable for at least the reason that these claims depend from allowable independent claims. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

Conclusion

Claims 1-16 are pending in this application. In view of the reasons stated above, Applicant respectfully submits that the independent claims patentably define the present invention over the citations of record, and Applicant respectfully requests a favorable reconsideration and issuing allowance accordingly. Further, the dependent claims should also be allowable for the same reasons as their respective base claims and further due to the additional features that they recite. Separate and individual consideration of the dependent claims is respectfully requested. Examiner is invited to contact the attorney on record to expedite the prosecution in pursuance of allowance.

Respectfully submitted,
WPAT, P.C.

By___/Justin I. King/_____
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March 6, 2011
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Electronic Acknowledgement Receipt

EFS ID:	9599714
Application Number:	90009697
International Application Number:	
Confirmation Number:	5947
Title of Invention:	ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE
First Named Inventor/Applicant Name:	6689629
Customer Number:	65358
Filer:	Anthony King/Justin King
Filer Authorized By:	Anthony King
Attorney Docket Number:	67507-008Re-exam
Receipt Date:	07-MAR-2011
Filing Date:	16-MAR-2010
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Application Type:	Reexam (Third Party)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Reexam Certificate of Service	certificate_of_service_OAR.pdf	3830 e3e644616ac3b521161a46e40bbaacedea51a626	no	1

Warnings:	
Information:	

2		OARV1.pdf	250201 aecb3235c310dfa58d1eafcb24a8a55b3db74ded	yes	18

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Claims	2	4
Applicant Arguments/Remarks Made in an Amendment	5	18

Warnings:	
Information:	
Total Files Size (in bytes):	254031

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IN THE UNITED STATES PATENET AND TRADEMARK OFFICE

Application No.:		90/009,697
Filing Date	:	03-16-2010
Applicant	:	Takatoshi Tsujimura
Assignee	:	AU Optronics Corp.
Art Unit	:	3992
Examiner	:	Nguyen, Tuan H.

CERTIFICATE OF SERVICE

I hereby certify that the foregoing **RESPONSE TO OFFICE ACTION IN EX PARTE REEXAMINATION** was served upon the following:

Song K. Jung
McKenna Long & Aldridge LLP
1900 K St., N.W.
Washington, DC 20006

by depositing a true and correct copy of the same with the U.S. Postal Service (via First Class mail service) with full postage prepaid.

March 7, 2011
Date

/Justin King/
Justin King, Reg. No. 50,464

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United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,697	03/16/2010	6689629	67507-008Re-exam	5947

65358 7590 03/07/2011

WPAT, PC
INTELLECTUAL PROPERTY ATTORNEYS
7225 BEVERLY ST.
ANNANDALE, VA 22003

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 03/07/2011

Please find below and/or attached an Office communication concerning this application or proceeding.

PTOL-90C (Rev. 10/03)

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MAR 07 2011

CENTRAL REEXAMINATION UNIT

SONG K. JUNG

MCKENNA LONG AND ALDRIDGE LLP

1900 K STREET, NW

WASHINGTON, DC 20006

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,697*.

PATENT NO. *6689629*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

PTOL-465 (Rev.07-04)

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
90009697	3/16/10	6689629	67507-008Re-exam

WPAT, PC
INTELLECTUAL PROPERTY ATTORNEYS
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EXAMINER	
MARK REINHART	
ART UNIT	**PAPER**
3992	20110307

MAILED

DATE MAILED: MAR 07 2011

CENTRAL REEXAMINATION UNIT

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The Office action dated 06 January 2011 did not set the period for response. The period for response is three (3) months from the date of the Office action.

Mark Reinhart
SPE AU 3992

PTO-90C (Rev.04-03)

Doc Code: M865 or FAI.REQ.INTV

PTOL-413A (10-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Applicant Initiated Interview Request Form

Application No.: 90/009,697 First Named Applicant: Takatoshi Tsujimura et al.
Examiner: Nguyen, Tuan H. Art Unit: 3992 Status of Application: Pending

Tentative Participants:
(1) Nguyen, Tuan H. (2) Justin King

(3) (4)

Proposed Date of Interview: 3/24/2011 **Proposed Time:** 11AM (AM/PM)

Type of Interview Requested:
(1) [ ] Telephonic (2) [x] Personal (3) [ ] Video Conference

Exhibit To Be Shown or Demonstrated: [ ] YES [ ] NO
If yes, provide brief description:

Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims/ Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(1) 102(b)	1 and 9	Hirabayashi	[ ]	[ ]	[ ]
(2) 102(b)	1 and 9	Zhang	[ ]	[ ]	[ ]
(3)			[ ]	[ ]	[ ]
(4)			[ ]	[ ]	[ ]

[ ] Continuation Sheet Attached
[ ] Proposed Amendment or Arguments Attached
Brief Description of Arguments to be Presented:

Neither Hirabayashi nor Zheng discloses the limitation/structure of the connection pad contacting the first end of at most one of the plurality of wirings.

An interview was conducted on the above-identified application on _____.
NOTE: This form should be completed by applicant and submitted to the examiner in advance of the interview (see MPEP § 713.01).
This application will not be delayed from issue because of applicant's failure to submit a written record of this interview. Therefore, applicant is advised to file a statement of the substance of this interview (37 CFR 1.133(b)) as soon as possible.

/Justin King/
Applicant/Applicant's Representative Signature

Examiner/SPE Signature

Typed/Printed Name of Applicant or Representative

50464
Registration Number, if applicable

UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,697	03/16/2010	6689629	67507-008Re-exam	5947

65358 7590 03/24/2011

WPAT, PC
INTELLECTUAL PROPERTY ATTORNEYS
7225 BEVERLY ST.
ANNANDALE, VA 22003

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 03/24/2011

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

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MCKENNA LONG AND ALDRIDGE LLP

1900 K STREET, NW

WASHINGTON, DC 20006

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MAR 24 2011

CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,697*.

PATENT NO. *6689629*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Ex Parte Reexamination Interview Summary	Control No.	Patent Under Reexamination	
	90/009,697	6689629	
	Examiner	Art Unit	
	TUAN H. NGUYEN	3992	

All participants (USPTO personnel, patent owner, patent owner's representative):

(1) *TUAN H. NGUYEN* (3) *JUSTIN KING*

(2) *SUE LAO, MINH NGUYEN* (4) _____

Date of Interview: *24 March 2011*

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal (copy given to: 1)☐ patent owner 2)☐ patent owner's representative)

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.
Any other agreement(s) are set forth below under "Description of the general nature of what was agreed to..."

Claim(s) discussed: *1 and 9*.

Identification of prior art discussed: *Hirabayashi, Zhang*.

Description of the general nature of what was agreed to if an agreement was reached, or any other comments:
Discussed the difference between the claimed invention and Hirabayashi and Zhang. Disagreed that Hirabayashi and Zhang do not teach the claimed invention as noted in the Office action .

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims patentable, if available, must be attached. Also, where no copy of the amendments that would render the claims patentable is available, a summary thereof must be attached.)

A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION MUST INCLUDE PATENT OWNER'S STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. (See MPEP § 2281). IF A RESPONSE TO THE LAST OFFICE ACTION HAS ALREADY BEEN FILED, THEN PATENT OWNER IS GIVEN **ONE MONTH** FROM THIS INTERVIEW DATE TO PROVIDE THE MANDATORY STATEMENT OF THE SUBSTANCE OF THE INTERVIEW (37 CFR 1.560(b)). THE REQUIREMENT FOR PATENT OWNER'S STATEMENT CAN NOT BE WAIVED. **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

Tuan H. Nguyen

Tuan H. Nguyen
Primary Examiner

cc: Requester (if third party requester)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

Appl No.:	**90/009,697**
Patentee:	**6,689,629**
Filing Date:	**3/16/2010**
Art Unit:	**3992**
Examiner:	**Tuan H. Nguyen**
Attorney Docket No.:	**67507-008Re-exam**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL RESPONSE TO OFFICE ACTION

Sir:

This paper responds to the Office Action dated January 6, 2011, and to supplement the Office Action Response submitted on 3/7/2011. Please amend the above–identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Interview Summary begins on page 6 of this paper.

Remarks/Arguments begin on page 8 of this paper.

Copies of the cited prior art reference and related judicial decision are attached as Exhibits.

If any necessary fee is not submitted via EFS, the Office is authorized to charge the necessary fee to Deposit Account No. 50-5064.

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

What is claimed is:

1. (Currently Amended) An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of [[wiring]] wirings arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array, and at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy [[patters]] patterns are not in contact with any of the [[wiring]] wirings.

2. (Cancelled)

3. (Currently Amended) The array substrate for display according to claim [[2]] 1

wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.

4. (Cancelled)

5. (Original) The array substrate for display according to claim 3 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

6. (Original) The array substrate for display according to claim 5 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

7. (Currently Amended) The array substrate for display according to claim [[4]] 1 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

8. (Original) The array substrate for display according to claim 5 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

9. (Currently Amended) A [[meted]] method for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array and a plurality of wirings [[formed]] on the insulating substrate, each wiring having a first end, the wiring in communication with at least [[on]] one of the transistors in the thin film array, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials, and

the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the [[wiring]] wirings.

10. (Cancelled)

11. (Currently Amended) The method for forming an array substrate for display according to claim [[10]] 9 wherein the lower layer wiring materials is selected from the group consisting of aluminum and aluminum alloys.

12. (Cancelled)

13. (Cancelled)

14. (Currently Amended) The method for forming an array substrate for display according to claim [[13]] 9 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

15. (Currently Amended) The method for forming an array substrate for display according to claim [[12]] 9 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

16. (Currently Amended) The method for forming an array substrate for display according to claim [[13]] 9 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

17 (New) An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wirings arranged on the insulating substrate, each wiring having a first end, the wiring directly connects with at least one of the transistors in the thin film array;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patterns are not in contact with any of the wirings.

INTERVIEW SUMMARY

Patentee hereby thanks the Examiners for the personal interview conducted on March 24, 2011. Patentee hereby files this written statement for the issues discussed during the interview on March 24, 2011.

Those present at the telephone interview were Examiner Tuan Nguyen, Examiner Minh Nguyen, Examiner Lao Sue, and Patentee representative Justin King.

Patentee detailed the structure and nature of functionality of the claimed invention to include a novel combination of various recited limitations; in particular the limitation of connection pad in a padding structure and each connection pad contacts the first end of the at most one of the plurality of wirings.

No claim amendment was proposed for this interview. During the interview, Patentee explained the invention in regard to both the padding structure and the wiring connection to the padding structure. Patentee further discussed with the Office in regard limitation mapping in regard that each connection pad contacts the first end of the at most one of the plurality of wirings as stated the adapted rejection. Patentee explained that since the recited Hirabayashi explicitly discloses that the wires are divided into different paths and are intertwined together, Hirabayashi does not disclose the recited limitation that each connection pad is connected to the first end of the at most one wire.

The Office remained firm that the cited reference can still read on the recited limitation, disregarding that Hirabayashi explicitly discloses that the wires are divided into different paths and are intertwined together. The Office stated that Hirabayahsi's figure 6 discloses line L splitting into multiple lines LIN; Office stated that the segment of line L between connection pad 26 and the splitting point reads on the recited limitation of "each connection pad is connected to the first end of the at most one wire".

The Office reported that the response as filed, or an updated response with additional amendment(s), would be treated accordingly. Patentee hereby, in view of the interview discussion, submits the following supplemental response with additional updated and new argument before timely action by the Office.

REMARKS/ARGUMENTS

Claim Status Summary

Claims 1-5, 7-13, and 15-16 are is rejected under 35 U.S.C. §102(b), as being anticipated by Hirabayashi.

Claims 2-8 and 10-16 are is rejected under 35 U.S.C. §103(a), as being unpatentable over Hirabayashi in view of the APA.

Claims 1-5, 7-13, and 15-16 are rejected under 35 U.S.C. §102(b), as being anticipated by Zhang.

Claim 1 is amended to incorporate the limitations which were previously recited in the claims 2 and 4.

Claims 2 and 4 are cancelled in this paper.

Claim 9 is amended to incorporate the limitations which were previously recited in the claim 10 and 12-13. The claim 9 is also amended to correct formality errors from the original prosecution.

Claims 10 and 12-13 are cancelled in this paper.

New Claim 17 is added in this paper; no new matter is inserted by adding this claim.

35 U.S.C. §102(b) and §103(a) Rejection over Hirabayashi

Claims 1-5, 7-13, and 15-16 are is rejected under 35 U.S.C. §102(b), as being anticipated by Hirabayashi, and claims 2-8 and 10-16 are is rejected under 35 U.S.C. §103(a), as being unpatentable over Hirabayashi in view of the APA. Patentee respectfully disagrees for the reasons discussed below.

The 35 U.S.C. §102(b) states the following:

> "A person shall be entitled to a patent unless
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States"

As indicated in MPEP 2131, to anticipate a claim, the cited reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631 (MPEP § 2131). As can be gleaned from the cited case law, the requirement is that each element must be either expressly or inherently described.

The 35 U.S.C. §103(a) states the following:

> "(a) A patent may not be obtained though the invention is not identically disclosed or described as set for the in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made."

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Patentee respectfully submits that Hirabayashi does not disclose or teach every recited limitation in amended claim 1, which incorporates the limitations previously recited in claims 2 and 4. The amended claim 1 recites the following limitations:

"An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wirings arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array, wherein at least one of the wirings comprises at least an upper layer and a lower layer of *conductive materials*, and *the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys* thereof;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patterns are not in contact with any of the wirings."

Hirabayashi Does Not Disclose the Recited Upper Layer Wiring Material in Claim 1

Patentee respectfully submits that Hirabayashi does not disclose or teach the recited plurality of wiring comprising an upper layer and a lower layer, and the upper layer is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof. The limitation was previously recited in the claims 2 and 4. In particular, Patentee respectfully submits that the cited Hirabayashi does not disclose

the recited *conductive material selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.*

The Office stated that Hirabayashi's column 16, lines 19-22 discloses that the wiring can comprise at least an upper layer and a lower layer of conductive materials wherein the lower layer is aluminum and the upper layer is titanium nitride (Office Action, page 4, last paragraph); the Office alleged that Hirabayashi discloses the recited multi-layer wires with conductive materials by mapping Hirabayashi's upper titanium nitride layer as the recited upper layer and Hirabayashi's aluminum layer as the recited lower layer. Patentee respectfully disagrees that such structure reads on the recited limitation in claim 1.

Hirabayashi discloses an electro-optical device substrate. Hirabayashi discloses that a first metal layer forms the source electrode wiring 7a and relay wiring 10 with a quadruple-layer structure of Ti/TiN/Al/TiN in that order from the bottom (Hirabayashi, column 16, lines 19-22, figure 3). Hirabayashi essentially discloses a wire structure with a *lower titanium layer* covered by a layer of titanium nitride, and an *upper aluminum layer* covered by another layer of titanium nitride.

Patentee respectfully submits that although the cited reference Hirabayashi discloses multiple layers, Hirabayashi does not disclose a multi-layer wire having an upper layer selected from the group of *conductive material* consisting of molybdenum, chromium, tantalum, titanium, and alloys. Patentee respectfully submits that, not only the titanium nitride is not one of the listed conductive materials, the titanium nitride is not a conductive material at all. Patentee respectfully submits that the titanium nitride is not an alloy mixture, it is a non-conductive ceramic compound.

As defined in the chemistry field, and also explicitly taught in the college textbook "The Science and Design of Engineering Material" by Schaffer, the ceramic compounds are known as poor conductors of electricity due to the nature of ionic and/or

covalent bonding; such that they are frequently used as insulators[1]. Further support can be found in the U.S. Patent No. 5,158,657 issued to Kadokura, which Kadokura discloses a circuit substrate using the titanium nitride as an insulating film on the top of the conductive wire (Kadokura, abstract and column 3, last paragraph). Thus, Patentee respectfully submits that since the titanium nitride is known to be used as a insulator, then it cannot be considered as a conductive material; and since titanium nitride is not a conductive material, Hirabayashi's multi-layer wire cannot read on the recited limitation which explicitly recites that "an upper layer and a lower layer of *conductive* materials."

In addition, in a related judicial proceeding between the opposing party and the patentee, LG Display Co. LTD vs. AU Optronics Corporation, the court has explicitly held that Hirabayashi does not anticipate the instant patent, and stated that "…the instant patent's claim requires the upper layer wiring material to be selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof. However Hirabayashi discloses an upper layer of TiN, which is a ceramic compound, not a conductive material or a titanium alloy" (District Court opinion, page 70, 1st paragraph, lines 9-13).

Hirabayashi's titanium nitride layer is not one of the materials listed in the claim limitation. In particular, Hirabayashi's titanium nitride layer is neither the recited titanium nor an alloy thereof. Patentee further submits that Hirabayashi's titanium nitride cannot even be considered as equivalent to any of the recited materials since it is not a conductive material. Therefore, for the reason discussed above, Patentee respectfully submits that the cited reference Hirabayashi does not disclose every recited limitation in the amended claim 1 as required under 35 USC 102(b) or 35 USC 103(a); hence, Patentee respectfully requests the Office to withdraw the rejection over claim 1 accordingly, and to issue favorable re-consideration.

---

1 Schaffer et al., "The Science and Design of Engineering Material", International Student Edition.

Claims 2-6

Claims 2 and 4 are now cancelled and the limitations previously recited in claims 2 and 4 are now inserted in the claim 1. The claims 3 and 5 depend on claim 1; thus they incorporate every recited limitation in claim 1. For the reasons stated above, the claims 3 and 5 are not anticipated by Hirabayashi, and Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 3 and 5, and to issue favorable re-consideration.

Claims 7 and 8

The claims 7 and 8 depend on claim 1; thus they incorporate every recited limitation in claim 1. For at least the reasons stated above, the claims 7 and 8 are not anticipated by Hirabayashi.

Furthermore, the dependent claims 7 and 8 each require that "the upper layer wiring material is selected such that the upper layer wiring material does not become insolvent in an acid or alkaline etchant." The Specification explicitly stated that the dummy patterns are located between the pixel electrodes, i.e., the array, and the contact pads, to increase the density of the metal in areas between the pixel electrodes and the contact pads, so as to avoid passivation of the upper conductive layer, and thus avoid undercut, during etching (Specification, Column 5, lines 11-38, column 5, line 55 to column 6 line 17). Patentee respectfully submits that the alleged dummy patterns in Hirabayashi are for a completely different purpose: to ensure uniform polishing of the substrate. Nothing in Hirabayashi discloses or suggests that dummy patterns are located in an area such that an upper layer wiring material does not become insolvent in an acid or alkaline etchant. There is no mention of the problem of an upper layer of wiring material becoming insoluble in an acid or alkaline etchant, much less a solution to that problem, in Hirabayashi.

For the reasons stated above, Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 7 and 8, and to issue favorable re-consideration.

Hirabayashi Does Not Disclose the Recited Upper Layer Wiring Material in Claim 9

Patentee respectfully submits that Hirabayashi does not disclose every recited limitation in amended claim 9, which incorporates the limitations previously recited in claims 10 and 12-13. The amended claim 1 recites the following limitations:

> "A method for forming an array substrate for display, comprising:
>
> forming a layer of an insulating substrate, having an area;
>
> forming a thin film transistor array and a plurality of wirings on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials, and the *upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof*;
>
> forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;
>
> forming pixel electrodes, and
>
> forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wirings."

Patentee respectfully submits that Hirabayashi does not disclose or teach the recited plurality of wiring comprising an upper layer and a lower layer, and the upper layer is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof. The limitation was previously recited in the claims 10 and

12-13. In particular, Patentee respectfully submits that the cited Hirabayashi does not disclose the recited *conductive material selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.*

The Office stated that Hirabayashi's column 16, lines 19-22 discloses that the wiring can comprise at least an upper layer and a lower layer of conductive materials wherein the lower layer is aluminum and the upper layer is titanium nitride (Office Action, page 4, last paragraph); the Office alleged that Hirabayashi discloses the recited multi-layer wires with conductive materials by mapping Hirabayashi's upper titanium nitride layer as the recited upper layer and Hirabayashi's aluminum layer as the recited lower layer. Patentee respectfully disagrees that such structure reads on the recited limitation in claim 9.

Hirabayashi discloses an electro-optical device substrate. Hirabayashi's column 16, lines 19-22 discloses that a first metal layer forms the source electrode wiring 7a and relay wiring 10 (also see Hirabayashi figure 3) with a quadruple-layer structure of Ti/TiN/Al/TiN in that order from the bottom. Hirabayashi essentially discloses a wire structure with a *lower titanium layer* covered by a layer of titanium nitride, and an *upper aluminum layer* covered by another layer of titanium nitride.

Patentee respectfully submits that although the cited reference Hirabayashi discloses multiple layers, Hirabayashi does not disclose a multi-layer wire having an upper layer selected from the group of *conductive material* consisting of molybdenum, chromium, tantalum, titanium, and alloys. Patentee respectfully submits that, not only the titanium nitride is not one of the listed conductive materials, the titanium nitride is not a conductive material at all. Patentee respectfully submits that the titanium nitride is not an alloy mixture, it is a non-conductive ceramic compound.

As defined in the chemistry field, and also explicitly taught in the college textbook "The Science and Design of Engineering Material" by Schaffer, the ceramic compounds are known as poor conductors of electricity due to the nature of ionic and/or

covalent bonding; such that they are frequently used as insulators[2]. Further support can be found in the U.S. Patent No. 5,158,657 issued to Kadokura, which Kadokura discloses a circuit substrate using the titanium nitride as an insulating film on the top of the conductive wire (Kadokura, abstract and column 3, last paragraph). Thus, Patentee respectfully submits that since the titanium nitride is known to be used as a insulator, then it cannot be considered as a conductive material; and since titanium nitride is not a conductive material, Hirabayashi's multi-layer wire cannot read on the recited limitation which explicitly recites that "an upper layer and a lower layer of *conductive* materials."

In addition, in a related judicial proceeding between the opposing party and the patentee, LG Display Co. LTD vs. AU Optronics Corporation, the court has explicitly held that Hirabayashi does not anticipate the instant patent, and stated that "…the instant patent's claim requires the upper layer wiring material to be selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof. However Hirabayashi discloses an upper layer of TiN, which is a ceramic compound, not a conductive material or a titanium alloy" (District Court opinion, page 70, 1st paragraph, lines 9-13).

Hirabayashi's titanium nitride layer is not one of the materials listed in the claim limitation. In particular, Hirabayashi's titanium nitride layer is neither the recited titanium nor an alloy thereof. Patentee further submits that Hirabayashi's titanium nitride cannot even be considered as equivalent to any of the recited materials since it is not a conductive material. Therefore, for the reason discussed above, Patentee respectfully submits that the cited reference Hirabayashi does not disclose every recited limitation in the amended claim 1 as required under 35 USC 102(b) or 35 USC 103(a); hence, Patentee respectfully requests the Office to withdraw the rejection over claim 9 accordingly, and to issue favorable re-consideration.

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2 Schaffer et al., "The Science and Design of Engineering Material", International Student Edition.

Claims 10-14

Claims 10 and 12-13 are now cancelled and the limitations previously recited in claims 10 and 12-13 are now inserted in the claim 9.

The claims 11 and 14 depend on claim 9; thus they incorporate every recited limitation in claim 9. For the reasons stated above, the claims 11 and 14 are not anticipated by Hirabayashi, and Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 11 and 14, and to issue favorable re-consideration.

Claims 15 and 16

The claims 15 and 16 depend on claim 9; thus they incorporate every recited limitation in claim 9. For at least the reasons stated above, the claims 15 and 16 are not anticipated by Hirabayashi.

Furthermore, the dependent claims 15 and 16 each require that "the upper layer wiring material is selected such that the upper layer wiring material does not become insolvent in an acid or alkaline etchant." The Specification explicitly stated that the dummy patterns are located between the pixel electrodes, i.e., the array, and the contact pads, to increase the density of the metal in areas between the pixel electrodes and the contact pads, so as to avoid passivation of the upper conductive material, and thus avoid undercut, during etching (Specification, Column 5, lines 11-38, column 5, line 55 to column 6 line 17). Patentee respectfully submits that the alleged dummy patterns in Hirabayashi are for a completely different purpose: to ensure uniform polishing of the substrate. Nothing in Hirabayashi discloses or suggests that dummy patterns are located in an area such that an upper layer wiring material does not become insolvent in an acid or alkaline etchant. There is no mention of the problem of an upper layer of wiring material becoming insoluble in an acid or alkaline etchant, much less a solution to that problem, in Hirabayashi.

For the reasons stated above, Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 15 and 16, and to issue favorable re-consideration.

35 U.S.C. §102(b) Rejection over Zhang

Claims 1-5, 7-13, and 15-16 are rejected under 35 U.S.C. §102(b), as being anticipated by Zhang. Patentee respectfully submits that Zhang does not disclose every recited limitation in claim 1. The amended claim 1 recites the following limitations:

"An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials, and the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, *the dummy conductive patterns situated between the connection pads and the pixel electrodes* such that the dummy patterns are not in contact with any of the wiring.."

Zhang Does Not Disclose the Recited Arrangement among Connection Pads, Dummy Conductive Patterns, and the Electrode as Recited in Claim 1

In particular, Patentee respectfully submits that the cited reference Zhang does not disclose or teach the limitation of the dummy conductive patterns *situated between the connection pads and the pixel electrodes.* As illustrated in the figure 2 of the instant patent, the dummy pattern 29 is located between the connection pad 27 and the pixel electrode 22.

The Office asserted that the proposed rejection CC-21 is adopted as proposed. The claim chart table in CC-21 alleged that Zhang discloses the reciting connection pads by disclosing that the signal lines 2 and scan lines 3 connect to extension terminal 6. The proposed rejection seems to equate the extension terminal 6 to the recited connections pads. The adapted rejection further alleged that the cited reference Zhang Figures 4, 8, and 16 disclose dummy wiring 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals (The adapted rejection, page CC21-1, last column of the table). Patentee respectfully disagrees. In particularly, Patentee respectfully submits that Zhang does not disclose or teach that the *dummy patterns are situated between the connection pads and the pixel electrodes* as recited in the claim 1.

The cited reference Zhang's figure 16 discloses a prior art without any dummy patterns but with a sealing material region 5 and extension terminal 6 located outside of the sealing material region 5 for connecting to the peripheral drive circuits. Zhang discloses that because the peripheral drive circuit is connected at the outside of the sealing material via the extension terminal 6, the moisture can enter into the electrode area and cause deterioration (Zhang, column 2, 3rd paragraph). The cited reference Zhang then discloses an improved embodiment in figures 1, 4, and 8. Zhang's figure 1 discloses an improved embodiment by relocating the peripheral drive circuits 103, 104, and additional extension terminal 303a within the sealed area surrounded by the sealing material region 107 (Zhang, column 8, 3rd paragraph, and column 10, lines 3-6, figure 4). Since the peripheral drive circuits, that the terminal 6 in Zhang's figure 16 is connecting to, are now located within the sealed area, Zhang's figures 4 and 8 implicitly disclose implementing figure 16's terminal 6 within the sealed area. Zhang further discloses positioning the alleged dummy patterns in the sealing material region 107, which is at the *outside* the electrodes, extension terminals, scanning line drive circuit 104, the signal line drive circuit 103. Zhang explicit discloses that the alleged dummy patterns are located in the sealing region 107 in order to uniform the sealing material's

structure for unifying the sealing as to overcome the problem know in the prior practice (Zhang, column 2, lines 45-52, and column 6, last paragraph to column 7, 1st paragraph).

Thus, patentee respectfully submits that Zhang does not disclose or teach that the dummy patterns are situated between the connection pad and the pixel section. As discussed above, Zhang discloses that the connection end 303a of the wiring 303 is located on the pixel section 102 side, which is within the sealed area; Zhang also implicitly discloses implementing figure 16's terminal 6 within the sealed area along with the driving circuits. Since Zhang's dummy patterns is on the sealing material region 107, Zhang's dummy patterns are located outside of the sealing area where all terminals, connection end 303a, and pixels reside. Since Zhang's dummy pattern is located outside of the sealing area where all terminals, connection end 303a, and pixels reside, Zhang's dummy pattern is not situated between the connection pads and the pixel electrodes as recited in the claim 1.

Hence, Patentee respectfully submits that Zhang does not disclose or teach that the recited limitation of "*the dummy conductive patterns situated between the connection pads and the pixel electrodes*". And for the reason discussed above, Patentee respectfully submits that the cited reference Zhang does not disclose every recited limitation in the claim 1 as required under 35 USC 102(b); hence, Patentee respectfully requests the Office to withdraw the rejection over claim 1 accordingly, and to issue favorable re-consideration.

Claims 2-6

Claims 2 and 4 are now cancelled and the limitations previously recited in claims 2 and 4 are now inserted in the claim 1. The remaining claims 3 and 5 depend on claim 1; thus they incorporate every recited limitation in claim 1. For the reasons stated above, the claims 3 and 5 are not anticipated by Zhang; and Patentee respectfully

requests the Office to withdraw the rejection over the remaining claims 3 and 5-8, and to issue favorable re-consideration.

Claims 7 and 8

The remaining claims 7 and 8 depend on claim 1; thus they incorporate every recited limitation in claim 1. For at least the reasons stated above, the claims 7 and 8 are not anticipated by Zhang.

Furthermore, the dependent claims 7 and 8 each require that "the upper layer wiring material is selected such that the upper layer wiring material does not become insolvent in an acid or alkaline etchant." The Specification explicitly stated that the dummy patterns are located between the pixel electrodes, i.e., the array, and the contact pads, to increase the density of the metal in areas between the pixel electrodes and the contact pads, so as to avoid passivation of the upper conductive layer, and thus avoid undercut, during etching (Specification, Column 5, lines 11-38, column 5, line 55 to column 6 line 17). Patentee respectfully submits that the alleged dummy patterns in Zhang are for a completely different purpose: unifying the sealing. Zhang explicit discloses that the alleged dummy patterns are located in the sealing region 107 in order to uniform the sealing material's structure for unifying the sealing as to overcome the problem know in the prior practice (Zhang, column 2, lines 45-52, and column 6, last paragraph to column 7, 1st paragraph). Nothing in Zhang discloses or suggests that dummy patterns are located in an area such that an upper layer wiring material does not become insolvent in an acid or alkaline etchant. There is no mention of the problem of an upper layer of wiring material becoming insoluble in an acid or alkaline etchant, much less a solution to that problem, in Zhang.

For the reasons stated above, Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 7 and 8, and to issue favorable re-consideration.

Zhang Does Not Disclose the Recited Arrangement among Connection Pads, Dummy Conductive Patterns, and the Electrode as Recited in Claim 9

Patentee respectfully submits that Zhang does not disclose every recited limitation in claim 9. The amended claim 9 recites the following limitations:

"A method for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array and a plurality of wirings on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials, and the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring."

In particular, Patentee respectfully submits that the cited reference Zhang does not disclose or teach the limitation of the dummy conductive patterns *situated between the connection pads and the pixel electrodes.* As illustrated in the figure 2 of the instant patent, the dummy pattern 29 is located between the connection pad 27 and the pixel electrode 22.

The Office asserted that the proposed rejection CC-21 is adopted as proposed. The claim chart table in CC-21 alleged that Zhang discloses the reciting connection pads by disclosing that the signal lines 2 and scan lines 3 connect to extension terminal

6. The proposed rejection maps the extension terminal 6 to the recited connections pads since each extension terminal 6 contacts the end of the at most one of the plurality of wirings (The adapted rejection, page CC21-1, 5th row of the table). The adapted rejection further alleged that the cited reference Zhang Figures 4, 8, and 16 disclose dummy wiring 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals (The adapted rejection, page CC21-1, last row of the table). Patentee respectfully disagrees. In particularly, Patentee respectfully submits that Zhang does not disclose or teach that the *dummy patterns are situated between the connection pads and the pixel electrodes* as recited in the claim 9.

The cited reference Zhang's figure 16 discloses a prior art without any dummy patterns but with a sealing material region 5 and extension terminal 6 located outside of the sealing material region 5 for connecting to the peripheral drive circuits. Zhang discloses that because the peripheral drive circuit is connected at the outside of the sealing material via the extension terminal 6, the moisture can enter into the electrode area and cause deterioration (Zhang, column 2, 3rd paragraph). The cited reference Zhang then discloses an improved embodiment in figures 1, 4, and 8. Zhang's figure 1 discloses an improved embodiment by relocating the peripheral drive circuits 103, 104, and additional extension terminal 303a within the sealed area surrounded by the sealing material region 107 (Zhang, column 8, 3rd paragraph, and column 10, lines 3-6, figure 4). Since the peripheral drive circuits, that the terminal 6 in Zhang's figure 16 is connecting to, are now located within the sealed area, Zhang's figures 4 and 8 implicitly disclose implementing figure 16's terminal 6 within the sealed area. Zhang further discloses positioning the alleged dummy patterns in the sealing material region 107, which is at the *outside* the electrodes, extension terminals, scanning line drive circuit 104, the signal line drive circuit 103. Zhang explicit discloses that the alleged dummy patterns are located in the sealing region 107 in order to uniform the sealing material's structure for unifying the sealing as to overcome the problem know in the prior practice

(Zhang, column 2, lines 45-52, and column 6, last paragraph to column 7, 1st paragraph).

Thus, patentee respectfully submits that Zhang does not disclose or teach that the dummy patterns are situated between the connection pad and the pixel section. As discussed above, Zhang discloses that the connection end 303a of the wiring 303 is located on the pixel section 102 side, which is within the sealed area; Zhang also implicitly discloses implementing figure 16's terminal 6 within the sealed area along with the driving circuits. Since Zhang's dummy patterns is on the sealing material region 107, Zhang's dummy patterns are located outside of the sealing area where all terminals, connection end 303a, and pixels reside. Since Zhang's dummy pattern is located outside of the sealing area where all terminals, connection end 303a, and pixels reside, Zhang's dummy pattern is not situated between the connection pads and the pixel electrodes as recited in the claim 9.

Hence, Patentee respectfully submits that Zhang does not disclose or teach that the recited limitation of "*the dummy conductive patterns situated between the connection pads and the pixel electrodes*". And for the reason discussed above, Patentee respectfully submits that the cited reference Zhang does not disclose every recited limitation in the claim 1 as required under 35 USC 102(b); hence, Patentee respectfully requests the Office to withdraw the rejection over claim 9 accordingly, and to issue favorable re-consideration.

Claims 10-14

Claims 10 and 12-13 are now cancelled and the limitations previously recited in claims 10 and 12-13 are now inserted in the claim 9. The remaining claims 11 and 14 depend on claim 9; thus they incorporate every recited limitation in claim 9. For the reasons stated above, the claims 11 and 14 are not anticipated by Zhang; and Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 11 and 14, and to issue favorable re-consideration.

Claims 15 and 16

The remaining claims 15 and 16 depend on claim 9; thus they incorporate every recited limitation in claim 9. For at least the reasons stated above, the claims 15 and 16 are not anticipated by Zhang.

Furthermore, the dependent claims 15 and 16 each require that "the upper layer wiring material is selected such that the upper layer wiring material does not become insolvent in an acid or alkaline etchant." The Specification explicitly stated that the dummy patterns are located between the pixel electrodes, i.e., the array, and the contact pads, to increase the density of the metal in areas between the pixel electrodes and the contact pads, so as to avoid passivation of the upper conductive layer, and thus avoid undercut, during etching (Specification, Column 5, lines 11-38, column 5, line 55 to column 6 line 17). Patentee respectfully submits that the alleged dummy patterns in Zhang are for a completely different purpose: unifying the sealing. Zhang explicit discloses that the alleged dummy patterns are located in the sealing region 107 in order to uniform the sealing material's structure for unifying the sealing as to overcome the problem know in the prior practice (Zhang, column 2, lines 45-52, and column 6, last paragraph to column 7, 1st paragraph). Nothing in Zhang discloses or suggests that dummy patterns are located in an area such that an upper layer wiring material does not become insolvent in an acid or alkaline etchant. There is no mention of the problem of an upper layer of wiring material becoming insoluble in an acid or alkaline etchant, much less a solution to that problem, in Zhang.

For the reasons stated above, Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 15 and 16, and to issue favorable re-consideration.

New Claim 17

The new claim 17 is added in this paper. The claim 17 recites the following limitations:

"An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring directly connects with at least one of the transistors in the thin film array;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patterns are not in contact with any of the wirings."

The claim 17 recites the similar limitations as previously recited in claim 1. The claim 17 further recites that the wiring directly connects with at least one of the transistors in the thin film array. Patentee respectfully submits that none of the cited references on record discloses or teach this limitation in combination with the rest of the recited limitations, such as the limitation that the dummy conductive patterns are situated between the connection pads and the pixel electrodes and t

he dummy patterns are not in contact with any of the wirings. Thus, patentee respectfully requests the Office to allow and confirm the newly added claim 17 along with the claims **1, 3, 5-9, 11, and 14-16**.

Conclusion

Claims 1, 3, 5-9, 11, and 14-17 are pending in this proceeding. In view of the reasons stated above, Patentee respectfully submits that the independent claims patentably define the present invention over the citations of record, and Patentee respectfully requests a favorable reconsideration and issuing allowance accordingly. Further, the dependent claims should also be allowable for the same reasons as their respective base claims and further due to the additional features that they recite. Separate and individual consideration of the dependent claims is respectfully requested. Examiner is invited to contact the attorney on record to expedite the prosecution in pursuance of allowance.

Respectfully submitted,
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EXHIBIT A

“The Science and Design of Engineering Material”

THE SCIENCE AND DESIGN OF ENGINEERING MATERIALS

INTERNATIONAL STUDENT EDITION

SCHAFFER SAXENA ANTOLOVICH SANDERS WARNER

are excellent conductors of electricity, are relatively strong, are dense, can be deformed into complex shapes, and are resistant to breaking in a brittle manner when subjected to high-impact forces. This set of mechanical and physical properties makes metals one of the most important classes of materials for both electrical and structural applications. Extensive (and in some cases exclusive) use of metals occurs in automobiles, airplanes, buildings, bridges, machine tools, ships, and many other applications where a combination of high strength and resistance to brittle fracture is required. In fact, it is largely the excellent combination of strength and toughness (i.e., resistance to fracture) that makes metals so attractive as structural materials.

The basic understanding of metals and their properties is advanced, and they are considered to be mature materials with relatively little potential for major breakthroughs. However, significant improvements have been and continue to be made as a result of advances in processing. Two examples are:

Higher operating temperatures in jet engines have been attained through the use of turbine blades that are produced by controlled solidification processes. The blades are made of nickel and other metal alloys (atomic-scale mixtures of atoms) and are in wide commercial use. Improvements will continue as processes are refined through use of advanced sensors and real-time computer control.

Frequently parts are fabricated from metal powders by compacting them into a desired shape at high temperature and pressure in a process known as powder metallurgy (PM). An important reason for using PM processing is reduced fabrication costs. While some improvement in properties can be obtained through PM, a major benefit is the reduced variation in properties, which will allow the operating loads to be safely increased. Reduced production costs through PM will continue to impact the aerospace and automotive fields.

1.4.2 Ceramics

Ceramics are composed of both metallic and nonmetallic atomic species. Many (but not all) ceramics are crystalline, and frequently the nonmetal is oxygen, as in Al_2O_3, MgO, and CaO, all of which are typical ceramics. One significant difference between ceramics and metals is that in ceramics, bonding is ionic and/or covalent. As a result there are no ''free'' electrons in ceramics. They are generally poor conductors of electricity, but are frequently used as insulators in electrical applications. One familiar example is spark plugs, in which a ceramic insulator separates the metal components.

Ionic and covalent bonds are extremely strong. As a result, ceramic materials are intrinsically stronger than metals. However, because of their more complex structure, the ions/atoms cannot easily be displaced as a result of applied forces. Rather than bend to accommodate such forces, ceramics tend to fracture in a brittle manner. This brittleness generally limits their use as structural materials, although recent improvements have been made by incorporating ceramic fibers into a ceramic matrix and other innovative techniques. Their rigid bond structure confers other advantages, including high temperature stability, resistance to chemical attack, and resistance to absorption of foreign substances. They are thus ideal in high-temperature applications such as the space shuttle, as containers for reactive chemicals, and as bowls and plates for foods where surface contamination is undesirable.

are excellent conductors of electricity, are relatively strong, are dense, can be deformed into complex shapes, and are resistant to breaking in a brittle manner when subjected to high-impact forces. This set of mechanical and physical properties makes metals one of the most important classes of materials for both electrical and structural applications. Extensive (and in some cases exclusive) use of metals occurs in automobiles, airplanes, buildings, bridges, machine tools, ships, and many other applications where a combination of high strength and resistance to brittle fracture is required. In fact, it is largely the excellent combination of strength and toughness (i.e., resistance to fracture) that makes metals so attractive as structural materials.

The basic understanding of metals and their properties is advanced, and they are considered to be mature materials with relatively little potential for major breakthroughs. However, significant improvements have been and continue to be made as a result of advances in processing. Two examples are:

Higher operating temperatures in jet engines have been attained through the use of turbine blades that are produced by controlled solidification processes. The blades are made of nickel and other metal alloys (atomic-scale mixtures of atoms) and are in wide commercial use. Improvements will continue as processes are refined through use of advanced sensors and real-time computer control.

Frequently parts are fabricated from metal powders by compacting them into a desired shape at high temperature and pressure in a process known as powder metallurgy (PM). An important reason for using PM processing is reduced fabrication costs. While some improvement in properties can be obtained through PM, a major benefit is the reduced variation in properties, which will allow the operating loads to be safely increased. Reduced production costs through PM will continue to impact the aerospace and automotive fields.

1.4.2 Ceramics

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Ionic and covalent bonds are extremely strong. As a result, ceramic materials are intrinsically stronger than metals. However, because of their more complex structure, the ions/atoms cannot easily be displaced as a result of applied forces. Rather than bend to accommodate such forces, ceramics tend to fracture in a brittle manner. This brittleness generally limits their use as structural materials, although recent improvements have been made by incorporating ceramic fibers into a ceramic matrix and other innovative techniques. Their rigid bond structure confers other advantages, including high temperature stability, resistance to chemical attack, and resistance to absorption of foreign substances. They are thus ideal in high-temperature applications such as the space shuttle, as containers for reactive chemicals, and as bowls and plates for foods where surface contamination is undesirable.

Some ceramics are not crystalline. The most common example is window glass, which is composed of various metal oxides. Optical properties are of major importance in glass and may be controlled through composition and processing. In addition the thermal and mechanical properties of glass can also be controlled. Safety glass is simply glass that has been subjected to a thermal cycle that leaves the surface in a state of compression and thereby resistant to cracking. In fact, glass treated in this way is even difficult to crack when struck with a hammer!

Some current and potential applications for ceramic materials with a large economic impact are listed below:

- In the automotive industry the thermal and strength properties of ceramics make them very attractive for engine components. For example, there are over 60,000 autos in Japan with ceramic turbochargers, which increase the efficiency of the automobile. The materials in this application are Si_3N_4 or SiC processed to have some ability to resist brittle fracture.
- Ceramics based on compounds such as $YBa_2Cu_3O_7$ and $Ba_2Sr_2CaCu_2O_x$ have increased critical superconducting temperatures to >95K. This means that superconducting films may be used as liners in microwave devices and as wires for all kinds of applications. Improving the current carrying capacity and connection technology are essential for widespread application of these materials.
- Next-generation computers will have ceramic electro-optic components that will give increased speed and efficiency.

1.4.3 Polymers

Polymers consist of long chain molecules with repeating groups that are largely covalently bonded. Common elements within the chain backbone include C, O, N, and Si. An example of a common polymer with a simple structure, polyethylene, is shown in Figure 1.4–1. The bonds within the backbone are all covalent, so the molecular chains are extremely strong. Chains are usually bonded to each other, however, by means of comparatively weak secondary bonds. This means that it is generally easy for the chains to slide by one another when forces are applied and the strength is thus relatively low. In addition, many polymers tend to soften at moderate temperatures, so they are not generally useful for high-temperature applications.

Polymers, however, have properties that make them attractive in many applications. Since they contain common elements and are relatively easy to synthesize, or exist in nature, they can be inexpensive. They have a low density (in part because of the light elements from which they are constituted) and are easily formed into complex shapes. They have thus replaced metals for molded parts in automobiles

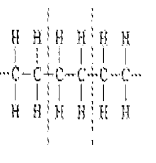

Figure 1.4–1 Schematic of the structure of polyethylene. The mer or basic repeating unit in the polymer is the $-CH_2-$ group.

EXHIBIT B

U.S. Patent No. 5,158,657 (Kadokura)

US005158657A

United States Patent [19]

Kadokura

[11] Patent Number: 5,158,657

[45] Date of Patent: Oct. 27, 1992

[54] **CIRCUIT SUBSTRATE AND PROCESS FOR ITS PRODUCTION**

[75] Inventor: **Susumu Kadokura**, Sagamihara, Japan

[73] Assignee: **Canon Kabushiki Kaisha**, Tokyo, Japan

[21] Appl. No.: **673,028**

[22] Filed: **Mar. 21, 1991**

[30] **Foreign Application Priority Data**

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Mar. 23, 1990	[JP]	Japan	2-74653
Mar. 24, 1990	[JP]	Japan	2-74203
Mar. 26, 1990	[JP]	Japan	2-77494
Mar. 26, 1990	[JP]	Japan	2-77495

[51] **Int. Cl.**[5] **C25D 13/04**

[52] **U.S. Cl.** **204/181.1**; 205/125

[58] **Field of Search** 204/181.1, 180.2

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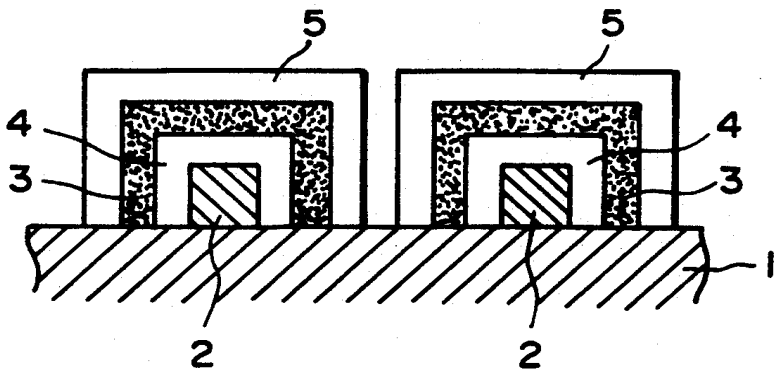
Assistant Examiner—Kishor Mayekar
Attorney, Agent, or Firm—Fitzpatrick, Cella, Harper & Scinto

[57] **ABSTRACT**

A circuit substrate has a substrate, a conductor wire provided on the substrate, a first insulating film that covers the conductor wire, and a conductive film that covers the first insulating film. At least one of the first insulating film and the conductive film is formed by electro-deposition coating.

18 Claims, 1 Drawing Sheet



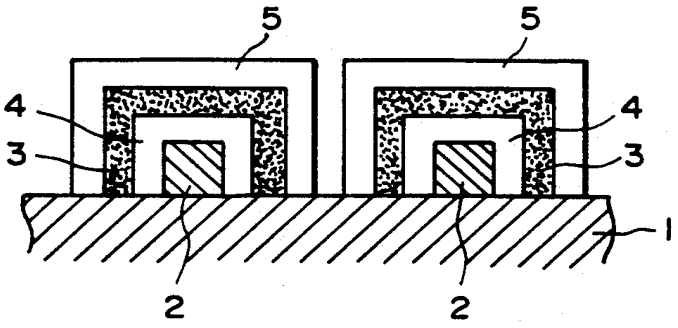

5
5
4
4
3
3
1
2
2

FIG. 1

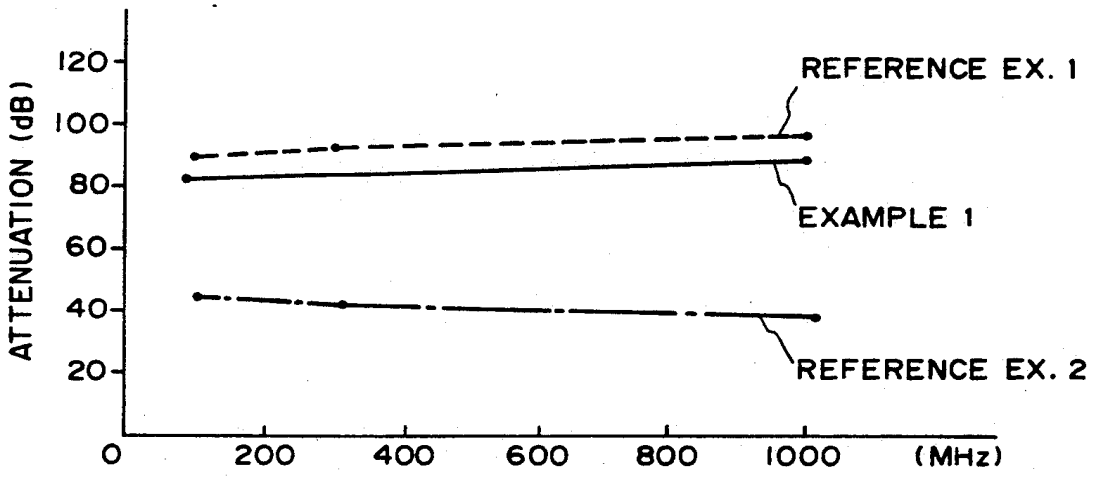

ATTENUATION (dB)
120
100
80
60
40
20
0
200
400
600
800
1000
(MHz)
REFERENCE EX. 1
EXAMPLE 1
REFERENCE EX. 2

FIG. 2

CIRCUIT SUBSTRATE AND PROCESS FOR ITS PRODUCTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a circuit substrate and a process for producing it. More particularly the present invention relates to a circuit substrate used in optical instruments such as cameras, home electric appliances, computers, word processors, measuring devices or the like, and a process for producing such a circuit substrate.

2. Related Background Art

Conventional processes commonly used to produce circuit substrates comprise the steps of (1) forming a copper foil circuit pattern on an insulated substrate by photolithography, or by screen printing using a conductive paste, (2) thereafter coating a solder resist or the like on the surface of the circuit to provide thereon an insulating layer, (3) subsequently coating a conductive paste on the surface of the insulating layer to provide thereon a shielding layer, and (4) further coating a solder resist or the like on the shielding layer to provide thereon an insulating layer. Methods for electromagnetic wave shielding may include, in addition to a method of providing the above shielding layer, a method in which shielding is effected by surrounding a circuit substrate with a sheet metal. The insulating layer on the circuit pattern can also be provided by laminating a dry film.

The conventional processes for producing circuit substrates, however, provide an insulating layer having a small thickness at the corners of copper wires that constitute a this arrangement results in a break of the insulating layer at the parts corresponding thereto. The conventional processes for producing circuit substrates also tend to cause a dielectric breakdown or defective insulation because of inclusion of bubbles or the like between copper wires, exacerbating the problem. In addition, the conventional processes for producing circuit substrates require complicated production steps which take a long time for their manufacture, also bringing about a problem in cost.

As for the conventional method in which shielding is effected by surrounding a circuit substrate with a sheet metal, it requires a broad space in order for the metal sheet to be provided, and hence has been not suitable for making products small-sized.

SUMMARY OF THE INVENTION

The present invention was made in order to overcome such disadvantages involved in the prior art. An object of the present invention is to provide a circuit substrate can provide uniform layer thicknesses for the insulating layer and shielding layer on a circuit pattern, can be free from defective insulation, and can also promise a high electromagnetic wave shielding effect, and a process for producing such a circuit substrate.

The circuit substrate of the present invention comprises a substrate, a conductor wire provided on said substrate, a first insulating film that covers said conductor wire, and a conductive film that covers said first insulating film; at least one of said first insulating film and said conductive film is formed by electro-deposition coating.

The process for producing a circuit substrate of the present invention comprises a first step of forming on a substrate a circuit pattern comprised of a conductor wire, a second step of providing a first insulating film to cover said circuit pattern, and a third step of providing a conductive film to cover said first insulating film. Electro-deposition coating is used in at least one step of said second step and said third step. Said electro-deposition coating is carried out by immersing said substrate in an electro-deposition coating composition, setting said conductor wire as an electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-section illustrating an example of the construction of the circuit substrate according to the present invention.

FIG. 2 is a graph illustrating an electromagnetic wave shielding effect of the circuit substrate according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The circuit substrate of the present invention can be used in all sorts of electric apparatuses including optical instruments such as cameras, home electric appliances, word processors, computers and measuring devices. The circuit substrate of the present invention comprises, as shown in FIG. 1, an insulated substrate 1 having a conductor wire 2 formed thereon, a first insulating film 4 that covers the whole surface of the conductor wire 2, and a conductive film 3 that covers the whole surface of the first insulating film 4. The conductive film 3 serves as a shielding layer that effects electromagnetic wave shielding. The conductor wire 2 forms a circuit pattern on the insulated substrate 1. The conductor wire 2 may preferably be formed of copper. The whole surface of the insulating film 4 may optionally be covered with an additional insulating film 5 (a second insulating film). The insulating film 5 is provided to prevent the circuit substrate of the present invention from contacting other component parts to short, when it has been set in an electric apparatus.

In the circuit substrate of the present invention, at least one of the films 3, 4 and 5 is formed by electro-deposition coating. A coating formed by the electro-deposition coating is finally cured by heating or irradiation with light.

The electro-deposition coating refers to a process in which a pair of electrodes are disposed in a solution in which a substance that gives a coating film has been dissolved (hereinafter "electro-deposition coating composition") and a DC current is applied to cause the substance to adhere onto one of the electrodes. Thus, in the present invention, the conductor wire 2 formed on the substrate serves as one of the electrodes. As the other electrode, it is preferred to use, for example, a stainless steel plate.

Proposals have been hitherto made on the electro-deposition coating. For example, Japanese Patent Application Laid-open No. 55-11175 proposes a method in which an electro-deposition coating composition is applied twice superposingly. The present applicants have also proposed in Japanese Patent Application Laid-open No. 2-6564 an electro-deposition coating composition containing a ceramic powder and a fluorine resin powder.

As the insulated substrate 1, it is possible to use commonly known insulated substrates as exemplified by those made of a polycarbonate resin, a polyetherimide

resin, a glass fiber packed ABS resin, a glass epoxy resin or the like.

The circuit pattern formed by the use of the conductor wire **2** can be formed by commonly known photolithography. More specifically, the circuit pattern can be formed by laminating, for example, copper foil on the insulated substrate **1**, further coating a resist on the copper foil, and then exposing the resist coating to light through a mask having the desired pattern, followed by development and etching.

On the whole surface of the conductor wire **2**, the insulating film **4** is formed by electro-deposition coating by the use of a resin feasible for electro-deposition.

Resins used in the electro-deposition coating have been hitherto studied in variety. In order for resin to be electro-deposited, the resin must be capable of being charged when the electro-deposition coating is carried out. The charged resin is attracted toward the anode or cathode when a DC current is applied, and thus deposited on the electrode to give a coating. As the resin used in the present invention, it is possible to use resins conventionally used in electro-deposition coating, as exemplified by those of an acrylic melamine type, an acrylic type, an epoxy type, a urethane type, an alkyd type or the like. The resin used in the present invention may be of either an anionic type or a cationic type. From the viewpoint of practical use, it is preferred to use a water-soluble resin or water-dispersible resin having a carboxyl group. Resin prepolymers having carboxyl groups can be dissolved or dispersed in water after they have been neutralized with ammonia or organic amines.

The resin in the electro-deposition coating composition should be in a concentration of from 5% by weight to 20% by weight, and preferably from 7% by weight to 15% by weight.

The electro-deposition coating composition used in the present invention may preferably be prepared by dissolving or dispersing the desired resin in water. The electro-deposition coating composition may further contain an organic solvent of an alcohol type, a glycol type or the like. Such an organic solvent is enough if it is contained in an amount of several % by weight.

The insulating film **4** may be incorporated with a ceramic powder. The insulating film **4** incorporated with the ceramic powder can be well cured at a low temperature of, for example, from 90° C. to 100° C. when the insulating film **4** is heated to effect curing. As a result, it becomes possible to obtain a circuit substrate free from thermal deformation.

Although it is unclear why the heat curing can be carried out at a low temperature when the electro-deposition coating film is formed using an electro-deposition coating composition containing the ceramic powder, it can be presumed that the ceramic powder is different from metal particles whose surfaces are susceptible to immediate oxidation and its particle surfaces kept activated to a certain degree can be maintained in a stable state, so that the active particle surfaces of the powder serve as cross-link points at the time of curing to accelerate the curing of the coating formed by electro-deposition.

The ceramic powder incorporated into the insulating film **4** includes, for example, aluminum oxide, titanium nitride, manganese nitride, tungsten nitride, tungsten carbide, lanthanum nitride, aluminum silicate, molybdenum disulfide, titanium oxide, graphite, and silicic acid compounds.

A ceramic powder with an excessively large particle diameter brings about an excessive curing of the insulating film **4** to make the film brittle. On the other hand, a ceramic powder with an excessively small particle diameter makes it impossible to achieve a sufficient effect. Hence, the ceramic powder may preferably have an average particle diameter ranging from 0.1 μm to 5 μm, and particularly from 0.5 μm to 2 μm.

As to the amount of the ceramic powder contained in the electro-deposition coating composition used to form the insulating film **4**, the ceramic powder may preferably be in an amount of from 0.5 part by weight to 30 parts by weight, and particularly from 2 parts by weight to 25 parts by weight, based on 100 parts by weight of the resin feasible for electro-deposition, in order to obtain a coating that can give good coating film properties, e.g., adhesion, and also can be cured even at a low temperature. The ceramic powder may preferably be contained in the insulating film **4** in a deposition quantity of from 10% by weight to 30% by weight, and particularly from 15% by weight to 25% by weight.

The reason why the powder can be deposited in the coating formed as a result of the electro-deposition coating carried out using the electro-deposition coating composition containing the powder is presumed due to the fact that resin molecules are adsorbed around powder particles in the electro-deposition coating composition and the resin molecules are attracted toward the electrode, with which the powder also is moved toward the electrode.

After the formation of the insulating film **4**, the conductive film **3** is formed on the whole surface of the insulating film **4**. The conductive film **3** is formed by electro-deposition coating using an electro-deposition coating composition containing a conductive powder. As the conductive powder contained in the electro-deposition coating composition, it is preferred to use a ceramic powder whose particle surfaces are coated with a metal (hereinafter "metallized ceramic powder") or a natural mica powder whose particle surfaces are coated with a metal (hereinafter "metallized natural mica powder"). Only one of the metallized ceramic powder and the metallized natural mica powder may be contained in the electro-deposition coating composition, or both of them may be contained in the form of a mixture. Incorporation of the metallized ceramic powder or metallized natural mica powder in the electro-deposition deposition coating composition is preferable since, as previously described, it enables complete curing at a low temperature of from 90° C. to 100° C., which is usually required to be 130° C. to 180° C. as a heating temperature, when the electro-deposition coating is cured by heat treatment after completion of electro-deposition.

The metallized ceramic powder or metallized natural mica powder used in the present invention may include a ceramic powder or natural mica powder whose particles surfaces are coated with Cu, Ni, Ag, Au, Sn or the like. For the coating of the particle surfaces of these powders, Cu, Ag, and Ni can be preferably used in view of the shielding performance and cost. As a method for the coating of the powder particle surfaces, it is suitable to use electroless plating. A superior shielding performance and good coating film properties at the time of low-temperature curing can be obtained when the powder particle surfaces are coated in a coating thickness of from 0.05 μm to 3 μm, and particularly from 0.15 μm to 2 μm. Formation of coatings with a thickness of more

than 3 μm makes the surface properties analogous to those of metal particles, so that the coatings are oxidized in the air because of their very active surfaces to tend to result in an insufficient curing of electro-deposition coatings at the time of low-temperature curing.

When Ni coatings are formed on the powder particles, the method as disclosed, for example, in Japanese Patent Application Laid-open No. 61-276979 can be used, according to which a water-based suspension of the powder is prepared, and then an aged solution for electroless nickel plating is added to the suspension to form nickel coatings on the powder particle surfaces so that Ni coatings with a low phosphorus content, e.g., of 5% or less can be applied. Thus it is possible to form an electro-deposition coating having an improved conductivity and substantially the same shielding properties as in Cu-coated powder.

As the ceramic powder used in the conductive powder, it is possible to use the same ceramic powder as the one incorporated into the insulating film **4**. The natural mica may include phlogopite, serisite and muscovite.

The metallized ceramic powder and the metallized natural mica powder should have an average particle diameter of from 0.1 μm to 5 μm, and preferably from 0.5 μm to 2 μm. A powder with an average particle diameter smaller than 0.1 μm may cause secondary agglomeration. On the other hand, a powder with an average particle diameter larger than 5 μm is not preferred in view of a problem of sedimentation of particles or decorativeness of coating films.

As the conductive particles, in addition to the metallized ceramic powder and the metallized natural mica powder, it is also possible to use a resin powder whose particle surfaces are coated with a metal (hereinafter "metallized resin powder") or a metal powder.

As the resin powder used in the metallized resin powder, it is possible to use, for example, fluorine resins, polyethylene resins, acrylic resins, polystyrene resins and nylons. The metal coating applied to the surfaces of the resin powder particles may be the same as used in the case of the metallized ceramic powder. The metallized resin powder may also have the same average particle diameter as in the case of the metallized ceramic powder.

The metal powder includes, for example, powders of Au, Pd, Ag, Ni, Cu, Sn, Co, Mn, Fe, Te, etc. The metal powder should have an average particle diameter ranging from 0.01 μm to 5 μm, preferably from 0.05 μm to 4 μm, and more preferably from 0.05 μm to 0.1 μm. A powder with an average particle diameter smaller than 0.01 μm may cause secondary agglomeration. On the other hand, a powder with an average particle diameter larger than 5 μm may result in sedimentation of particles in the electro-deposition coating composition. It is preferred for the metal powder to be those produced by, for example, heat plasma evaporation.

In the present invention, the particle diameters of the conductive powder are values measured using a centrifugal sedimentation type particle size distribution measuring device. What is actually used as this measuring device is SACP-3 (trade name; manufactured by Shimadzu Corporation).

The conductive powder should be contained in the electro-deposition coating composition in an amount ranging from 0.2 part by weight to 30 parts by weight, preferably from 10 parts by weight to 20 parts by weight, and more preferably from 7 parts by weight to 15 parts by weight, based on 100 parts by weight of the resin feasible for electro-deposition.

The presence of the conductive powder in the conductive film **3** can be determined using an X-ray microanalyzer. The deposition quantity of the conductive powder can be measured by analysis according to thermogravimetry analysis. The deposition quantity of the conductive powder in the coating film **3** may preferably be in the range of from 5% by weight to 50% by weight, particularly from 10 % by weight to 40% by weight, and more preferably from 15% by weight to 35% by weight.

As the conductive powder contained in the conductive film **3**, only one of the metallized ceramic powder, the metallized natural mica powder, the metallized resin powder and the metal powder may be used, or two or more of them as exemplified by the metallized ceramic powder and the metal powder may be used. It is preferred to use a conductive powder comprised of a mixture of at lease one conductive powder selected from the metallized ceramic powder and the metallized natural mica powder and at least one conductive powder selected from the metallized resin powder and the metal powder. This is because the gaps between particles of the metallized ceramic powder and/or metallized natural mica powder are filled with particles of the metal powder and/or metallized resin powder to increase contact areas between each powder, so that the shielding properties can be more improved and also the conductive film **3** can be cured at the low temperature by the action of the metallized ceramic powder and/or metallized natural mica powder. In this instance, the conductive powders may preferably be mixed in such a proportion that at least one conductive powder selected from the metallized resin powder and the metal powder is in an amount of from 20 parts by weight to 300 parts by weight based on 100 parts by weight of at least one conductive powder selected from the metallized ceramic powder and metallized natural mica powder.

Because of the formation of the conductive film **3** by electro-deposition coating, the conductive powder can be deposited in the conductive film **3** in a high density, and the film **3** can exhibit a superior shielding performance even if it is a thin film.

After the formation of the conductive film **3**, the insulating film **5** is optionally formed on the whole surface of the conductive film **3**. The insulating film **5** may be formed using the same material as the materials described in respect of the insulating film **4** and in the same manner as the formation of the insulating film **4**. Accordingly, the ceramic powder may be incorporated or need not be incorporated also in respect of the insulating film **5**. The ceramic powder may be contained in both the insulating film **4** and insulating film **5** or may be contained in only one of them. Alternatively, the ceramic powder may be contained in neither the insulating film **4** nor the insulating film **5**.

After the insulating film **4**, the conductive film **3** and the optional insulating film **5** are formed on the whole surface of the conductor wire **2**, the insulating films **4** and **5** and the conductive film **3** are cured by heat or light, or by both of them. The energy by which the resin is cured may be either of heat and light, but heat is preferred in view of the advantage that it can be applied uniformly and yet with ease. The films may be cured preferably at a temperature of from 90° C. to 100° C. for a heating time of from 20 minutes to 180 minutes. It is also possible to effect curing of the insulating films or

the conductive film by the use of energy other than heat and light.

The insulating film **4** may preferably have a thickness of from 5 μm to 30 μm, and more preferably from 7 μm to 25 μm.

The conductive film **3** may preferably have a thickness of from 7 μm to 40 μm, and more preferably from 10 μm to 25 μm.

The insulating film **5** optionally provided may preferably have a thickness of from 10 μm to 30 μm, and more preferably from 10 μm to 25 μm.

In the case when the insulating films **4** and **5** and the conductive film **3** are formed by electro-deposition coating, the substrate made to serve as one electrode is immersed in an electro-deposition coating composition together with the other electrode to carry out the electro-deposition coating. The electro-deposition coating composition may preferably be kept at a temperature of from 20° C. to 25° C. and have a hydrogen-ion concentration corresponding to pH 8 to 9. The voltage to be applied may preferably be a DC voltage of from 50 V to 170 V and the electro-deposition may preferably be carried out at a current density of from 0.5 A/dm^2 to 3 A/dm^2 for a treatment time of from 1 minute to 5 minutes. The resins used for the insulating films **4** and **5** and the conductive film **3** may be changed in their kinds for each film.

As described above, the present invention makes it possible to form the insulating film and conductive film of a circuit substrate as thin films which are dense and uniform in thickness. It also makes it possible to obtain a circuit substrate free from defective insulation and having a superior electromagnetic wave shielding effect.

The present invention will be described below in greater detail by giving Examples. The present invention is by no means limited to these Examples only.

EXAMPLE 1

To the surface of a glass epoxy resin substrate of 0.6 mm thick, laminated thereon with copper foil of 18 μm thick, a negative resist (trade name: OMR-83; produced by Tokyo Ohka Kogyo Co., Ltd.; viscosity: 450 cp) was applied by spin coating to form a photosensitive material layer of 5 μm thick. Subsequently, the resist coating was exposed to light using pattern masks of from 0.5 to 50 mm in line width and from 1 to 20 mm in space, followed by development. Next, using a copper etchant (trade name: Alfine; produced by Uemura Kogyo K.K.), etching was carried out according to a spray system to form a copper circuit pattern.

Thereafter, using an electro-deposition coating composition prepared by diluting an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) with desalted water to a concentration of 15% by weight, a DC voltage of 150 V was applied for 3 minutes under conditions of pH 8.5 and a bath temperature of 25° C., setting the substrate as the anode and a stainless steel sheet as the cathode. Thus an insulating film **4** of 15 μm thick was formed on the copper circuit pattern.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts of an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 15 parts by weight of an alumina powder with an average particle diameter of 0.7 μm whose particle surfaces were coated with nickel in a thickness of 0.2 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 17 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance and specific volume resistance of the resulting circuit substrate were evaluated or measured. Results obtained are shown in Tables 1 to 3 below.

The resulting insulating film and conductive film were dense and well adhered to adjoining films, having satisfactory resistance to acids, resistance to alkalis and resistance to flame.

The electromagnetic wave shielding effect of the circuit substrate was also measured by the transmission line method (ASTM ES7-83 Method) after it was set in an apparatus. The result is shown in FIG. **2**. As shown in FIG. **2**, the electromagnetic wave shielding effect was substantially the same as in the case of electroless plating (see Reference Examples 1 and 2).

This circuit substrate was crosscut as shown in FIG. **1** to observe its cross section using a metallurgical microscope (magnifications: 400) manufactured by Olympus Optical Co., Ltd. As a result, it was confirmed that all the insulating films **4** and **5** and the conductive film **3** were formed in uniform thicknesses.

REFERENCE EXAMPLE 1

On an ABS resin substrate, a copper thin film of 0.7 μm thick and a nickel thin film of 0.4 μm thick were successively laminated by electroless plating to give a metal-coated member.

The electromagnetic wave shielding effect of this metal-coated member was measured in the same manner as in Example 1. The result is shown in FIG. **2**.

REFERENCE EXAMPLE 2

On an ABS resin substrate, a coating composition comprising a nickel powder was sprayed to form thereon a nickel coating.

The electromagnetic wave shielding effect of the resulting member on which this nickel coating had been formed was measured in the same manner as in Example 1. The result is shown in FIG. **2**.

COMPARATIVE EXAMPLE 1

To the surface of the same glass epoxy resin substrate as used in Example 1, a copper circuit pattern was formed in the same manner as in Example 1, and thereafter a solder resist (trade name: FINEDEL DSR-2200(C); produced by Tamura Seisakusho), a silver paste (trade name LS-500; produced by Asahi Kagaku Kenkyusho) and a solder resist (trade name: FINEDEL DSR-2200(C); produced by Tamura Seisakusho) were applied successively from the substrate side in thick-

nesses of 30 μm, 35 μm and 30 μm, respectively, to give a circuit substrate.

Physical properties, insulation resistance and specific volume resistance of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. Results obtained are shown in Tables 1 to 3.

TABLE 1

Results of Evaluation on Physical Properties of Film

Adhesion	Resistance to acids	Resistance to alkalis	Resist. to flame
Example 1:			
Adhesion rate: 100/100 Completely adhered.	No changes in insulating film.	No changes in insulating film.	Cleared 94V-0.
Comparative Example 1:			
Adhesion rate: 95/100 A little peeled.	A little change in insulating film.	A little change in insulating film.	Cleared 94V-1.

Notes:
Tests on the items in the above table were carried out by the following methods:
(1) Adhesion: JIS D0202
(2) Resistance to acids: Immersion treatment with 10 vol. % H_2SO_4 at room temperature for 20 minutes.
(3) Resistance to alkalis: Immersion treatment with 5 wt. % NaOH at room temperature for 30 minutes.
(4) Resistance to flame: UL94 Test Method.

TABLE 2

Insulation Resistance of Film

	Initial value	After 96 hour moisture absorption treatment
Example 1:	$1.7 \times 10^{13}\ \Omega \cdot cm$	$1.5 \times 10^{13}\ \Omega \cdot cm$
Comparative Example 1:	$1.0 \times 10^{13}\ \Omega \cdot cm$	$1.6 \times 10^{11}\ \Omega \cdot cm$

Notes:
The insulation resistance in the above table was measured according to JIS Z3197; comb electrode G-10; substrate moisture absorption treatment: at 55° C., 98% RH, DC 500 V for 1 minute. The resistivity was measured using a insulation resistance measuring device HP4329A, manufactured by YHP Co.

TABLE 3

Specific Volume Resistance of Film

	Initial value	After 96 hour moisture absorption treatment
Example 1:	$1.5 \times 10^{13}\ \Omega \cdot cm$	$1.4 \times 10^{13}\ \Omega \cdot cm$
Comparative Example 1:	$1.2 \times 10^{13}\ \Omega \cdot cm$	$1.8 \times 10^{10}\ \Omega \cdot cm$

Notes:
The above specific resistivity was measured according to JIS C6481.

EXAMPLE 2

A circuit substrate of the present invention was prepared in the same manner as in Example 1 except that 15 parts by weight of the nickel-coated alumina powder used in Example 1 was replaced with 10 parts by weight of copper-coated alumina powder. Coating thickness of the copper-coated alumina powder was 0.2 μm. Average particle diameter of the alumina powder was 1.2 μm.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 3

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern and an insulating film **4** were formed in the same manner as in Example 1.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 7 parts by weight of an alumina powder with an average particle diameter of 1.0 μm whose particle surfaces were coated with copper in a thickness of 0.2 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 17 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame) and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 4

On a glass epoxy resin substrate of 0.8 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, using an electro-deposition coating composition prepared by diluting an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.) with desalted water to a concentration of 15% by weight, a DC voltage of 150 V was applied for 3 minutes under conditions of pH 8.5 and a bath temperature of 25° C., setting the substrate as the anode and a stainless steel sheet as the cathode. Thus an insulating film **4** of 15 μm thick was formed on the copper circuit pattern.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.) separately made ready for use, 7 parts by weight of an alumina powder with an average particle diameter of 1.0 μm whose particle surfaces were coated with nickel in a thickness of 0.1 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 17 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 5

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern and an insulating film **4** were formed in the same manner as in Example 1.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 10 parts by weight of a copper powder with an average particle diameter of 0.03 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 17 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 6

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern and an insulating film **4** were formed in the same manner as in Example 1.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 10 parts by weight of a copper powder with an average particle diameter of 0.02 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 15 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame) and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 7

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, using an electro-deposition coating composition prepared by diluting an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.) with desalted water to a concentration of 15% by weight, a DC voltage of 150 V was applied for 3 minutes under conditions of pH 8.5 and a bath temperature of 25° C., setting the substrate as the anode and a stainless steel sheet as the cathode. Thus an insulating film **4** of 15 μm thick was formed on the copper circuit pattern.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.) separately made ready for use, 15 parts by weight of a nickel powder with an average particle diameter of 0.03 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 20 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 8

A circuit substrate of the present invention was prepared in the same manner as in Example 1 except that 15 parts by weight of the nickel-coated alumina powder used in Example 1 was replaced with a mixture of 7 parts by weight of nickel-coated alumina powder and 5

parts by weight of copper powder. Coating thickness of the nickel-coated alumina powder was 0.2 μm. Average particle diameter of the alumina powder was 1.2 μm. Average particle diameter of the copper powder was 0.03 μm.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 9

A circuit substrate of the present invention was prepared in the same manner as in Example 6 except that 10 parts by weight of the copper powder used in Example 6 was replaced with a mixture of 5 parts by weight of nickel-coated alumina powder and 10 parts by weight of copper powder. Coating thickness of the nickel-coated alumina powder was 0.2 μm. Average particle diameter of the alumina powder was 1.0 μm. Average particle diameter of the copper powder was 0.02 μm.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame) and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 10

A circuit substrate of the present invention was prepared in the same manner as in Example 4 except that 7 parts by weight of the nickel-coated alumina powder used in Example 4 was replaced with a mixture of 7 parts by weight of copper-coated alumina powder and 5 parts by weight of nickel powder. Coating thickness of the copper-coated alumina powder was 0.2 μm. Average particle diameter of the alumina powder was 1.0 μm. Average particle diameter of the nickel powder was 0.03 μm.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame) insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 11

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, using an electro-deposition coating composition prepared by dispersing, in an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.), aluminum nitride with an average particle diameter of 1.5 μm in a concentration of 3% by weight of the resin and then diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a DC voltage of 150 V was applied for 3 minutes under conditions of pH 8.5 and a bath temperature of 25° C., setting the substrate as the anode and a stainless steel sheet as the cathode. Thus an insulating film 4 of 15 μm in thickness and 25% by weight in deposition quantity of the powder was formed on the copper circuit pattern.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 10 parts by weight of an alumina powder with an average particle diameter of 1.0 μm whose particle surfaces were coated with nickel in a thickness of 0.1 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film 3 of 17 μm in thickness and 30% by weight in deposition quantity of the powder was formed on the whole surface of the insulating film 4 under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film 5 of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance, hardness (pencil) and resistance to scratching (eraser) of the resulting circuit substrate were evaluated or measured. Results obtained are shown in Tables 4 to 6 below.

The resulting insulating film and conductive film were dense and well adhered to adjoining films, having satisfactory resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching.

The electromagnetic wave shielding effect of the circuit substrate was also measured by the transmission line method after it was set in an apparatus. As a result, the electromagnetic wave shielding effect was as good as that in Example 1.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

TABLE 4

Results of Evaluation on Physical Properties of Film					
Adhesion	Resistance to acids	Resistance to alkalis	Resistance to flame	Hardness	<1>
Example 11:*					
Adhesion rate: 100/100 Completely adhered.	No changes in insulating film.	No changes in insulating film.	Cleared 94V-0.	4 H	>700
Comparative Example 1:					
See	See	See	See	2 H	<100*

TABLE 4-continued

Results of Evaluation on Physical Properties of Film					
Adhesion	Resistance to acids	Resistance to alkalis	Resistance to flame	Hardness	<1>
Table 1.	Table 1.	Table 1.	Table 1.	to H	

<1>: Resistance to scratching
*times
Notes:
Tests on the items in the above table were carried out by the following methods:
(1) Adhesion: JIS D0202
(2) Resistance to acid: Immersion treatment with 10 Vol. % H_2SO_4 at room temperature for 20 minutes.
(3) Resistance to alkali: Immersion treatment with 5 wt. % NaOH at room temperature for 30 minutes.
(4) Resistance to flame: UL94 Test Method.
(5) Hardness: JIS K5400
(6) Resistance to scratching: The times required until the substrate was exposed when the insulating film was rubbed with an eraser.

TABLE 5

Insulation Resistance of Film		
	Initial value	After 96 hour moisture absorption treatment
Example 1:	$1.3 \times 10^{13}\ \Omega \cdot cm$	$1.2 \times 10^{13}\ \Omega \cdot cm$

Notes:
The insulation resistance in the above table was measured according to JIS Z3197; comb electrode G-10; substrate moisture absorption treatment: at 55° C., 98% RH, DC 500 V for 1 minute. The resistivity was measured using a insulation resistance measuring device HP4329A. manufactured by YHP Co.

TABLE 6

Specific Volume Resistance of Film		
	Initial value	After 96 hour moisture absorption treatment
Example 1:	$1.0 \times 10^{13}\ \Omega \cdot cm$	$1.3 \times 10^{13}\ \Omega \cdot cm$

Notes:
The above specific resistivity was measured according to JIS C6481.

EXAMPLE 12

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, an insulating film **4** was formed thereon in the same manner as in Example 11 except that 3% by weight of the aluminum nitride powder used for the insulating film **4** in Example 11 was replaced with 5% by weight of an alumina powder with an average particle diameter of 1.0 μm.

Next, in an electo-deposition coating composition prepared by dispersing, in 100 parts by weight of an acrylic malamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 15 parts by weight of an alumina powder with an average particle diameter of 1.0 μm whose particle surfaces were coated with nickel in a thickness of 0.3 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 15 μm in thickness and 27% by weight in deposition quantity of the powder was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 13

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, using an electro-deposition coating composition prepared by dispersing, in an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.), silicon carbide with an average particle diameter of 2.0 μm in a concentration of 1% by weight of the resin and then diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a DC voltage of 150 V was applied for 3 minutes under conditions of pH 8.5 and a bath temperature of 25° C., setting the substrate as the anode and a stainless steel sheet as the cathode. Thus an insulating film **4** of the 15 μm in thickness and 25% by weight in deposition quantity of the powder was formed on the copper circuit pattern.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.) separately made ready for use, 10 parts by weight of an alumina powder with an average particle diameter of 1.0 **82** m whose particle surfaces were coated with copper in a thickness of 0.2 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 17 μm in thickness and 30% by weight in deposition quantity of the powder was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 14

On glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, an insulating film **4** was formed thereon in the same manner as in Example 11 except that 3% by weight of the aluminum nitride powder used for the insulating film **4** in Example 11 was replaced with 1.5% by weight of an alumina powder with an average particle diameter of 5.6 μm.

Next, the same conductive film **3** as in Example 11 was formed in the same manner as in Example 11.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching) and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thickness.

EXAMPLE 15

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern and an insulating film **4** were formed in the same manner as in Example 1.

Thereafter, the same conductive film **3** as in Eaxample 5 was formed in the same manner as in Example 5.

Then, the same insulating film **5** as in Example 11 was formed in the same manner as in Example 11, and finally the coatings were cured in the same manner as in Example 11. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 16

A circuit substrate of the present invention was prepared in the same manner as in Example 12 except that 10 parts by weight of the nickel-coated alumina powder used for the conductive film **3** in Example 12 was replaced with 5 parts by weight of a silver powder with an average particle diameter of 0.02 μm.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 17

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, an insulating film **4**, a conductive film **3** and an insulating film **5** were formed thereon in the same manner as in Example 11, Example 8 and Example 11, respectively.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thicknesses.

I claim:

1. A circuit substrate comprising a substrate, a conductive circuit pattern provided on said substrate, a first insulating film that covers said conductive circuit pattern, and a conductive film that covers said first insulating film, wherein both said first insulating film and said conductive film are formed by electro-depositing coating.

2. A circuit substrate according to claim **1**, wherein said conductive film is covered with a second insulating film.

3. A circuit substrate according to claim **2**, wherein said second insulating film is formed by electro-deposition coating.

4. A circuit substrate according to claim **1**, wherein said first insulating film comprises a ceramic powder.

5. A circuit substrate according to claim **3**, wherein said second insulating film comprises a ceramic powder.

6. A circuit substrate according to claim **1**, wherein said conductive film comprises a conductive powder.

7. A circuit substrate according to claim **6**, wherein said conductive powder comprises a material selected from the group consisting of a metallized ceramic powder and a metallized natural mica powder.

8. A circuit substrate according to claim **6**, wherein said conductive powder comprises a mixture selected from the group consisting of a metallized ceramic powder and a metallized natural mica powder and a material selected from the group consisting of a metallized resin powder and a metal powder.

9. A circuit substrate according to claim **1** wherein a second insulating film is provided to cover said conductive film, and said first insulating film, said conductive film and said second insulating film are all formed by electro-deposition coating.

10. A process for producing a circuit substrate, comprising a first step of forming on a substrate a circuit pattern comprising a conductor wire, a second step of porviding a first insulating film to cover the circuit

pattern, and a third step of providing a conductive film to cover the first insulating film, wherein said second step and said third step each comprises an electro-deposition coating, said electro-deposition coating being carried out by immersing said substrate in an electro-deposition coating composition, and setting the conductor wire as an electrode.

11. A process for producing a circuit substrate according to claim **10**, wherein the step of forming said conductive film is followed by a fourth step of providing a second insulating film to cover the conductive film.

12. A process for producing a circuit substrate according to claim **11**, wherein said fourth step comprises an elector-deposition coating.

13. A process for producing a circuit substrate according to claim **10**, wherein said second step comprises said electro-deposition coating, and wherein a ceramic powder is incorporated into said elecro-deposition coating composition to form the first insulating film.

14. A process for producing a circuit substrate according to claim **10**, wherein third step comprises said electro-deposition coating and wherein a conductive powder is incorporated into said electro-deposition coating composition to form the conductive film.

15. A process for producing a circuit substrate according to claim **14**, wherein said conductive powder comprises a material selected from the group consisting of a metallized ceramic powder and a metallized natural mica powder.

16. A process for producing a circuit substrate according to claim **14**, wherein said conductive powder comprises a mixture selected from the group consisting of a metallized ceramic powder and a metallized natural mica powder and a material selected from the group consisting of metallized resin powder and a metal powder.

17. A process for producing a circuit substrate according to cliam **10**, wherein said fourth step comprises said electro-depositing coating, and wherein a ceramic powder is incorporated into said electro-deposition coating composition to form the second insulating film.

18. A process for producing a circuit substrate according to claim **10**, wherein a fourth step is provided to form a second insulating film that covers the conductive film, and wherein said second step, said third step and said fourth step each comprises an electro-deposition.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,158,657

DATED : October 27, 1992

INVENTOR(S) : SUSUMU KADOKURA

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

COLUMN 1

Line 35, "a this" should read --a circuit. This--.
Line 55, "can" should read --that can--.

COLUMN 4

Line 48, "deposition" (second occurrence) should be deleted.

COLUMN 15

Line 47, "electo-deposition" should read --electro-deposition--.

COLUMN 16

Line 41, "1.0 82 m" should read --1.0 μm--.

COLUMN 17

Line 15, "5.6" should read --5.0--.

COLUMN 18

Line 60, "1 wherein" should read --1, wherein--.
Line 68, "porviding" should read --providing--.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,158,657

DATED : October 27, 1992

INVENTOR(S) : SUSUMU KADOKURA

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

COLUMN 19

Line 16, "elector-deposition" should read --electro-deposition--.
Line 20, "elecro-deposition" should read --electro-deposition--.
Line 24, "wherein third" should read --wherein said third--.

Signed and Sealed this

Thirtieth Day of November, 1993

Attest:

Attesting Officer

BRUCE LEHMAN

Commissioner of Patents and Trademarks

EXHIBIT C

The Judicial Decision from the District of Delaware

LG Display Co., LTD., vs AU Optronics Corporation

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU OPTRONICS CORPORATION AMERICA; CHI MEI OPTOELECTRONICS CORPORATION; and CHI MEI OPTOELECTRONICS USA, INC., Defendants.	:	Civil Action No. 06-726-JJF
AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG DISPLAY AMERICA, INC.,	:	Civil Action No. 07-357-JJF

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Attorneys for AU Optronics Corporation and AU Optronics Corporation America.

O P I N I O N

February 16, 2010

Wilmington, Delaware.

Farnan, District Judge.

These proceedings involve three related patent infringement cases involving 23 patents. In the first-filed action, LG Display Co., Ltd. ("LGD") alleges infringement of nine asserted patents (collectively, the "LGD Patents") against AU Optronics Corporation ("AUO") and Chi Mei Optoelectronics Corporation ("CMO"). AUO and CMO have also brought separate actions against LGD and LG Display America, Inc. ("LGD America") alleging infringement of eight patents asserted by AUO and six patents asserted by CMO.

Proceedings with respect to CMO have been stayed. The Court required the parties to reduce the number of patents and claims asserted to a total of four patents and seven claims per side.[1] As a result, LGD identified the following patents and claims for trial against AUO: U.S. Patent No. 5,019,002 (claim 8); U.S. Patent No. 5,825,449 (claims 10 and 11); U.S. Patent No. 6,815,321 (claims 7, 17 and 19) and U.S. Patent No. 7,218,374 (claim 9). AUO identified the following four patents and claims for trial against LGD and LGD America: U.S. Patent No. 6,778,160

[1] The Court notes that, in contravention of the spirit of the Court's order reducing the number of claims to be tried in this case, the parties chose to assert several dependent claims. In the case of AUO's asserted patents, the assertion of numerous dependent claims has expanded the number of claims asserted from the seven that the Court ordered as a means of streamlining this case to a total of 16 claims. Similarly, LGD's selection has resulted in a total of 11 claims being presented to the Court.

(claims 1 and 3); U.S. Patent No. 6,689,629 (claims 7 and 16); U.S. Patent No. 7,125,157 (claim 1) and U.S. Patent No. 7,090,506 (claims 7 and 17).

A bench trial was held on the claims brought by the parties and was bifurcated into two phases. The first phase of trial was held from June 2-8, 2009, and addressed AUO's infringement claims against LGD. The second phase of trial was held from June 16-22, 2009, and addressed LGD's infringement claims against AUO.

The claims and counterclaims for infringement and declaratory judgment in this case arise under the patent laws of the United States, Title 35, United States Code. Accordingly, the Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331, 1338(a), and 2201(a). Personal jurisdiction over the parties exists pursuant to 10 Del. C. § 3104, the Delaware long-arm statute. D.I. 1170 at 12. Likewise, venue in this district is appropriate under 28 U.S.C. §§ 1391(b), (c) and (d) and 1400. Neither jurisdiction nor venue is contested by the parties.

This Memorandum Opinion constitutes the Court's findings of fact and conclusions of law on the claims brought by the parties.

BACKGROUND

I. The Parties

LGD, formerly named LG Phillips LCD Co., Ltd., is a Korean corporation with a place of business in Korea. D.I. 1170 at Exh.

1, Stipulated Fact No. 1. LGD America is a California corporation with a place of business in San Jose, California. Id., Stipulated Fact No. 2. LGD and LGD America are collectively referred to as "LGD." Id., Stipulated Fact No. 3.

AU Optronics Corporation ("AUO") is a Taiwanese corporation with a place of business located in Taiwan. Id., Stipulated Fact No. 5. AU Optronics Corporation of America ("AUO America") is a California corporation with a place of business located in Santa Clara, California. Id. at Stipulated Fact No. 6. AUO Corp. and AUO America are collectively referred to as "AUO."

II. The Patents And The Technology Generally

The asserted patents relate to liquid crystal display ("LCD") products or methods of producing and assembling such products. Id., Stipulated Fact No. 13. An LCD is a flat panel display device that is used to generate images in a variety of products, including such devices as computer monitors, television screens, notebook computers and mobile phones. Id., Stipulated Fact No. 14.

DISCUSSION

I. Claim Construction

A. The Legal Principles of Claim Construction

Claim construction is a question of law. Markman v. Westview Instruments, Inc., 52 F.3d 967, 977-78 (Fed. Cir. 1995), aff'd, 517 U.S. 370, 388-90 (1996). When construing the claims

of a patent, a court considers the literal language of the claim, the patent specification and the prosecution history. Markman, 52 F.3d at 979. Of these sources, the specification is "always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term." Phillips v. AWH Corporation, 415 F.3d 1303, 1312-17 (Fed. Cir. 2005) (citing Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996)). However, "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" Liebel-Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 906 (Fed. Cir. 2004) (quoting Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1327 (Fed. Cir. 2002)).

A court may consider extrinsic evidence, including expert and inventor testimony, dictionaries, and learned treatises, in order to assist it in understanding the underlying technology, the meaning of terms to one skilled in the art and how the invention works. Phillips, 415 F.3d at 1318-19; Markman, 52 F.3d at 979-80. However, extrinsic evidence is considered less reliable and less useful in claim construction than the patent and its prosecution history. Phillips, 415 F.3d at 1318-19 (discussing "flaws" inherent in extrinsic evidence and noting

that extrinsic evidence "is unlikely to result in a reliable interpretation of a patent claim scope unless considered in the context of intrinsic evidence").

In addition to these fundamental claim construction principles, a court should also interpret the language in a claim by applying the ordinary and accustomed meaning of the words in the claim. Envirotech Corp. v. Al George, Inc., 730 F.2d 753, 759 (Fed. Cir. 1984). If the patent inventor clearly supplies a different meaning, however, then the claim should be interpreted according to the meaning supplied by the inventor. Markman, 52 F.3d at 980 (noting that patentee is free to be his own lexicographer, but emphasizing that any special definitions given to words must be clearly set forth in patent). If possible, claims should be construed to uphold validity. In re Yamamoto, 740 F.2d 1569, 1571 (Fed. Cir. 1984).

B. AUO's Patents

The parties dispute a number of claim terms from the asserted patents. The Court has selected for construction those terms that appear most pertinent to the disputes and trial positions argued by the parties in the post-trial briefing.[2]

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[2] The Court notes that claim construction in this case has been a "moving target." The parties have altered definitions that were advanced and have offered different terms for construction at different times during this litigation. In addition, the post-trial briefing between the parties is inconsistent as to which terms are genuinely in dispute. For example, disputed terms are identified in the post-trial briefing

1. U.S. Patent No. 6,778,160 (the "'160 patent")

AUO asserts claims 1 and 3 of the '160 patent. Claim 3 is a dependent claim that stems from claim 2. Accordingly, the relevant claims of the '160 patent are provided below, in full:

> 1. A liquid crystal display, comprising: an input logic for inputting a video signal from a host; a storage for storing the previous brightness level of the video signal input through said input logic; a determinator for determining an output brightness level based on the previous brightness level stored in said storage and the next brightness level of the next video signal input to said input logic so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level; and a driver for driving an image displaying liquid crystal cell based on said output brightness level determined by said determination logic.
>
> 2. The liquid crystal display according to claim 1, wherein said determinator comprising a table for storing a brightness level determined by the characteristic of a liquid crystal cell according to a relation between the previous brightness level and the next brightness level, and determining the output brightness level by modifying said next brightness level based on the brightness level read from said table.
>
> 3. The liquid crystal display according to claim 2, wherein: said video signal input through said input logic comprises a plurality of color signals; and said table in said determinator is provided for each of said color signals.

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in claim construction sections, and later, additional terms appear to be added for construction in the infringement sections of the briefs. The parties' inability to agree on the central terms for dispute and succinctly state their positions in a parallel format has enhanced the difficulty of this case.

The parties agree that one of ordinary skill in the art with respect to the '160 patent at the time of its filing is a person with at least a bachelor's degree in electrical engineering and several years experience working with liquid crystal displays, or the equivalent combined education and work experience. D.I. 1388 at ¶ 389; D.I. 1383 at ¶ 122.

a. **a storage for storing the previous brightness level**

The parties agree that the term "storage" refers to a "memory." D.I. 1388 at ¶ 390; D.I. 1387 at 23. The parties dispute the meaning of "brightness level." LGD contends that "brightness level" means a "gray scale value or luminance value" and proposes that the phrase "a storage for storing the previous brightness level" be defined as "memory that temporarily holds the brightness level of the video signal received from the host through input logic for the previous time increment." Id. at ¶ 394. AUO contends that the term "brightness level means "a level of intensity of light," and therefore, the term "a storage for storing the previous brightness level" should be defined as "memory for storing a previous level of light intensity of a video signal input through input logic." D.I. 376 at Exh. M-2.

After reviewing the claim language in light of the specification, the Court concludes that "brightness level" means a "level of intensity of light." This construction is consistent with the specification which explains that brightness "should be

considered in terms of the quantity of light." AUO-5 ('160 patent) at col. 8, ll. 32-35. While it is true that the specification suggests that a "brightness level can be represented as a target brightness by a gray scale," the Court does not read the specification to limit the representation of a video signal's brightness level to "gray scale values." Id. at col. 3, l. 67.

b. **determinator for determining an output brightness level**

AUO contends that this term means "logic, such as a circuitry, for determining an output brightness value. D.I. 376 at Exh. M—3. LGD contends that this phrase should be defined as "circuit or logic that determines the output brightness level by applying an offset to the next brightness level that is predetermined based on a difference in quantity of light between the actual and ideal response characteristics of the liquid crystal cell. D.I. 1388 at ¶ 395.

The parties are in agreement that this term refers to logic or circuitry. Their disagreement arises from LGD's additional limitations which purport to limit the manner in which the determinator determines the output brightness. The Court has reviewed the claim language in light of the specification, and concludes that such additional limitations are not required. Accordingly, the Court adopts AUO's proposed construction of the phrase "determinator for determining an output brightness level"

as "logic, such as a circuitry, for determining an output brightness value."

c. **so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level**

1. **substantially equal**

AUO contends that the term "substantially equal" should be construed in accordance with its plain meaning such that "substantially equal" means "a level that is not completely the same but can be accepted as a substantially equal level." LGD contends that the phrase "substantially equal" is indefinite, or in the alternative, should be construed as "a level which is not completely the same but can be accepted as a substantially equivalent level, and includes a level which is closer to an ideal quantity of light than [sic] no preventive measures are taken." D.I. 1388 at 101.

The Court concludes that the term "substantially equal" is not indefinite and should be defined as AUO proposes. This construction is consistent with the plain meaning of the term and the specification, which explains that the "representation 'substantially equal level' refers to a level which is not completely the same but can be accepted as a substantially equivalent level." '160 patent, col. 4, ll. 56-58; col. 9, ll. 19-23 (referring to Fig. 6 and the desire to obtain a "quantity of light (S") . . . which is approximately the same as the

quantity of light (S) . . . [from an LC with] ideal response characteristic[s] (S".S)"; col. 8, ll. 45-47 (quantity of light is "almost the same as" that of an ideal LC). In the Court's view, LGD's construction, improperly imports limitations from the preferred embodiment into the claims.

2. **time integration quantity of a brightness change/ideal quantity of light in a stationary state**

AUO contends that the term "time integration quantity of a brightness change" means "a quantity of light equal to the actual brightness level output through a liquid crystal, summed over the rise and fall response time of the liquid crystal." D.I. 376 at M-13. According to AUO, the plain meaning of "integration, in this context, is summing a change value (here, brightness level) over a period of time (here, the response time of the crystal)." Id. AUO also contends that the term "ideal quantity of light in a stationary state" refers to the "quantity of light emitted by a pixel during one time increment in which the pixel is in a non-changing state." Id.

LGD contends that these terms are indefinite. In the alternative, LGD appears to conflate the terms and offer a combined definition as follows: "quantity of light based on the actual response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness

level before and after the next time increment." D.I. 376 at Exh. M-13.

After reviewing the claim language in light of the specification, the Court concludes that the terms are not indefinite and will adopt AUO's proposed construction of these terms. The specification explains that the "[q]uantity of light can be considered as a time integration quantity of a brightness change." '160 patent, col. 4, ll. 53-57. The specification further explains that "brightness of a pixel to the human eye . . . should be considered in terms of the quantity of light, that is brightness change integrated with respect to time." Id. col. 8, ll. 30-34. In the Court's view, this supports AUO's position that the "time integration quantity of a brightness change" is the quantity of light that is emitted due to the change in brightness. LGD's proposed construction adds limitations that are not supported by the specification.

Likewise, the Court will adopt AUO's proposed construction of the term "ideal quantity of light in a stationary state." The specification teaches, by way of example, that an ideal quantity of light is that quantity of light output by an ideal LC over one time increment. Id., col. 4, ll. 42-47, Fig. 4. However, an ideal LC does not exist, id. at col. 8, ll. 63-65, and the specification's example teaches that the ideal quantity of light from a conventional LC is that quantity of light emitted from the

LC during one time increment when the brightness is constant, meaning the image is stationary. Id. col. 8, ll. 37-39 (when the particular pixel or LC is driven at a target brightness for an entire time increment, the pixel or LC may be described as being in a non-changing or "stationary state"). As with LGD's previous construction, its proposed construction of "ideal quantity of light in a stationary state" adds limitations that are not supported by the specification.

2. U.S. Patent No. 6,689,629 (the "'629 patent")

AUO asserts claims 7 and 16 against LGD. Claim 7 is a dependent claim which depends upon claim 4. Claim 4, in turn depends upon claim 2, and claim 2, depends on claim 1.

Similarly, Claim 16 is a dependent claim which depends on claim 13. Claim 13 in turn depends on claim 11. Claim 11 depends on claim 10, and claim 10 depends on independent claim 9.

Accordingly, the relevant claims of the '629 patent are provided below in full:

1. An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate; a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patterns are not in contact with any of the wiring.

2. The array substrate for display according to claim 1 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

4. The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

7. The array substrate for display according to claim 4 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

* * *

9. A method for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array formed on the insulating substrate, each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

> 10. The method for forming an array substrate for display according to claim 9 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.
>
> 11. The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring materials is selected from the group consisting of aluminum and aluminum alloys.
>
> 13. The method for forming an array substrate for display according to claim 11 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and allays thereof.
>
> 16. The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

The parties agree that one of ordinary skill in the art with respect to the '629 patent would be a person with at least a Bachelor's degree in chemical or electrical engineering, chemistry, or physics with 2 or more years experience working with liquid crystal display fabrication processing, or the equivalent combined education and work experience. D.I. 1383 at ¶ 299; D.I. 1388 at ¶ 132; Tr. 118:3-16 (Silzars).

a. **dummy conductive patterns**

LGD contends that the term "dummy conductive patterns" means "portions of the layer that do not receive or convey voltages or signals." D.I. 1388 at ¶ 133. Refining this construction further, LGD contends that this construction requires that the dummy patterns do not conduct or convey signals "at least during

testing or operation of the display." D.I. 1387 at 6. In this regard, LGD further contends that dummy patterns are structures that are put into the design of a product to aid in the manufacturing of the product, but do not have a function during the operation of the display. D.I. 1388 at ¶ 136-138. LGD contends that AUO has changed its position on the construction of this term, and that this change in position demonstrates that AUO's currently proposed definition should not be accepted.

AUO contends that the term "dummy conductive patterns" refers to "one or more metal patterns in the specified region that are not in contact with any of the wiring." D.I. 1384 at 24. AUO acknowledges that this construction is different than its previously proposed construction which was "a metal pattern that does not conduct signals or current used in the operation of the display." Id. at 25. However, AUO contends that its previous construction was too restrictive. In this regard, AUO contends that the wiring recited in the claims connects the connection pads to the transistors in the TFT array. AUO contends that dummy patterns are not needed for the operation of the transistors of the TFT array, and therefore, they "are not in contact with any of the wiring" that is "in communication with at least one of the transistors in the TFT array." Id., citing '629 patent, col. 8, ll. 14-19. However, AUO maintains that there is nothing in the intrinsic evidence that precludes the dummy

conductive patterns from performing some function, such as conducting a voltage or signal used in the operation of a display, so long as they are not in contact with the TFT wiring. AUO points out that even under its prior construction, nothing required dummy conductive patterns to be unable to receive any voltages or signals, and that the dummy conductive patterns could still be connected to a ground or voltage supply. D.I. 1384 at 24-26.

As the Federal Circuit has recognized, the Court's task in claim construction is not to decide which of the adversaries is correct, but to independently determine the meaning of disputed claims. Exxon Chem. Patents, Inc. v. Lubrizol Corp., 64 F.3d 1553, 1556 (Fed. Cir. 1995). For this reason, the Court does not take AUO's change in its claim construction position to be indicative of the merits of its current argument.

Reviewing the disputed term in light of the claim language and specification, the Court concludes that the term "dummy conductive patterns" is properly construed to mean "conductive patterns in the specified region that are not in contact with any of the wiring." The claim terms expressly state that the dummy conductive patterns must comprise "at least about 30% of the area" and "are not in contact with any of the wiring." '629 patent, col. 8, ll. 13-19, 57-63. The Court does not read the claims or the specification from precluding the dummy conductive

patterns from performing some function, so long as that they are not in contact with the TFT wiring. Accordingly, the Court concludes that LGD's claim construction and AUO's prior claim construction were both too restrictive, and that "dummy conducive patterns" are "conductive patterns in the specified region that are not in contact with any of the wiring."

b. **area**

LGD contends that the term "area" is indefinite because one of ordinary skill in the art would be unable to unambiguously discern the boundaries of the asserted claims. D.I. 1388 at ¶ 168-170. In this regard, LGD contends that there is no disclosure on how the 30% of the area should be calculated. Alternatively, LGD contends that the term "area" refers to "material deposited and patterned on a substrate, such as glass, that covers part of the array substrate surface." Id. at ¶ 171.

In response, AUO contends that "area" should be construed according to its ordinary meaning as a "specified region." D.I. 1384 at 23-24. Turning to the context of the claims more specifically, AUO contends that "area" refers to a region of the array substrate, specifically a region containing the dummy conductive patterns.

After reviewing the claim language in light of the specification, the Court concludes that the term "area" is not indefinite and should be construed according to its plain meaning

as a "specified region." In the Court's view, this is consistent with the specification which explains that the substrate coverage "of the dummy conductive patterns themselves [is] 30% or more on an area of a specified surface." '629 patent, col. 5, ll. 55-61. Similarly, the specification explains that "dummy conductive patterns are formed on an area of a specified region where the dummy conductive patterns are formed." Id., col. 6, ll. 1-6. Thus, the Court concludes that an "area" is "a specified region," more specifically, the region where dummy conductive patterns are located.

c. **a plurality of wiring / each wiring**

LGD contends that the term "each wiring" is indefinite, because it is unclear as to which wiring the term "each wiring" is referring from the plurality of wiring. LGD contends that "[t]o the extent the term 'each wiring' can be construed, the term 'a plurality of wiring arranged on the insulating substrate' should be construed to mean 'portions of the layer that convey voltages or signals from the connection pads to the thin-film transistors in the pixel array." D.I. 1407 at ¶ 56.

AUO contends that the these terms should be construed in accordance with their plain meaning in the context of the claim element in which they are used. Thus, AUO contends that "a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at

least one of the transistors in the thin film array" means "each individual wiring in a plurality of wirings," with the plurality of wirings being a plurality of electrical conductors. D.I. 1383 at ¶ 347. In this regard, AUO points out that the specification explains "this connection of 'each wiring' [by] describing 'wirings such as scan lines and signal lines connected with' the electrodes of the transistors." D.I. 1383 at ¶ 344 (citing '629 patent, col. 1, ll. 17-19, col. 4, ll. 49-51, Fig. 2).

The Court concludes that the terms "each wiring" and "plurality of wiring" as recited in the claim element "a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array" are not indefinite. The Court further concludes that these terms should be construed according to their plain meaning in the context of the patent, such that a plurality of wiring is a plurality of electrical conductors and "each wiring" is "each individual wiring in a plurality of wiring." '629 patent, col. 8, l. 6, 11, col. 8, ll. 54-55; Tr. 139:10-140:1 (Silzars).

d. the upper layer wiring material does not become insoluble in an acid or alkaline etchant

Although not identified in the parties' claim construction charts, it is apparent from their briefing that disputes exist regarding the proper construction and/or application of this

phrase. Specifically, AUO contends that the solubility issue in claim 7 and 16 must be evaluated in the context of a two layer structure - that is a wiring structure having a lower and upper layer of wiring. D.I. 1384 at 26-27.

LGD contends that AUO's interpretation of this claim improperly imports into the claims limitations contained in the specification. In particular, LGD contends that claim 7 and 16 do not refer to the passivity problem described in the specification and contain no limitation that the insolubility of the upper layer is during the etching process. D.I. 1406 at 17-18.

After reviewing the claim language in light of the specification, the Court concludes that the limitation of claim 7 and 16 must be read in the context of a two layer structure. Fuji Photo Film Co., Ltd. v. International Trade Com'n, 386 F.3d 1095 (Fed. Cir. 2004) ("Claims must be read in the context of the specification of which they are a part.") This reading is consistent with claims 7 and 16 which are dependent upon claims 2 and 10. Claims 2 and 10 expressly contemplate two layer wiring, and therefore, the claim language makes it evident, that it is within the context of two-layer wiring that solubility must be evaluated. In the Court's view, this is also consistent with the purpose of the invention which is to prevent the upper layer from becoming insoluble during etching of the two-layer wiring. Tr.

870:18-871:8, 872:9-13, 873:7-23 (Rubloff); Tr. 1388:20-1391:2 (Silzars). In this regard, the Court agrees with the testimony of Dr. Silzars that whether material would become insoluble if dropped by itself in a vat of etchant is irrelevant to the context of the claimed invention. Tr. 1388:20-24 (Silzars). Accordingly, the Court does not view its construction as importing limitations from the specification as LGD contends, but as an attempt to view the claim in its proper context.

3. U.S. Patent No. 7,125,157 (the "'157 patent")

AUO asserts independent claim 1 of the '157 patent. In full, claim 1 provides:

> 1. A backlight unit for a liquid crystal display, comprising: a frame; a first supporting portion, disposed on the frame; a second supporting portion, further disposed on the frame; and a film comprising a first constraining portion and a second constraining portion, positioned on the frame by the first supporting portion and the second supporting portion passing through the first constraining portion and the second constraining portion, respectively; when the frame is disposed in a first position, the first supporting portion partially contacts an inner wall of the first constraining portion for positioning the film, and the second supporting portion does not contact the second constraining portion; and when the frame is disposed in a second position, the second supporting portion partially contacts an inner wall of the second constraining portion for positioning the film and the first supporting portion does not contact the first constraining portion.

The parties agree that one of ordinary skill in the art with respect to the '157 patent at the time of its filing "would be a person with a bachelors degree in mechanical engineering or

physics and several years of experience working with aspects of the backlight modules for liquid crystal displays or the equivalent combined education and work experience." D.I. 1383 at ¶ 497; D.I. 1388 at ¶ 678; Tr. 207:24-208:12 (Silzars).

a. **supporting portion**

LGD contends that a "supporting portion" should be construed as a projection from the frame. D.I. 376 at Exh. Q-1. AUO contends that the "supporting portion" should not be limited to a projection, which may be defined to have a specified shape. Id.

The Court adopts AUO's construction of "supporting portion" as "any structure protruding from the frame, (including but not limited to a cylinder or a cuboid) intended to support the optical film." '157 patent, col. 2, ll. 61-62, col. 3, ll. 4-12, col. 4, ll. 17-24, Fig. 2A and 2B; col. 6, ll. 4-8, 31-42 Fig. 3A and 3B; Fig. 3C, col. 7, ll. 39-45, Fig. 4A-4D.

b. **constraining portion**

AUO contends that a constraining portion is "any formation on or in the optical film (including but not limited to a hole or groove) intended to restrict the movement range of the film." D.I. 376 at Exh. Q-2. LGD contends that this term should be defined as "a passage through the film that has a gap in the gravity acting direction after receiving a supporting portion." Id.

In the Court's view, LGD's construction improperly limits the constraining portion "to a passage through the film" and "a gap." This is contrary to the specification which expressly contemplates that a constraining portion may be a "groove" which does not equate with a "gap." '157 patent, col. 2, ll. 27-30, 63-65, col. 4, ll. 7-16.

c. **first position / second position**

With respect to the first and second orientations described in these terms, LGD argues that the first supporting portion or position must be located near an upper edge of the frame. LGD and AUO generally agree that the second position is determined by reference to the first position, but to the extent LGD's construction of the second position depends from its upper frame requirement of the first position, AUO contends that LGD's construction is incorrect. According to AUO, there is no upper edge location requirement and the first position is simply an initial position. D.I. 1383 at ¶¶ 513-516.

The Court agrees with AUO and concludes that no such upper edge limitation exists in the claim. In the Court's view, adopting LGD's proposal in this regard would improperly limit the claims to the preferred embodiments. Liebel-Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 906 (Fed. Cir. 2004). Accordingly, the Court concludes that a first position means "an initial position of a liquid crystal display unit" and a "second

position" means "the position determined by reference to the angle of rotation between the first and second position."

d. **does not contact**

LGD contends that the phrase "does not contact" means "does not touch;" however, LGD further explains that this "requires that a supporting portion does not touch a constraining portion when in a non-supporting position, including when the film expands or contracts due to temperature variation." D.I. 1388 at ¶ 681. AUO contends that this phrase should be construed according to its plain meaning and should not include any thermal expansion and contraction limitations. In this regard, AUO points out that such limitations are included in dependent claim 9, and therefore, the doctrine of claim differentiation should preclude claim 1 from being construed to include these additional limitations. D.I. 1384 at 40-41; D.I. 1440 at 17.

Claim differentiation "refers to the presumption that an independent claim should not be construed as requiring a limitation added by a dependent claim." Curtiss-Wright Control Corp. v. Velan, Inc., 438 F.3d 1374, 1380 (Fed. Cir. 2006). However, claim construction positions based on claim differentiation are rebuttable, taking a secondary role if an alternate construction is dictated by the written description or prosecution history. See Regents of the Univ. of Cal. v. Dakocytomation Cal., Inc., 517 F.3d 1364, 1375 (Fed. Cir. 2008).

After reviewing the claim language, specification and prosecution history, the Court concludes that the term "does not contact" should be construed as AUO proposes, according to its plain meaning without the additional temperature and thermal contraction and expansion limitations from claim 9 that inform LGD's proposed claim construction. Claim 9 depends on claim 1 and adds the limitations that "when the frame is disposed in the second position, a first gap is formed between the first supporting portion and the first constraining portion, and the first gap is an allowance for film expansion or contraction due to temperature variation; when the frame is disposed in the first position, a second gap is formed between the second supporting portion and the second constraining portion, and the second gap is an allowance for film expansion or contraction due to temperature variation." '157 patent, col. 9, ll. 16-20. During prosecution of the application for the '157 patent, the Examiner did not require the applicant to combine the elements of claims 1 and 9 into a single claim, and instead determined that claim 1 was separately patentable without any of the limitations of claim 9. AUO-10 at AUO-LGD 0001333, 0001452, 0001487-88; Tr. 1202:21-1203:6 (Smith-Gillespie). LGD points out that the embodiments of the '157 patent refer to thermal considerations, however limitations from the specification should not be read into claims. Claim 1 has no limitation relating to thermal expansion

or contraction, and the Court is persuaded that, consistent with the doctrine of claim differentiation, claim 1 should not be read in a manner so as to incorporate the limitations of claim 9.

4. U.S. Patent No. 7,090,506 (the "'506 patent")

AUO asserts claim 7 and 17 of the '506 patent. Claim 7 is a dependent claim that depends on independent claim 1. Claim 17 is also an independent claim. Accordingly, the relevant claims of the '506 patent provide, in full:

> 1. A signal transmission device, connecting a display module and a system, comprising: a first flexible printed circuit board, electrically connecting the display module and the system and a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board, wherein the first and second flexible printed circuit boards are joined by hot bar soldering.
>
> 7. The signal transmission device as claimed in claim 1, wherein the second flexible printed circuit board transmits a light source signal.
>
> 17. A signal transmission device, connecting an display module and a system, comprising: a first flexible printed circuit board, electrically connecting the display module and the system; and a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board, wherein the first flexible printed circuit board has a first alignment mark, and the second flexible printed circuit board has a second alignment mark overlapped with and aligned to the first alignment mark.

The parties agree that a person of ordinary skill in the art of the '506 patent is a person with a bachelors degree in mechanical engineering or physics and several years of experience working with aspects of liquid crystal display, or the equivalent

combined education and work experience. D.I. 1383 at ¶ 571; Tr. 227:12-20 (Silzars).

a. **the first and second flexible printed circuit boards are joined by hot bar soldering**

LGD contends that this term describes a process by which the circuit boards are joined, and is thus, a process limitation. LGD contends that the term "the first and second flexible printed circuit boards are joined by hot bar soldering" means

> both flexible printed circuit boards are connected to each other by a soldering process where the circuit boards are heated with a bar to melt the solder at multiple points simultaneously along each circuit board while pressure is applied to the connection.

D.I. 1388 at ¶ 541.

In response, AUO contends that this term is not a process limitation, but a structural limitation. In this regard, AUO contends that claim 1 does not include any of the typical product-by-process language and is a pure product claim defined solely by structural limitations. Thus, AUO contends that "joined by hot bar soldering" means "joined by solder material." D.I. 1384 at 45. Alternatively, AUO contends that if this term is construed as a process limitation, it should be construed as

> the first and second printed circuits made on flexible film are joined by a soldering process where the solder and flux are applied to the contact area and the contact area is heated with a bar to melt the solder.

D.I. 376 at Exh. O-4. AUO contends that LGD's construction is overly narrow, because hot bar soldering does not require

"pressure" beyond that which is necessary to hold the two items being soldered together and does not require melting solder at "multiple" contact points.

"Courts must generally take care to avoid reading process limitations into an apparatus claim . . . ." Baldwin Graphic Systems, Inc. v. Siebert, Inc., 512 F.3d 1338, 1344 (Fed. Cir. 2008). "Even where terms are amenable to interpretation as a procedure of manufacture, apparent 'process' terms should be interpreted as structural limitations when used in an adjective non-process sense and define a physical characteristic of the apparatus." R2 Medical Sys., Inc. v. Katecho, Inc., 931 F. Supp. 1392, 1425 n.5 (N.D. Ill. 1996) (citing 2 Donald S. Chisum, Patents § 8.05[5], at 8-96 (1994)); Biacore v. Thermo Bioanalysis Corp., 79 F. Supp. 2d 422, 456 (D. Del. 1999) ("The mere use in a claim of structural or characterizing terms derived from processes or methods, however, does not prevent a claim from being considered a true product claim.")

Considering the claim language in light of the specification and prosecution history, the Court concludes that the limitation "joined by hot bar soldering" does not amount to a process limitation, but instead describes the structural relationship between the first and second flexible printed circuit boards. Claim 1 of the '506 patent was distinguished over the prior art based on the limitation requiring that solder material join the

two flexible printed circuit boards rather than a foldable flat cable. AUO-12 at AUO-LGD 1948. Thus, the Court views the soldering described in this claim as a structural limitation. Accordingly, the Court construes the phrase "first and second printed circuit boards are joined by hot bar soldering" to mean that the "first and second printed circuit boards are joined by solder material."[3]

b. **alignment mark**

During the claim construction proceedings in this case, neither party proposed a construction for the term "alignment mark." However, it appears that post-trial the parties are now disputing the meaning of this term. According to LGD, a person of ordinary skill in the art would understand an "alignment mark" to "be a distinctive identifying feature that is provided solely for positioning of the flexible printed circuit boards during assembly." D.I. 1388 at ¶ 544.

In response, AUO contends that alignment marks can have more than one purpose. For example, they can function for both

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[3] Even if the Court concludes that this phrase is a process limitation, the Court concludes LGD's proposed construction is too narrow. In reaching this conclusion, the Court credits the testimony of Dr. Silzars regarding the hot bar soldering process. Specifically, Dr. Silzars explained that hot bar soldering requires applying a hot bar to a solder joint. However, this does not require that multiple joints be soldered simultaneously, and the Court finds no support for this additional limitation in the patent specification or prosecution history. Tr. 320:19-322:11, 336:11-18 (Silzars).

positioning and bonding. Thus, AUO contends that LGD's definition of alignment marks is too restrictive, and "alignment marks" should be more broadly defined as patterns used for accurate positioning and connection of flexible printed circuit boards. D.I. 1383 at ¶¶ 657-663; D.I. 1384 at 46, 50.

Reviewing this claim term in light of the specification of the '506 patent, the Court concludes that AUO's more expansive definition is correct. The '506 patent discloses more than one type of alignment mark. For example, pad electrodes are disclosed on the first and second printed boards in Figure 3a. These pad electrodes serve as both alignment marks for positioning and as contact pads for bonding or electrically joining two flexible printed circuit boards. '506 patent, col. 2, ll. 26-38. Accordingly, the Court concludes that an alignment mark is a pattern used for accurate positioning and connection of flexible printed circuit boards.

II. Direct Infringement

A. Applicable Law

A patent is infringed when a person "without authority makes, uses or sells any patented invention, within the United States during the term of the patent . . . ." 35 U.S.C. § 271(a). A patent owner may prove infringement under either of two theories: literal infringement or the doctrine of equivalents. Literal infringement occurs where each element of at least one

claim of the patent is found in the alleged infringer's product. Panduit Corp. v. Dennison Mfg. Co., 836 F.2d 1329, 1330 n. 1 (Fed. Cir. 1987); Robert L. Harmon, Patents and the Federal Circuit 195 & n. 31 (3d ed. 1994).

"The doctrine of equivalents allows the patentee to claim those insubstantial alterations that were not captured in drafting the original patent claim but which could be created through trivial changes." Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., 535 U.S. 722, 733 (U.S. 2002). "An element in the accused device is equivalent to a claim limitation if the only differences between the two are insubstantial." Honeywell Int'l v. Hamilton Sundstrand Corp., 370 F.3d 1131, 1139 (Fed. Cir. 2004). To prove infringement by the doctrine of equivalents, a patentee must provide "particularized testimony and linking argument" as to the "insubstantiality of the differences" between the claimed invention and the accused product, or with respect to the function/way/result test. See Texas Instruments Inc. v. Cypress Semiconductor Corp., 90 F.3d 1558, 1567 (Fed. Cir. 1996). "[E]vidence and argument on the doctrine of equivalents cannot merely be subsumed in plaintiff's case of literal infringement." Lear Siegler, Inc. v. Sealy Mattress Co., 873 F.2d 1422, 1425 (Fed. Cir. 1989).

Infringement is a two step inquiry. Step one requires a court to construe the disputed terms of the patent at issue.

Construction of the claims is a question of law subject to de novo review. See Cybor Corp. v. FAS Techs., 138 F.3d 1448, 1454 (Fed. Cir. 1998). Step two requires the fact-finder to compare the accused products with the properly construed claims of the patent. This second step is a question of fact. See Bai v. L & L Wings, Inc., 160 F.3d 1350, 1353 (Fed. Cir. 1998). The party asserting infringement under either the theory of literal infringement or the doctrine of equivalents has the burden of proof and must meet its burden by a preponderance of the evidence. SmithKline Diagnostics, Inc. v. Helena Lab. Corp., 859 F.2d 878, 889 (Fed. Cir. 1988) (citations omitted).

B. Whether LGD Infringes claims 1 and 3 of AUO's '160 Patent

After comparing LGD's accused products with claims 1 and 3 of the '160 patent, the Court concludes that AUO has established by a preponderance of the evidence that LGD literally infringes the '160 patent.[4] In reaching this conclusion, the Court credits the testimony of Dr. Silzars.

[4] LCD modules that include the New Monde chip are representative of the accused products. Tr. 169:6-170:18 (Silzars); AUO-1553. For purposes of infringement, the Court finds that there are no relevant differences between the LGD products that Dr. Silzars analyzed. Tr. 169:6-169:11 (Silzars). In addition, the accused LGD products that use overdrive are the same for purposes of infringement, based on Dr. Silzars' examination of the products and his analysis of the specification and the testimony of LGD witnesses. Tr. 169:12-23.

Claim 1 Preamble: A liquid crystal display, comprising

LGD does not dispute that this element of the claims is present in the accused devices, and the Court finds that LGD's accused display modules are liquid crystal displays. AUO-164 at 1/51; AUO-859.

Claim 1: an input logic for inputting a video signal from a host

Page 1 of the New Monde specification shows that the New Monde timing controller chip includes LVDS input logic for inputting a video signal from a host. AUO-165 at 1/51; Tr. 173:19-174:17 (Silzars). All of the timing controllers in the accused LGD modules receive an LVDS input through an input logic, the LVDS interface. AUO-1533; AUO-135 at 1/46; AUO-160 at 1/36; AUO 161 at 1/36; AUO 149 at 1/50; AUO 150 at 1/50; AUO-155 at 2/41; AUO 156 at 2/41; AUO-157 at 1/35; AUO-158 at 1/35; AUO-159 at 2/41; AUO-137 at 1/48; AUO-138 at 1/48; AUO-145 at 1/45; AUO-146 at 1/45; AUO-143 at 1/46; AUO-144 at 1/46; AUO-133 at 1/53; AUO-134 at 1/53; AUO-167 at 1/51; AUO-168 at 1/51; AUO-151 at 1/51; AUO-152 at 1/51; AUO-153 at 2/35; AUO-154 at 2/35; AUO-162 at 2/33; AUO-169 at 1/51; AUO-170 at 1/51; AUO-164 at 1/51; AUO-165 at 1/51; AUO-139 at 1/45; AUO-140 at 1/45; AUO-131 at 1/44; AUO-132 at 1/44; AUO-166 at 2/39; AUO-141 at 1/25; AUO-142 at 1/25; AUO-147 at 1/47; AUO-148 at 1/47.

Claim 1: storage for storing the previous brightness level of the video signal input through said input logic

The Court finds that the accused devices meet this claim element. The frame memory is the "storage for storing." The system block diagram of New Monde includes a "frame memory" identified as the "Frame Memory SDRAM" in the System Block Diagram and as a Field Store, in the Over Driving Scheme Diagram. Tr. 177:14-179:7 (Silzars); AUO-164/165 at 1/51 and 4/51. The frame memory stores the previous level of light intensity of the video signal input through the input logic. The frame memory temporarily holds the brightness level of the video signal received from the host through input logic for the previous time increment. Tr. 178:13-179:7 (Silzars); AUO-165 at 1. Each of the timing controller chips analyzed by Dr. Silzars is used in a system that includes a similar frame memory SDRAM, also called the Field Store in the Over Driving Scheme block diagram. AUO-1533; AUO-1553; AUO-135 at 1/46 and 4/46; AUO-136 at 1/46 and 4/46; AUO-160 at 1/36 and 3/36; AUO-161 at 1/36 and 3/36; AUO-149 at 150 and 4/50; AUO-150 at 1/50 and 4/50; AUO-155 at 2/41; AUO-156-2/41; AUO-157 at 3/35; AUO-158 at 3/35; AUO-159 at 2/41; AUO-137 at 1/48 and 4/48; AUO-138 at 1/48 and 4/48; AUO-145 at 1/45 and 4/45; AUO-146 at 1/45 and 4/45; AUO-143 at 1/46 and 4/46; AUO-144 at 1/46 and 4/46; AUO-133 at 3/53 and 4/53; AUO-134 at 3/53 and 4/53; AUO-167 at 1/51 and 4/51; AUO-168 at 1/51 and

4/51; AUO-151 at 1/51 and 4/51; AUO-152 at 4/51; AUO-153 at 2/35; AUO-154 at 2/35; AUO-162 at 2/33; AUO-169 at 1/51 and 4/51; AUO-170 at 1/51 and 4/51; AUO-164 at 1/51 and 4/51; AUO-165 at 1/51 and 4/51; AUO-139 at 1/45 and 4/45; AUO-140 at 1/45 and 4/45; AUO-131 at 3/44 and 4/44; AUO-132 at 3/44 and 4/44; AUO-166 at 2/39; AUO-141 at 2/25 and 4/25; AUO-142 at 2/25 and 4/25; AUO-147 at 1/47 and 4/47 and AUO-148 at 1/47 and 4/47.

LGD contends that the accused products do not meet this claim limitation, because the accused timing controllers store compressed data that represents a comparison of brightness levels to the average grayscale level of a block of liquid crystal cells. LGD contends that the compressed data is not actual previous brightness levels, nor can it be used to recreate actual previous brightness levels.

However, the Court finds that LGD's contentions are not supported by the record. The compressed data is used to recreate actual brightness levels. This is supported by LDG's presentation, AUO-1538 at page 9, which describes the decompressed data as the "reconstructed previous frame." This is also supported by the testimony of LGD's witness, Mr. Kim, who testified that decompression recovers "the original image or close to the original image" and that ideally the decompressed data is "identical" to the original data but there may be "some small," "acceptable" changes. Tr. 78:5-22 (C.G. Kim); Tr.

179:22-181:22 (Silzars). While it is true that the decompressed data is not used to actually display the images, it is used to look up overdrive values, which in turn display the image. Thus, errors in the decompressed data would impact the quality of the displayed image. Tr. 1363:3-1364:9 (Silzars). In sum, the Court concludes that the timing controllers do store the actual previous brightness levels in compressed form, and therefore, the Court finds that the accused devices meet the "storage for storing the previous brightness level of the video signal input through said input logic" claim element.

Claim 1: a determinator for determining an output brightness level based on the previous brightness level stored in said storage and the next brightness level of the next video signal input to said input logic

The Court concludes that the accused devices meet this claim limitation, because LGD's timing controller chips include a lookup table, which is the determinator for determining an output brightness level. The brightness level output by the lookup table is based on the previous brightness level, which was stored in the frame memory, and the next brightness level. In the example of the New Monde lookup table, the brightness level for the previous frame and the current frame ranges from 0 to 255. Tr. 172:14-173:9 (Silzars); AUO-165 at 26/51. The lookup table is used to compare the video information (i.e. the brightness level) in the previous frame to the brightness information in the current frame and apply a correction. Tr. 171:15-172:13

(Silzars); AUO-165 at 4/51. Each of the timing controllers analyzed by Dr. Silzars includes a similar lookup table.

LGD's argument that this claim limitation is not met relates to its argument regarding the storage of previous brightness levels, which the Court has declined to accept. In addition, LGD argues that the timing controllers in the accused products do not use "offset" values as required by the limitation "a determinator for determining an output brightness level." However, the claim terms do not include the term "offset," and the Court is not persuaded that an "offset" should be read into the accused devices. Accordingly, the Court concludes that the accused devices satisfy this claim limitation.

Claim 1: so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level

The Court concludes that the accused products meet the limitations of this claim element. The determinator must provide an output brightness level that achieves the claimed results: a time integration of a brightness change that is substantially equal to an ideal quantity of light. Dr. Silzars tested the accused products, measuring the brightness change and noting that the brightness change was within 20% of the ideal response. See e.g. AUO-1075; Tr. 193:17-195:8; 1370:23-1372:9 (Silzars).

LGD contends that Dr. Silzars's test results are inaccurate for several reasons, including that Dr. Silzars's calculations

did not reflect the "total amount of light" that would be emitted from the liquid crystal cell. Based on the Court's claim construction, however, the claims do not refer to the total amount of light that would be emitted by an ideal liquid crystal cell. Rather, the claims are directed to the amount of light that would be emitted due to the brightness change. Further, the Court credits Dr. Silzars's test results, and concludes, based on his testimony, that a brightness change within 20% is substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level.

LGD's argument that this claim element is not met in the accused devices is premised on the notion that "substantially equal" should also represent an improvement in the context of the "ideal quality of light." However, the Court has not included this additional language in its construction of the relevant terms, and therefore, the Court concludes that an improvement is not necessary to establish this claim element.

In sum, the Court finds that AUO has established by a preponderance of the evidence, that the accused LGD products meet the elements of claim 1 of the '160 patent. Accordingly, the Court concludes that LGD infringes claim 1 of the '160 patent.

> **Claim 2: The liquid crystal display according to claim 1, wherein said determinator comprising a table for storing a brightness level determined by the characteristic of a liquid crystal cell according to a relation between the previous brightness level and the next brightness level, and determining the output brightness level by modifying said next brightness level based on the brightness level read from said table.**

The Court concludes that the limitations described in claim 2 are met in the accused devices. The determinator in LGD's timing controller chips comprises a table for storing a brightness level. This table is the lookup table, which stores a brightness level. Tr. 204:11-16, 172:14-173:18 (Silzars); AUO-165 at 26/51. The lookup table stores brightness levels that vary according to the relation between the previous brightness level and the next brightness level. Id. The lookup table values are determined by the characteristics of the liquid crystal cell. They are determined by trial and error using measurements of the response of the liquid crystal cell. A person makes the measurements using a photodiode, which measures light, and an oscilloscope. Tr. 79:24-80:24 (C.G. Kim).

> **Claim 3: The liquid crystal display according to claim 2, wherein: said video signal input through said input logic comprises a plurality of color signals; and**

The Court concludes that this claim element is met in the accused devices. The video signal input includes a plurality of color signals. In particular, the LVDS video signal includes three separate colors: red, green and blue. Tr. 204:17-205:4;

434:24-435:10 (Silzars); AUO-165 at 1/51. The LVDS receiver, which inputs the LVDS signal, converts the LVDS data stream back into 28 bits or RGB, that is red, green and blue data. AUO-165 at 3/51, 4/51.

Claim 3: said table in said determinator is provided for each of said color signals.

The Court concludes that this claim element is also met in the accused devices. The lookup table includes three separate lookup tables, one each for red, blue and green data. Specifically, there are three Arithmetic LUTs, or lookup tables, in the block diagram for the New Monde chip. The Arithmetic LUTs each output 8 bits of red, green and blue, respectively. Tr. 205:5-10 (Silzars); AUO-165 at 3/51, 14/51; Tr. 958:12-23 (Eccles).

In sum, the Court concludes that AUO has established by a preponderance of the evidence, that the accused LGD products meet the elements of claim 3 of the '157 patent. The LGD LCD modules containing the New Monde controller chip include every element of claim 3 of the '160 patent. Further, the LGD modules containing the New Monde timing controller chip, which infringe claim 1 are representative of the accused products containing the timing controller chips identified in AUO-1553, the listing of timing controller chips analyzed for infringement. Tr. 169:6-23, 170:8-18 (Silzars). Each of these products therefore also infringes claim 3. Accordingly, the Court concludes that LGD infringes

claim 3 of the '160 patent.

C. Whether LGD Infringes claims 7 and 16 of AUO's '629 Patent

1. AUO's standing to assert the '629 patent

As a threshold matter, LGD contends that AUO lacks constitutional standing to assert the '629 patent against LGD, because AUO was not the owner of the '629 patent at the time this action was filed. LGD contends that the inventors of the '629 patent assigned their rights in the patent to IBM Japan, but IBM Japan never assigned its rights to International Business Machines Corporation (US) ("IBM USA") before IBM USA assigned its rights to AUO in June 2005. Thus, LGD contends that the June 2005 assignment could not have included the '629 patent. In addition, LGD contends that AUO cannot cure this standing defect through the retroactive application of the Patent Assignment Form filed with the PTO in May 2007 (LGDTX 931), which purported to assign the rights in the '629 patent from the named inventors to IBM USA.

In response, AUO contends that the '629 patent issued naming IBM USA as the assignee on the face of the patent, and IBM USA received title to the '629 patent through a succession of assignment agreements. As a result, AUO contends that the June 2005 Patent Assignment Agreement, in which IBM USA transferred and assigned to AUO "all right, title and interest in and to" certain specified patents, including the '629 patent "along with

any and all damages for infringement of any of the assigned patents before, on and after" June 30, 2005, "and the sole right to sue therefor under the assigned patents," was sufficient to transfer title of the '629 patent from IBM USA to AUO.

In a patent case, as in all federal actions, a plaintiff must have standing to sue before a claim can be brought. Sicom Sys. v. Agilent Techs., Inc., 427 F.3d 971, 975 (Fed. Cir. 2005). The burden to establish standing rests on the party bringing suit. Id.

The assignation on the face of a patent is "not a conclusive indication" of patent ownership.[5] U.S. Philips Corp. v. Iwasaki Elec. Co., 505 F.3d 1371, 1375 (Fed. Cir. 2007). Rather, the plaintiff must demonstrate that it is the owner/patentee, assignee, or grantee of the patent-in-suit. See 35 U.S.C. § 281; Morrow v. Microsoft Corp., 499 F.3d 1332, 1339 (Fed. Cir. 2007); Fairchild Semiconductor Corp. v. Power Integrations, Inc., 2007 U.S. Dist. Lexis 93711, *13-14 (D. Del. 2007).

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[5] There is some authority, however, suggesting that the ownership data provided on the face of a patent creates a presumption of ownership. Arachnid v. Merit Indust., Inc., 939 F.2d 1574, 1578 n.2 (Fed. Cir. 1991); Board of Trustees of the Leland Stanford Junior Univ. v. Roche Molecular Sys., Inc., 487 F. Supp. 2d 1099, 1111 n.4 (N.D. Cal. 2007). Regardless of whether the Court views the naming of IBM USA as the assignee on the face of the patent as a presumption of ownership or not, the Court concludes that assignment to IBM USA has been demonstrated either affirmatively by AUO or by the fact that LGD has not overcome the presumption that legal title to the '629 patent vested in IBM USA as the assignee.

On the record presented, the Court concludes that AUO has demonstrated by credible chain of title evidence that it is the assignee of the '629 patent.[6] LGD contends that the inventors assigned their rights to the invention claimed in the '629 patent to IBM Japan in 2000, and there was no direct conveyance of rights between IBM Japan and IBM USA prior to IBM USA's assignment to AUO. However, LGD's argument ignores the assignment documents predating 2000. Specifically, IBM USA and IBM World Trade ("World Trade") entered into an agreement dated January 1, 1963, in which IBM USA acquired any patents that World Trade had or thereafter acquired. AUO-302 at IBM 300004. Thereafter, IBM Japan and World Trade executed two agreements in which IBM Japan granted to World trade the right to all of IBM's patent applications and patents in countries other than Japan. The first agreement dated June 25, 1981, amended a previous 1960 agreement and provided that IBM Japan grants "to World Trade and/or its designees, in respect to inventions owned or controlled by IBM Japan, the right in countries other than Japan to file or have filed on its behalf or on behalf of such designees, and to own such applications for patents and the patents issuing thereon . . ." AUO-303 at IBM 3000014-300015. The 1981 agreement was extended by the December 1990 letter

[6] LGD's objections to the admission of this evidence are addressed by a separately issued Memorandum Opinion and Order.

agreement which provided that the 1960 agreement, as amended, would not terminate until December 31, 2000. AUO-304.

The inventors transferred their ownership interests to IBM Japan in August 2000, prior to the termination of the 1960 agreement between IBM Japan and IBM World Trade, as amended by the 1981 and 1990 agreements. AUO-258, AUO-P-963. Thus, by operation of these agreements and the earlier 1963 agreement between World Trade and IBM USA, title of the '629 patent flowed from IBM Japan to IBM USA through World Trade's designation of IBM USA as its designee. Accordingly, the Court concludes that IBM USA held title to the '629 patent on the date of its issuance and in 2005 when IBM USA assigned the '629 patent to AUO, and therefore, AUO was the rightful owner of the '629 patent at the time it commenced this action.

2. Infringement of Claim 7 and Claim 16

After comparing LGD's accused products with claims 7 and 16 of AUO's '629 patent, the Court concludes that AUO has established by a preponderance of the evidence that LGD literally infringes the '629 patent.

Claim 1 Preamble: An array substrate for display

The Court finds that this claim element is met in the accused devices. An array substrate, in the context of liquid crystal display modules, is an insulating substrate carrying one or more arrays of components such as thin film transistors. '629

patent, col. 1, ll.8-20; Tr. 142:20-143:3 (Silzars). LGD does not appear to object to this characterization of an array substrate, yet LGD appears to take issue with whether this limitation is met in the accused products. In the Court's view, LGD's argument here is apparently based on semantics rather than on substance. Based on the representation demonstrated in court by Dr. Silzars, the Court finds that the LGD's accused products include a substrate made from a layer of glass and an array of thin film transistors among the components formed on the glass substrate. Tr. 142:11-143:3, 128:11-129:4 (Silzars); AUO-1571.

Claim 1: a layer of an insulating substrate, having an area

The Court concludes that this claim element is met in the accused devices. Glass is a suitable insulating material, and the array substrate of the representative accused product, LC320W01, includes a layer of glass as the insulating material. Tr. 142:11-143:3 (Silzars); Tr. 843:22-845:8, 864:16-21 (Rubloff). In addition, that layer of glass has an area or specified region where the dummy conductive patterns are located, as discussed more fully below. Tr. 143:4-145:5 (Silzars); AUO-1567.

Claim 1: a thin film transistor array formed on the insulating substrate

The Court concludes that this element is met in the accused devices. LC320W01 includes a thin film transistor array. AUO-

1567; AUO-774-1; Tr. 140:16-141:9 (Silzars). The thin film transistor array is formed on an insulating substrate when manufactured. Tr. 140:16-141:9, Tr. 128:11-129:4, 129:13-131:2 (Silzars); AUO-1568-1574. Dr. Rubloff did not dispute Dr. Silzars's testimony that the accused products meet this claim element. LGD-1084 at 629-009.

Claim 1: a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array

The Court concludes that the accused products include a plurality of wiring as the Court has construed that term. The plurality of wiring in LC320W01 is labeled in AUO-1567. As shown in AUO-1567, the plurality of wiring is formed and arranged on the device's insulating substrate in a fan-out pattern between the connection pads and the edge of the thin film transistor array. Tr. 125:1-15, 140:11-15 (Silzars); AUO-P-1479-02, AUO-P-1479-39; AUO-P-1479-45; AUO 1568; AUO-1570; AUO-1571. The plurality of wiring also extends between, on a first end, connection pads, and on a second end, the thin film transistors of the TFT array. Tr. 125:1-126:7 (Silzars). The wiring of the LC320W01 communicates with the thin film transistors of the TFT array. Tr. 125:16-129:4, 139:10-140:15 (Silzars); AUO-1567; AUO-1568; AUO-1570; AUO-1571. Dr. Rubloff did not dispute Dr. Silzars' testimony that this claim element was met in the accused products. LGD-1084 at 629-009.

Claim 1: connection pads, each connection pad contacting the first end of at most one of the plurality of wirings

LGD does not appear to dispute that this claim element is met in the accused devices. The parties agreed that the claim term "connection pads" means "conductive patterns on the substrate that electrically connect the plurality of wiring to circuits located external to the substrate." Tr. 138:5-139:9 (Silzars). The Court concludes that this claim element is found in LC320W01. In LC320W01, the connection pads are identified in AUO-1567 and AUO-1568 and are located along at least one edge of the insulating substrate of the LC320W01. Tr. 123:19-124:22 (Silzars).

Claim 1: pixel electrodes

LGD does not appear to dispute that this claim element is met in the accused devices. Pixels or picture elements are included on a thin film transistor array. Tr. 310:5-311:3 (Rubloff - Phase II). Pixels include pixel electrodes that operate to allow the passage of light. Tr. 310:5-311:3 (Rubloff - Phase II). The Court concludes that pixel electrodes are present in the array substrate of the LC320W01. Specifically, the LC320W01 includes a plurality of transparent electrodes which, in a completed product, store and apply a driving voltage to a pixel in an LCD. AUO-1567; Tr. 141:10-142:10 (Silzars).

Claim 1: dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patterns are not in contact with any of the wiring

The Court concludes that this claim element is present in the accused devices. LGD refers to the accused dummy conductive patterns as "line-on-glass" or LOG patterns. Tr. 831:11-832:23 (Rubloff). These patterns are located near the edge of the insulating substrate, between the connection pads and pixel electrodes. They are not in contact with any of the wiring. Tr. 131:3-23, 144:5-145:5, 146:19-22 (Silzars); AUO-1567, AUO-1569. These patterns cover more than 50% of the area or specified region in which they are situated. Tr. 146:11-18 (Silzars).

LGD's noninfringement argument regarding this claim element is two-fold. First, LGD contends that the accused devices do not have "dummy conductive patterns" that are meant to aid during etching and do not convey signals. More specifically, LGD's argument suggests that after the completed array substrate has been combined with a number of components to form a completed LCD module there is an indirect connection to the wiring and the accused dummy patterns convey signals. LGD's argument, however, is based upon claim construction limitations that the Court has not accepted. In addition, the claim language does not prohibit indirect electrical connection or communication between dummy conductive patterns and the wiring. Rather, the claims only

require that the dummy conductive patterns do not contact the wiring. Furthermore, that the accused dummy patterns may transmit signals after the accused array substrates have been assembled into an LCD module is not relevant to the claims asserted here, because those claims are directed to "an array substrate" alone, not an LCD module including an array substrate. See e.g., Gemtron Corp. v. Saint-Gobain Corp., 572 F.3d 1371, 1377-1379 (Fed. Cir. July 20, 2009) (claim directed to a shelf required the shelf to have the claimed characteristics before it was assembled into a finished product).

LGD's second argument focuses on the term "area." Specifically, LGD contends that any alleged dummy conductive patterns in its accused products do not comprise at least about 30% of the area of the insulating substrate. As with its previous argument, however, LGD's argument concerning the term "area" depends upon a claim construction which the Court has not adopted. Further, the Court credits the testimony of Dr. Silzars that the accused dummy conductive patterns in each of the accused products covers more than 50% of the region in which they are situated. Accordingly, the Court concludes that this claim element is met in the accused devices.

Claim 2: The array substrate according to claim 1 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials

LGD does not appear to dispute that this claimed element is present in the accused devices, and the Court finds this claim element to be present in LC320W01. The wiring of LC320W01 is made from a lower layer of aluminum with neodymium, an aluminum alloy, and an upper layer of molybdenum. Both neodymium and molybdenum are conductive materials. Tr. 858:4-9 (Rubloff); Tr. 138:21-139:9, 291:9-15 (Silzars); Tr. 101:16-102:1 (I.D. Song).[7]

Claim 4: The array substrate according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium, and alloys thereof.

LGD does not appear to dispute that this claim element is present in the accused device, and as discussed above, the Court has found that the upper layer wiring material in the accused devices is molybdenum. Tr. 291:9-15 (Silzars); Tr. 101:16-102:1 (I.D. Song). Accordingly, the Court concludes that this claim element is met in the accused devices.[8]

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[7] Claims 2 and 10 recite the same claim limitation. Because the LC320W01 includes the limitation of claim 2, it includes the limitation of claim 10. Further, claim 11 requires the wiring of the LC320W01 to include a lower layer of aluminum with neodymium, an aluminum alloy. As explained with respect to claim 2, the limitation of claim 11 is met here, as well.

[8] This claim limitation is also asserted in claim 13. Because the LC320W01 includes the limitation of claim 4, the Court concludes is also meets the same limitation as set forth in claim 13.

Claim 7: The array substrate for display according to claim 3 wherein the upper layer wiring material is selected such that the upper layers wiring material does not become insoluble in an acid or alkaline etchant.

The Court concludes that the accused devices satisfy this claim element. In LC320W01, the wiring of the array substrate is formed using an acid etchant. Tr. 98:3-8 (I.D. Song). During the wet etching process, the upper layer wiring material is etched at a faster rate than the lower layer wiring material. Tr. 102:7-13 (I.D. Song); Tr. 148:24-149:17 (Silzars). This confirms that the upper layer material in the wiring of the LC320W01 array substrate remains soluble through the etching process, because if the upper layer of conductive material in the wiring of the accused products were to become insoluble, the etching of the upper layer would have been slowed or stopped altogether.[9] Tr. 148:24-149:17; Tr. 147:24-148:15 (Silzars).

Claim 9 Limitations

Claim 9 corresponds essentially to claim 1. Tr. 826:17-827:4 (Rubloff). Because the Court has concluded that the representative accused product, LC320W01, includes the limitations of claim 1, the Court also concludes that it includes the limitations of claim 9.

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[9] This claim limitation is also asserted in claim 16. Because the LC320W01 includes the limitation of claim 7, the Court concludes it also meets the same limitation as set forth in claim 16.

In sum, the Court finds that AUO has established by a preponderance of the evidence, that the accused LGD products meet the elements of claims 7 and 16 of the '629 patent. Accordingly, the Court concludes that LGD infringes claims 7 and 16 of the '629 patent.

D. Whether LGD Infringes claim 1 of AUO's '157 Patent

After comparing LGD's accused products with claim 1 of the '157 patent, the Court concludes that AUO has established by a preponderance of the evidence that LGD directly infringes the '157 patent. In reaching this conclusion, the Court credits the testimony of Dr. Silzars.

Claim 1 Preamble: A backlight unit for a liquid crystal display, comprising

LGD does not dispute that this claim element is met in the accused products, Tr. 1103:23-1104:14 (Smith-Gillespie), and the Court finds the element to be present in the accused devices as shown in the engineering drawings of the backlight assembly.

Claim 1: a frame

Although LGD's expert witness Mr. Smith-Gillespie initially disputed in his expert report that the accused products had a frame, LGD did not raise this argument at trial. In any event, the Court finds that all of the accused products include a frame. The frame is comprised of a metal portion, denoted as a "cover bottom" in LGD's engineering drawings and a white "tray," denoted as a "supporter side" in LGD's engineering drawings. Tr. 215:13-

216:3 (Silzars).

Claim 1: a first supporting portion, disposed on the frame

Claim 1: a second supporting portion, further disposed on the frame

As defined by the Court, a "supporting portion" is "any structure protruding from the frame, (including but not limited to a cylinder or cuboid) intended to support the optical film." The Court finds that all of the accused products meet this limitation because they have pins that protrude from two edges of the frame. AUO-541-543; Tr. 216:4-217:10 (Silzars). The Court further finds that all of the accused products have a first and second supporting portion, and it is arbitrary whether the pins protruding from the (i) left vertical edge or (ii) the top horizontal edge are referred to as the "first" or "second" supporting portion.

Claim 1: a film comprising a first constraining portion and a second constraining portion

The Court concludes that the accused products meet this claim limitation because they all have optical films with holes on two different edges, the top horizontal edge or the left vertical side, constituting the first and second constraining portions. Tr. 218:13-219:6 (Silzars); 1102:9-1103:4, 1104:15-20 (Smith-Gillespie). Consistent with the Court's discussion of the first and second orientation above, the determination of which holes are the first constraining portion and which holes are the

second constraining portion depends upon which set of protrusions is deemed the first or second supporting portion.

> **Claim 1: a film comprising a first constraining portion and a second constraining portion, position on the frame by the first supporting portion and the second supporting portion passing through the first constraining portion and the second constraining portion, respectively**

The Court concludes that this element is met in all of the accused products. The optical film in the accused products is positioned on the frame by having the protrusions on the edge of the frame pass through the respective holes in the optical film. Tr. 219:19-221:17 (Silzars); AUO 545, 546; Tr. 92:11-94:22 (Moon); Table 1.

> **Claim 1: when the frame is disposed in a first position, the first supporting position partially contacts an inner wall of the first constraining portion for positioning the film, and the second supporting portion does not contact the second constraining portion**

The Court concludes that each of the accused products has the aforementioned element. When the frame is disposed in a first position, for example, the landscape orientation, there are pins protruding from the top horizontal edge of the frame that pass through and support the optical films. In this position, the second set of vertical pins on the side edge do not contact the holes. AUO-563; Tr. 222:18-223:3 (Silzars). This conclusion is consistent with Mr. Moon's testimony explaining that LC420WX5 is designed so that there are gaps on all sides between the pins

and the holes in the optical film through which the pins pass. Tr. 94:4-22 (Moon). As Dr. Silzars explained, the dimensions of the gaps change when the film is disposed in different orientations, essentially, the film "floats" within the frame. Tr. 223:17-224:6 (Silzars); AUO 563-565, Table 1.

LGD contends that the accused products do not meet the "does not contact" requirement of this claim because there is contact when the film expands or contracts due to temperature variations. However, Mr. Smith-Gillespie admitted that at room temperature, when in a first position of landscape orientation, there is a "clearance" between the holes and the pins on the vertical side edge. LGD 1090 at LGD 157-030, LGD 157-031; LGD-837; LGD-840; Tr. 1109:7-16, 1204:20-23 (Smith Gillespie). LGD contends that this evidence is insufficient to establish infringement, because "claim 1 requires that thermal expansion and contraction of the film be accounted for so that the supporting portions do not contact the constraining portions when in a non-supporting position during the entire temperature range of the backlight unit." D.I. 1407 at ¶ 233. In this regard, LGD maintains that it was unnecessary for the patent to expressly include a specific temperature range for the accommodation of film expansion and contraction, because "[i]f the thermal expansion and contraction requirement applied to an amount less than the entire temperature range as suggested by AUO, this requirement would be meaningless

because it could read on standard engineering tolerances (clearance) or fit clearances." Id. However, the Court has concluded that the "does not contact" requirement does not include any thermal expansion or contraction limitation and neither the patent nor the prosecution history specifies any temperatures over which thermal expansion or contraction must be accommodated. Accordingly, the Court declines to accept Mr. Smith-Gillespie's infringement opinion which is predicated upon a claim construction that was not adopted by the Court, and therefore, the Court concludes that the aforementioned claim element is met in the accused devices.

Claim 1: when the frame is disposed in a second position, the second supporting portion partially contacts an inner wall of the second constraining portion for positioning the film, and the first supporting portion does not contact the first constraining portion

The Court likewise concludes that this element is satisfied in all of the accused products. When the frame is disposed in a second position, for example moving from the landscape to portrait orientation, there are pins protruding from the top horizontal edge of the frame that pass through and support the optical films while the second set of vertical pins on the side edge do not contact the holes. AUO-563. The "does not contact" limitation here is satisfied for the same reasons discussed in connection with the previous claim element. To the extent that "incidental contact" occurs, the Court notes that the patent

discloses the possibility of "incidental contact," and as Dr. Silzars explained, such incidental contact is the nature of what is taught in the patent when film is not securely fixed to the frame. Tr. 225:8-10; Tr. 224:24-225:1 (Silzars).

With respect to this and other claim elements, LGD contends that not all of its displays are intended to be displayed in both landscape and portrait orientation, and therefore, they cannot meet claim elements which require orientation in a second position. However, the evidence demonstrates that all LGD public displays can support viewing in both landscape and portrait orientations, AUO-81; Tr. 213:2-24 (Silzars), and the other LGD non-public display products are capable of being used in portrait orientation at least temporarily, even if LGD does not guarantee the quality or lifetime of a non-public display unit used in that orientation. Tr. 90:24-91:11, 92:7-10 (Moon).

In sum, the Court finds that AUO has established by a preponderance of the evidence, that the accused LGD products meet the elements of claim 1 of the '157 patent. Accordingly, the Court concludes that LGD infringes claim 1 of the '157 patent.

E. Whether LGD Infringes Claims 7 and 17 of the '506 Patent

After comparing LGD's accused products with the claim 7 and 17 of the '506 patent, the Court concludes that AUO has established by a preponderance of the evidence that LGD literally infringes the '506 patent. In reaching this conclusion, the

Court finds LB035Q02 to be representative of the accused products. Tr. 228:13-229:3 (Silzars).

Claim 1 Preamble: A signal transmission device connecting a display module and a system

The Court finds that the accused products include a signal transmission device connecting a display and module and a system. "The LB035Q02 is a Color Active Matrix Liquid Crystal Display with a white LED backlight assembly." AUO-61 at 4/35; AUO-64 at 4/31; AUO-66 at 4/33. "This LCD employs one interface connection for the operation of [the] module, LED B/L [backlight] and TSP (touch screen panel)." AUO-61 at 6/35. The signals received over the 60-pin flexible printed circuit board is described in the pin configuration for the connector. AUO-61 at 6/35-7/35.

Claim 1: a first flexible printed circuit board, electrically connecting the display module and the system and a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board

Although AUO advances arguments and terms for claim construction related to this claim element, LGD does not appear to offer a response to those arguments. Further, it appears to the Court that LGD does not genuinely dispute the presence of this element in the accused devices, but instead focuses its argument on evidentiary based objections to the drawings and specifications used by AUO to support its argument.[10] D.I. 1407

[10] The parties have separately briefed any evidentiary objections that were maintained, and the Court has addressed

at ¶¶ 253-255. The Court finds that this element is met in the accused products. AUO-1575; Tr. 229:4-232:8 (Silzars); Tr. 86:6-17 (J.D. Kim); AUO-61 at 31/35; AUO-62; AUO-331 through AUO-340; AUO-63; AUO-64 at 27/31; AUO-65; AUO-66 at 30/33; AUO-67; AUO-340; AUO-341; AUO-P-1491; AUO-P-1492; AUO-425; AUO-426.

Claim 1: wherein the first and second flexible printed circuit boards are joined by hot bar soldering

In light of the Court's construction of the phrase, "hot bar soldering," the Court concludes that each of the accused products meets this claim limitation. The first and second flexible printed circuit boards of LB035Q02, which is representative of the accused products, are joined by soldering material. Tr. 233:22-234:5 (Silzars); Tr. 1316:20-1317:23 (J.D. Kim); Tr. 1120:6-1130:6, 1132:8-1133:8 (Smith-Gillespie); AUO at 16/23, 18/23.

Claim 7: The signal transmission device as claimed in claim 1 wherein the second flexible printed circuit board transmits a light source signal

LGD does not appear to dispute that the accused products meet this claim limitation and again focuses its argument on certain evidentiary issues. D.I. 1407 at ¶ 276. The Court finds that this element is met in the accused devices. By way of example, the Court points out that LB035Q02 has a white LED

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those objections that were briefed by the parties in their evidentiary briefs by separate Memorandum Opinion and Order.

(light emitting diode) backlight assembly connected to the main or first flexible printed circuit board through an LED flexible printed circuit board. Tr. 85:6-11, 87:16-89:2 (J.D. Kim); AUO-63.

Claim 17: A signal transmission device, connecting an [sic] display module and a system, comprising: a first flexible printed circuit board, electrically connecting the display module and the system; and a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board

With regard to the above claim element, the Court notes that claim 17 is identical to portions of claim 1. For the reasons discussed in the context of claim 1, the Court finds that the accused products meet these claim elements.

Claim 17: wherein the first flexible printed circuit board has a first alignment mark, and the second flexible printed circuit board has a second alignment mark overlapped and aligned to the first alignment mark

The Court concludes that the accused products meet this claim element. The accused products include both holes as alignment marks, Tr. 232:9-233:18 (Silzars); Tr. 83:5-85:5, 86:18-87:5, 1319:5-1320:6 (J.D. Kim); AUO-67 ("4"), and extended pad electrodes. Tr. 232:23-233:18, 240:15-241:12 (Silzars). Prior to the soldering process, an operator assembling the accused product visually observes and aligns the pad electrodes of the first and second flexible printed circuit boards. Tr. 81:20-82:22 (J.D. Kim); Tr. 233:5-13 (Silzars).

In sum, the Court finds that AUO has established by a preponderance of the evidence, that the accused LGD products meet the elements of claims 7 and 17 of the '506 patent. Accordingly, the Court concludes that LGD infringes claims 7 and 17 of the '506 patent.

III. Invalidity

A. Whether Claims 1 and 3 of the '160 Patent Are Invalid

1. Indefiniteness

LGD contends that claims 1 and 3 of the '160 patent are invalid because the terms "time integration quantity" and "substantially equal" are indefinite. The Court has concluded, in the context of its claim construction rulings, that these terms are not indefinite. Accordingly, the Court concludes that LGD cannot establish invalidity of the '160 patent on the basis of indefiniteness.

2. Anticipation and/or obviousness in light of the Mori, Kido and Johnson references

LGD contends that claims 1 and 3 of the '160 patent are invalid and/or obvious in light of the Mori JP '532 publication reference, which is disclosed in the background section of the '160 patent, and the Kido and Johnson references. According to LGD, Mori discloses a liquid crystal display with a conventional overdrive circuit and each of the claimed elements of the '160 patent. While the Mori reference does not explicitly teach that the overdrive circuit is applied to each of red, green and blue

signals, LGD contends that it would have been obvious to apply the overdrive circuit to each red, green and blue signals, as evidenced by the Kido and Okumura references. With respect to the Kido and Johnson references, LGD also makes arguments independent of the Mori reference, that Kido and Johnson render the '160 patent invalid as anticipated and/or obvious.

In response, AUO contends that Mori, Johnson and Kido do not mention improving the quantity of light, and that even if one uses a conventional prior art overdrive system such as Mori, Kido or Johnson that seeks to improve response time, the pixel may emit, but will not necessarily emit, a quantity of light that approaches the ideal. Thus, AUO maintains that Mori, Johnson and Kido do not inherently disclose an output brightness level so as to make a time integration quantity of a brightness change substantially equal to the ideal. In addition, AUO contends that Kido does not disclose "a determinator for determining an output brightness level," a "determinator for comprising a table for storing brightness level," and a "table in said determinator [] provided for each of said color signals." AUO further contends that Johnson does not disclose "a determinator for determining an output brightness level," and a "determinator for comprising a table for storing brightness level."

After reviewing the prior art references in light of the testimony and evidence adduced at trial, the Court concludes that

LGD has not established by clear and convincing evidence that the Mori, Kido and Johnson references invalidate the '160 patent. The Court is persuaded that none of the cited references disclose the time integration quantity of a brightness change that is substantially equal to an ideal quantity of light. These references do not mention improving the quantity of light, Tr. 1003:6-24 (Eccles), and both experts who testified at trial agreed that using these prior art systems to improve response time does not necessarily result in the pixel emitting a quantity of light that is substantially equal to the idea. Tr. 1380:9-23, 1377:9-23, 1381:8-1382:20 (Silzars); Tr. 1002:2-11; 1025:17-1026:3 (Eccles); LGD-245 (Mori); LGD-297 (Kido); LGD-318 (Johnson).

In addition, the Court concludes that Kido and Johnson do not disclose the required determinator and table elements. LGD's expert Mr. Eccles testified that the ROM discussed in Kido is the required "table for storing a brightness levels." As Dr. Silzars explained, however, the ROM stores coefficient values K1 and K2, which are used to create the compensating waveform. These are not brightness levels, but abstract mathematical concepts. Tr. 1384:10-1385:8 (Silzars); LGD-297 (Kido) at col. 7, ll. 61-68, col. 9, ll. 27-33; Tr. 1029:23-1032:2 (Eccles). As for the Johnson reference, LGD's expert, Mr. Eccles, identified the required determinator and table as Table 1 disclosed in Johnson.

LGD-318 (Johnson) at col. 4, l. 6 - col. 5, l. 14. However, Johnson expressly indicates that the disclosed table pertains to voltages. LGD-318 (Johnson) at col. 4, ll. 47-64; Tr. 991:11-992:2 (Eccles). A voltage is not the same as a brightness level. Tr. 1028:19-1029:2 (Eccles). Accordingly, the Court concludes that the '160 patent is not invalid as anticipated or obvious in light of Mori, Kido and Johnson, alone or in combination with each other.

B. Whether Claim 1 of the '157 Patent Is Invalid

1. Anticipation by the Shimuzu reference

LGD contends that claim 1 of the '157 patent is invalid because it is anticipated by U.S. Patent No. 7,380,972 issued to Shimizu (the "Shimizu reference"). LGD contends that the Shimuzu reference qualifies as prior art under Section 102(e) because it was filed on August 19, 2003, as PCT Application No. PCT/jp03/10458. LGD further contends that the Shimuzu reference discloses each and every limitation of claim 1 of the '157 patent.

In response, AUO contends that the Shimizu reference is not prior art to the '157 patent, because the earliest date for which the Shimizu patent could be relied upon as prior art is March 11, 2004, the publication date of PCT Pub. No. WO2004/020899. Because the '157 patent was invented by February 6, 2004 as evidenced by the invention disclosure form for the '157 patent,

AUO contends that it cannot be invalidated by the Shimizu reference.

Section 102 provides, in pertinent part, that a "person shall be entitled to a patent," unless

> (e) the invention was described in . . . (2) a patent granted on an application for patent by another filing in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

35 U.S.C. § 102(e)(emphasis added). Article 21 provides that "[t]he language . . . of the international publication is governed by the Regulations," which in turn require that "[i]f the international application is published in a language other than English, . . . the title of the invention, the abstract and any text matter pertaining to the figure or figures accompanying the abstract shall be published both in that language and in English. D.I. 1403 at Exh. G (Article 21); Exh. H (PCT Regulation 48.3(c)). Thus, the abstract and text relating to the figures in the abstract are required to be in English regardless of what language the application was published in.

In this case, only the abstract and characters accompanying the figures are in English as required by Article 21, but the remaining application, consisting of more than 45 pages, is in Japanese. The biographical data for the international

application confirms that the application was not published in English because it states that the "Publication Language" is "Japanese." D.I. 1403, Exh. I. Accordingly, the Court concludes that the earliest publication date for the Shimizu reference is the English document, PCT Pub. No. WO2004/020899, which is dated March 11, 2004. Because the '157 patent was invented before this date, the Court concludes that the Shimizu reference is not prior art, and therefore, LGD cannot establish that the '157 patent was invalid as anticipated by the Shimizu reference.

2. Obviousness with regard to the Fukayama and Sakamoto patents

LGD contends that either Fukayama alone, or in combination with Sakamoto renders claim 1 of the '157 patent obvious. The parties' dispute regarding these references primarily centers on whether the Fukayama reference, alone or in combination with Sakamoto, discloses the "does not contact" limitation in the various claim elements of the '157 patent.

LGD's expert, Mr. Smith Gillespie, contends that the "does not contact" limitation is met, because Figure 13 of Fukayama discloses that the second supporting portion "does not contact" the second constraining portion. Specifically, Mr. Smith Gillespie relies on the sentence in the Fukayama patent which explains: "Although this embodiment is similar to the first embodiment, as described in conjunction with Fig. 1, with respect to the holding of other sides of the optical sheet OPS and the

other constitutions, the columnar member may be replaced with an insertion member having a pin shape with a head which is similar to the above-mentioned insertion member BT having the pin shape with the head which is loosely engaged with a through hole formed in the optical sheets." LGD-332 at col. 18, ll. 34-43; Tr. 1121:3-13 (Smith-Gillespie).

However, the Court credits the testimony of Dr. Silzars over the testimony of Mr. Smith Gillespie with respect to this issue. As Dr. Silzars's explained, "loosely engages" and "does not contact" are not synonymous terms. Further, the Fukayama patent is directed to the secure holding of optical films. As Figure 1 shows, the optical film is "firmly fixed" by the use of adhesive tape. LGD-332 at Fig. 1, col. 15, ll. 5-7; Tr. 1412:6-16 (Silzars). While the "other sides" referred to in the sentence relied upon by Mr. Smith-Gillespie may be "loosely engaged," there is nothing in that sentence suggesting that the "firmly fixed" side may be loosely engaged.

To the extent rotation of a display device is an issue, the Court concludes that Fukayama does not disclose rotation, Tr. 1224:21-1225:6 (Smith-Gillespie), and there is no reason to combine Fukayama with Sakamoto, which does disclose rotation. Tr. 1412:6-8 (Silzars). Moreover, the '157 patent acknowledges that rotatable LCDs were known in the prior art, and this prior art including, Fukayama, was before the Examiner when he

concluded that the claims were not obvious in light of Fukayama. AUO-09 ('157 patent) at col. 1, ll. 11-12; Tr. 1222:11-1224:9 (Smith-Gillespie); Tr. 1417:1-13 (Silzars). Accordingly, the Court concludes that LGD has not established by clear and convincing evidence that the '157 patent is invalid as obvious in light of Fukayama, alone or in combination with Sakamoto.

C. Whether Claims 7 and 17 of the '506 Patent Are Invalid

LGD contends that the '506 patent is invalid as anticipated or obvious by Hewlett Packard prior art identified as HP iPAQ h2210 and h2215. LGD contends that these devices raise an on-sale bar to the '506 patent, because they have the same design as tens of thousands of products with the same product numbers sold in the United States prior to August 19, 2003. With respect to the HP iPAQ h2215 specifically, LGD presents a sales receipt which evidences that the device was sold in the United States by at least November 22, 2003. LGD contends that the '506 patent was not invented until December 16, 2003, and therefore, the HP devices constitute prior art.

In response, AUO contends that the invention date for the '506 patent was not December 16, 2003, but January 15, 2003, and the invention was diligently reduced to practice thereafter. Although AUO acknowledges that the operative date for an on-sale bar is August 19, 2003, one year prior to the filing of its United States application on August 19, 2004, AUO contends that

there is no evidence that the identified HP products were sold or offered for sale prior to August 19, 2003.

After considering the evidence presented on this issue, the Court cannot conclude that LGD has established by clear and convincing evidence that the identified HP devices are prior art that was on sale before August 19, 2003. The only concrete evidence LGD has presented concerning the sale of these specific devices is the sales receipt dated November 22, 2003. This evidence post-dates the on-sale bar.

Further, the Court is persuaded that the '506 patent is entitled to an invention date of January 15, 2003, and that the invention was diligently reduced to practice thereafter. Tr. 1469:7-1474:24, 1475:1-1479:18, 1484:4-18 (Sung); AUO-1544 to AUO-1546; AUO-1611 to AUO-1614; AUO-235; AUO-222. Therefore, the Court cannot conclude that the HP devices are prior art that anticipated or rendered obvious the invention claimed in the '506 patent.

D. Whether Claims 7 and 16 of the '629 Patent Are Invalid

LGD contends that claims 7 and 16 of the '629 patent are invalid as anticipated in light of European Patent Publication No. 887695 (the "Hirabayashi reference") and invalid as obvious in light of U.S. Patent No. 5,850,275 ("Watanabe"). LGD also raises an argument concerning the on-sale bar based upon U.S. sales of LGD Display's LT060VI and LT071VI.

1. Anticipation/Obviousness in light of Hirabayashi and Watanabe

After considering the evidence presented on this issue, the Court cannot conclude that LGD has established by clear and convincing evidence that claims 7 and 16 are invalid in light of Hirabayashi or Watanabe. To the extent LGD's argument is premised on the allegation that Hirabayashi discloses the claimed "area," the Court cannot accept LGD's argument because it is based upon a claim construction that the Court has not adopted. Further, the claims upon which claims 7 and 16 depend require the upper layer wiring material to be selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof. However, Hirabayashi discloses an upper layer of TiN, which is a ceramic compound, not a conductive material or a titanium alloy.

In addition, the Court is persuaded that the claimed invention when viewed in the context of the specification must be considered from the perspective of a two-layer structure in which the upper layer material of the dual-layer wire material does not become insoluble in an acid or alkaline etchant. Neither the Watanabe nor the Hirabayashi references expressly disclose the problem or, or solution to, an upper layer of wiring material of a dual-layer wire becoming insoluble in an acid or alkaline etchant. Indeed, Watanabe discloses only single layer wiring, Tr. 885:20-886:2 (Rubloff); Tr. 1403:7-10, 1405:20-1406:23

(Silzars), and LGD's expert agreed that the dummy patterns disclosed in the Watanabe and Hirabayashi references do not necessarily prevent the upper layer material from becoming insoluble in an acid or alkaline etchant. Tr. 880:1-881:1, 885:5-887:5 (Rubloff); Tr. 1402:3-17 (Silzars). Because the Hirabayashi and Watanabe references do not expressly or inherently disclose use of etchants that will solve the passivity problem addressed by claims 7 and 16 of the '629 patent, the Court concludes that neither Watanabe nor Hirabayashi render the claims of the '629 patent invalid.

2. On-Sale Bar

LGD contends that the '629 patent is subject to the on-sale bar in light of two LGD products, LT060V1 and LT071V1. The Court has considered the evidence presented by LGD in connection with its on-sale bar argument, and concludes that LGD cannot establish by clear and convincing evidence that the on-sale bar applies to the '629 patent. First, the Court is not persuaded that LGD has presented clear and convincing evidence that these two products were, in fact, on sale more than one year before the application resulting in the '629 patent was filed. In addition, LGD's correlation chart shows mask files associated with the identified LGD products, which differ from the mask file used by Dr. Rubloff in his analysis of these products. The mask files associated with these products confirm that the GDS data for these two

products was modified after the priority date of the '629 patent, which would not make these patents prior art to the '629 patent. However, regardless of which mask filed is used, the Court credits the testimony of Dr. Silzars, that none of the mask files associated with the identified LGD products include dummy conductive patterns that comprise at least 30% of the area in which they are situated. Tr. 1397:8-16, 1398:10-1400:13 (Silzars); AUO-1594. Accordingly, the Court concludes that LGD has not established by clear and convincing evidence invalidity based upon the on-sale bar.

IV. Inducement of Infringement

A. Applicable Law

To establish liability for inducing infringement, a patent holder must prove that "there has been direct infringement, and second, that the alleged infringer knowingly induced infringement and possessed specific intent to encourage another's infringement." MEMC Elec. Materials, Inc. v. Mitsubishi Materials Silicon Corp., 420 F.3d 1369, 1378 (Fed. Cir. 2005) (quotations omitted). That the defendant merely had knowledge of the acts alleged to constitute infringement is not enough. Rather, the "plaintiff must establish that the defendant possessed specific intent to encourage another's infringement." Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc., 589 F. Supp. 2d 505, 511 (D. Del. 2008). In this regard, the

plaintiff has the burden of showing that the alleged infringer's actions induced infringing acts and that he knew or should have known his actions would induce actual infringement. These requirements may be shown by direct or circumstantial evidence. See Metabolite Labs., Inc. v. Lab. Corp. of Am. Holdings, 370 F.3d 1354, 1365 (Fed. Cir. 2004).

B. Whether AUO Has Established Inducement Of Infringement

Having concluded that LGD's products directly infringe the asserted patents, the Court further concludes that LGD's customers, distributors and sales representatives have directly infringed the asserted patents. The record contains an abundance of evidence in this regard, but by way of example, the Court points out Mr. Putnam's unrebutted testimony that LGD sold millions of dollars of accused products in the United States. Tr. 764:17-765:2 (Putnam); AUO-284.

In addition, the Court concludes that LGD possessed the requisite intent to induce infringement. In this regard, the Court finds that LGD actively targets the U.S. market and encourages its sales representatives and distributors to build their U.S. market[11] and maintains multiple U.S. locations[12],

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[11] See e.g., AUO-246, AUO-247; Tr. 628:8-14, 18-22, 629:3-19 (Joo Sup Kim); Tr. 490:16-24, 493:16-494:9 (Catalyst/T. Griffin); Tr. 536:22-537:7 (Avnet/S. Gereb); Tr. 548:5-21 (Dell/S. Peana); AUO-125 at Centric 000165.

[12] See e.g. AUO-819 at AUO-LGD 0013940-41; AUO-27 at Catalyst 001044; AUO-119 at AVNET007544.

employees dedicated to key customers in the U.S. and a vast U.S. sales network[13], a technical support, warranty and repair service for its U.S. customers[14], and regular contact and communication with its U.S. customers.[15] LGD also provided product information and marketing materials to its U.S. customers for the purpose of encouraging U.S. sales. AUO-249, AUO-306; AUO-596; AUO-31; AUO-27; AUO-126; Tr. 499:17-503:8 (Catalyst/T. Griffin). In addition, the Court finds that the evidence demonstrates that LGD touted AUO's patented features to LGD's U.S. customers, and that based on the foregoing findings, LGD knew its customers were selling the infringing devices in the U.S. Tr. 559:8-12 (Centric Sales/Edwards); AUO-126; Tr. 545:20-547:19 (Dell/S. Peana); AUO-27 at Catalyst 001064-65; AUO-89 at LGD 190503-05. Accordingly, the Court concludes that AUO has established that LGD induces infringement of the asserted patents.

CONCLUSION

For the reasons discussed, the Court has defined the disputed terms in the asserted patents as set forth in this

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[13] See e.g. Tr. 493:1-15 (Griffing/Catalyst); Tr. 610:3-5, 601:22-603:1 (H. Lee); AUO-228 at LGD 2080258; AUO-27 at Catalyst 001043, AUO-819, AUO-974, AUO-123, AUO-20.

[14] See e.g. AUO-33; AUO-255; Tr. 541:20-542:6; AUO-27; AUO-70, AUO-71; Tr. 589:16-590:16, 591:22-592:8 (Jacobson/Jabil).

[15] See e.g. AUO-309; AUO-321; AUO-982; AUO-1524; AUO-249; AUO-24; Tr. 532:23-533:22 (Avnet/S. Gereb); Tr. 588:10-21 (D. Woo/Westinghouse); Tr. 539:24-540:2; AUO-315.

Memorandum Opinion. In addition, the Court concludes that AUO has established by a preponderance of the evidence that LGD literally infringes the patents asserted by AUO in this action, and that LGD has not established by clear and convincing evidence that the asserted patents are invalid.

The Court will withhold entry of a Final Judgment Order until the Phase II trial is completed.

Electronic Acknowledgement Receipt

EFS ID:	10026476
Application Number:	90009697
International Application Number:	
Confirmation Number:	5947
Title of Invention:	ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE
First Named Inventor/Applicant Name:	6689629
Customer Number:	65358
Filer:	Anthony King/Justin King
Filer Authorized By:	Anthony King
Attorney Docket Number:	67507-008Re-exam
Receipt Date:	05-MAY-2011
Filing Date:	16-MAR-2010
Time Stamp:	11:27:49
Application Type:	Reexam (Third Party)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Reexam Certificate of Service	certificate_of_service_OAR.pdf	3858 5458f921426945cb979fdb67e8bb9e0db77cff8c	no	1

Warnings:
Information:

2		SupplementalOAR.pdf	8586102 1cfab70bda03c1b07b237a7c58da871e157156ee	yes	125

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Supplemental Response or Supplemental Amendment	1	1
Claims	2	5
Applicant summary of interview with examiner	6	7
Applicant Arguments/Remarks Made in an Amendment	8	125

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Information:

Total Files Size (in bytes):	8589960

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENET AND TRADEMARK OFFICE

Application No.:		90/009,697
Filing Date	:	03-16-2010
Applicant	:	Takatoshi Tsujimura
Assignee	:	AU Optronics Corp.
Art Unit	:	3992
Examiner	:	Nguyen, Tuan H.

CERTIFICATE OF SERVICE

I hereby certify that the foregoing **SUPPLEMENTAL RESPONSE TO OFFICE ACTION IN EX PARTE REEXAMINATION** was served upon the following:

Song K. Jung
McKenna Long & Aldridge LLP
1900 K St., N.W.
Washington, DC 20006

by depositing a true and correct copy of the same with the U.S. Postal Service (via First Class mail service) with full postage prepaid.

May 5, 2011
Date

/Justin King/
Justin King, Reg. No. 50,464

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

Appl No.:	**90/009,697**
Patentee:	**6,689,629**
Filing Date:	**3/16/2010**
Art Unit:	**3992**
Examiner:	**Tuan H. Nguyen**
Attorney Docket No.:	**67507-008Re-exam**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL RESPONSE TO OFFICE ACTION

Sir:

This paper responds to the Office Action dated January 6, 2011, and to supplement the Office Action Response submitted on 3/7/2011 and 5/5/2011. This additional supplemental response is to correct the claim amendment format from the previously filed response on 5/5/2011. Please amend the above–identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Interview Summary begins on page 7 of this paper.

Remarks/Arguments begin on page 9 of this paper.

Copies of the cited prior art reference and related judicial decision are attached as Exhibits.

If any necessary fee is not submitted via EFS, the Office is authorized to charge the necessary fee to Deposit Account No. 50-5064.

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

What is claimed is:

1. (Amended) An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of [wiring] wirings arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array, and at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy [patters] patterns are not in contact with any of the [wiring] wirings.

2. (Cancelled)

3. (Amended) The array substrate for display according to claim [2] 1 wherein the lower

layer wiring material is selected from the group consisting of aluminum and aluminum alloys.

4. (Cancelled)

5. (Original) The array substrate for display according to claim 3 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

6. (Original) The array substrate for display according to claim 5 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

7. (Amended) The array substrate for display according to claim [4] 1 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

8. (Original) The array substrate for display according to claim 5 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

9. (Amended) A [meted] method for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array and a plurality of wirings [formed] on the insulating substrate, each wiring having a first end, the wiring in communication with at least [on] one of the transistors in the thin film array, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials, and the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the [wiring] wirings.

10. (Cancelled)

11. (Amended) The method for forming an array substrate for display according to claim [10] 9 wherein the lower layer wiring materials is selected from the group consisting of aluminum and aluminum alloys.

12. (Cancelled)

13. (Cancelled)

14. (Amended) The method for forming an array substrate for display according to claim [13] 9 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

15. (Amended) The method for forming an array substrate for display according to claim [12] 9 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

16. (Amended) The method for forming an array substrate for display according to

claim [13] 9 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

17 (New) An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wirings arranged on the insulating substrate, each wiring having a first end, the wiring directly connects with at least one of the transistors in the thin film array;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patterns are not in contact with any of the wirings.

INTERVIEW SUMMARY

Patentee hereby thanks the Examiners for the personal interview conducted on March 24, 2011. Patentee hereby files this written statement for the issues discussed during the interview on March 24, 2011.

Those present at the telephone interview were Examiner Tuan Nguyen, Examiner Minh Nguyen, Examiner Lao Sue, and Patentee representative Justin King.

Patentee detailed the structure and nature of functionality of the claimed invention to include a novel combination of various recited limitations; in particular the limitation of connection pad in a padding structure and each connection pad contacts the first end of the at most one of the plurality of wirings.

No claim amendment was proposed for this interview. During the interview, Patentee explained the invention in regard to both the padding structure and the wiring connection to the padding structure. Patentee further discussed with the Office in regard limitation mapping in regard that each connection pad contacts the first end of the at most one of the plurality of wirings as stated the adapted rejection. Patentee explained that since the recited Hirabayashi explicitly discloses that the wires are divided into different paths and are intertwined together, Hirabayashi does not disclose the recited limitation that each connection pad is connected to the first end of the at most one wire.

The Office remained firm that the cited reference can still read on the recited limitation, disregarding that Hirabayashi explicitly discloses that the wires are divided into different paths and are intertwined together. The Office stated that Hirabayahsi's figure 6 discloses line L splitting into multiple lines L_{IN}; Office stated that the segment of line L between connection pad 26 and the splitting point reads on the recited limitation of "each connection pad is connected to the first end of the at most one wire".

The Office reported that the response as filed, or an updated response with additional amendment(s), would be treated accordingly. Patentee hereby, in view of the interview discussion, submits the following supplemental response with additional updated and new argument before timely action by the Office.

REMARKS/ARGUMENTS

Claim Status Summary

Claims 1-5, 7-13, and 15-16 are is rejected under 35 U.S.C. §102(b), as being anticipated by Hirabayashi.

Claims 2-8 and 10-16 are is rejected under 35 U.S.C. §103(a), as being unpatentable over Hirabayashi in view of the APA.

Claims 1-5, 7-13, and 15-16 are rejected under 35 U.S.C. §102(b), as being anticipated by Zhang.

Claim 1 is amended to incorporate the limitations which were previously recited in the claims 2 and 4.

Claims 2 and 4 are cancelled in this paper.

Claim 9 is amended to incorporate the limitations which were previously recited in the claim 10 and 12-13. The claim 9 is also amended to correct formality errors from the original prosecution.

Claims 10 and 12-13 are cancelled in this paper.

New Claim 17 is added in this paper; no new matter is inserted by adding this claim.

35 U.S.C. §102(b) and §103(a) Rejection over Hirabayashi

Claims 1-5, 7-13, and 15-16 are is rejected under 35 U.S.C. §102(b), as being anticipated by Hirabayashi, and claims 2-8 and 10-16 are is rejected under 35 U.S.C. §103(a), as being unpatentable over Hirabayashi in view of the APA. Patentee respectfully disagrees for the reasons discussed below.

The 35 U.S.C. §102(b) states the following:

> "A person shall be entitled to a patent unless
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States"

As indicated in MPEP 2131, to anticipate a claim, the cited reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631 (MPEP § 2131). As can be gleaned from the cited case law, the requirement is that each element must be either expressly or inherently described.

The 35 U.S.C. §103(a) states the following:

> "(a) A patent may not be obtained though the invention is not identically disclosed or described as set for the in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made."

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Patentee respectfully submits that Hirabayashi does not disclose or teach every recited limitation in amended claim 1, which incorporates the limitations previously recited in claims 2 and 4. The amended claim 1 recites the following limitations:

"An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wirings arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array, wherein at least one of the wirings comprises at least an upper layer and a lower layer of *conductive materials*, and *the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys* thereof;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patterns are not in contact with any of the wirings."

Hirabayashi Does Not Disclose the Recited Upper Layer Wiring Material in Claim 1

Patentee respectfully submits that Hirabayashi does not disclose or teach the recited plurality of wiring comprising an upper layer and a lower layer, and the upper layer is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof. The limitation was previously recited in the claims 2 and 4. In particular, Patentee respectfully submits that the cited Hirabayashi does not disclose

the recited *conductive material selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.*

The Office stated that Hirabayashi's column 16, lines 19-22 discloses that the wiring can comprise at least an upper layer and a lower layer of conductive materials wherein the lower layer is aluminum and the upper layer is titanium nitride (Office Action, page 4, last paragraph); the Office alleged that Hirabayashi discloses the recited multi-layer wires with conductive materials by mapping Hirabayashi's upper titanium nitride layer as the recited upper layer and Hirabayashi's aluminum layer as the recited lower layer. Patentee respectfully disagrees that such structure reads on the recited limitation in claim 1.

Hirabayashi discloses an electro-optical device substrate. Hirabayashi discloses that a first metal layer forms the source electrode wiring 7a and relay wiring 10 with a quadruple-layer structure of Ti/TiN/Al/TiN in that order from the bottom (Hirabayashi, column 16, lines 19-22, figure 3). Hirabayashi essentially discloses a wire structure with a *lower titanium layer* covered by a layer of titanium nitride, and an *upper aluminum layer* covered by another layer of titanium nitride.

Patentee respectfully submits that although the cited reference Hirabayashi discloses multiple layers, Hirabayashi does not disclose a multi-layer wire having an upper layer selected from the group of *conductive material* consisting of molybdenum, chromium, tantalum, titanium, and alloys. Patentee respectfully submits that, not only the titanium nitride is not one of the listed conductive materials, the titanium nitride is not a conductive material at all. Patentee respectfully submits that the titanium nitride is not an alloy mixture, it is a non-conductive ceramic compound.

As defined in the chemistry field, and also explicitly taught in the college textbook "The Science and Design of Engineering Material" by Schaffer, the ceramic compounds are known as poor conductors of electricity due to the nature of ionic and/or

covalent bonding; such that they are frequently used as insulators[1]. Further support can be found in the U.S. Patent No. 5,158,657 issued to Kadokura, which Kadokura discloses a circuit substrate using the titanium nitride as an insulating film on the top of the conductive wire (Kadokura, abstract and column 3, last paragraph). Thus, Patentee respectfully submits that since the titanium nitride is known to be used as a insulator, then it cannot be considered as a conductive material; and since titanium nitride is not a conductive material, Hirabayashi's multi-layer wire cannot read on the recited limitation which explicitly recites that "an upper layer and a lower layer of *conductive* materials."

In addition, in a related judicial proceeding between the opposing party and the patentee, LG Display Co. LTD vs. AU Optronics Corporation, the court has explicitly held that Hirabayashi does not anticipate the instant patent, and stated that "…the instant patent's claim requires the upper layer wiring material to be selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof. However Hirabayashi discloses an upper layer of TiN, which is a ceramic compound, not a conductive material or a titanium alloy" (District Court opinion, page 70, 1st paragraph, lines 9-13).

Hirabayashi's titanium nitride layer is not one of the materials listed in the claim limitation. In particular, Hirabayashi's titanium nitride layer is neither the recited titanium nor an alloy thereof. Patentee further submits that Hirabayashi's titanium nitride cannot even be considered as equivalent to any of the recited materials since it is not a conductive material. Therefore, for the reason discussed above, Patentee respectfully submits that the cited reference Hirabayashi does not disclose every recited limitation in the amended claim 1 as required under 35 USC 102(b) or 35 USC 103(a); hence, Patentee respectfully requests the Office to withdraw the rejection over claim 1 accordingly, and to issue favorable re-consideration.

---

1 Schaffer et al., "The Science and Design of Engineering Material", International Student Edition.

Claims 2-6

Claims 2 and 4 are now cancelled and the limitations previously recited in claims 2 and 4 are now inserted in the claim 1. The claims 3 and 5 depend on claim 1; thus they incorporate every recited limitation in claim 1. For the reasons stated above, the claims 3 and 5 are not anticipated by Hirabayashi, and Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 3 and 5, and to issue favorable re-consideration.

Claims 7 and 8

The claims 7 and 8 depend on claim 1; thus they incorporate every recited limitation in claim 1. For at least the reasons stated above, the claims 7 and 8 are not anticipated by Hirabayashi.

Furthermore, the dependent claims 7 and 8 each require that "the upper layer wiring material is selected such that the upper layer wiring material does not become insolvent in an acid or alkaline etchant." The Specification explicitly stated that the dummy patterns are located between the pixel electrodes, i.e., the array, and the contact pads, to increase the density of the metal in areas between the pixel electrodes and the contact pads, so as to avoid passivation of the upper conductive layer, and thus avoid undercut, during etching (Specification, Column 5, lines 11-38, column 5, line 55 to column 6 line 17). Patentee respectfully submits that the alleged dummy patterns in Hirabayashi are for a completely different purpose: to ensure uniform polishing of the substrate. Nothing in Hirabayashi discloses or suggests that dummy patterns are located in an area such that an upper layer wiring material does not become insolvent in an acid or alkaline etchant. There is no mention of the problem of an upper layer of wiring material becoming insoluble in an acid or alkaline etchant, much less a solution to that problem, in Hirabayashi.

For the reasons stated above, Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 7 and 8, and to issue favorable re-consideration.

Hirabayashi Does Not Disclose the Recited Upper Layer Wiring Material in Claim 9

Patentee respectfully submits that Hirabayashi does not disclose every recited limitation in amended claim 9, which incorporates the limitations previously recited in claims 10 and 12-13. The amended claim 1 recites the following limitations:

> "A method for forming an array substrate for display, comprising:
>
> forming a layer of an insulating substrate, having an area;
>
> forming a thin film transistor array and a plurality of wirings on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials, and the *upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof*;
>
> forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;
>
> forming pixel electrodes, and
>
> forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wirings."

Patentee respectfully submits that Hirabayashi does not disclose or teach the recited plurality of wiring comprising an upper layer and a lower layer, and the upper layer is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof. The limitation was previously recited in the claims 10 and

12-13. In particular, Patentee respectfully submits that the cited Hirabayashi does not disclose the recited *conductive material selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.*

The Office stated that Hirabayashi's column 16, lines 19-22 discloses that the wiring can comprise at least an upper layer and a lower layer of conductive materials wherein the lower layer is aluminum and the upper layer is titanium nitride (Office Action, page 4, last paragraph); the Office alleged that Hirabayashi discloses the recited multi-layer wires with conductive materials by mapping Hirabayashi's upper titanium nitride layer as the recited upper layer and Hirabayashi's aluminum layer as the recited lower layer. Patentee respectfully disagrees that such structure reads on the recited limitation in claim 9.

Hirabayashi discloses an electro-optical device substrate. Hirabayashi's column 16, lines 19-22 discloses that a first metal layer forms the source electrode wiring 7a and relay wiring 10 (also see Hirabayashi figure 3) with a quadruple-layer structure of Ti/TiN/Al/TiN in that order from the bottom. Hirabayashi essentially discloses a wire structure with a *lower titanium layer* covered by a layer of titanium nitride, and an *upper aluminum layer* covered by another layer of titanium nitride.

Patentee respectfully submits that although the cited reference Hirabayashi discloses multiple layers, Hirabayashi does not disclose a multi-layer wire having an upper layer selected from the group of *conductive material* consisting of molybdenum, chromium, tantalum, titanium, and alloys. Patentee respectfully submits that, not only the titanium nitride is not one of the listed conductive materials, the titanium nitride is not a conductive material at all. Patentee respectfully submits that the titanium nitride is not an alloy mixture, it is a non-conductive ceramic compound.

As defined in the chemistry field, and also explicitly taught in the college textbook "The Science and Design of Engineering Material" by Schaffer, the ceramic compounds are known as poor conductors of electricity due to the nature of ionic and/or

covalent bonding; such that they are frequently used as insulators[2]. Further support can be found in the U.S. Patent No. 5,158,657 issued to Kadokura, which Kadokura discloses a circuit substrate using the titanium nitride as an insulating film on the top of the conductive wire (Kadokura, abstract and column 3, last paragraph). Thus, Patentee respectfully submits that since the titanium nitride is known to be used as a insulator, then it cannot be considered as a conductive material; and since titanium nitride is not a conductive material, Hirabayashi's multi-layer wire cannot read on the recited limitation which explicitly recites that "an upper layer and a lower layer of *conductive* materials."

In addition, in a related judicial proceeding between the opposing party and the patentee, LG Display Co. LTD vs. AU Optronics Corporation, the court has explicitly held that Hirabayashi does not anticipate the instant patent, and stated that "…the instant patent's claim requires the upper layer wiring material to be selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof. However Hirabayashi discloses an upper layer of TiN, which is a ceramic compound, not a conductive material or a titanium alloy" (District Court opinion, page 70, 1st paragraph, lines 9-13).

Hirabayashi's titanium nitride layer is not one of the materials listed in the claim limitation. In particular, Hirabayashi's titanium nitride layer is neither the recited titanium nor an alloy thereof. Patentee further submits that Hirabayashi's titanium nitride cannot even be considered as equivalent to any of the recited materials since it is not a conductive material. Therefore, for the reason discussed above, Patentee respectfully submits that the cited reference Hirabayashi does not disclose every recited limitation in the amended claim 1 as required under 35 USC 102(b) or 35 USC 103(a); hence, Patentee respectfully requests the Office to withdraw the rejection over claim 9 accordingly, and to issue favorable re-consideration.

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2 Schaffer et al., "The Science and Design of Engineering Material", International Student Edition.

Claims 10-14

Claims 10 and 12-13 are now cancelled and the limitations previously recited in claims 10 and 12-13 are now inserted in the claim 9.

The claims 11 and 14 depend on claim 9; thus they incorporate every recited limitation in claim 9. For the reasons stated above, the claims 11 and 14 are not anticipated by Hirabayashi, and Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 11 and 14, and to issue favorable re-consideration.

Claims 15 and 16

The claims 15 and 16 depend on claim 9; thus they incorporate every recited limitation in claim 9. For at least the reasons stated above, the claims 15 and 16 are not anticipated by Hirabayashi.

Furthermore, the dependent claims 15 and 16 each require that "the upper layer wiring material is selected such that the upper layer wiring material does not become insolvent in an acid or alkaline etchant." The Specification explicitly stated that the dummy patterns are located between the pixel electrodes, i.e., the array, and the contact pads, to increase the density of the metal in areas between the pixel electrodes and the contact pads, so as to avoid passivation of the upper conductive material, and thus avoid undercut, during etching (Specification, Column 5, lines 11-38, column 5, line 55 to column 6 line 17). Patentee respectfully submits that the alleged dummy patterns in Hirabayashi are for a completely different purpose: to ensure uniform polishing of the substrate. Nothing in Hirabayashi discloses or suggests that dummy patterns are located in an area such that an upper layer wiring material does not become insolvent in an acid or alkaline etchant. There is no mention of the problem of an upper layer of wiring material becoming insoluble in an acid or alkaline etchant, much less a solution to that problem, in Hirabayashi.

For the reasons stated above, Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 15 and 16, and to issue favorable re-consideration.

35 U.S.C. §102(b) Rejection over Zhang

Claims 1-5, 7-13, and 15-16 are rejected under 35 U.S.C. §102(b), as being anticipated by Zhang. Patentee respectfully submits that Zhang does not disclose every recited limitation in claim 1. The amended claim 1 recites the following limitations:

> "An array substrate for display, comprising:
>
> a layer of an insulating substrate, having an area;
>
> a thin film transistor array formed on the insulating substrate;
>
> a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials, and the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof;
>
> connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;
>
> pixel electrodes, and
>
> dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, *the dummy conductive patterns situated between the connection pads and the pixel electrodes* such that the dummy patterns are not in contact with any of the wiring.."

Zhang Does Not Disclose the Recited Arrangement among Connection Pads, Dummy Conductive Patterns, and the Electrode as Recited in Claim 1

In particular, Patentee respectfully submits that the cited reference Zhang does not disclose or teach the limitation of the dummy conductive patterns *situated between the connection pads and the pixel electrodes.* As illustrated in the figure 2 of the instant patent, the dummy pattern 29 is located between the connection pad 27 and the pixel electrode 22.

The Office asserted that the proposed rejection CC-21 is adopted as proposed. The claim chart table in CC-21 alleged that Zhang discloses the reciting connection pads by disclosing that the signal lines 2 and scan lines 3 connect to extension terminal 6. The proposed rejection seems to equate the extension terminal 6 to the recited connections pads. The adapted rejection further alleged that the cited reference Zhang Figures 4, 8, and 16 disclose dummy wiring 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals (The adapted rejection, page CC21-1, last column of the table). Patentee respectfully disagrees. In particularly, Patentee respectfully submits that Zhang does not disclose or teach that the *dummy patterns are situated between the connection pads and the pixel electrodes* as recited in the claim 1.

The cited reference Zhang's figure 16 discloses a prior art without any dummy patterns but with a sealing material region 5 and extension terminal 6 located outside of the sealing material region 5 for connecting to the peripheral drive circuits. Zhang discloses that because the peripheral drive circuit is connected at the outside of the sealing material via the extension terminal 6, the moisture can enter into the electrode area and cause deterioration (Zhang, column 2, 3rd paragraph). The cited reference Zhang then discloses an improved embodiment in figures 1, 4, and 8. Zhang's figure 1 discloses an improved embodiment by relocating the peripheral drive circuits 103, 104, and additional extension terminal 303a within the sealed area surrounded by the sealing material region 107 (Zhang, column 8, 3rd paragraph, and column 10, lines 3-6, figure 4). Since the peripheral drive circuits, that the terminal 6 in Zhang's figure 16 is connecting to, are now located within the sealed area, Zhang's figures 4 and 8 implicitly disclose implementing figure 16's terminal 6 within the sealed area. Zhang further discloses positioning the alleged dummy patterns in the sealing material region 107, which is at the *outside* the electrodes, extension terminals, scanning line drive circuit 104, the signal line drive circuit 103. Zhang explicit discloses that the alleged dummy patterns are located in the sealing region 107 in order to uniform the sealing material's

structure for unifying the sealing as to overcome the problem know in the prior practice (Zhang, column 2, lines 45-52, and column 6, last paragraph to column 7, 1st paragraph).

Thus, patentee respectfully submits that Zhang does not disclose or teach that the dummy patterns are situated between the connection pad and the pixel section. As discussed above, Zhang discloses that the connection end 303a of the wiring 303 is located on the pixel section 102 side, which is within the sealed area; Zhang also implicitly discloses implementing figure 16's terminal 6 within the sealed area along with the driving circuits. Since Zhang's dummy patterns is on the sealing material region 107, Zhang's dummy patterns are located outside of the sealing area where all terminals, connection end 303a, and pixels reside. Since Zhang's dummy pattern is located outside of the sealing area where all terminals, connection end 303a, and pixels reside, Zhang's dummy pattern is not situated between the connection pads and the pixel electrodes as recited in the claim 1.

Hence, Patentee respectfully submits that Zhang does not disclose or teach that the recited limitation of "*the dummy conductive patterns situated between the connection pads and the pixel electrodes*". And for the reason discussed above, Patentee respectfully submits that the cited reference Zhang does not disclose every recited limitation in the claim 1 as required under 35 USC 102(b); hence, Patentee respectfully requests the Office to withdraw the rejection over claim 1 accordingly, and to issue favorable re-consideration.

Claims 2-6

Claims 2 and 4 are now cancelled and the limitations previously recited in claims 2 and 4 are now inserted in the claim 1. The remaining claims 3 and 5 depend on claim 1; thus they incorporate every recited limitation in claim 1. For the reasons stated above, the claims 3 and 5 are not anticipated by Zhang; and Patentee respectfully

requests the Office to withdraw the rejection over the remaining claims 3 and 5-8, and to issue favorable re-consideration.

Claims 7 and 8

The remaining claims 7 and 8 depend on claim 1; thus they incorporate every recited limitation in claim 1. For at least the reasons stated above, the claims 7 and 8 are not anticipated by Zhang.

Furthermore, the dependent claims 7 and 8 each require that "the upper layer wiring material is selected such that the upper layer wiring material does not become insolvent in an acid or alkaline etchant." The Specification explicitly stated that the dummy patterns are located between the pixel electrodes, i.e., the array, and the contact pads, to increase the density of the metal in areas between the pixel electrodes and the contact pads, so as to avoid passivation of the upper conductive layer, and thus avoid undercut, during etching (Specification, Column 5, lines 11-38, column 5, line 55 to column 6 line 17). Patentee respectfully submits that the alleged dummy patterns in Zhang are for a completely different purpose: unifying the sealing. Zhang explicit discloses that the alleged dummy patterns are located in the sealing region 107 in order to uniform the sealing material's structure for unifying the sealing as to overcome the problem know in the prior practice (Zhang, column 2, lines 45-52, and column 6, last paragraph to column 7, 1st paragraph). Nothing in Zhang discloses or suggests that dummy patterns are located in an area such that an upper layer wiring material does not become insolvent in an acid or alkaline etchant. There is no mention of the problem of an upper layer of wiring material becoming insoluble in an acid or alkaline etchant, much less a solution to that problem, in Zhang.

For the reasons stated above, Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 7 and 8, and to issue favorable re-consideration.

Zhang Does Not Disclose the Recited Arrangement among Connection Pads, Dummy Conductive Patterns, and the Electrode as Recited in Claim 9

Patentee respectfully submits that Zhang does not disclose every recited limitation in claim 9. The amended claim 9 recites the following limitations:

"A method for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array and a plurality of wirings on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials, and the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring."

In particular, Patentee respectfully submits that the cited reference Zhang does not disclose or teach the limitation of the dummy conductive patterns *situated between the connection pads and the pixel electrodes.* As illustrated in the figure 2 of the instant patent, the dummy pattern 29 is located between the connection pad 27 and the pixel electrode 22.

The Office asserted that the proposed rejection CC-21 is adopted as proposed. The claim chart table in CC-21 alleged that Zhang discloses the reciting connection pads by disclosing that the signal lines 2 and scan lines 3 connect to extension terminal

6. The proposed rejection maps the extension terminal 6 to the recited connections pads since each extension terminal 6 contacts the end of the at most one of the plurality of wirings (The adapted rejection, page CC21-1, 5th row of the table). The adapted rejection further alleged that the cited reference Zhang Figures 4, 8, and 16 disclose dummy wiring 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals (The adapted rejection, page CC21-1, last row of the table). Patentee respectfully disagrees. In particularly, Patentee respectfully submits that Zhang does not disclose or teach that the *dummy patterns are situated between the connection pads and the pixel electrodes* as recited in the claim 9.

The cited reference Zhang's figure 16 discloses a prior art without any dummy patterns but with a sealing material region 5 and extension terminal 6 located outside of the sealing material region 5 for connecting to the peripheral drive circuits. Zhang discloses that because the peripheral drive circuit is connected at the outside of the sealing material via the extension terminal 6, the moisture can enter into the electrode area and cause deterioration (Zhang, column 2, 3rd paragraph). The cited reference Zhang then discloses an improved embodiment in figures 1, 4, and 8. Zhang's figure 1 discloses an improved embodiment by relocating the peripheral drive circuits 103, 104, and additional extension terminal 303a within the sealed area surrounded by the sealing material region 107 (Zhang, column 8, 3rd paragraph, and column 10, lines 3-6, figure 4). Since the peripheral drive circuits, that the terminal 6 in Zhang's figure 16 is connecting to, are now located within the sealed area, Zhang's figures 4 and 8 implicitly disclose implementing figure 16's terminal 6 within the sealed area. Zhang further discloses positioning the alleged dummy patterns in the sealing material region 107, which is at the *outside* the electrodes, extension terminals, scanning line drive circuit 104, the signal line drive circuit 103. Zhang explicit discloses that the alleged dummy patterns are located in the sealing region 107 in order to uniform the sealing material's structure for unifying the sealing as to overcome the problem know in the prior practice

(Zhang, column 2, lines 45-52, and column 6, last paragraph to column 7, 1st paragraph).

Thus, patentee respectfully submits that Zhang does not disclose or teach that the dummy patterns are situated between the connection pad and the pixel section. As discussed above, Zhang discloses that the connection end 303a of the wiring 303 is located on the pixel section 102 side, which is within the sealed area; Zhang also implicitly discloses implementing figure 16's terminal 6 within the sealed area along with the driving circuits. Since Zhang's dummy patterns is on the sealing material region 107, Zhang's dummy patterns are located outside of the sealing area where all terminals, connection end 303a, and pixels reside. Since Zhang's dummy pattern is located outside of the sealing area where all terminals, connection end 303a, and pixels reside, Zhang's dummy pattern is not situated between the connection pads and the pixel electrodes as recited in the claim 9.

Hence, Patentee respectfully submits that Zhang does not disclose or teach that the recited limitation of "*the dummy conductive patterns situated between the connection pads and the pixel electrodes*". And for the reason discussed above, Patentee respectfully submits that the cited reference Zhang does not disclose every recited limitation in the claim 1 as required under 35 USC 102(b); hence, Patentee respectfully requests the Office to withdraw the rejection over claim 9 accordingly, and to issue favorable re-consideration.

Claims 10-14

Claims 10 and 12-13 are now cancelled and the limitations previously recited in claims 10 and 12-13 are now inserted in the claim 9. The remaining claims 11 and 14 depend on claim 9; thus they incorporate every recited limitation in claim 9. For the reasons stated above, the claims 11 and 14 are not anticipated by Zhang; and Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 11 and 14, and to issue favorable re-consideration.

Claims 15 and 16

The remaining claims 15 and 16 depend on claim 9; thus they incorporate every recited limitation in claim 9. For at least the reasons stated above, the claims 15 and 16 are not anticipated by Zhang.

Furthermore, the dependent claims 15 and 16 each require that "the upper layer wiring material is selected such that the upper layer wiring material does not become insolvent in an acid or alkaline etchant." The Specification explicitly stated that the dummy patterns are located between the pixel electrodes, i.e., the array, and the contact pads, to increase the density of the metal in areas between the pixel electrodes and the contact pads, so as to avoid passivation of the upper conductive layer, and thus avoid undercut, during etching (Specification, Column 5, lines 11-38, column 5, line 55 to column 6 line 17). Patentee respectfully submits that the alleged dummy patterns in Zhang are for a completely different purpose: unifying the sealing. Zhang explicit discloses that the alleged dummy patterns are located in the sealing region 107 in order to uniform the sealing material's structure for unifying the sealing as to overcome the problem know in the prior practice (Zhang, column 2, lines 45-52, and column 6, last paragraph to column 7, 1st paragraph). Nothing in Zhang discloses or suggests that dummy patterns are located in an area such that an upper layer wiring material does not become insolvent in an acid or alkaline etchant. There is no mention of the problem of an upper layer of wiring material becoming insoluble in an acid or alkaline etchant, much less a solution to that problem, in Zhang.

For the reasons stated above, Patentee respectfully requests the Office to withdraw the rejection over the remaining claims 15 and 16, and to issue favorable re-consideration.

New Claim 17

The new claim 17 is added in this paper. The claim 17 recites the following limitations:

"An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring directly connects with at least one of the transistors in the thin film array;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patterns are not in contact with any of the wirings."

The claim 17 recites the similar limitations as previously recited in claim 1. The claim 17 further recites that the wiring directly connects with at least one of the transistors in the thin film array. Patentee respectfully submits that none of the cited references on record discloses or teach this limitation in combination with the rest of the recited limitations, such as the limitation that the dummy conductive patterns are situated between the connection pads and the pixel electrodes and t

he dummy patterns are not in contact with any of the wirings. Thus, patentee respectfully requests the Office to allow and confirm the newly added claim 17 along with the claims **1, 3, 5-9, 11, and 14-16**.

Conclusion

Claims 1, 3, 5-9, 11, and 14-17 are pending in this proceeding. In view of the reasons stated above, Patentee respectfully submits that the independent claims patentably define the present invention over the citations of record, and Patentee respectfully requests a favorable reconsideration and issuing allowance accordingly. Further, the dependent claims should also be allowable for the same reasons as their respective base claims and further due to the additional features that they recite. Separate and individual consideration of the dependent claims is respectfully requested. Examiner is invited to contact the attorney on record to expedite the prosecution in pursuance of allowance.

Respectfully submitted,
WPAT, P.C.

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Registration No. 50,464

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EXHIBIT A

“The Science and Design of Engineering Material”

THE SCIENCE AND DESIGN OF ENGINEERING MATERIALS

INTERNATIONAL STUDENT EDITION

SCHAFFER SAXENA ANTOLOVICH SANDERS WARNER

are excellent conductors of electricity, are relatively strong, are dense, can be deformed into complex shapes, and are resistant to breaking in a brittle manner when subjected to high-impact forces. This set of mechanical and physical properties makes metals one of the most important classes of materials for both electrical and structural applications. Extensive (and in some cases exclusive) use of metals occurs in automobiles, airplanes, buildings, bridges, machine tools, ships, and many other applications where a combination of high strength and resistance to brittle fracture is required. In fact, it is largely the excellent combination of strength and toughness (i.e., resistance to fracture) that makes metals so attractive as structural materials.

The basic understanding of metals and their properties is advanced, and they are considered to be mature materials with relatively little potential for major breakthroughs. However, significant improvements have been and continue to be made as a result of advances in processing. Two examples are:

Higher operating temperatures in jet engines have been attained through the use of turbine blades that are produced by controlled solidification processes. The blades are made of nickel and other metal alloys (atomic-scale mixtures of atoms) and are in wide commercial use. Improvements will continue as processes are refined through use of advanced sensors and real-time computer control.

Frequently parts are fabricated from metal powders by compacting them into a desired shape at high temperature and pressure in a process known as powder metallurgy (PM). An important reason for using PM processing is reduced fabrication costs. While some improvement in properties can be obtained through PM, a major benefit is the reduced variation in properties, which will allow the operating loads to be safely increased. Reduced production costs through PM will continue to impact the aerospace and automotive fields.

1.4.2 Ceramics

Ceramics are composed of both metallic and nonmetallic atomic species. Many (but not all) ceramics are crystalline, and frequently the nonmetal is oxygen, as in Al_2O_3, MgO, and CaO, all of which are typical ceramics. One significant difference between ceramics and metals is that in ceramics, bonding is ionic and/or covalent. As a result there are no ''free'' electrons in ceramics. They are generally poor conductors of electricity, but are frequently used as insulators in electrical applications. One familiar example is spark plugs, in which a ceramic insulator separates the metal components.

Ionic and covalent bonds are extremely strong. As a result, ceramic materials are intrinsically stronger than metals. However, because of their more complex structure, the ions/atoms cannot easily be displaced as a result of applied forces. Rather than bend to accommodate such forces, ceramics tend to fracture in a brittle manner. This brittleness generally limits their use as structural materials, although recent improvements have been made by incorporating ceramic fibers into a ceramic matrix and other innovative techniques. Their rigid bond structure confers other advantages, including high temperature stability, resistance to chemical attack, and resistance to absorption of foreign substances. They are thus ideal in high-temperature applications such as the space shuttle, as containers for reactive chemicals, and as bowls and plates for foods where surface contamination is undesirable.

are excellent conductors of electricity, are relatively strong, are dense, can be deformed into complex shapes, and are resistant to breaking in a brittle manner when subjected to high-impact forces. This set of mechanical and physical properties makes metals one of the most important classes of materials for both electrical and structural applications. Extensive (and in some cases exclusive) use of metals occurs in automobiles, airplanes, buildings, bridges, machine tools, ships, and many other applications where a combination of high strength and resistance to brittle fracture is required. In fact, it is largely the excellent combination of strength and toughness (i.e., resistance to fracture) that makes metals so attractive as structural materials.

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Ionic and covalent bonds are extremely strong. As a result, ceramic materials are intrinsically stronger than metals. However, because of their more complex structure, the ions/atoms cannot easily be displaced as a result of applied forces. Rather than bend to accommodate such forces, ceramics tend to fracture in a brittle manner. This brittleness generally limits their use as structural materials, although recent improvements have been made by incorporating ceramic fibers into a ceramic matrix and other innovative techniques. Their rigid bond structure confers other advantages, including high temperature stability, resistance to chemical attack, and resistance to absorption of foreign substances. They are thus ideal in high-temperature applications such as the space shuttle, as containers for reactive chemicals, and as bowls and plates for foods where surface contamination is undesirable.

Some ceramics are not crystalline. The most common example is window glass, which is composed of various metal oxides. Optical properties are of major importance in glass and may be controlled through composition and processing. In addition the thermal and mechanical properties of glass can also be controlled. Safety glass is simply glass that has been subjected to a thermal cycle that leaves the surface in a state of compression and thereby resistant to cracking. In fact, glass treated in this way is even difficult to crack when struck with a hammer!

Some current and potential applications for ceramic materials with a large economic impact are listed below:

- In the automotive industry the thermal and strength properties of ceramics make them very attractive for engine components. For example, there are over 60,000 autos in Japan with ceramic turbochargers, which increase the efficiency of the automobile. The materials in this application are Si_3N_4 or SiC processed to have some ability to resist brittle fracture.
- Ceramics based on compounds such as $YBa_2Cu_3O_7$ and $Ba_2Sr_2CaCu_2O_x$ have increased critical superconducting temperatures to >95K. This means that superconducting films may be used as liners in microwave devices and as wires for all kinds of applications. Improving the current carrying capacity and connection technology are essential for widespread application of these materials.
- Next-generation computers will have ceramic electro-optic components that will give increased speed and efficiency.

1.4.3 Polymers

Polymers consist of long chain molecules with repeating groups that are largely covalently bonded. Common elements within the chain backbone include C, O, N, and Si. An example of a common polymer with a simple structure, polyethylene, is shown in Figure 1.4–1. The bonds within the backbone are all covalent, so the molecular chains are extremely strong. Chains are usually bonded to each other, however, by means of comparatively weak secondary bonds. This means that it is generally easy for the chains to slide by one another when forces are applied and the strength is thus relatively low. In addition, many polymers tend to soften at moderate temperatures, so they are not generally useful for high-temperature applications.

Polymers, however, have properties that make them attractive in many applications. Since they contain common elements and are relatively easy to synthesize, or exist in nature, they can be inexpensive. They have a low density (in part because of the light elements from which they are constituted) and are easily formed into complex shapes. They have thus replaced metals for molded parts in automobiles

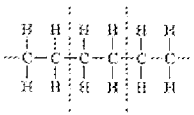

Figure 1.4–1 Schematic of the structure of polyethylene. The mer or basic repeating unit in the polymer is the $-C_2H_4-$ group.

EXHIBIT B

U.S. Patent No. 5,158,657 (Kadokura)

US005158657A

United States Patent [19]

Kadokura

[11] Patent Number: 5,158,657

[45] Date of Patent: Oct. 27, 1992

[54] CIRCUIT SUBSTRATE AND PROCESS FOR ITS PRODUCTION

[75] Inventor: Susumu Kadokura, Sagamihara, Japan

[73] Assignee: Canon Kabushiki Kaisha, Tokyo, Japan

[21] Appl. No.: 673,028

[22] Filed: Mar. 21, 1991

[30] Foreign Application Priority Data

Mar. 22, 1990	[JP]	Japan	2-75148
Mar. 23, 1990	[JP]	Japan	2-72177
Mar. 23, 1990	[JP]	Japan	2-74653
Mar. 24, 1990	[JP]	Japan	2-74203
Mar. 26, 1990	[JP]	Japan	2-77494
Mar. 26, 1990	[JP]	Japan	2-77495

[51] Int. Cl.[5] C25D 13/04

[52] U.S. Cl. 204/181.1; 205/125

[58] Field of Search 204/181.1, 180.2

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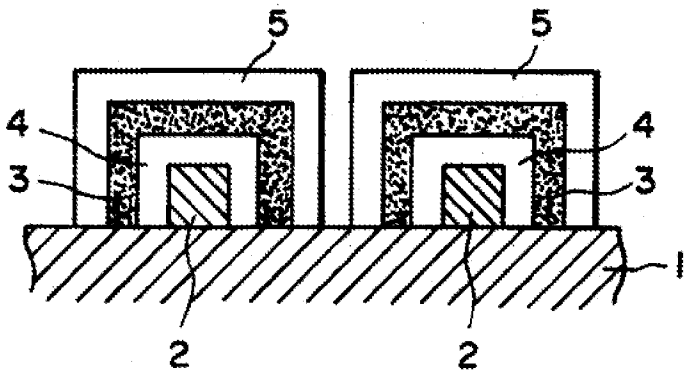
022885	1/1990	Japan .
138798	5/1990	Japan .

Primary Examiner—John Niebling
Assistant Examiner—Kishor Mayekar
Attorney, Agent, or Firm—Fitzpatrick, Cella, Harper & Scinto

[57] ABSTRACT

A circuit substrate has a substrate, a conductor wire provided on the substrate, a first insulating film that covers the conductor wire, and a conductive film that covers the first insulating film. At least one of the first insulating film and the conductive film is formed by electro-deposition coating.

18 Claims, 1 Drawing Sheet



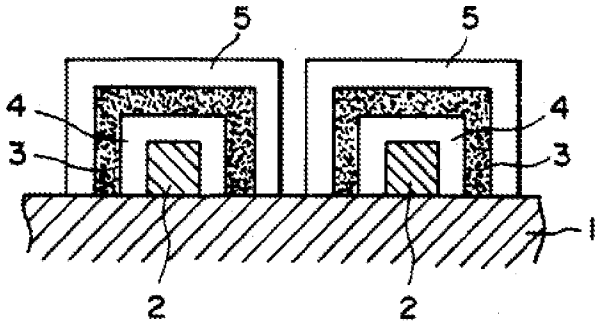

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FIG. 1

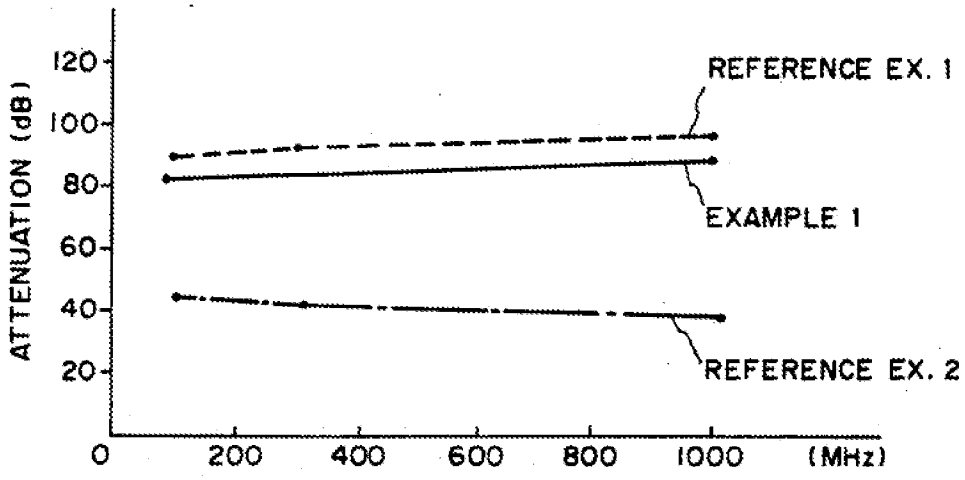
ATTENUATION (dB)
120
100
80
60
40
20
0
200
400
600
800
1000
(MHz)
REFERENCE EX. 1
EXAMPLE 1
REFERENCE EX. 2

FIG. 2

CIRCUIT SUBSTRATE AND PROCESS FOR ITS PRODUCTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a circuit substrate and a process for producing it. More particularly the present invention relates to a circuit substrate used in optical instruments such as cameras, home electric appliances, computers, word processors, measuring devices or the like, and a process for producing such a circuit substrate.

2. Related Background Art

Conventional processes commonly used to produce circuit substrates comprise the steps of (1) forming a copper foil circuit pattern on an insulated substrate by photolithography, or by screen printing using a conductive paste, (2) thereafter coating a solder resist or the like on the surface of the circuit to provide thereon an insulating layer, (3) subsequently coating a conductive paste on the surface of the insulating layer to provide thereon a shielding layer, and (4) further coating a solder resist or the like on the shielding layer to provide thereon an insulating layer. Methods for electromagnetic wave shielding may include, in addition to a method of providing the above shielding layer, a method in which shielding is effected by surrounding a circuit substrate with a sheet metal. The insulating layer on the circuit pattern can also be provided by laminating a dry film.

The conventional processes for producing circuit substrates, however, provide an insulating layer having a small thickness at the corners of copper wires that constitute a this arrangement results in a break of the insulating layer at the parts corresponding thereto. The conventional processes for producing circuit substrates also tend to cause a dielectric breakdown or defective insulation because of inclusion of bubbles or the like between copper wires, exacerbating the problem. In addition, the conventional processes for producing circuit substrates require complicated production steps which take a long time for their manufacture, also bringing about a problem in cost.

As for the conventional method in which shielding is effected by surrounding a circuit substrate with a sheet metal, it requires a broad space in order for the metal sheet to be provided, and hence has been not suitable for making products small-sized.

SUMMARY OF THE INVENTION

The present invention was made in order to overcome such disadvantages involved in the prior art. An object of the present invention is to provide a circuit substrate can provide uniform layer thicknesses for the insulating layer and shielding layer on a circuit pattern, can be free from defective insulation, and can also promise a high electromagnetic wave shielding effect, and a process for producing such a circuit substrate.

The circuit substrate of the present invention comprises a substrate, a conductor wire provided on said substrate, a first insulating film that covers said conductor wire, and a conductive film that covers said first insulating film; at least one of said first insulating film and said conductive film is formed by electro-deposition coating.

The process for producing a circuit substrate of the present invention comprises a first step of forming on a substrate a circuit pattern comprised of a conductor wire, a second step of providing a first insulating film to cover said circuit pattern, and a third step of providing a conductive film to cover said first insulating film. Electro-deposition coating is used in at least one step of said second step and said third step. Said electro-deposition coating is carried out by immersing said substrate in an electro-deposition coating composition, setting said conductor wire as an electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-section illustrating an example of the construction of the circuit substrate according to the present invention.

FIG. 2 is a graph illustrating an electromagnetic wave shielding effect of the circuit substrate according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The circuit substrate of the present invention can be used in all sorts of electric apparatuses including optical instruments such as cameras, home electric appliances, word processors, computers and measuring devices. The circuit substrate of the present invention comprises, as shown in FIG. 1, an insulated substrate 1 having a conductor wire 2 formed thereon, a first insulating film 4 that covers the whole surface of the conductor wire 2, and a conductive film 3 that covers the whole surface of the first insulating film 4. The conductive film 3 serves as a shielding layer that effects electromagnetic wave shielding. The conductor wire 2 forms a circuit pattern on the insulated substrate 1. The conductor wire 2 may preferably be formed of copper. The whole surface of the insulating film 4 may optionally be covered with an additional insulating film 5 (a second insulating film). The insulating film 5 is provided to prevent the circuit substrate of the present invention from contacting other component parts to short, when it has been set in an electric apparatus.

In the circuit substrate of the present invention, at least one of the films 3, 4 and 5 is formed by electro-deposition coating. A coating formed by the electro-deposition coating is finally cured by heating or irradiation with light.

The electro-deposition coating refers to a process in which a pair of electrodes are disposed in a solution in which a substance that gives a coating film has been dissolved (hereinafter "electro-deposition coating composition") and a DC current is applied to cause the substance to adhere onto one of the electrodes. Thus, in the present invention, the conductor wire 2 formed on the substrate serves as one of the electrodes. As the other electrode, it is preferred to use, for example, a stainless steel plate.

Proposals have been hitherto made on the electro-deposition coating. For example, Japanese Patent Application Laid-open No. 55-11175 proposes a method in which an electro-deposition coating composition is applied twice superposingly. The present applicants have also proposed in Japanese Patent Application Laid-open No. 2-6564 an electro-deposition coating composition containing a ceramic powder and a fluorine resin powder.

As the insulated substrate 1, it is possible to use commonly known insulated substrates as exemplified by those made of a polycarbonate resin, a polyetherimide

resin, a glass fiber packed ABS resin, a glass epoxy resin or the like.

The circuit pattern formed by the use of the conductor wire 2 can be formed by commonly known photolithography. More specifically, the circuit pattern can be formed by laminating, for example, copper foil on the insulated substrate 1, further coating a resist on the copper foil, and then exposing the resist coating to light through a mask having the desired pattern, followed by development and etching.

On the whole surface of the conductor wire 2, the insulating film 4 is formed by electro-deposition coating by the use of a resin feasible for electro-deposition.

Resins used in the electro-deposition coating have been hitherto studied in variety. In order for resin to be electro-deposited, the resin must be capable of being charged when the electro-deposition coating is carried out. The charged resin is attracted toward the anode or cathode when a DC current is applied, and thus deposited on the electrode to give a coating. As the resin used in the present invention, it is possible to use resins conventionally used in electro-deposition coating, as exemplified by those of an acrylic melamine type, an acrylic type, an epoxy type, a urethane type, an alkyd type or the like. The resin used in the present invention may be of either an anionic type or a cationic type. From the viewpoint of practical use, it is preferred to use a water-soluble resin or water-dispersible resin having a carboxyl group. Resin prepolymers having carboxyl groups can be dissolved or dispersed in water after they have been neutralized with ammonia or organic amines.

The resin in the electro-deposition coating composition should be in a concentration of from 5% by weight to 20% by weight, and preferably from 7% by weight to 15% by weight.

The electro-deposition coating composition used in the present invention may preferably be prepared by dissolving or dispersing the desired resin in water. The electro-deposition coating composition may further contain an organic solvent of an alcohol type, a glycol type or the like. Such an organic solvent is enough if it is contained in an amount of several % by weight.

The insulating film 4 may be incorporated with a ceramic powder. The insulating film 4 incorporated with the ceramic powder can be well cured at a low temperature of, for example, from 90° C. to 100° C. when the insulating film 4 is heated to effect curing. As a result, it becomes possible to obtain a circuit substrate free from thermal deformation.

Although it is unclear why the heat curing can be carried out at a low temperature when the electro-deposition coating film is formed using an electro-deposition coating composition containing the ceramic powder, it can be presumed that the ceramic powder is different from metal particles whose surfaces are susceptible to immediate oxidation and its particle surfaces kept activated to a certain degree can be maintained in a stable state, so that the active particle surfaces of the powder serve as cross-link points at the time of curing to accelerate the curing of the coating formed by electro-deposition.

The ceramic powder incorporated into the insulating film 4 includes, for example, aluminum oxide, titanium nitride, manganese nitride, tungsten nitride, tungsten carbide, lanthanum nitride, aluminum silicate, molybdenum disulfide, titanium oxide, graphite, and silicic acid compounds.

A ceramic powder with an excessively large particle diameter brings about an excessive curing of the insulating film 4 to make the film brittle. On the other hand, a ceramic powder with an excessively small particle diameter makes it impossible to achieve a sufficient effect. Hence, the ceramic powder may preferably have an average particle diameter ranging from 0.1 μm to 5 μm, and particularly from 0.5 μm to 2 μm.

As to the amount of the ceramic powder contained in the electro-deposition coating composition used to form the insulating film 4, the ceramic powder may preferably be in an amount of from 0.5 part by weight to 30 parts by weight, and particularly from 2 parts by weight to 25 parts by weight, based on 100 parts by weight of the resin feasible for electro-deposition, in order to obtain a coating that can give good coating film properties, e.g., adhesion, and also can be cured even at a low temperature. The ceramic powder may preferably be contained in the insulating film 4 in a deposition quantity of from 10% by weight to 30% by weight, and particularly from 15% by weight to 25% by weight.

The reason why the powder can be deposited in the coating formed as a result of the electro-deposition coating carried out using the electro-deposition coating composition containing the powder is presumed due to the fact that resin molecules are adsorbed around powder particles in the electro-deposition coating composition and the resin molecules are attracted toward the electrode, with which the powder also is moved toward the electrode.

After the formation of the insulating film 4, the conductive film 3 is formed on the whole surface of the insulating film 4. The conductive film 3 is formed by electro-deposition coating using an electro-deposition coating composition containing a conductive powder. As the conductive powder contained in the electro-deposition coating composition, it is preferred to use a ceramic powder whose particle surfaces are coated with a metal (hereinafter "metallized ceramic powder") or a natural mica powder whose particle surfaces are coated with a metal (hereinafter "metallized natural mica powder"). Only one of the metallized ceramic powder and the metallized natural mica powder may be contained in the electro-deposition coating composition, or both of them may be contained in the form of a mixture. Incorporation of the metallized ceramic powder or metallized natural mica powder in the electro-deposition deposition coating composition is preferable since, as previously described, it enables complete curing at a low temperature of from 90° C. to 100° C., which is usually required to be 130° C. to 180° C. as a heating temperature, when the electro-deposition coating is cured by heat treatment after completion of electro-deposition.

The metallized ceramic powder or metallized natural mica powder used in the present invention may include a ceramic powder or natural mica powder whose particles surfaces are coated with Cu, Ni, Ag, Au, Sn or the like. For the coating of the particle surfaces of these powders, Cu, Ag, and Ni can be preferably used in view of the shielding performance and cost. As a method for the coating of the powder particle surfaces, it is suitable to use electroless plating. A superior shielding performance and good coating film properties at the time of low-temperature curing can be obtained when the powder particle surfaces are coated in a coating thickness of from 0.05 μm to 3 μm, and particularly from 0.15 μm to 2 μm. Formation of coatings with a thickness of more

than 3 μm makes the surface properties analogous to those of metal particles, so that the coatings are oxidized in the air because of their very active surfaces to tend to result in an insufficient curing of electro-deposition coatings at the time of low-temperature curing.

When Ni coatings are formed on the powder particles, the method as disclosed, for example, in Japanese Patent Application Laid-open No. 61-276979 can be used, according to which a water-based suspension of the powder is prepared, and then an aged solution for electroless nickel plating is added to the suspension to form nickel coatings on the powder particle surfaces so that Ni coatings with a low phosphorus content, e.g., of 5% or less can be applied. Thus it is possible to form an electro-deposition coating having an improved conductivity and substantially the same shielding properties as in Cu-coated powder.

As the ceramic powder used in the conductive powder, it is possible to use the same ceramic powder as the one incorporated into the insulating film **4**. The natural mica may include phlogopite, serisite and muscovite.

The metallized ceramic powder and the metallized natural mica powder should have an average particle diameter of from 0.1 μm to 5 μm, and preferably from 0.5 μm to 2 μm. A powder with an average particle diameter smaller than 0.1 μm may cause secondary agglomeration. On the other hand, a powder with an average particle diameter larger than 5 μm is not preferred in view of a problem of sedimentation of particles or decorativeness of coating films.

As the conductive particles, in addition to the metallized ceramic powder and the metallized natural mica powder, it is also possible to use a resin powder whose particle surfaces are coated with a metal (hereinafter "metallized resin powder") or a metal powder.

As the resin powder used in the metallized resin powder, it is possible to use, for example, fluorine resins, polyethylene resins, acrylic resins, polystyrene resins and nylons. The metal coating applied to the surfaces of the resin powder particles may be the same as used in the case of the metallized ceramic powder. The metallized resin powder may also have the same average particle diameter as in the case of the metallized ceramic powder.

The metal powder includes, for example, powders of Au, Pd, Ag, Ni, Cu, Sn, Co, Mn, Fe, Te, etc. The metal powder should have an average particle diameter ranging from 0.01 μm to 5 μm, preferably from 0.05 μm to 4 μm, and more preferably from 0.05 μm to 0.1 μm. A powder with an average particle diameter smaller than 0.01 μm may cause secondary agglomeration. On the other hand, a powder with an average particle diameter larger than 5 μm may result in sedimentation of particles in the electro-deposition coating composition. It is preferred for the metal powder to be those produced by, for example, heat plasma evaporation.

In the present invention, the particle diameters of the conductive powder are values measured using a centrifugal sedimentation type particle size distribution measuring device. What is actually used as this measuring device is SACP-3 (trade name; manufactured by Shimadzu Corporation).

The conductive powder should be contained in the electro-deposition coating composition in an amount ranging from 0.2 part by weight to 30 parts by weight, preferably from 10 parts by weight to 20 parts by weight, and more preferably from 7 parts by weight to 15 parts by weight, based on 100 parts by weight of the resin feasible for electro-deposition.

The presence of the conductive powder in the conductive film **3** can be determined using an X-ray microanalyzer. The deposition quantity of the conductive powder can be measured by analysis according to thermogravimetry analysis. The deposition quantity of the conductive powder in the coating film **3** may preferably be in the range of from 5% by weight to 50% by weight, particularly from 10 % by weight to 40% by weight, and more preferably from 15% by weight to 35% by weight.

As the conductive powder contained in the conductive film **3**, only one of the metallized ceramic powder, the metallized natural mica powder, the metallized resin powder and the metal powder may be used, or two or more of them as exemplified by the metallized ceramic powder and the metal powder may be used. It is preferred to use a conductive powder comprised of a mixture of at lease one conductive powder selected from the metallized ceramic powder and the metallized natural mica powder and at least one conductive powder selected from the metallized resin powder and the metal powder. This is because the gaps between particles of the metallized ceramic powder and/or metallized natural mica powder are filled with particles of the metal powder and/or metallized resin powder to increase contact areas between each powder, so that the shielding properties can be more improved and also the conductive film **3** can be cured at the low temperature by the action of the metallized ceramic powder and/or metallized natural mica powder. In this instance, the conductive powders may preferably be mixed in such a proportion that at least one conductive powder selected from the metallized resin powder and the metal powder is in an amount of from 20 parts by weight to 300 parts by weight based on 100 parts by weight of at least one conductive powder selected from the metallized ceramic powder and metallized natural mica powder.

Because of the formation of the conductive film **3** by electro-deposition coating, the conductive powder can be deposited in the conductive film **3** in a high density, and the film **3** can exhibit a superior shielding performance even if it is a thin film.

After the formation of the conductive film **3**, the insulating film **5** is optionally formed on the whole surface of the conductive film **3**. The insulating film **5** may be formed using the same material as the materials described in respect of the insulating film **4** and in the same manner as the formation of the insulating film **4**. Accordingly, the ceramic powder may be incorporated or need not be incorporated also in respect of the insulating film **5**. The ceramic powder may be contained in both the insulating film **4** and insulating film **5** or may be contained in only one of them. Alternatively, the ceramic powder may be contained in neither the insulating film **4** nor the insulating film **5**.

After the insulating film **4**, the conductive film **3** and the optional insulating film **5** are formed on the whole surface of the conductor wire **2**, the insulating films **4** and **5** and the conductive film **3** are cured by heat or light, or by both of them. The energy by which the resin is cured may be either of heat and light, but heat is preferred in view of the advantage that it can be applied uniformly and yet with ease. The films may be cured preferably at a temperature of from 90° C. to 100° C. for a heating time of from 20 minutes to 180 minutes. It is also possible to effect curing of the insulating films or

the conductive film by the use of energy other than heat and light.

The insulating film **4** may preferably have a thickness of from 5 μm to 30 μm, and more preferably from 7 μm to 25 μm.

The conductive film **3** may preferably have a thickness of from 7 μm to 40 μm, and more preferably from 10 μm to 25 μm.

The insulating film **5** optionally provided may preferably have a thickness of from 10 μm to 30 μm, and more preferably from 10 μm to 25 μm.

In the case when the insulating films **4** and **5** and the conductive film **3** are formed by electro-deposition coating, the substrate made to serve as one electrode is immersed in an electro-deposition coating composition together with the other electrode to carry out the electro-deposition coating. The electro-deposition coating composition may preferably be kept at a temperature of from 20° C. to 25° C. and have a hydrogen-ion concentration corresponding to pH 8 to 9. The voltage to be applied may preferably be a DC voltage of from 50 V to 170 V and the electro-deposition may preferably be carried out at a current density of from 0.5 A/dm^2 to 3 A/dm^2 for a treatment time of from 1 minute to 5 minutes. The resins used for the insulating films **4** and **5** and the conductive film **3** may be changed in their kinds for each film.

As described above, the present invention makes it possible to form the insulating film and conductive film of a circuit substrate as thin films which are dense and uniform in thickness. It also makes it possible to obtain a circuit substrate free from defective insulation and having a superior electromagnetic wave shielding effect.

The present invention will be described below in greater detail by giving Examples. The present invention is by no means limited to these Examples only.

EXAMPLE 1

To the surface of a glass epoxy resin substrate of 0.6 mm thick, laminated thereon with copper foil of 18 μm thick, a negative resist (trade name: OMR-83; produced by Tokyo Ohka Kogyo Co., Ltd.; viscosity: 450 cp) was applied by spin coating to form a photosensitive material layer of 5 μm thick. Subsequently, the resist coating was exposed to light using pattern masks of from 0.5 to 50 mm in line width and from 1 to 20 mm in space, followed by development. Next, using a copper etchant (trade name: Alfine; produced by Uemura Kogyo K.K.), etching was carried out according to a spray system to form a copper circuit pattern.

Thereafter, using an electro-deposition coating composition prepared by diluting an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) with desalted water to a concentration of 15% by weight, a DC voltage of 150 V was applied for 3 minutes under conditions of pH 8.5 and a bath temperature of 25° C., setting the substrate as the anode and a stainless steel sheet as the cathode. Thus an insulating film **4** of 15 μm thick was formed on the copper circuit pattern.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts of an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 15 parts by weight of an alumina powder with an average particle diameter of 0.7 μm whose particle surfaces were coated with nickel in a thickness of 0.2 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 17 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance and specific volume resistance of the resulting circuit substrate were evaluated or measured. Results obtained are shown in Tables 1 to 3 below.

The resulting insulating film and conductive film were dense and well adhered to adjoining films, having satisfactory resistance to acids, resistance to alkalis and resistance to flame.

The electromagnetic wave shielding effect of the circuit substrate was also measured by the transmission line method (ASTM ES7-83 Method) after it was set in an apparatus. The result is shown in FIG. **2**. As shown in FIG. **2**, the electromagnetic wave shielding effect was substantially the same as in the case of electroless plating (see Reference Examples 1 and 2).

This circuit substrate was crosscut as shown in FIG. **1** to observe its cross section using a metallurgical microscope (magnifications: 400) manufactured by Olympus Optical Co., Ltd. As a result, it was confirmed that all the insulating films **4** and **5** and the conductive film **3** were formed in uniform thicknesses.

REFERENCE EXAMPLE 1

On an ABS resin substrate, a copper thin film of 0.7 μm thick and a nickel thin film of 0.4 μm thick were successively laminated by electroless plating to give a metal-coated member.

The electromagnetic wave shielding effect of this metal-coated member was measured in the same manner as in Example 1. The result is shown in FIG. **2**.

REFERENCE EXAMPLE 2

On an ABS resin substrate, a coating composition comprising a nickel powder was sprayed to form thereon a nickel coating.

The electromagnetic wave shielding effect of the resulting member on which this nickel coating had been formed was measured in the same manner as in Example 1. The result is shown in FIG. **2**.

COMPARATIVE EXAMPLE 1

To the surface of the same glass epoxy resin substrate as used in Example 1, a copper circuit pattern was formed in the same manner as in Example 1, and thereafter a solder resist (trade name: FINEDEL DSR-2200(C); produced by Tamura Seisakusho), a silver paste (trade name LS-500; produced by Asahi Kagaku Kenkyusho) and a solder resist (trade name: FINEDEL DSR-2200(C); produced by Tamura Seisakusho) were applied successively from the substrate side in thick-

nesses of 30 μm, 35 μm and 30 μm, respectively, to give a circuit substrate.

Physical properties, insulation resistance and specific volume resistance of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. Results obtained are shown in Tables 1 to 3.

TABLE 1

Results of Evaluation on Physical Properties of Film

Adhesion	Resistance to acids	Resistance to alkalis	Resist. to flame
Example 1:			
Adhesion rate: 100/100 Completely adhered.	No changes in insulating film.	No changes in insulating film.	Cleared 94V-0.
Comparative Example 1:			
Adhesion rate: 95/100 A little peeled.	A little change in insulating film.	A little change in insulating film.	Cleared 94V-1.

Notes:
Tests on the items in the above table were carried out by the following methods:
(1) Adhesion: JIS D0202
(2) Resistance to acids: Immersion treatment with 10 vol. % H_2SO_4 at room temperature for 20 minutes.
(3) Resistance to alkalis: Immersion treatment with 5 wt. % NaOH at room temperature for 30 minutes.
(4) Resistance to flame: UL94 Test Method.

TABLE 2

Insulation Resistance of Film

	Initial value	After 96 hour moisture absorption treatment
Example 1:	1.7×10^{13} Ω · cm	1.5×10^{13} Ω · cm
Comparative Example 1:	1.0×10^{13} Ω · cm	1.6×10^{11} Ω · cm

Notes:
The insulation resistance in the above table was measured according to JIS Z3197; comb electrode G-10; substrate moisture absorption treatment: at 55° C., 98% RH, DC 500 V for 1 minute. The resistivity was measured using a insulation resistance measuring device HP4329A, manufactured by YHP Co.

TABLE 3

Specific Volume Resistance of Film

	Initial value	After 96 hour moisture absorption treatment
Example 1:	1.5×10^{13} Ω · cm	1.4×10^{13} Ω · cm
Comparative Example 1:	1.2×10^{13} Ω · cm	1.8×10^{10} Ω · cm

Notes:
The above specific resistivity was measured according to JIS C6481.

EXAMPLE 2

A circuit substrate of the present invention was prepared in the same manner as in Example 1 except that 15 parts by weight of the nickel-coated alumina powder used in Example 1 was replaced with 10 parts by weight of copper-coated alumina powder. Coating thickness of the copper-coated alumina powder was 0.2 μm. Average particle diameter of the alumina powder was 1.2 μm.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 3

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern and an insulating film **4** were formed in the same manner as in Example 1.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 7 parts by weight of an alumina powder with an average particle diameter of 1.0 μm whose particle surfaces were coated with copper in a thickness of 0.2 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 17 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame) and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 4

On a glass epoxy resin substrate of 0.8 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, using an electro-deposition coating composition prepared by diluting an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.) with desalted water to a concentration of 15% by weight, a DC voltage of 150 V was applied for 3 minutes under conditions of pH 8.5 and a bath temperature of 25° C., setting the substrate as the anode and a stainless steel sheet as the cathode. Thus an insulating film **4** of 15 μm thick was formed on the copper circuit pattern.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.) separately made ready for use, 7 parts by weight of an alumina powder with an average particle diameter of 1.0 μm whose particle surfaces were coated with nickel in a thickness of 0.1 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 17 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 5

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern and an insulating film **4** were formed in the same manner as in Example 1.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 10 parts by weight of a copper powder with an average particle diameter of 0.03 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 17 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 6

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern and an insulating film **4** were formed in the same manner as in Example 1.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 10 parts by weight of a copper powder with an average particle diameter of 0.02 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 15 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame) and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 7

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, using an electro-deposition coating composition prepared by diluting an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.) with desalted water to a concentration of 15% by weight, a DC voltage of 150 V was applied for 3 minutes under conditions of pH 8.5 and a bath temperature of 25° C., setting the substrate as the anode and a stainless steel sheet as the cathode. Thus an insulating film **4** of 15 μm thick was formed on the copper circuit pattern.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.) separately made ready for use, 15 parts by weight of a nickel powder with an average particle diameter of 0.03 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 20 μm thick was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 8

A circuit substrate of the present invention was prepared in the same manner as in Example 1 except that 15 parts by weight of the nickel-coated alumina powder used in Example 1 was replaced with a mixture of 7 parts by weight of nickel-coated alumina powder and 5

parts by weight of copper powder. Coating thickness of the nickel-coated alumina powder was 0.2 μm. Average particle diameter of the alumina powder was 1.2 μm. Average particle diameter of the copper powder was 0.03 μm.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 9

A circuit substrate of the present invention was prepared in the same manner as in Example 6 except that 10 parts by weight of the copper powder used in Example 6 was replaced with a mixture of 5 parts by weight of nickel-coated alumina powder and 10 parts by weight of copper powder. Coating thickness of the nickel-coated alumina powder was 0.2 μm. Average particle diameter of the alumina powder was 1.0 μm. Average particle diameter of the copper powder was 0.02 μm.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame) and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 10

A circuit substrate of the present invention was prepared in the same manner as in Example 4 except that 7 parts by weight of the nickel-coated alumina powder used in Example 4 was replaced with a mixture of 7 parts by weight of copper-coated alumina powder and 5 parts by weight of nickel powder. Coating thickness of the copper-coated alumina powder was 0.2 μm. Average particle diameter of the alumina powder was 1.0 μm. Average particle diameter of the nickel powder was 0.03 μm.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame) insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 1. As a result, the same good results as in Example 1 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 11

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, using an electro-deposition coating composition prepared by dispersing, in an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.), aluminum nitride with an average particle diameter of 1.5 μm in a concentration of 3% by weight of the resin and then diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a DC voltage of 150 V was applied for 3 minutes under conditions of pH 8.5 and a bath temperature of 25° C., setting the substrate as the anode and a stainless steel sheet as the cathode. Thus an insulating film 4 of 15 μm in thickness and 25% by weight in deposition quantity of the powder was formed on the copper circuit pattern.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an acrylic melamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 10 parts by weight of an alumina powder with an average particle diameter of 1.0 μm whose particle surfaces were coated with nickel in a thickness of 0.1 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film 3 of 17 μm in thickness and 30% by weight in deposition quantity of the powder was formed on the whole surface of the insulating film 4 under the same conditions as those for the formation of the insulating film 4.

Then, using the same electro-deposition coating composition as used for the insulating film 4, an insulating film 5 of 15 μm thick was further formed on the whole surface of the conductive film 3 under the same conditions as those for the formation of the insulating film 4.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis and resistance to flame), insulation resistance, specific volume resistance, hardness (pencil) and resistance to scratching (eraser) of the resulting circuit substrate were evaluated or measured. Results obtained are shown in Tables 4 to 6 below.

The resulting insulating film and conductive film were dense and well adhered to adjoining films, having satisfactory resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching.

The electromagnetic wave shielding effect of the circuit substrate was also measured by the transmission line method after it was set in an apparatus. As a result, the electromagnetic wave shielding effect was as good as that in Example 1.

The cross section of this circuit substrate was also observed in the same manner as in Example 1 to confirm that all the films were formed in uniform thicknesses.

TABLE 4

Results of Evaluation on Physical Properties of Film					
Adhesion	Resistance to acids	Resistance to alkalis	Resistance to flame	Hardness	<1>
Example 11:*					
Adhesion rate: 100/100 Completely adhered.	No changes in insulating film.	No changes in insulating film.	Cleared 94V-0	4 H	>700
Comparative Example 1:					
See	See	See	See	2 H	<100*

TABLE 4-continued

Results of Evaluation on Physical Properties of Film					
Adhesion	Resistance to acids	Resistance to alkalis	Resistance to flame	Hardness	<1>
Table 1.	Table 1.	Table 1.	Table 1.	to H	

<1>: Resistance to scratching
*times
Notes:
Tests on the items in the above table were carried out by the following methods:
(1) Adhesion: JIS D0202
(2) Resistance to acid: Immersion treatment with 10 Vol. % H_2SO_4 at room temperature for 20 minutes.
(3) Resistance to alkali: Immersion treatment with 5 wt. % NaOH at room temperature for 30 minutes.
(4) Resistance to flame: UL94 Test Method
(5) Hardness: JIS K5400
(6) Resistance to scratching: The times required until the substrate was exposed when the insulating film was rubbed with an eraser.

TABLE 5

	Insulation Resistance of Film	
	Initial value	After 96 hour moisture absorption treatment
Example 1:	$1.3 \times 10^{13}\ \Omega \cdot cm$	$1.2 \times 10^{13}\ \Omega \cdot cm$

Notes:
The insulation resistance in the above table was measured according to JIS Z3197; comb electrode G-10; substrate moisture absorption treatment: at 55° C., 98% RH, DC 500 V for 1 minute. The resistivity was measured using a insulation resistance measuring device HP4329A, manufactured by YHP Co.

TABLE 6

	Specific Volume Resistance of Film	
	Initial value	After 96 hour moisture absorption treatment
Example 1:	$1.0 \times 10^{13}\ \Omega \cdot cm$	$1.3 \times 10^{13}\ \Omega \cdot cm$

Notes:
The above specific resistivity was measured according to JIS C6481.

EXAMPLE 12

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, an insulating film **4** was formed thereon in the same manner as in Example 11 except that 3% by weight of the aluminum nitride powder used for the insulating film **4** in Example 11 was replaced with 5% by weight of an alumina powder with an average particle diameter of 1.0 μm.

Next, in an electo-deposition coating composition prepared by dispersing, in 100 parts by weight of an acrylic malamine resin (trade name: Honey Bright CL-1; produced by Honey Chemical Co.) separately made ready for use, 15 parts by weight of an alumina powder with an average particle diameter of 1.0 μm whose particle surfaces were coated with nickel in a thickness of 0.3 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 15 μm in thickness and 27% by weight in deposition quantity of the powder was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 13

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, using an electro-deposition coating composition prepared by dispersing, in an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.), silicon carbide with an average particle diameter of 2.0 μm in a concentration of 1% by weight of the resin and then diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a DC voltage of 150 V was applied for 3 minutes under conditions of pH 8.5 and a bath temperature of 25° C., setting the substrate as the anode and a stainless steel sheet as the cathode. Thus an insulating film **4** of the 15 μm in thickness and 25% by weight in deposition quantity of the powder was formed on the copper circuit pattern.

Next, in an electro-deposition coating composition prepared by dispersing, in 100 parts by weight of an alkyd resin (trade name: TF121; produced by Shinto Paint Co., Ltd.) separately made ready for use, 10 parts by weight of an alumina powder with an average particle diameter of 1.0 82 m whose particle surfaces were coated with copper in a thickness of 0.2 μm and further diluting the dispersion with desalted water to 15% by weight as concentration of a mixture of the resin and the powder, a conductive film **3** of 17 μm in thickness and 30% by weight in deposition quantity of the powder was formed on the whole surface of the insulating film **4** under the same conditions as those for the formation of the insulating film **4**.

Then, using the same electro-deposition coating composition as used for the insulating film **4**, an insulating film **5** of 15 μm thick was further formed on the whole surface of the conductive film **3** under the same conditions as those for the formation of the insulating film **4**.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 14

On glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, an insulating film **4** was formed thereon in the same manner as in Example 11 except that 3% by weight of the aluminum nitride powder used for the insulating film **4** in Example 11 was replaced with 1.5% by weight of an alumina powder with an average particle diameter of 5.6 μm.

Next, the same conductive film **3** as in Example 11 was formed in the same manner as in Example 11.

Finally, the resulting substrate was washed with water and then put the substrate in an oven of 97° C.±1° C. to carry out heat treatment for 150 minutes. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching) and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thickness.

EXAMPLE 15

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern and an insulating film **4** were formed in the same manner as in Example 1.

Thereafter, the same conductive film **3** as in Eaxample 5 was formed in the same manner as in Example 5.

Then, the same insulating film **5** as in Example 11 was formed in the same manner as in Example 11, and finally the coatings were cured in the same manner as in Example 11. A circuit substrate of the present invention was thus obtained.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 16

A circuit substrate of the present invention was prepared in the same manner as in Example 12 except that 10 parts by weight of the nickel-coated alumina powder used for the conductive film **3** in Example 12 was replaced with 5 parts by weight of a silver powder with an average particle diameter of 0.02 μm.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thicknesses.

EXAMPLE 17

On a glass epoxy resin substrate of 0.6 mm thick, a copper circuit pattern was formed in the same manner as in Example 1.

Thereafter, an insulating film **4**, a conductive film **3** and an insulating film **5** were formed thereon in the same manner as in Example 11, Example 8 and Example 11, respectively.

Physical properties (adhesion, resistance to acids, resistance to alkalis, resistance to flame, hardness, and resistance to scratching), insulation resistance, specific volume resistance and electromagnetic wave shielding effect of the resulting circuit substrate were evaluated or measured in the same manner as in Example 11. As a result, the same good results as in Example 11 were obtained.

The cross section of this circuit substrate was also observed in the same manner as in Example 11 to confirm that all the films were formed in uniform thicknesses.

I claim:

1. A circuit substrate comprising a substrate, a conductive circuit pattern provided on said substrate, a first insulating film that covers said conductive circuit pattern, and a conductive film that covers said first insulating film, wherein both said first insulating film and said conductive film are formed by electro-depositing coating.

2. A circuit substrate according to claim **1**, wherein said conductive film is covered with a second insulating film.

3. A circuit substrate according to claim **2**, wherein said second insulating film is formed by electro-deposition coating.

4. A circuit substrate according to claim **1**, wherein said first insulating film comprises a ceramic powder.

5. A circuit substrate according to claim **3**, wherein said second insulating film comprises a ceramic powder.

6. A circuit substrate according to claim **1**, wherein said conductive film comprises a conductive powder.

7. A circuit substrate according to claim **6**, wherein said conductive powder comprises a material selected from the group consisting of a metallized ceramic powder and a metallized natural mica powder.

8. A circuit substrate according to claim **6**, wherein said conductive powder comprises a mixture selected from the group consisting of a metallized ceramic powder and a metallized natural mica powder and a material selected from the group consisting of a metallized resin powder and a metal powder.

9. A circuit substrate according to claim **1** wherein a second insulating film is provided to cover said conductive film, and said first insulating film, said conductive film and said second insulating film are all formed by electro-deposition coating.

10. A process for producing a circuit substrate, comprising a first step of forming on a substrate a circuit pattern comprising a conductor wire, a second step of porviding a first insulating film to cover the circuit

pattern, and a third step of providing a conductive film to cover the first insulating film, wherein said second step and said third step each comprises an electro-deposition coating, said electro-deposition coating being carried out by immersing said substrate in an electro-deposition coating composition, and setting the conductor wire as an electrode.

11. A process for producing a circuit substrate according to claim **10**, wherein the step of forming said conductive film is followed by a fourth step of providing a second insulating film to cover the conductive film.

12. A process for producing a circuit substrate according to claim **11**, wherein said fourth step comprises an elector-deposition coating.

13. A process for producing a circuit substrate according to claim **10**, wherein said second step comprises said electro-deposition coating, and wherein a ceramic powder is incorporated into said elecro-deposition coating composition to form the first insulating film.

14. A process for producing a circuit substrate according to claim **10**, wherein third step comprises said electro-deposition coating and wherein a conductive powder is incorporated into said electro-deposition coating composition to form the conductive film.

15. A process for producing a circuit substrate according to claim **14**, wherein said conductive powder comprises a material selected from the group consisting of a metallized ceramic powder and a metallized natural mica powder.

16. A process for producing a circuit substrate according to claim **14**, wherein said conductive powder comprises a mixture selected from the group consisting of a metallized ceramic powder and a metallized natural mica powder and a material selected from the group consisting of metallized resin powder and a metal powder.

17. A process for producing a circuit substrate according to cliam **10**, wherein said fourth step comprises said electro-depositing coating, and wherein a ceramic powder is incorporated into said electro-deposition coating composition to form the second insulating film.

18. A process for producing a circuit substrate according to claim **10**, wherein a fourth step is provided to form a second insulating film that covers the conductive film, and wherein said second step, said third step and said fourth step each comprises an electro-deposition.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,158,657

DATED : October 27, 1992

INVENTOR(S) : SUSUMU KADOKURA

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

COLUMN 1

Line 35, "a this" should read --a circuit. This--.
Line 55, "can" should read --that can--.

COLUMN 4

Line 48, "deposition" (second occurrence) should be deleted.

COLUMN 15

Line 47, "electo-deposition" should read
--electro-deposition--.

COLUMN 16

Line 41, "1.0 82 m" should read --1.0 μm--.

COLUMN 17

Line 15, "5.6" should read --5.0--.

COLUMN 18

Line 60, "1 wherein" should read --1, wherein--.
Line 68, "porviding" should read --providing--.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,158,657

DATED : October 27, 1992

INVENTOR(S) : SUSUMU KADOKURA

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

COLUMN 19

Line 16, "elector-deposition" should read --electro-deposition--.
Line 20, "elecro-deposition" should read --electro-deposition--.
Line 24, "wherein third" should read --wherein said third--.

Signed and Sealed this

Thirtieth Day of November, 1993

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

EXHIBIT C

The Judicial Decision from the District of Delaware

LG Display Co., LTD., vs AU Optronics Corporation

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU OPTRONICS CORPORATION AMERICA; CHI MEI OPTOELECTRONICS CORPORATION; and CHI MEI OPTOELECTRONICS USA, INC., Defendants.	:	Civil Action No. 06-726-JJF
AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG DISPLAY AMERICA, INC.,	:	Civil Action No. 07-357-JJF

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Attorneys for AU Optronics Corporation and AU Optronics Corporation America.

O P I N I O N

February 16 , 2010

Wilmington, Delaware.

Farnan, District Judge.

These proceedings involve three related patent infringement cases involving 23 patents. In the first-filed action, LG Display Co., Ltd. ("LGD") alleges infringement of nine asserted patents (collectively, the "LGD Patents") against AU Optronics Corporation ("AUO") and Chi Mei Optoelectronics Corporation ("CMO"). AUO and CMO have also brought separate actions against LGD and LG Display America, Inc. ("LGD America") alleging infringement of eight patents asserted by AUO and six patents asserted by CMO.

Proceedings with respect to CMO have been stayed. The Court required the parties to reduce the number of patents and claims asserted to a total of four patents and seven claims per side.[1] As a result, LGD identified the following patents and claims for trial against AUO: U.S. Patent No. 5,019,002 (claim 8); U.S. Patent No. 5,825,449 (claims 10 and 11); U.S. Patent No. 6,815,321 (claims 7, 17 and 19) and U.S. Patent No. 7,218,374 (claim 9). AUO identified the following four patents and claims for trial against LGD and LGD America: U.S. Patent No. 6,778,160

[1] The Court notes that, in contravention of the spirit of the Court's order reducing the number of claims to be tried in this case, the parties chose to assert several dependent claims. In the case of AUO's asserted patents, the assertion of numerous dependent claims has expanded the number of claims asserted from the seven that the Court ordered as a means of streamlining this case to a total of 16 claims. Similarly, LGD's selection has resulted in a total of 11 claims being presented to the Court.

(claims 1 and 3); U.S. Patent No. 6,689,629 (claims 7 and 16); U.S. Patent No. 7,125,157 (claim 1) and U.S. Patent No. 7,090,506 (claims 7 and 17).

A bench trial was held on the claims brought by the parties and was bifurcated into two phases. The first phase of trial was held from June 2-8, 2009, and addressed AUO's infringement claims against LGD. The second phase of trial was held from June 16-22, 2009, and addressed LGD's infringement claims against AUO.

The claims and counterclaims for infringement and declaratory judgment in this case arise under the patent laws of the United States, Title 35, United States Code. Accordingly, the Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331, 1338(a), and 2201(a). Personal jurisdiction over the parties exists pursuant to 10 Del. C. § 3104, the Delaware long-arm statute. D.I. 1170 at 12. Likewise, venue in this district is appropriate under 28 U.S.C. §§ 1391(b), (c) and (d) and 1400. Neither jurisdiction nor venue is contested by the parties.

This Memorandum Opinion constitutes the Court's findings of fact and conclusions of law on the claims brought by the parties.

BACKGROUND

I. The Parties

LGD, formerly named LG Phillips LCD Co., Ltd., is a Korean corporation with a place of business in Korea. D.I. 1170 at Exh.

1, Stipulated Fact No. 1. LGD America is a California corporation with a place of business in San Jose, California. Id., Stipulated Fact No. 2. LGD and LGD America are collectively referred to as "LGD." Id., Stipulated Fact No. 3.

AU Optronics Corporation ("AUO") is a Taiwanese corporation with a place of business located in Taiwan. Id., Stipulated Fact No. 5. AU Optronics Corporation of America ("AUO America") is a California corporation with a place of business located in Santa Clara, California. Id. at Stipulated Fact No. 6. AUO Corp. and AUO America are collectively referred to as "AUO."

II. The Patents And The Technology Generally

The asserted patents relate to liquid crystal display ("LCD") products or methods of producing and assembling such products. Id., Stipulated Fact No. 13. An LCD is a flat panel display device that is used to generate images in a variety of products, including such devices as computer monitors, television screens, notebook computers and mobile phones. Id., Stipulated Fact No. 14.

DISCUSSION

I. Claim Construction

A. The Legal Principles of Claim Construction

Claim construction is a question of law. Markman v. Westview Instruments, Inc., 52 F.3d 967, 977-78 (Fed. Cir. 1995), aff'd, 517 U.S. 370, 388-90 (1996). When construing the claims

of a patent, a court considers the literal language of the claim, the patent specification and the prosecution history. Markman, 52 F.3d at 979. Of these sources, the specification is "always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term." Phillips v. AWH Corporation, 415 F.3d 1303, 1312-17 (Fed. Cir. 2005) (citing Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996)). However, "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" Liebel-Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 906 (Fed. Cir. 2004) (quoting Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1327 (Fed. Cir. 2002)).

A court may consider extrinsic evidence, including expert and inventor testimony, dictionaries, and learned treatises, in order to assist it in understanding the underlying technology, the meaning of terms to one skilled in the art and how the invention works. Phillips, 415 F.3d at 1318-19; Markman, 52 F.3d at 979-80. However, extrinsic evidence is considered less reliable and less useful in claim construction than the patent and its prosecution history. Phillips, 415 F.3d at 1318-19 (discussing "flaws" inherent in extrinsic evidence and noting

that extrinsic evidence "is unlikely to result in a reliable interpretation of a patent claim scope unless considered in the context of intrinsic evidence").

In addition to these fundamental claim construction principles, a court should also interpret the language in a claim by applying the ordinary and accustomed meaning of the words in the claim. Envirotech Corp. v. Al George, Inc., 730 F.2d 753, 759 (Fed. Cir. 1984). If the patent inventor clearly supplies a different meaning, however, then the claim should be interpreted according to the meaning supplied by the inventor. Markman, 52 F.3d at 980 (noting that patentee is free to be his own lexicographer, but emphasizing that any special definitions given to words must be clearly set forth in patent). If possible, claims should be construed to uphold validity. In re Yamamoto, 740 F.2d 1569, 1571 (Fed. Cir. 1984).

B. AUO's Patents

The parties dispute a number of claim terms from the asserted patents. The Court has selected for construction those terms that appear most pertinent to the disputes and trial positions argued by the parties in the post-trial briefing.[2]

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[2] The Court notes that claim construction in this case has been a "moving target." The parties have altered definitions that were advanced and have offered different terms for construction at different times during this litigation. In addition, the post-trial briefing between the parties is inconsistent as to which terms are genuinely in dispute. For example, disputed terms are identified in the post-trial briefing

1. U.S. Patent No. 6,778,160 (the "'160 patent")

AUO asserts claims 1 and 3 of the '160 patent. Claim 3 is a dependent claim that stems from claim 2. Accordingly, the relevant claims of the '160 patent are provided below, in full:

> 1. A liquid crystal display, comprising: an input logic for inputting a video signal from a host; a storage for storing the previous brightness level of the video signal input through said input logic; a determinator for determining an output brightness level based on the previous brightness level stored in said storage and the next brightness level of the next video signal input to said input logic so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level; and a driver for driving an image displaying liquid crystal cell based on said output brightness level determined by said determination logic.
>
> 2. The liquid crystal display according to claim 1, wherein said determinator comprising a table for storing a brightness level determined by the characteristic of a liquid crystal cell according to a relation between the previous brightness level and the next brightness level, and determining the output brightness level by modifying said next brightness level based on the brightness level read from said table.
>
> 3. The liquid crystal display according to claim 2, wherein: said video signal input through said input logic comprises a plurality of color signals; and said table in said determinator is provided for each of said color signals.

---

in claim construction sections, and later, additional terms appear to be added for construction in the infringement sections of the briefs. The parties' inability to agree on the central terms for dispute and succinctly state their positions in a parallel format has enhanced the difficulty of this case.

The parties agree that one of ordinary skill in the art with respect to the '160 patent at the time of its filing is a person with at least a bachelor's degree in electrical engineering and several years experience working with liquid crystal displays, or the equivalent combined education and work experience. D.I. 1388 at ¶ 389; D.I. 1383 at ¶ 122.

a. **a storage for storing the previous brightness level**

The parties agree that the term "storage" refers to a "memory." D.I. 1388 at ¶ 390; D.I. 1387 at 23. The parties dispute the meaning of "brightness level." LGD contends that "brightness level" means a "gray scale value or luminance value" and proposes that the phrase "a storage for storing the previous brightness level" be defined as "memory that temporarily holds the brightness level of the video signal received from the host through input logic for the previous time increment." Id. at ¶ 394. AUO contends that the term "brightness level means "a level of intensity of light," and therefore, the term "a storage for storing the previous brightness level" should be defined as "memory for storing a previous level of light intensity of a video signal input through input logic." D.I. 376 at Exh. M-2.

After reviewing the claim language in light of the specification, the Court concludes that "brightness level" means a "level of intensity of light." This construction is consistent with the specification which explains that brightness "should be

considered in terms of the quantity of light." AUO-5 ('160 patent) at col. 8, ll. 32-35. While it is true that the specification suggests that a "brightness level can be represented as a target brightness by a gray scale," the Court does not read the specification to limit the representation of a video signal's brightness level to "gray scale values." Id. at col. 3, l. 67.

b. **determinator for determining an output brightness level**

AUO contends that this term means "logic, such as a circuitry, for determining an output brightness value. D.I. 376 at Exh. M—3. LGD contends that this phrase should be defined as "circuit or logic that determines the output brightness level by applying an offset to the next brightness level that is predetermined based on a difference in quantity of light between the actual and ideal response characteristics of the liquid crystal cell. D.I. 1388 at ¶ 395.

The parties are in agreement that this term refers to logic or circuitry. Their disagreement arises from LGD's additional limitations which purport to limit the manner in which the determinator determines the output brightness. The Court has reviewed the claim language in light of the specification, and concludes that such additional limitations are not required. Accordingly, the Court adopts AUO's proposed construction of the phrase "determinator for determining an output brightness level"

as "logic, such as a circuitry, for determining an output brightness value."

c. **so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level**

1. **substantially equal**

AUO contends that the term "substantially equal" should be construed in accordance with its plain meaning such that "substantially equal" means "a level that is not completely the same but can be accepted as a substantially equal level." LGD contends that the phrase "substantially equal" is indefinite, or in the alternative, should be construed as "a level which is not completely the same but can be accepted as a substantially equivalent level, and includes a level which is closer to an ideal quantity of light than [sic] no preventive measures are taken." D.I. 1388 at 101.

The Court concludes that the term "substantially equal" is not indefinite and should be defined as AUO proposes. This construction is consistent with the plain meaning of the term and the specification, which explains that the "representation 'substantially equal level' refers to a level which is not completely the same but can be accepted as a substantially equivalent level." '160 patent, col. 4, ll. 56-58; col. 9, ll. 19-23 (referring to Fig. 6 and the desire to obtain a "quantity of light (S") . . . which is approximately the same as the

quantity of light (S) . . . [from an LC with] ideal response characteristic[s] (S".S)"; col. 8, ll. 45-47 (quantity of light is "almost the same as" that of an ideal LC). In the Court's view, LGD's construction, improperly imports limitations from the preferred embodiment into the claims.

2. **time integration quantity of a brightness change/ideal quantity of light in a stationary state**

AUO contends that the term "time integration quantity of a brightness change" means "a quantity of light equal to the actual brightness level output through a liquid crystal, summed over the rise and fall response time of the liquid crystal." D.I. 376 at M-13. According to AUO, the plain meaning of "integration, in this context, is summing a change value (here, brightness level) over a period of time (here, the response time of the crystal)." Id. AUO also contends that the term "ideal quantity of light in a stationary state" refers to the "quantity of light emitted by a pixel during one time increment in which the pixel is in a non-changing state." Id.

LGD contends that these terms are indefinite. In the alternative, LGD appears to conflate the terms and offer a combined definition as follows: "quantity of light based on the actual response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness

level before and after the next time increment." D.I. 376 at Exh. M-13.

After reviewing the claim language in light of the specification, the Court concludes that the terms are not indefinite and will adopt AUO's proposed construction of these terms. The specification explains that the "[q]uantity of light can be considered as a time integration quantity of a brightness change." '160 patent, col. 4, ll. 53-57. The specification further explains that "brightness of a pixel to the human eye . . . should be considered in terms of the quantity of light, that is brightness change integrated with respect to time." Id. col. 8, ll. 30-34. In the Court's view, this supports AUO's position that the "time integration quantity of a brightness change" is the quantity of light that is emitted due to the change in brightness. LGD's proposed construction adds limitations that are not supported by the specification.

Likewise, the Court will adopt AUO's proposed construction of the term "ideal quantity of light in a stationary state." The specification teaches, by way of example, that an ideal quantity of light is that quantity of light output by an ideal LC over one time increment. Id., col. 4, ll. 42-47, Fig. 4. However, an ideal LC does not exist, id. at col. 8, ll. 63-65, and the specification's example teaches that the ideal quantity of light from a conventional LC is that quantity of light emitted from the

LC during one time increment when the brightness is constant, meaning the image is stationary. Id. col. 8, ll. 37-39 (when the particular pixel or LC is driven at a target brightness for an entire time increment, the pixel or LC may be described as being in a non-changing or "stationary state"). As with LGD's previous construction, its proposed construction of "ideal quantity of light in a stationary state" adds limitations that are not supported by the specification.

2. U.S. Patent No. 6,689,629 (the "'629 patent")

AUO asserts claims 7 and 16 against LGD. Claim 7 is a dependent claim which depends upon claim 4. Claim 4, in turn depends upon claim 2, and claim 2, depends on claim 1.

Similarly, Claim 16 is a dependent claim which depends on claim 13. Claim 13 in turn depends on claim 11. Claim 11 depends on claim 10, and claim 10 depends on independent claim 9.

Accordingly, the relevant claims of the '629 patent are provided below in full:

1. An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate; a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patterns are not in contact with any of the wiring.

2. The array substrate for display according to claim 1 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

4. The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

7. The array substrate for display according to claim 4 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

* * *

9. A method for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array formed on the insulating substrate, each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

> 10. The method for forming an array substrate for display according to claim 9 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.
>
> 11. The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring materials is selected from the group consisting of aluminum and aluminum alloys.
>
> 13. The method for forming an array substrate for display according to claim 11 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and allays thereof.
>
> 16. The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

The parties agree that one of ordinary skill in the art with respect to the '629 patent would be a person with at least a Bachelor's degree in chemical or electrical engineering, chemistry, or physics with 2 or more years experience working with liquid crystal display fabrication processing, or the equivalent combined education and work experience. D.I. 1383 at ¶ 299; D.I. 1388 at ¶ 132; Tr. 118:3-16 (Silzars).

a. **dummy conductive patterns**

LGD contends that the term "dummy conductive patterns" means "portions of the layer that do not receive or convey voltages or signals." D.I. 1388 at ¶ 133. Refining this construction further, LGD contends that this construction requires that the dummy patterns do not conduct or convey signals "at least during

testing or operation of the display." D.I. 1387 at 6. In this regard, LGD further contends that dummy patterns are structures that are put into the design of a product to aid in the manufacturing of the product, but do not have a function during the operation of the display. D.I. 1388 at ¶ 136-138. LGD contends that AUO has changed its position on the construction of this term, and that this change in position demonstrates that AUO's currently proposed definition should not be accepted.

AUO contends that the term "dummy conductive patterns" refers to "one or more metal patterns in the specified region that are not in contact with any of the wiring." D.I. 1384 at 24. AUO acknowledges that this construction is different than its previously proposed construction which was "a metal pattern that does not conduct signals or current used in the operation of the display." Id. at 25. However, AUO contends that its previous construction was too restrictive. In this regard, AUO contends that the wiring recited in the claims connects the connection pads to the transistors in the TFT array. AUO contends that dummy patterns are not needed for the operation of the transistors of the TFT array, and therefore, they "are not in contact with any of the wiring" that is "in communication with at least one of the transistors in the TFT array." Id., citing '629 patent, col. 8, ll. 14-19. However, AUO maintains that there is nothing in the intrinsic evidence that precludes the dummy

conductive patterns from performing some function, such as conducting a voltage or signal used in the operation of a display, so long as they are not in contact with the TFT wiring. AUO points out that even under its prior construction, nothing required dummy conductive patterns to be unable to receive any voltages or signals, and that the dummy conductive patterns could still be connected to a ground or voltage supply. D.I. 1384 at 24-26.

As the Federal Circuit has recognized, the Court's task in claim construction is not to decide which of the adversaries is correct, but to independently determine the meaning of disputed claims. Exxon Chem. Patents, Inc. v. Lubrizol Corp., 64 F.3d 1553, 1556 (Fed. Cir. 1995). For this reason, the Court does not take AUO's change in its claim construction position to be indicative of the merits of its current argument.

Reviewing the disputed term in light of the claim language and specification, the Court concludes that the term "dummy conductive patterns" is properly construed to mean "conductive patterns in the specified region that are not in contact with any of the wiring." The claim terms expressly state that the dummy conductive patterns must comprise "at least about 30% of the area" and "are not in contact with any of the wiring." '629 patent, col. 8, ll. 13-19, 57-63. The Court does not read the claims or the specification from precluding the dummy conductive

patterns from performing some function, so long as that they are not in contact with the TFT wiring. Accordingly, the Court concludes that LGD's claim construction and AUO's prior claim construction were both too restrictive, and that "dummy conducive patterns" are "conductive patterns in the specified region that are not in contact with any of the wiring."

b. **area**

LGD contends that the term "area" is indefinite because one of ordinary skill in the art would be unable to unambiguously discern the boundaries of the asserted claims. D.I. 1388 at ¶ 168-170. In this regard, LGD contends that there is no disclosure on how the 30% of the area should be calculated. Alternatively, LGD contends that the term "area" refers to "material deposited and patterned on a substrate, such as glass, that covers part of the array substrate surface." Id. at ¶ 171.

In response, AUO contends that "area" should be construed according to its ordinary meaning as a "specified region." D.I. 1384 at 23-24. Turning to the context of the claims more specifically, AUO contends that "area" refers to a region of the array substrate, specifically a region containing the dummy conductive patterns.

After reviewing the claim language in light of the specification, the Court concludes that the term "area" is not indefinite and should be construed according to its plain meaning

as a "specified region." In the Court's view, this is consistent with the specification which explains that the substrate coverage "of the dummy conductive patterns themselves [is] 30% or more on an area of a specified surface." '629 patent, col. 5, ll. 55-61. Similarly, the specification explains that "dummy conductive patterns are formed on an area of a specified region where the dummy conductive patterns are formed." Id., col. 6, ll. 1-6. Thus, the Court concludes that an "area" is "a specified region," more specifically, the region where dummy conductive patterns are located.

c. **a plurality of wiring / each wiring**

LGD contends that the term "each wiring" is indefinite, because it is unclear as to which wiring the term "each wiring" is referring from the plurality of wiring. LGD contends that "[t]o the extent the term 'each wiring' can be construed, the term 'a plurality of wiring arranged on the insulating substrate' should be construed to mean 'portions of the layer that convey voltages or signals from the connection pads to the thin-film transistors in the pixel array." D.I. 1407 at ¶ 56.

AUO contends that the these terms should be construed in accordance with their plain meaning in the context of the claim element in which they are used. Thus, AUO contends that "a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at

least one of the transistors in the thin film array" means "each individual wiring in a plurality of wirings," with the plurality of wirings being a plurality of electrical conductors. D.I. 1383 at ¶ 347. In this regard, AUO points out that the specification explains "this connection of 'each wiring' [by] describing 'wirings such as scan lines and signal lines connected with' the electrodes of the transistors." D.I. 1383 at ¶ 344 (citing '629 patent, col. 1, ll. 17-19, col. 4, ll. 49-51, Fig. 2).

The Court concludes that the terms "each wiring" and "plurality of wiring" as recited in the claim element "a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array" are not indefinite. The Court further concludes that these terms should be construed according to their plain meaning in the context of the patent, such that a plurality of wiring is a plurality of electrical conductors and "each wiring" is "each individual wiring in a plurality of wiring." '629 patent, col. 8, l. 6, 11, col. 8, ll. 54-55; Tr. 139:10-140:1 (Silzars).

d. the upper layer wiring material does not become insoluble in an acid or alkaline etchant

Although not identified in the parties' claim construction charts, it is apparent from their briefing that disputes exist regarding the proper construction and/or application of this

phrase. Specifically, AUO contends that the solubility issue in claim 7 and 16 must be evaluated in the context of a two layer structure - that is a wiring structure having a lower and upper layer of wiring. D.I. 1384 at 26-27.

LGD contends that AUO's interpretation of this claim improperly imports into the claims limitations contained in the specification. In particular, LGD contends that claim 7 and 16 do not refer to the passivity problem described in the specification and contain no limitation that the insolubility of the upper layer is during the etching process. D.I. 1406 at 17-18.

After reviewing the claim language in light of the specification, the Court concludes that the limitation of claim 7 and 16 must be read in the context of a two layer structure. Fuji Photo Film Co., Ltd. v. International Trade Com'n, 386 F.3d 1095 (Fed. Cir. 2004) ("Claims must be read in the context of the specification of which they are a part.") This reading is consistent with claims 7 and 16 which are dependent upon claims 2 and 10. Claims 2 and 10 expressly contemplate two layer wiring, and therefore, the claim language makes it evident, that it is within the context of two-layer wiring that solubility must be evaluated. In the Court's view, this is also consistent with the purpose of the invention which is to prevent the upper layer from becoming insoluble during etching of the two-layer wiring. Tr.

870:18-871:8, 872:9-13, 873:7-23 (Rubloff); Tr. 1388:20-1391:2 (Silzars). In this regard, the Court agrees with the testimony of Dr. Silzars that whether material would become insoluble if dropped by itself in a vat of etchant is irrelevant to the context of the claimed invention. Tr. 1388:20-24 (Silzars). Accordingly, the Court does not view its construction as importing limitations from the specification as LGD contends, but as an attempt to view the claim in its proper context.

3. U.S. Patent No. 7,125,157 (the "'157 patent")

AUO asserts independent claim 1 of the '157 patent. In full, claim 1 provides:

> 1. A backlight unit for a liquid crystal display, comprising: a frame; a first supporting portion, disposed on the frame; a second supporting portion, further disposed on the frame; and a film comprising a first constraining portion and a second constraining portion, positioned on the frame by the first supporting portion and the second supporting portion passing through the first constraining portion and the second constraining portion, respectively; when the frame is disposed in a first position, the first supporting portion partially contacts an inner wall of the first constraining portion for positioning the film, and the second supporting portion does not contact the second constraining portion; and when the frame is disposed in a second position, the second supporting portion partially contacts an inner wall of the second constraining portion for positioning the film and the first supporting portion does not contact the first constraining portion.

The parties agree that one of ordinary skill in the art with respect to the '157 patent at the time of its filing "would be a person with a bachelors degree in mechanical engineering or

physics and several years of experience working with aspects of the backlight modules for liquid crystal displays or the equivalent combined education and work experience." D.I. 1383 at ¶ 497; D.I. 1388 at ¶ 678; Tr. 207:24-208:12 (Silzars).

a. **supporting portion**

LGD contends that a "supporting portion" should be construed as a projection from the frame. D.I. 376 at Exh. Q-1. AUO contends that the "supporting portion" should not be limited to a projection, which may be defined to have a specified shape. Id.

The Court adopts AUO's construction of "supporting portion" as "any structure protruding from the frame, (including but not limited to a cylinder or a cuboid) intended to support the optical film." '157 patent, col. 2, ll. 61-62, col. 3, ll. 4-12, col. 4, ll. 17-24, Fig. 2A and 2B; col. 6, ll. 4-8, 31-42 Fig. 3A and 3B; Fig. 3C, col. 7, ll. 39-45, Fig. 4A-4D.

b. **constraining portion**

AUO contends that a constraining portion is "any formation on or in the optical film (including but not limited to a hole or groove) intended to restrict the movement range of the film." D.I. 376 at Exh. Q-2. LGD contends that this term should be defined as "a passage through the film that has a gap in the gravity acting direction after receiving a supporting portion." Id.