wirings;	Abstract, Figs 1, 5-6.	
Forming pixel electrodes, and	Tomoyuki discloses pixel electrodes 12. See, e.g., Tomoyuki, Figs 1, 5-6.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Tomoyuki discloses dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figures 1, 5-6. Further, the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel electrode. See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6. The dummy film 5 and 5a would comprise at least 30% of the area or a specified region.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium,

from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

APPENDIX CC20

U.S. PATENT NO. 6,689,629 - TOMOYUKI IN VIEW OF KUBOTA

Japanese Pub. No. 2000-098909 to Tomoyuki in view of U.S. Patent No. 6,157,430 to Kubota renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE - TOMOYUKI '909	PRIOR ART DISCLOSURE – KUBOTA
An array substrate for display, comprising:	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
a layer of an insulating substrate, having an area;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
a thin film transistor array formed on the insulating substrate;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Tomoyuki discloses TFT array substrate including wiring, drain lines DLs and gate lines GLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Tomoyuki discloses that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
pixel electrodes, and	Tomoyuki discloses pixel electrodes 12. See, e.g., Tomoyuki, Figs 1, 5-6.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in	Tomoyuki discloses dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figures 1, 5-6. Further, the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel	

contact with any of the wiring.	electrode. See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6. The dummy film 5 and 5a would comprise at least 30% of the area or a specified region.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium,		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of

tantalum, titanium and alloys thereof.		chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 9		
A meted for forming an array substrate for display, comprising:	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	

forming a layer of an insulating substrate, having an area;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
forming a thin film transistor array formed on the insulating substrate;	Tomoyuki discloses a TFT array substrate 11 including display pixels. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Tomoyuki discloses TFT array substrate including wiring, drain lines DLs and gate lines GLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Tomoyuki discloses that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6.	
Forming pixel electrodes, and	Tomoyuki discloses pixel electrodes 12. See, e.g., Tomoyuki, Figs 1, 5-6.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Tomoyuki discloses dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs. See, e.g., Tomoyuki, Abstract, Figures 1, 5-6. Further, the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel electrode. See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6. The dummy film 5 and 5a would comprise at least 30% of the area or a specified region.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g.,

		Kubota, col. 4, ll. 39-55.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

APPENDIX CC21

U.S. PATENT NO. 6, 689, 629 - ZHANG

U.S. Patent No. 5,995,189 to Zhang anticipates Claims 1-5, 7-13, and 15-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – ZHANG
An array substrate for display, comprising:	Zhang discloses a liquid crystal display device. See, e.g., Zhang, Title, Figs. 1 and 16-17.
a layer of an insulating substrate, having an area;	Zhang discloses a substrate 1 made of glass or quartz, including an area. See, e.g., Zhang, 1:35-36, Figs. 1 and 16-17.
a thin film transistor array formed on the insulating substrate;	Zhang discloses scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines. See, e.g., Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17.
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Zhang discloses scan lines 2 and signal lines 3 and are connected to the TFTs. See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17.
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Zhang discloses that the signal lines 2 and scan lines 3 also connect to extension terminals 6. See, e.g., Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17.
pixel electrodes, and	Zhang discloses a pixel section 12. See, e.g., Zhang, Figs. 1 and 16-17.
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Zhang discloses dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals. See, e.g., Zhang, Figs. 4, 8 and 16. Further, the dummy wirings are not in contact with the wiring. Zhang also discloses that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, 10:7-17. Thus, the dummy patterns would comprise at least 30% of the area.

CLAIM 2	
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33.
CLAIM 3	
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33.
CLAIM 4	
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33.
CLAIM 5	
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33.
CLAIM 7	
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. The upper layer of titanium would inherently meet this limitation. See, e.g., Zhang, 9:29-33.
CLAIM 8	
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. The upper layer of titanium would inherently meet this limitation. See, e.g., Zhang, 9:29-33.
CLAIM 9	
A meted for forming an array substrate for display, comprising:	Zhang discloses a liquid crystal display device. See, e.g., Zhang, Title, Figs. 1 and 16-17.
forming a layer of an insulating substrate, having an area;	Zhang discloses a substrate 1 made of glass or quartz, including an area. See, e.g., Zhang, 1:35-36, Figs. 1 and 16-17.
forming a thin film transistor array formed on the insulating substrate;	Zhang discloses scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix

	with TFTs and pixel electrodes at the crossover points of the scan and signal lines. See, e.g., Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17.
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Zhang discloses scan lines 2 and signal lines 3 and are connected to the TFTs. See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17.
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Zhang discloses that the signal lines 2 and scan lines 3 also connect to extension terminals 6. See, e.g., Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17.
forming pixel electrodes, and	Zhang discloses a pixel section 12. See, e.g., Zhang, Figs. 1 and 16-17.
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Zhang discloses dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals. See, e.g., Zhang, Figs. 4, 8 and 16. Further, the dummy wirings are not in contact with the wiring. Zhang also discloses that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, 10:7-17. Thus, the dummy patterns would comprise at least 30% of the area.
CLAIM 10	
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33.
CLAIM 11	
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33.
CLAIM 12	
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium,	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33.

tantalum, titanium and alloys thereof.	
CLAIM 13	
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33.
CLAIM 15	
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. The upper layer of titanium would inherently meet this limitation. See, e.g., Zhang, 9:29-33.
CLAIM 16	
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Zhang discloses that the wiring can comprise of a three layer film of titanium, aluminum, and titanium. The upper layer of titanium would inherently meet this limitation. See, e.g., Zhang, 9:29-33.

APPENDIX CC22

U.S. PATENT NO. 6,689,629 - ZHANG IN VIEW OF SONG

U.S. Patent No. 5,995,189 to Zhang in view of U.S. Patent No. 6,163,356 to Song renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – ZHANG	PRIOR ART DISCLOSURE – SONG
An array substrate for display, comprising:	Zhang discloses a liquid crystal display device. See, e.g., Zhang, Title, Figs. 1 and 16-17.	
a layer of an insulating substrate, having an area;	Zhang discloses a substrate 1 made of glass or quartz, including an area. See, e.g., Zhang, 1:35-36, Figs. 1 and 16-17.	
a thin film transistor array formed on the insulating substrate;	Zhang discloses scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines. See, e.g., Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Zhang discloses scan lines 2 and signal lines 3 and are connected to the TFTs. See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Zhang discloses that the signal lines 2 and scan lines 3 also connect to extension terminals 6. See, e.g., Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17.	
pixel electrodes, and	Zhang discloses a pixel section 12. See, e.g., Zhang, Figs. 1 and 16-17.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns	Zhang discloses dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals. See, e.g.,	

situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Zhang, Figs. 4, 8 and 16. Further, the dummy wirings are not in contact with the wiring. Zhang also discloses that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, 10:7-17. Thus, the dummy patterns would comprise at least 30% of the area.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium,		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll.

tantalum, titanium and alloys thereof.		5-18.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Zhang discloses a liquid crystal display device. See, e.g., Zhang, Title, Figs. 1 and 16-17.	
forming a layer of an insulating substrate, having an area;	Zhang discloses a substrate 1 made of glass or quartz, including an area. See, e.g., Zhang, 1:35-36, Figs. 1 and 16-17.	
forming a thin film transistor array formed on the insulating substrate;	Zhang discloses scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines. See, e.g., Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17.	

each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Zhang discloses scan lines 2 and signal lines 3 and are connected to the TFTs. See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Zhang discloses that the signal lines 2 and scan lines 3 also connect to extension terminals 6. See, e.g., Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17.	
Forming pixel electrodes, and	Zhang discloses a pixel section 12. See, e.g., Zhang, Figs. 1 and 16-17.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Zhang discloses dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals. See, e.g., Zhang, Figs. 4, 8 and 16. Further, the dummy wirings are not in contact with the wiring. Zhang also discloses that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, 10:7-17. Thus, the dummy patterns would comprise at least 30% of the area.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 11		
The method for forming an array substrate for display according to claim 10		Song discloses a dual layer wiring including aluminum with chromium,

wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

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APPENDIX CC23

U.S. PATENT NO. 6, 689, 629 - ZHANG IN VIEW OF THE '629 APA

U.S. Patent No. 5,995,189 to Zhang in view of the '629 Admitted Prior Art renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – ZHANG	PRIOR ART DISCLOSURE – THE '629 APA
An array substrate for display, comprising:	Zhang discloses a liquid crystal display device. See, e.g., Zhang, Title, Figs. 1 and 16-17.	
a layer of an insulating substrate, having an area;	Zhang discloses a substrate 1 made of glass or quartz, including an area. See, e.g., Zhang, 1:35-36, Figs. 1 and 16-17.	
a thin film transistor array formed on the insulating substrate;	Zhang discloses scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines. See, e.g., Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Zhang discloses scan lines 2 and signal lines 3 and are connected to the TFTs. See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Zhang discloses that the signal lines 2 and scan lines 3 also connect to extension terminals 6. See, e.g., Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17.	
pixel electrodes, and	Zhang discloses a pixel section 12. See, e.g., Zhang, Figs. 1 and 16-17.	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns	Zhang discloses dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals. See, e.g.,	

situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Zhang, Figs. 4, 8 and 16. Further, the dummy wirings are not in contact with the wiring. Zhang also discloses that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, 10:7-17. Thus, the dummy patterns would comprise at least 30% of the area.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder

from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 9		
A meted for forming an array substrate for display, comprising:	Zhang discloses a liquid crystal display device. See, e.g., Zhang, Title, Figs. 1 and 16-17.	
forming a layer of an insulating substrate, having an area;	Zhang discloses a substrate 1 made of glass or quartz, including an area. See, e.g., Zhang, 1:35-36, Figs. 1 and 16-17.	
forming a thin film transistor array formed on the insulating substrate;	Zhang discloses scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points	

	of the scan and signal lines. See, e.g., Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Zhang discloses scan lines 2 and signal lines 3 and are connected to the TFTs. See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Zhang discloses that the signal lines 2 and scan lines 3 also connect to extension terminals 6. See, e.g., Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17.	
Forming pixel electrodes, and	Zhang discloses a pixel section 12. See, e.g., Zhang, Figs. 1 and 16-17.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Zhang discloses dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals. See, e.g., Zhang, Figs. 4, 8 and 16. Further, the dummy wirings are not in contact with the wiring. Zhang also discloses that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, 10:7-17. Thus, the dummy patterns would comprise at least 30% of the area.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 11		

The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

APPENDIX CC24

U.S. PATENT NO. 6, 689, 629 - ZHANG IN VIEW OF KUBOTA

U.S. Patent No. 5,995,189 to Zhang in view of U.S. Patent No. 6,157,430 to Kubota renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – ZHANG	PRIOR ART DISCLOSURE – KUBOTA
An array substrate for display, comprising:	Zhang discloses a liquid crystal display device. See, e.g., Zhang, Title, Figs. 1 and 16-17.	
a layer of an insulating substrate, having an area;	Zhang discloses a substrate 1 made of glass or quartz, including an area. See, e.g., Zhang, 1:35-36, Figs. 1 and 16-17.	
a thin film transistor array formed on the insulating substrate;	Zhang discloses scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines. See, e.g., Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17.	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Zhang discloses scan lines 2 and signal lines 3 and are connected to the TFTs. See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17.	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Zhang discloses that the signal lines 2 and scan lines 3 also connect to extension terminals 6. See, e.g., Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17.	
pixel electrodes, and	Zhang discloses a pixel section 12. See, e.g., Zhang, Figs. 1 and 16-17.	
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns	Zhang discloses dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals. See, e.g.,	

situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Zhang, Figs. 4, 8 and 16. Further, the dummy wirings are not in contact with the wiring. Zhang also discloses that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, 10:7-17. Thus, the dummy patterns would comprise at least 30% of the area.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 9		
A meted for forming an array substrate for display, comprising:	Zhang discloses a liquid crystal display device. See, e.g., Zhang, Title, Figs. 1 and 16-17.	
forming a layer of an insulating substrate, having an area;	Zhang discloses a substrate 1 made of glass or quartz, including an area. See, e.g., Zhang, 1:35-36, Figs. 1 and 16-17.	
forming a thin film transistor array formed on the insulating substrate;	Zhang discloses scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines. See, e.g., Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17.	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Zhang discloses scan lines 2 and signal lines 3 and are connected to the TFTs. See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17.	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	Zhang discloses that the signal lines 2 and scan lines 3 also connect to extension terminals 6. See, e.g., Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17.	
Forming pixel electrodes, and	Zhang discloses a pixel section 12. See, e.g., Zhang, Figs. 1 and 16-17.	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the	Zhang discloses dummy wirings 304 located in the sealing material formation region patterns which can be located	

insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	between the pixel section and the extension terminals. See, e.g., Zhang, Figs. 4, 8 and 16. Further, the dummy wirings are not in contact with the wiring. Zhang also discloses that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, 10:7-17. Thus, the dummy patterns would comprise at least 30% of the area.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium,		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium,

tantalum, titanium and alloys thereof.		tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

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APPENDIX CC25

U.S. PATENT NO. 6, 689, 629 - WATANABE '811

Japanese Publication No. H06-082811 to Watanabe '811 anticipates Claims 1-5, 7-13, and 15-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – Watanabe '811
An array substrate for display, comprising:	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].
a layer of an insulating substrate, having an area;	Watanabe '811 discloses a glass and thus insulating substrate upon which a TFT array of a liquid crystal display is formed. *See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038].
a thin film transistor array formed on the insulating substrate;	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Watanabe '811 discloses thin film transistors connected by signal and scanning lines 5 and 9. *See e.g.*, Watanabe '811, [0035].
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Watanabe '811 is an active matrix display that as discussed above includes scanning and signal lines that provide video-signal to thin film transistors. *See e.g.*, Watanabe '811, [0035]. These lines are shown to connect to respective signal lines and scanning lines driving circuits. *See e.g.*, Watanabe '811, Fig. 5. Connection pads would be inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits.
pixel electrodes, and	Watanabe '811 shows pixel electrodes as items 7 in figure 4. *See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035].
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Watanabe '811 shows metal dummy patterns in figure 5 as items 25 and 27 situated between the connection pads and pixel electrode array and are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed shown in figure 5 where at least 30% of the area shown is covered by the dummy pattern to meet this limitation. *See e.g.*, Watanabe '811, Figs. 5.

CLAIM 2	
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.	Watanabe '811 discloses that the wiring structures are multilayers with the lower layer including aluminum and the upper layer including, chromium or titanium. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].
CLAIM 3	
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.	Watanabe '811 discloses that the wiring structures are multilayers with the lower layer including aluminum and the upper layer including, chromium or titanium. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].
CLAIM 4	
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Watanabe '811 discloses that the wiring structures are multilayers with the lower layer including aluminum and the upper layer including, chromium or titanium. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].
CLAIM 5	
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Watanabe '811 discloses that the wiring structures are multilayers with the lower layer including aluminum and the upper layer including, chromium or titanium. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].
CLAIM 7	
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Watanabe '811 discloses an upper layer of chromium or titanium, which inherently meets this limitation. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].
CLAIM 8	
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Watanabe '811 discloses an upper layer of chromium or titanium, which inherently meets this limitation. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].
CLAIM 9	
A meted [sic] for forming an array substrate for display, comprising:	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].
forming a layer of an insulating substrate, having an area;	Watanabe '811 discloses a glass and thus insulating substrate upon which a TFT array of a liquid crystal display is formed. *See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038].

forming a thin film transistor array formed on the insulating substrate;	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Watanabe '811 discloses thin film transistors connected by signal and scanning lines 5 and 9. *See e.g.*, Watanabe '811, [0035].
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Watanabe '811 is an active matrix display that as discussed above includes scanning and signal lines that provide video-signal to thin film transistors. *See e.g.*, Watanabe '811, [0035]. These lines are shown to connect to respective signal lines and scanning lines driving circuits. *See e.g.*, Watanabe '811, Fig. 5. Connection pads would be inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits.
forming pixel electrodes, and	Watanabe '811 shows pixel electrodes as items 7 in figure 4. *See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035].
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Watanabe '811 shows metal dummy patterns in figure 5 as items 25 and 27 situated between the connection pads and pixel electrode array and are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed shown in figure 5 where at least 30% of the area shown is covered by the dummy pattern to meet this limitation. *See e.g.*, Watanabe '811, Figs. 5.
CLAIM 10	
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.	Watanabe '811 discloses that the wiring structures are multilayers with the lower layer including aluminum and the upper layer including, chromium or titanium. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].
CLAIM 11	
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.	Watanabe '811 discloses that the wiring structures are multilayers with the lower layer including aluminum and the upper layer including, chromium or titanium. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].
CLAIM 12	

The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Watanabe '811 discloses that the wiring structures are multilayers with the lower layer including aluminum and the upper layer including, chromium or titanium. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].
CLAIM 13	
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.	Watanabe '811 discloses that the wiring structures are multilayers with the lower layer including aluminum and the upper layer including, chromium or titanium. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].
CLAIM 15	
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Watanabe '811 discloses an upper layer of chromium or titanium, which inherently meets this limitation. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].
CLAIM 16	
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	Watanabe '811 discloses an upper layer of chromium or titanium, which inherently meets this limitation. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059].

APPENDIX CC26

U.S. PATENT NO. 6, 689, 629 - WATANABE '811 IN VIEW OF SONG

Japanese Publication No. H06-082811 to Watanabe in view of U.S. Patent No. 6,163,356 to Song renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – Watanabe '811	PRIOR ART DISCLOSURE – SONG
An array substrate for display, comprising:	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
a layer of an insulating substrate, having an area;	Watanabe '811 discloses a glass and thus insulating substrate upon which a TFT array of a liquid crystal display is formed. *See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038].	
a thin film transistor array formed on the insulating substrate;	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Watanabe '811 discloses thin film transistors connected by signal and scanning lines 5 and 9. *See e.g.*, Watanabe '811, [0035].	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Watanabe '811 is an active matrix display that as discussed above includes scanning and signal lines that provide video-signal to thin film transistors. *See e.g.*, Watanabe '811, [0035]. These lines are shown to connect to respective signal lines and scanning lines driving circuits. *See e.g.*, Watanabe '811, Fig. 5. Connection pads would be	

	inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits.	
pixel electrodes, and	Watanabe '811 shows pixel electrodes as items 7 in figure 4. *See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035].	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Watanabe '811 shows metal dummy patterns in figure 5 as items 25 and 27 situated between the connection pads and pixel electrode array and are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed shown in figure 5 where at least 30% of the area shown is covered by the dummy pattern to meet this limitation. *See e.g.*, Watanabe '811, Figs. 5.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.	].	Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 9		
A meted [sic] for forming	Watanabe '811 discloses an array	

an array substrate for display, comprising:	substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
forming a layer of an insulating substrate, having an area;	Watanabe '811 discloses a glass and thus insulating substrate upon which a TFT array of a liquid crystal display is formed. *See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038].	
forming a thin film transistor array formed on the insulating substrate;	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Watanabe '811 discloses thin film transistors connected by signal and scanning lines 5 and 9. *See e.g.*, Watanabe '811, [0035].	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Watanabe '811 is an active matrix display that as discussed above includes scanning and signal lines that provide video-signal to thin film transistors. *See e.g.*, Watanabe '811, [0035]. These lines are shown to connect to respective signal lines and scanning lines driving circuits. *See e.g.*, Watanabe '811, Fig. 5. Connection pads would be inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits.	
forming pixel electrodes, and	Watanabe '811 shows pixel electrodes as items 7 in figure 4. *See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035].	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the	Watanabe '811 shows metal dummy patterns in figure 5 as items 25 and 27 situated between the connection pads and pixel	

insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	electrode array and are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed shown in figure 5 where at least 30% of the area shown is covered by the dummy pattern to meet this limitation. *See e.g.*, Watanabe '811, Figs. 5.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 13		
The method for forming an array substrate for display		Song discloses a dual layer wiring including aluminum

according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

APPENDIX CC27

U.S. PATENT NO. 6, 689, 629 - WATANABE '811 IN VIEW OF THE '629 APA

Japanese Publication No. H06-082811 to Watanabe in view of the '629 Admitted Prior Art renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – Watanabe '811	PRIOR ART DISCLOSURE – THE '629 APA
An array substrate for display, comprising:	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
a layer of an insulating substrate, having an area;	Watanabe '811 discloses a glass and thus insulating substrate upon which a TFT array of a liquid crystal display is formed. *See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038].	
a thin film transistor array formed on the insulating substrate;	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Watanabe '811 discloses thin film transistors connected by signal and scanning lines 5 and 9. *See e.g.*, Watanabe '811, [0035].	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Watanabe '811 is an active matrix display that as discussed above includes scanning and signal lines that provide video-signal to thin film transistors. *See e.g.*, Watanabe '811, [0035]. These lines are shown to connect to respective signal lines and scanning lines driving circuits. *See e.g.*, Watanabe '811, Fig. 5. Connection pads would be	

	inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits.	
pixel electrodes, and	Watanabe '811 shows pixel electrodes as items 7 in figure 4. *See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035].	
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Watanabe '811 shows metal dummy patterns in figure 5 as items 25 and 27 situated between the connection pads and pixel electrode array and are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed shown in figure 5 where at least 30% of the area shown is covered by the dummy pattern to meet this limitation. *See e.g.*, Watanabe '811, Figs. 5.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
forming a layer of an insulating substrate, having an area;	Watanabe '811 discloses a glass and thus insulating substrate upon which a TFT array of a liquid crystal display is formed. *See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038].	
forming a thin film transistor array formed on the insulating substrate;	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Watanabe '811 discloses thin film transistors connected by signal and scanning lines 5 and 9. *See e.g.*, Watanabe '811, [0035].	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Watanabe '811 is an active matrix display that as discussed above includes scanning and signal lines that provide video-signal to thin film transistors. *See e.g.*, Watanabe '811, [0035]. These lines are shown to connect to respective signal lines and scanning lines driving circuits. *See e.g.*, Watanabe '811, Fig. 5. Connection pads would be inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits.	
forming pixel electrodes, and	Watanabe '811 shows pixel electrodes as items 7 in figure 4. *See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035].	
forming dummy conductive patterns, the dummy	Watanabe '811 shows metal dummy patterns in figure 5 as	

patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	items 25 and 27 situated between the connection pads and pixel electrode array and are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed shown in figure 5 where at least 30% of the area shown is covered by the dummy pattern to meet this limitation. *See e.g.*, Watanabe '811, Figs. 5.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 13		

The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

APPENDIX CC28

U.S. PATENT NO. 6, 689, 629 - WATANABE '811 IN VIEW OF KUBOTA

Japanese Publication No. H06-082811 to Watanabe in view of U.S. Patent No. 6,157,430 to Kubota renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – Watanabe '811	PRIOR ART DISCLOSURE – KUBOTA
An array substrate for display, comprising:	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
a layer of an insulating substrate, having an area;	Watanabe '811 discloses a glass and thus insulating substrate upon which a TFT array of a liquid crystal display is formed. *See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038].	
a thin film transistor array formed on the insulating substrate;	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Watanabe '811 discloses thin film transistors connected by signal and scanning lines 5 and 9. *See e.g.*, Watanabe '811, [0035].	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Watanabe '811 is an active matrix display that as discussed above includes scanning and signal lines that provide video-signal to thin film transistors. *See e.g.*, Watanabe '811, [0035]. These lines are shown to connect to respective signal lines and scanning lines driving circuits. *See e.g.*, Watanabe '811, Fig. 5. Connection pads would be	

	inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits.	
pixel electrodes, and	Watanabe '811 shows pixel electrodes as items 7 in figure 4. *See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035].	
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Watanabe '811 shows metal dummy patterns in figure 5 as items 25 and 27 situated between the connection pads and pixel electrode array and are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed shown in figure 5 where at least 30% of the area shown is covered by the dummy pattern to meet this limitation. *See e.g.*, Watanabe '811, Figs. 5.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or

		alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g.,

		Kubota, col. 4, ll. 39-55.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 9		
A meted for forming an array substrate for display, comprising:	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
forming a layer of an insulating substrate, having an area;	Watanabe '811 discloses a glass and thus insulating substrate upon which a TFT array of a liquid crystal display is formed. *See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038].	
forming a thin film transistor array formed on the insulating substrate;	Watanabe '811 discloses an array substrate for a liquid crystal display and method of forming an array substrate. *See e.g.*, Watanabe '811, Fig. 5, and [0034].	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Watanabe '811 discloses thin film transistors connected by signal and scanning lines 5 and 9. *See e.g.*, Watanabe '811, [0035].	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Watanabe '811 is an active matrix display that as discussed above includes scanning and signal lines that provide video-signal to thin film transistors. *See e.g.*, Watanabe '811, [0035]. These lines are shown to connect to respective signal lines and scanning lines	

	driving circuits. *See e.g.*, Watanabe '811, Fig. 5. Connection pads would be inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits.	
Forming pixel electrodes, and	Watanabe '811 shows pixel electrodes as items 7 in figure 4. *See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035].	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Watanabe '811 shows metal dummy patterns in figure 5 as items 25 and 27 situated between the connection pads and pixel electrode array and are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed shown in figure 5 where at least 30% of the area shown is covered by the dummy pattern to meet this limitation. *See e.g.*, Watanabe '811, Figs. 5.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a

from the group consisting of aluminum and aluminum alloys.		group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of

or alkaline etchant.		chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

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APPENDIX CC29

U.S. PATENT NO. 6, 689, 629 - MIYASHITA

Japanese Publication No. H09-197415 to Miyashita anticipates Claims 1 and 9 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – MIYASHITA
An array substrate for display, comprising:	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].
a layer of an insulating substrate, having an area;	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].
a thin film transistor array formed on the insulating substrate;	The device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate. *See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019].
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Miyashita discloses thin film transistors connected by gate and data lines 5 and 6. *See e.g.*, Miyashita , [0019] and Fig 2..
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Miyashita is an active matrix display that as discussed above includes gate and data line that provide gate and data signals to thin film transistors. *See e.g.*, JP '415, [0019]. These lines extend to the edge of the substrate and contact pads 5b and 6b. *See e.g.*, Miyashita, [0019], and Fig. 1.
pixel electrodes, and	Miyashita shows pixel electrodes as items 3 in figure 3. *See e.g.*, Miyashita, Fig. 3, item 3. The pixel electrodes are transparent and correspond to display areas that are arranged as a matrix. *See e.g.*, Miyashita, [0019]. Miyashita also discloses that the pixel electrode drive the liquid crystal. *See e.g.*, Miyashita, [002]-[003].
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the	Dummy patterns in Miyashita are formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3. *See e.g.*, Miyashita, Fig 2 (dummy film forming region D); [0023]. A closer view is shown in figure 3, also shows the dummy patterns 8 are situated between the connection pads and the pixel electrodes and are not in contact with any of the wiring. *See e.g.*,

wiring.	Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed as shown in, for example, in figure 3, where at least 30% of the area shown is covered by the dummy pattern. *See e.g.*, Miyashita, Fig. 3.
CLAIM 9	
A meted for forming an array substrate for display, comprising:	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].
forming a layer of an insulating substrate, having an area;	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].
forming a thin film transistor array formed on the insulating substrate;	The device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate. *See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019].
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Miyashita discloses thin film transistors connected by gate and data lines 5 and 6. *See e.g.*, Miyashita , [0019] and Fig 2..
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Miyashita is an active matrix display that as discussed above includes gate and data line that provide gate and data signals to thin film transistors. *See e.g.*, JP '415, [0019]. These lines extend to the edge of the substrate and contact pads 5b and 6b. *See e.g.*, Miyashita, [0019], and Fig. 1.
forming pixel electrodes, and	Miyashita shows pixel electrodes as items 3 in figure 3. *See e.g.*, Miyashita, Fig. 3, item 3. The pixel electrodes are transparent and correspond to display areas that are arranged as a matrix. *See e.g.*, Miyashita, [0019]. Miyashita also discloses that the pixel electrode drive the liquid crystal. *See e.g.*, Miyashita, [002]-[003].
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters	Dummy patterns in Miyashita are formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3. *See e.g.*, Miyashita, Fig 2 (dummy film forming region D); [0023]. A closer view is shown in figure 3, also shows the dummy patterns 8 are situated between the connection pads and the pixel electrodes

are not in contact with any of the wiring.	and are not in contact with any of the wiring. *See e.g.*, Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed as shown in, for example, in figure 3, where at least 30% of the area shown is covered by the dummy pattern. *See e.g.*, Miyashita, Fig. 3.

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APPENDIX CC30

U.S. PATENT NO. 6, 689, 629 - MIYASHITA IN VIEW OF SONG

Japanese Publication No. H09-197415 to Miyashita in view of U.S. Patent No. 6,163,356 to Song renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – MIYASHITA	PRIOR ART DISCLOSURE – SONG
An array substrate for display, comprising:	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	
a layer of an insulating substrate, having an area;	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	
a thin film transistor array formed on the insulating substrate;	The device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate. *See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019].	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Miyashita discloses thin film transistors connected by gate and data lines 5 and 6. *See e.g.*, Miyashita , [0019] and Fig 2..	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Miyashita is an active matrix display that as discussed above includes gate and data line that provide gate and data signals to thin film transistors. *See e.g.*, JP '415, [0019]. These lines extend to the edge of the substrate and contact pads 5b and 6b. *See e.g.*, Miyashita, [0019], and Fig. 1.	

pixel electrodes, and	Miyashita shows pixel electrodes as items 3 in figure 3. *See e.g.*, Miyashita, Fig. 3, item 3. The pixel electrodes are transparent and correspond to display areas that are arranged as a matrix. *See e.g.*, Miyashita, [0019]. Miyashita also discloses that the pixel electrode drive the liquid crystal. *See e.g.*, Miyashita, [002]-[003].	
Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Dummy patterns in Miyashita are formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3. *See e.g.*, Miyashita, Fig 2 (dummy film forming region D); [0023]. A closer view is shown in figure 3, also shows the dummy patterns 8 are situated between the connection pads and the pixel electrodes and are not in contact with any of the wiring. *See e.g.*, Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed as shown in, for example, in figure 3, where at least 30% of the area shown is covered by the dummy pattern. *See e.g.*, Miyashita, Fig. 3.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	
forming a layer of an insulating substrate, having an area;	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	
forming a thin film transistor array formed on the insulating substrate;	The device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate. *See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019].	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Miyashita discloses thin film transistors connected by gate and data lines 5 and 6. *See e.g.*, Miyashita , [0019] and Fig 2..	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Miyashita is an active matrix display that as discussed above includes gate and data line that provide gate and data signals to thin film transistors. *See e.g.*, JP '415, [0019]. These lines extend to the edge of the substrate and contact pads 5b and 6b. *See e.g.*, Miyashita, [0019], and Fig. 1.	

forming pixel electrodes, and	Miyashita shows pixel electrodes as items 3 in figure 3. *See e.g.*, Miyashita, Fig. 3, item 3. The pixel electrodes are transparent and correspond to display areas that are arranged as a matrix. *See e.g.*, Miyashita, [0019]. Miyashita also discloses that the pixel electrode drive the liquid crystal. *See e.g.*, Miyashita, [002]-[003].	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Dummy patterns in Miyashita are formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3. *See e.g.*, Miyashita, Fig 2 (dummy film forming region D); [0023]. A closer view is shown in figure 3, also shows the dummy patterns 8 are situated between the connection pads and the pixel electrodes and are not in contact with any of the wiring. *See e.g.*, Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed as shown in, for example, in figure 3, where at least 30% of the area shown is covered by the dummy pattern. *See e.g.*, Miyashita, Fig. 3.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18.

APPENDIX CC31

U.S. PATENT NO. 6, 689, 629 - MIYASHITA IN VIEW OF THE '629 APA

Japanese Publication No. H09-197415 to Miyashita in view of the '629 Admitted Prior Art renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – MIYASHITA	PRIOR ART DISCLOSURE – THE '629 APA
An array substrate for display, comprising:	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	
a layer of an insulating substrate, having an area;	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	
a thin film transistor array formed on the insulating substrate;	The device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate. *See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019].	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Miyashita discloses thin film transistors connected by gate and data lines 5 and 6. *See e.g.*, Miyashita , [0019] and Fig 2..	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Miyashita is an active matrix display that as discussed above includes gate and data line that provide gate and data signals to thin film transistors. *See e.g.*, JP '415, [0019]. These lines extend to the edge of the substrate and contact pads 5b and 6b. *See e.g.*, Miyashita, [0019], and Fig. 1.	

pixel electrodes, and	Miyashita shows pixel electrodes as items 3 in figure 3. *See e.g.*, Miyashita, Fig. 3, item 3. The pixel electrodes are transparent and correspond to display areas that are arranged as a matrix. *See e.g.*, Miyashita, [0019]. Miyashita also discloses that the pixel electrode drive the liquid crystal. *See e.g.*, Miyashita, [002]-[003].	
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Dummy patterns in Miyashita are formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3. *See e.g.*, Miyashita, Fig 2 (dummy film forming region D); [0023]. A closer view is shown in figure 3, also shows the dummy patterns 8 are situated between the connection pads and the pixel electrodes and are not in contact with any of the wiring. *See e.g.*, Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed as shown in, for example, in figure 3, where at least 30% of the area shown is covered by the dummy pattern. *See e.g.*, Miyashita, Fig. 3.	
CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	
forming a layer of an insulating substrate, having an area;	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	
forming a thin film transistor array formed on the insulating substrate;	The device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate. *See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019].	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Miyashita discloses thin film transistors connected by gate and data lines 5 and 6. *See e.g.*, Miyashita , [0019] and Fig 2..	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Miyashita is an active matrix display that as discussed above includes gate and data line that provide gate and data signals to thin film transistors. *See e.g.*, JP '415, [0019]. These lines extend to the edge of the substrate and contact pads 5b and 6b. *See e.g.*, Miyashita, [0019], and Fig. 1.	

forming pixel electrodes, and	Miyashita shows pixel electrodes as items 3 in figure 3. *See e.g.*, Miyashita, Fig. 3, item 3. The pixel electrodes are transparent and correspond to display areas that are arranged as a matrix. *See e.g.*, Miyashita, [0019]. Miyashita also discloses that the pixel electrode drive the liquid crystal. *See e.g.*, Miyashita, [002]-[003].	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Dummy patterns in Miyashita are formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3. *See e.g.*, Miyashita, Fig 2 (dummy film forming region D); [0023]. A closer view is shown in figure 3, also shows the dummy patterns 8 are situated between the connection pads and the pixel electrodes and are not in contact with any of the wiring. *See e.g.*, Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed as shown in, for example, in figure 3, where at least 30% of the area shown is covered by the dummy pattern. *See e.g.*, Miyashita, Fig. 3.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 12		
The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		The '629 APA discloses a lower layer wiring material of aluminum and an upper layer wiring material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum. See e.g., the '629 patent, col. 1, ll. 26-39.

APPENDIX CC32

U.S. PATENT NO. 6, 689, 629 - MIYASHITA IN VIEW OF KUBOTA

Japanese Publication No. H09-197415 to Miyashita in view of U.S. Patent No. 6,157,430 to Kubota renders obvious Claims 2-8 and 10-16 of the '629 patent.

CLAIM 1	PRIOR ART DISCLOSURE – MIYASHITA	PRIOR ART DISCLOSURE – KUBOTA
An array substrate for display, comprising:	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	
a layer of an insulating substrate, having an area;	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	
a thin film transistor array formed on the insulating substrate;	The device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate. *See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019].	
a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;	Miyashita discloses thin film transistors connected by gate and data lines 5 and 6. *See e.g.*, Miyashita , [0019] and Fig 2..	
connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Miyashita is an active matrix display that as discussed above includes gate and data line that provide gate and data signals to thin film transistors. *See e.g.*, JP '415, [0019]. These lines extend to the edge of the substrate and contact pads 5b and 6b. *See e.g.*, Miyashita, [0019], and Fig. 1.	

pixel electrodes, and	Miyashita shows pixel electrodes as items 3 in figure 3. *See e.g.*, Miyashita, Fig. 3, item 3. The pixel electrodes are transparent and correspond to display areas that are arranged as a matrix. *See e.g.*, Miyashita, [0019]. Miyashita also discloses that the pixel electrode drive the liquid crystal. *See e.g.*, Miyashita, [002]-[003].	
dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	Dummy patterns in Miyashita are formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3. *See e.g.*, Miyashita, Fig 2 (dummy film forming region D); [0023]. A closer view is shown in figure 3, also shows the dummy patterns 8 are situated between the connection pads and the pixel electrodes and are not in contact with any of the wiring. *See e.g.*, Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed as shown in, for example, in figure 3, where at least 30% of the area shown is covered by the dummy pattern. *See e.g.*, Miyashita, Fig. 3.	

CLAIM 2		
The array substrate for display according to claim 1, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 3		
The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 4		
The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 5		
The array substrate for display according to claim 3, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

CLAIM 6		
The array substrate for display according to claim 5, wherein the upper layer wiring material is selected from the group consisting of molybdenum and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 7		
The array substrate for display according to claim 4 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 8		
The array substrate for display according to claim 5 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 9		
A meted [sic] for forming an array substrate for display, comprising:	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	

forming a layer of an insulating substrate, having an area;	Miyashita discloses an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed. *See e.g.*, Miyashita, Fig. 3, and [0018]-[0019].	
forming a thin film transistor array formed on the insulating substrate;	The device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate. *See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019].	
each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;	Miyashita discloses thin film transistors connected by gate and data lines 5 and 6. *See e.g.*, Miyashita , [0019] and Fig 2..	
forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;	The device in Miyashita is an active matrix display that as discussed above includes gate and data line that provide gate and data signals to thin film transistors. *See e.g.*, JP '415, [0019]. These lines extend to the edge of the substrate and contact pads 5b and 6b. *See e.g.*, Miyashita, [0019], and Fig. 1.	
forming pixel electrodes, and	Miyashita shows pixel electrodes as items 3 in figure 3. *See e.g.*, Miyashita, Fig. 3, item 3. The pixel electrodes are transparent and correspond to display areas that are arranged as a matrix. *See e.g.*, Miyashita, [0019]. Miyashita also discloses that the pixel electrode drive the liquid crystal. *See e.g.*, Miyashita, [002]-[003].	
forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the	Dummy patterns in Miyashita are formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3. *See e.g.*, Miyashita, Fig 2 (dummy film forming	

connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.	region D); [0023]. A closer view is shown in figure 3, also shows the dummy patterns 8 are situated between the connection pads and the pixel electrodes and are not in contact with any of the wiring. *See e.g.*, Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025]. It is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed as shown in, for example, in figure 3, where at least 30% of the area shown is covered by the dummy pattern. *See e.g.*, Miyashita, Fig. 3.	
CLAIM 10		
The method for forming an array substrate for display according to claim 9, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 11		
The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 12		
The method for forming an array substrate for display according to claim 10		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy

wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 13		
The method for forming an array substrate for display according to claim 11, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 14		
The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum, and alloys thereof.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 15		
The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material does not become insoluble in an acid or alkaline etchant.		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.
CLAIM 16		
The method for forming an array substrate for display according to claim 13 wherein the upper layer		Kubota discloses a lower layer wiring material is aluminum or aluminum alloy and the upper layer wiring

wiring material does not become insoluble in an acid or alkaline etchant.		material is selected from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof. See e.g., Kubota, col. 4, ll. 39-55.

DC:50680741.1

Re-Exam

PTO/SB/57 (02-09)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also referred to as PTO/SB/57(A))

REQUEST FOR *EX PARTE* REEXAMINATION TRANSMITTAL FORM

Address to:
Mail Stop *Ex Parte* Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney Docket No.: 7773.0084

Date: February 26, 2010

1. ☒ This is a request for *ex parte* reexamination pursuant to 37 CFR 1.510 of patent number 6,689,629 issued February 10, 2004. The request is made by:
   ☐ patent owner. ☒ third party requester.

2. ☒ The name and address of the person requesting reexamination is:
   Song K. Jung
   McKenna Long and Aldridge LLP
   1900 K Street, N.W., Washington D.C. 20006

3. ☒ a. A check in the amount of $2,520.00 is enclosed to cover the reexamination fee, 37 CFR 1.20(c)(1);
   ☐ b. The Director is hereby authorized to charge the fee as set forth in 37 CFR 1.20(c)(1) to Deposit Account No. _____ ; **or**
   ☐ c. Payment by credit card. Form PTO-2038 is attached.

4. ☒ Any refund should be made by ☐ check or ☒ credit to Deposit Account No. 50-0911 37 CFR 1.26(c). If payment is made by credit card, refund must be to credit card account.

5. ☒ A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.510(b)(4)

6. ☐ CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
   ☐ Landscape Table on CD

7. ☐ Nucleotide and/or Amino Acid Sequence Submission
   If applicable, items a. – c. are required.
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM (2 copies) or CD-R (2 copies); **or**
      ii. ☐ paper
   c. ☐ Statements verifying identity of above copies

8. ☐ A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.

9. ☒ Reexamination of claim(s) 1-16 is requested.

10. ☒ A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.

11. ☒ An English language translation of all necessary and pertinent non-English language patents and/or printed publications is included.

12. [X] The attached detailed request includes at least the following items:

a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.510(b)(1)
b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR 1.510(b)(2).

13. [ ] A proposed amendment is included (only where the patent owner is the requester). 37 CFR 1.510(e)

14. [X] a. It is certified that a copy of this request (if filed by other than the patent owner) has been served in its entirety on the patent owner as provided in 37 CFR 1.33(c).
The name and address of the party served and the date of service are:

Daniel McClure

Thomas, Kayden, Horstmeyer & Risley, LLP

600 Galleria Parkway, S.E., 15th Floor, Atlanta, GA 30339-5994

Date of Service: February 26, 2010 ; **or**

[ ] b. A duplicate copy is enclosed because service on patent owner was not possible. An explanation of the efforts made to serve patent owner **is attached**. See MPEP 2220.

15. Correspondence Address: Direct all communications about the reexamination to:

[X] The address associated with Customer Number: 30827

OR

[ ] Firm or Individual Name

Address

City	State	Zip
Country		
Telephone	Email	

16. [X] The patent is currently the subject of the following concurrent proceeding(s):

[ ] a. Copending reissue Application No.
[ ] b. Copending reexamination Control No.
[ ] c. Copending Interference No.
[X] d. Copending litigation styled:

LG Display Co., Ltd. v. Chi Mei Optoelectronics Corp.,

C.A. Nos. 06-726(JJF) (D. Del. 2006).

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

~~Authorized Signature~~ — Date: February 26, 2010

Song K. Jung — Typed/Printed Name

35,210 — Registration No.

[ ] For Patent Owner Requester
[X] For Third Party Requester

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re: Reexamination of U.S. Patent No. 6,689,629 B2

Inventors: Tsujimura et al.

Issued: February 10, 2004

Filed: February 5, 2002

Titled: Array Substrate For Display, Method of Manufacturing Array Substrate For Display and Display Device Using the Array Substrate

Atty. Docket: 7773.084.60

CERTIFICATE OF SERVICE

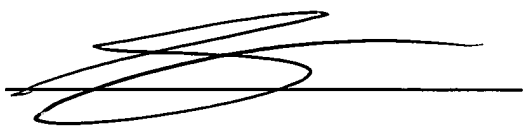
Mail Stop ***Ex Parte Reexamination***
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.33(c) and M.P.E.P. § 2220, I hereby certify that a true and correct copy of the Request For *Ex Parte* Reexamination of U.S. Patent No. 6,689,629 with attachments; Form PTO/SB/08, and this certificate were served on February 26, 2010, on the following attorney of record in U.S. Patent No. 6,689,629 via first class mail at the following addresses.

Daniel McClure
Thomas, Kayden, Horstmeyer & Risley, LLP
600 Galleria Parkway, S.E.
15th Floor
Atlanta, GA 30339-5994

DATED this 26th day of February, 2010



Song K. Jung

US006689629B2

(12) **United States Patent**
Tsujimura et al.

(10) **Patent No.: US 6,689,629 B2**
(45) **Date of Patent: Feb. 10, 2004**

(54) **ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE**

(75) Inventors: **Takatoshi Tsujimura**, Fujisawa (JP); **Atsuya Makita**, Sagamihara (JP); **Toshiaki Arai**, Yokohama (JP)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 54 days.

(21) Appl. No.: **10/068,500**

(22) Filed: **Feb. 5, 2002**

(65) **Prior Publication Data**

US 2002/0106843 A1 Aug. 8, 2002

(30) **Foreign Application Priority Data**

Feb. 6, 2001 (JP) 2001-029587

(51) **Int. Cl.**[7] **H01L 21/00**

(52) **U.S. Cl.** **438/25**; 438/149; 438/73; 257/72; 257/748

(58) **Field of Search** 438/25, 22, 30, 438/149, 73; 257/72, 748

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,285,301 A * 2/1994 Shirahashi et al. 359/59
6,163,356 A * 12/2000 Song et al. 349/152

* cited by examiner

Primary Examiner—Caridad Everhart
(74) *Attorney, Agent, or Firm*—Tiffany L. Townsend

(57) **ABSTRACT**

Disclosed is to provide an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display.

The present invention is an array substrate for display, which includes: a thin film transistor array formed on an insulating substrate **1**; a plurality of wirings **23** and **24** arranged on the insulating substrate **1**; connection pads **25** and **27** arranged on unilateral ends of the wirings **23** and **24** and respectively connected therewith; and pixel electrodes **22**, wherein dummy conductive patterns **29** are arranged between the ends of the connection pads **25** and **27** and ends of the pixel electrodes **22**.

16 Claims, 11 Drawing Sheets

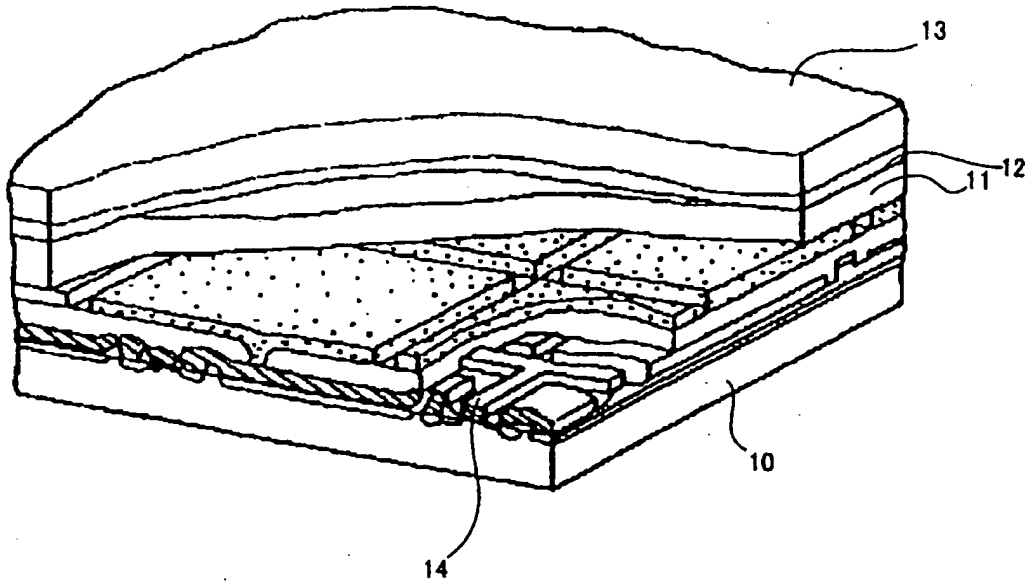


FIG. 1

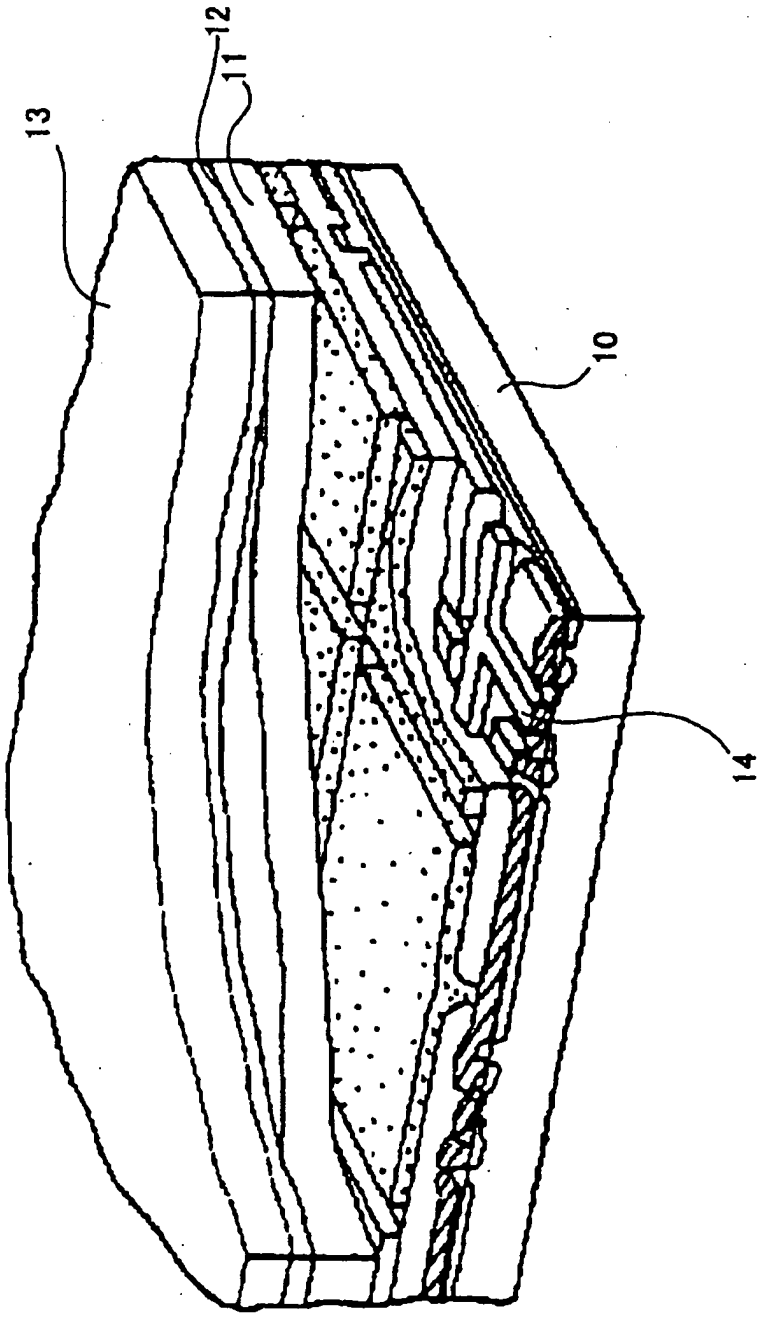


FIG. 2

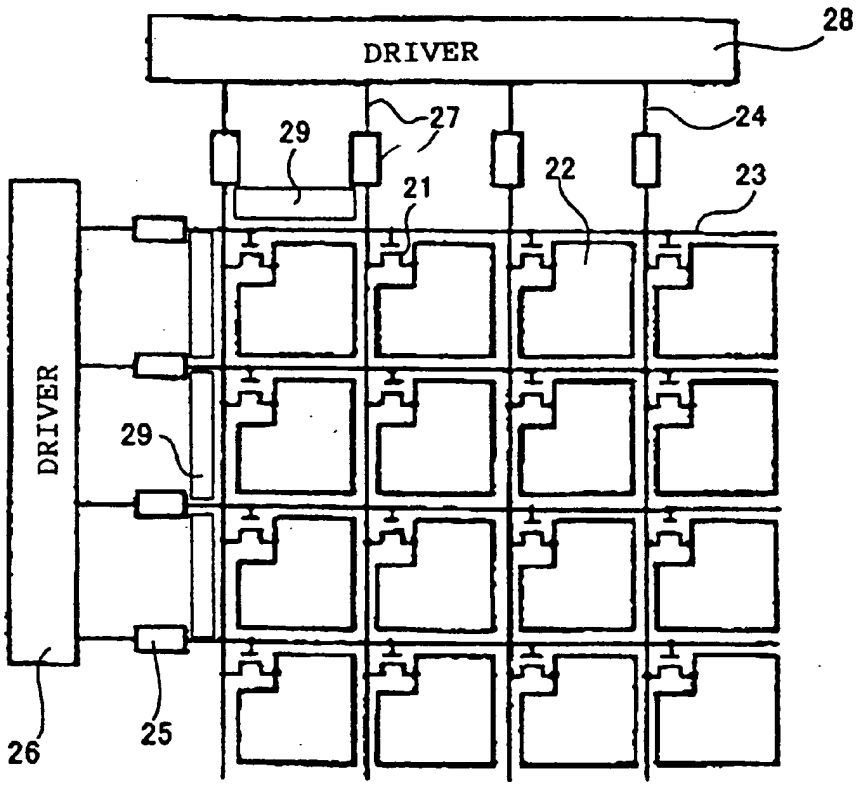


FIG. 3

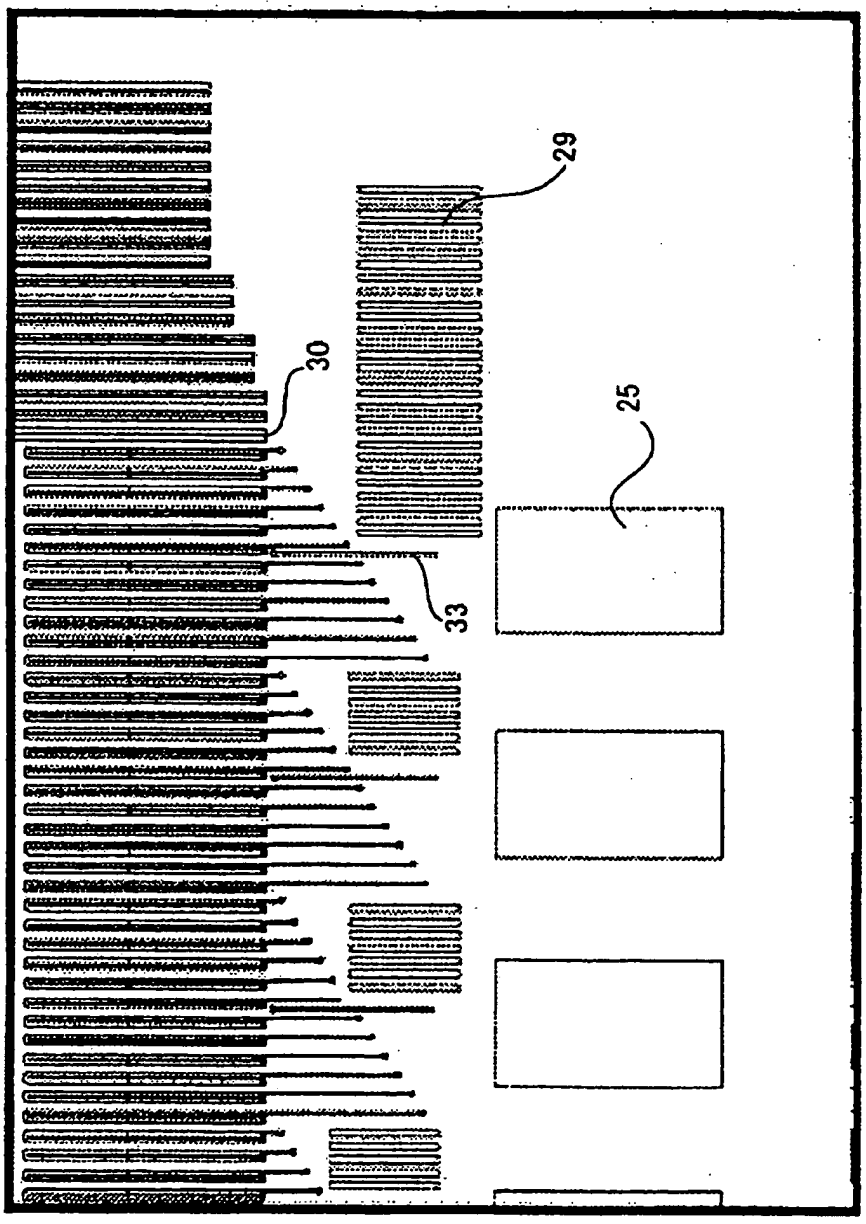


FIG. 4

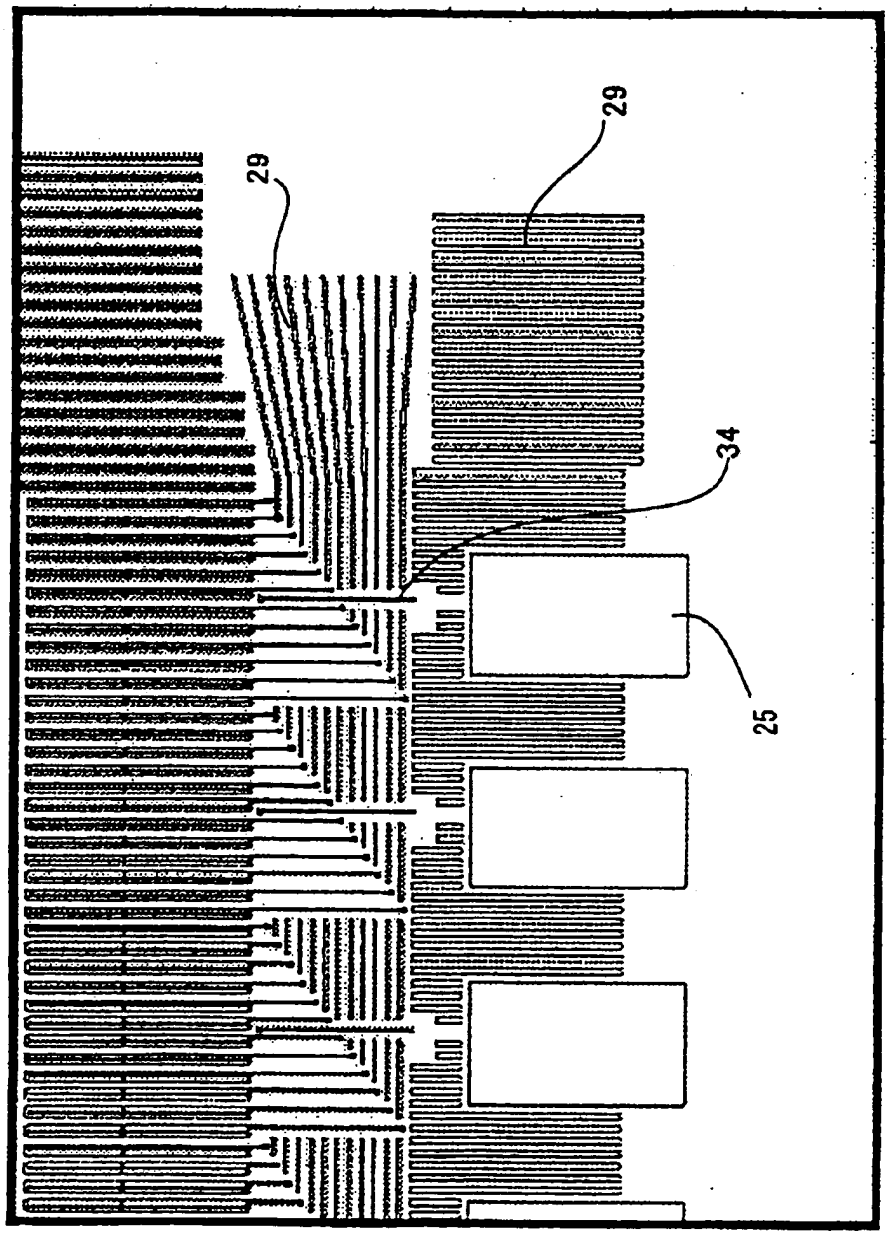


FIG. 5

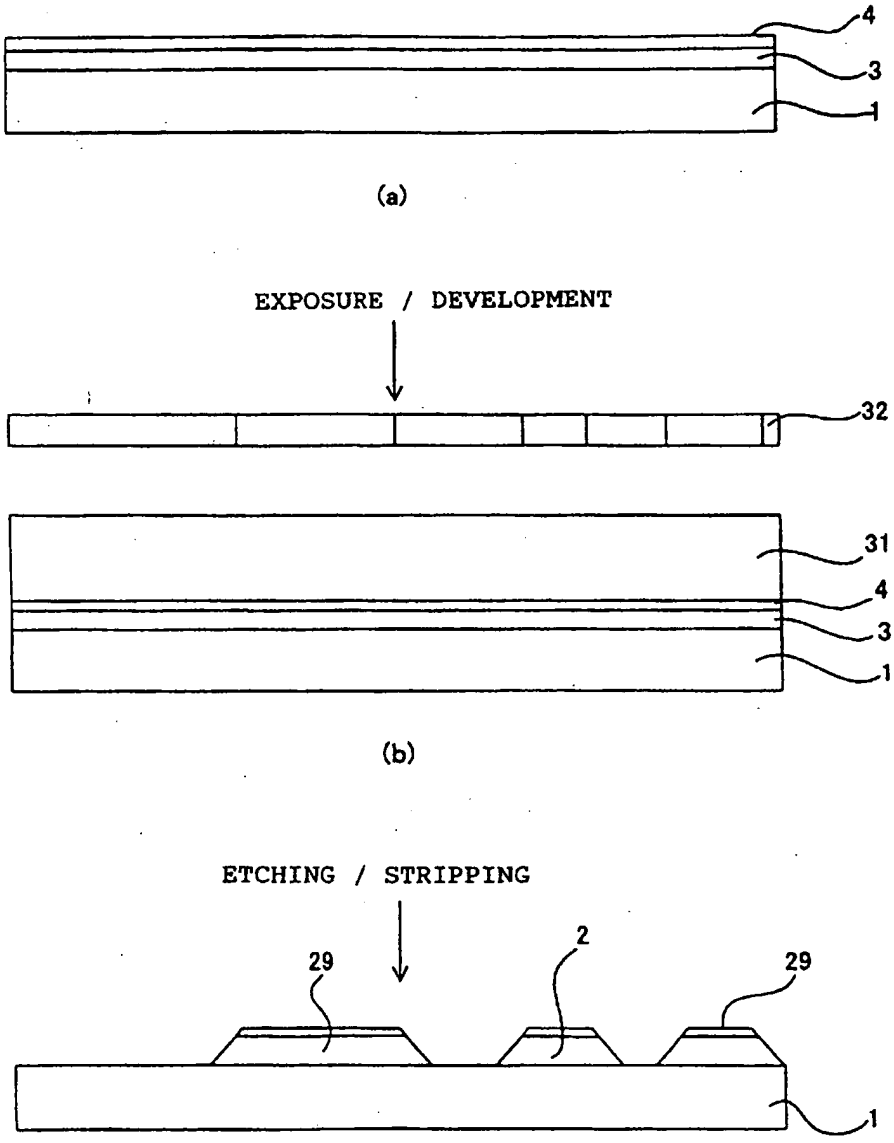

4
3
1
(a)
EXPOSURE / DEVELOPMENT
32
31
4
3
1
(b)
ETCHING / STRIPPING
29
2
29
1
(c)

FIG. 6

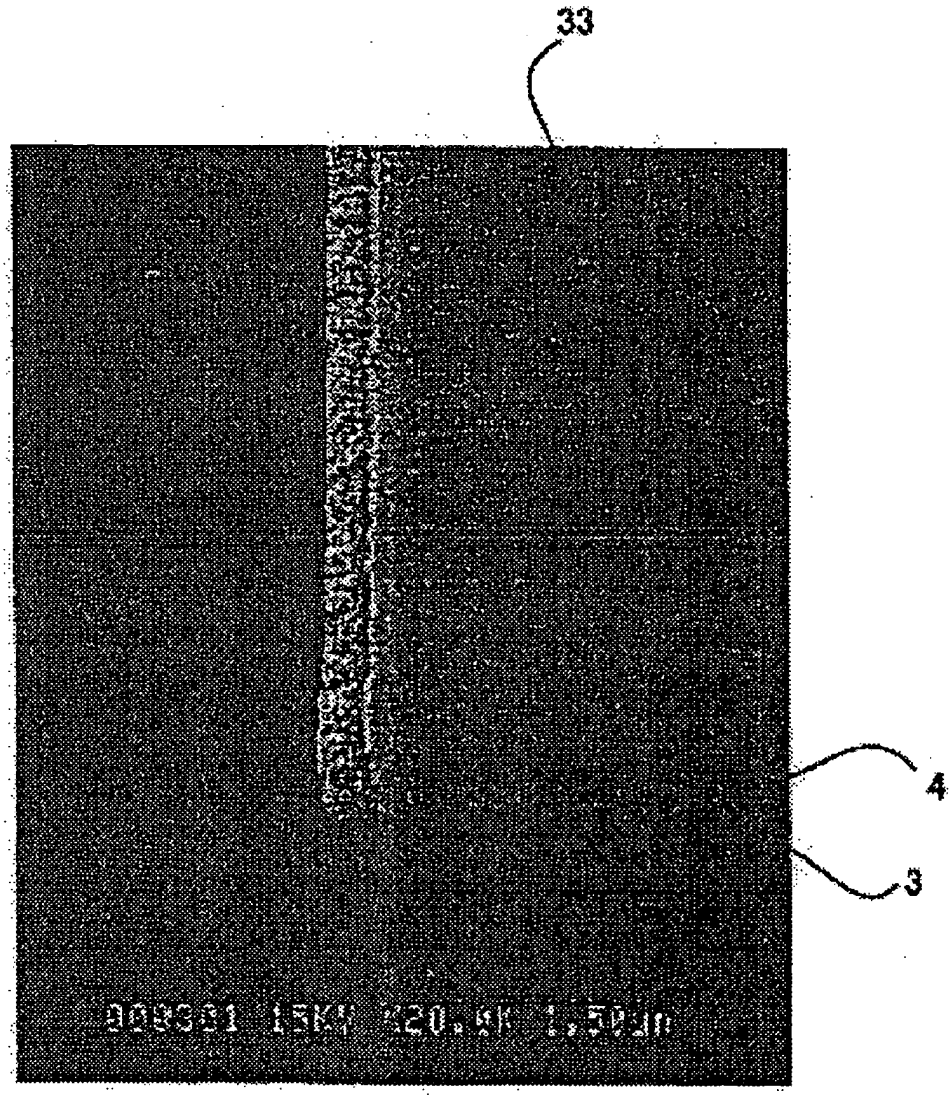


FIG. 7

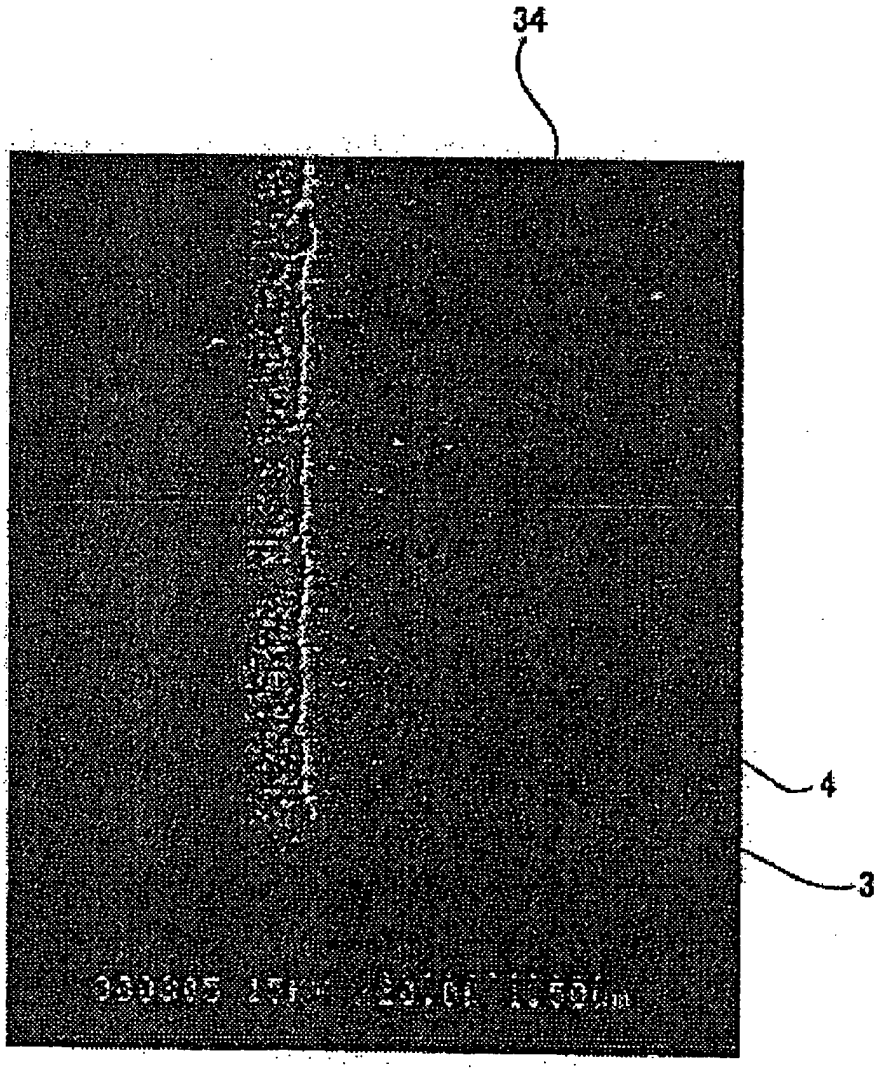


FIG. 8

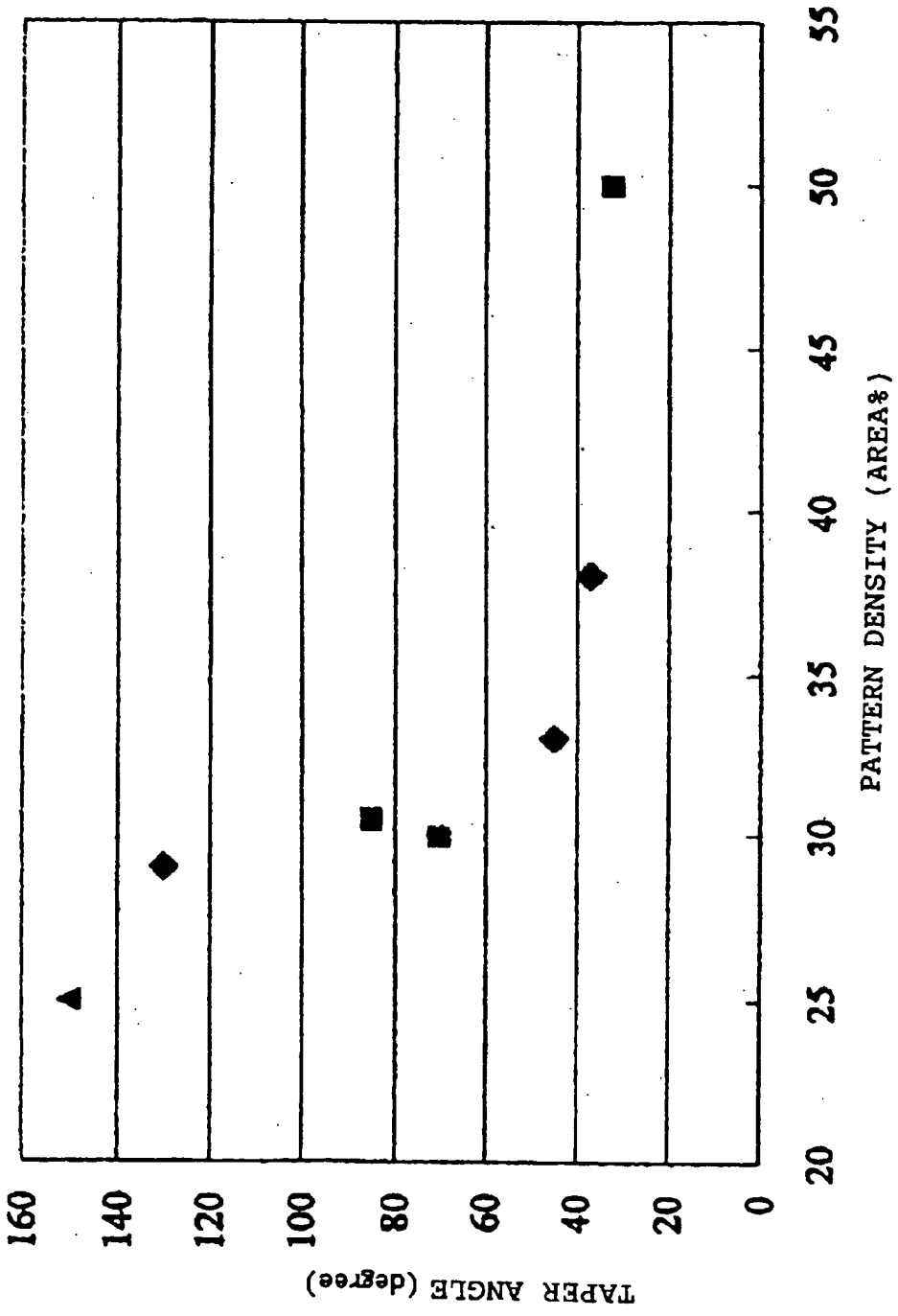

PATTERN DENSITY (AREA%)
20
25
30
35
40
45
50
55
TAPER ANGLE (degree)
160
140
120
100
80
60
40
20
0

FIG. 9

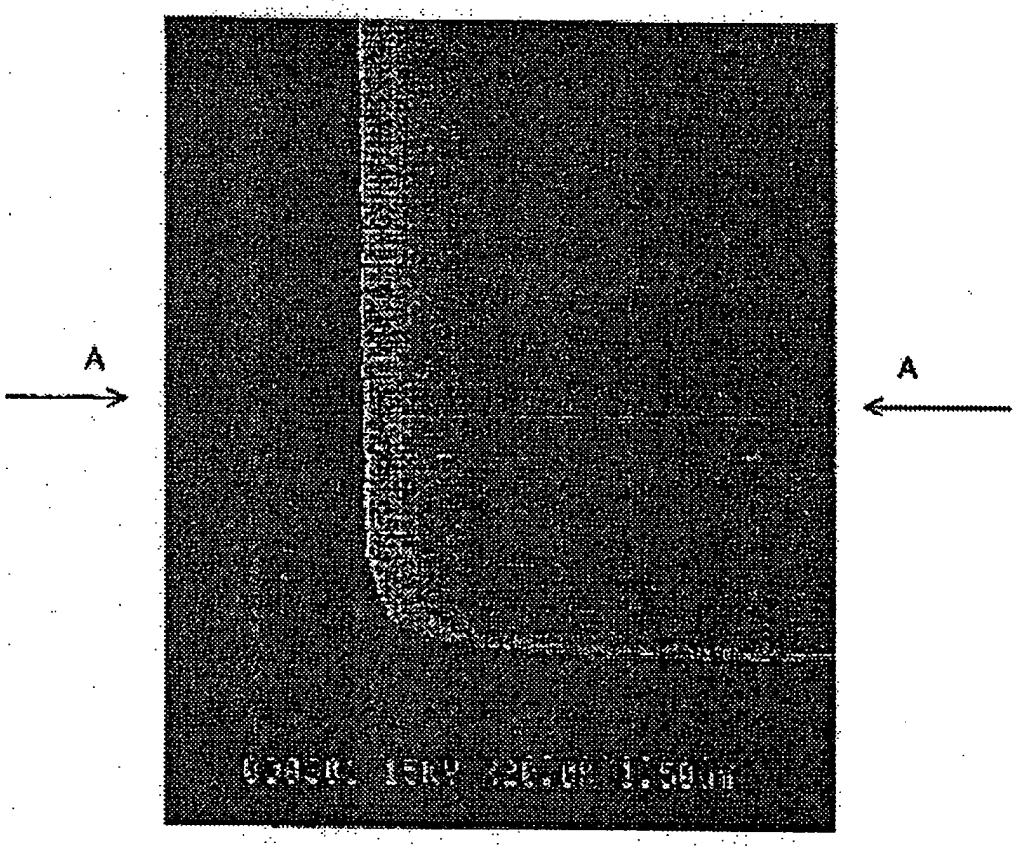


FIG. 10

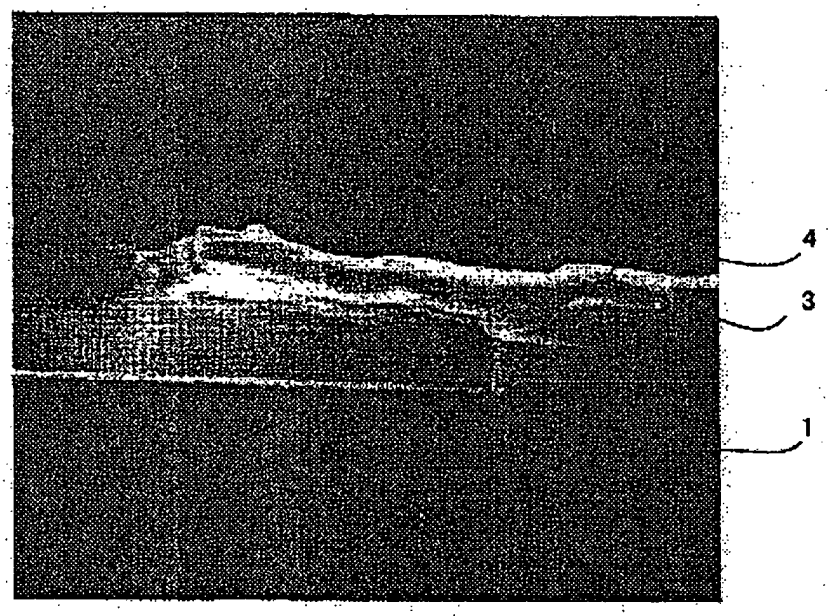


FIG. 11

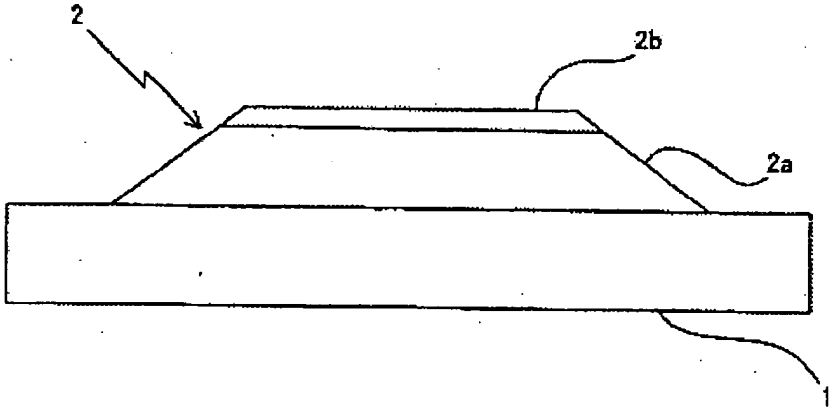
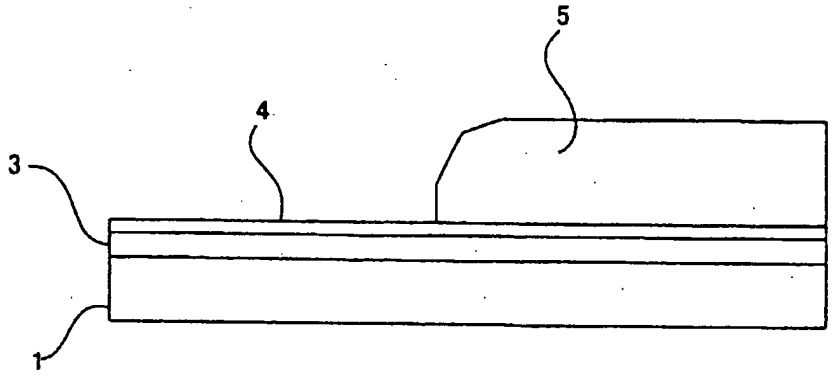
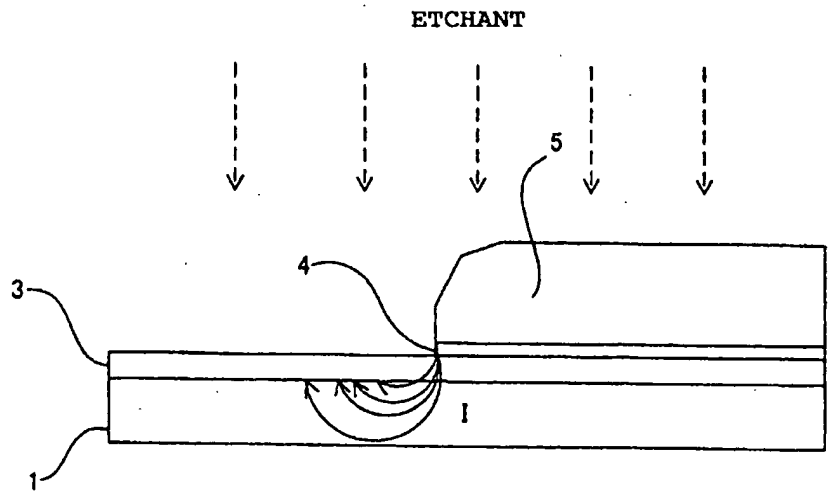


FIG. 12



(a)



(b)

ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

BACKGROUND OF THE INVENTION

The present invention relates to an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display.

A display device using a thin film transistor (TFT) array has been frequently used owing to low power consumption and capability of downsizing the display device. The thin film transistor array is manufactured by forming thin film transistors, each being composed of electrodes such as a gate electrode, a source electrode and a drain electrode, wirings such as scan lines and signal lines connected with the above-mentioned electrodes, and pixel electrodes on an insulating substrate.

In recent years, a higher operating speed, a higher resolution and a larger size have been required for the display device described above in many cases. A high speed and a high density have been required for each constituent component of the array for display, which forms a display device. Particularly, in order to operate the thin film transistor array at a high speed, it is preferable to use low-resistance aluminum (Al) for the wirings such as the scan lines and the signal lines since delay in gate pulses can be reduced and a writing speed to the thin film transistor can be increased.

Incidentally, aluminum tends to be easily oxidized in spite of its low resistance. Therefore, in many cases, wiring using aluminum is constituted as a two-layer structure, in which aluminum is used as a lower conductive material, and a material harder to be oxidized than aluminum such as chromium, tantalum, titanium or molybdenum is used as an upper conductive material. FIG. **11** is a view schematically showing a state where wiring **2** is deposited on an insulating substrate **1**. A lower conductive material film **2***a* is deposited on an insulating substrate **1** made of such as glass, and an upper conductive material film **2***b* is deposited on the lower conductive material film **2***a*. Each of these films **2***a* and **2***b* is patterned by, for example, a proper etching process so as to have tapered ends.

In order to form a tapered shape shown in FIG. **11**, an etching rate for the upper conductive material is required to be increased. In order to form the tapered shape shown in FIG. **11**, various methods have been proposed up to now. For example, in the gazette of Japanese Patent Laid-Open No. Hei 10 (1998)-90706, a method has been proposed, in which dummy connection pads are provided on sides opposite to scan line connection pads and signal line connection pads, respectively. According to this method, over etching due to an etchant that will be relatively increased by lowering wiring density at ends of the substrate is prevented. Thus, undercut of a lower conductive material **3** is prevented, and an interlayer short circuit is prevented by imparting a proper tapered shape to the wiring **2**.

However, though this method enables evenness of etching at the ends of the thin film transistor array substrate to be improved, the method cannot effectively prevent the undercut of the signal lines in a region where the wiring density is apt to be lowered from ends of the pixel electrodes to the connection pads, for example, in a portion where drawing wiring is formed.

Moreover, in the gazette of Japanese Patent Laid-Open No. Hei 10 (1998)-240150, disclosed is a method of forming a tapered shape at an angle ranging from 20 degrees to 70 degrees on wiring constituted of two layers, in which a pad formed of aluminum and metal such as molybdenum formed on the aluminum is subjected to wet etching. According to this method, a specified tapered shape can be imparted to the wiring formed of a conductive film of a two-layer structure by the wet etching. However, the method never discloses a method of evenly etching a substrate region while maintaining a selection ratio thereof even in the substrate region where the wiring density is lowered.

FIGS. **12**A and **12**B are enlarged schematic views for explaining a patterning process using a conventionally used wet process in order to impart the above-described tapered shape to the wiring. As shown in FIG. **12**A, the lower conductive material **3** and an upper conductive material **4** are deposited on the insulating substrate **1** by a method such as physical vapor deposition. FIG. **12**A shows that a photoresist film **5** is coated on a film of the upper conductive material **4** and is patterned in a desired shape. The respective films are etched by an etchant such as a solution of phosphoric acid, nitric acid, acetic acid or mixtures thereof, and desired tapered shapes are formed thereon.

FIG. **12**B is a view for explaining an electrochemical process generated as each film is being etched when the wiring constituted of the upper conductive material **4** and the lower conductive material **3** is subjected to wet etching. In FIG. **12**B, an internal layer portion of the upper conductive material **4** coated with the photoresist film **5** is not dissolved. However, at the end of the photoresist film **5**, the upper conductive material **4** is dissolved by the etchant. When the wiring is formed by the wet etching, the upper conductive material **4** protected by the photoresist film **5** is further dissolved in a lateral direction from the end of the photoresist film **5** to turn into positive ions, and electrons emitted as a result are supplied to the lower conductive material **3**. Thus, the upper conductive material **4** serves as an anode. In this connection, the lower conductive material **3** comes to serve as a cathode. Accordingly, an electrochemical cell is formed. Here, when the etching rate for the upper conductive material **4** is increased to form a required tapered shape, the density of the electrons generated by dissolving the upper conductive material **4** and flowing to the lower conductive material **3** is increased accompanied with an increase of a dissolution rate of the upper conductive material **4**. FIG. **12**B schematically shows currents I flowing from the upper conductive material **4** to the lower conductive material **3**.

As the etching rate is increased, the density of the current flowing to an area of the upper conductive material **4**, which is exposed to the etchant, exceeds a current density causing passivity of the upper conductive material **4**. In such a case, the upper conductive material **4** is passivated not to be dissolved by the etchant, and only the lower conductive material **3** is dissolved accompanied with the progress of the etching, resulting in the occurrence of the undercut. When such undercut occurs, the wiring, for example, the gate wiring cannot be sufficiently coated with an insulating film in some cases, thus causing inconvenience such as an interlayer short circuit, resulting in lowering a yield of the display device.

SUMMARY OF THE INVENTION

The present invention was made with the foregoing problems in mind. An object of the present invention is to

provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of being etched at a sufficiently high etching rate and a sufficient selection ratio, eliminating undercut, and providing a large-sized and high-resolution display device.

The foregoing object of the present invention is achieved by providing the array substrate for display, the method of manufacturing an array substrate for display and the display device using the array substrate for display of the present invention.

Specifically, according to the present invention, provided is an array substrate for display, comprising: a thin film transistor array formed on an insulating substrate; a plurality of wirings arranged on the insulating substrate; connection pads arranged on unilateral ends of the wirings and respectively connected with the wirings; pixel electrodes, and dummy conductive patterns arranged between the ends of the connection pads and ends of the pixel electrodes. The dummy conductive patterns can occupy 30 area % or more. In the present invention, the dummy conductive patterns can be formed as any of land patterns and line-and-space patterns. In the present invention, the wirings are constituted of a lower conductive material and an upper conductive material, and the lower conductive material can be any one of aluminum and an aluminum alloy. In the present invention, the upper conductive material has a passivating potential. The upper conductive material can be any one of molybdenum and a molybdenum alloy.

According to the present invention, provided is a method of manufacturing an array substrate for display, the method comprising the steps of: forming a thin film transistor array including: a plurality of wirings arranged on an insulating substrate; and connection pads arranged on unilateral ends of the wirings and respectively connected with the wirings; forming pixel electrodes; and forming dummy conductive patterns between ends of the connection pads and ends of the pixel electrodes. In the present invention, it is preferable that the dummy conductive patterns be formed so as to occupy 30 area % or more. In the present invention, the dummy conductive patterns can be formed as any of land patterns and line-and-space patterns. In the present invention, the wirings are constituted of a lower conductive material and an upper conductive material, the lower conductive material can be any one of aluminum and an aluminum alloy, and the upper conductive material can be any one of molybdenum and a molybdenum alloy. In the present invention, the wirings are formed by wet etching.

Moreover, in the present invention, provided is a display device, comprising the array substrate for display mentioned above.

In the present invention, the display device used as a liquid crystal display device or an electroluminescence display device can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings.

FIG. **1** is a view showing an embodiment of a liquid crystal display device using an array substrate for display of the present invention.

FIG. **2** is a top plan view of the array substrate for display of the present invention.

FIG. **3** is an enlarged view showing a dummy conductive pattern in the present invention.

FIG. **4** is an enlarged view showing another dummy conductive pattern in the present invention.

FIGS. **5**A to **5**C are views illustrating a method of manufacturing the array substrate for display of the present invention.

FIG. **6** is an electron microscope photograph showing a pattern shape of wiring in the case of using the dummy conductive pattern shown in FIG. **3**.

FIG. **7** is an electron microscope photograph showing a pattern shape of wiring in the case of using the dummy conductive pattern shown in FIG. **4**.

FIG. **8** is a graph showing a relation between a taper angle of the wiring and a pattern density of the wiring.

FIG. **9** is an electron microscope photograph showing a wiring shape in the case of performing etching without using the dummy conductive pattern.

FIG. **10** is an electron microscope photograph showing a sectional shape of the wiring shape shown in FIG. **9**.

FIG. **11** is a schematic view showing a tapered shape of the wiring.

FIGS. **12**A and **12**B are views showing currents formed by a cell formed during an etching process.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinbelow, description will be made in detail for the present invention with reference to embodiments shown in the accompanying drawings. However, the present invention is not limited to the embodiments shown in the drawings.

FIG. **1** is a partially cutaway perspective view showing an embodiment of a display device using an array substrate for display of the present invention. As shown in FIG. **1**, the display device of the present invention is constituted by sequentially laminating a liquid crystal layer **11**, a transparent electrode **12** and a glass substrate **13** on an array substrate **10** for display, which is formed on an insulating substrate. Wiring **14** formed on the insulating substrate **10** is extended to an end (not shown) of the array substrate for display, and is connected with a driving system (not shown) through a connection pad (not shown).

FIG. **2** is a top plan view of the display device using the array substrate **10** for display of the present invention, which is shown in FIG. **1**. In the array substrate **10** for display of the present invention, a plurality of thin film transistors **21** constitute an array. A pixel electrode **22** is connected with each thin film transistor **21** that controls a potential of the pixel electrode. In the array substrate **10** for display shown in FIG. **2**, what is further shown is that a scan line **23** and a signal line **24** are connected with each thin film transistor **21**.

The respective scan lines **23** are connected with a driver **26** through scan line connection pads **25**, and the respective signal lines **24** are connected with a driver **28** through signal line connection pads **27**. These scan lines **23** and the signal lines **24** are formed so as to have the same constitution. As shown in FIG. **11**, each of these lines is constituted of the lower conductive material **3** and the upper conductive material **4**.

In the present invention, aluminum can be used for the lower conductive material **3** usable as wiring from a viewpoint of lowering resistance thereof. Moreover, it is preferable to use molybdenum (Mo) for the upper conductive material **4** usable in the present invention from a viewpoint of protecting the aluminum. However in the present invention, besides the aluminum, an aluminum alloy can be used for the lower conductive material **3**. Moreover, for the

upper conductive material **4**, alloys of chromium, tantalum, titanium and molybdenum can be used. Film thickness of the lower conductive material **3** is not particularly limited, but film thickness of the upper conductive material **4** is preferably thick since a current tends to be concentrated thereto as the film thickness becomes thinner. However, a problem regarding stress occurs as the thickness becomes thicker. Therefore, in the present invention, it is preferable to set the film thickness of the upper conductive material **4** in a range of 30 to 100 nm.

The present invention makes it possible to prevent undercut of the lower conductive material **3**, which occurs due to passivity of the upper conductive material **4**. In the present invention, the term "passivity" is referred to as a phenomenon that metal such as molybdenum or a metal alloy such as a molybdenum alloy becomes insoluble in an acid or alkaline etchant. For example, the term "passivity" is referred to as a phenomenon that metal serving as an anode becomes insoluble in such etchant. In the present invention, specifically as for such passivated metal or a metal alloy, metal or a metal alloy with a passivating potential, that is, a Flade potential can be mentioned. Note that, in the present invention, the Flade potential is referred to as a potential which causes a current density for passivating metal, which is described in the Encyclopedia Chimica (miniature edition 32nd printing, issued by Kyoritsu Shuppan Co., Ltd., edited by editorial committee of the Encyclopedia Chimica), vol. 7, p. 911.

Furthermore, in the embodiment shown in FIG. **2**, dummy conductive patterns **29** are disposed between the pixel electrodes **22** and each scan line connection pad **25** and between the pixel electrodes **22** and each signal line connection pad **27**. Thus, the wiring density is increased. Therefore, it is made possible to form good wiring over the entire surface of the array substrate for display without causing defects such as undercut and a mouse hole of the lower conductive material **3** during etching for the scan lines **23** and the signal lines **24**. Each of these dummy conductive patterns **29** can be formed as a two-layers structure with the same materials as those of the scan lines **23** and the signal lines **24** at the same time when the patterning is performed therefor.

FIG. **3** is an enlarged view showing a portion where the dummy conductive pattern **29** is formed in the embodiment of the array substrate **10** for display of the present invention shown in FIG. **2**. FIG. **3** shows the dummy conductive pattern **29** formed as a line-and-space pattern between the connection pad **25** and an end **30** of the pixel electrode. In the present invention, the dummy conductive pattern **29** can be formed as the line-and-space pattern shown in FIG. **3**. Alternatively, the dummy conductive pattern **29** can be formed as a land pattern completely coating a region where the dummy conductive pattern **29** is formed.

In any case of the patterns, in the present invention, it is preferable that the wiring density of the dummy conductive patterns **29** themselves be 30% or more on an area of a specified surface from a viewpoint of forming a properly tapered shape on the lower conductive material **3** without forming the undercut thereto while dissolving the upper conductive material **4** at a required rate.

Moreover, when the dummy conductive patterns **29** are arranged in the present invention, it is more preferable that the dummy conductive patterns **29** be formed between the end **30** of the pixel electrode **22** and each connection pads **25** and **27** so that the wiring density including the dummy conductive patterns **29** can be 30% or more on the area of a specified surface. In the present invention, the term "wiring density" refers to an area ratio of an area of portions where the signal lines, the scan lines, the drawing lines, and the dummy conductive patterns are formed on an area of a specified region where the dummy conductive patterns are formed.

FIG. **4** is a view showing another embodiment of the dummy conductive pattern **29** of the present invention. In the embodiment shown in FIG. **4**, the dummy conductive pattern **29** is disposed so that the wiring density thereof, which is specified at 30% or more, is further increased, thus reducing concentration of electric current to exposed portions of the upper conductive material to the etchant during the etching. As shown in FIG. **4**, the dummy conductive pattern **29** may have any shapes and any patterns. Moreover, any combination of a plural type of the dummy conductive patterns **29** can be used.

FIGS. **5A**, **5B** and **5C** are views showing an embodiment of a method of manufacturing the array substrate **10** for display of the present invention. With reference to FIG. **5**, description will be made for the method of manufacturing the array substrate **10** for display of the present invention, exemplifying a case where the thin film transistor **21** of a reverse stagger type is formed. First, as shown in FIG. **5A**, the lower conductive material **3** using aluminum and the upper conductive material **4** using molybdenum are deposited on the transparent or untransparent insulating substrate **1**, thus forming a film.

Next, as shown in FIG. **5B**, photoresist **31** is coated on the film. The photoresist is exposed and developed by use of a photo mask **32** provided with patterns for forming the dummy conductive patterns **29** in portions where the wiring density is lowered between the pixel electrodes and the connection pads, which are not particularly shown.

Subsequently, etching is performed by use of an etchant such as a solution of phosphoric acid, nitric acid, acetic acid and mixtures thereof, thus forming the wiring **2** and the dummy conductive patterns **29**. The dummy conductive patterns **29** are arranged in the portions where the wiring density is low. Thus, it is made possible to form wirings having good tapered shape as shown in FIG. **5C** even in regions where the conductive material such as molybdenum tends to be passivated. A taper angle can be set in a range of 20 degrees to 70 degrees by adjusting a composition of the etchant and etching conditions. It is more preferable to set the taper angle in a range of about 20 degrees to about 60 degrees.

Thereafter, in the present invention, gate insulating films, the gate electrodes, the source electrodes, the drain electrodes, the pixel electrodes and the like are formed, thus the array substrate **10** for display of the present invention is manufactured. In the present invention, the dummy conductive patterns **29** may be removed if necessary. Alternatively, the dummy conductive patterns **29** may be left as they are without being eliminated.

FIG. **6** is an electron microscope photograph showing a shape of the wiring **33** shown in FIG. **3**, which was obtained when the dummy conductive pattern **29** shown in FIG. **3** was provided and the etching was performed. In this case, molybdenum was used for the upper conductive material **4**, and aluminum was used for the lower conductive material **3**. The film thickness of molybdenum is about 50 nm, and wet etching is performed by use of an etchant of a mixed solution of phosphoric acid, nitric acid and acetic acid. As shown in FIG. **6**, a good tapered shape is formed even in a wiring portion where the undercut is formerly apt to occur by forming the dummy conductive pattern **29**.

FIG. 7 is a photograph showing a shape of the wiring 34 shown in FIG. 4, which was obtained when the dummy conductive pattern 29 shown in FIG. 4 was formed and the etching was performed under the same conditions as those in FIG. 6. As shown in FIG. 7, even when the density of the dummy conductive pattern 29 is increased, a good tapered shape is obtained.

FIG. 8 is a graph plotting values of the taper angle of the formed wiring relative to values of the pattern density (area %) of the wiring including the portions of the dummy conductive patterns 29 on the substrate when the dummy conductive patterns 29 are arranged. As shown in FIG. 8, the taper angle of the wiring obtained by the etching is reduced as the pattern density of the wiring is increased, and a more gentle taper is formed. Therefore, it is understood that the upper conductive material 4 can impart a sufficient selective ratio to the etching of the lower conductive material 3 by arranging the dummy conductive patterns 29.

FIG. 9 is an electron microscope photograph showing, for comparison, a shape of wiring obtained when etching is performed by use of the array substrate 10 for display, which has the same pattern as those shown in FIGS. 3 and 4, but without forming the dummy conductive patterns 29 at all. As shown in FIG. 9, large undercut occurs in the wiring since the molybdenum used for the upper conductive material 4 is passivated, and only the etching for the aluminum as the lower conductive material 3 progresses.

FIG. 10 is an electron microscope photograph showing a cross section taken along a cutting plane line A—A of the wiring shown in FIG. 9. As shown in FIG. 10, the etching for the aluminum used for the lower conductive material 3 progresses more than that for the molybdenum used for the upper conductive material 4, resulting in the occurrence of the great undercut.

The present invention can be applied not only to the thin film transistor of a reverse stagger type as described above but also to a thin film transistor of a top gate type including wiring formed of aluminum and any metal other than the aluminum, of which passivating current density is known.

Moreover, although the array device for display of the present invention can be applied to a liquid crystal display device using a transparent insulating substrate made of such as glass, the array device for display of the present invention can be also used as an organic or inorganic electroluminescence device, wherein an untransparent insulating substrate is used and an array for display is formed on the insulating substrate.

As described above, according to the present invention, it is made possible to provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of being etched at a sufficiently high etching rate and a sufficient selection ratio, and eliminating the under cut and the lowering of a yield in manufacturing due to the inconvenience such as an interlayer short circuit. Moreover, according to the present invention, it is made possible to provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of providing a large-sized and high-resolution display device.

Although the preferred embodiments of the present invention have been described in detail, it should be understood that various changes, substitutions and alternations can be made therein without departing from spirit and scope of the inventions as defined by the appended claims.

What is claimed is:

1. An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

2. The array substrate for display according to claim 1 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

3. The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.

4. The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

5. The array substrate for display according to claim 3 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

6. The array substrate for display according to claim 5 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

7. The array substrate for display according to claim 4 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

8. The array substrate for display according to claim 5 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

9. A meted for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array formed on the insulating substrate, each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

10. The method for forming an array substrate for display according to claim 9 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

11. The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring materials is selected from the group consisting of aluminum and aluminum alloys.

12. The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

13. The method for forming an array substrate for display according to claim 11 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and allays thereof.

14. The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

15. The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

16. The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

* * * * *

US006689629B2

(12) **United States Patent**
Tsujimura et al.

(10) Patent No.: **US 6,689,629 B2**
(45) Date of Patent: **Feb. 10, 2004**

(54) **ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE**

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(73) Assignee: International Business Machines Corporation, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 54 days.

(21) Appl. No.: 10/068,500

(22) Filed: Feb. 5, 2002

(65) Prior Publication Data

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(30) Foreign Application Priority Data

Feb. 6, 2001 (JP) 2001-029587

(51) Int. Cl.[7] H01L 21/00

(52) U.S. Cl. 438/25; 438/149; 438/73; 257/72; 257/748

(58) Field of Search 438/25, 22, 30, 438/149, 73; 257/72, 748

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Primary Examiner—Caridad Everhart
(74) *Attorney, Agent, or Firm*—Tiffany L. Townsend

(57) ABSTRACT

Disclosed is to provide an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display.

The present invention is an array substrate for display, which includes: a thin film transistor array formed on an insulating substrate 1; a plurality of wirings 23 and 24 arranged on the insulating substrate 1; connection pads 25 and 27 arranged on unilateral ends of the wirings 23 and 24 and respectively connected therewith; and pixel electrodes 22, wherein dummy conductive patterns 29 are arranged between the ends of the connection pads 25 and 27 and ends of the pixel electrodes 22.

16 Claims, 11 Drawing Sheets

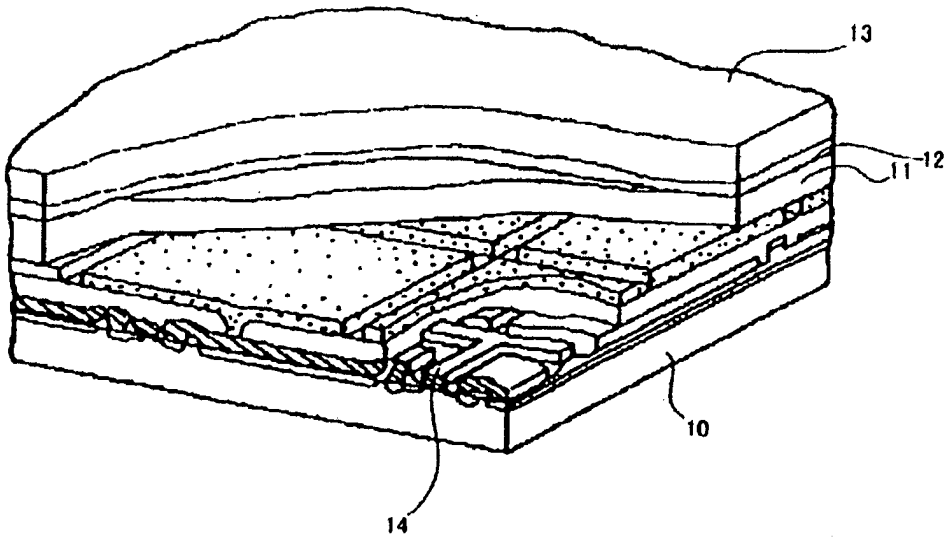

FIG. 1

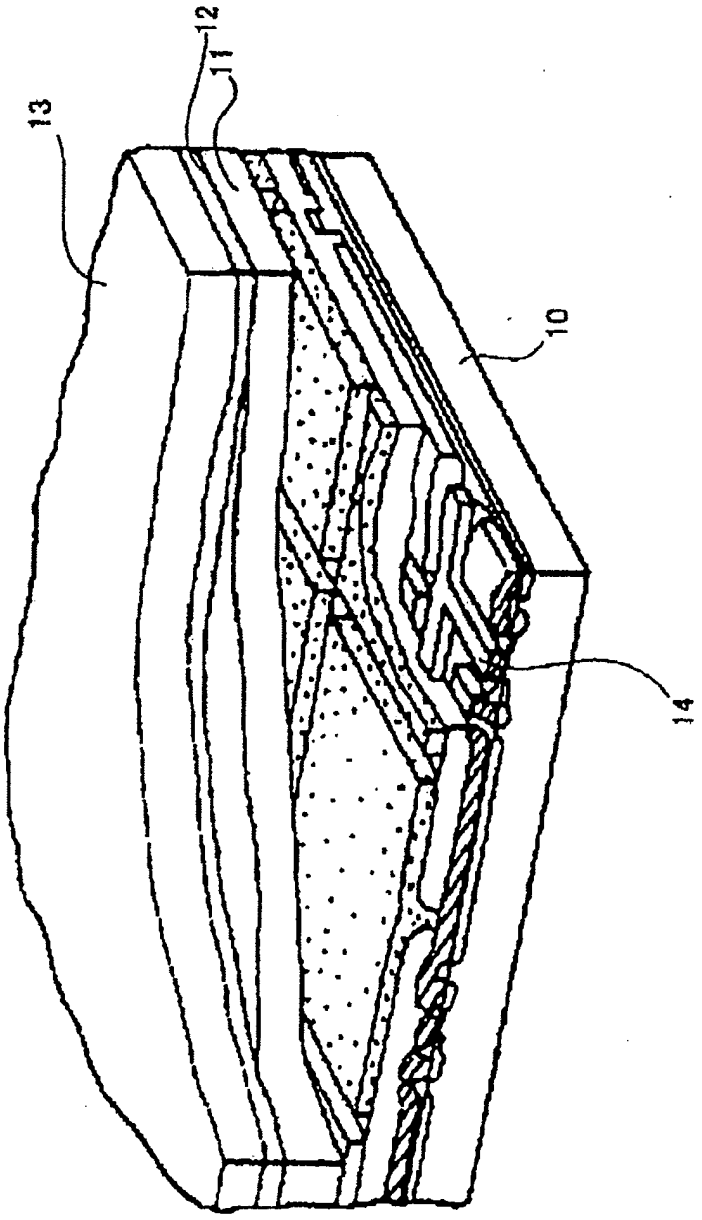

FIG. 2

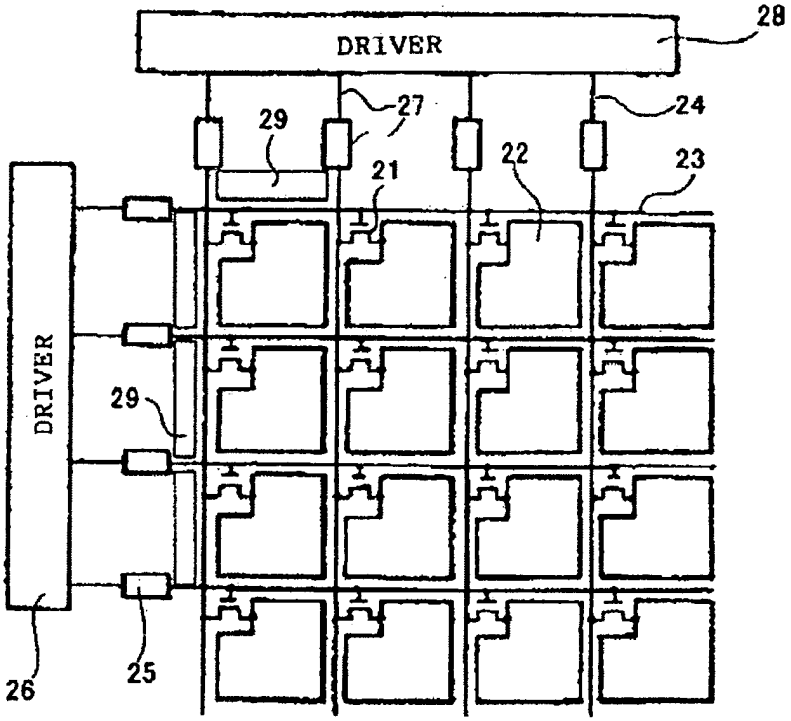

FIG. 3

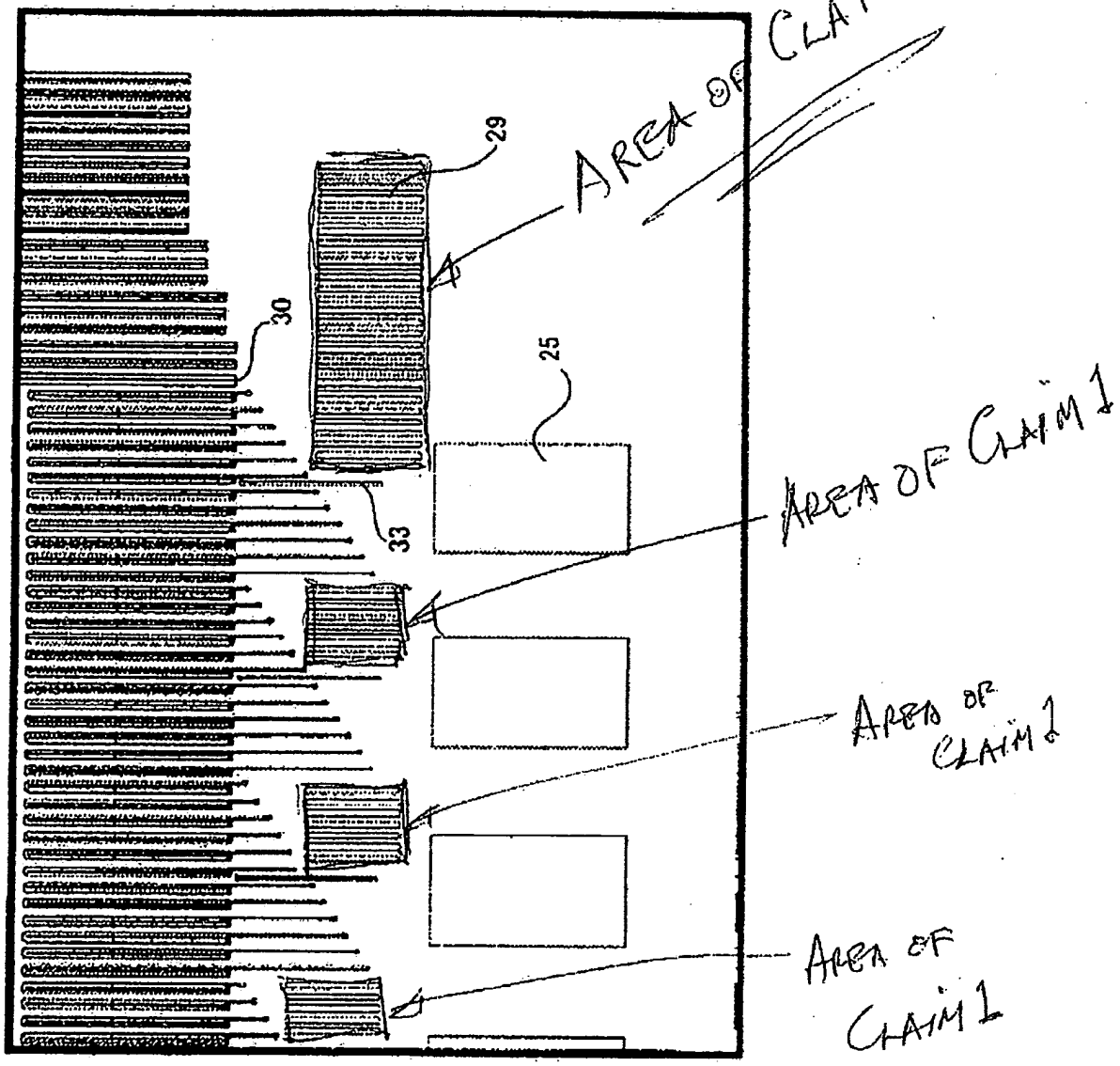
29
30
25
33
AREA OF CLAIM 1
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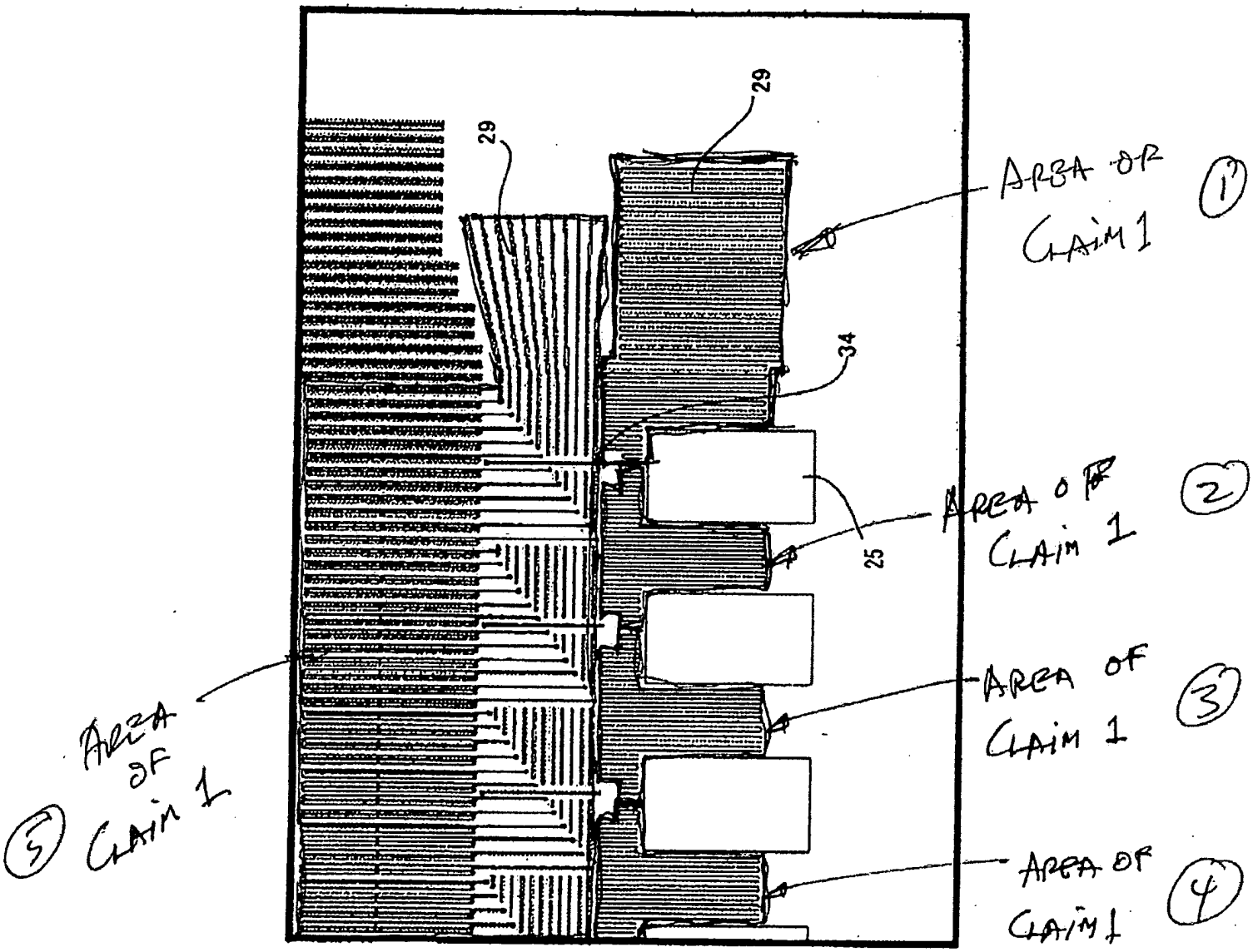
FIG. 4


29
29
34
25
AREA OF CLAIM 1
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AREA OF CLAIM 1
2
AREA OF CLAIM 1
3
AREA OF CLAIM 1
4
AREA OF CLAIM 1
5

FIG. 5

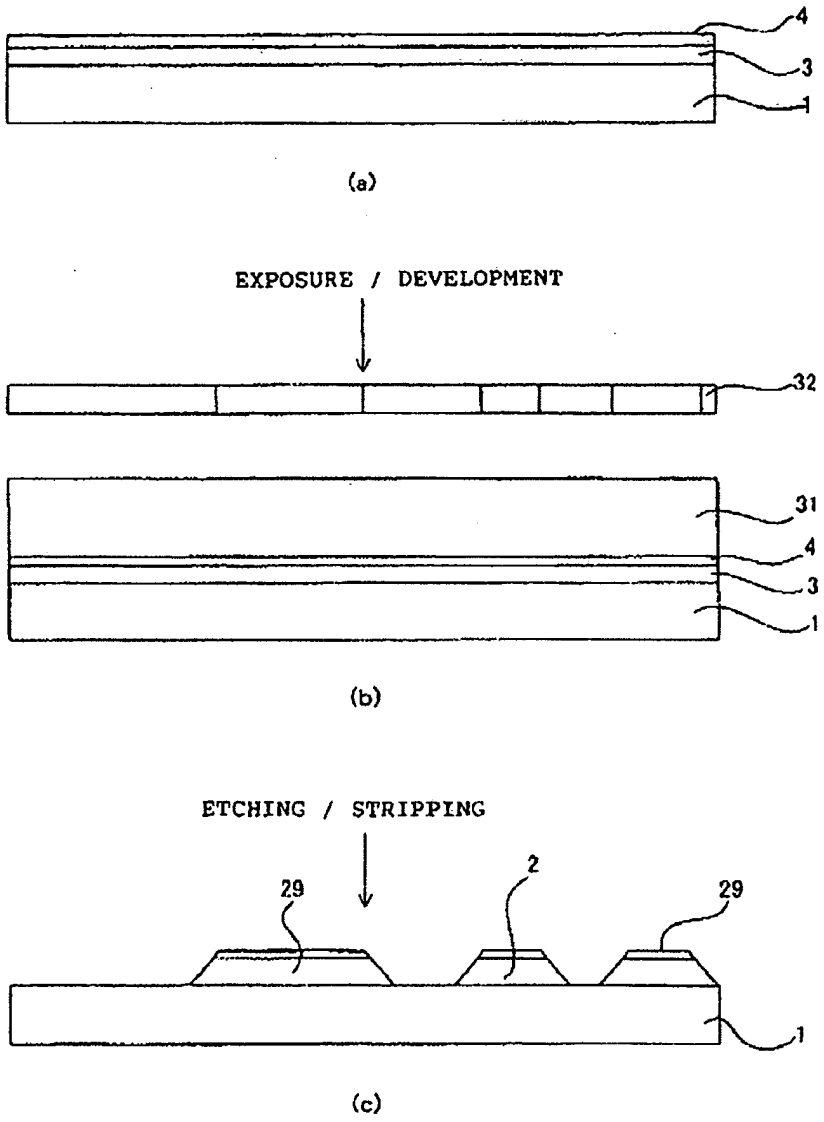

4
3
1
(a)
EXPOSURE / DEVELOPMENT
32
31
4
3
1
(b)
ETCHING / STRIPPING
29
2
29
1
(c)

FIG. 6

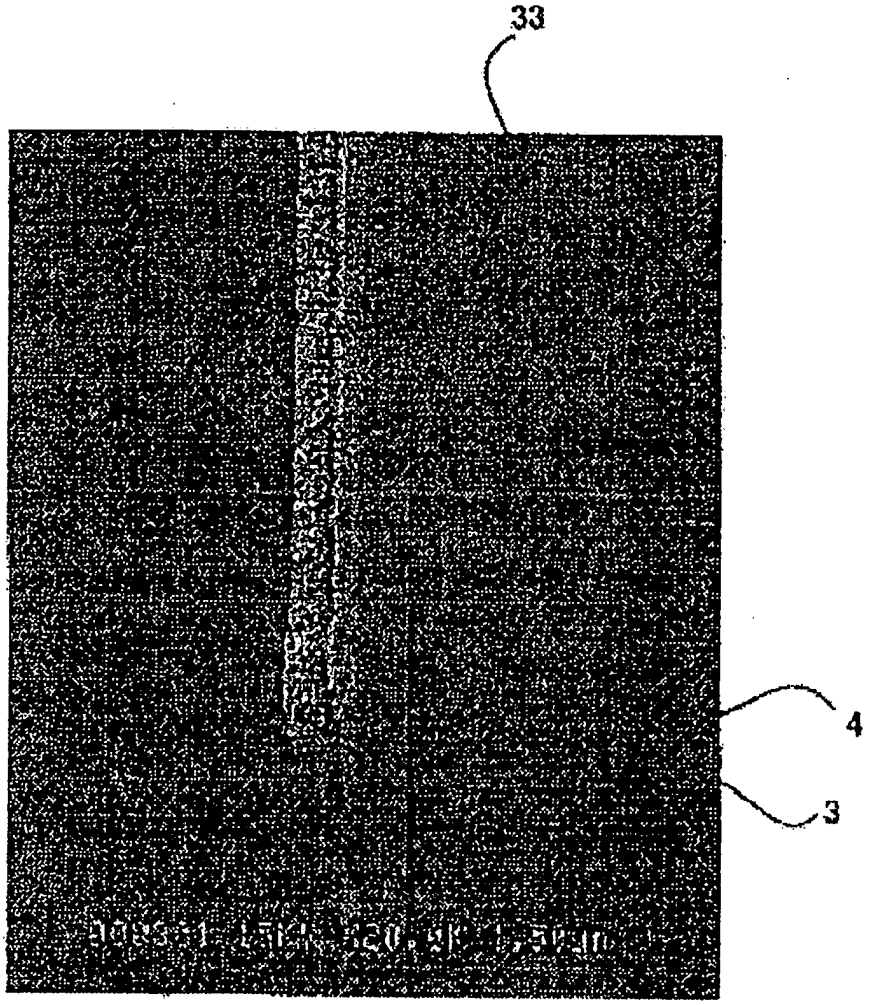


FIG. 7

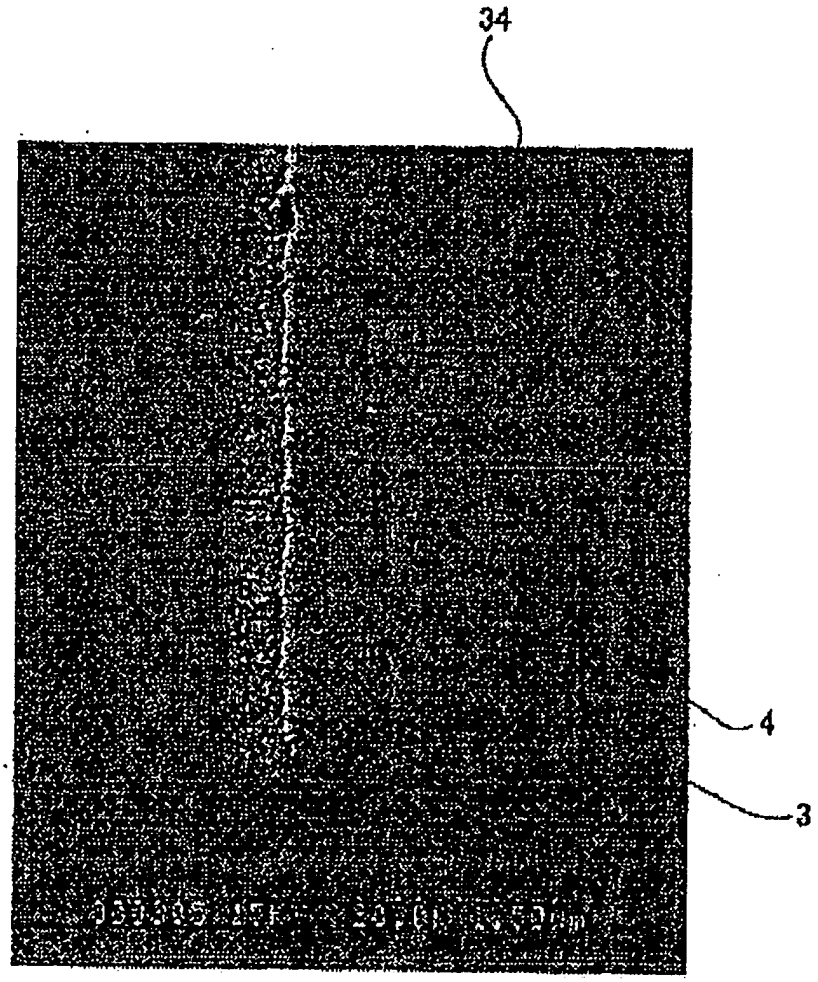


FIG. 8

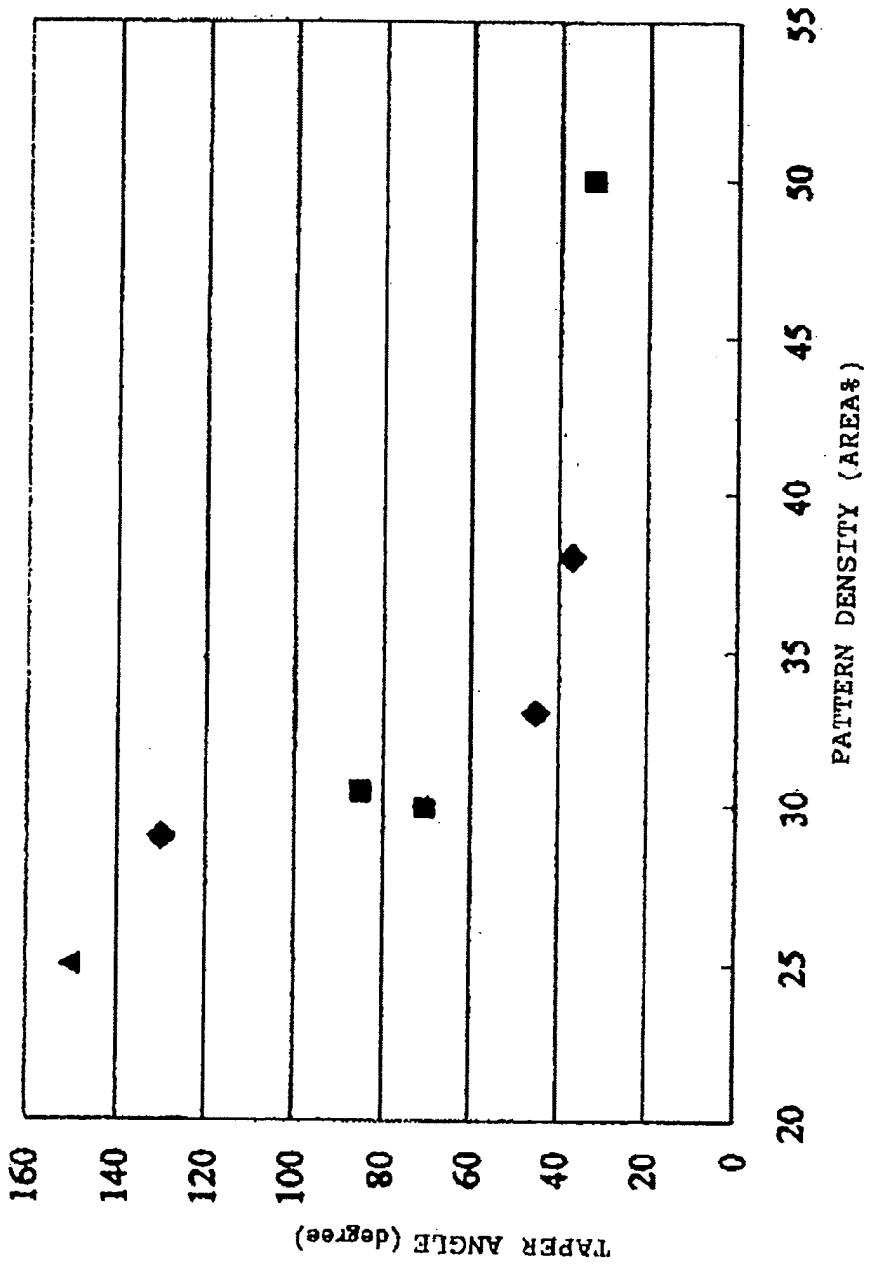

PATTERN DENSITY (AREA%)
20
25
30
35
40
45
50
55
TAPER ANGLE (degree)
160
140
120
100
80
60
40
20
0

FIG. 9

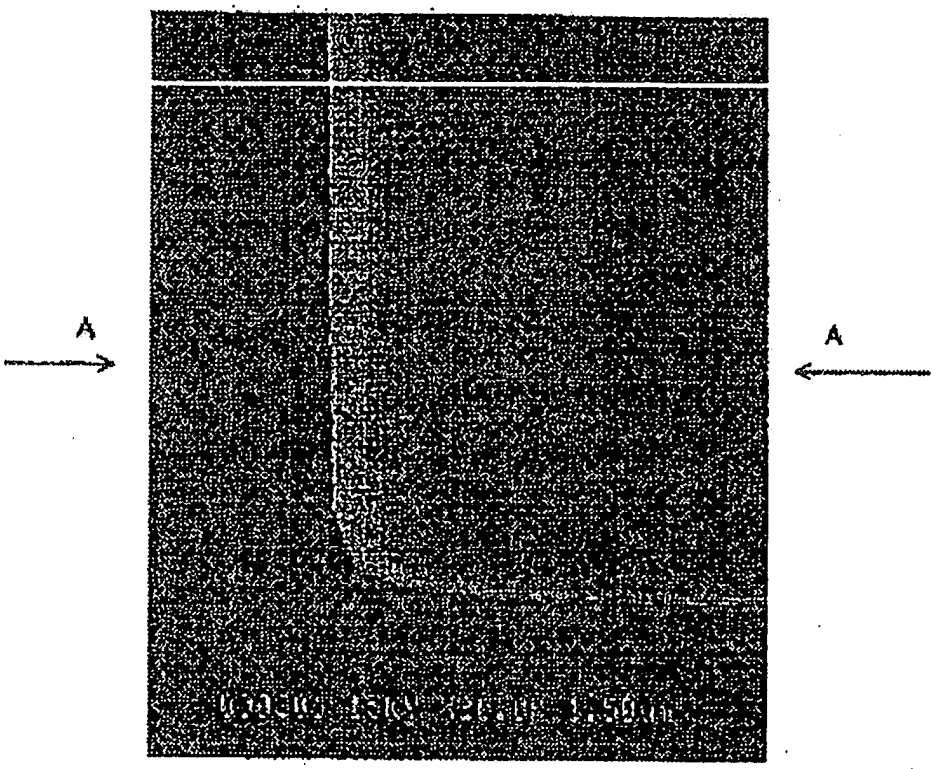


FIG. 10

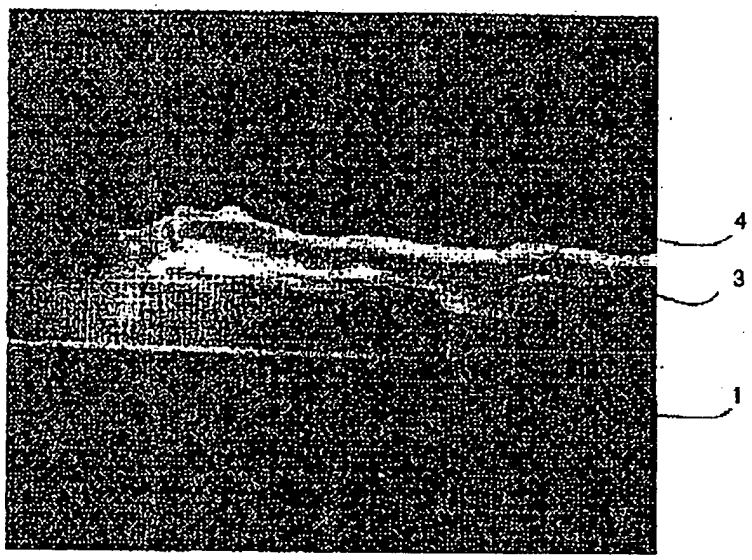


FIG. 11

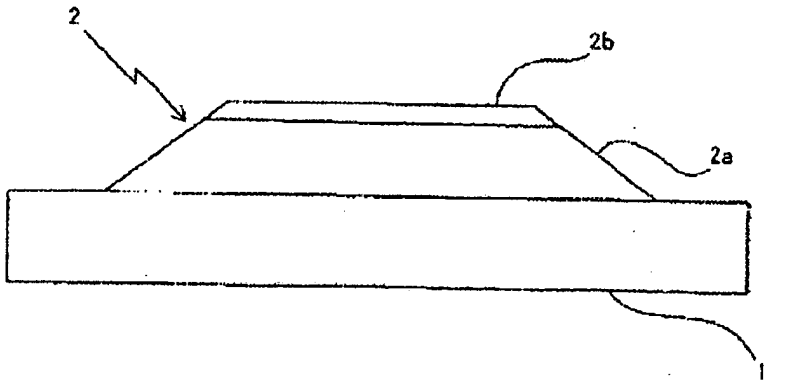
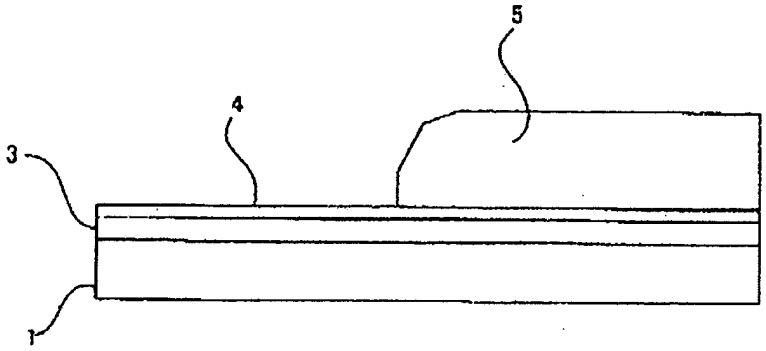
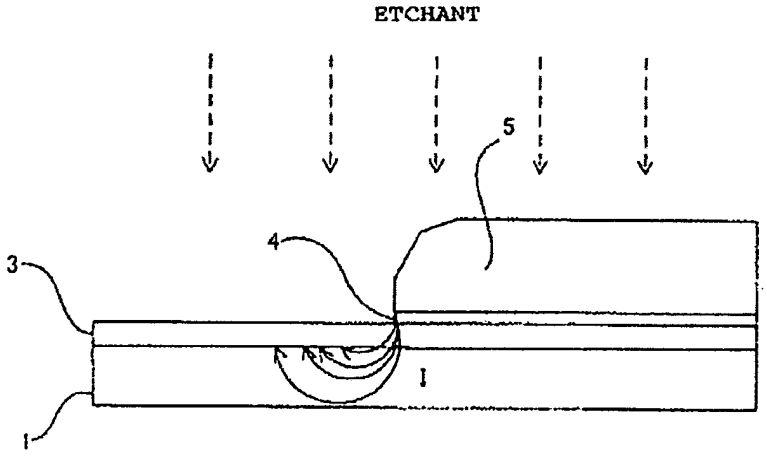


FIG. 12



(a)



(b)

ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

BACKGROUND OF THE INVENTION

The present invention relates to an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display.

A display device using a thin film transistor (TFT) array has been frequently used owing to low power consumption and capability of downsizing the display device. The thin film transistor array is manufactured by forming thin film transistors, each being composed of electrodes such as a gate electrode, a source electrode and a drain electrode, wirings such as scan lines and signal lines connected with the above-mentioned electrodes, and pixel electrodes on an insulating substrate.

In recent years, a higher operating speed, a higher resolution and a larger size have been required for the display device described above in many cases. A high speed and a high density have been required for each constituent component of the array for display, which forms a display device. Particularly, in order to operate the thin film transistor array at a high speed, it is preferable to use low-resistance aluminum (Al) for the wirings such as the scan lines and the signal lines since delay in gate pulses can be reduced and a writing speed to the thin film transistor can be increased.

Incidentally, aluminum tends to be easily oxidized in spite of its low resistance. Therefore, in many cases, wiring using aluminum is constituted as a two-layer structure, in which aluminum is used as a lower conductive material, and a material harder to be oxidized than aluminum such as chromium, tantalum, titanium or molybdenum is used as an upper conductive material. FIG. 11 is a view schematically showing a state where wiring 2 is deposited on an insulating substrate 1. A lower conductive material film 2*a* is deposited on an insulating substrate 1 made of such as glass, and an upper conductive material film 2*b* is deposited on the lower conductive material film 2*a*. Each of these films 2*a* and 2*b* is patterned by, for example, a proper etching process so as to have tapered ends.

In order to form a tapered shape shown in FIG. 11, an etching rate for the upper conductive material is required to be increased. In order to form the tapered shape shown in FIG. 11, various methods have been proposed up to now. For example, in the gazette of Japanese Patent Laid-Open No. Hei 10 (1998)-90706, a method has been proposed, in which dummy connection pads are provided on sides opposite to scan line connection pads and signal line connection pads, respectively. According to this method, over etching due to an etchant that will be relatively increased by lowering wiring density at ends of the substrate is prevented. Thus, undercut of a lower conductive material 3 is prevented, and an interlayer short circuit is prevented by imparting a proper tapered shape to the wiring 2.

However, though this method enables evenness of etching at the ends of the thin film transistor array substrate to be improved, the method cannot effectively prevent the undercut of the signal lines in a region where the wiring density is apt to be lowered from ends of the pixel electrodes to the connection pads, for example, in a portion where drawing wiring is formed.

Moreover, in the gazette of Japanese Patent Laid-Open No. Hei 10 (1998)-240150, disclosed is a method of forming a tapered shape at an angle ranging from 20 degrees to 70 degrees on wiring constituted of two layers, in which a pad formed of aluminum and metal such as molybdenum formed on the aluminum is subjected to wet etching. According to this method, a specified tapered shape can be imparted to the wiring formed of a conductive film of a two-layer structure by the wet etching. However, the method never discloses a method of evenly etching a substrate region while maintaining a selection ratio thereof even in the substrate region where the wiring density is lowered.

FIGS. 12A and 12B are enlarged schematic views for explaining a patterning process using a conventionally used wet process in order to impart the above-described tapered shape to the wiring. As shown in FIG. 12A, the lower conductive material 3 and an upper conductive material 4 are deposited on the insulating substrate 1 by a method such as physical vapor deposition. FIG. 12A shows that a photoresist film 5 is coated on a film of the upper conductive material 4 and is patterned in a desired shape. The respective films are etched by an etchant such as a solution of phosphoric acid, nitric acid, acetic acid or mixtures thereof, and desired tapered shapes are formed thereon.

FIG. 12B is a view for explaining an electrochemical process generated as each film is being etched when the wiring constituted of the upper conductive material 4 and the lower conductive material 3 is subjected to wet etching. In FIG. 12B, an internal layer portion of the upper conductive material 4 coated with the photoresist film 5 is not dissolved. However, at the end of the photoresist film 5, the upper conductive material 4 is dissolved by the etchant. When the wiring is formed by the wet etching, the upper conductive material 4 protected by the photoresist film 5 is further dissolved in a lateral direction from the end of the photoresist film 5 to turn into positive ions, and electrons emitted as a result are supplied to the lower conductive material 3. Thus, the upper conductive material 4 serves as an anode. In this connection, the lower conductive material 3 comes to serve as a cathode. Accordingly, an electrochemical cell is formed. Here, when the etching rate for the upper conductive material 4 is increased to form a required tapered shape, the density of the electrons generated by dissolving the upper conductive material 4 and flowing to the lower conductive material 3 is increased accompanied with an increase of a dissolution rate of the upper conductive material 4. FIG. 12B schematically shows currents I flowing from the upper conductive material 4 to the lower conductive material 3.

As the etching rate is increased, the density of the current flowing to an area of the upper conductive material 4, which is exposed to the etchant, exceeds a current density causing passivity of the upper conductive material 4. In such a case, the upper conductive material 4 is passivated not to be dissolved by the etchant, and only the lower conductive material 3 is dissolved accompanied with the progress of the etching, resulting in the occurrence of the undercut. When such undercut occurs, the wiring, for example, the gate wiring cannot be sufficiently coated with an insulating film in some cases, thus causing inconvenience such as an interlayer short circuit, resulting in lowering a yield of the display device.

SUMMARY OF THE INVENTION

The present invention was made with the foregoing problems in mind. An object of the present invention is to

provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of being etched at a sufficiently high etching rate and a sufficient selection ratio, eliminating undercut, and providing a large-sized and high-resolution display device.

The foregoing object of the present invention is achieved by providing the array substrate for display, the method of manufacturing an array substrate for display and the display device using the array substrate for display of the present invention.

Specifically, according to the present invention, provided is an array substrate for display, comprising: a thin film transistor array formed on an insulating substrate; a plurality of wirings arranged on the insulating substrate; connection pads arranged on unilateral ends of the wirings and respectively connected with the wirings; pixel electrodes, and dummy conductive patterns arranged between the ends of the connection pads and ends of the pixel electrodes. The dummy conductive patterns can occupy 30 area % or more. In the present invention, the dummy conductive patterns can be formed as any of land patterns and line-and-space patterns. In the present invention, the wirings are constituted of a lower conductive material and an upper conductive material, and the lower conductive material can be any one of aluminum and an aluminum alloy. In the present invention, the upper conductive material has a passivating potential. The upper conductive material can be any one of molybdenum and a molybdenum alloy.

According to the present invention, provided is a method of manufacturing an array substrate for display, the method comprising the steps of: forming a thin film transistor array including: a plurality of wirings arranged on an insulating substrate; and connection pads arranged on unilateral ends of the wirings and respectively connected with the wirings; forming pixel electrodes; and forming dummy conductive patterns between ends of the connection pads and ends of the pixel electrodes. In the present invention, it is preferable that the dummy conductive patterns be formed so as to occupy 30 area % or more. In the present invention, the dummy conductive patterns can be formed as any of land patterns and line-and-space patterns. In the present invention, the wirings are constituted of a lower conductive material and an upper conductive material, the lower conductive material can be any one of aluminum and an aluminum alloy, and the upper conductive material can be any one of molybdenum and a molybdenum alloy. In the present invention, the wirings are formed by wet etching.

Moreover, in the present invention, provided is a display device, comprising the array substrate for display mentioned above.

In the present invention, the display device used as a liquid crystal display device or an electroluminescence display device can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings.

FIG. 1 is a view showing an embodiment of a liquid crystal display device using an array substrate for display of the present invention.

FIG. 2 is a top plan view of the array substrate for display of the present invention.

FIG. 3 is an enlarged view showing a dummy conductive pattern in the present invention.

FIG. 4 is an enlarged view showing another dummy conductive pattern in the present invention.

FIGS. 5A to 5C are views illustrating a method of manufacturing the array substrate for display of the present invention.

FIG. 6 is an electron microscope photograph showing a pattern shape of wiring in the case of using the dummy conductive pattern shown in FIG. 3.

FIG. 7 is an electron microscope photograph showing a pattern shape of wiring in the case of using the dummy conductive pattern shown in FIG. 4.

FIG. 8 is a graph showing a relation between a taper angle of the wiring and a pattern density of the wiring.

FIG. 9 is an electron microscope photograph showing a wiring shape in the case of performing etching without using the dummy conductive pattern.

FIG. 10 is an electron microscope photograph showing a sectional shape of the wiring shape shown in FIG. 9.

FIG. 11 is a schematic view showing a tapered shape of the wiring.

FIGS. 12A and 12B are views showing currents formed by a cell formed during an etching process.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinbelow, description will be made in detail for the present invention with reference to embodiments shown in the accompanying drawings. However, the present invention is not limited to the embodiments shown in the drawings.

FIG. 1 is a partially cutaway perspective view showing an embodiment of a display device using an array substrate for display of the present invention. As shown in FIG. 1, the display device of the present invention is constituted by sequentially laminating a liquid crystal layer 11, a transparent electrode 12 and a glass substrate 13 on an array substrate 10 for display, which is formed on an insulating substrate. Wiring 14 formed on the insulating substrate 10 is extended to an end (not shown) of the array substrate for display, and is connected with a driving system (not shown) through a connection pad (not shown).

FIG. 2 is a top plan view of the display device using the array substrate 10 for display of the present invention, which is shown in FIG. 1. In the array substrate 10 for display of the present invention, a plurality of thin film transistors 21 constitute an array. A pixel electrode 22 is connected with each thin film transistor 21 that controls a potential of the pixel electrode. In the array substrate 10 for display shown in FIG. 2, what is further shown is that a scan line 23 and a signal line 24 are connected with each thin film transistor 21.

The respective scan lines 23 are connected with a driver 26 through scan line connection pads 25, and the respective signal lines 24 are connected with a driver 28 through signal line connection pads 27. These scan lines 23 and the signal lines 24 are formed so as to have the same constitution. As shown in FIG. 11, each of these lines is constituted of the lower conductive material 3 and the upper conductive material 4.

In the present invention, aluminum can be used for the lower conductive material 3 usable as wiring from a viewpoint of lowering resistance thereof. Moreover, it is preferable to use molybdenum (Mo) for the upper conductive material 4 usable in the present invention from a viewpoint of protecting the aluminum. However in the present invention, besides the aluminum, an aluminum alloy can be used for the lower conductive material 3. Moreover, for the

upper conductive material 4, alloys of chromium, tantalum, titanium and molybdenum can be used. Film thickness of the lower conductive material 3 is not particularly limited, but film thickness of the upper conductive material 4 is preferably thick since a current tends to be concentrated thereto as the film thickness becomes thinner. However, a problem regarding stress occurs as the thickness becomes thicker. Therefore, in the present invention, it is preferable to set the film thickness of the upper conductive material 4 in a range of 30 to 100 nm.

The present invention makes it possible to prevent undercut of the lower conductive material 3, which occurs due to passivity of the upper conductive material 4. In the present invention, the term "passivity" is referred to as a phenomenon that metal such as molybdenum or a metal alloy such as a molybdenum alloy becomes insoluble in an acid or alkaline etchant. For example, the term "passivity" is referred to as a phenomenon that metal serving as an anode becomes insoluble in such etchant. In the present invention, specifically as for such passivated metal or a metal alloy, metal or a metal alloy with a passivating potential, that is, a Flade potential can be mentioned. Note that, in the present invention, the Flade potential is referred to as a potential which causes a current density for passivating metal, which is described in the Encyclopedia Chimica (miniature edition 32nd printing, issued by Kyoritsu Shuppan Co., Ltd., edited by editorial committee of the Encyclopedia Chimica), vol. 7, p. 911.

Furthermore, in the embodiment shown in FIG. 2, dummy conductive patterns 29 are disposed between the pixel electrodes 22 and each scan line connection pad 25 and between the pixel electrodes 22 and each signal line connection pad 27. Thus, the wiring density is increased. Therefore, it is made possible to form good wiring over the entire surface of the array substrate for display without causing defects such as undercut and a mouse hole of the lower conductive material 3 during etching for the scan lines 23 and the signal lines 24. Each of these dummy conductive patterns 29 can be formed as a two-layers structure with the same materials as those of the scan lines 23 and the signal lines 24 at the same time when the patterning is performed therefor.

FIG. 3 is an enlarged view showing a portion where the dummy conductive pattern 29 is formed in the embodiment of the array substrate 10 for display of the present invention shown in FIG. 2. FIG. 3 shows the dummy conductive pattern 29 formed as a line-and-space pattern between the connection pad 25 and an end 30 of the pixel electrode. In the present invention, the dummy conductive pattern 29 can be formed as the line-and-space pattern shown in FIG. 3. Alternatively, the dummy conductive pattern 29 can be formed as a land pattern completely coating a region where the dummy conductive pattern 29 is formed.

In any case of the patterns, in the present invention, it is preferable that the wiring density of the dummy conductive patterns 29 themselves be 30% or more on an area of a specified surface from a viewpoint of forming a properly tapered shape on the lower conductive material 3 without forming the undercut thereto while dissolving the upper conductive material 4 at a required rate.

Moreover, when the dummy conductive patterns 29 are arranged in the present invention, it is more preferable that the dummy conductive patterns 29 be formed between the end 30 of the pixel electrode 22 and each connection pads 25 and 27 so that the wiring density including the dummy conductive patterns 29 can be 30% or more on the area of a specified surface. In the present invention, the term "wiring density" refers to an area ratio of an area of portions where the signal lines, the scan lines, the drawing lines, and the dummy conductive patterns are formed on an area of a specified region where the dummy conductive patterns are formed.

FIG. 4 is a view showing another embodiment of the dummy conductive pattern 29 of the present invention. In the embodiment shown in FIG. 4, the dummy conductive pattern 29 is disposed so that the wiring density thereof, which is specified at 30% or more, is further increased, thus reducing concentration of electric current to exposed portions of the upper conductive material to the etchant during the etching. As shown in FIG. 4, the dummy conductive pattern 29 may have any shapes and any patterns. Moreover, any combination of a plural type of the dummy conductive patterns 29 can be used.

FIGS. 5A, 5B and 5C are views showing an embodiment of a method of manufacturing the array substrate 10 for display of the present invention. With reference to FIG. 5, description will be made for the method of manufacturing the array substrate 10 for display of the present invention, exemplifying a case where the thin film transistor 21 of a reverse stagger type is formed. First, as shown in FIG. 5A, the lower conductive material 3 using aluminum and the upper conductive material 4 using molybdenum are deposited on the transparent or untransparent insulating substrate 1, thus forming a film.

Next, as shown in FIG. 5B, photoresist 31 is coated on the film. The photoresist is exposed and developed by use of a photo mask 32 provided with patterns for forming the dummy conductive patterns 29 in portions where the wiring density is lowered between the pixel electrodes and the connection pads, which are not particularly shown.

Subsequently, etching is performed by use of an etchant such as a solution of phosphoric acid, nitric acid, acetic acid and mixtures thereof, thus forming the wiring 2 and the dummy conductive patterns 29. The dummy conductive patterns 29 are arranged in the portions where the wiring density is low. Thus, it is made possible to form wirings having good tapered shape as shown in FIG. 5C even in regions where the conductive material such as molybdenum tends to be passivated. A taper angle can be set in a range of 20 degrees to 70 degrees by adjusting a composition of the etchant and etching conditions. It is more preferable to set the taper angle in a range of about 20 degrees to about 60 degrees.

Thereafter, in the present invention, gate insulating films, the gate electrodes, the source electrodes, the drain electrodes, the pixel electrodes and the like are formed, thus the array substrate 10 for display of the present invention is manufactured. In the present invention, the dummy conductive patterns 29 may be removed if necessary. Alternatively, the dummy conductive patterns 29 may be left as they are without being eliminated.

FIG. 6 is an electron microscope photograph showing a shape of the wiring 33 shown in FIG. 3, which was obtained when the dummy conductive pattern 29 shown in FIG. 3 was provided and the etching was performed. In this case, molybdenum was used for the upper conductive material 4, and aluminum was used for the lower conductive material 3. The film thickness of molybdenum is about 50 nm, and wet etching is performed by use of an etchant of a mixed solution of phosphoric acid, nitric acid and acetic acid. As shown in FIG. 6, a good tapered shape is formed even in a wiring portion where the undercut is formerly apt to occur by forming the dummy conductive pattern 29.

FIG. 7 is a photograph showing a shape of the wiring 34 shown in FIG. 4, which was obtained when the dummy conductive pattern 29 shown in FIG. 4 was formed and the etching was performed under the same conditions as those in FIG. 6. As shown in FIG. 7, even when the density of the dummy conductive pattern 29 is increased, a good tapered shape is obtained.

FIG. 8 is a graph plotting values of the taper angle of the formed wiring relative to values of the pattern density (area %) of the wiring including the portions of the dummy conductive patterns 29 on the substrate when the dummy conductive patterns 29 are arranged. As shown in FIG. 8, the taper angle of the wiring obtained by the etching is reduced as the pattern density of the wiring is increased, and a more gentle taper is formed. Therefore, it is understood that the upper conductive material 4 can impart a sufficient selective ratio to the etching of the lower conductive material 3 by arranging the dummy conductive patterns 29.

FIG. 9 is an electron microscope photograph showing, for comparison, a shape of wiring obtained when etching is performed by use of the array substrate 10 for display, which has the same pattern as those shown in FIGS. 3 and 4, but without forming the dummy conductive patterns 29 at all. As shown in FIG. 9, large undercut occurs in the wiring since the molybdenum used for the upper conductive material 4 is passivated, and only the etching for the aluminum as the lower conductive material 3 progresses.

FIG. 10 is an electron microscope photograph showing a cross section taken along a cutting plane line A—A of the wiring shown in FIG. 9. As shown in FIG. 10, the etching for the aluminum used for the lower conductive material 3 progresses more than that for the molybdenum used for the upper conductive material 4, resulting in the occurrence of the great undercut.

The present invention can be applied not only to the thin film transistor of a reverse stagger type as described above but also to a thin film transistor of a top gate type including wiring formed of aluminum and any metal other than the aluminum, of which passivating current density is known.

Moreover, although the array device for display of the present invention can be applied to a liquid crystal display device using a transparent insulating substrate made of such as glass, the array device for display of the present invention can be also used as an organic or inorganic electroluminescence device, wherein an untransparent insulating substrate is used and an array for display is formed on the insulating substrate.

As described above, according to the present invention, it is made possible to provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of being etched at a sufficiently high etching rate and a sufficient selection ratio, and eliminating the under cut and the lowering of a yield in manufacturing due to the inconvenience such as an interlayer short circuit. Moreover, according to the present invention, it is made possible to provide an array substrate for display, a method of manufacturing an array substrate for display and a display device using the array substrate for display, which are capable of providing a large-sized and high-resolution display device.

Although the preferred embodiments of the present invention have been described in detail, it should be understood that various changes, substitutions and alternations can be made therein without departing from spirit and scope of the inventions as defined by the appended claims.

What is claimed is:

1. An array substrate for display, comprising:

a layer of an insulating substrate, having an area;

a thin film transistor array formed on the insulating substrate;

a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array;

connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

pixel electrodes, and

dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

2. The array substrate for display according to claim 1 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

3. The array substrate for display according to claim 2 wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.

4. The array substrate for display according to claim 2 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

5. The array substrate for display according to claim 3 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

6. The array substrate for display according to claim 5 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

7. The array substrate for display according to claim 4 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

8. The array substrate for display according to claim 5 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

9. A meted for forming an array substrate for display, comprising:

forming a layer of an insulating substrate, having an area;

forming a thin film transistor array formed on the insulating substrate, each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array;

forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming pixel electrodes, and

forming dummy conductive patterns, the dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

10. The method for forming an array substrate for display according to claim 9 wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials.

11. The method for forming an array substrate for display according to claim 10 wherein the lower layer wiring materials is selected from the group consisting of aluminum and aluminum alloys.

12. The method for forming an array substrate for display according to claim 10 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

13. The method for forming an array substrate for display according to claim 11 wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof.

14. The method for forming an array substrate for display according to claim 13 wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

15. The method for forming an array substrate for display according to claim 12 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

16. The method for forming an array substrate for display according to claim 13 wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

* * * * *

Patent Assignment Abstract of Title

Total Assignments: 2

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PCT #: NONE **Publication #:** US20020106843 **Pub Dt:** 08/08/2002

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Title: ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

Assignment: 1

Reel/Frame: 016926 / 0247 **Received:** 12/21/2005 **Recorded:** 12/21/2005 **Mailed:** 12/21/2005 **Pages:** 17

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

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Date Mailed: 03/10/10

NOTICE OF FAILURE TO COMPLY WITH *EX PARTE* REEXAMINATION REQUEST FILING REQUIREMENTS (37 CFR 1.510(c))

The Central Reexamination Unit (CRU) in the United States Patent and Trademark Office (USPTO) has received a request for *ex parte* reexamination. The request cannot be processed, because the below-identified filing date requirements for an *ex parte* reexamination request have not been satisfied. If a fully compliant response is not received within 30 days of the mailing date of this notice, the request will be treated as a prior art citation under 37 CFR 1.501 or closed from public view, at the Office's option. A **filing date** will **NOT** be assigned to the request until the deficiencies noted below are corrected (37 CFR 1.510(d)):

The following items required by **37 CFR 1.510(a) and (b)** are missing:

☐ 1. The *ex parte s* reexamination filing fee under 37 CFR 1.20(c)(1) – see attached Form PTO-2057.

☐ 2. An identification of the patent by its patent number, and of every claim of the patent for which reexamination is requested.

☐ 3. A citation of the patents and printed publications that are presented to raise a substantial new question of patentability.

☒ 4. A statement pointing out each substantial new question of patentability based on the cited patents & printed publications, and a detailed explanation of the pertinency and manner of applying the patents & printed publications to every claim for which reexamination is requested.

☐ 5. A legible copy of every patent or printed publication (other than U.S. patents or U.S. patent publications) relied upon or referred to in (3) and (4) above, accompanied by an English language translation of all the necessary and pertinent parts of any non-English language document.

☐ 6. A legible copy of the entire patent including the front face, drawings, and specification/claims (in **double** column format) for which reexamination is requested, and a legible copy of any disclaimer, certificate of correction, or reexamination certificate issued in the patent. All copies must have each page plainly written on only one side of a sheet of paper.

☐ 7. A certification by the third party requester that a copy of the request has been served in its entirety on the patent owner at the address provided for in 37 CFR 1.33(c). The name and address of the party served must be indicated. If service was not possible, a duplicate copy of the request must be supplied to the Office.

☐ 8. Other:

☒ Explanation of above item(s): See Attachment.

Any written correspondence in response to this notice must include a submission pursuant to the attached instructions. **The instructions for a detailed explanation for an *ex parte* reexamination request differ from those for an *inter partes* reexamination request.** Any written correspondence in response to this notice should be mailed to the Central Reexamination Unit (CRU), ATTN: "Box *Ex Parte* Reexam" at the USPTO address indicated at the top of this notice. Any "replacement documents" may be facsimile transmitted to the CRU at the FAX number indicated below. A REPLACEMENT STATEMENT AND EXPLANATION UNDER 37 CFR 1.510(b)(1) and (2) MAY NOT BE FACSIMILE TRANSMITTED.

Manuel Salazar

Patent Reexamination Specialist, Central Reexamination Unit
(571) 272- 7740 ; FAX No. (571) 273-9900

cc: Patent Owner's Name and Address: THOMAS KAYDEN HORSTEMEYER & RISLEY LLP
600 GALLERIA PARKWAY SE
STE 1500
ATLANTA, GA 30339-5994

ATTACHMENT TO PTOL 2077

Control Number: 90/009,697
Patent Number: 6,689,629
Request Receipt Date: February 26, 2010

Please read the instructions that accompany this Notice and Attachment.

The request for *Ex Parte* Reexamination of U.S. Patent 6,689,629 filed on February 26, 2010 does not comply with the filing requirements of *ex parte* reexamination proceedings under 37 CFR 1.510(b)(1) and (2).

37 CFR 1.510(b)(1) and (2) state:

> **(b) Any request for reexamination must include the following parts:**
> **(1) A statement pointing out each substantial new question of patentability based on prior patents and printed publications.**
> **(2) An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. If appropriate, the party requesting reexamination may also point out how claims distinguish over cited prior art.**

The request has failed to provide the requisite identification and explanation in compliance with 37 CFR 1.510(b)(1), of what substantial new questions of patentability (SNQs) are being raised by the cited prior art documents under 37 CFR 1.510(b). The request fails to clearly explain how each asserted SNQ is substantially different from those raised in the previous examination of the patent before the Office. As pointed out in MPEP 2216:

> "It is not sufficient that a request for reexamination merely proposes one or more rejections of a patent claim or claims as a basis for reexamination. It must first be demonstrated that a patent or printed publication that is relied upon in a proposed rejection presents a new, non-cumulative technological teaching that was not previously considered and discussed on the record during the prosecution of the application that resulted in the patent for which reexamination is requested, and during the prosecution of any other prior proceeding involving the patent for which reexamination is requested." [Emphasis added]

While the request does address what some of the references teach individually, the request does not clearly explain, for each identified SNQ, which teachings are substantially different than those considered in the previous examination of the patent by the Office. Accordingly, any corrected request filed in response to this decision must clearly establish, for each substantial new question/proposed rejection identified, what is the new technical teaching being provided by the citation of the newly cited references. See MPEP 2242.

On page 6 of the request for reexamination the following statement is unclear "As such, Requester believes that these teachings of Hirabayashi raise a substantial new question of patentability with respect to at least independent claims 1 and 9, and consequently claims 2-5 and 7-8 dependent on claim 1 and claims 10-13 and 15-16 dependent on claim 9." The phrase "at least" does not limit the number of claims for which reexamination is being requested. The term "at least" urges the examiner to apply the cited art to the remainder of the claims that are requested, thus placing a burden of identifying the claims and applying the references to the remainder of the claims. See also pages (7-24, 34, 40, 43, 44, 47, 51, 56, 60, 64, 68, 73, 77, 81, 85, 90, 93, 97, 98, 101,105, 108, 109, 112, 116, 121, 124, 125, 128, 132, 137, 141, 142, 145, 149, 153, 157, 161). Since the request has not properly advanced, and explained, a substantial new question with respect to all of the '629 patent claims for which reexamination has been requested, the request fails to comply with the requirements for granting a filing date for a reexamination request.

Each substantial new question of patentability (SNQ) must be identified. Each proposed rejection based on the SNQ must be identified separately. For each identified rejection based on a SNQ, the request must explain how the cited documents identified for that proposed rejection are applied to meet/teach the patent claim limitations to thus establish the identified proposed rejection.

If the requester were permitted to omit an explanation of the SNQs raised and how such documents cited in the request are applied to the patent claims, an undue burden would be placed on the Office to address each document in the determination on the request, without an explanation of the relevance to the patent claims. Accordingly, such an omission is prohibited by law.

REQUESTER'S RECOURSE

Requester has the option to respond to this identification of defects in the request papers by applying the appropriate option(s) set forth below:

Providing an identification of each substantial new question of patentability, a statement of each proposed rejection based on an SNQ, and an explanation of the manner and pertinent of applying each cited document to the patent claims for which reexamination is requested, as required by 37 CFR 1.510(b)(1) and (2). Every limitation in each patent claim for which reexamination is requested must be addressed. Where the references applied in combination, each combination must be individually identified, and the basis for applying each identified combination of references must be supplied.

In order to obtain a filing date for the request papers, the requester must, within thirty (30) days of the mailing date of this decision, file a response to this decision which makes the request papers filing date complaint. The response may be supplied as either a corrected request, or a submission of only the missing information.

A request for *ex parte* reexamination (or for *inter partes* reexamination) must now meet all the applicable statutory and regulatory requirements before a filing date is accorded to

the request. See MPEP 2227 Part B.1 and MPEP 2217, Part 1. See also *Clarification of Filing Date Requirements for Ex Parte and Inter Partes Reexamination Proceedings*, 71 Fed. Reg. 44219 (August 4, 2006), 1309 *Off. Gaz. Pat. Office* 216 (August 29, 2006) (Final Rule).

Failure to submit a proper response to this Notice may result in the termination of the request, with no filing date accorded.

All correspondence related to this ex parte reexamination proceeding should be directed:

By EFS: Registered users may submit via the electronic filing system EFS-Web, at http://sportal.gov/authenticate/authenticateuserlocalepf.html.

By Mail to: Mail Stop Ex Parte Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By Hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

INSTRUCTIONS TO NOTICE OF FAILURE TO COMPLY WITH *EX PARTE* REEXAMINATION REQUEST FILING REQUIREMENTS (37 CFR 1.510(c))

HOW TO REPLY TO THIS NOTICE

Any written correspondence in response to this notice must include either a **replacement document**, or, **if item #4 is checked and/or it is otherwise specifically required by the Office, a paper containing a replacement statement and explanation under 37 CFR 1.510(b)(1) and (2)** that either replaces the originally-filed statement and explanation or provides a previously missing statement and explanation. A replacement document either replaces an originally-filed document, or provides a previously missing document, that contains part(s) of the request other than the statement and explanation as set forth in 37 CFR 1.510(b)(1) and (2). For example, a replacement to the originally-filed listing of cited patents and printed publications, PTO/SB/08 (formerly designated as PTO-1449) or its equivalent, is a replacement document.

If a paper containing a replacement statement and explanation, or a replacement document (other than a replacement certificate of service), is submitted by a third party requester, it must be **accompanied by a certification that a copy of the replacement statement and explanation under 37 CFR 1.510(b)(1) and (2), or that a copy of the replacement document, has been served** in its entirety on the patent owner at the address provided for in 37 CFR 1.33(c). The name and address of the party served must be indicated. If service was not possible, a duplicate copy of the replacement statement and explanation (or replacement document) must be supplied to the Office.

REPLACEMENT STATEMENT AND EXPLANATION UNDER 37 CFR 1.510(b)(1) and (2) (ITEM #4 IS CHECKED)

The **statement and explanation under 37 CFR 1.510(b)(1) and (2)** (see item #4) must discuss **EVERY patent or printed publication cited in the information disclosure statement** in at least one proposed rejection or statement identifying a substantial new question of patentability (SNQ), AND in a corresponding detailed explanation (see the below discussion). Furthermore, **EVERY claim for which reexamination is requested** must be discussed in at least one proposed rejection or statement identifying an SNQ and in the corresponding detailed explanation. If item #4 is missing or incomplete, a paper containing a **replacement statement and explanation under 37 CFR 1.510(b)(1) and (2) is required.**

A paper containing a replacement statement and explanation under 37 CFR 1.510(b)(1) and (2) may NOT be facsimile transmitted. It must be received by first class mail or by USPS Express Mail.

If an originally-filed information disclosure statement cites patents or printed publications that are NOT discussed in at least one proposed rejection or statement identifying an SNQ AND in the corresponding detailed explanation **in the originally-filed request**, the requester must file either (a) a **replacement document, i.e., a replacement PTO/SB/08 (former PTO-1449)** or its equivalent, listing **ONLY** those patents and printed publications that are so discussed, or (b) a paper containing a **replacement statement and explanation under 37 CFR 1.510(b)(1) and (2).** If the first option is chosen, the replacement PTO/SB/08 or its equivalent should include a cover letter expressly withdrawing from the request any previously cited references that are being omitted by the replacement PTO/SB/08 or its equivalent. The requester may, if desired, file both a replacement PTO/SB/08 or its equivalent and a paper containing a replacement statement and explanation, if the replacement statement and explanation discusses EVERY patent or printed publication, cited in the replacement PTO/SB/08 or its equivalent, in at least one proposed rejection or statement identifying an SNQ and in the corresponding detailed explanation.

Requester is NOT required to, and should not, additionally file a replacement copy of any exhibits, references, etc., or other replacement parts of the request (i.e., replacement documents) if a defect requiring a replacement document is not specifically identified by this notice.

Examples of When a Replacement Statement and Explanation under 37 CFR 1.510(b)(1) and (2) Is Required:

1. The originally-filed request fails to discuss **EVERY** patent or printed publication cited in the originally-filed information disclosure statement in at least one proposed rejection or statement identifying an SNQ and in the corresponding detailed explanation, and the requester does not wish to file a replacement PTO/SB/08 (formerly designated as PTO-1449) or its equivalent listing ONLY those patents and printed publications that are so discussed.

2. The originally-filed request discusses every patent or printed publication cited in the information disclosure statement in at least one proposed rejection or statement identifying an SNQ, but **fails to discuss EVERY patent or printed publication cited in the information disclosure statement in a detailed explanation that corresponds to the proposed rejection or statement identifying an SNQ.**

3. The originally-filed request fails to discuss **EVERY CLAIM** for which reexamination is requested in at least one proposed rejection or statement identifying an SNQ, and in the corresponding detailed explanation.

Examples of Proposed Rejections and Statements Identifying a Substantial New Question of Patentability (SNQ)

Proposed rejections

Claims 1-3 are obvious over reference A in view of reference B.
Claims 4-6 are obvious over reference A in view of references B and C.
Claims 7-10 are obvious over reference Q in view of reference R.

Statements identifying a substantial new question of patentability

A substantial new question of patentability as to claims 1-3 is raised by reference A in view of reference B.
A substantial new question of patentability as to claims 4-6 is raised by reference A in view of references B and C.
A substantial new question of patentability as to claims 7-10 is raised by reference Q in view of reference R.

A proposed rejection or statement identifying an SNQ must be repeated with any *replacement* detailed explanation that corresponds to the proposed rejection or statement identifying an SNQ, in any paper containing a replacement statement and explanation under 37 CFR 1.510(b)(1) and (2).

In addition, the requester should include an explanation of *how the SNQ is raised.*

1. Assume that claim 1 of the patent recites, as one of the limitations, widget W. Requester would state that the XYZ reference, cited in the information disclosure statement, contains a teaching of widget W as recited in claim 1, and that this teaching was not present during the prior examination of the patent under reexamination (i.e., the teaching is "new"). Requester would also state that he believes that a reasonable examiner would consider this teaching important in determining whether or not the claims are patentable. For this reason, requester would state that this teaching by the XYZ reference raises a substantial new question of patentability (SNQ) with respect to at least claim 1 of the patent. Similarly, if dependent claim 6 adds widget H, the requester would state that the ABC reference, cited in the information disclosure statement, contains a teaching of widget H as recited in claim 6, that this teaching was not present during the prior concluded examination of the patent, that a reasonable examiner would consider this teaching important in determining whether or not the claims are patentable, and that this teaching raises an SNQ with respect to dependent claim 6 of the patent.

2. Assume that claim 1 of the patent recites, as one of its limitations, limitation W. Assume either that reference XYZ was applied in a rejection during the prior examination of the patent, or that the teachings of reference XYZ are purely cumulative to a reference cited in a rejection during the prior examination of the patent. Assume further that reference ABC teaches that limitation W would have been either inherent given the teachings of reference XYZ, or would have been obvious in view of the combination of XYZ and ABC. Reference ABC was cited in an information disclosure statement but was never discussed or applied in a rejection ***in combination with the XYZ reference*** during the prior examination of the patent under reexamination. **Requester would state** that reference XYZ was present during the prior examination of the patent under reexamination because it was applied in a rejection during the prosecution of the patent, and that reference ABC was cited in an information disclosure statement but never applied in a rejection (or never discussed), **in combination with the XYZ reference** during the prior examination of the patent under reexamination Requester would then state (1) that the ***combination*** of the XYZ reference and the ABC reference, both of which are cited in the information disclosure statement, contains a teaching of limitation W as recited in claim 1, (2) that this teaching provided by the **combination** of the XYZ and ABC references was not present during the prior examination of the patent under reexamination, (3) that a reasonable examiner would consider this teaching important in determining whether or not the claims are patentable, and (4) that this teaching raises an SNQ with respect to claim 1 of the patent.

Example of a Detailed Explanation

Assume, for example, that a requester believes that the XYZ reference, alone, anticipates claims 1-5. The requester would expressly propose a rejection of claims 1-5 under 35 USC 102(b) as being anticipated by the XYZ reference. In a claim chart, the requester would then show how **each limitation** of claims 1-5 is anticipated by the XYZ reference. If the requester believes that the XYZ reference, in view of the ABC reference, renders obvious claims 6-10, the requester would expressly propose a rejection of claims 6-10 under 35 USC 103 as being obvious over the XYZ reference in view of the ABC reference. In a claim chart, the requester would then show which limitations of claims 6-10 are taught by the XYZ reference, and which limitations of claims 6-10 are taught by the ABC reference. The requester should quote each pertinent teaching in the prior art reference, referencing each quote by page, column and line number, and any relevant figure numbers.

A **patent owner**, when filing a request for reexamination in an *ex parte* reexamination proceeding, may satisfy the requirement under 37 CFR 1.510(b) for supplying a detailed explanation by comparing, limitation-by-limitation, the claim(s) under reexamination with the teachings of each reference cited in the information disclosure statement and in the statement pointing out an SNQ. Each limitation of the claim(s) must be separately discussed. For each claim limitation, the patent owner must do one of the following: (a) show how at least one reference teaches or suggests the limitation, (b) admit that the limitation is "old", or (c) state that the limitation is believed to be missing from the reference. In a claim chart, the patent owner should quote each pertinent teaching in the prior art reference,

referencing each quote by page, column and line number, and any relevant figure numbers. Proposed applications of the cited references and/or proposed combinations of the cited references should separately identified. The patent owner is not required to

expressly propose a rejection of the claim(s) or provide a statement of why the claim(s) under reexamination would have been obvious over a proposed reference combination.

REPLACEMENT DOCUMENTS

If the originally-filed PTO/SB/08 (former PTO-1449) or its equivalent lists patents or printed publications that are NOT discussed in at least one proposed rejection or statement identifying an SNQ AND in the corresponding detailed explanation **in the originally-filed request**, the requester may file a paper containing a **replacement PTO/SB/08 (former PTO-1449) or its equivalent** listing **ONLY** those patents and printed publications that are so discussed. The replacement PTO/SB/08 or its equivalent should include a cover letter expressly withdrawing from the request any formerly cited references that are now being omitted by the replacement PTO/SB/08 or its equivalent. Similarly, if **any patent or printed publication discussed** in at least one proposed rejection or statement identifying an SNQ AND in the corresponding detailed explanation **in the originally-filed request is not listed in the originally-filed PTO/SB/08 (former PTO-1449)** or its equivalent, the requester must file a **replacement PTO/SB/08 (former PTO-1449)** or its equivalent listing all of the patents and printed publications, including the previously omitted reference(s), and provide copies of the missing references if copies were not provided with the originally-filed request

If a copy of a patent, printed publication, or an English-language translation of a patent or printed publication, that is cited in the PTO/SB/08 (former PTO-1449) or its equivalent, is illegible, missing, or incomplete (i.e., it does not contain all of the pages indicated in the PTO/SB/08 (former PTO-1449) or its equivalent), a replacement copy of the patent or printed publication is required.

If a copy of any disclaimer, certificate of correction, or reexamination certificate issued in the patent, or a copy of the entire patent for which reexamination is requested as described in item #6, is missing, or if the copy that was received by the Office was illegible or incomplete, a replacement document (i.e., a replacement copy of the disclaimer, certificate of correction, reexamination certificate, or entire patent under reexamination as described in item #6) is required.

If the requester fails to correctly identify the patent number or the claims for which reexamination is requested on the transmittal form for the request (PTO/SB/57, or an equivalent) as described in item #2, and the patent number and the claims for which reexamination is requested are correctly identified in the originally-filed request, a **replacement transmittal form** is required.

If a certificate of service on the patent owner, as described in item #7, is missing, or if the certificate of service received by the Office is inaccurate or incomplete, a replacement certificate of service is required.

Replacement documents may be facsimile transmitted. A paper containing a replacement statement and explanation may NOT be facsimile transmitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re: Reexamination of U.S. Patent No. 6,689,629 B2

Control No.: 90/009,697

Inventors: Tsujimura et al.

Issued: February 10, 2004

Filed: February 5, 2002

Titled: Array Substrate For Display, Method Of Manufacturing Array Substrate For Display and Display Device Using the Array Substrate

Atty. Docket No.: 7773.0084.61

RESPONSE TO NOTICE OF FAILURE TO COMPLY WITH EX PARTE REEXAMINATION REQUEST

Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Notice of Failure to Comply with Ex Parte Reexamination Request ("Notice") mailed March 10, 2010 the Requestor hereby submits the attached Revised Request for Ex Parte Reexamination.

Requestor respectfully thanks the Examiner for courtesies extended during the telephone conversation on March 15, 2010 to discuss the Notice and for the initial review of this Request. Requestor has made an earnest effort to respond to all issues presented in the Notice. If for any reason the Examiner finds the Request still does not satisfy all the requirements under 37 C.F.R. 1.510, the Requestor cordially invites the Examiner to call the undersigned attorney at (202) 496-7500.

The Notice states that the Request did not include a statement pointing out each substantial new question of patentability raised by the cited prior art because the Request included the language "at least" when identifying the claims for which the substantial new question is raised. Further, the Notice states that this places "a burden of identifying the claims and applying the references to the remainder of the claims," and fails to comply with the requirements for granting a filing date for a reexamination request. Although the Requestor believes the original Request complied with the requirements, Requestor has revised the Request to remove the "at least" language. Accordingly, Requestor believes the Revised Request addresses the issues raised by the Notice and meets the requirements for granting a filing date.

Respectfully submitted,

Date: March 16, 2010

By __/ Song K. Jung /_____

Song K. Jung
Reg. No. 35,210
McKenna Long & Aldridge LLP
1900 K St., N.W.
Washington D.C. 20006
(202) 496-7500

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re:	Reexamination of U.S. Patent No. 6,689,629 B2
Control No.:	90/009,697
Inventors:	Tsujimura et al.
Issued:	February 10, 2004
Filed:	February 5, 2002
Titled:	Array Substrate For Display, Method of Manufacturing Array Substrate For Display and Display Device Using the Array Substrate
Atty. Docket:	07773.084.61

REVISED REQUEST FOR *EX PARTE* REEXAMINATION UNDER 37 C.F.R. § 1.510

Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

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2. Yoshinori Discloses Each and Every Element of Claims 1-5, 7-13, and 15-16 85

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REQUESTOR'S STATEMENT

Ex parte Reexamination under 35 U.S.C. §§ 302-307 and 37 C.F.R. § 1.510 is hereby requested of United States Patent No. 6,689,629 ("the '629 patent") issued to inventors Takatoshi Tsujimura, Atsuya Makita, and Toshiaki Arai (the "Request"). Presented hereinafter is substantial new questions of patentability ("SNQs") based upon patents and publications.

The '629 patent, attached as Exhibit A, was issued on February 10, 2004. The original assignee of the patent was International Business Machines ("IBM"). The current assignee is AU Optronics Corporation ("AUO"). The '629 patent has not expired and remains in effect. Pursuant to 37 C.F.R. § 1.510, this request includes the following:

a. a statement pointing out each substantial new question of patentability based on prior patents and printed publications;

b. an identification of every claim for which reexamination is requested and an explanation of the pertinence and manner of applying the cited reference to every claim for which reexamination is requested;

c. a copy of the cited prior references relied upon;

d. a copy of the above-identified patent;

e. a certification that a copy of the request has been served in its entirety on the patent owner in accordance with 37 C.F.R. §1.33(c); and

f. a fee as required in 37 CFR 1.20(c)(1).

The '629 patent was at issue in a bench trial in June 2009, in case *LG Display Co., Ltd. v. Chi Mei Optoelectronics Corporation, et al.*, Civil Action Nos. 06-726-JJF (D. Del. 2006). Post trial briefing was completed in September 2009 and the parties are currently waiting for a final order.

I. CLAIMS FOR WHICH REEXAMINATION IS REQUESTED AND CITATION OF PRIOR ART

Reexamination is requested of claims 1-16 of the '629 patent. Requestor believes that the apparatus and method set forth in claims 1-16 are unpatentable as being fully anticipated under 35 U.S.C. § 102 and rendered obvious under 35 U.S.C. §103 by any of the following: Hirabayashi, Watanabe '275, Kwak, Yoshinori, Tomoyuki, Zhang, Watanabe '811, and Miyashita. These patent documents fully disclose the claimed structure and process steps of claims 1-16 of the '629 patent.

Specifically, the proposed rejections that raise a substantial new question of patentability as to claims 1-16 are as follows:

- Claims 1-5, 7-13, and 15-16 are unpatentable as being fully anticipated under 35 U.S.C. § 102(b) by European Patent No. 0887695 to Hirabayashi (hereinafter "Hirabayashi") (attached as Exhibit B);
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Hirabayashi in view of U.S. Patent No. 6,163,356 to Song et al. (hereinafter "Song") (attached as Exhibit C);
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Hirabayashi in view of the '629 Admitted Prior Art ("the '629 APA");
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Hirabayashi in view of U.S. Patent No. 6,157,430 to Kubota et al. (herein after "Kubota")(attached as Exhibit O);
- Claims 1-16 are unpatentable as being fully anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 5,850,275 to Watanabe et al. (hereinafter "Watanabe '275") (attached as Exhibit D);

- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Watanabe '275 in view of Song;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Watanabe '275 in view of the '629 APA;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Watanabe '275 in view of Kubota;
- Claims 1-2 and 9-10 are unpatentable as being fully anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 6,862,069 to Kwak et al. ("Kwak") (attached as Exhibit E);
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Kwak in view of Song;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Kwak in view of the '629 APA;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Kwak in view of Kubota;
- Claims 1-5, 7-13, and 15-16 are unpatentable as being fully anticipated under 35 U.S.C. § 102(b) by Japanese Publication No. H10-333151 to Yoshinori et al. ("Yoshinori") (attached as Exhibit F including certified translation);
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Yoshinori in view of Song;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Yoshinori in view of the '629 APA;

- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Yoshinori in view of Kubota;
- Claims 1 and 9 are unpatentable as being fully anticipated under 35 U.S.C. § 102(b) by Japanese Publication No. 2000-098909 to Tomoyuki ("Tomoyuki") (attached as Exhibit G including certified translation);
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Tomoyuki in view of Song;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Tomoyuki in view of the '629 APA;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Tomoyuki in view of Kubota;
- Claims 1-5, 7-13, and 15-16 are unpatentable as being fully anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 5,995,189 to Zhang ("Zhang") (attached as Exhibit H);
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Zhang in view of Song;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Zhang in view of the '629 APA;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Zhang in view of Kubota;
- Claims 1-5, 7-13, and 15-16 are unpatentable as being fully anticipated under 35 U.S.C. § 102(b) by Japanese Publication No. H06-082811 to Watanabe ("Watanabe '811") (attached as Exhibit I including certified translation);

- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Watanabe '811 in view of Song;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Watanabe '811 in view of the '629 APA;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Watanabe '811 in view of Kubota;
- Claims 1 and 9 are unpatentable as being fully anticipated under 35 U.S.C. § 102(b) by Japanese Publication No. H09-197415 to Miyashita ("Miyashita") (attached as Exhibit J including certified translation);
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Miyashita in view of Song;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Miyashita in view of the '629 APA;
- Claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) as being obvious by Miyashita in view of Kubota;

These patent documents fully disclose the claimed structure and process steps of claims 1-16 of the '629 patent.

II. SUBSTANTIAL NEW QUESTION OF PATENTABILITY

As discussed in more detail below, Requestor respectfully submits that a substantial new question of patentability exists with respect to claims 1-16 of the '629 patent. Section 2242 of the MPEP provides that "[a] prior art patent or printed publication raises a substantial question of patentability where there is a substantial likelihood that a reasonable examiner would consider

the prior art patent or printed publication important in deciding whether or not the claim is patentable."

More specifically:

1. A substantial new question of patentability as to claims 1-5, 7-13, and 15-16 is raised by Hirabayashi. Hirabayashi was not considered by the Patent Office during the prosecution of the '629 patent. As discussed below, the Patent Office, without knowledge of Hirabayashi, allowed the'629 patent on the rationale that the art did not teach or suggest:

> An array substrate for display, comprising: a layer of an insulating substrate, *having an area*;...dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Hirabayashi teaches this feature. *See e.g.,* Hirabayashi, Fig. 1 (the hatch pattern); col. 9, ll. 35-42; col. 11, ll. 19-24. Hirabayashi teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider these teachings of Hirabayashi important to the patentability of the '629 patent and is new and non-cumulative. As such, Requestor believes that these teachings of Hirabayashi raise a substantial new question of patentability with respect to independent claims 1 and 9, and consequently claims 2-5 and 7-8 dependent on claim 1 and claims 10-13 and 15-16 dependent on claim 9.

2. A substantial new question of patentability is raised by Hirabayashi in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. However, Song was not considered in conjunction with Hirabayashi, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely,

Hirabayashi provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.,* Hirabayashi, Fig. 1 (the hatch pattern); col. 9, ll. 35-42; col. 11, ll. 19-24), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Hirabayashi and Song important to the patentability of the '629 patent and new and non-cumulative. As such, Hirabayashi in view of Song raises a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

3. A substantial new question of patentability is raised by the Hirabayashi in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. However, the '629 APA was not considered in conjunction with Hirabayashi, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Hirabayashi provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.,* Hirabayashi, Fig. 1 (the hatch pattern); col. 9, ll. 35-42; col. 11, ll. 19-24), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Hirabayashi and the '629 APA important to the patentability of the '629 patent and new and non-cumulative. As such, Hirabayashi in view of the '629 APA raise a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

4. A substantial new question of patentability is raised by Hirabayashi in view of Kubota. Neither Hirabayashi nor Kubota were before the Patent Office during the prosecution of the '629 patent. Hirabayashi, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Hirabayashi provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.,* Hirabayashi, Fig. 1 (the hatch pattern); col. 9, ll. 35-42; col. 11, ll. 19-24), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Hirabayashi and Kubota important to the patentability of the '629 patent and new and non-cumulative. As such, Hirabayashi in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

5. A substantial new question of patentability as to claims 1-16 is raised by Watanabe '275. Watanabe '275 was not considered by the Patent Office during the prosecution of the '629 patent. As discussed below, the Patent Office, without knowledge of Watanabe '275, allowed the'629 patent on the rationale that the art did not teach or suggest:

> a layer of an insulating substrate, *having an area*;…dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate.*

As discussed below, Watanabe '275 teaches this feature. See, e.g. Watanabe '275, Fig. 2 (light shield area 20); col. 4, ll. 28-34. Watanabe '275 teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider these teachings of

Watanabe '275 important to the patentability of the '629 patent and new and non-cumulative art. As such, Requestor believes that Watanabe '275 raises a substantial new question of patentability with respect to independent claims 1 and 9, and consequently claims 2-8 dependent on claim 1 and claims 10-16 dependent on claim 9.

6. A substantial new question of patentability is raised by Watanabe '275 in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. However, Song was not considered in conjunction with Watanabe '275, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Watanabe '275 provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g. Watanabe '275, Fig. 2 (light shield area 20); col. 4, ll. 28-34), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Watanabe '275 and Song are important to the patentability of the '629 patent and are new and non-cumulative. As such, Watanabe '275 in view of Song raises a substantial new question of patentability as to as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

7. A substantial new question of patentability is raised by Watanabe '275 in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. However, the '629 APA was not considered in conjunction with Watanabe '275, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Watanabe '275 provides dummy patterns comprising at

least about 30% of an area of the insulating substrate (See, e.g. Watanabe '275, Fig. 2 (light shield area 20); col. 4, ll. 28-34), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Watanabe '275 and the '629 APA are important to the patentability of the '629 patent and are new and non-cumulative. As such, Watanabe '275 in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

8. A substantial new question of patentability is raised by Watanabe '275 in view of Kubota. Neither Watanabe '275 nor Kubota were before the Patent Office during the prosecution of the '629 patent. Watanabe '275, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Watanabe '275 provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g. Watanabe '275, Fig. 2 (light shield area 20); col. 4, ll. 28-34), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Watanabe '275 and Kubota are important to the patentability of the '629 patent and are new and non-cumulative. As such, Watanabe '275 in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

9. A substantial new question of patentability as to claims 1-2 and 9-10 is raised by Kwak. Kwak was not considered by the Patent Office during the prosecution of the '629 patent. As discussed below, the Patent Office, without knowledge of Kwak, allowed the'629 patent on the rationale that the art did not teach or suggest:

> a layer of an insulating substrate, *having an area*;…dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed below, Kwak teaches this feature. See, e.g., Kwak, col. 4, ll. 28-41, Fig 7 (item 36). Kwak teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider these teachings of Kwak important to the patentability of the '629 patent and new, non-cumulative art. As such, Requestor believes that Kwak raises a substantial new question of patentability as to least independent claims 1 and 9 and claim 2 dependent on claim 1 and claim 10 dependent from claim 9.

10. A substantial new question of patentability is raised by Kwak in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. However, Song was not considered in conjunction with Kwak, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Kwak provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Kwak, col. 4, ll. 28-41, Fig 7 (item 36), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Kwak and Song are important to

the patentability of the '629 patent and are new and non-cumulative. As such, Kwak in view of Song constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

11. A substantial new question of patentability is raised by Kwak in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. However, the '629 APA was not considered in conjunction with Kwak, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Kwak provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Kwak, col. 4, ll. 28-41, Fig 7 (item 36)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Kwak and the '629 APA are important to the patentability of the '629 patent and are non-cumulative art. As such, Kwak in view of the '629 APA constitutes a substantial new question of patentability.

12. A substantial new question of patentability is raised by Kwak in view of Kubota. Neither Kwak nor Kubota were before the Patent Office during the prosecution of the '629 patent. Kwak, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Kwak provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Kwak, col. 4, ll. 28-41, Fig 7 (item 36)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner

would consider the combined teachings of Kwak and Kubota are important to the patentability of the '629 patent and are new and non-cumulative. As such, Kwak in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

13. A substantial new question of patentability as to claims 1-5,7-13, and 15-16 is raised by Yoshinori. Yoshinori was not considered by the Patent Office during the prosecution of the '629 patent. As discussed below, the Patent Office, without knowledge of Yoshinori, allowed the'629 patent on the rationale that the art did not teach or suggest:

> a layer of an insulating substrate, *having an area*;…dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Yoshinori teaches this feature. See, e.g., Yoshinori, ¶ 20, Fig 1 (B) (interval projection steps 5). Yoshinori teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner woud consider these teachings of Yoshinori important to the patentability of the '629 patent and new and non-cumulative. As such, Requestor believes that these teachings of Yoshinori raise a substantial new question of patentability with respect to independent claims 1 and 9, and consequently claims 2-5 and 7-8 dependent on claim 1 and claims 10-13 and 15-16 dependent on claim 9.

14. A substantial new question of patentability is raised by Yoshinori in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. However, Song was not considered in conjunction with Yoshinori, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely,

Yoshinori provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Yoshinori, ¶ 20, Fig 1 (B) (interval projection steps 5)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Yoshinori and Song are important to the patentability of the '629 patent and are new and non-cumulative. As such, Yoshinori in view of Song constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

15. A substantial new question of patentability is raised by Yoshinori in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. However, the '629 APA was not considered in conjunction with Yoshinori, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Yoshinori provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Yoshinori, ¶ 20, Fig 1 (B) (interval projection steps 5)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Yoshinori and the '629 APA are important to the patentability of the '629 patent and are new and non-cumulative. As such, Yoshinori in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

16. A substantial new question of patentability is raised by Yoshinori in view of Kubota. Neither Yoshinori nor Kubota were before the Patent Office during the prosecution of the '629 patent. Yoshinori, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Yoshinori provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Yoshinori, ¶ 20, Fig 1 (B) (interval projection steps 5)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Yoshinori and Kubota are important to the patentability of the '629 patent and are new and non-cumulative. As such, Yoshinori in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

17. A substantial new question of patentability as to claims 1 and 9 is raised by Tomoyuki. Tomoyuki was not considered by the Patent Office during the prosecution of the '629 patent. As discussed below, the Patent Office, without knowledge of Tomoyuki, allowed the'629 patent on the rationale that the art did not teach or suggest:

> a layer of an insulating substrate, *having an area*;…dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Tomoyuki teaches this feature. See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (dummy patterns 5a). Tomoyuki teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus a reasonable examiner would consider these teachings of Tomoyuki important to the patentability of the '629 patent and new and non-cumulative. As such,

Requestor believes that these teachings of Tomoyuki raise a substantial new question of patentability with respect to independent claims 1 and 9.

18. A substantial new question of patentability is raised by Tomoyuki in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. However, Song was not considered in conjunction with Tomoyuki, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Tomoyuki provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (dummy patterns 5a)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Tomoyuki and Song are important to the patentability of the '629 patent and are new and non-cumulative. As such, Tomoyuki in view of Song constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

19. A substantial new question of patentability is raised by Tomoyuki in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. However, the '629 APA was not considered in conjunction with Tomoyuki, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Tomoyuki provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (dummy patterns 5a)), which was identified as the allowable subject matter of the '629 patent, and as a

feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Tomoyuki and the '629 APA important to the patentability of the '629 patent and non-cumulative art. As such, Tomoyuki in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

20. A substantial new question of patentability is raised by Tomoyuki in view of Kubota. Neither Tomoyuki nor Kubota were before the Patent Office during the prosecution of the '629 patent. Tomoyuki, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Yoshinori provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (dummy patterns 5a)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Tomoyuki and Kubota important to the patentability of the '629 patent and new and non-cumulative. As such, Tomoyuki in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

21. A substantial new question of patentability as to claims 1-5, 7-13, and 15-16 is raised by Zhang. Zhang was not considered by the Patent Office during the prosecution of the '629 patent. As discussed below, the Patent Office, without knowledge of Zhang, allowed the'629 patent on the rationale that the art did not teach or suggest:

a layer of an insulating substrate, *having an area*;…dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Zhang teaches this feature. See, e.g., Zhang, col. 10, lines 7-17; Figs 4 and 8 (dummy patterns 304). Zhang teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider these teachings of Zhang important to the patentability of the '629 patent and new and non-cumulative. As such, Requestor believes that these teachings of Zhang raise a substantial new question of patentability with respect to independent claims 1 and 9, and consequently claims 2-5 and 7-8 dependent on claim 1 and claims 10-13 and 15-16 dependent on claim 9.

22. A substantial new question of patentability is raised by Zhang in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. However, Song was not considered in conjunction with Zhang, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Zhang provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Zhang, col. 10, lines 7-17; Figs 4 and 8 (dummy patterns 304)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Zhang and Song important to the patentability of the '629 patent and new and non-cumulative. As such, Zhang in view of Song constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

23. A substantial new question of patentability is raised by Zhang in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. However, the '629 APA was not considered in conjunction with Zhang, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Zhang provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Zhang, col. 10, lines 7-17; Figs 4 and 8 (dummy patterns 304)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Zhang and the '629 APA important to the patentability of the '629 patent and new and non-cumulative. As such, Zhang in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

24. A substantial new question of patentability is raised by Zhang in view of Kubota. Neither Zhang nor Kubota were before the Patent Office during the prosecution of the '629 patent. Zhang, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Zhang provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Zhang, col. 10, lines 7-17; Figs 4 and 8 (dummy patterns 304)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, the combined teachings of Zhang and Kubota important to the patentability of the '629 patent and new and non-cumulative. As such, Zhang in view of Kubota constitutes a substantial new

question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

25. A substantial new question of patentability as to claims 1-5, 7-13, and 15-16 is raised by Watanabe '811. Watanabe '811 was not considered by the Patent Office during the prosecution of the '629 patent. As discussed below, the Patent Office, without knowledge of Watanabe '811, allowed the'629 patent on the rationale that the art did not teach or suggest:

> a layer of an insulating substrate, *having an area*;...dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Watanabe '811 teaches this feature. *See e.g.*, Watanabe '811, Fig. 5, and [0071]. Watanabe '811 teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider these teachings of Watanabe '811 important to the patentability of the '629 patent and new and non-cumulative. As such, Requestor believes that these teachings of Watanabe '811 raise a substantial new question of patentability with respect to independent claims 1 and 9, and consequently claims 2-5 and 7-8 dependent on claim 1 and claims 10-13 and 15-16 dependent on claim 9.

26. A substantial new question of patentability is raised by Watanabe '811 in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. However, Song was not considered in conjunction with Watanabe '811, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Watanabe '811 provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Watanabe '811, Fig. 5, and [0071]), which was identified as the

allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Watanabe '811 and Song important to the patentability of the '629 patent and new and non-cumulative. As such, Watanabe '811 in view of Song constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

27. A substantial new question of patentability is raised by Watanabe '811 in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. However, the '629 APA was not considered in conjunction with Watanabe '811, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Watanabe '811 provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Watanabe '811, Fig. 5, and [0071]), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Watanabe '811 and the '629 APA important to the patentability of the '629 patent and new and non-cumulative. As such, Watanabe '811 in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

28. A substantial new question of patentability is raised by Watanabe '811 in view of Kubota. Neither Watanabe '811 nor Kubota were before the Patent Office during the prosecution of the '629 patent. Watanabe '811, as discussed above, raises a substantial new

question of patentability and teaches each and every element of claims 1 and 9. Namely, Watanabe '811 provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Watanabe '811, Fig. 5, and [0071]), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Watanabe '811 and Kubota important to the patentability of the '629 patent and new and non-cumulative. As such, Watanabe '811 in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

29. A substantial new question of patentability as to claims 1 and 9 is raised by Miyashita. Miyashita was not considered by the Patent Office during the prosecution of the '629 patent. As discussed below, the Patent Office, without knowledge of Miyashita, allowed the'629 patent on the rationale that the art did not teach or suggest:

> a layer of an insulating substrate, *having an area*;…dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Miyashita teaches this feature. *See e.g.*, Miyashita, Fig. 2 (dummy film forming region D); Fig 3 (dummy film 8); [0023]-[0025]. Miyashita teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider these teachings of Miyashita important to the patentability of the '629 patent and new and non-cumulative. As such, Requestor believes that these teachings of Miyashita raise a substantial new question of patentability with respect to independent claims 1 and 9.

30. A substantial new question of patentability is raised by Miyashita in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. However, Song was not considered in conjunction with Miyashita, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Miyashita provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Miyashita, Fig. 2 (dummy film forming region D); Fig 3 (dummy patterns 8); [0023]-[0025]), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Miyashita and Song important to the patentability of the '629 patent and new and non-cumulative. As such, Miyashita in view of Song constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

31. A substantial new question of patentability is raised by Miyashita in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. However, the '629 APA was not considered in conjunction with Miyashita, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Miyashita provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Miyashita, Fig. 2 (dummy film forming region D); Fig 3 (dummy patterns 8); [0023]-[0025]), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16.

Thus, a reasonable examiner would consider the combined teachings of Miyashita and the '629 APA important to the patentability of the '629 patent and new and non-cumulative. As such, Miyashita in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

32. A substantial new question of patentability is raised by Miyashita in view of Kubota. Neither Miyashita nor Kubota were before the Patent Office during the prosecution of the '629 patent. Miyashita, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Miyashita provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Miyashita, Fig. 2 (dummy film forming region D); Fig 3 (dummy patterns 8); [0023]-[0025]), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. Thus, a reasonable examiner would consider the combined teachings of Miyashita and Kubota important to the patentability of the '629 patent and new and non-cumulative. As such, Miyashita in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

As discussed in more detail below, because a reasonable examiner would consider each prior art references important in deciding whether to allow the claims of the '629 patent, this Request raises a substantial new question of patentability as to claims 1-16 that should be considered during reexamination.

III. THE '629 PATENT

A. The '629 Invention

The '629 patent is directed to an array substrate for display including dummy patterns. The background section of the '629 describes that it was well-known to use a double layer structure for the wiring, namely low resistance aluminum with a metal that is harder to be oxidized than aluminum, such as chromium, tantalum, titanium, or molybdenum, on top. '629 patent, column 1, lines 33-39. And also identifies that wiring should have a proper tapered edge. '629 patent, col. 1, ll. 33-39. However, the '629 patent notes that while etching this double-layered wiring, under certain conditions such as a high etching rate, an undercut may occur of the upper conductive layer preventing the desired tapered shape. *See e.g.*, '629 patent, col. 1, ll. 43-60.

The prior art prescribes providing dummy connection pads in an a particular area to address the undercut issue, but the '629 patent maintains this is only a partial solution. '629 patent, col. 1, ll. 47-60. Namely, the '629 patent states including dummy connection pads opposite the scan and signal connection pads, increasing the wiring density, prevents an undercut only "at the ends of the thin film transistor array substrate." '629 patent, col. 1, ll. 47-60. According to the '629 patent, this solution does not address an undercut of the wiring in a region where the wiring density is low, such as between the pixel electrodes and connection pads.

Thus, while the prior art identifies that providing dummy patterns to increase wiring density addresses undercut of the upper conductive material, the '629 proposes providing dummy patterns in the particular area where the wiring density is low to address the same issue. Particularly, the '629 patent focuses on the areas such as between connection pads and the pixel array in comparison to the active pixel region. *See e.g.*, '629 patent, col. 5, l. 62-, col. 6, l. 6; col. 5, ll. 38-40. The '629 patent also describes that the dummy patterns should be made of the

same structure and at the same time as the scan or signal wiring. *See e.g.*, '629 patent, col. 5, ll. 38-41.

B. Prosecution of the Claims that Led to Issuance of the '629 Patent

The '629 Patent issued from Application Serial No. 10/068,500, filed February 5, 2002. A copy of the file history is attached as Exhibit K.

At the time of the first office action, claims 1-18 were pending. The first office action, mailed on May 29, 2003, rejected claims 1 and 9 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,285,301 to Shirahashi. Claims 3-9 and 12-18 were rejected under 35 U.S.C. 103(a) as unpatentable over Shirahashi in view of U.S. Patent No. 6,163,356 to Song et al. Claims 2 and 11 were objected to as being dependent on a rejected base claim but would be allowable if rewritten in independent form.

In response to the office action, Applicant amended claims 1 and 10 to incorporate the subject matter of claims 2 and 11. A notice of allowance was then issued on October 1, 2003.

While the Notice of Allowance did not include a statement of reasons for allowance, allowable subject matter was identified in the previous office action. It stated:

> The prior art of record does not teach or suggest the area protected by the dummy metallization recited in claims 2 and 11. '629 File History, Office Action Dated May 29, 2003 at page 3.

Original claim 2 recited:

> The array substrate for display according to claim 1 wherein ***the dummy conductive patterns comprise at least about 30% of the area of the insulating substrate***.

Claim 11 recited the corresponding element of claim 2 in method form.

C. Claim Scope of the '629 Patent

During reexamination, the claims must be interpreted as broadly as their terms reasonably allow. MPEP § 2111.01. The words of a claim must be given their plain meaning unless the

plain meaning is inconsistent with the specification. *Id.* Thus, in the analysis and discussion below, the claims are given their broadest reasonable interpretation.

Independent claim 1 of the '629 patent recites in part:

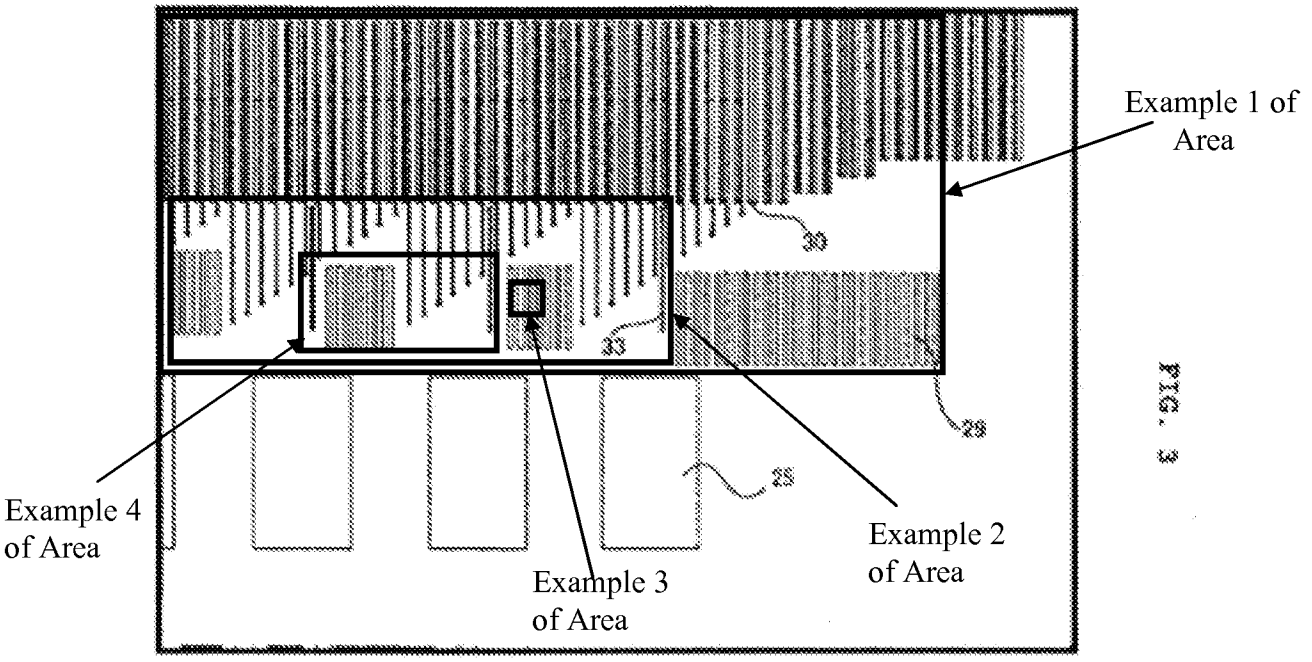
> a layer of an insulating substrate, ***having an area***;…
>
> dummy conductive patterns, ***the dummy patterns comprising at least about 30% of the area of the insulating substrate***, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring.

In other words, the claim identifies that there must be an "area" and requires that the dummy patterns comprise 30% of this area. The identified allowable subject matter indicates that this "area" is critical to the invention, however, the claim fails to identify or provide any guidance as to the location or any requirements of this area, thus *any randomly selected area* of the substrate, large or small, could satisfy this area limitation. Consistent with this position, AUO at trial admitted that "area" should be construed as "a specified region." *See* Ex. L at K-2 (Joint Claim Construction Statement for the '629 patent including AUO's proposed claim construction for the term "area").

This definition of area is also supported by testimony of Dr. Silzars, AUO's expert. For example, Dr. Silzars explained that each individual area of dummy patterns shown in Fig. 3 of the '629 patent would meet the limitations of claim 1 if the area of dummy patterns covered at least 30% of that area. *See* Trial Transcripts at 254:11-256:2 (Excerpted portions of the trial transcripts of Dr. Silzars's testimony attached as Exhibit P); *See also* Trial Exhibit LGD1049 at Figs. 3 and 4 (Trial Exhibit LGD 1049 including annotated Figs. 3 and 4 of the '629 patent, attached as Exhibit Q). Even further, Dr. Silzars admitted that you could "randomly" subdivide any of the areas and the limitations of claim 1 would still be met by the subdivided area if the

dummy patterns covered at least 30% of that subdivided area. *See,* Ex P at 251:3-11, Excerpted portions of the deposition of Dr. Silzars.

Therefore, according to the plain language of the claim and AUO's position, the area could be anywhere a dummy pattern or even a portion of a dummy pattern is located. For example, any of the boxes identified in annotated Fig. 3 below could be the area of claims 1 and 9.



Also, in litigation, AUO admitted that the wiring of the '629 invention may include "using *single or multi-layer* wiring." Ex M at ¶ 95 (Rebuttal Expert report of Dr. Aris Silzars (AUO's expert) on Validity of U.S. Patent No. 6,689,629 stating "Thus, the claims themselves teach that at least the wiring of claims 1 and 9 may be single or multi-layered."). Further, nothing in the claims suggest that the wiring is limited to a dual layer structure. Accordingly, single or multi-layer wiring should be included in the scope of the '629 claims.

IV. THE CLAIMS OF THE '629 PATENT ARE INVALID OVER THE CITED PRIOR ART

A. Overview of Prior Art Cited in this Request and Raised Substantial New Questions of Patentability

As discussed in more detail below, the prior art cited in this Request includes every feature of claims 1-16 of the '629 patent. Specifically, the prior art cited in this Request include explicit teachings of the following features of claims 1:

An array substrate for display, comprising. *See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1; Watanabe '275 col 3, lines 22-23; Figs 1, 3-4; Kwak, col. 1, ll. 34-36, Fig. 1; Yoshinori, Abstract, Figs 1-3; Tomoyuki, Abstract, Figs 1, 5-6; Zhang, Title, Figs. 1 and 16-17; Watanabe '811, Fig. 5, and [0034]; Miyashita, Fig. 3, and [0018]-[0019].

A layer of an insulating substrate, having an area. *See e.g.*, Hirabayashi, col. 31, ll. 16-20, Figs. 1 and 4-6; Watanabe '275, col 3, lines 27-30; Figs. 1-4; Kwak, col. 2, ll. 6-9, 20-23, Figs 1 and 3; Yoshinori, Abstract, Figs 1-3; Tomoyuki, Abstract, Figs 1, 5-6; Zhang, 1:35-36, Figs. 1 and 16-17; Watanabe '811, Fig. 5, item 200, and [0034]-[0038]; Miyashita, Fig. 3, and [0018]-[0019].

A thin film transistor array formed on the insulating substrate. *See e.g.*, Hirabayashi,, col. 31, ll. 16-23; Watanabe '275, col. 3:37-44; Fig 1-4; Kwak at col. 1, ll. 43-45, Fig. 1; Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7; Tomoyuki, Abstract, Figs 1, 5-6; Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17; Watanabe '811, Fig. 5, and [0034]; Miyashita, Fig. 3, item 4 (TFT), and [0019].

A plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array. *See e.g.*, Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin ; Watanabe '275, col. 3:37-44; Figs 1-2; Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12; Yoshinori, ¶ 20, Figs 1-3; Tomoyuki, Abstract, Figs 1, 5-6; Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17; Watanabe '811, [0035]; Miyashita , [0019] and Fig 2..

Connections pads, each connection pad contacting the first end of at most one of the plurality of wirings. *See e.g.,* Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18; Watanabe '275, col. 3:37-44; Figs 1-2; Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9; Yoshinori, ¶ 20, Figs 1-3; Tomoyuki, Abstract, Figs 1, 5-6; Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17; Watanabe '811, [0035], Fig. 5; Miyashita, [0019], and Fig. 1.

Pixel electrodes. *See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7; Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4; Kwak at col. 1, ll. 45-46; Yoshinori, Abstract, Figs 1-3; Tomoyuki, Figs 1, 5-6; Zhang, Figs. 1 and 16-17; Watanabe '811, Fig. 4, item 7, and [0035]; Miyashita, Fig. 3, item 3, [0019],[002]-[003].

Dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Hirabayashi, Figs. 1, 4-6, (dummy patterns shown in hatch pattern); col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54; Watanabe '275, Watanabe '275, col 4, lines 28-30, col. 3:28-35, Figs 1-2, and 6; Kwak, col. 4, ll. 28-41, Figs 7 and 9; Yoshinori, ¶ 20, Figs 1-3; Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6; Zhang, Figs. 4, 8 and 16, 10:7-17; Watanabe '811, Fig. 5, and [0071]; Miyashita, Fig 2 (dummy film forming region D); Fig 3 (dummy patterns 8); [0023]-[0025].

Specifically, the prior art cited in this Request include explicit teachings of the following features of claims 9:

A meted [sic] for forming an array substrate for display, comprising. *See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1; Watanabe '275 col 3, lines 22-23; Figs 1, 3-4; Kwak, col.

1, ll. 34-36, Fig. 1; Yoshinori, Abstract, Figs 1-3; Tomoyuki, Abstract, Figs 1, 5-6; Zhang, Title, Figs. 1 and 16-17; Watanabe '811, Fig. 5, and [0034]; Miyashita, Fig. 3, and [0018]-[0019].

Forming a layer of an insulating substrate, having an area. *See e.g.*, Hirabayashi, col. 31, ll. 16-20, Figs. 1 and 4-6; Watanabe '275, col 3, lines 27-30; Figs. 1-4; Kwak, col. 2, ll. 6-9, 20-23, Figs 1 and 3; Yoshinori, Abstract, Figs 1-3; Tomoyuki, Abstract, Figs 1, 5-6; Zhang, 1:35-36, Figs. 1 and 16-17; Watanabe '811, Fig. 5, item 200, and [0034]-[0038]; Miyashita, Fig. 3, and [0018]-[0019].

Forming a thin film transistor array formed on the insulating substrate; *See e.g.*, Hirabayashi,, col. 31, ll. 16-23; Watanabe '275, col. 3:37-44; Fig 1-4; Kwak at col. 1, ll. 43-45, Fig. 1; Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7; Tomoyuki, Abstract, Figs 1, 5-6; Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17; Watanabe '811, Fig. 5, and [0034]; Miyashita, Fig. 3, item 4 (TFT), and [0019].

Each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array. *See e.g.*, Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin ; Watanabe '275, col. 3:37-44; Figs 1-2; Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12; Yoshinori, ¶ 20, Figs 1-3; Tomoyuki, Abstract, Figs 1, 5-6; Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17; Watanabe '811, [0035]; Miyashita , [0019] and Fig 2..

Forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings. *See e.g.,* Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18; Watanabe '275, col. 3:37-44; Figs 1-2; Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9; Yoshinori, ¶ 20, Figs 1-3; Tomoyuki, Abstract, Figs 1, 5-6; Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17; Watanabe '811, [0035], Fig. 5; Miyashita, [0019], and Fig. 1.

Forming pixel electrodes. *See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7; Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4; Kwak at col. 1, ll. 45-46; Yoshinori, Abstract, Figs 1-3; Tomoyuki, Figs 1, 5-6; Zhang, Figs. 1 and 16-17; Watanabe '811, Fig. 4, item 7, and [0035]; Miyashita, Fig. 3, item 3, [0019],[002]-[003].

Forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Hirabayashi, Figs. 1, 4-6, (dummy patterns shown in hatch pattern); col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54; Watanabe '275, col 4, lines 28-30, col. 3:28-35, Figs 1-2, and 6; Kwak, col. 4, ll. 28-41, Figs 7 and 9; Yoshinori, ¶ 20, Figs 1-3; Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6; Zhang, Figs. 4, 8 and 16, 10:7-17; Watanabe '811, Fig. 5, and [0071]; Miyashita, Fig 2 (dummy film forming region D); Fig 3 (dummy patterns 8); [0023]-[0025].

V. STATEMENT UNDER 37 C.F.R. 1.510(B)(2) PROVIDING A DETAILED EXPLANATION OF HOW THE CITED REFERENCES RAISE A SUBSTANTIAL NEW QUESTION OF PATENTABILITY AND RENDER INVALID CLAIMS 1-16 OF THE '629 PATENT

A prior art patent or printed publication raises a substantial question of patentability where there is a substantial likelihood that a reasonable examiner would consider the prior art patent or printed publication *important* in deciding whether or not the claim is patentable (emphasis added). *See* MPEP § 2242. The "existence of a substantial new question of patentability is not precluded by the fact that a patent or printed publication was previously cited by or to the Office or considered by the Office." *See* 35 U.S.C. § 303(a). In addition to patents and printed publications, admissions by a patentee may also be used as evidence to establish a substantial new question of patentability in combination with a patent or a printed publication.

MPEP § 2217. An admission by a patentee may reside in a record created during litigation. Id. Such admissions by patentee may be relied upon for any matter affecting patentability. *See* 37 C.F.R. 1.104(c)(3).

A single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. *See Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005). A patent claim is also invalid for obviousness under 35 U.S.C. §103 where the differences between the claimed invention and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." *See* 35 U.S.C. §103. The Supreme Court recently relaxed the Federal Circuit's requirement of a "teaching/suggestion/motivation test," and instead held that "[t]he combination of familiar elements according to a know method is likely to be obvious when it does no more than yield predictable results." *See KSR International Co. v. Teleflex Inc. et al., 127 S. Ct. 1727, 1739* (U.S. April 30, 2007). The Court noted that "[w]hen a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation" of an existing system, then "§103 likely bars its patentability." *See* Id. at 1740; *see also* Examination Guideline for Determining Obviousness in View of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.*, at 57531-32 ("Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results" provides a rational to reject a claim under 35 U.S.C. §103.)

Requestor believes that every aspect of claims 1-16 of the '629 patent was known and publicly available to those skilled in the field of LCD technology, thus rendering claims 1-16 invalid.

A. European Patent Application 0887695 to Hirabayashi Raises A Substantial New Question of Patentability and Anticipates Claims 1-5, 7-13, and 15-16 of the '629 Patent

Hirabayashi was filed with the European Patent Office on June 17, 1998 and was published on Dec. 30, 1998. Because Hirabayashi was published more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability as to claims 1-5, 7-13, and 15-16 is raised by Hirabayashi. Hirabayashi was not considered by the Patent Office during the prosecution of the '629 patent. As discussed above, the Patent Office, without knowledge of Hirabayashi, allowed the'629 patent on the rationale that the art did not teach or suggest:

> An array substrate for display, comprising: a layer of an insulating substrate, *having an area*;…dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Hirabayashi teaches this feature. *See e.g.,* Hirabayashi, Fig. 1 (the hatch pattern); col. 9, ll. 35-42; col. 11, ll. 19-24. **Hirabayashi teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record**. **Thus a reasonable examiner would consider these teachings of Hirabayashi important to the patentability of the '629 patent and new and non-cumulative.** As such, Requestor believes that these teachings of Hirabayashi raise a substantial new question of patentability with respect to independent claims 1 and 9, and consequently claims 2-5 and 7-8 dependent on claim 1 and claims 10-13 and 15-16 dependent on claim 9.

1. Hirabayashi Is New, Non-Cumulative Art Because It Discloses the Identified Allowable Feature of the '629 Patent, Dummy Patterns Comprising at Least about 30% of the Area

Hirabayashi discloses an electro-optical device substrate that provides a configuration to achieve uniform polishing across the entire substrate. *See e.g.,* Hirabayashi, Abstract.

Hirabayashi describes that in order to obtain a uniform level across the substrate, dummy patterns are included at various locations, such as the area surrounding the pixel region 20 as well as near the terminal pads 26. *See e.g.,* Hirabayashi, col. 11, ll. 19-24. In other words, "the surface level is made uniform over the entire surface" of the substrate. *See e.g.,* Hirabayashi col. 9, ll. 43-50; . Additionally, Hirabayashi teaches in one embodiment the dummy patterns are "formed such that the pattern density reaches almost 100% in the entire region at the exterior of the pixel region and the peripheral circuit region." *See e.g.,* Hirabayashi col. 19, ll. 49-56; see also col. 20, ll.22-27. For example, the dummy patterns, shown in the hatch pattern in Fig. 1 below, cover almost the entire substrate outside the pixel region, including the region surrounding the pixel region 20 as well as the region between the pixel region 20 and the terminal pads 26. *See e.g.,* Hirabayashi, Fig. 1; co. 9, ll. 35-42; col. 11, ll. 19-24.

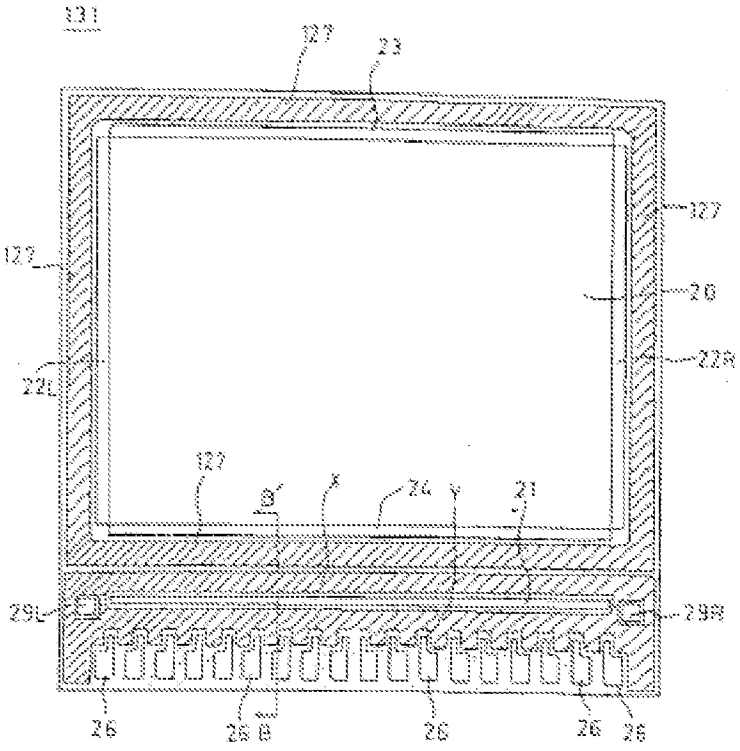


Fig. 1

In other words, **Hirabayashi discloses an insulating substrate having an area, with dummy patterns comprising 30% of the area, which was identified as the allowable subject matter of claims 1 and 9 of the '629 patent.**

Hirabayashi also describes that the dummy patterns are "electrically floating" or "isolated patterns" made with the same structure and at the same time as the wiring layer. *See e.g.,* Hirabayashi, col. 11, l. 57- col. 12, l. 6; col. 18, ll. 48-54; col. 19, ll. 15-19; col. 20, l. 55 - col. 21, l. 4. An example of a closer top view of the dummy patterns, shown as the hatch pattern in Figs. 4-7, demonstrates that the dummy patterns are not in contact with the wiring and are situated between the connection pads and the pixel electrodes as required by claims 1 and 9 of the '629 patent. *See e.g.,* Hirabayashi, Fig. 5 (showing that the dummy patterns, the hatched rectangles, do not contact the wirings Lin or Lout).

2. Hirabayashi Discloses Each and Every Element of Claims 1-5, 7-13, and 15-16

Regarding each element of claim 1, Hirabayashi discloses an array substrate for display (*See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1); including an insulating substrate (*See e.g.*, Hirabayashi, col. 31, ll. 16-23), having an area (*See e.g.*, Hirabayashi, Figs. 1 and 4-6); a thin film transistor array formed on the insulating substrate (*See e.g.*, Hirabayashi, col. 31, ll. 16-23); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18); pixel electrodes (*See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and

the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Hirabayashi, Figs. 1, 4-6, (dummy patterns shown in hatch pattern); col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54.

Regarding each element of claim 9, Hirabayashi discloses a method for forming an array substrate for display, comprising (*See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1): forming a layer of an insulating substrate (*See e.g.*, Hirabayashi, col. 31, ll. 16-23), having an area (*See e.g.*, Hirabayashi, Figs. 1 and 4-6); forming a thin film transistor array formed on the insulating substrate (*See e.g.*, Hirabayashi, col. 31, ll. 16-23); each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array (*See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin); forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18); forming pixel electrodes (*See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7); and forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Hirabayashi, Figs. 1, 4-6, (dummy patterns shown in hatch pattern); col. 11, l. 57 - col. 12, l. 6, ll. 35-42; col. 11, ll. 19-24; col. 18, ll. 52-54. Accordingly, Hirabayashi discloses each and every element of claims 1 and 9.

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof

(claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Regarding dependent claims 2-5 and 10-13 of the '629 patent, Hirabayashi describes that the wiring comprise a multi-layer structure of titanium, titanium nitride, aluminum, and titanium nitride, respectively. *See e.g.*, Hirabayashi, col. 16, ll. 19-22. Thus, Hirabayashi discloses wiring including at least an upper layer and lower layer of conductive materials (claims 2 and 10), with the lower layer of aluminum (claim 3 and 11) and the upper layer of titanium nitride (claims 4, 5, 12, and 13). *See e.g.*, Hirabayashi, col. 16, ll. 19-22. Therefore, Hirabayashi meets the limitations of claims 2-5 and 10-13 of the '629 patent.

Regarding dependent claims 7-8 and 15-16, Hirabayashi inherently teaches the limitation of these claims, namely that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant. As demonstrated by the Examiner in the prosecution of the '629 patent, disclosure of materials such as those identified in the '629 APA, molybdenum, chromium, titanium, or tantalum, for the upper layer wiring meet the limitation of claims 7-8 and 15-16. For example, the examiner stated that because Song taught a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum the limitation of claims 7-8 and 15-16 were met. See '629 file history, Office Action dated May 29, 2003 at page 3. Furthermore, it is well known in the industry that the upper layer material of Hirabayashi, titanium nitride, inherently does not become insoluble in acid or alkaline etchants. See Ex N, Sandhu et al., Metalorganic Chemical Vapor Deposition of

TiN films for Advanced Metallization, Appl. Phys. Lett. 62 (3), 18 Jan. 1993 at 240- 241. Therefore, Hirabayashi meets the limitations of claims 7-8 and 15-16 of the '629 patent.

Accordingly, Hirabayashi discloses every element, and thus fully anticipates, claims 1-5, 7-13, and 15-16 of the '629 patent. A detailed element by element analysis is provided in the claim chart attached as Appendix CC1.

B. European Patent Application 0887695 to Hirabayashi in view of U.S. Patent No. 6,163,356 to Song Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent Obvious

Song was filed with the U.S. Patent Office on Jul. 24, 1997 and was issued on Dec. 19, 2000. Because Song issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Hirabayashi in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. **However, Song was not considered in conjunction with Hirabayashi, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Hirabayashi provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.,* Hirabayashi, Fig. 1 (the hatch pattern); col. 9, ll. 35-42; col. 11, ll. 19-24), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Hirabayashi and Song important to the patentability of the '629 patent and new and non-cumulative.** As such, Hirabayashi in view of Song raises a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Hirabayashi Discloses Each and Every Element of Claims 1 and 9

As discussed above, Hirabayashi discloses each and every element of claims 1 and 9. Hirabayashi includes dummy patterns, for example the hatch pattern of Fig. 1, covering almost all of the area of the substrate outside of the pixel region 20, including the area between the pixel region 20 and the terminal pads 26. *See e.g.,* Hirabayashi, Fig. 1, the hatch pattern; col. 9, ll. 35-42; col. 11, ll. 19-24; col. 16, l. 65- col. 17, l. 3. Hirabayashi provides a configuration with dummy patterns arranged near the terminal pads allowing the surface level to be substantially the same as the surface level of the pixel region. In other words, "the surface level is made uniform over the entire surface" of the substrate. *See e.g.,* Hirabayashi col. 9, ll. 43-50. Additionally, Hirabayashi teaches in one embodiment the dummy patterns are "formed such that the pattern density reaches almost 100% in the entire region at the exterior of the pixel region and the peripheral circuit region." *See e.g.,* Hirabayashi col. 19, ll. 49-56; see also col. 20, ll. 22-27. Thus, the dummy patterns disclosed in Hirabayashi would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads and that they comprise 30% of the area, as required by claims 1 and 9 of the '629 patent.

Hirabayashi also describes that the dummy patterns are "electrically floating" or "isolated patterns" made with the same structure and at the same time as the wiring layer. *See e.g.,* Hirabayashi, col. 11, l. 57- col. 12, l. 6; col. 18, ll. 48-54; col. 19, ll. 15-19; col. 20, l. 55 - col. 21, l. 4. An example of a closer top view of the dummy patterns, shown as the hatch pattern in Figs. 4-7, demonstrates that the dummy patterns are not in contact with the wiring as required by claims 1 and 9 of the '629 patent. *See e.g.,* Hirabayashi, Fig. 5 (showing that the dummy patterns, the hatched rectangles, do not contact the wirings Lin or Lout).

Regarding the remaining elements of claims 1 and 9, Hirabayashi discloses an array substrate for display (*See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1); including an insulating

substrate (*See e.g.*, Hirabayashi, col. 31, ll. 16-23), having an area (*See e.g.*, Hirabayashi, Figs. 1 and 4-6); a thin film transistor array formed on the insulating substrate (*See e.g.*, Hirabayashi, col. 31, ll. 16-23); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18); and pixel electrodes (*See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7). Accordingly, Hirabayashi discloses each and every element of claims 1 and 9.[1]

2. Song Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. **As noted by the examiner during the prosecution of the '629 patent, this wiring structure of Song meets all**

[1] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Hirabayashi disclosures.

of the limitations of claims 2-8 and 10-16. See '629 File History, Office Action dated May 29, 2003 at page 3. Namely, Song discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum (claim 3 and 11) and the upper layer wiring material can be one of a variety of upper layer wiring materials such as molybdenum (claims 4-6 and 14). Song col 4, ll. 30-50; col. 8 ll. 5-18. The disclosed upper layer wiring material, such as molybdenum, inherently does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

3. The Combined Teachings of Hirabayashi and Song Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Hirabayashi describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. *See e.g.*, Hirabayashi, col. 16, ll. 19-22. Song teaches an improved wiring structure with low resistance and protective covering. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Song for the wiring in Hirabayashi in a predictable way to obtain predictable results.

Accordingly, Hirabayashi in view of Song discloses each and every element, and renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of obviousness by Hirabayashi in view of Song of claims 2-8 and 10-16 of the '629 patent in attached as Appendix CC2.

C. European Patent Application 0887695 to Hirabayashi in view of the '629 Admitted Prior Art Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

A substantial new question of patentability is raised by the Hirabayashi in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. **However, the '629 APA was not considered in conjunction with Hirabayashi, which**

as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Hirabayashi provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.,* Hirabayashi, Fig. 1 (the hatch pattern); col. 9, ll. 35-42; col. 11, ll. 19-24), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Hirabayashi and the '629 APA important to the patentability of the '629 patent and new and non-cumulative.** As such, Hirabayashi in view of the '629 APA raise a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Hirabayashi Discloses Each and Every Element of Claims 1 and 9

As discussed above, Hirabayashi discloses each and every element of claims 1 and 9. Hirabayashi includes dummy patterns, for example the hatch pattern shown in Fig. 1, covering almost all of the area of the substrate outside of the pixel region 20, including the area between the pixel region 20 and the terminal pads 26. *See e.g.,* Hirabayashi, Fig. 1, the hatch pattern; col. 9, ll. 35-42; col. 11, ll. 19-24; col. 16, l. 65- col. 17, l. 3. Hirabayashi provides a configuration with dummy patterns arranged near the terminal pads allowing the surface level to be substantially the same as the surface level of the pixel region. In other words, "the surface level is made uniform over the entire surface" of the substrate. *See e.g.,* Hirabayashi col. 9, ll. 43-50; . Additionally, Hirabayashi teaches in one embodiment the dummy patterns are "formed such that the pattern density reaches almost 100% in the entire region at the exterior of the pixel region and the peripheral circuit region." *See e.g.,* Hirabayashi col. 19, ll. 49-56; see also col. 20, ll.22-27. Thus, the dummy patterns disclosed in Hirabayashi would meet the limitations that the

dummy patterns be located between the pixel electrode and the connection pads and that they comprise 30% of the area, as required by claims 1 and 9 of the '629 patent.

Hirabayashi also describes that the dummy patterns are "electrically floating" or "isolated patterns" made with the same structure and at the same time as the wiring layer. *See e.g.,* Hirabayashi, col. 11, l. 57- col. 12, l. 6; col. 18, ll. 48-54; col. 19, ll. 15-19; col. 20, l. 55 - col. 21, l. 4. An example of a closer top view of the dummy patterns, shown as the hatch pattern in Figs. 4-7, demonstrates that the dummy patterns are not in contact with the wiring as required by claims 1 and 9 of the '629 patent. *See e.g.,* Hirabayashi, Fig. 5 (showing that the dummy patterns, the hatched rectangles, do not contact the wirings Lin or Lout).

Regarding the remaining elements of claims 1 and 9, Hirabayashi discloses an array substrate for display (*See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1); including an insulating substrate (*See e.g.*, Hirabayashi, col. 31, ll. 16-23), having an area (*See e.g.*, Hirabayashi, Figs. 1 and 4-6); a thin film transistor array formed on the insulating substrate (*See e.g.*, Hirabayashi, col. 31, ll. 16-23); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18); and pixel electrodes (*See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7). Accordingly, Hirabayashi discloses each and every element of claims 1 and 9.[2]

2. The '629 APA Discloses Each And Every Element of Claims 2-8 and 10-16

[2] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Hirabayashi disclosures.

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

The '629 APA discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is low resistance aluminum (claim 3 and 11) and the upper layer wiring material of a material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum (claims 4-6 and 14). See e.g., the '629 patent, col. 1, ll. 26-39. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Hirabayashi and the '629 APA Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Hirabayashi describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. *See e.g.*, Hirabayashi, col. 16, ll. 19-22. The '629 APA teaches an improved wiring structure with low resistance and is harder is oxidize. See e.g., the '629 patent, col. 1, ll. 26-39. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual

layer wiring of the '629 APA for the wiring in Hirabayashi in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the upper material of Hirabayashi for the molybdenum as taught in the '629 APA, since molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Hirabayashi in view of the '629 APA discloses each and every element, and renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Hirabayashi in view of the '629 APA of claims 2-8 and 10-16 of the '629 patent in attached as appendix CC3.

D. European Patent Application 0887695 to Hirabayashi in view of U.S. Patent No. 6,157,430 to Kubota Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Kubota was filed with the U.S. Patent Office on Sept. 29, 1997 and was issued on Dec. 5, 2000. Because Kubota issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Hirabayashi in view of Kubota. Neither Hirabayashi nor Kubota were before the Patent Office during the prosecution of the '629 patent. Hirabayashi, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Hirabayashi provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.,* Hirabayashi, Fig. 1 (the hatch pattern); col. 9, ll. 35-42; col. 11, ll. 19-24), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Hirabayashi and Kubota important to the patentability**

of the '629 patent and new and non-cumulative. As such, Hirabayashi in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Hirabayashi Discloses Each and Every Element of Claims 1 and 9 of the '629 Patent

As discussed above, Hirabayashi discloses each and every element of claims 1 and 9. Hirabayashi includes dummy patterns, for example the hatch pattern shown in Fig. 1, covering almost all of the area of the substrate outside of the pixel region 20, including the area between the pixel region 20 and the terminal pads 26. *See e.g.,* Hirabayashi, Fig. 1, the hatch pattern; col. 9, ll. 35-42; col. 11, ll. 19-24; col. 16, l. 65- col. 17, l. 3. Hirabayashi provides a configuration with dummy patterns arranged near the terminal pads allowing the surface level to be substantially the same as the surface level of the pixel region. In other words, "the surface level is made uniform over the entire surface" of the substrate. *See e.g.,* Hirabayashi col. 9, ll. 43-50; . Additionally, Hirabayashi teaches in one embodiment the dummy patterns are "formed such that the pattern density reaches almost 100% in the entire region at the exterior of the pixel region and the peripheral circuit region." *See e.g.,* Hirabayashi col. 19, ll. 49-56; see also col. 20, ll.22-27. Thus, the dummy patterns disclosed in Hirabayashi would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads and that they comprise 30% of the area, as required by claims 1 and 9 of the '629 patent.

Hirabayashi also describes that the dummy patterns are "electrically floating" or "isolated patterns" made with the same structure and at the same time as the wiring layer. *See e.g.,* Hirabayashi, col. 11, l. 57- col. 12, l. 6; col. 18, ll. 48-54; col. 19, ll. 15-19; col. 20, l. 55 - col. 21, l. 4. An example of a closer top view of the dummy patterns, shown as the hatch pattern in Figs. 4-7, demonstrates that the dummy patterns are not in contact with the wiring as required by

claims 1 and 9 of the '629 patent. *See e.g.,* Hirabayashi, Fig. 5 (showing that the dummy patterns, the hatched rectangles, do not contact the wirings Lin or Lout).

Regarding the remaining elements of claims 1 and 9, Hirabayashi discloses an array substrate for display (*See e.g.*, Hirabayashi, col. 1, ll. 1-7, and Fig. 1); including an insulating substrate (*See e.g.*, Hirabayashi, col. 31, ll. 16-23), having an area (*See e.g.*, Hirabayashi, Figs. 1 and 4-6); a thin film transistor array formed on the insulating substrate (*See e.g.*, Hirabayashi, col. 31, ll. 16-23); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Hirabayashi, Fig. 2, item 7; Fig. 5, item Lin); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Hirabayashi, Fig. 10, items 26; col. 14, ll. 16-18); and pixel electrodes (*See e.g.*, Hirabayashi, Fig. 1, item 20; col. 14, ll. 6-7). Accordingly, Hirabayashi discloses each and every element of claims 1 and 9.[3]

2. Kubota Discloses Each and Every Element of Claims 2-8 and 10-16 of the '629 Patent

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is

[3] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Hirabayashi disclosures.

selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Kubota discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum or aluminum alloy (claim 3 and 11) and the upper layer wiring material from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof (claims 4-6 and 14). See e.g., Kubota, col. 4, ll. 39-55. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Hirabayashi and Kubota Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Hirabayashi describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. *See e.g.*, Hirabayashi, col. 16, ll. 19-22. Kubota teaches an improved wiring structure with the upper layer having a high hardness. See e.g., Kubota, col. 4, ll. 39-45. Kubota also recognizes that the benefit of using the two layer structure, aluminum with molybdenum on top, is known in the art for the benefit of the low resistance of aluminum and the anti-oxidation protection of molybdenum. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Kubota for the wiring in Hirabayashi in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the upper material of Hirabayashi for the molybdenum as taught in Kubota, since molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Hirabayashi in view of Kubota discloses each and every element, and renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of obviousness by Hirabayashi in view of Kubota of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC4.

E. U.S. Patent No. 5,850,275 To Watanabe Raises A Substantial New Question of Patentability and Anticipates Claims 1-16 of the '629 Patent

Watanabe '275 was filed with the U.S. Patent Office on Jan. 29, 1997 and was issued on Dec. 15, 1998. Because Watanabe '275 issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability as to claims 1-16 is raised by Watanabe '275. Watanabe '275 was not considered by the Patent Office during the prosecution of the '629 patent. As discussed above, the Patent Office, without knowledge of Watanabe '275, allowed the'629 patent on the rationale that the art did not teach or suggest:

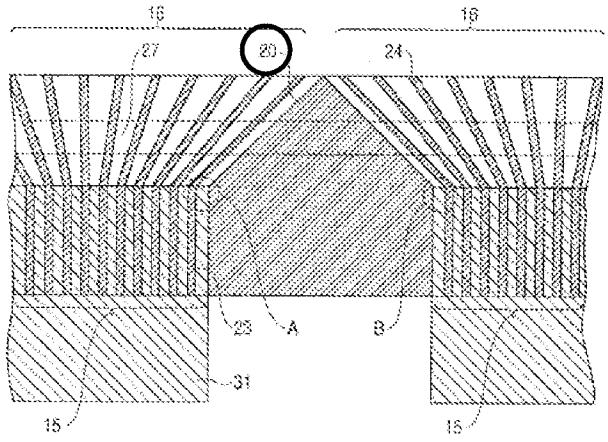
> a layer of an insulating substrate, *having an area*;...dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate.*

As discussed below, Watanabe '275 teaches this feature. See, e.g. Watanabe '275, Fig. 2 (light shield area 20); col. 4, ll. 28-34. **Watanabe '275 teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner woud consider these teachings of Watanabe '275 important to the patentability of the '629 patent and new and non-cumulative art.** As such, Requestor believes that Watanabe '275 raises a substantial new question of patentability with respect to independent claims 1 and 9, and consequently claims 2-8 dependent on claim 1, and claims 10-16 dependent on claim 9.

1. Watanabe '275 Is New, Non-Cumulative Art Because It Discloses the Identified Allowable Feature of the '629 Patent, Dummy Patterns Comprising at Least about 30% of the Area

Watanabe '275 is directed to a liquid crystal display device including light shield areas, or dummy patterns, arranged between the terminal groups and outgoing line groups to reduce uneven brightness. See e.g., Watanabe '275, Abstract; col. 2, lines 44-50, Figs 1-2 and 6. Watanabe '275 includes an insulating substrate with an area including dummy patterns. Id. For example, as shown in Figs 1-2, and 6, areas of light shield areas 20 or dummy patterns are located precisely between the display portion 14, or pixel area, and the terminal groups 15 or connection pads. Moreover, Watanabe '275 describes it is favorable to include a light shield area as large as possible. *See, e.g.,* Watanabe '275, col 4, lines 28-30. One example depicted the light shield area 20 as a pentagon-like shape covering almost the entire area between the terminal groups 23 and outgoing lines 24, shown here in Fig. 2. See, e.g. Watanabe '275, col. 4, ll. 28-34.

FIG. 2



In other words, **Watanabe '275 discloses an insulating substrate having an area, with dummy patterns comprising 30% of the area, which was identified as the allowable subject matter of claims 1 and 9 of the '629 patent.**

Furthermore, the light shield areas or dummy patterns do not contact the outgoing wiring. Watanabe '275, col. 3, ll. 28-35; Figs 2 and 6. Accordingly, the dummy patterns of Watanabe

'275 would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

2. Watanabe '275 Discloses Each and Every Element of Claims 1-16

Regarding each element of claim 1, Watanabe '275 discloses an array substrate for display comprising (*See e.g.*, Watanabe '275 col 3, lines 22-23; Figs 1, 3-4 (liquid crystal panel 11 including a display portion 14): a layer of an insulating substrate, having an area (*See e.g.*, Watanabe '275, col 3, lines 27-30; Figs. 1-4 (TFT glass substrate 21 having an area, for example portion G); a thin film transistor array formed on the insulating substrate (*See e.g.*, Watanabe '275, col. 3:37-44; Fig 1-4 (glass substrate 21 including thin film transistors); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See e.g.*, Watanabe '275, col. 3:37-44; Figs 1-2 (outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Watanabe '275, col. 3:37-44; Figs 1-2 (outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22); pixel electrodes (*See e.g.*, Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4 (a plurality of transparent pixel electrodes 22 are formed in a matrix on the TFT substrate); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. (*See e.g.*, Watanabe '275, col 4, lines 28-30, Figs 1-2, and 6. (a light shield area 20 as shown in figure 2 is located between the terminals 23 and the matrix of pixel electrodes 22, with the light shield area 20 having a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area); *See also*,

Watanabe '275, col 4, lines 28-30 (stating that the light shield area 20 should be as large as possible); *See also*, Watanabe '275, col. 3:28-35; Figs 2 and 6 (stating and depicting that the light shield area is not in contact with the outgoing lines 24)).

Regarding each element of claim 9, Watanabe '275 discloses a method for forming an array substrate for display, comprising (*See e.g.*, Watanabe '275 col 3, lines 22-23; Figs 1, 3-4 (liquid crystal panel 11 including a display portion 14): forming a layer of an insulating substrate, having an area (*See e.g.*, Watanabe '275, col 3, lines 27-30; Figs. 1-4 (TFT glass substrate 21 having an area, for example portion G); forming a thin film transistor array formed on the insulating substrate (*See e.g.*, Watanabe '275, col. 3:37-44; Fig 1-4 (glass substrate 21 including thin film transistors); each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See e.g.*, Watanabe '275, col. 3:37-44; Figs 1-2 (outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22); forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Watanabe '275, col. 3:37-44; Figs 1-2 (outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22); forming pixel electrodes, (*See e.g.*, Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4 (a plurality of transparent pixel electrodes 22 are formed in a matrix on the TFT substrate); and forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. (*See e.g.*, Watanabe '275, col 4, lines 28-30, Figs 1-2, and 6. (a light shield area 20 as shown in figure 2 is located between the terminals 23 and the matrix of pixel electrodes 22, with the light shield area 20 having a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area); *See also*,

Watanabe '275, col 4, lines 28-30 (stating that the light shield area 20 should be as large as possible); *See also*, Watanabe '275, col. 3:28-35; Figs 2 and 6 (stating and depicting that the light shield area is not in contact with the outgoing lines 24)). Accordingly, Watanabe '275 discloses each and every element of claims 1 and 9.

Claims 2-8 and 10-16 of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Regarding dependent claims 2-6 and 10-14 of the '629 patent, Watanabe '275 discloses that the materials for the electrodes can include for example aluminum and molybdenum. See e.g., Watanabe '275, col 4, lines 24-28. Therefore, Watanabe '275 meets the limitations of claims 2-6 and 10-14 of the '629 patent.

Regarding dependent claims 7-8 and 15-16, Watanabe '275 inherently discloses these features. **As demonstrated by the Examiner in the prosecution of the '629 patent, disclosure of materials such as those identified in the '629 APA, molybdenum, chromium, titanium, or tantalum, for the upper layer wiring meet the limitation of claims 7-8 and 15-16, that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.** For example, the examiner stated that because Song taught a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum the limitation of claims 7-

8 and 15-16 were met. See '629 prosecution history, Office Action dated May 29, 2003 at page 3. Similarly, Watanabe '275 teaches including molybdenum, which would inherently be soluble in acid or alkaline etchants. Thus, Watanabe '275 teaches each and every element of claims 7-8 and 15-16 of the '629 patent.

Accordingly, Watanabe '275 discloses each and every element, and thus fully anticipates, claims 1-16 of the '629 patent. A claim chart providing a more detailed element by element analysis is attached as Appendix CC5.

F. U.S. Patent No. 5,850,275 To Watanabe in view of U.S. Patent No. 6,163,356 to Song Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Song was filed with the U.S. Patent Office on Jul. 24, 1997 and was issued on Dec. 19, 2000. Because Song issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Watanabe '275 in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. **However, Song was not considered in conjunction with Watanabe '275, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Watanabe '275 provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g. Watanabe '275, Fig. 2 (light shield area 20); col. 4, ll. 28-34), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Watanabe '275 and Song important to the patentability of the '629 patent and new and non-cumulative.** As such, Watanabe '275 in view of Song raises a

substantial new question of patentability as to as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Watanabe '275 Discloses Each and Every Element of Claims 1 and 9

As discussed above, Watanabe '275 discloses each and every element of claims 1 and 9. Watanabe '275 is directed to a liquid crystal display device including light shield areas, or dummy patterns, arranged between the terminal groups and outgoing line groups to reduce uneven brightness. See e.g., Watanabe '275, Abstract; col. 2, lines 44-50, Figs 1-2 and 6. Watanabe '275 includes an insulating substrate with an area including dummy patterns. For example, as shown in Figs 1-2, and 6, areas of light shield areas 20 or dummy patterns are located precisely between the display portion 14, or pixel area, and the terminal groups 15 or connection pads. Moreover, Watanabe '275 describes it is favorable to include a light shield area as large as possible. One example depicted the light shield area 20 as a pentagon-like shape covering almost the entire area between the terminal groups 23 and outgoing lines 24, shown here in Fig. 2, meeting the 30% of an area requirement. See, e.g. Watanabe '275, col. 4, ll. 28-34. Furthermore, the light shield areas or dummy patterns do not contact the outgoing wiring. Watanabe '275, col. 3, ll. 28-35; Figs 2 and 6. Accordingly, the dummy patterns of Watanabe '275 would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claims 1 and 9, Watanabe '275 discloses an array substrate for display comprising (*See e.g.*, Watanabe '275 col 3, lines 22-23; Figs 1, 3-4 (liquid crystal panel 11 including a display portion 14): a layer of an insulating substrate, having an area (*See e.g.*, Watanabe '275, col 3, lines 27-30; Figs. 1-4 (TFT glass substrate 21 having an area, for example portion G); a thin film transistor array formed on the insulating substrate (*See e.g.*,

Watanabe '275, col. 3:37-44; Fig 1-4 (glass substrate 21 including thin film transistors); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See e.g.*, Watanabe '275, col. 3:37-44; Figs 1-2 (outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Watanabe '275, col. 3:37-44; Figs 1-2 (outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22); pixel electrodes (*See e.g.*, Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4 (a plurality of transparent pixel electrodes 22 are formed in a matrix on the TFT substrate); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. (*See e.g.*, Watanabe '275, col 4, lines 28-30, Figs 1-2, and 6. (a light shield area 20 as shown in figure 2 is located between the terminals 23 and the matrix of pixel electrodes 22, with the light shield area 20 having a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area); *See also*, Watanabe '275, col 4, lines 28-30 (stating that the light shield area 20 should be as large as possible); *See also*, Watanabe '275, col. 3:28-35; Figs 2 and 6 (stating and depicting that the light shield area is not in contact with the outgoing lines 24)). Accordingly, Watanabe '275 discloses each and every element of claims 1 and 9.[4]

2. Song Discloses Each And Every Element of Claims 2-8 and 10-16

[4] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Watanabe '275 disclosures.

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. **As noted by the examiner during the prosecution of the '629 patent, this wiring structure of Song meets all of the limitations of claims 2-8 and 10-16.** See '629 File History, Office Action dated May 29, 2003 at page 3. Namely, Song discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum (claim 3 and 11) and the upper layer wiring material can be one of a variety of upper layer wiring materials such as molybdenum (claims 4-6 and 14). Song col 4, ll. 30-50; col. 8 ll. 5-18. The disclosed upper layer wiring material, such as molybdenum, inherently does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

3. The Combined Teachings of Watanabe '275 and Song Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Watanabe '275 describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. *See e.g.*, Watanabe '275, col. 4, ll. 22-28. Song teaches an improved wiring structure with low resistance and protective covering. See e.g., Song col 4, ll.

30-50; col. 8 ll. 5-18. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Song for the wiring in Watanabe '275 in a predictable way to obtain predictable results.

Accordingly, Watanabe '275 in view of Song discloses each and every element, and render obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Watanabe '275 in view of Song of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC6.

G. U.S. Patent No. 5,850,275 To Watanabe in view of the '629 Admitted Prior Art Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

A substantial new question of patentability is raised by Watanabe '275 in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. **However, the '629 APA was not considered in conjunction with Watanabe '275, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Watanabe '275 provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g. Watanabe '275, Fig. 2 (light shield area 20); col. 4, ll. 28-34), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Watanabe '275 and the '629 APA important to the patentability of the '629 patent and new and non-cumulative.** As such, Watanabe '275 in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Watanabe '275 Discloses Each and Every Element of Claims 1 and 9

As discussed above, Watanabe '275 discloses each and every element of claims 1 and 9. Watanabe '275 is directed to a liquid crystal display device including light shield areas, or dummy patterns, arranged between the terminal groups and outgoing line groups to reduce uneven brightness. See e.g., Watanabe '275, Abstract; col. 2, lines 44-50, Figs 1-2 and 6. Watanabe '275 includes an insulating substrate with an area including dummy patterns. For example, as shown in Figs 1-2, and 6, areas of light shield areas 20 or dummy patterns are located precisely between the display portion 14, or pixel area, and the terminal groups 15 or connection pads. Moreover, Watanabe '275 describes it is favorable to include a light shield area as large as possible. One example depicted the light shield area 20 as a pentagon-like shape covering almost the entire area between the terminal groups 23 and outgoing lines 24, shown here in Fig. 2, meeting the 30% of an area requirement. See, e.g. Watanabe '275, col. 4, ll. 28-34. Furthermore, the light shield areas or dummy patterns do not contact the outgoing wiring. Watanabe '275, col. 3, ll. 28-35; Figs 2 and 6. Accordingly, the dummy patterns of Watanabe '275 would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claims 1 and 9, Watanabe '275 discloses an array substrate for display comprising (*See e.g.*, Watanabe '275 col 3, lines 22-23; Figs 1, 3-4 (liquid crystal panel 11 including a display portion 14): a layer of an insulating substrate, having an area (*See e.g.*, Watanabe '275, col 3, lines 27-30; Figs. 1-4 (TFT glass substrate 21 having an area, for example portion G); a thin film transistor array formed on the insulating substrate (*See e.g.*, Watanabe '275, col. 3:37-44; Fig 1-4 (glass substrate 21 including thin film transistors); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in

communication with at least one of the transistors in the thin film array (*See e.g.*, Watanabe '275, col. 3:37-44; Figs 1-2 (outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Watanabe '275, col. 3:37-44; Figs 1-2 (outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22); pixel electrodes (*See e.g.*, Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4 (a plurality of transparent pixel electrodes 22 are formed in a matrix on the TFT substrate); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. (*See e.g.*, Watanabe '275, col 4, lines 28-30, Figs 1-2, and 6. (a light shield area 20 as shown in figure 2 is located between the terminals 23 and the matrix of pixel electrodes 22, with the light shield area 20 having a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area); *See also*, Watanabe '275, col 4, lines 28-30 (stating that the light shield area 20 should be as large as possible); *See also*, Watanabe '275, col. 3:28-35; Figs 2 and 6 (stating and depicting that the light shield area is not in contact with the outgoing lines 24)).[5]

2. The '629 APA Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected

[5] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Watanabe '275 disclosures.

from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

The '629 APA discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is low resistance aluminum (claim 3 and 11) and the upper layer wiring material of a material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum (claims 4-6 and 14). See e.g., the '629 patent, col. 1, ll. 26-39. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Watanabe '275 and the '629 APA Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Watanabe '275 describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. *See e.g.*, Watanabe '275, col. 4, ll. 22-28. The '629 APA teaches an improved wiring structure with low resistance and is harder is oxidize. See e.g., the '629 patent, col. 1, ll. 26-39. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of the '629 APA for the wiring in Watanabe '275 in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the wiring of Watanabe '275 with the aluminum/molybdenum wiring as taught in the '629 APA, since aluminum provides low

resistance and molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Watanabe '275 in view of the '629 APA discloses each and every element and renders obvious claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Watanabe '275 in view of the '629 APA of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC7.

H. U.S. Patent No. 5,850,275 To Watanabe in view of U.S. Patent No. 6,157,430 to Kubota Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Kubota was filed with the U.S. Patent Office on Sept. 29, 1997 and was issued on Dec. 5, 2000. Because Kubota issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Watanabe '275 in view of Kubota. Neither Watanabe '275 nor Kubota were before the Patent Office during the prosecution of the '629 patent. Watanabe '275, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Watanabe '275 provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g. Watanabe '275, Fig. 2 (light shield area 20); col. 4, ll. 28-34), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Watanabe '275 and Kubota important to the patentability of the '629 patent and new and non-cumulative.** As such, Watanabe '275 in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Watanabe '275 Discloses Each and Every Element of Claims 1 and 9

As discussed above, Watanabe '275 discloses each and every element of claims 1 and 9. Watanabe '275 is directed to a liquid crystal display device including light shield areas, or dummy patterns, arranged between the terminal groups and outgoing line groups to reduce uneven brightness. See e.g., Watanabe '275, Abstract; col. 2, lines 44-50, Figs 1-2 and 6. Watanabe '275 includes an insulating substrate with an area including dummy patterns. For example, as shown in Figs 1-2, and 6, areas of light shield areas 20 or dummy patterns are located precisely between the display portion 14, or pixel area, and the terminal groups 15 or connection pads. Moreover, Watanabe '275 describes it is favorable to include a light shield area as large as possible. One example depicted the light shield area 20 as a pentagon-like shape covering almost the entire area between the terminal groups 23 and outgoing lines 24, shown here in Fig. 2, meeting the 30% of an area requirement. See, e.g. Watanabe '275, col. 4, ll. 28-34. Furthermore, the light shield areas or dummy patterns do not contact the outgoing wiring. Watanabe '275, col. 3, ll. 28-35; Figs 2 and 6. Accordingly, the dummy patterns of Watanabe '275 would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claim 1, Watanabe '275 discloses an array substrate for display comprising (*See e.g.*, Watanabe '275 col 3, lines 22-23; Figs 1, 3-4 (liquid crystal panel 11 including a display portion 14): a layer of an insulating substrate, having an area (*See e.g.*, Watanabe '275, col 3, lines 27-30; Figs. 1-4 (TFT glass substrate 21 having an area, for example portion G); a thin film transistor array formed on the insulating substrate (*See e.g.*, Watanabe '275, col. 3:37-44; Fig 1-4 (glass substrate 21 including thin film transistors); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in

communication with at least one of the transistors in the thin film array (*See e.g.*, Watanabe '275, col. 3:37-44; Figs 1-2 (outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Watanabe '275, col. 3:37-44; Figs 1-2 (outgoing lines 24 to connect the terminals 23 to the respective pixel electrodes 22); pixel electrodes (*See e.g.*, Watanabe '275, col. 1, ll. 37-39; Figs 1, 3-4 (a plurality of transparent pixel electrodes 22 are formed in a matrix on the TFT substrate); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. (*See e.g.*, Watanabe '275, col 4, lines 28-30, Figs 1-2, and 6. (a light shield area 20 as shown in figure 2 is located between the terminals 23 and the matrix of pixel electrodes 22, with the light shield area 20 having a pentagon shape covering almost the entire area G and thus would consist at least 30% of the area); *See also*, Watanabe '275, col 4, lines 28-30 (stating that the light shield area 20 should be as large as possible); *See also*, Watanabe '275, col. 3:28-35; Figs 2 and 6 (stating and depicting that the light shield area is not in contact with the outgoing lines 24)). Accordingly, Watanabe '275 discloses each and every element of claims 1 and 9.[6]

2. Kubota Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of

[6] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Watanabe '275 disclosures.

aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Kubota discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum or aluminum alloy (claim 3 and 11) and the upper layer wiring material from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof (claims 4-6 and 14). See e.g., Kubota, col. 4, ll. 39-55. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Watanabe '275 and Kubota Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Watanabe '275 describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. *See e.g.*, Watanabe '275, col. 4, ll. 22-28. Kubota teaches an improved wiring structure with the upper layer having a high hardness. See e.g., Kubota, col. 4, ll. 39-45. Kubota also recognizes that the benefit of using the two layer structure, aluminum with molybdenum on top, is known in the art for the benefit of the low resistance of aluminum and the anti-oxidation protection of molybdenum. *See e.g.*, Watanabe '275, col. 4, ll. 25-54. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Kubota for the

wiring in Watanabe '275 in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the wiring of Watanabe '275 for the aluminum/molybdenum wiring as taught in Kubota, since aluminum provides low resistance and molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Watanabe '275 in view of Kubota discloses each and every element, and thus renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Watanabe '275 in view of Kubota of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC8.

I. U.S. Patent No. 6,862,069 to Kwak et al Raises A Substantial New Question of Patentability and Anticipates Claims 1-2 and 9-10 of the '629 Patent

Kwak was filed with the U.S. Patent Office on Dec. 29, 2000 and was issued on Mar. 1, 2005. Because Kwak was filed in the U.S. before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(e).

A substantial new question of patentability as to claims 1-2 and 9-10 is raised by Kwak. Kwak was not considered by the Patent Office during the prosecution of the '629 patent. As discussed above, the Patent Office, without knowledge of Kwak, allowed the'629 patent on the rationale that the art did not teach or suggest:

> a layer of an insulating substrate, *having an area*;...dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed below, Kwak teaches this feature. See, e.g., Kwak, col. 4, ll. 28-41, Fig 7 (item 36). **Kwak teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider these teachings of Kwak important to the**

patentability of the '629 patent and new and non-cumulative. As such, Requestor believes that Kwak raises a substantial new question of patentability as to least independent claims 1 and 9 and claim 2, dependent on claim 1, and claim 10, dependent from claim 9.

1. Kwak Is New, Non-Cumulative Art Because It Discloses the Identified Allowable Feature of the '629 Patent, Dummy Patterns Comprising at Least about 30% of the Area

Kwak discloses a liquid crystal display device including dummy patterns between the gate links and between the data links. See. e.g., Kwak, Abstract, Figs. 7-12. Kwak describes a concern with the cell gap in a specified region, the etching area EA, between the data links or wiring 34 and gate links or wiring 15, as shown in Figs. 3 and 5. Kwak proposes incorporating dummy patterns to fill most of the etching area EA as shown in Figs 10 and 12 to achieve a uniform cell gap. See, e.g., Kwak, col. 4, lines 25-33. As shown, for example, in Fig. 7 the dummy patterns 36 are between the display area and the connection pads 14 and are not in contact with the wiring 15. See, e.g., Kwak, Fig. 7.

Furthermore, the cross sectional view identifies the minimal distance exposed between the dummy patterns 36 (circled below) and the gate or data wiring 15, shown here for example in

FIG 11

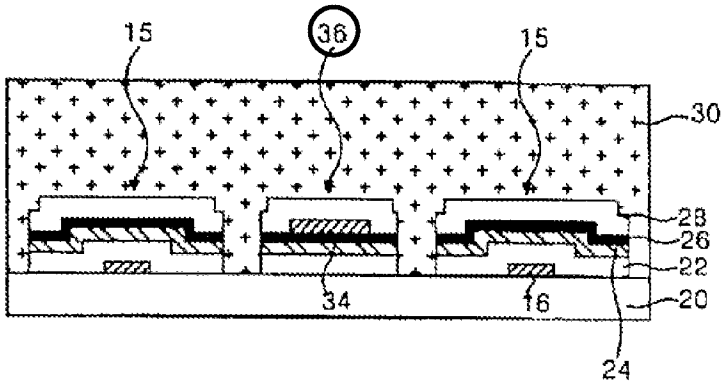


Fig. 11. Kwak describes that the distance between the gate links in the convention art was

100 μm, but Kwak teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus the dummy patterns would comprise the majority of the distance between each gate or data link, or approximately 80 μm of the conventional 100 μm between gate links, meeting the at least 30% of the area limitation. See, e.g., Kwak, col. 4, ll. 28-41. In other words, **Kwak discloses an insulating substrate having an area, with dummy patterns comprising 30% of the area, which was identified as the allowable subject matter of claims 1 and 9 of the '629 patent.** Further, the dummy patterns of Kwak would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads and that they not be in contact with the wiring, as required by claims 1 and 9 of the '629 patent. See, e.g., Kwak, Fig. 7.

2. Kwak Discloses Each and Every Element of Claims 1-2 and 9-10

Regarding each element of claim 1, Kwak discloses an array substrate for display (*See e.g.*, Kwak, col. 1, ll. 34-36, Fig. 1 (disclosing a liquid crystal display panel includes a display part 10)): including an insulating substrate, having an area (*See e.g.*, col. 2, ll. 6-9, 20-23, Figs 1 and 3 (disclosing a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15); a thin film transistor array formed on the insulating substrate (*See e.g.*, Kwak at col. 1, ll. 43-45, Fig. 1 (disclosing that at each crossover point of the gate lines and data lines there is a thin film transistor)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12 (disclosing gate links 15 and data links 33 are formed on transparent substrate 20 that connect to TFTs at the crossover points)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9 (disclosing gate pads 14 and data pad 32 that contact

the gate links 15 and data links 33)); pixel electrodes (*See e.g.*, Kwak at col. 1, ll. 45-46 (disclosing a pixel electrode is connected to the TFT to drive the liquid crystal cell)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Kwak at Figs 7 and 9 (disclosing dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10); *see also* Kwak at col. 4, ll. 28-41 (stating that the majority of the area between the gate links, which in the convention art was 100 μm, is covered by dummy patterns, or approximately 80 μm), *see also* Kwak at Figs 7-12 (disclosing that the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33).

Regarding each element of claim 9, Kwak discloses a method for forming an array substrate for display, comprising (*See e.g.*, Kwak, col. 1, ll. 34-36, Fig. 1 (disclosing a liquid crystal display panel includes a display part 10)): forming a layer of an insulating substrate, having an area (*See e.g.*, col. 2, ll. 6-9, 20-23, Figs 1 and 3 (disclosing a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15); forming a thin film transistor array formed on the insulating substrate (*See e.g.*, Kwak at col. 1, ll. 43-45, Fig. 1 (disclosing that at each crossover point of the gate lines and data lines there is a thin film transistor)); each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array (*See* e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12 (disclosing gate links 15 and data links 33 are formed on transparent substrate 20 that connect to TFTs at the crossover points)); forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9 (disclosing gate pads

14 and data pad 32 that contact the gate links 15 and data links 33)); forming pixel electrodes (*See e.g.*, Kwak at col. 1, ll. 45-46 (disclosing a pixel electrode is connected to the TFT to drive the liquid crystal cell)); and forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Kwak at Figs 7 and 9 (disclosing dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10); *see also* Kwak at col. 4, ll. 28-41 (stating that the majority of the area between the gate links, which in the convention art was 100 μm, is covered by dummy patterns, or approximately 80 μm), *see also* Kwak at Figs 7-12 (disclosing that the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33). Accordingly, Kwak discloses each and every element of claims 1 and 9.

Claims 2 and 10 of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10). Kwak discloses the gate links and data links comprise multiple layers of conductive materials, such as metal layer 16 and 34, amorphous silicon 24 , and n+ layer 26. *See e.g.*, Kwak at col. 4, ll. 21-25. Therefore, Kwak meets the limitations of claims 2 and 10 of the '629 patent.

Accordingly, Kwak discloses each and every element, and thus fully anticipates, claims 1-2 and 9-10 of the '629 patent. A claim chart providing a detailed element by element analysis is attached as Appendix CC9.

J. U.S. Patent No. 6,862,069 to Kwak in view of U.S. Patent No. 6,163,356 to Song Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Song was filed with the U.S. Patent Office on Jul. 24, 1997 and was issued on Dec. 19, 2000. Because Song issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Kwak in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. **However, Song was not considered in conjunction with Kwak, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Kwak provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Kwak, col. 4, ll. 28-41, Fig 7 (item 36), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Kwak and Song important to the patentability of the '629 patent and new and non-cumulative.** As such, Kwak in view of Song constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Kwak Discloses Each and Every Element of Claims 1 and 9

As discussed above, Kwak discloses each and every element of claims 1 and 9. Kwak discloses a liquid crystal display device including dummy patterns between the gate links and between the data links. See. e.g., Kwak, Abstract, Figs. 7-12. Kwak describes a concern with the cell gap in a specified region, the etching area EA, between the data links or wiring 34 and gate links or wiring 15, as shown in Figs. 3 and 5. Kwak proposes incorporating dummy patterns to fill most of the etching area EA as shown in Figs 10 and 12 to achieve a uniform cell gap. See,

e.g., Kwak, col. 4, lines 25-33. As shown, for example, in Fig. 7 the dummy patterns 36 are between the display area and the connection pads 14 and are not in contact with the wiring 15.

Furthermore, the cross sectional view identifies the minimal distance exposed between the dummy patterns and the gate or data wiring, for example shown here in Fig. 11. Kwak describes that the distance between the gate links in the convention art was 100 μm, but Kwak '069 teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus the dummy patterns would comprise the majority of the distance between each gate or data link, or approximately 80 μm of the conventional 100 μm between gate links, meeting the at least 30% of the area limitation. See, e.g., Kwak, col. 4, ll. 28-41. Accordingly, the dummy patterns of Kwak would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claims 1 and 9, Kwak discloses an array substrate for display (*See e.g.*, Kwak, col. 1, ll. 34-36, Fig. 1 (disclosing a liquid crystal display panel includes a display part 10)): including an insulating substrate, having an area (*See e.g.*, col. 2, ll. 6-9, 20-23, Figs 1 and 3 (disclosing a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15); a thin film transistor array formed on the insulating substrate (*See e.g.*, Kwak at col. 1, ll. 43-45, Fig. 1 (disclosing that at each crossover point of the gate lines and data lines there is a thin film transistor)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12 (disclosing gate links 15 and data links 33 are formed on transparent substrate 20 that connect to TFTs at the crossover points)); connections pads, each connection

pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9 (disclosing gate pads 14 and data pad 32 that contact the gate links 15 and data links 33)); pixel electrodes (*See e.g.*, Kwak at col. 1, ll. 45-46 (disclosing a pixel electrode is connected to the TFT to drive the liquid crystal cell)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Kwak at Figs 7 and 9 (disclosing dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10); *see also* Kwak at col. 4, ll. 28-41 (stating that the majority of the area between the gate links, which in the convention art was 100 μm, is covered by dummy patterns, or approximately 80 μm), *see also* Kwak at Figs 7-12 (disclosing that the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33). Accordingly, Kwak discloses each and every element of claims 1 and 9.[7]

2. Song Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is

[7] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Kwak disclosures.

selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. **As noted by the examiner during the prosecution of the '629 patent, this wiring structure of Song meets all of the limitations of claims 2-8 and 10-16.** See '629 File History, Office Action dated May 29, 2003 at page 3. Namely, Song discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum (claim 3 and 11) and the upper layer wiring material can be one of a variety of upper layer wiring materials such as molybdenum (claims 4-6 and 14). Song col 4, ll. 30-50; col. 8 ll. 5-18. The disclosed upper layer wiring material, such as molybdenum, inherently does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

3. The Combined Teachings of Kwak and Song Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Kwak describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. See, e.g., Kwak at col. 4, ll. 21-25. Song teaches an improved wiring structure with low resistance and protective covering. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Song for the wiring in Kwak in a predictable way to obtain predictable results.

Accordingly, Kwak in view of Song discloses each and every element and renders obvious claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Kwak in view of Song of claims 2-8 and 10-16 of the '629 patent is attached as appendix CC10.

K. U.S. Patent No. 6,862,069 to Kwak in view of the '629 Admitted Prior Art Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

A substantial new question of patentability is raised by Kwak in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. **However, the '629 APA was not considered in conjunction with Kwak, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Kwak provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Kwak, col. 4, ll. 28-41, Fig 7 (item 36)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Kwak and the '629 APA important to the patentability of the '629 patent and non-cumulative art.** As such, Kwak in view of the '629 APA constitutes a substantial new question of patentability.

1. Kwak Discloses Each and Every Element of Claims 1 and 9

As discussed above, Kwak discloses each and every element of claims 1 and 9. Kwak discloses a liquid crystal display device including dummy patterns between the gate links and between the data links. See. e.g., Kwak, Abstract, Figs. 7-12. Kwak describes a concern with the cell gap in a specified region, the etching area EA, between the data links or wiring 34 and gate links or wiring 15, as shown in Figs. 3 and 5. Kwak proposes incorporating dummy patterns to fill most of the etching area EA as shown in Figs 10 and 12 to achieve a uniform cell gap. See, e.g., Kwak, col. 4, lines 25-33. As shown, for example, in Fig. 7 the dummy patterns 36 are between the display area and the connection pads 14 and are not in contact with the wiring 15.

Furthermore, the cross sectional view identifies the minimal distance exposed between

the dummy patterns and the gate or data wiring, for example shown here in Fig. 11. Kwak describes that the distance between the gate links in the convention art was 100 μm, but Kwak '069 teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus the dummy patterns would comprise the majority of the distance between each gate or data link, or approximately 80 μm of the conventional 100 μm between gate links, meeting the 30% of the area limitation. See, e.g., Kwak, col. 4, ll. 28-41. Accordingly, the dummy patterns of Kwak would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claims 1 and 9, Kwak discloses an array substrate for display (*See e.g.*, Kwak, col. 1, ll. 34-36, Fig. 1 (disclosing a liquid crystal display panel includes a display part 10)): including an insulating substrate, having an area (*See e.g.*, col. 2, ll. 6-9, 20-23, Figs 1 and 3 (disclosing a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15); a thin film transistor array formed on the insulating substrate (*See e.g.*, Kwak at col. 1, ll. 43-45, Fig. 1 (disclosing that at each crossover point of the gate lines and data lines there is a thin film transistor)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12 (disclosing gate links 15 and data links 33 are formed on transparent substrate 20 that connect to TFTs at the crossover points)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9 (disclosing gate pads 14 and data pad 32 that contact the gate links 15 and data links 33)); pixel electrodes (*See e.g.*, Kwak at col. 1,

ll. 45-46 (disclosing a pixel electrode is connected to the TFT to drive the liquid crystal cell)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Kwak at Figs 7 and 9 (disclosing dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10); *see also* Kwak at col. 4, ll. 28-41 (stating that the majority of the area between the gate links, which in the convention art was 100 μm, is covered by dummy patterns, or approximately 80 μm), *see also* Kwak at Figs 7-12 (disclosing that the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33). Accordingly, Kwak discloses each and every element of claims 1 and 9.[8]

2. The '629 APA Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

[8] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Kwak disclosures.

The '629 APA discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is low resistance aluminum (claim 3 and 11) and the upper layer wiring material of a material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum (claims 4-6 and 14). See e.g., the '629 patent, col. 1, ll. 26-39. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Kwak and the '629 APA Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Kwak describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. See, e.g., Kwak at col. 4, ll. 21-25. The '629 APA teaches an improved wiring structure with low resistance and is harder is oxidize. See e.g., the '629 patent, col. 1, ll. 26-39. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of the '629 APA for the wiring in Kwak in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the wiring of Kwak for the aluminum/molybdenum wiring as taught in the '629 APA, since aluminum has low resistance and molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Kwak in view of the '629 APA discloses each and every element and renders obvious claims 2-8 and 9-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Kwak in view of the '629 APA of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC11.

L. U.S. Patent No. 6,862,069 to Kwak in view of U.S. Patent No. 6,157,430 to Kubota Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Kubota was filed with the U.S. Patent Office on Sept. 29, 1997 and was issued on Dec. 5, 2000. Because Kubota issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Kwak in view of Kubota. Neither Kwak nor Kubota were before the Patent Office during the prosecution of the '629 patent. Kwak, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Kwak provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Kwak, col. 4, ll. 28-41, Fig 7 (item 36)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Kwak and Kubota important to the patentability of the '629 patent and new and non-cumulative.** As such, Kwak in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Kwak Discloses Each and Every Element of Claims 1 and 9

As discussed above, Kwak discloses each and every element of claims 1 and 9. Kwak discloses a liquid crystal display device including dummy patterns between the gate links and between the data links. See. e.g., Kwak, Abstract, Figs. 7-12. Kwak describes a concern with the cell gap in a specified region, the etching area EA, between the data links or wiring 34 and gate links or wiring 15, as shown in Figs. 3 and 5. Kwak proposes incorporating dummy patterns to fill most of the etching area EA as shown in Figs 10 and 12 to achieve a uniform cell gap. See,

e.g., Kwak, col. 4, lines 25-33. As shown, for example, in Fig. 7 the dummy patterns 36 are between the display area and the connection pads 14 and are not in contact with the wiring 15.

Furthermore, the cross sectional view identifies the minimal distance exposed between the dummy patterns and the gate or data wiring, for example shown here in Fig. 11. Kwak describes that the distance between the gate links in the convention art was 100 μm, but Kwak '069 teaches that the distance between the gate links and the dummy patterns is only 10 μm, thus the dummy patterns would comprise the majority of the distance between each gate or data link, or approximately 80 μm of the conventional 100 μm between gate links, meeting the at least 30% of the area limitation. See, e.g., Kwak, col. 4, ll. 28-41. Accordingly, the dummy patterns of Kwak would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claims 1 and 9, Kwak discloses an array substrate for display (*See e.g.*, Kwak, col. 1, ll. 34-36, Fig. 1 (disclosing a liquid crystal display panel includes a display part 10)): including an insulating substrate, having an area (*See e.g.*, col. 2, ll. 6-9, 20-23, Figs 1 and 3 (disclosing a transparent substrate 20 having an area, such as the etching area EA between gate link parts 15); a thin film transistor array formed on the insulating substrate (*See e.g.*, Kwak at col. 1, ll. 43-45, Fig. 1 (disclosing that at each crossover point of the gate lines and data lines there is a thin film transistor)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Kwak at col. 1, ll. 43-46, col. 2, ll. 1-9, 26-30; col. 4, ll. 21-25, 49; Figs 1-12 (disclosing gate links 15 and data links 33 are formed on transparent substrate 20 that connect to TFTs at the crossover points)); connections pads, each connection

pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Kwak at col. 2, ll. 1-2, 26-27; col. 4, ll. 64-67; col. 5, ll. 6-10; Figs 2, 4, 7, and 9 (disclosing gate pads 14 and data pad 32 that contact the gate links 15 and data links 33)); pixel electrodes (*See e.g.*, Kwak at col. 1, ll. 45-46 (disclosing a pixel electrode is connected to the TFT to drive the liquid crystal cell)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Kwak at Figs 7 and 9 (disclosing dummy patterns 36 and 38 are located between gate pads 14 and data pads 32 and the display part 10); *see also* Kwak at col. 4, ll. 28-41 (stating that the majority of the area between the gate links, which in the convention art was 100 μm, is covered by dummy patterns, or approximately 80 μm), *see also* Kwak at Figs 7-12 (disclosing that the dummy patterns 36 and 38 of Kwak do not contact the gate links 15 or data links 33). Accordingly, Kwak discloses each and every element of claims 1 and 9.[9]

2. The '629 APA Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is

[9] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Kwak disclosures.

selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Kubota discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum or aluminum alloy (claim 3 and 11) and the upper layer wiring material from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof (claims 4-6 and 14). See e.g., Kubota, col. 4, ll. 39-55. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Kwak and Kubota Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Kwak describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. See, e.g., Kwak at col. 4, ll. 21-25. Kubota teaches an improved wiring structure with the upper layer having a high hardness. See e.g., Kubota, col. 4, ll. 39-45. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Kubota for the wiring in Kwak in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the wiring of Kwak for the aluminum/molybdenum wiring as taught in Kubota, since aluminum has a low resistance molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Kwak in view of Kubota discloses each and every element, and thus renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by

element analysis of the obviousness by Kwak in view of Kubota of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC12.

M. Japanese Pub. No. H10-333151 to Yoshinori et al. Raises A Substantial New Question of Patentability and Anticipates Claims 1-5, 7-13, and 15-16 of the '629 Patent

Yoshinori filed with the Japanese Patent Office on May 28, 1997 and was published on Dec. 18, 1998 Because Yoshinori was published more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

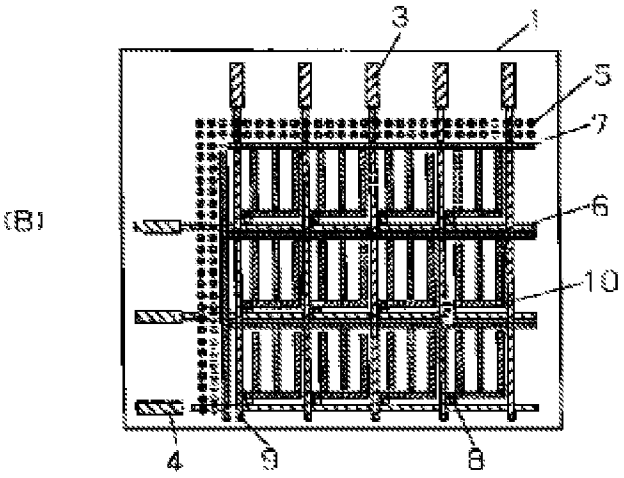
A substantial new question of patentability as to claims 1-5,7-13, and 15-16 is raised by Yoshinori. Yoshinori was not considered by the Patent Office during the prosecution of the '629 patent. As discussed above, the Patent Office, without knowledge of Yoshinori, allowed the'629 patent on the rationale that the art did not teach or suggest:

> a layer of an insulating substrate, *having an area*;...dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Yoshinori teaches this feature. See, e.g., Yoshinori, ¶ 20, Fig 1 (B) (interval projection steps 5). **Yoshinori teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider these teachings of Yoshinori important to the patentability of the '629 patent and new and non-cumulative.** As such, Requestor believes that these teachings of Yoshinori raise a substantial new question of patentability with respect to independent claims 1 and 9, and consequently claims 2-5 and 7-8, dependent on claim 1, and claims 10-13 and 15-16, dependent on claim 9.

1. Yoshinori Is New, Non-Cumulative Art Because It Discloses the Identified Allowable Feature of the '629 Patent, Dummy Patterns Comprising at Least about 30% of the Area

Yoshinori discloses a liquid crystal display device including equal-interval projection steps 5, or dummy patterns, around the display area. See, e.g., Yoshinori, Abstract; Fig 1. As depicted here in Fig. 1 (B), the projection steps 5 are located between the display region 2 and the connection pads 3 and do not contact the wiring.



Further, Yoshinori describes an example of the projection steps having a diameter 5 μm and being located at 5 μm intervals. See, e.g., Yoshinori, ¶ 20. Thus, the step projections would comprise approximately 50% of an area of the insulating substrate such as between the display region and the connection pads. Alternatively, the area can be specificied such that a projection step or multiple projection steps would cover at least 30% of the area. In other words, **Yoshinori discloses an insulating substrate having an area, with dummy patterns comprising 30% of the area, which was identified as the allowable subject matter of claims 1 and 9 of the '629 patent.** Additionally, the dummy patterns are located between the pixel electrode and the connection pads, are not in contact with the wiring, and comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

2. Yoshinori Discloses Each and Every Element of Claims 1-5, 7-13, and 15-16

Regarding each element of claim 1, Yoshinori discloses an array substrate for display comprising (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing an array substrate 1 including a display area 2): including an insulating substrate, having an area (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing an array substrate 1, including an area); a thin film transistor array formed on the insulating substrate (*See e.g.*, Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7 (disclosing an array including TFTs formed on the array substrate 1 in the display area 2)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Yoshinori, ¶ 20, Figs 1-3 (disclosing scan and signal wiring that connect to the scan and signal electrodes 6 and 9); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Yoshinori, ¶ 20, Figs 1-3 (disclosing connection pads 3 and 4 that connect to the scan and signal wiring)); pixel electrodes (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing pixels electrodes 10)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Yoshinori, ¶ 20 (disclosing that equal-interval projection steps 5 (dummy patterns) are located between the connection pads 3 and 4 and the pixel electrodes 10 and the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area, *see also* Yoshinori, Figs 1-3 (disclosing that the projection steps 5 or dummy patterns do not contact the scan and signal wirings)).

Regarding each element of claim 9, Yoshinori discloses a method for forming an array substrate for display, comprising (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing an array substrate 1 including a display area 2): forming a layer of an insulating substrate, having an area

(*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing an array substrate 1, including an area); forming a thin film transistor array formed on the insulating substrate (*See e.g.*, Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7 (disclosing an array including TFTs formed on the array substrate 1 in the display area 2 each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Yoshinori, ¶ 20, Figs 1-3 (disclosing scan and signal wiring that connect to the scan and signal electrodes 6 and 9); forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Yoshinori, ¶ 20, Figs 1-3 (disclosing connection pads 3 and 4 that connect to the scan and signal wiring)); forming pixel electrodes (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing pixels electrodes 10)); and forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Yoshinori, ¶ 20 (disclosing that equal-interval projection steps 5 (dummy patterns) are located between the connection pads 3 and 4 and the pixel electrodes 10 and the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area, *see also* Yoshinori, Figs 1-3 (disclosing that the projection steps 5 or dummy patterns do not contact the scan and signal wirings)). Accordingly, Yoshinori discloses each and every element of claims 1 and 9.

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof

(claims 4 and 5), and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Regarding dependent claims 2-5 and 10-13 of the '629 patent, Yoshinori discloses the signal electrode 9 comprises a bilayer of titanium/aluminum or the electrodes or wiring can be a monolayer or multilayer film of conductive metal. See, e.g., Yoshinori, ¶ 20. Therefore, Yoshinori meets the limitations of claims 2-5, 7-8, 10-13, and 15-16 of the '629 patent.

As demonstrated by the Examiner in the prosecution of the '629 patent, disclosure of materials such as those identified in the '629 APA, molybdenum, chromium, titanium, or tantalum, for the upper layer wiring meet the limitation of claims 7-8 and 15-16, that the upper layer wiring material does not become insoluble in an acid or alkaline etchant. For example, the examiner stated that because Song taught a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum the limitation of claims 7-8 and 15-16 were met. See '629 prosecution history, Office Action dated May 29, 2003 at page 3. Similarly, Yoshinori teaches an upper layer wiring of titanium, which would inherently is soluble in acid or alkaline etchants. Thus, Yoshinori teaches each and every element of claims 7-8 and 15-16 of the '629 patent.

Accordingly, Yoshinori discloses each and every element, and thus fully anticipates, claims 1-5, 7-13, and 15-16 of the '629 patent. A claim chart providing a detailed element by element analysis is attached as Appendix CC13.

N. Japanese Pub. No. H10-333151 to Yoshinori et al. in view of U.S. Patent No. 6,163,356 to Song Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Song was filed with the U.S. Patent Office on Jul. 24, 1997 and was issued on Dec. 19, 2000. Because Song issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Yoshinori in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. **However, Song was not considered in conjunction with Yoshinori, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Yoshinori provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Yoshinori, ¶ 20, Fig 1 (B) (interval projection steps 5)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Yoshinori and Song important to the patentability of the '629 patent and new and non-cumulative.** As such, Yoshinori in view of Song constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Yoshinori Discloses Each and Every Element of Claims 1 and 9

As discussed above, Yoshinori discloses each and every element of claims 1 and 9. Yoshinori discloses a liquid crystal display device including equal-interval projection steps, or dummy patterns, around the display area. See, e.g., Yoshinori, Abstract; Fig 1. As depicted here in Fig. 1 (B), the projection steps 5 are located between the display region 2 and the connection pads 3 and do not contact the wiring. Further, Yoshinori describes an example of the projection steps having a diameter 5 μm and being located at 5 μm intervals. See, e.g., Yoshinori, ¶ 20. Thus, the step projections would comprise approximately 50% of the area of the insulating substrate such as between the display region and the connection pads. Accordingly, the dummy patterns of Yoshinori would meet the limitations that the dummy patterns be located between

the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claims 1 and 9, Yoshinori discloses an array substrate for display comprising (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing an array substrate 1 including a display area 2): including an insulating substrate, having an area (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing an array substrate 1, including an area); a thin film transistor array formed on the insulating substrate (*See e.g.*, Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7 (disclosing an array including TFTs formed on the array substrate 1 in the display area 2)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Yoshinori, ¶ 20, Figs 1-3 (disclosing scan and signal wiring that connect to the scan and signal electrodes 6 and 9); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Yoshinori, ¶ 20, Figs 1-3 (disclosing connection pads 3 and 4 that connect to the scan and signal wiring)); pixel electrodes (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing pixels electrodes 10)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Yoshinori, ¶ 20 (disclosing that equal-interval projection steps 5 (dummy patterns) are located between the connection pads 3 and 4 and the pixel electrodes 10 and the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area, *see also* Yoshinori, Figs 1-3 (disclosing that the projection

steps 5 or dummy patterns do not contact the scan and signal wirings)). Accordingly, Yoshinori discloses each and every element of claims 1 and 9.[10]

2. Song Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. **As noted by the examiner during the prosecution of the '629 patent, this wiring structure of Song meets all of the limitations of claims 2-8 and 10-16.** See '629 File History, Office Action dated May 29, 2003 at page 3. Namely, Song discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum (claim 3 and 11) and the upper layer wiring material can be one of a variety of upper layer wiring materials such as molybdenum (claims 4-6 and 14). Song col 4, ll. 30-50; col. 8 ll. 5-18. The disclosed upper layer wiring

[10] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Yoshinori disclosures.

material, such as molybdenum, inherently does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

3. The Combined Teachings of Yoshinori and Song Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Yoshinori describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. See, e.g., Yoshinori, ¶ 20. Song teaches an improved wiring structure with low resistance and protective covering. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Song for the wiring in Yoshinori in a predictable way to obtain predictable results.

Accordingly, Yoshinori in view of Song discloses each and every element and renders obvious claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Yoshinori in view of Song of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC14.

O. Japanese Pub. No. H10-333151 to Yoshinori et al. in view the '629 Admitted Prior Art Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

A substantial new question of patentability is raised by Yoshinori in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. **However, the '629 APA was not considered in conjunction with Yoshinori, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Yoshinori provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Yoshinori, ¶ 20, Fig 1 (B) (interval projection steps 5)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally,

the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Yoshinori and the '629 APA important to the patentability of the '629 patent and new and non-cumulative.** As such, Yoshinori in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Yoshinori Discloses Each and Every Element of Claims 1 and 9

As discussed above, Yoshinori discloses each and every element of claims 1 and 9. Yoshinori discloses a liquid crystal display device including equal-interval projection steps, or dummy patterns, around the display area. See, e.g., Yoshinori, Abstract; Fig 1. As depicted here in Fig. 1 (B), the projection steps 5 are located between the display region 2 and the connection pads 3 and do not contact the wiring. Further, Yoshinori describes an example of the projection steps having a diameter 5 μm and being located at 5 μm intervals. See, e.g., Yoshinori, ¶ 20. Thus, the step projections would comprise approximately 50% of the area of the insulating substrate such as between the display region and the connection pads. Accordingly, the dummy patterns of Yoshinori would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claims 1 and 9, Yoshinori discloses an array substrate for display comprising (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing an array substrate 1 including a display area 2): including an insulating substrate, having an area (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing an array substrate 1, including an area); a thin film transistor array formed on the insulating substrate (*See e.g.*, Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7 (disclosing an array including TFTs formed on the array substrate 1 in the display area 2)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in

communication with at least one of the transistors in the thin film array (*See* e.g., Yoshinori, ¶ 20, Figs 1-3 (disclosing scan and signal wiring that connect to the scan and signal electrodes 6 and 9); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Yoshinori, ¶ 20, Figs 1-3 (disclosing connection pads 3 and 4 that connect to the scan and signal wiring)); pixel electrodes (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing pixels electrodes 10)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Yoshinori, ¶ 20 (disclosing that equal-interval projection steps 5 (dummy patterns) are located between the connection pads 3 and 4 and the pixel electrodes 10 and the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area, *see also* Yoshinori, Figs 1-3 (disclosing that the projection steps 5 or dummy patterns do not contact the scan and signal wirings)). Accordingly, Yoshinori discloses each and every element of claims 1 and 9.[11]

2. The '629 APA Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of

[11] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Yoshinori disclosures.

molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

The '629 APA discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is low resistance aluminum (claim 3 and 11) and the upper layer wiring material of a material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum (claims 4-6 and 14). See e.g., the '629 patent, col. 1, ll. 26-39. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Yoshinori and the '629 APA Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Yoshinori describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. See, e.g., Yoshinori, ¶ 20. The '629 APA teaches an improved wiring structure with low resistance and is harder is oxidize. See e.g., the '629 patent, col. 1, ll. 26-39. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of the '629 APA for the wiring in Yoshinori in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the upper material of Yoshinori for the molybdenum as taught in the '629 APA, since molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Yoshinori in view of the '629 APA discloses each and every element, and thus renders obvious, claims 2-8 and 9-16 of the '629 patent. A claim chart providing a detailed

element by element analysis of the obviousness by Yoshinori in view of the '629 APA of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC15.

P. Japanese Pub. No. H10-333151 to Yoshinori et al. in view of U.S. Patent No. 6,157,430 to Kubota Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Kubota was filed with the U.S. Patent Office on Sept. 29, 1997 and was issued on Dec. 5, 2000. Because Kubota issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Yoshinori in view of Kubota. Neither Yoshinori nor Kubota were before the Patent Office during the prosecution of the '629 patent. Yoshinori, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Yoshinori provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Yoshinori, ¶ 20, Fig 1 (B) (interval projection steps 5)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Yoshinori and Kubota important to the patentability of the '629 patent and new and non-cumulative.** As such, Yoshinori in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Yoshinori Discloses Each and Every Element of Claims 1 and 9

As discussed above, Yoshinori discloses each and every element of claims 1 and 9. Yoshinori discloses a liquid crystal display device including equal-interval projection steps, or dummy patterns, around the display area. See, e.g., Yoshinori, Abstract; Fig 1. As depicted here

in Fig. 1 (B), the projection steps 5 are located between the display region 2 and the connection pads 3 and do not contact the wiring. Further, Yoshinori describes an example of the projection steps having a diameter 5 μm and being located at 5 μm intervals. See, e.g., Yoshinori, ¶ 20. Thus, the step projections would comprise approximately 50% of the area of the insulating substrate such as between the display region and the connection pads. Accordingly, the dummy patterns of Yoshinori would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claims 1 and 9, Yoshinori discloses an array substrate for display comprising (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing an array substrate 1 including a display area 2): including an insulating substrate, having an area (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing an array substrate 1, including an area); a thin film transistor array formed on the insulating substrate (*See e.g.*, Yoshinori, Abstract, ¶ 20, Figs 1-3, 6-7 (disclosing an array including TFTs formed on the array substrate 1 in the display area 2)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Yoshinori, ¶ 20, Figs 1-3 (disclosing scan and signal wiring that connect to the scan and signal electrodes 6 and 9); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Yoshinori, ¶ 20, Figs 1-3 (disclosing connection pads 3 and 4 that connect to the scan and signal wiring)); pixel electrodes (*See e.g.*, Yoshinori, Abstract, Figs 1-3 (disclosing pixels electrodes 10)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in

contact with any of the wiring. *See e.g.*, Yoshinori, ¶ 20 (disclosing that equal-interval projection steps 5 (dummy patterns) are located between the connection pads 3 and 4 and the pixel electrodes 10 and the projection steps of 5 μm in diameter are located at 5 μm intervals, thus covering at least 30% of the area, *see also* Yoshinori, Figs 1-3 (disclosing that the projection steps 5 or dummy patterns do not contact the scan and signal wirings)). Accordingly, Yoshinori discloses each and every element of claims 1 and 9.[12]

2. Kubota Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Kubota discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum or aluminum alloy (claim 3 and 11) and the upper layer wiring material from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof (claims 4-6 and 14). See e.g., Kubota, col. 4, ll. 39-55. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant

[12] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Yoshinori disclosures.

(claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Yoshinori and Kubota Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Yoshinori describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. See, e.g., Yoshinori, ¶ 20. Kubota teaches an improved wiring structure with the upper layer having a high hardness. See e.g., Kubota, col. 4, ll. 39-45. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Kubota for the wiring in Yoshinori in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the upper material of Yoshinori for the molybdenum as taught in Kubota, since molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Yoshinori in view of Kubota discloses each and every element, and thus renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Yoshinori in view of Kubota of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC16.

Q. Japanese Pub. No. 2000-098909 to Tomoyuki Raises A Substantial New Question of Patentability and Anticipates Claims 1 and 9 of the '629 Patent

Tomoyuki was filed with the Japanese Patent Office on Sept. 22, 1998 and was published on April 7, 2000. Because Tomoyuki was published more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability as to claims 1 and 9 is raised by Tomoyuki. Tomoyuki was not considered by the Patent Office during the prosecution of

the '629 patent. As discussed above, the Patent Office, without knowledge of Tomoyuki, allowed the'629 patent on the rationale that the art did not teach or suggest:

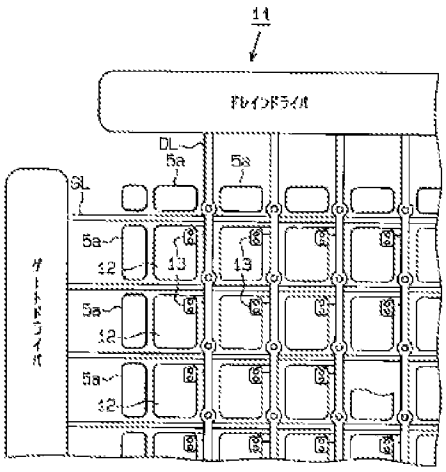
> a layer of an insulating substrate, *having an area*;…dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Tomoyuki teaches this feature. See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (dummy patterns 5a). **Tomoyuki teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider these teachings of Tomoyuki is important to the patentability of the '629 patent and new and non-cumulative.** As such, Requestor believes that these teachings of Tomoyuki raise a substantial new question of patentability with respect to independent claims 1 and 9.

1. Tomoyuki Is New, Non-Cumulative Art Because It Discloses the Identified Allowable Feature of the '629 Patent, Dummy Patterns Comprising at Least about 30% of the Area

Tomoyuki discloses a liquid crystal display device including dummy film that is patterned to enclose the outer periphery of the pixel electrodes. See, e.g., Tomoyuki, Abstract, Fig 1 and 5-6. Tomoyuki describes the dummy film being a continuous shape as shown in Fig. 1 or the shape of pixel electrodes as shown in Figs. 5 and 6. See, e.g., Tomoyuki, Abstract, ¶ 32, Figs. 1 and 5-6. For example, Fig. 5, shown here, depicts dummy patterns 5a in the area of the substrate between the pixel electrodes and the connection pads and not in contact with the wiring GL and DL.

【図5】



Selecting an area or specified region where the dummy patterns or a portion of the dummy patterns would satisfy the 30% requirement. In other words, **Tomoyuki discloses an insulating substrate having an area, with dummy patterns comprising 30% of the area, which was identified as the allowable subject matter of claims 1 and 9 of the '629 patent.** Additionally, the dummy patterns of Tomoyuki would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads and that they not be in contact with the wiring, as required by claims 1 and 9 of the '629 patent.

2. Tomoyuki Discloses Each and Every Element of Claims 1 and 9

Regarding each element of claim 1, Tomoyuki discloses an array substrate for display (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels): including an insulating substrate, having an area (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Tomoyuki, Abstract, Figs 1, 5-6 (disclosing TFT array

substrate including wiring, drain lines DLs and gate lines GLs)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs)); pixel electrodes (*See e.g.*, Tomoyuki, Figs 1, 5-6 (disclosing pixel electrodes 12)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Tomoyuki, Abstract, Figures 1, 5-6 (disclosing dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs), see also Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (stating that the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel electrode, thus the dummy film 5 and 5a would comprise at least 30% of the area or a specified region).

Regarding each element of claim 9, Tomoyuki discloses a method for forming an array substrate for display, comprising (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels): forming a layer of an insulating substrate, having an area (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels)); forming a thin film transistor array formed on the insulating substrate (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels)); each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array (*See* e.g., Tomoyuki, Abstract, Figs 1, 5-6 (disclosing TFT array substrate including wiring, drain lines DLs and gate lines GLs)); forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*,

Tomoyuki, Abstract, Figs 1, 5-6 (disclosing that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs)); forming pixel electrodes (*See e.g.*, Tomoyuki, Figs 1, 5-6 (disclosing pixel electrodes 12)); and forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. (*See e.g.*, Tomoyuki, Abstract, Figures 1, 5-6 (disclosing dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs), see also Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (stating that the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel electrode, thus the dummy film 5 and 5a would comprise at least 30% of the area or a specified region). Accordingly, Tomoyuki discloses each and every element of claims 1 and 9.

Accordingly, Tomoyuki discloses each and every element and fully anticipates claims 1 and 9 of the '629 patent. A claim chart providing a detailed element by element analysis is attached as Appendix CC17.

R. Japanese Pub. No. 2000-098909 to Tomoyuki in view of U.S. Patent No. 6,163,356 to Song Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Song was filed with the U.S. Patent Office on Jul. 24, 1997 and was issued on Dec. 19, 2000. Because Song issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Tomoyuki in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. **However, Song was not considered in conjunction with Tomoyuki, which as discussed above raises a substantial**

new question of patentability and teaches each and every element of claims 1 and 9. Namely, Tomoyuki provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (dummy patterns 5a)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Tomoyuki and Song important to the patentability of the '629 patent and new and non-cumulative.** As such, Tomoyuki in view of Song constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Tomoyuki Discloses Each and Every Element of Claims 1 and 9

As discussed above, Tomoyuki discloses each and every element of claims 1 and 9. Tomoyuki discloses a liquid crystal display device including dummy film that is patterned to enclose the outer periphery of the pixel electrodes. See, e.g., Tomoyuki, Abstract, Fig 1 and 5-6. Tomoyuki describes the dummy film being a continuous shape as shown in Fig. 1 or the shape of pixel electrodes as shown in Figs. 5 and 6. See, e.g., Tomoyuki, Abstract, ¶ 32. For example, Fig. 5, shown here, depicts dummy patterns 5a in the area of the substrate between the pixel electrodes and the connection pads and not in contact with the wiring GL and DL. Selecting an area or specified region where the dummy patterns or a portion of the dummy patterns would satisfy the 30% requirement. Accordingly, the dummy patterns of Tomoyuki would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claims 1 and 9, Tomoyuki discloses an array substrate for display (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels): including an insulating substrate, having an area (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Tomoyuki, Abstract, Figs 1, 5-6 (disclosing TFT array substrate including wiring, drain lines DLs and gate lines GLs)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs)); pixel electrodes (*See e.g.*, Tomoyuki, Figs 1, 5-6 (disclosing pixel electrodes 12)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Tomoyuki, Abstract, Figures 1, 5-6 (disclosing dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs), see also Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (stating that the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel electrode, thus the dummy film 5 and 5a would comprise at least 30% of the area or a specified region). Accordingly, Tomoyuki discloses each and every element of claims 1 and 9.[13]

[13] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed
(footnote continued on next page)

2. Song Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. **As noted by the examiner during the prosecution of the '629 patent, this wiring structure of Song meets all of the limitations of claims 2-8 and 10-16.** See '629 File History, Office Action dated May 29, 2003 at page 3. Namely, Song discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum (claim 3 and 11) and the upper layer wiring material can be one of a variety of upper layer wiring materials such as molybdenum (claims 4-6 and 14). Song col 4, ll. 30-50; col. 8 ll. 5-18. The disclosed upper layer wiring material, such as molybdenum, inherently does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

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above, are met by the same Tomoyuki disclosures.

3. The Combined Teachings of Tomoyuki and Song Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Tomoyuki describes and depicts wiring structures, but does not provide materials or a structure, suggesting any of a variety of wiring structures may be implemented as appropriate. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6. Song teaches an improved wiring structure with low resistance and protective covering. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Song for the wiring in Tomoyuki in a predictable way to obtain predictable results.

Accordingly, Tomoyuki in view of Song discloses each and every element, and thus renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Tomoyuki in view of Song of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC18.

S. Japanese Pub. No. 2000-098909 to Tomoyuki in view of the '629 Admitted Prior Art Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

A substantial new question of patentability is raised by Tomoyuki in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. **However, the '629 APA was not considered in conjunction with Tomoyuki, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Tomoyuki provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (dummy patterns 5a)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16.

Thus, a reasonable examiner would consider the combined teachings of Tomoyuki and the '629 APA important to the patentability of the '629 patent and new and non-cumulative art. As such, Tomoyuki in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Tomoyuki Discloses Each and Every Element of Claims 1 and 9

As discussed above, Tomoyuki discloses each and every element of claims 1 and 9. Tomoyuki discloses a liquid crystal display device including dummy film that is patterned to enclose the outer periphery of the pixel electrodes. See, e.g., Tomoyuki, Abstract, Fig 1 and 5-6. Tomoyuki describes the dummy film being a continuous shape as shown in Fig. 1 or the shape of pixel electrodes as shown in Figs. 5 and 6. See, e.g., Tomoyuki, Abstract, ¶ 32. For example, Fig. 5, shown here, depicts dummy patterns 5a in the area of the substrate between the pixel electrodes and the connection pads and not in contact with the wiring GL and DL. Selecting an area or specified region where the dummy patterns or a portion of the dummy patterns would satisfy the 30% requirement. Accordingly, the dummy patterns of Tomoyuki would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claims 1 and 9, Tomoyuki discloses an array substrate for display (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels): including an insulating substrate, having an area (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels)); a plurality of wiring arranged on the insulating

substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Tomoyuki, Abstract, Figs 1, 5-6 (disclosing TFT array substrate including wiring, drain lines DLs and gate lines GLs)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing that the gate driver and drain driver connect to the gate lines GLs and drain lines DLs)); pixel electrodes (*See e.g.*, Tomoyuki, Figs 1, 5-6 (disclosing pixel electrodes 12)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Tomoyuki, Abstract, Figures 1, 5-6 (disclosing dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs), see also Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (stating that the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel electrode, thus the dummy film 5 and 5a would comprise at least 30% of the area or a specified region). Accordingly, Tomoyuki discloses each and every element of claims 1 and 9.[14]

2. The '629 APA Discloses Each and Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected

[14] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Tomoyuki disclosures.

from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

The '629 APA discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is low resistance aluminum (claim 3 and 11) and the upper layer wiring material of a material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum (claims 4-6 and 14). See e.g., the '629 patent, col. 1, ll. 26-39. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Tomoyuki and the '629 APA Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Tomoyuki describes and depicts wiring structures, but does not provide materials or a structure, suggesting any of a variety of wiring structures may be implemented as appropriate. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6. The '629 APA teaches an improved wiring structure with low resistance and is harder is oxidize. See e.g., the '629 patent, col. 1, ll. 26-39. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of the '629 APA for the wiring in Tomoyuki in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the wiring of Tomoyuki for the aluminum/molybdenum wiring as taught in

the '629 APA, since aluminum has a low resistance and molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Tomoyuki in view of the '629 APA discloses each and every element and, thus renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Tomoyuki in view of the '629 APA of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC19.

T. Japanese Pub. No. 2000-098909 to Tomoyuki in view of U.S. Patent No. 6,157,430 to Kubota Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Kubota was filed with the U.S. Patent Office on Sept. 29, 1997 and was issued on Dec. 5, 2000. Because Kubota issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Tomoyuki in view of Kubota. Neither Tomoyuki nor Kubota were before the Patent Office during the prosecution of the '629 patent. Tomoyuki, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Yoshinori provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (dummy patterns 5a)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Tomoyuki and Kubota important to the patentability of the '629 patent and new and non-cumulative.** As such, Tomoyuki in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Tomoyuki Discloses Each and Every Element of Claims 1 and 9

As discussed above, Tomoyuki discloses each and every element of claims 1 and 9. Tomoyuki discloses a liquid crystal display device including dummy film that is patterned to enclose the outer periphery of the pixel electrodes. See, e.g., Tomoyuki, Abstract, Fig 1 and 5-6. Tomoyuki describes the dummy film being a continuous shape as shown in Fig. 1 or the shape of pixel electrodes as shown in Figs. 5 and 6. See, e.g., Tomoyuki, Abstract, ¶ 32. For example, Fig. 5, shown here, depicts dummy patterns 5a in the area of the substrate between the pixel electrodes and the connection pads and not in contact with the wiring GL and DL. Selecting an area or specified region where the dummy patterns or a portion of the dummy patterns would satisfy the 30% requirement. Accordingly, the dummy patterns of Tomoyuki would meet the limitations that the dummy patterns be located between the pixel electrode and the connection pads, that they not be in contact with the wiring, and that they comprise 30% of the area as required by claims 1 and 9 of the '629 patent.

Regarding each element of claims 1 and 9, Tomoyuki discloses an array substrate for display (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels): including an insulating substrate, having an area (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing a TFT array substrate 11 including display pixels)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., Tomoyuki, Abstract, Figs 1, 5-6 (disclosing TFT array substrate including wiring, drain lines DLs and gate lines GLs)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Tomoyuki, Abstract, Figs 1, 5-6 (disclosing that the gate driver and drain driver connect to the

gate lines GLs and drain lines DLs)); pixel electrodes (*See e.g.*, Tomoyuki, Figs 1, 5-6 (disclosing pixel electrodes 12)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Tomoyuki, Abstract, Figures 1, 5-6 (disclosing dummy film 5 and 5a is located between the gate and drain drivers and the pixel electrodes 12 and not in contact with the gate lines GLs and drain lines DLs), see also Tomoyuki, Abstract, ¶ 32, Figures 1, 5-6 (stating that the dummy 5 and 5a can be continuous or can be a shape corresponding to a pixel electrode, thus the dummy film 5 and 5a would comprise at least 30% of the area or a specified region). Accordingly, Tomoyuki discloses each and every element of claims 1 and 9.[15]

2. Kubota Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

[15] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Tomoyuki disclosures.

Kubota discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum or aluminum alloy (claim 3 and 11) and the upper layer wiring material from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof (claims 4-6 and 14). See e.g., Kubota, col. 4, ll. 39-55. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Tomoyuki and Kubota Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Tomoyuki describes and depicts wiring structures, but does not provide materials or a structure, suggesting any of a variety of wiring structures may be implemented as appropriate. See, e.g., Tomoyuki, Abstract, Figs 1, 5-6. Kubota teaches an improved wiring structure with the upper layer having a high hardness. See e.g., Kubota, col. 4, ll. 39-45. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Kubota for the wiring in Tomoyuki in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the wiring of Tomoyuki for the aluminum/molybdenum wiring as taught in Kubota, since aluminum has a low resistance and molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Tomoyuki in view of Kubota discloses each and every element, and thus renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Tomoyuki in view of Kubota of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC20.

U. U.S. Patent No. 5,995,189 to Zhang Raises A Substantial New Question of Patentability and Anticipates Claims 1-5, 7-13, and 15-16 of the '629 Patent

Zhang was filed with the U.S. Patent Office on Dec. 16, 1996 and issued on Nov. 30, 1999. Because Zhang issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability as to claims 1-5, 7-13, and 15-16 is raised by Zhang. Zhang was not considered by the Patent Office during the prosecution of the '629 patent. As discussed above, the Patent Office, without knowledge of Zhang, allowed the'629 patent on the rationale that the art did not teach or suggest:

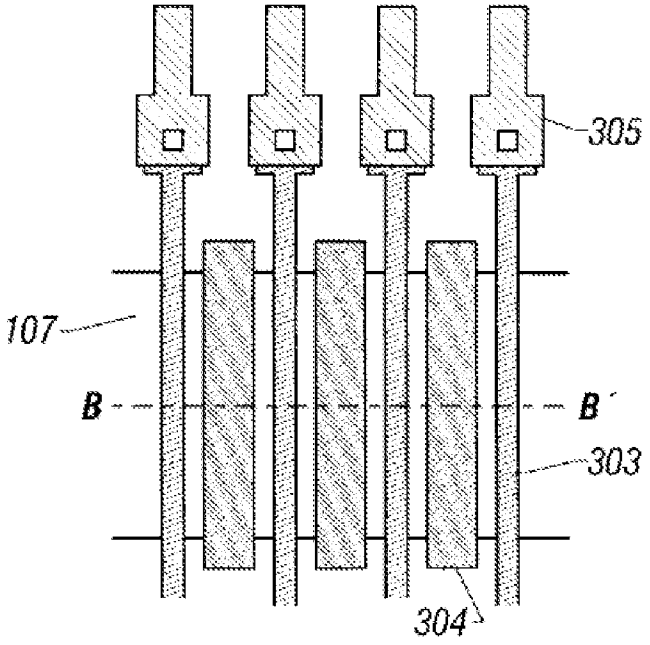
> a layer of an insulating substrate, *having an area*;…dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Zhang teaches this feature. See, e.g., Zhang, col. 10, lines 7-17; Figs 4 and 8 (dummy patterns 304). **Zhang teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider these teachings of Zhang important to the patentability of the '629 patent and new and non-cumulative.** As such, Requestor believes that these teachings of Zhang raise a substantial new question of patentability with respect to independent claims 1 and 9, and consequently claims 2-5 and 7-8 dependent on claim 1 and claims 10-13 and 15-16 dependent on claim 9.

1. Zhang Is New, Non-Cumulative Art Because It Discloses the Identified Allowable Feature of the '629 Patent, Dummy Patterns Comprising at Least about 30% of the Area

Zhang discloses a liquid crystal display device including dummy wirings to be in the gaps between the scan and signal wirings. See, e.g., Zhang, Figs 4 and 8. As shown, for example, in

Fig. 8 below, the dummy patterns 304 are located between the wiring 303 extending out from the display region.



See, e.g., Zhang, Figs 4 and 8. Additionally, Zhang describes, in one example, that the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm, on each side, between the wiring and dummy wiring. See, e.g., Zhang, col. 10, lines 7-17. In other words, **Zhang discloses an insulating substrate having an area, with dummy patterns comprising 30% of the area, which was identified as the allowable subject matter of claims 1 and 9 of the '629 patent.**

2. Zhang Discloses Each and Every Element of Claims 1-5, 7-13, and 15-16

Regarding each element of claims 1 and 9, Zhang discloses an array substrate for display comprising (*See e.g.*, Zhang, Title, Figs. 1 and 16-17 (disclosing a liquid crystal display device): including an insulating substrate, having an area (*See e.g.*, Zhang, 1:35-36, Figs. 1 and 16-17 (disclosing a substrate 1 made of glass or quartz, including an area); a thin film transistor array

formed on the insulating substrate (*See e.g.*, Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17 (disclosing scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17 (disclosing scan lines 2 and signal lines 3 and are connected to the TFTs); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17 (disclosing that the signal lines 2 and scan lines 3 also connect to extension terminals 6)); pixel electrodes (*See e.g.*, Zhang, Figs. 1 and 16-17 (disclosing a pixel section 12)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, See, e.g., Zhang, Figs. 4, 8 and 16 (disclosing dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals and that the dummy wirings are not in contact with the wiring), *see also* Zhang, 10:7-17 (stating that that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring, thus, the dummy patterns would comprise at least 30% of the area)). Accordingly, Zhang discloses each and every element of claim 1.

Regarding each element of claim 9, Zhang discloses a method for forming an array substrate for display, comprising (*See e.g.*, Zhang, Title, Figs. 1 and 16-17 (disclosing a liquid crystal display device): forming a layer of an insulating substrate, having an area (*See e.g.*,

Zhang, 1:35-36, Figs. 1 and 16-17 (disclosing a substrate 1 made of glass or quartz, including an area); forming a thin film transistor array formed on the insulating substrate (*See e.g.*, Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17 (disclosing scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines)); each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17 (disclosing scan lines 2 and signal lines 3 and are connected to the TFTs); forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17 (disclosing that the signal lines 2 and scan lines 3 also connect to extension terminals 6)); forming pixel electrodes (*See e.g.*, Zhang, Figs. 1 and 16-17 (disclosing a pixel section 12)); and forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. (*See e.g.*, Zhang, Figs. 4, 8 and 16 (disclosing dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals and that the dummy wirings are not in contact with the wiring), *see also* Zhang, 10:7-17 (stating that that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring, thus, the dummy patterns would comprise at least 30% of the area)). Accordingly, Zhang discloses each and every element of claims 1 and 9.

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive

material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Zhang also discloses the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33. Similar to the previous references discussed above, this meets the limitations of claims 2-5, 7-8, 10-13 and 15-16, with a lower layer of aluminum and an upper layer of titanium. *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

Accordingly, Zhang discloses each and every element, and fully anticipates, claims 1-5, 7-13, and 15-16 of the '629 patent. A claim chart providing a more detailed element by element analysis is attached as Appendix CC21.

V. U.S. Patent No. 5,995,189 to Zhang in view of U.S. Patent No. 6,163,356 to Song Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Song was filed with the U.S. Patent Office on Jul. 24, 1997 and was issued on Dec. 19, 2000. Because Song issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Zhang in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. **However, Song was not**

considered in conjunction with Zhang, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Zhang provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Zhang, col. 10, lines 7-17; Figs 4 and 8 (dummy patterns 304)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Zhang and Song important to the patentability of the '629 patent and new and non-cumulative.** As such, Zhang in view of Song constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Zhang Discloses Each And Every Element of Claims 1 and 9

As discussed above, Zhang discloses each and every element of claims 1 and 9. Zhang discloses a liquid crystal display device including dummy wirings to be in the gaps between the scan and signal wirings. See, e.g., Zhang, Figs 4 and 8. As shown, for example, in Fig. 8 the dummy patterns are located between the wiring extending out from the display region. See, e.g., Zhang, Figs 4 and 8. Zhang describes, in one example, that the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, col. 10, lines 7-17. Thus, as the dummy patterns of Zhang would cover greater than 30% of the area. Zhang also discloses the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33. Similar to the previous references discussed above, this meets the limitations of claims 2-5, 7-8, 10-13 and 15-16.

Regarding each element of claims 1 and 9, Zhang discloses an array substrate for display comprising (*See e.g.*, Zhang, Title, Figs. 1 and 16-17 (disclosing a liquid crystal display device):

including an insulating substrate, having an area (*See e.g.*, Zhang, 1:35-36, Figs. 1 and 16-17 (disclosing a substrate 1 made of glass or quartz, including an area); a thin film transistor array formed on the insulating substrate (*See e.g.*, Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17 (disclosing scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17 (disclosing scan lines 2 and signal lines 3 and are connected to the TFTs); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17 (disclosing that the signal lines 2 and scan lines 3 also connect to extension terminals 6)); pixel electrodes (*See e.g.*, Zhang, Figs. 1 and 16-17 (disclosing a pixel section 12)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, See, e.g., Zhang, Figs. 4, 8 and 16 (disclosing dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals and that the dummy wirings are not in contact with the wiring), *see also* Zhang, 10:7-17 (stating that that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring, thus, the dummy patterns would comprise at least 30% of the area)). Accordingly, Zhang discloses each and every element of claims 1 and 9.[16]

[16] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed
(footnote continued on next page)

2. Song Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. **As noted by the examiner during the prosecution of the '629 patent, this wiring structure of Song meets all of the limitations of claims 2-8 and 10-16.** See '629 File History, Office Action dated May 29, 2003 at page 3. Namely, Song discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum (claim 3 and 11) and the upper layer wiring material can be one of a variety of upper layer wiring materials such as molybdenum (claims 4-6 and 14). Song col 4, ll. 30-50; col. 8 ll. 5-18. The disclosed upper layer wiring material, such as molybdenum, inherently does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

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above, are met by the same Zhang disclosures.

3. The Combined Teachings of Zhang and Song Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Zhang describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. See, e.g., See, e.g., Zhang, 9:29-33. Song teaches an improved wiring structure with low resistance and protective covering. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Song for the wiring in Zhang in a predictable way to obtain predictable results.

Accordingly, Zhang in view of Song discloses each and every element, and thus renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Zhang in view of Song of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC22.

W. U.S. Patent No. 5,995,189 to Zhang in view of the '629 Admitted Prior Art Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

A substantial new question of patentability is raised by Zhang in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. **However, the '629 APA was not considered in conjunction with Zhang, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Zhang provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Zhang, col. 10, lines 7-17; Figs 4 and 8 (dummy patterns 304)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Zhang and the '629 APA important to**

the patentability of the '629 patent and new and non-cumulative. As such, Zhang in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Zhang Discloses Each And Every Element of Claims 1 and 9

As discussed above, Zhang discloses each and every element of claims 1 and 9. Zhang discloses a liquid crystal display device including dummy wirings to be in the gaps between the scan and signal wirings. See, e.g., Zhang, Figs 4 and 8. As shown, for example, in Fig. 8 the dummy patterns are located between the wiring extending out from the display region. See, e.g., Zhang, Figs 4 and 8. Zhang describes, in one example, that the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, col. 10, lines 7-17. Thus, as the dummy patterns of Zhang would cover greater than 30% of the area. Zhang also discloses the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33. Similar to the previous references discussed above, this meets the limitations of claims 2-5, 7-8, 10-13 and 15-16.

Regarding each element of claims 1 and 9, Zhang discloses an array substrate for display comprising (*See e.g.*, Zhang, Title, Figs. 1 and 16-17 (disclosing a liquid crystal display device): including an insulating substrate, having an area (*See e.g.*, Zhang, 1:35-36, Figs. 1 and 16-17 (disclosing a substrate 1 made of glass or quartz, including an area); a thin film transistor array formed on the insulating substrate (*See e.g.*, Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17 (disclosing scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17 (disclosing scan lines 2 and signal lines 3 and are

connected to the TFTs); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17 (disclosing that the signal lines 2 and scan lines 3 also connect to extension terminals 6)); pixel electrodes (*See e.g.*, Zhang, Figs. 1 and 16-17 (disclosing a pixel section 12)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, See, e.g., Zhang, Figs. 4, 8 and 16 (disclosing dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals and that the dummy wirings are not in contact with the wiring), *see also* Zhang, 10:7-17 (stating that that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring, thus, the dummy patterns would comprise at least 30% of the area)). Accordingly, Zhang discloses each and every element of claims 1 and 9.[17]

2. The '629 APA Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of

[17] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Zhang disclosures.

molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

The '629 APA discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is low resistance aluminum (claim 3 and 11) and the upper layer wiring material of a material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum (claims 4-6 and 14). See e.g., the '629 patent, col. 1, ll. 26-39. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Zhang and The '629 APA Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Zhang describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. See, e.g., See, e.g., Zhang, 9:29-33. The '629 APA teaches an improved wiring structure with low resistance and is harder is oxidize. See e.g., the '629 patent, col. 1, ll. 26-39. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of the '629 APA for the wiring in Zhang in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the upper material of Zhang for the molybdenum as taught in the '629 APA, since molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Zhang in view of the '629 APA discloses each and every element, and thus renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed

element by element analysis of the obviousness by Zhang in view of the '629 APA of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC23.

X. U.S. Patent No. 5,995,189 to Zhang in view of U.S. Patent No. 6,157,430 to Kubota Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Kubota was filed with the U.S. Patent Office on Sept. 29, 1997 and was issued on Dec. 5, 2000. Because Kubota issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Zhang in view of Kubota. Neither Zhang nor Kubota were before the Patent Office during the prosecution of the '629 patent. Zhang, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Zhang provides dummy patterns comprising at least about 30% of an area of the insulating substrate (See, e.g., Zhang, col. 10, lines 7-17; Figs 4 and 8 (dummy patterns 304)), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Zhang and Kubota important to the patentability of the '629 patent and new and non-cumulative.** As such, Zhang in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Zhang Discloses Each And Every Element of Claims 1 and 9

As discussed above, Zhang discloses each and every element of claims 1 and 9. Zhang discloses a liquid crystal display device including dummy wirings to be in the gaps between the scan and signal wirings. See, e.g., Zhang, Figs 4 and 8. As shown, for example, in Fig. 8 the dummy patterns are located between the wiring extending out from the display region. See, e.g.,

Zhang, Figs 4 and 8. Zhang describes, in one example, that the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring. See, e.g., Zhang, col. 10, lines 7-17. Thus, as the dummy patterns of Zhang would cover greater than 30% of the area. Zhang also discloses the wiring can comprise of a three layer film of titanium, aluminum, and titanium. See, e.g., Zhang, 9:29-33. Similar to the previous references discussed above, this meets the limitations of claims 2-5, 7-8, 10-13 and 15-16.

Regarding each element of claims 1 and 9, Zhang discloses an array substrate for display comprising (*See e.g.*, Zhang, Title, Figs. 1 and 16-17 (disclosing a liquid crystal display device): including an insulating substrate, having an area (*See e.g.*, Zhang, 1:35-36, Figs. 1 and 16-17 (disclosing a substrate 1 made of glass or quartz, including an area); a thin film transistor array formed on the insulating substrate (*See e.g.*, Zhang, 1:34-40, 6:40-44, Figs. 1 and 16-17 (disclosing scan lines 2 and signal lines 3 are formed on the element substrate 1 and 101 in a matrix with TFTs and pixel electrodes at the crossover points of the scan and signal lines)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See* e.g., See, e.g., Zhang, 1:34-40, 3:32-40, Figs. 1 and 16-17 (disclosing scan lines 2 and signal lines 3 and are connected to the TFTs); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Zhang, 1:45-47, 6:51-60, Figs. 1 and 16-17 (disclosing that the signal lines 2 and scan lines 3 also connect to extension terminals 6)); pixel electrodes (*See e.g.*, Zhang, Figs. 1 and 16-17 (disclosing a pixel section 12)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See*

e.g., See, e.g., Zhang, Figs. 4, 8 and 16 (disclosing dummy wirings 304 located in the sealing material formation region patterns which can be located between the pixel section and the extension terminals and that the dummy wirings are not in contact with the wiring), *see also* Zhang, 10:7-17 (stating that that, for example, the distance between wiring is 50 μm and that the dummy wirings are 30 μm leaving only 10 μm between the wiring and dummy wiring, thus, the dummy patterns would comprise at least 30% of the area)). Accordingly, Zhang discloses each and every element of claims 1 and 9.[18]

2. Kubota Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Kubota discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum or aluminum alloy (claim 3 and 11) and the upper layer wiring material from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof (claims 4-6 and 14). See e.g., Kubota, col. 4, ll. 39-55. The disclosed upper layer wiring

[18] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Zhang disclosures.

materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Zhang and Kubota Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Zhang describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. See, e.g., See, e.g., Zhang, 9:29-33. Kubota teaches an improved wiring structure with the upper layer having a high hardness. See e.g., Kubota, col. 4, ll. 39-45. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Kubota for the wiring in Zhang in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the upper material of Zhang for the molybdenum as taught in Kubota, since molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Zhang in view of Kubota discloses each and every element and thus renders obvious claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Zhang in view of Kubota of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC24.

Y. Japanese Publication No. H06-082811 to Watanabe '811 Raises A Substantial New Question of Patentability and Anticipates Claims 1-5, 7-13, and 15-16 of the '629 Patent

Watanabe '811 was published March 25, 1994. Because Watanabe '811 was published more than one year before the filing date of the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

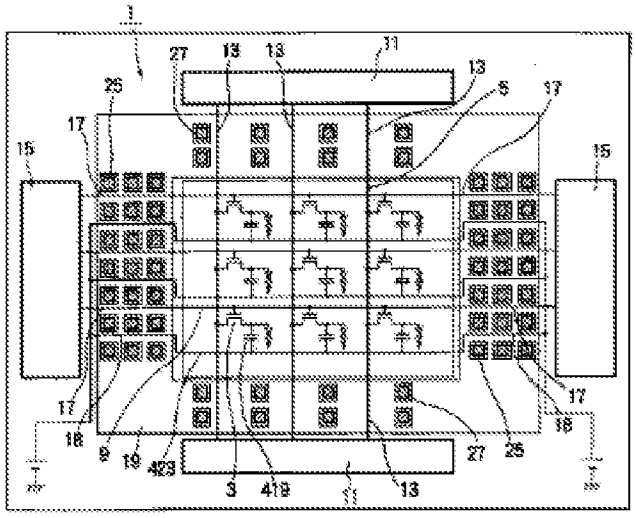
A substantial new question of patentability as to claims 1-5, 7-13, and 15-16 is raised by Watanabe '811. Watanabe '811 was not considered by the Patent Office during the prosecution of the '629 patent. As discussed above, the Patent Office, without knowledge of Watanabe '811, allowed the'629 patent on the rationale that the art did not teach or suggest:

> a layer of an insulating substrate, *having an area*;…dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Watanabe '811 teaches this feature. *See e.g.*, Watanabe '811, Fig. 5, and [0071]. **Watanabe '811 teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider the teachings of Watanabe '811 important to the patentability of the '629 patent and new and non-cumulative.** As such, Requestor believes that these teachings of Watanabe '811 raise a substantial new question of patentability with respect to independent claims 1 and 9, and consequently claims 2-5 and 7-8, dependent on claim 1, and claims 10-13 and 15-16, dependent on claim 9.

1. Watanabe '811 Is New, Non-Cumulative Art Because It Discloses the Identified Allowable Feature of the '629 Patent, Dummy Patterns Comprising at Least About 30% of the Area

Watanabe '811 addresses the issue of cell gap uniformity to achieve a better quality display. To resolve this issue, Watanabe '811 provides additional conductive dummy patterns in the region between the pixel array and the contact pads. As shown below in Fig. 5, the dummy patterns 25 and 27 cover different areas between the pixel array and the connection terminals 15 and 11. *See e.g.*, Watanabe '811, Fig. 5, and [0071].



For example, if the selected area is limited to where a single dummy pattern or just a portion of the dummy pattern is located, it will cover 100% of the specified region. In other words, **Watanabe '811 discloses an insulating substrate having an area, with dummy patterns comprising 30% of the area, which was identified as the allowable subject matter of claims 1 and 9 of the '629 patent.**

2. Watanabe '811 Discloses Each and Every Element of Claims 1-5, 7-13, and 15-16

Regarding each element of claims 1, Watanabe '811 discloses an array substrate for display (*See e.g.*, Watanabe '811, Fig. 5, and [0034] (disclosing an array substrate for a liquid crystal display and method of forming an array substrate): including an insulating substrate, having an area (*See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038] (disclosing a glass, and thus insulating, substrate upon which a TFT array of a liquid crystal display is formed)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Watanabe '811, Fig. 5, and [0034] (disclosing an array substrate for a liquid crystal display and method of forming an array substrate); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See*

e.g., Watanabe '811, [0035] (disclosing thin film transistors connected by signal and scanning lines 5 and 9)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Watanabe '811, [0035] (disclosing that the active matrix display includes scanning and signal lines that provide video-signal to thin film transistors), *see also* Watanabe '811, Fig. 5 (depicting that the scanning and signal lines connect to respective driving circuits, thus connection pads would be inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits)); pixel electrodes (*See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035] (identifying pixel electrodes as items 7 in figure 4)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071] (disclosing that the metal dummy patterns, items 25 and 27, in figure 5 are situated between the connection pads and pixel electrode array and are not in contact with any of the wiring), see also Watanabe '811, Figs. 5 (depicting it is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed, shown in figure 5, where at least 30% of the area shown is covered by the dummy pattern to meet this limitation)). Accordingly, Watanabe '811 discloses each and every element of claims 1.

Regarding each element of claim 9, Watanabe '811 discloses a method for forming an array substrate for display, comprising (*See e.g.*, Watanabe '811, Fig. 5, and [0034] (disclosing an array substrate for a liquid crystal display and method of forming an array substrate): forming a layer of an insulating substrate, having an area (*See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038] (disclosing a glass, and thus insulating, substrate upon which a TFT array of a

liquid crystal display is formed)); forming a thin film transistor array formed on the insulating substrate (*See e.g.*, Watanabe '811, Fig. 5, and [0034] (disclosing an array substrate for a liquid crystal display and method of forming an array substrate); each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See e.g.*, Watanabe '811, [0035] (disclosing thin film transistors connected by signal and scanning lines 5 and 9)); forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Watanabe '811, [0035] (disclosing that the active matrix display includes scanning and signal lines that provide video-signal to thin film transistors), *see also* Watanabe '811, Fig. 5 (depicting that the scanning and signal lines connect to respective driving circuits, thus connection pads would be inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits)); forming pixel electrodes (*See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035] (identifying pixel electrodes as items 7 in figure 4)); and forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071] (disclosing that the metal dummy patterns, items 25 and 27, in figure 5 are situated between the connection pads and pixel electrode array and are not in contact with any of the wiring), *see also* Watanabe '811, Figs. 5 (depicting it is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed, shown in figure 5, where at least 30% of the area shown is covered by the dummy pattern to meet this limitation)). Accordingly, Watanabe '811 discloses each and every element of claims 1 and 9.

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Regarding dependent claims 2-5 and 10-13 of the '629 patent, Watanabe '811 discloses that the wiring structures are multilayers with the lower layer including aluminum and the upper layer including, chromium or titanium. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059]. Thus, Watanabe discloses a wiring including at least an upper layer and lower layer of conductive materials (claims 2 and 10), with the lower layer of aluminum (claim 3) and the upper layer of chromium or titanium (claims 4 and 5). *See e.g.*, Watanabe '811, [0047] and [0058]-[0059]. Therefore, Watanabe '811 meets the limitations of claims 2-5 and 10-13 of the '629 patent.

Regarding dependent claims 7-8 and 15-16, Watanabe '811 inherently teaches the limitation of these claims, namely that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant. As demonstrated by the Examiner in the prosecution of the '629 patent, disclosure of materials such as those identified in the '629 APA, molybdenum, chromium, titanium, or tantalum, for the upper layer wiring meet the limitation of claims 7-8 and 15-16. For example, the examiner

stated that because Song taught a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum the limitation of claims 7-8 and 15-16 were met. See '629 file history, Office Action dated May 29, 2003 at page 3. Therefore, Watanabe '811 meets the limitations of claims 7-8 and 15-16 of the '629 patent.

Accordingly, Watanabe '811 discloses each and every element, and fully anticipates claims 1-5, 7-13, and 15-16 of the '629 patent. A claim chart providing a detailed element by element analysis is provided in the attached Appendix CC25.

Z. Japanese Publication No. H06-082811 to Watanabe in view of U.S. Patent No. 6,163,356 to Song Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Song was filed with the U.S. Patent Office on Jul. 24, 1997 and was issued on Dec. 19, 2000. Because Song issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Watanabe '811 in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. **However, Song was not considered in conjunction with Watanabe '811, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Watanabe '811 provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Watanabe '811, Fig. 5, and [0071]), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Watanabe '811 and Song important to the patentability of the '629 patent and new and non-cumulative.** As such, Watanabe '811 in view of Song constitutes a substantial new

question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Watanabe '811 Discloses Each and Every Element of Claims 1 and 9

As discussed above, Watanabe '811 discloses each and every element of claims 1 and 9. Watanabe '811 addresses the issue of cell gap uniformity to achieve a better quality display. To resolve this issue, Watanabe '811 provides additional conductive dummy patterns in the region between the pixel array and the contact pads. As shown in Fig. 5, the dummy patterns comprise 30% of the "area." For example, if the selected area is limited to where a single dummy pattern or just a portion of the dummy pattern is located, it will cover 100% of the selected area.

Regarding each element of claims 1 and 9, Watanabe '811 discloses an array substrate for display (*See e.g.*, Watanabe '811, Fig. 5, and [0034] (disclosing an array substrate for a liquid crystal display and method of forming an array substrate): including an insulating substrate, having an area (*See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038] (disclosing a glass, and thus insulating, substrate upon which a TFT array of a liquid crystal display is formed)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Watanabe '811, Fig. 5, and [0034] (disclosing an array substrate for a liquid crystal display and method of forming an array substrate); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See e.g.*, Watanabe '811, [0035] (disclosing thin film transistors connected by signal and scanning lines 5 and 9)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Watanabe '811, [0035] (disclosing that the active matrix display includes scanning and signal lines that provide video-signal to thin film transistors), *see also* Watanabe '811, Fig. 5 (depicting that the scanning and signal lines connect to respective driving circuits, thus connection pads would be inherently present in Watanabe '811 because

such is the typical connection between the lines and the driving circuits)); pixel electrodes (*See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035] (identifying pixel electrodes as items 7 in figure 4)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071] (disclosing that the metal dummy patterns, items 25 and 27, in figure 5 are situated between the connection pads and pixel electrode array and are not in contact with any of the wiring), see also Watanabe '811, Figs. 5 (depicting it is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed, shown in figure 5, where at least 30% of the area shown is covered by the dummy pattern to meet this limitation)). Accordingly, Watanabe '811 discloses each and every element of claims 1 and 9.[19]

2. Song Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is

[19] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Watanabe '811 disclosures.

selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. **As noted by the examiner during the prosecution of the '629 patent, this wiring structure of Song meets all of the limitations of claims 2-8 and 10-16.** See '629 File History, Office Action dated May 29, 2003 at page 3. Namely, Song discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum (claim 3 and 11) and the upper layer wiring material can be one of a variety of upper layer wiring materials such as molybdenum (claims 4-6 and 14). Song col 4, ll. 30-50; col. 8 ll. 5-18. The disclosed upper layer wiring material, such as molybdenum, inherently does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

3. The Combined Teachings of Watanabe '811 and Song Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Watanabe '811 describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059]. Song teaches an improved wiring structure with low resistance and protective covering. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Song for the wiring in Watanabe '811 in a predictable way to obtain predictable results.

Accordingly, Watanabe '811 in view of Song discloses each and every element, and thus renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed

element by element analysis of the obviousness by Watanabe '811 in view of Song of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC26.

AA. Japanese Publication No. H06-082811 to Watanabe in view of the '629 Admitted Prior Art Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

A substantial new question of patentability is raised by Watanabe '811 in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. **However, the '629 APA was not considered in conjunction with Watanabe '811, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Watanabe '811 provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Watanabe '811, Fig. 5, and [0071]), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Watanabe '811 and the '629 APA important to the patentability of the '629 patent and new and non-cumulative.** As such, Watanabe '811 in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Watanabe '811 Discloses Each and Every Element of Claims 1 and 9

As discussed above, Watanabe '811 discloses each and every element of claims 1 and 9. Watanabe '811 addresses the issue of cell gap uniformity to achieve a better quality display. To resolve this issue, Watanabe '811 provides additional conductive dummy patterns in the region between the pixel array and the contact pads. As shown in Fig. 5, the dummy patterns comprise 30% of the "area." For example, if the selected area is limited to where a single dummy pattern or just a portion of the dummy pattern is located, it will cover 100% of the selected area.

Regarding each element of claims 1 and 9, Watanabe '811 discloses an array substrate for display (*See e.g.*, Watanabe '811, Fig. 5, and [0034] (disclosing an array substrate for a liquid crystal display and method of forming an array substrate): including an insulating substrate, having an area (*See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038] (disclosing a glass, and thus insulating, substrate upon which a TFT array of a liquid crystal display is formed)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Watanabe '811, Fig. 5, and [0034] (disclosing an array substrate for a liquid crystal display and method of forming an array substrate); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See e.g.*, Watanabe '811, [0035] (disclosing thin film transistors connected by signal and scanning lines 5 and 9)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Watanabe '811, [0035] (disclosing that the active matrix display includes scanning and signal lines that provide video-signal to thin film transistors), *see also* Watanabe '811, Fig. 5 (depicting that the scanning and signal lines connect to respective driving circuits, thus connection pads would be inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits)); pixel electrodes (*See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035] (identifying pixel electrodes as items 7 in figure 4)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071] (disclosing that the metal dummy patterns, items 25 and 27, in figure 5 are situated between the connection pads and pixel electrode array and are not in contact with any of the wiring), see also Watanabe '811, Figs. 5 (depicting it is

possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed, shown in figure 5, where at least 30% of the area shown is covered by the dummy pattern to meet this limitation)). Accordingly, Watanabe '811 discloses each and every element of claims 1 and 9.[20]

2. The '629 APA Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

The '629 APA discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is low resistance aluminum (claim 3 and 11) and the upper layer wiring material of a material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum (claims 4-6 and 14). See e.g., the '629 patent, col. 1, ll. 26-39. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29,

[20] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Watanabe '811 disclosures.

2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Watanabe '811 and the '629 APA Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Watanabe '811 describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059]. The '629 APA teaches an improved wiring structure with low resistance and is harder is oxidize. See e.g., the '629 patent, col. 1, ll. 26-39. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of the '629 APA for the wiring in Watanabe '811 in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the upper material of Watanabe '811 for the molybdenum as taught in the '629 APA, since molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Watanabe '811 in view of the '629 APA discloses each and every element and renders obvious claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Watanabe '811 in view of the '629 APA of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC27.

BB. Japanese Publication No. H06-082811 to Watanabe in view of U.S. Patent No. 6,157,430 to Kubota Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Kubota was filed with the U.S. Patent Office on Sept. 29, 1997 and was issued on Dec. 5, 2000. Because Kubota issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Watanabe '811 in view of Kubota. Neither Watanabe '811 nor Kubota were before the Patent Office during the prosecution of the '629 patent. Watanabe '811, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Watanabe '811 provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Watanabe '811, Fig. 5, and [0071]), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Watanabe '811 and Kubota important to the patentability of the '629 patent and new and non-cumulative.** As such, Watanabe '811 in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Watanabe '811 Discloses Each and Every Element of Claims 1 and 9

As discussed above, Watanabe '811 discloses each and every element of claims 1 and 9. Watanabe '811 addresses the issue of cell gap uniformity to achieve a better quality display. To resolve this issue, Watanabe '811 provides additional conductive dummy patterns in the region between the pixel array and the contact pads. As shown in Fig. 5, the dummy patterns comprise 30% of the "area." For example, if the selected area is limited to where a single dummy pattern or just a portion of the dummy pattern is located, it will cover 100% of the selected area.

Regarding each element of claims 1 and 9, Watanabe '811 discloses an array substrate for display (*See e.g.*, Watanabe '811, Fig. 5, and [0034] (disclosing an array substrate for a liquid crystal display and method of forming an array substrate): including an insulating substrate, having an area (*See e.g.*, Watanabe '811, Fig. 5, item 200, and [0034]-[0038] (disclosing a glass,

and thus insulating, substrate upon which a TFT array of a liquid crystal display is formed)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Watanabe '811, Fig. 5, and [0034] (disclosing an array substrate for a liquid crystal display and method of forming an array substrate); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See e.g.*, Watanabe '811, [0035] (disclosing thin film transistors connected by signal and scanning lines 5 and 9)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Watanabe '811, [0035] (disclosing that the active matrix display includes scanning and signal lines that provide video-signal to thin film transistors), *see also* Watanabe '811, Fig. 5 (depicting that the scanning and signal lines connect to respective driving circuits, thus connection pads would be inherently present in Watanabe '811 because such is the typical connection between the lines and the driving circuits)); pixel electrodes (*See e.g.*, Watanabe '811, Fig. 4, item 7, and [0035] (identifying pixel electrodes as items 7 in figure 4)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. *See e.g.*, Watanabe '811, Fig. 5, and [0071] (disclosing that the metal dummy patterns, items 25 and 27, in figure 5 are situated between the connection pads and pixel electrode array and are not in contact with any of the wiring), see also Watanabe '811, Figs. 5 (depicting it is possible to select any region between the pixel electrode and the connection pads where the dummy patterns are formed, shown in figure 5, where at least 30% of the area shown is covered

by the dummy pattern to meet this limitation)). Accordingly, Watanabe '811 discloses each and every element of claims 1 and 9.[21]

2. Kubota Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Kubota discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum or aluminum alloy (claim 3 and 11) and the upper layer wiring material from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof (claims 4-6 and 14). See e.g., Kubota, col. 4, ll. 39-55. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Watanabe '811 and Kubota Render Obvious Claims 2-8 and 10-16 of the '629 Patent

[21] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Watanabe '811 disclosures.

Watanabe '811 describes exemplary wiring structures, suggesting other wiring structures may be substituted as appropriate. *See e.g.*, Watanabe '811, [0047] and [0058]-[0059]. Kubota teaches an improved wiring structure with the upper layer having a high hardness. See e.g., Kubota, col. 4, ll. 39-45. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Kubota for the wiring in Watanabe '811 in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the upper material of Watanabe '811 for the molybdenum as taught in Kubota, since molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Watanabe '811 in view of Kubota discloses each and every element and renders obvious claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Watanabe '811 in view of Kubota of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC28.

CC. Japanese Publication No. H09-197415 to Miyashita Raises A Substantial New Question of Patentability and Anticipates Claims 1 and 9 of the '629 Patent

Miyashita was published July 31, 1997. Because Miyashita was published more than one year before the filing date of the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability as to claims 1 and 9 is raised by Miyashita. Miyashita was not considered by the Patent Office during the prosecution of the '629 patent. As discussed above, the Patent Office, without knowledge of Miyashita, allowed the'629 patent on the rationale that the art did not teach or suggest:

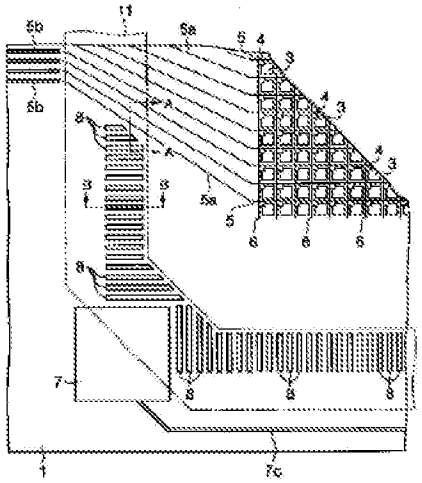
> a layer of an insulating substrate, *having an area*;...dummy conductive patterns, *the dummy patterns comprising at least about 30% of the area of the insulating substrate*.

As discussed in more detail below, Miyashita teaches this feature. *See e.g.*, Miyashita, Fig. 2 (dummy film forming region D); Fig 3 (dummy film 8); [0023]-[0025]. **Miyashita teaches the feature which was identified as the allowable subject matter of the '629 patent and was not previously disclosed or suggested by the art of record. Thus, a reasonable examiner would consider these teachings of Miyashita important to the patentability of the '629 patent and new and non-cumulative.** As such, Requestor believes that these teachings of Miyashita raise a substantial new question of patentability with respect to independent claims 1 and 9.

1. Miyashita Is New, Non-Cumulative Art Because It Discloses the Identified Allowable Feature of the '629 Patent, Dummy Patterns Comprising at Least about 30% of the Area

Miyashita addresses issues resulting from the non-uniformity of cell gap. Accordingly, Miyashita provides a method of achieving uniformity by adding dummy patterns arranged around the TFT array. Ultimately, this results in better quality liquid crystal displays. As shown below in Fig. 3, the dummy film 8 in the dummy film region D comprises a significant portion of the area between the pixel electrodes 3 and the lead part 5a and 6a. *See e.g.*, Miyashita, Fig. 3.

[図３]



For example, if the selected area is limited to where a single dummy pattern or even the entire dummy film area D, identified in Fig. 2, the dummy patterns will comprise will cover 100% or close thereto of the selected area. *See e.g.*, Miyashita, Figs. 2-3, [0023]-[0025]. In other words, **Mayashita discloses an insulating substrate having an area, with dummy patterns comprising 30% of the area, which was identified as the allowable subject matter of claims 1 and 9 of the '629 patent.** Further, the dummy patterns are also located between the pixel electrode and the connection pads and not in contact with the wiring.

2. Miyashita Discloses Each and Every Element of Claims 1 and 9

Regarding each element of claims 1, Miyashita discloses an array substrate for display (*See e.g.*, Miyashita, Fig. 3, and [0018]-[0019] (disclosing an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed): including an insulating substrate, having an area (*See e.g.*, Miyashita, Fig. 3, and [0018]-[0019] (disclosing an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019] (disclosing that the device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See e.g.*, Miyashita , [0019] and Fig 2 (disclosing thin film transistors connected by gate and data lines 5 and 6)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Miyashita, [0019] (disclosing that the active matrix display includes gate and data lines that provide gate and data signals to thin film transistors), *see also* Miyashita, [0019] and Fig. 1 (disclosing that the gate and data lines extend to the edge of the substrate and contact pads 5b and 6b)); pixel electrodes (*See e.g.*, Miyashita, Fig. 3 (depicting pixel electrodes items 3), *see also e.g.*, Miyashita, [0019]

(describing that the pixel electrodes are transparent and correspond to display areas that are arranged as a matrix), *see also e.g.*, Miyashita, [002]-[003] (disclosing that the pixel electrode drive the liquid crystal)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. (*See e.g.* Miyashita, Fig 2 (dummy film forming region D); [0023] (disclosing that dummy film is formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3), *see also e.g.*,. Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025] (providing a closer view depicting the dummy patterns 8, covering a various areas, thus dummy patterns comprise at least 30% of the area shown)). Accordingly, Miyashita discloses each and every element of claims 1.

Regarding each element of claim 9, Miyashita discloses a method for forming an array substrate for display, comprising (*See e.g.*, Miyashita, Fig. 3, and [0018]-[0019] (disclosing an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed): forming a layer of an insulating substrate, having an area (*See e.g.*, Miyashita, Fig. 3, and [0018]-[0019] (disclosing an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed)); forming a thin film transistor array formed on the insulating substrate (*See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019] (disclosing that the device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate)); each wiring having a first end, the wiring in communication with at least on of the transistors in the thin film array (*See e.g.*, Miyashita , [0019] and Fig 2 (disclosing thin film transistors connected by gate and data lines 5 and 6)); forming connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*,

Miyashita, [0019] (disclosing that the active matrix display includes gate and data lines that provide gate and data signals to thin film transistors), *see also* Miyashita, [0019] and Fig. 1 (disclosing that the gate and data lines extend to the edge of the substrate and contact pads 5b and 6b)); forming pixel electrodes (*See e.g.*, Miyashita, Fig. 3 (depicting pixel electrodes items 3), *see also e.g.*, Miyashita, [0019] (describing that the pixel electrodes are transparent and correspond to display areas that are arranged as a matrix), *see also e.g.*, Miyashita, [002]-[003] (disclosing that the pixel electrode drive the liquid crystal)); and forming dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patterns are not in contact with any of the wiring. (*See e.g.* Miyashita, Fig 2 (dummy film forming region D); [0023] (disclosing that dummy film is formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3), *see also e.g.*,. Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025] (providing a closer view depicting the dummy patterns 8, covering a various areas, thus dummy patterns comprise at least 30% of the area shown)). Accordingly, Miyashita discloses each and every element of claims 1 and 9.

Accordingly, Miyashita discloses each and every element, and fully anticipates, claims 1 and 9 of the '629 patent. A claim chart providing a detailed element by element analysis is attached as Appendix CC29.

DD. Japanese Publication No. H09-197415 to Miyashita in view of U.S. Patent No. 6,163,356 to Song Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Song was filed with the U.S. Patent Office on Jul. 24, 1997 and was issued on Dec. 19, 2000. Because Song issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Miyashita in view of Song. Song was considered by the Patent Office during the prosecution of the '629 patent and was applied for teaching the limitations of dependent claims 2-8 and 10-16. **However, Song was not considered in conjunction with Miyashita, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Miyashita provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Miyashita, Fig. 2 (dummy film forming region D); Fig 3 (dummy patterns 8); [0023]-[0025]), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Song teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Miyashita and Song important to the patentability of the '629 patent and new and non-cumulative.** As such, Miyashita in view of Song constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9**.**

1. Miyashita Discloses Each and Every Element of Claims 1 and 9

As discussed above, Miyashita discloses each and every element of claims 1 and 9. Miyashita addresses issues resulting from the non-uniformity of cell gap. Accordingly, Miyashita provides a method of achieving uniformity by adding dummy patterns arranged around the TFT array. Ultimately, this results in better quality liquid crystal displays. As shown in Figs. 2-3, the dummy patterns comprise 30% of an "area." For example, if the selected area is limited to where a single dummy pattern or just a portion of the dummy pattern is located, it will cover 100% of the selected area. The dummy patterns are also located between the pixel electrode and the connection pads and not in contact with the wiring.

Regarding each element of claims 1 and 9, Miyashita discloses an array substrate for display (*See e.g.*, Miyashita, Fig. 3, and [0018]-[0019] (disclosing an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed): including an insulating substrate, having an area (*See e.g.*, Miyashita, Fig. 3, and [0018]-[0019] (disclosing an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019] (disclosing that the device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See e.g.*, Miyashita , [0019] and Fig 2 (disclosing thin film transistors connected by gate and data lines 5 and 6)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Miyashita, [0019] (disclosing that the active matrix display includes gate and data lines that provide gate and data signals to thin film transistors), *see also* Miyashita, [0019] and Fig. 1 (disclosing that the gate and data lines extend to the edge of the substrate and contact pads 5b and 6b)); pixel electrodes (*See e.g.*, Miyashita, Fig. 3 (depicting pixel electrodes items 3), *see also e.g.*, Miyashita, [0019] (describing that the pixel electrodes are transparent and correspond to display areas that are arranged as a matrix), *see also e.g.*, Miyashita, [002]-[003] (disclosing that the pixel electrode drive the liquid crystal)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. (*See e.g.* Miyashita, Fig 2 (dummy film forming region D); [0023] (disclosing that dummy film is formed in the dummy film forming region D, shown in

Fig. 2, which is located between the connection pads 5b the pixel electrodes 3), *see also e.g.,*. Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025] (providing a closer view depicting the dummy patterns 8, covering a various areas, thus dummy patterns comprise at least 30% of the area shown)). Accordingly, Miyashita discloses each and every element of claims 1 and 9.[22]

2. Song Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Song discloses a dual layer wiring including aluminum with chromium, molybdenum, tantalum or antimony on top. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18**. As noted by the examiner during the prosecution of the '629 patent, this wiring structure of Song meets all of the limitations of claims 2-8 and 10-16.** See '629 File History, Office Action dated May 29, 2003 at page 3. Namely, Song discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum (claim 3 and 11) and the upper layer wiring material can be one of a variety of upper layer wiring materials such as molybdenum

[22] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Miyashita disclosures.

(claims 4-6 and 14). Song col 4, ll. 30-50; col. 8 ll. 5-18. The disclosed upper layer wiring material, such as molybdenum, inherently does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

3. The Combined Teachings of Miyashita and Song Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Miyashita describes exemplary wiring structures, such as an aluminum/chromium film, suggesting other wiring structures may be substituted as appropriate. See, e.g., Miyashita, [0038]-[0039]. Song teaches an improved wiring structure with low resistance and protective covering. See e.g., Song col 4, ll. 30-50; col. 8 ll. 5-18. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Song for the wiring in Miyashita in a predictable way to obtain predictable results.

Accordingly, Miyashita in view of Song discloses each and every element, and thus renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Miyashita in view of Song of claims 2-8 and 10-16 of the '629 patent is attached as Appendix CC30.

EE. Japanese Publication No. H09-197415 to Miyashita in view of the '629 Admitted Prior Art Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

A substantial new question of patentability is raised by Miyashita in view of the '629 APA. The '629 APA was before the Patent Office during the prosecution of the '629 patent. **However, the '629 APA was not considered in conjunction with Miyashita, which as discussed above raises a substantial new question of patentability and teaches each and every element of claims 1 and 9.** Namely, Miyashita provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Miyashita, Fig. 2 (dummy film

forming region D); Fig 3 (dummy patterns 8); [0023]-[0025]), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, the '629 APA teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would consider the combined teachings of Miyashita and the '629 APA important to the patentability of the '629 patent and new and non-cumulative.** As such, Miyashita in view of the '629 APA constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Miyashita Discloses Each and Every Element of Claims 1 and 9

As discussed above, Miyashita discloses each and every element of claims 1 and 9. Miyashita addresses issues resulting from the non-uniformity of cell gap. Accordingly, Miyashita provides a method of achieving uniformity by adding dummy patterns arranged around the TFT array. Ultimately, this results in better quality liquid crystal displays. As shown in Figs. 2-3, the dummy patterns comprise 30% of an "area." For example, if the selected area is limited to where a single dummy pattern or just a portion of the dummy pattern is located, it will cover 100% of the selected area. The dummy patterns are also located between the pixel electrode and the connection pads and not in contact with the wiring.

Regarding each element of claims 1 and 9, Miyashita discloses an array substrate for display (*See e.g.*, Miyashita, Fig. 3, and [0018]-[0019] (disclosing an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed): including an insulating substrate, having an area (*See e.g.*, Miyashita, Fig. 3, and [0018]-[0019] (disclosing an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019] (disclosing that the device in Miyashita is an active matrix

display with a thin film transistor array on the insulating substrate)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See e.g.*, Miyashita , [0019] and Fig 2 (disclosing thin film transistors connected by gate and data lines 5 and 6)); connections pads, each connection pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Miyashita, [0019] (disclosing that the active matrix display includes gate and data lines that provide gate and data signals to thin film transistors), *see also* Miyashita, [0019] and Fig. 1 (disclosing that the gate and data lines extend to the edge of the substrate and contact pads 5b and 6b)); pixel electrodes (*See e.g.*, Miyashita, Fig. 3 (depicting pixel electrodes items 3), *see also e.g.*, Miyashita, [0019] (describing that the pixel electrodes are transparent and correspond to display areas that are arranged as a matrix), *see also e.g.*, Miyashita, [002]-[003] (disclosing that the pixel electrode drive the liquid crystal)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. (*See e.g.* Miyashita, Fig 2 (dummy film forming region D); [0023] (disclosing that dummy film is formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3), *see also e.g.*,. Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025] (providing a closer view depicting the dummy patterns 8, covering a various areas, thus dummy patterns comprise at least 30% of the area shown)). Accordingly, Miyashita discloses each and every element of claims 1 and 9.[23]

[23] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Miyashita disclosures.

2. The '629 APA Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

The '629 APA discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is low resistance aluminum (claim 3 and 11) and the upper layer wiring material of a material that is harder to oxidize such as chromium, tantalum, titanium or molybdenum (claims 4-6 and 14). See e.g., the '629 patent, col. 1, ll. 26-39. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Miyashita and the '629 APA Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Miyashita describes exemplary wiring structures, such as an aluminum/chromium film, suggesting other wiring structures may be substituted as appropriate. See, e.g., Miyashita, [0038]-[0039]. The '629 APA teaches an improved wiring structure with low resistance and is harder is oxidize. See e.g., the '629 patent, col. 1, ll. 26-39. Thus, based on these teachings, it

would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of the '629 APA for the wiring in Miyashita in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the upper material of Miyashita for the molybdenum as taught in the '629 APA, since molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Miyashita in view of the '629 APA discloses each and every element, and this renders obvious, claims 2-8 and 10-16 of the '629 patent. The following chart provides a detailed element by element analysis of the obviousness by Miyashita in view of the '629 APA of claims 2-8 and 10-16 of the '629 patent.

FF. Japanese Publication No. H09-197415 to Miyashita in view of U.S. Patent No. 6,157,430 to Kubota Raises A Substantial New Question of Patentability and Renders Obvious Claims 2-8 and 10-16 of the '629 Patent

Kubota was filed with the U.S. Patent Office on Sept. 29, 1997 and was issued on Dec. 5, 2000. Because Kubota issued more than one year before the filing date the '629 patent, it constitutes prior art under 35 U.S.C. § 102(b).

A substantial new question of patentability is raised by Miyashita in view of Kubota. Neither Miyashita nor Kubota were before the Patent Office during the prosecution of the '629 patent. Miyashita, as discussed above, raises a substantial new question of patentability and teaches each and every element of claims 1 and 9. Namely, Miyashita provides dummy patterns comprising at least about 30% of an area of the insulating substrate (*See e.g.*, Miyashita, Fig. 2 (dummy film forming region D); Fig 3 (dummy patterns 8); [0023]-[0025]), which was identified as the allowable subject matter of the '629 patent, and as a feature not previously disclosed or suggested by the art of record. Additionally, Kubota teaches each and every limitation of dependent claims 2-8 and 10-16. **Thus, a reasonable examiner would**

consider the combined teachings of Miyashita and Kubota important to the patentability of the '629 patent and new and non-cumulative. As such, Miyashita in view of Kubota constitutes a substantial new question of patentability as to claims 2-8, which depend from claim 1, and 10-16, which depend from claim 9.

1. Miyashita Discloses Each and Every Element of Claims 1 and 9

As discussed above, Miyashita discloses each and every element of claims 1 and 9. Miyashita addresses issues resulting from the non-uniformity of cell gap. Accordingly, Miyashita provides a method of achieving uniformity by adding dummy patterns arranged around the TFT array. Ultimately, this results in better quality liquid crystal displays. As shown in Figs. 2-3, the dummy patterns comprise 30% of an "area." For example, if the selected area is limited to where a single dummy pattern or just a portion of the dummy pattern is located, it will cover 100% of the selected area. The dummy patterns are also located between the pixel electrode and the connection pads and not in contact with the wiring.

Regarding each element of claims 1 and 9, Miyashita discloses an array substrate for display (*See e.g.*, Miyashita, Fig. 3, and [0018]-[0019] (disclosing an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed): including an insulating substrate, having an area (*See e.g.*, Miyashita, Fig. 3, and [0018]-[0019] (disclosing an insulating substrate that may consist of glass on which an active matrix type liquid crystal cell is formed)); a thin film transistor array formed on the insulating substrate (*See e.g.*, Miyashita, Fig. 3, item 4 (TFT), and [0019] (disclosing that the device in Miyashita is an active matrix display with a thin film transistor array on the insulating substrate)); a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array (*See e.g.*, Miyashita , [0019] and Fig 2 (disclosing thin film transistors connected by gate and data lines 5 and 6)); connections pads, each connection

pad contacting the first end of at most one of the plurality of wirings (*See e.g.*, Miyashita, [0019] (disclosing that the active matrix display includes gate and data lines that provide gate and data signals to thin film transistors), *see also* Miyashita, [0019] and Fig. 1 (disclosing that the gate and data lines extend to the edge of the substrate and contact pads 5b and 6b)); pixel electrodes (*See e.g.*, Miyashita, Fig. 3 (depicting pixel electrodes items 3), *see also e.g.*, Miyashita, [0019] (describing that the pixel electrodes are transparent and correspond to display areas that are arranged as a matrix), *see also e.g.*, Miyashita, [002]-[003] (disclosing that the pixel electrode drive the liquid crystal)); and dummy conductive patterns, the dummy patterns comprising at least about 30% of the area of the insulating substrate, the dummy conductive patterns situated between the connection pads and the pixel electrodes such that the dummy patters are not in contact with any of the wiring. (*See e.g.* Miyashita, Fig 2 (dummy film forming region D); [0023] (disclosing that dummy film is formed in the dummy film forming region D, shown in Fig. 2, which is located between the connection pads 5b the pixel electrodes 3), *see also e.g.*,. Miyashita, Fig 3 (dummy patterns 8); [0024]-[0025] (providing a closer view depicting the dummy patterns 8, covering a various areas, thus dummy patterns comprise at least 30% of the area shown)). Accordingly, Miyashita discloses each and every element of claims 1 and 9.[24]

2. Kubota Discloses Each And Every Element of Claims 2-8 and 10-16

Claims 2-8, depending from claim 1, and 10-16, depending from claim 9, of the '629 Patent require that the wiring include at least an upper layer and lower layer of conductive material (claims 2 and 10); that the lower layer wiring is selected from a group consisting of aluminum and aluminum alloys (claims 3 and 11); that the upper layer wiring material is selected

[24] While only the text of claim 1 is cited in this section, the corresponding elements of method claim 9, as discussed above, are met by the same Miyashita disclosures.

from the group consisting of molybdenum, chromium, tantalum, titanium or alloys thereof (claims 4 and 5), that the upper wiring material is selected from the group consisting of molybdenum and alloys thereof (claims 6 and 14); and that the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16).

Kubota discloses a wiring with an upper and lower layer (claims 2 and 10), where the lower layer wiring material is aluminum or aluminum alloy (claim 3 and 11) and the upper layer wiring material from a group consisting of chromium, titanium, tantalum, molybdenum or alloys thereof (claims 4-6 and 14). See e.g., Kubota, col. 4, ll. 39-55. The disclosed upper layer wiring materials, such as molybdenum, inherently do not become insoluble in an acid or alkaline etchant (claims 7-8 and 15-16). *See* '629 file history, Office Action dated May 29, 2003 at page 3 (rejecting the claims based on the disclosure of a bilayer with a bottom layer of aluminum and an upper layer of chromium, molybdenum, or tantalum).

3. The Combined Teachings of Miyashita and Kubota Render Obvious Claims 2-8 and 10-16 of the '629 Patent

Miyashita describes exemplary wiring structures, such as aluminum/chromium film, suggesting other wiring structures may be substituted as appropriate. See, e.g., Miyashita, [0038]-[0039]. Kubota teaches an improved wiring structure with the upper layer having a high hardness. See e.g., Kubota, col. 4, ll. 39-45. Thus, based on these teachings, it would be obvious to one of ordinary skill in the art at the time of the '629 patent to substitute the well known improved dual layer wiring of Kubota for the wiring in Miyashita in a predictable way to obtain predictable results. Additionally, one of skill would have replaced the upper material of Miyashita for the molybdenum as taught in Kubota, since molybdenum is harder to oxidize and because it is obvious to one of ordinary skill in the art to employ a material for its intended use.

Accordingly, Miyashita in view of Kubota discloses each and every element, and thus renders obvious, claims 2-8 and 10-16 of the '629 patent. A claim chart providing a detailed element by element analysis of the obviousness by Miyashita in view of Kubota of claims 2-8 and 10-16 of the '629 patent is attached is Appendix CC32.

VI. CONCLUSION

Because a reasonable examiner would consider the above identified teachings and prior art references important in deciding whether to allow the claims of the '629 patent, this Request raises a substantial new question of patentability as to claims 1-16 that should be considered during reexamination.

Respectfully submitted,

Date: March 16, 2010

By /Song K. Jung/

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(202) 496-7500

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re: Reexamination of U.S. Patent No. 6,689,629 B2

Control No.: 90/009,697

Inventors: Tsujimura et al.

Issued: February 10, 2004

Filed: February 5, 2002

Titled: Array Substrate For Display, Method of Manufacturing Array Substrate For Display and Display Device Using the Array Substrate

Atty. Docket: 7773.084

CERTIFICATE OF SERVICE

Mail Stop ***Ex Parte Reexamination***
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.33(c) and M.P.E.P. § 2220, I hereby certify that a true and correct copy of the Revised Request For *Ex Parte* Reexamination of U.S. Patent No. 6,689,629 was served on March 16, 2010, on the following attorney of record in U.S. Patent No. 6,689,629 via first class mail at the following addresses.

Daniel McClure
Thomas, Kayden, Horstmeyer & Risley, LLP
600 Galleria Parkway, S.E.
15th Floor
Atlanta, GA 30339-5994

DATED this 16th day of March, 2010 /Song K. Jung/
Song K. Jung

DC:50680151.3

Electronic Acknowledgement Receipt

EFS ID:	7222139
Application Number:	90009697
International Application Number:	
Confirmation Number:	5947
Title of Invention:	ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE
First Named Inventor/Applicant Name:	6689629
Customer Number:	24504
Filer:	Song K. Jung/Angela Ellis
Filer Authorized By:	Song K. Jung
Attorney Docket Number:	7773.0084
Receipt Date:	16-MAR-2010
Filing Date:	
Time Stamp:	17:35:49
Application Type:	Reexam (Third Party)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		07773_084_61_FINAL_revised_reexam.pdf	1036753 39c27d3d563eed85191bc2f824461de97df6e386	yes	177

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Trans Letter filing of a response in a reexam	1	2
	Reexam Miscellaneous Incoming Letter	3	176
	Reexam Certificate of Service	177	177
Warnings:			
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Bib Data Sheet

CONFIRMATION NO. 5947

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
90/009,697	03/16/2010 RULE	438	3992	7773.0084

APPLICANTS

6689629, Residence Not Provided;
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SONG K. JUNG (3RD PTY REQ.), WASHINGTON, DC;
MCKENNA LONG & ALDRIDGE, LLP, WASHINGTON, DC

**** CONTINUING DATA ***************************

This application is a REX of 10/068,500 02/05/2002 PAT 6,689,629

**** FOREIGN APPLICATIONS ***********************

JAPAN 2001-029587 02/06/2001

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☐ no				
35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature Initials			16	2

ADDRESS
24504

TITLE
ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE

FILING FEE RECEIVED	FEES: Authority has been given in Paper
2520	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:

- ☐ All Fees
- ☐ 1.16 Fees (Filing)
- ☐ 1.17 Fees (Processing Ext. of time)
- ☐ 1.18 Fees (Issue)
- ☐ Other _____
- ☐ Credit

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	90/009,697	6689629	
	Examiner	Art Unit	
		3992	

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
90/009,697	6689629
Examiner	**Art Unit** 3992

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Issue Classification	Application/Control No. 90/009,697	Applicant(s)/Patent under Reexamination 6689629
	Examiner	Art Unit 3992

ISSUE CLASSIFICATION

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
438	25	/	/
CROSS REFERENCES		/	/
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)		
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(Assistant Examiner) (Date)		Total Claims Allowed:
(Legal Instruments Examiner) (Date)	(Primary Examiner) (Date)	O.G. Print Claim(s) / O.G. Print Fig.

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
	4		34		64		94		124		154		184
	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
	14		44		74		104		134		164		194
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	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
	21		51		81		111		141		171		201
	22		52		82		112		142		172		202
	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Reexamination	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/009,697	6689629
	Certificate Date	Certificate Number

Requester Correspondence Address: ☐ Patent Owner ☒ Third Party

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LITIGATION REVIEW ☐	(examiner initials)	(date)
Case Name		Director Initials

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	NUMBER
1.	
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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
90/009,697	6689629	
Examiner	Art Unit	
	3992	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR

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REEXAM CONTROL NUMBER	FILING OR 371 (c) DATE	PATENT NUMBER
90/009,697	03/16/2010	6689629

CONFIRMATION NO. 5947

MCKENNA LONG & ALDRIDGE, LLP
1900 K STREET, NW
WASHINGTON, DC 20006

REEXAMINATION REQUEST NOTICE

OC000000040730875

Date Mailed: 03/19/2010

NOTICE OF REEXAMINATION REQUEST FILING DATE

(Third Party Requester)

Requester is hereby notified that the filing date of the request for reexamination is 03/16/2010, the date that the filing requirements of 37 CFR § 1.510 were received.

A decision on the request for reexamination will be mailed within three months from the filing date of the request for reexamination. (See 37 CFR 1.515(a)).

A copy of the Notice is being sent to the person identified by the requester as the patent owner. Further patent owner correspondence will be the latest attorney or agent of record in the patent file. (See 37 CFR 1.33). Any paper filed should include a reference to the present request for reexamination (by Reexamination Control Number).

cc: Patent Owner
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Legal Instruments Examiner
Central Reexamination Unit 571-272-7705; FAX No. 571-273-9900

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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www.uspto.gov

REEXAM CONTROL NUMBER	FILING OR 371 (c) DATE	PATENT NUMBER
90/009,697	03/16/2010	6689629

CONFIRMATION NO. 5947

REEXAM ASSIGNMENT NOTICE

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Date Mailed: 03/19/2010

NOTICE OF ASSIGNMENT OF REEXAMINATION REQUEST

The above-identified request for reexamination has been assigned to Art Unit 3992. All future correspondence to the proceeding should be identified by the control number listed above and directed to the assigned Art Unit.

A copy of this Notice is being sent to the latest attorney or agent of record in the patent file or to all owners of record. (See 37 CFR 1.33(c)). If the addressee is not, or does not represent, the current owner, he or she is required to forward all communications regarding this proceeding to the current owner(s). An attorney or agent receiving this communication who does not represent the current owner(s) may wish to seek to withdraw pursuant to 37 CFR 1.36 in order to avoid receiving future communications. If the address of the current owner(s) is unknown, this communication should be returned within the request to withdraw pursuant to Section 1.36.

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Central Reexamination Unit 571-272-7705; FAX No. 571-273-9900

Litigation Search Report CRU 3999

Reexam Control No. 90/009,697

TO: MARK REINHART **Location: CRU** **Art Unit: 3992** **Date: 03/20/10**	**From: MANUEL SALDANA** **Location: CRU 3999** **MDW 7C55** **Phone: (571) 272-7740** **MANUEL.SALDANA@uspto.gov**

Search Notes

Litigation was found for US Patent Number: 6,689,629.
DOCKET 1:07CV357 (NOT CLOSED)
DOCKET 1:07CV137 (CLOSED 05/30/07).

1) I performed a KeyCite Search in Westlaw, which retrieves all history on the patent including any litigation.

2) I performed a search on the patent in Lexis CourtLink for any open dockets or closed cases.

3) I performed a search in Lexis in the Federal Courts and Administrative Materials databases for any cases found.

4) I performed a search in Lexis in the IP Journal and Periodicals database for any articles on the patent.

5) I performed a search in Lexis in the news databases for any articles about the patent or any articles about litigation on this patent.

Date of Printing: Mar 20, 2010

KEYCITE

H US PAT 6689629 ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE, Assignee: International Business Machines (Feb 10, 2004)

History

Direct History

=> 1 **ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE,** US PAT 6689629, 2004 WL 247094 (U.S. PTO Utility Feb 10, 2004) (NO. 10/068500)

Construed and Ruled Infringed by

H 2 LG Display Co., Ltd. v. AU Optronics Corp., --- F.Supp.2d ----, 2010 WL 545921, 2010 Markman 545921 (D.Del. Feb 16, 2010) (NO. CIV.A. 06-726-JJF, CIV.A. 07-357-JJF) (Markman Order Version)

H 3 LIQUID-CRYSTAL DISPLAY, LIQUID-CRYSTAL CONTROL CIRCUIT, FLICKER INHIBITION METHOD, AND LIQUID-CRYSTAL DRIVING METHOD, US PAT 6778160, 2004 WL 1839025 (U.S. PTO Utility Aug 17, 2004) (NO. 09/760131)

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H 5 SIGNAL TRANSMISSION DEVICE HAVING FLEXIBLE PRINTED CIRCUIT BOARDS, US PAT 7090506, 2006 WL 2358291 (U.S. PTO Utility Aug 15, 2006) (NO. 10/921462)

Construed and Ruled Infringed by

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H 7 BACKLIGHT UNIT AND LIQUID CRYSTAL DISPLAY UTILIZING THE SAME, US PAT 7125157, 2006 WL 3011617 (U.S. PTO Utility Oct 24, 2006) (NO. 10/902914)

Construed and Ruled Infringed by

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H 11 LG Display Co., Ltd. v. AU Optronics Corp., --- F.R.D. ----, 2010 WL 723673 (D.Del. Mar 02, 2010) (NO. CIV.A. 06-726-JJF, CIV.A. 07-357-JJF)

Court Documents

Trial Court Documents (U.S.A.)

D.Del. Trial Pleadings

12 LG. PHILIPS LCD CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION; AU Optronics Corporation, AU Optronics Corporation of America; Tatung Company; Tatung Company of America, Inc.; and Viewsonic Corporation, Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG.PHILIPS LCD CO., LTD and LG., 2008 WL 1995673 (Trial Pleading) (D.Del. Mar. 6, 2008) **Chi Mei Optoelectronics USA, Incanswer, Affirmative Defenses and Counterclaims to the Counterclaims of LG.Philips LCD CO., Ltd.** (NO. 106CV00726)

13 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 1995674 (Trial Pleading) (D.Del. Mar. 13, 2008) **LG Display Co., Ltd.'s Answer to Chi Mei Optoelectronics USA, Inc.'s Counterclaims and Counterclaims Asserted Against Chi Mei Optoelectronics Corporation** (NO. 106CV00726)

14 LG. DISPLAY CO., LTD, Plaintiff, v. CHI MEI OPTOELETRONICS CORPORATION; Chi Mei Optoelectronics USA, Inc.; Auo Optronics Corporation; and Au Optronics Corporation America, Defendants., 2009 WL 1347868 (Trial Pleading) (D.Del. Jan. 6, 2009) **Auo Defendants' First Amended Answer to and Counterclaim Against Plaintiff and Additional Party Lg. Display America, Inc.** (NO. 106CV00726)

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18 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680917 (Expert Report and Affidavit) (D.Del. Aug. 10, 2008) **Declaration of Dr. Pochi Yeh** (NO. 06-726, JJF)

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22 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680920 (Expert Report and Affidavit) (D.Del. Sep. 4, 2008) **Declaration of David Eccles** (NO. 06-726, JJF)

23 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680922 (Expert Report and Affidavit) (D.Del. Sep. 4, 2008) **Declaration of Dr. Allan R. Kmetz** (NO. 06-726, JJF)

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26 LG DISPLAY CO., LTD., v. AU OPTRONICS CORPORATION and Au Optronics Corporation America et al., 2009 WL 5850939 (Expert Report and Affidavit) (D.Del. Feb. 27, 2009) **Report of Expert Tsu-Jae King Liu, Ph.D. Regarding Invalidity of United States Patent Number 5,019,002** (NO. 06CV00726)

27 LG DISPLAY CO., LTD., v. AU OPTRONICS CORPORATION and Au Optronics Corporation AMerica., 2009 WL 5850940 (Expert Report and Affidavit) (D.Del. Feb. 27, 2009) **Report of Expert Regarding Invalidity of United States Patent Number 7,218,374 of Lawrence Tannas, Jr.** (NO. 06CV00726)

28 LG DISPLAY CO., LTD., v. AU OPTRONICS CORPORATION and Au Optronics Corporation

America., 2009 WL 5850941 (Expert Report and Affidavit) (D.Del. Feb. 27, 2009) **Report of Expert Webster Howard, Ph.D. Regarding Invalidity of United States Patent Numbers 5,905,274, 6,815,321, and 7,176,489** (NO. 06CV00726)

D.Del. Trial Depositions and Discovery

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D.Del. Trial Motions, Memoranda And Affidavits

31 AU OPTRONICS CORPORATION, Plaintiff, v. LG.PHILIPS LCD CO., LTD. and LG.Philips LCD America, Inc., Defendants; LG.Philips LCD Co., Ltd. and LG.Philips LCD America, Inc., Counterclaim Plaintiffs, v. AU Optronics Corporation; AU Optronics Corporation of America; Chi Mei Optoelectronics Corporation; an, 2007 WL 2933013 (Trial Motion, Memorandum and Affidavit) (D.Del. Jul. 19, 2007) **LG.Philips LCD Co., Ltd. and LG.Philips LCD America, Inc.'s Answering Brief in Opposition to Chi Mei Optoelectronics Corporation's Motion to Dismiss for Lack of Personal Jurisdiction and for Insuffici** (NO. 07-CV-357-JJF)

32 LG. PHILIPS LCD CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION; Au Optronics Corporation, Au Optronics Corporation of America; Tatung Company; Tatung Company of America, Inc.; and Viewsonic Corporation, Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG. PHILIPS LCD CO., LTD and LG, 2008 WL 1995672 (Trial Motion, Memorandum and Affidavit) (D.Del. Mar. 4, 2008) **Chi Mei Optoelectronics Corporation's Opening Brief in Support of Its Motion to Strike Plaintiff's Second ""first Amended Complaint"** (NO. 106CV00726)

33 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 1995675 (Trial Motion, Memorandum and Affidavit) (D.Del. Mar. 17, 2008) **Plaintiff's Answering Brief in Opposition to Chi Mei Optoelectronics Corporation's Motion to Strike Plaintiff's Amended Complaint** (NO. 106CV00726)

34 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION; Au Optronics Corporation, Au Optronics Corporation of America; Tatung Company; Tatung Company of America,inc.; and Viewsonic Corporation, Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD and LG Display Am, 2008 WL 1995676 (Trial Motion, Memorandum and Affidavit) (D.Del. Mar. 25, 2008) **Reply Brief of Chi Mei Optoelectronics Corporation in Support of Its Motion to Strike Plaintiff's Second ""First Amended Complaint"** (NO. 106CV00726)

35 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Cor-

poration America; Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2008 WL 6002377 (Trial Motion, Memorandum and Affidavit) (D.Del. Aug. 11, 2008) **Auo's Opening Claim Construction Brief** (NO. 106CV00726)

36 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002378 (Trial Motion, Memorandum and Affidavit) (D.Del. Aug. 11, 2008) **Memorandum In Support of Defendants Chi Mei Optoelectronics' Proposed Claim Constructions** (NO. 106CV00726)

37 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002379 (Trial Motion, Memorandum and Affidavit) (D.Del. Aug. 12, 2008) **Opening Claim Construction Brief of Plaintiff LG Display Co., Ltd.** (NO. 106CV00726)

38 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2008 WL 6002380 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Auo's Response To Lgd's Claim Construction Briefing On Auo's Patents** (NO. 106CV00726)

39 LG DISPLAY CO., Ltd., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; CHI, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2008 WL 6002381 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Auo's Responsive Claim Construction Brief for Lg Display's Patents** (NO. 106CV00726)

40 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002382 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Response of Plaintiff Lg Display Co., Ltd. To Auo's Opening Claim Construction Brief** (NO. 106CV00726)

41 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002383 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Response of Plaintiff Lg Display Co., Ltd. To Cmo's Opening Claim Construction Brief** (NO. 106CV00726)

42 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002384 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Chi Mei Optoelectronics' Answering Memorandum Regarding Proposed Claim Constructions** (NO. 106CV00726)

43 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002385 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 10, 2008) **Plaintiff LG Display Co., Ltd.'s Brief in Support of its Motion to Strike AU Optronics Corporation's Claim Construction Briefs** (NO. 106CV00726)

44 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6137427 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 10, 2008) **Plaintiff Lg Display Co., Ltd.'s Brief in Support of Its Motion to Strike Chi Mei Opto-**

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45 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002386 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 29, 2008) **Defendants Chi Mei Optoelectronics' Answering Brief In Opposition To Plaintiff LG Display's Motion to Strike Claim Construction Briefs** (NO. 106CV00726)

46 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002387 (Trial Motion, Memorandum and Affidavit) (D.Del. Oct. 8, 2008) **Plaintiff LG Display Co., Ltd.'s Reply Brief In Support of its Motion to Strike CMO's Claim Construction Briefs** (NO. 106CV00726)

47 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendats., 2009 WL 1347872 (Trial Motion, Memorandum and Affidavit) (D.Del. Jan. 20, 2009) **Plaintiff Lg Display's Opening Brief in Support of its Motion to Compel Au Optronics Corporation and Chi Mei Optoelectronics Corporation to Provide Knowledgeable Deposition Witnesses and for Entry of** (NO. 106CV00726)

48 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 1347876 (Trial Motion, Memorandum and Affidavit) (D.Del. Feb. 6, 2009) **Defendant Au Optronics Corporation's Answering Brief in Opposition to Plaintiff Lg Display Co., Ltd.'s Motion to Compel Auo to Provide Knowledgeable Deposition Witnesses and for Entry of Protective Or** (NO. 106CV00726)

49 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi Mei Optoelectronics Corporation, and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 1347859 (Trial Motion, Memorandum and Affidavit) (D.Del. Feb. 17, 2009) **Defendant AU Optronics Corporation's Corrected Answering Brief in Opposition to Plaintiff's Motion to Strike Advice of Counsel Defense or in the Alternative, to Compel Production of Documents, Witness** (NO. 106CV00726)

50 LG DISPLAY CO., LTD., Plaintiff, v. AU OPIRONICS CORPORATION; AU Optronics Corporation America; Chi Mei Optoelectronics Corporation, and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 1347866 (Trial Motion, Memorandum and Affidavit) (D.Del. Feb. 17, 2009) **Defendant AU Optronics Corporation's Answering Brief in Opposition to Plaintiff Lg Display Co., Ltd.'s Motion to Compel Additional Correlation Charts, Technical Documents, and Damages Discovery** (NO. 106CV00726)

51 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants. CHI MEI OPTOELECTRONICS CORPORATION and Chi Mei Optoelectronics USA, Inc., Plaintiffs, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 3242274 (Trial Motion, Memorandum and Affidavit) (D.Del. May 1, 2009) **Chi Mei Optoelectronics' Motion in Limine No.2 to Preclude Lg Display from Presenting Evidence or Argument Regarding Findings of Infringment or Validity from Prior Litigation** (NO. 106CV00726)

52 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA,

Inc., Defendants., 2009 WL 3242275 (Trial Motion, Memorandum and Affidavit) (D.Del. May 8, 2009) **Auo's Opening Brief in Support of Its Motion for Summary Judgment of Unenforeability of Claim 1 of Lgd's 449 Patent** (NO. 106CV00726)

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54 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants. CHI MEI OPTOELECTRONICS CORPORATION and CHI Mei Optoelectronics USA, Inc., Plaintiffs, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 3242277 (Trial Motion, Memorandum and Affidavit) (D.Del. May 8, 2009) **Chi Mei Optoelectronics' Motion in Limine No. 4 to Exclude Testimony By Lgd's Expert Witness Arthur Cobb Due to Failure to Comply with the Requirements of FRCP 26** (NO. 106CV00726)

55 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTONICS CORPORATION, et al., Defendants. CHI MEI OPTOELECTRONICS CORPORATION and Chi Mei Optoelectronics USA, Inc., Plaintiffs, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 3242278 (Trial Motion, Memorandum and Affidavit) (D.Del. May 8, 2009) **Chi Mei Optoelectronics' Motion in Limine No. 5 to Preclude Lg Display from Presenting Evidence or Argument Regarding the Supplemental Expert Report of Dr. Elliott Schlam and to Strike the Report** (NO. 106CV00726)

56 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants. CHI MEI OPTOELECTRONICS CORPORATION and Chi Mei Optoelectronics USA, Inc., Plaintiffs, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 3242279 (Trial Motion, Memorandum and Affidavit) (D.Del. May 8, 2009) **Chi Mei Optoelectronics' Motion in Limine No.6 to Preclude Lg Display Form Presenting Evidence or Argument Regarding the Rebuttal Expert Reports of Dr. Elliott Schlam and to Strike the Reports** (NO. 106CV00726)

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61 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3242284 (Trial Motion, Memorandum and Affidavit) (D.Del. May 12, 2009) **Plaintiff LG Display Company Ltd.'s Reply Breif in Support of Its Motion to Strike or Preclude Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA, Inc. From Asserting an Advice of Cou** (NO. 106CV00726)

62 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3242285 (Trial Motion, Memorandum and Affidavit) (D.Del. May 12, 2009) **LG Display Co., Ltd.'s Reply Brief in Support of Its Motion to Compel Auo to Provide Knowledgeable Witnesses on Key Inducement and Damages Deposition Topics** (NO. 106CV00726)

63 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORAION, et al., Defendants., 2009 WL 3242286 (Trial Motion, Memorandum and Affidavit) (D.Del. May 13, 2009) **LG Display Co., Ltd.'s Opposition to AUO's Motion to Supplement Briefing of Its Motion to Preclude LG Display's Reliance On Invalidating Prior Art** (NO. 106CV00726)

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66 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245830 (Trial Motion, Memorandum and Affidavit) (D.Del. May 21, 2009) **Au Optronicss' Motion in Limine No.2 to Preclude Any Reference to the Prior Cpt Litigations** (NO. 106CV00726)

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poration America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245831 (Trial Motion, Memorandum and Affidavit) (D.Del. May 21, 2009) **Au Optronics' Motion in Limine No.3 to Preclude Any Testimony from the Prior CPT Litigations, Including Reliance by Experts on the Prior Testimony of Expert Michael Keeley in the California CPT Litiga** (NO. 106CV00726)

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69 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245833 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **Au Optronics' Motion in Limine No.5 to Preclude Lg Display from Introducing Any Evidence Regarding Yield Percentage and to Preclude Mr. Cobb from Offering Any Opinions Based Upon Yield Improvements** (NO. 106CV00726)

70 LG DISPLAY COMPANY, LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245834 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **LG Display Co., Ltd.'s Motion in Limine No. 1 to Preclude Joyce Pan and James Chen from Testifying at Trial because They Were not Timely Identified by AU Optronics Corporation** (NO. 106CV00726)

71 LG DISPLAY COMPANY, LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245835 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **Lg Display Co., Ltd.'s Motion in Limine No. 2 to Preclude Auo's Experts from Asserting Prior Art Against Lg Display's Patents that They Did not Address in Their Expert Reports** (NO. 106CV00726)

72 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORP., et al., Defendants., 2009 WL 3245836 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **LG Display Co., Ltd's Motion Inlimine No. 4 to Preclude the Introduction of Testimony from the Depostion of Third Party Catalyst Sales, Inc. Prior to Appearance At the Deposition By All Counsel** (NO. 106CV00726)

73 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245837 (Trial Motion, Memorandum and Affidavit) (D.Del. May 22, 2009) **Lg Display Co., Ltd.'s Motion in Limine No. 3 to Preclude Auo from Offering Evidence Regarding Advice of Counsel** (NO. 106CV00726)

74 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245838 (Trial Motion, Memorandum and Affidavit) (D.Del. May 28, 2009) **Lg Display Co., Ltd.'s Opposition to Auo's ""Addendum" to Its Motion Limine No. 7** (NO. 106CV00726)

75 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245839 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 5,

2009) **Auo's Opposition to Lgd's Motion in Limine to Preclude Auo from Introducing Live Testimony from Mr. Kuang-Tao (""Surf") Sung or Other Evidence Allegedly Showing Dates of Conception and Reduction to P** (NO. 106CV00726)

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77 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245841 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 8, 2009) **Au Optronics' Response to Lg Display Co. Ltd.'s Motion in Limine No.5 to Preclude Introduction of Evidence or Opinion Testimony Concerning Electro-Static Discharge Repairs and Repair Costs** (NO. 106CV00726)

78 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 3245842 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 8, 2009) **Au Optronics' Response to Lg Display Co. Ltd.'s Motion in Limine No. 3** (NO. 106CV00726)

79 LG DISPLAY COMPANY, LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245843 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Motion in Limine No.5 to Preclude Auo from Introducing Evidence or Opinion Testimony Concerning Purported Electro-Static Discharge Repairs and Repair Costs** (NO. 106CV00726)

80 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245844 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Memorandum in Opposition to Auo's Motion in Limine No. 5** (NO. 106CV00726)

81 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORP., et al., Defendants., 2009 WL 3245845 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **Lg Display Co., Ltd.'s Opposition to Au Optronics Corporation's Motion in Limine No.6 to Preclude Lgd from Relying On Certain Defenses and Evidence that Lgd Failed to Disclose During Discovery** (NO. 106CV00726)

82 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245846 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Memorandum in Opposition to Auo's Motion in Limine No. 4 to Preclude Any Testimony from the Prior CPT Litigations, Including Reliance By Experts On the Prior Testimony of Dr. Ho** (NO. 106CV00726)

83 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245847 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Memorandum in Opposition to Auo's Motion in Limine No. 1** (NO. 106CV00726)

84 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245848 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **Lg Display Co., Ltd.'s Memorandum in Opposition to Auo's Motion in Limine No. 2 to Preclude Any Reference to the Prior Cpt Litigations** (NO. 106CV00726)

85 LG DISPLAY COMPANY, LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2009 WL 3245849 (Trial Motion, Memorandum and Affidavit) (D.Del. Jun. 12, 2009) **LG Display Co., Ltd.'s Motion in Limine to Preclude AU Optronics Corporation from Introducing Live Testimony from Mr. Kuang-Tao (""Surf") Sung or Other Evidence Allegedly Showing Dates of Conception** (NO. 106CV00726)

D.Del.

86 John D. Villasenor, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6877461 (Court-filed Expert Resume) (D.Del. Aug. 12, 2008) **Expert Resume of John D. V** (NO. 106CV00726)

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88 Miltiadis K. Hatalis, curriculum vitae filed in LG,Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6889167 (Court-filed Expert Resume) (D.Del. Aug. 12, 2008) **Expert Resume of Miltiadis K. Hatalis** (NO. 106CV00726)

89 David A. Eccles, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6877462 (Court-filed Expert Resume) (D.Del. Sep. 4, 2008) **Expert Resume of David A. Eccles** (NO. 106CV00726)

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91 George M. Pharr, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6882352 (Court-filed Expert Resume) (D.Del. Sep. 4, 2008) **Expert Resume of George M. Pharr** (NO. 106CV00726)

D.Del. Trial Filings

92 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159025 (Trial Filing) (D.Del. Jul. 29, 2008) **Claim Construction Chart** (NO. 06CV00726)

93 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159026 (Trial Filing) (D.Del. Jul. 29, 2008) **Claim Construction Chart** (NO. 06CV00726)

94 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159027 (Trial Filing) (D.Del. Jul. 29, 2008) **Claim Construction Chart** (NO. 06CV00726)

95 LG PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159028 (Trial Filing) (D.Del. Jul. 29, 2008) **Claim Construction Chart** (NO. 06CV00726)

96 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159029 (Trial Filing) (D.Del. Jul. 29, 2008) **Claim Construction Chart** (NO. 06CV00726)

97 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008

WL 6159030 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

98 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159031 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

99 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159032 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

100 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159033 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

101 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159034 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

102 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159035 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

103 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159036 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

104 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159037 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

105 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159038 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

106 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159039 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

107 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159040 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

108 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159041 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

109 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159042 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

110 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159043 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

111 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159044 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

112 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159045 (Trial Filing) (D.Del. Aug. 6, 2008) **Claim Construction Chart** (NO. 06CV00726)

113 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159046 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit B LG Display USP 5,019,002** (NO. 06CV00726)

114 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159047 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit C LG Display USP 5,825,449** (NO. 06CV00726)

115 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159048 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit D LG Display USP 6,664,569** (NO. 06CV00726)

116 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008

WL 6159049 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit E LG Display USP 6,803,984** (NO. 06CV00726)

117 LG.PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159050 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit F LG Display USP 5,905,274** (NO. 06CV00726)

118 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159051 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit G LG Display USP 6,815,321** (NO. 06CV00726)

119 LG. PHILIPS LCD CO. LTD., v. CHI MEI OPTOELECTRONICS CORPORATION et al., 2008 WL 6159052 (Trial Filing) (D.Del. Aug. 6, 2008) **Joint Claim Construction Statement - Exhibit H LG Display USP 7,176,489** (NO. 06CV00726)

Dockets (U.S.A.)

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120 LG.PHILIPS LCD CO. LTD. v. CHI MEI OPTOELECTRONICS CORPORATION ET AL, NO. 1:06cv00726 (Docket) (D.Del. Dec. 1, 2006)

121 AU OPTRONICS CORPORATION v. LG.PHILIPS LCD CO. LTD. ET AL, NO. 1:07cv00357 (Docket) (D.Del. Jun. 6, 2007)

Expert Court Documents (U.S.A.)

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122 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680917 (Expert Report and Affidavit) (D.Del. Aug. 10, 2008) **Declaration of Dr. Pochi Yeh** (NO. 06-726, JJF)

123 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680918 (Expert Report and Affidavit) (D.Del. Aug. 10, 2008) **Declaration of Dr. John D. Villasenor in Support of Cmo's Opening Brief on Claim Construction** (NO. 06-726, JJF)

124 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680919 (Expert Report and Affidavit) (D.Del. Aug. 11, 2008) **Declaration of Dr. Miltiadis Hatalis in Support of Defendants Chi Mei Optoelectronics' Proposed Claim Constructions** (NO. 06-726, JJF)

125 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680921 (Expert Report and Affidavit) (D.Del. Aug. 29, 2008) **Declaration of Dr. George M. Pharr** (NO. 06-726, JJF)

126 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680920 (Expert Report and Affidavit) (D.Del. Sep. 4, 2008) **Declaration of David Eccles** (NO. 06-726, JJF)

127 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al.,

Defendants., 2008 WL 5680922 (Expert Report and Affidavit) (D.Del. Sep. 4, 2008) **Declaration of Dr. Allan R. Kmetz** (NO. 06-726, JJF)

128 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 5680923 (Expert Report and Affidavit) (D.Del. Sep. 4, 2008) **Declaration of Dr. Pochi Yeh in Support of Responsive Brief** (NO. 06-726, JJF)

129 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants; Au Optronics Corporation, Plaintiff, v. LG Display Co., Ltd. and LG Display America, Inc., Defendants., 2008 WL 7505544 (Expert Report and Affidavit) (D.Del. Oct. 31, 2008) **Supplemental Declaration of Aris K. Silzars in Support of Au Optronics' Reply Brief in Support of Its Motion to Compel LGD to Produce Complete GDS Files** (NO. 06-726-JJF, 07-357-JJF)

130 LG DISPLAY CO., LTD., v. AU OPTRONICS CORPORATION and Au Optronics Corporation America et al., 2009 WL 5850939 (Expert Report and Affidavit) (D.Del. Feb. 27, 2009) **Report of Expert Tsu-Jae King Liu, Ph.D. Regarding Invalidity of United States Patent Number 5,019,002** (NO. 06CV00726)

131 LG DISPLAY CO., LTD., v. AU OPTRONICS CORPORATION and Au Optronics Corporation AMerica., 2009 WL 5850940 (Expert Report and Affidavit) (D.Del. Feb. 27, 2009) **Report of Expert Regarding Invalidity of United States Patent Number 7,218,374 of Lawrence Tannas, Jr.** (NO. 06CV00726)

132 LG DISPLAY CO., LTD., v. AU OPTRONICS CORPORATION and Au Optronics Corporation America., 2009 WL 5850941 (Expert Report and Affidavit) (D.Del. Feb. 27, 2009) **Report of Expert Webster Howard, Ph.D. Regarding Invalidity of United States Patent Numbers 5,905,274, 6,815,321, and 7,176,489** (NO. 06CV00726)

D.Del. Trial Motions, Memoranda And Affidavits

133 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002378 (Trial Motion, Memorandum and Affidavit) (D.Del. Aug. 11, 2008) **Memorandum In Support of Defendants Chi Mei Optoelectronics' Proposed Claim Constructions** (NO. 106CV00726)

134 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2008 WL 6002380 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Auo's Response To Lgd's Claim Construction Briefing On Auo's Patents** (NO. 106CV00726)

135 LG DISPLAY CO., Ltd., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; CHI, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2008 WL 6002381 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Auo's Responsive Claim Construction Brief for Lg Display's Patents** (NO. 106CV00726)

136 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al.,

Defendants., 2008 WL 6002382 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Response of Plaintiff Lg Display Co., Ltd. To Auo's Opening Claim Construction Brief** (NO. 106CV00726)

137 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002383 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Response of Plaintiff Lg Display Co., Ltd. To Cmo's Opening Claim Construction Brief** (NO. 106CV00726)

138 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002384 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 4, 2008) **Chi Mei Optoelectronics' Answering Memorandum Regarding Proposed Claim Constructions** (NO. 106CV00726)

139 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6002385 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 10, 2008) **Plaintiff LG Display Co., Ltd.'s Brief in Support of its Motion to Strike AU Optronics Corporation's Claim Construction Briefs** (NO. 106CV00726)

140 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendants., 2008 WL 6137427 (Trial Motion, Memorandum and Affidavit) (D.Del. Sep. 10, 2008) **Plaintiff Lg Display Co., Ltd.'s Brief in Support of Its Motion to Strike Chi Mei Optoelectronics Corporation's Claim Construction Briefs** (NO. 06-726, JJF)

141 LG DISPLAY CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION, et al., Defendats., 2009 WL 1347872 (Trial Motion, Memorandum and Affidavit) (D.Del. Jan. 20, 2009) **Plaintiff Lg Display's Opening Brief in Support of its Motion to Compel Au Optronics Corporation and Chi Mei Optoelectronics Corporation to Provide Knowledgeable Deposition Witnesses and for Entry of** (NO. 106CV00726)

142 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; Au Optronics Corporation America; Chi, Mei Optoelectronics Corporation; and Chi Mei Optoelectronics USA, Inc., Defendants., 2009 WL 1347876 (Trial Motion, Memorandum and Affidavit) (D.Del. Feb. 6, 2009) **Defendant Au Optronics Corporation's Answering Brief in Opposition to Plaintiff Lg Display Co., Ltd.'s Motion to Compel Auo to Provide Knowledgeable Deposition Witnesses and for Entry of Protective Or** (NO. 106CV00726)

143 LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU Optronics Corporation America; Chi Mei Optoelectronics Corporation, and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 1347859 (Trial Motion, Memorandum and Affidavit) (D.Del. Feb. 17, 2009) **Defendant AU Optronics Corporation's Corrected Answering Brief in Opposition to Plaintiff's Motion to Strike Advice of Counsel Defense or in the Alternative, to Compel Production of Documents, Witness** (NO. 106CV00726)

144 LG DISPLAY CO., LTD., Plaintiff, v. AU OPIRONICS CORPORATION; AU Optronics Corporation America; Chi Mei Optoelectronics Corporation, and Chi Mei Optoelectronics USA, Inc., Defendants. AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG Display America, Inc., Defendants., 2009 WL 1347866 (Trial Motion, Memorandum and Affidavit) (D.Del. Feb. 17, 2009) **Defendant AU Optronics Corporation's Answering Brief in Opposition to Plaintiff Lg Display Co., Ltd.'s Motion to Compel Additional Correlation**

Charts, Technical Documents, and Damages Discovery (NO. 106CV00726)

D.Del.

145 John D. Villasenor, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6877461 (Court-filed Expert Resume) (D.Del. Aug. 12, 2008) **Expert Resume of John D. V** (NO. 106CV00726)

146 Pochi Yeh, curriculum vitae filed in LG. Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6889166 (Court-filed Expert Resume) (D.Del. Aug. 12, 2008) **Expert Resume of Pochi Yeh** (NO. 106CV00726)

147 Miltiadis K. Hatalis, curriculum vitae filed in LG,Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6889167 (Court-filed Expert Resume) (D.Del. Aug. 12, 2008) **Expert Resume of Miltiadis K. Hatalis** (NO. 106CV00726)

148 David A. Eccles, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6877462 (Court-filed Expert Resume) (D.Del. Sep. 4, 2008) **Expert Resume of David A. Eccles** (NO. 106CV00726)

149 Allan R. Kmetz, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6877463 (Court-filed Expert Resume) (D.Del. Sep. 4, 2008) **Expert Resume of Allan R. Kmetz** (NO. 106CV00726)

150 George M. Pharr, curriculum vitae filed in LG.Philips LCD Co. Ltd. v. Chi Mei Optoelectronics Corporation et al, 2008 WL 6882352 (Court-filed Expert Resume) (D.Del. Sep. 4, 2008) **Expert Resume of George M. Pharr** (NO. 106CV00726)

D.Del.

151 AU OPTRONICS CORPORATION v. LG.PHILIPS LCD CO. LTD. ET AL, NO. 1:07cv00357 (Docket) (D.Del. Jun. 6, 2007)

Patent Family

152 ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY, INCLUDES DUMMY CONDUCTIVE PATTERNS ARRANGED BETWEEN CONNECTION PADS AND PIXEL ELECTRODES, Derwent World Patents Legal 2002-674166

Assignments

153 Action: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS). Number of Pages: 008, (DATE RECORDED: May 18, 2007)

154 Action: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS). Number of Pages: 017, (DATE RECORDED: Dec 21, 2005)

Docket Summaries

155 AU OPTRONICS CORPORATION v. LG.PHILIPS LCD CO. LTD. ET AL, (D.DEL. Jun 06, 2007) (NO. 1:07CV00357), (35 USC 271 PATENT INFRINGEMENT)

156 AU OPTRONICS CORPORATION v. LG.PHILIPS LCD CO., LTD., (W.D.WIS. Mar 08, 2007)

(NO. 3:07C00137), (PROPERTY RIGHTS; PATENT)

Prior Art (Coverage Begins 1976)

C 157 LIQUID CRYSTAL DISPLAY DEVICE HAVING PERIPHERAL DUMMY LINES, US PAT 5285301Assignee: Hitachi, Ltd., (U.S. PTO Utility 1994)

C 158 LIQUID CRYSTAL DISPLAY WITH ENHANCED GATE PAD PROTECTION AND METHOD OF MANUFACTURING THE SAME, US PAT 6163356Assignee: LG Electronics, (U.S. PTO Utility 2000)

Click a docket number below to view a docket.

Patent Search Results

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Items 1 to 2 of 2

	Patent	Class	Subclass	Description	Court (All)	Docket Number	Filed	Date Retrieved
☐	6,689,629	438	25	AU Optronics Corporation v. Lg.philips LCD Co Ltd et al	US-DIS-DED	1:07cv357	6/6/2007	2/19/2010
☐	6,689,629	438	25	AU Optronics Corporation v. Lg.philips LCD Co, Ltd	US-DIS-WIWD	1:07cv137	3/8/2007	11/5/2009

Items 1 to 2 of 2

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US District Court Civil Docket

U.S. District - Delaware
(Wilmington)

1:07cv357

Au Optronics Corporation v. Lg.Philips Lcd Co Ltd et al

This case was retrieved from the court on Friday, February 19, 2010

Date Filed:	**06/06/2007**	**Class Code:**	
Assigned To:	**Judge Joseph J Farnan, Jr**	**Closed:**	**No**
Referred To:		**Statute:**	**35:271**
Nature of suit:	**Patent (830)**	**Jury Demand:**	**Defendant**
Cause:	**Patent Infringement**	**Demand Amount:**	**$0**
Lead Docket:	**1:06-cv-00726-JJF**	**NOS Description:**	**Patent**
Other Docket:	**1:06-cv-00726-JJF** **1:08-cv-00355**		
Jurisdiction:	**Federal Question**		

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Date	#	Proceeding Text
06/06/2007	49	Record of case transferred in from District of Wisconsin(Western); Case Number in Other District: 07-C-137. Copy of Docket Sheet and original file with documents numbered 1-49 attached. (Attachments: # 1 DI #1# 2 DI #2# 3 Exhibit A to DI #2# 4 Exhibit B to DI #2# 5 Exhibit C to DI #2# 6 DI #3# 7 DI #4# 8 DI #5# 9 DI #6# 10 DI #7# 11 DI #8# 12 DI #9# 13 DI #10# 14 DI #11# 15 DI #12# 16 DI #13# 17 DI #14# 18 DI #15# 19 DI #16# 20 DI #17# 21 DI #18# 22 DI #19# 23 DI #20# 24 DI #21# 25 DI #22# 26 DI #23# 27 DI #24- SEALED DOCUMENT# 28 DI #25# 29 DI #26# 30 DI #27# 31 DI #28# 32 DI #29# 33 Exhibit A to DI #29# 34 Exhibit B to DI #29# 35 Exhibit C to DI #29# 36 Exhibit D to DI #29# 37 Exhibit E to DI #29# 38 DI #30# 39 DI #31# 40 DI #32- SEALED DOCUMENT# 41 DI #33# 42 DI #34# 43 DI #35# 44 DI #36# 45 DI #37# 46 DI #38# 47 DI #39# 48 Exhibit A to DI #39# 49 DI #40# 50 DI #41# 51 DI #42# 52 DI #43# 53 DI #44# 54 DI #45# 55 DI #46# 56 Exhibit A to DI #46# 57 Exhibit B to DI #46# 58 DI #47# 59 DI #48# 60 DI #49)(ead) (Entered: 06/08/2007)
06/06/2007	--	Order granting Motion To Transfer matter to U.S. District Court for the District of Delaware, signed by Judge Shabaz on 5/30/07 in U.S.D.C., Wisconsin(Western) - DI # in other district: 49. (ead) (Entered: 06/08/2007)
06/06/2007	50	COMPLAINT filed against LG.Philips LCD Co. Ltd., LG.Philips LCD America - - filed by AU Optronics Corporation. (Filed in USDC/WD/WI on 3/8/07 as DI #2)(Attachments: # 1 Civil Cover Sheet)(ead) (Entered: 06/08/2007)
06/06/2007	51	MOTION to Dismiss for Improper Venue - filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 3/29/07 as DI #6) (ead) (Entered: 06/08/2007)
06/06/2007	52	OPENING BRIEF in Support re 51 MOTION to Dismiss for Improper Venue filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 3/29/07 as DI #7) (ead) (Entered: 06/08/2007)
06/06/2007	53	AFFIDAVIT of Dong Hoon Han- filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 3/29/07 as DI #8) (ead) (Entered: 06/08/2007)
06/06/2007	54	ANSWERING BRIEF in Opposition re 51 MOTION to Dismiss for Improper Venue filed by AU Optronics Corporation. (Filed in USDC/WD/WI on 4/18/07 as DI #27) (ead) (Entered: 06/08/2007)
06/06/2007	55	REPLY BRIEF re 51 MOTION to Dismiss for Improper Venue filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 4/30/07 as DI #31)(ead) (Entered: 06/08/2007)
06/06/2007	56	REPLY BRIEF re 51 MOTION to Dismiss for Improper Venue filed by LG.Philips LCD America. CORRECTED (Filed in USDC/WD/WI on 5/3/07 as DI #36) (ead) (Entered: 06/08/2007)
06/06/2007	57	MOTION to Compel LG.Philips LCD America to Respond to Requests for Production and Interrogatories and for Other Relief - filed by AU Optronics Corporation. (Filed in USDC/WD/WI on 5/18/07 as DI #41) (ead) (Entered: 06/08/2007)
06/06/2007	58	OPENING BRIEF in Support re 57 MOTION to Compel filed by AU Optronics Corporation. (Filed in USDC/WD/WI on 5/18/07 as DI #42) (ead) (Entered: 06/08/2007)
06/06/2007	59	AFFIDAVIT of James R. Troupis re 57 MOTION to Compel filed by AU Optronics Corporation. (Filed in USDC/WD/WI on 5/18/07 as DI #43) (ead) (Entered: 06/08/2007)
06/06/2007	60	AFFIDAVIT of David W. Panneck re 57 MOTION to Compel filed by AU Optronics Corporation. (Attachments: # 1 Notice of Filing of Papaer Documents- Exhibits A-G) (Filed in USDC/WD/WI on 5/18/07 as DI #44)(ead) (Entered: 06/08/2007)
06/06/2007	61	ANSWERING BRIEF in Opposition re 57 MOTION to Compel filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 5/22/07 as DI #45) (ead) (Entered: 06/08/2007)
06/06/2007	62	AFFIDAVIT of Nicole Talbott Settle re 61 Answering Brief in Opposition filed by LG.Philips LCD America. (Filed in USDC/WD/WI on 5/22/07 as DI #46) (ead) (Entered: 06/08/2007)
06/06/2007	63	NOTICE of filing the following document(s) in paper format: Exhibits A-T to Declaration of David W. Panneck (DI #28 Filed in USDC/WD/WI on 4/18/07)). Original document(s) on file in Clerk's Office. Notice filed by AU Optronics Corporation. (ead) (Entered: 06/08/2007)

06/06/2007	64	NOTICE of filing the following document(s) in paper format: Exhibits A-W to Declaration of Paul Barbato. (DI #38 Filed in USDC/WD/WI on 5/7/07) Original document(s) on file in Clerk's Office. Notice filed by AU Optronics Corporation. (ead) (Entered: 06/08/2007)
06/06/2007	65	NOTICE of filing the following document(s) in paper format: Exhibits A-G to Declaration of David W. Panneck. (Filed as DI #44 in USDC/WD/WI on 5/18/07) Original document(s) on file in Clerk's Office. Notice filed by AU Optronics Corporation (ead) (Entered: 06/08/2007)
06/08/2007	66	Local Counsel Letter sent to James D. Peterson.Notice of Compliance deadline set for 7/12/2007. (ead) (Entered: 06/08/2007)
06/08/2007	67	Local Counsel Letter sent to James P. Troupis. Notice of Compliance deadline set for 7/12/2007. (ead) (Entered: 06/08/2007)
06/08/2007	68	Report to the Commissioner of Patents and Trademarks for Patent/Trademark Number(s) 6,689,629; 6,976,781; 6,778,160; (ead) (Entered: 06/08/2007)
06/08/2007	69	SEALED AFFIDAVIT of R. Tyler Goodwyn in Support of LG.Philips LCD Co. Ltd's Motion to Transfer to the District of Delaware filed by LG.Philips LCD Co. Ltd. (Filed in USDC/WD/WI on 4/16/07 as DI #24) (ead) (Entered: 06/08/2007)
06/08/2007	70	SEALED AFFIDAVIT of Dong Hoon Han in Support of LG.Philips LCD America's Motion to Dismiss re 51 MOTION to Dismiss for Improper Venue filed by LG.Philips LCD America. (ead) (Entered: 06/08/2007)
06/08/2007	71	NOTICE of Appearance by Richard D. Kirk on behalf of LG.Philips LCD Co. Ltd., LG.Philips LCD America (Kirk, Richard) (Entered: 06/08/2007)
06/11/2007	72	ANSWER to Complaint with Jury Demand, COUNTERCLAIM against AU Optronics Corporation by LG.Philips LCD America. (Attachments: # 1 Certificate of Service)(Kirk, Richard) (Entered: 06/11/2007)
06/11/2007	73	ANSWER to Complaint with Jury Demand, COUNTERCLAIM against AU Optronics Corporation America, Chi Mei Optoelectronics Corporation, CHI MEI OPTOELECTRONICS USA, INC., AU Optronics Corporation by LG.Philips LCD Co. Ltd.. (Attachments: # 1 Exhibit A# 2 Exhibit B# 3 Exhibit C# 4 Certificate of Service)(Kirk, Richard) (Entered: 06/11/2007)
06/12/2007	74	PRAECIPE filed by Richard D. Kirk on behalf of LG.Philips LCD Co. Ltd. requesting Clerk to issue Summonses (Attachments: # 1 Certifidate of Service)(Kirk, Richard) (Entered: 06/12/2007)
06/12/2007	--	Summons Issued as to AU Optronics Corporation America on 6/12/2007; CHI MEI OPTOELECTRONICS USA, INC. on 6/12/2007. (eew) (Entered: 06/12/2007)
06/13/2007	--	Summons Issued as to Chi Mei Optoelectronics Corporation on 6/13/2007. (eew) (Entered: 06/13/2007)
06/14/2007	75	Return of Service Executed by LG.Philips LCD Co. Ltd.. CHI MEI OPTOELECTRONICS USA, INC. served on 6/12/2007, answer due 7/2/2007. (Kirk, Richard) (Entered: 06/14/2007)
06/14/2007	76	NOTICE OF SERVICE OF ANSWER TO COMPLAINT WITH COUNTERCLAIMS ON DEFENDANT CHI MEI OPTOELECTRONICS CORPORATION PURSUANT TO 10 DEL.C. SECTION 3104 by LG.Philips LCD Co. Ltd. (Kirk, Richard) (Entered: 06/14/2007)
06/14/2007	77	NOTICE OF SERVICE OF ANSWER TO COMPLAINT WITH COUNTERCLAIMS ON DEFENDANT AU OPTRONICS CORPORATION AMERICA A/K/A AU OPTRONICS AMERICA, INC. PURSUANT TO 10 DEL.C.SECTION 3104 by LG.Philips LCD Co. Ltd. (Kirk, Richard) (Entered: 06/14/2007)
06/18/2007	78	NOTICE of Appearance by Ashley Blake Stitzer on behalf of LG.Philips LCD Co. Ltd., LG.Philips LCD America (Stitzer, Ashley) (Entered: 06/18/2007)
06/18/2007	79	NOTICE OF SERVICE of LG. PHILIPS LCD'S OBJECTIONS TO AU OPTRONICS CORPORATION'S SECOND SET OF INTERROGATORIES (NO. 17) by LG.Philips LCD Co. Ltd..(Stitzer, Ashley) (Entered: 06/18/2007)
06/21/2007	80	ANSWER to Counterclaim, COUNTERCLAIM against LG.Philips LCD Co. Ltd. by AU Optronics Corporation America.(Pascale, Karen) (Entered: 06/21/2007)
06/21/2007	81	ANSWER to Counterclaim of LG.Philips LCD Co., LTD. , COUNTERCLAIM against LG.Philips LCD Co. Ltd. by AU Optronics Corporation. (Attachments: # 1 Exhibit A-C)(Pascale, Karen) (Entered: 06/21/2007)
06/21/2007	82	ANSWER to Counterclaim of LG.Philips LCD America, Inc. , COUNTERCLAIM against LG.Philips LCD America by AU Optronics Corporation. (Attachments: # 1 Exhibit A-C)(Pascale, Karen) (Entered: 06/21/2007)
06/26/2007	83	Joint MOTION to Consolidate Cases - filed by AU Optronics Corporation America, AU Optronics Corporation, LG.Philips LCD Co. Ltd., LG.Philips LCD America. (Attachments: # 1 Text of Proposed Order Of Consolidation# 2 Certificate of Compliance Local Rule 7.1.1 Statement)(Pascale, Karen) (Entered: 06/26/2007)
06/26/2007	84	NOTICE of Joint Motion To Consolidate by AU Optronics Corporation America, AU Optronics Corporation, LG.Philips LCD Co. Ltd., LG.Philips LCD America re 83 MOTION to Consolidate Cases (Pascale, Karen) (Entered: 06/26/2007)
06/26/2007	85	Joint STATEMENT re 83 MOTION to Consolidate Cases, 84 Notice (Other) Following Transfer Pursuant To Local Rule 81.2 by AU Optronics Corporation, LG.Philips LCD Co. Ltd., LG.Philips LCD America. (Pascale, Karen) (Entered: 06/26/2007)
06/29/2007	86	NOTICE OF SERVICE of LG.PHILIPS LCD CO., LTD.'S OBJECTIONS TO AU OPTRONICS CORPORATION'S SECOND SET OF DOCUMENTS REQUESTS (NOS. 143-152) by LG.Philips LCD Co. Ltd..(Stitzer, Ashley) (Entered: 06/29/2007)
07/02/2007	87	ANSWER to Counterclaim, COUNTERCLAIM CHI MEI OPTOELECTRONICS USA, INC.'S ANSWER, AFFIRMATIVE DEFENSES AND COUNTERCLAIMS TO THE COUNTERCLAIMS OF LG. PHILIPS LCD CO., LTD. against LG.Philips

		LCD Co. Ltd. by CHI MEI OPTOELECTRONICS USA, INC..(Rovner, Philip) (Entered: 07/02/2007)
07/03/2007	88	MOTION for Pro Hac Vice Appearance of Attorney M. Craig Tyler, Brian D. Range and Julie M. Holloway - filed by AU Optronics Corporation America, AU Optronics Corporation. (Pascale, Karen) (Entered: 07/03/2007)
07/05/2007	89	MOTION to Dismiss for Lack of Jurisdiction Over the Person, MOTION to Dismiss for Insufficiency of Service of Process - filed by Chi Mei Optoelectronics Corporation. (Rovner, Philip) (Entered: 07/05/2007)
07/05/2007	--	Set Briefing Schedule: re 89 MOTION to Dismiss for Lack of Jurisdiction Over the Person MOTION to Dismiss for Insufficiency of Service of Process. Answering Brief due 7/23/2007. (lec) (Entered: 07/06/2007)
07/06/2007	90	Joint MOTION to Consolidate Cases - filed by LG. Philips LCD America, Inc., AU Optronics Corporation America, AU Optronics Corporation, LG.Philips LCD Co. Ltd.. (Pascale, Karen) (Entered: 07/06/2007)
07/06/2007	91	Joint NOTICE of Motion (Re-Notice) and Withdrawal of Motion by LG. Philips LCD America, Inc., AU Optronics Corporation America, AU Optronics Corporation, LG.Philips LCD Co. Ltd. re 92 Joint MOTION to Consolidate Cases, 90 MOTION to Consolidate Cases (Pascale, Karen) (Entered: 07/06/2007)
07/10/2007	92	Amended ANSWER to Counterclaim of LG. Philips LCD Co. Ltd. , COUNTERCLAIM against LG.Philips LCD Co. Ltd. by AU Optronics Corporation America.(Pascale, Karen) (Entered: 07/10/2007)
07/10/2007	93	Amended ANSWER to Counterclaim of LG.Philips LCD Co. Ltd. , COUNTERCLAIM against LG.Philips LCD Co. Ltd. by AU Optronics Corporation. (Attachments: # 1 Exhibit A - C)(Pascale, Karen) (Entered: 07/10/2007)
07/10/2007	--	SO ORDERED D.I. 88 MOTION for Pro Hac Vice Appearance of Attorney M. Craig Tyler, Brian D. Range and Julie M. Holloway filed by AU Optronics Corporation, AU Optronics Corporation America. Signed by Judge Joseph J. Farnan, Jr. on 7/10/2007. (lec) (Entered: 07/10/2007)
07/11/2007	--	ORAL ORDER re 57 MOTION to Compel filed by AU Optronics Corporation. This motion will be decided after a decision has been rendered on the pending Motion to Consolidate. Therefore, the Notice for the Motion Day Hearing of July 13, 2007 is cancelled. Ordered by Judge Joseph Farnan this 11th day of July, 2007. (dlk) (Entered: 07/11/2007)
07/11/2007	94	ANSWER to Counterclaim filed by AU Optronics Corporation by LG.Philips LCD America.(Kirk, Richard) (Entered: 07/11/2007)
07/12/2007	95	NOTICE of Withdrawal of Motion to Compel LG.Philips LCD America to Respond to Requests for Production and Interrogatories and for Other Relief by AU Optronics Corporation re 57 MOTION to Compel (Pascale, Karen) (Entered: 07/12/2007)
07/16/2007	96	Disclosure Statement pursuant to Rule 7.1 filed by AU Optronics Corporation, AU Optronics Corporation America. (Pascale, Karen) (Entered: 07/16/2007)
07/19/2007	97	Disclosure Statement pursuant to Rule 7.1 filed by Chi Mei Optoelectronics Corporation identifying CHI MEI CORPORATION as Corporate Parent. (Rovner, Philip) (Entered: 07/19/2007)
07/19/2007	98	Disclosure Statement pursuant to Rule 7.1 filed by CHI MEI OPTOELECTRONICS USA, INC. identifying CMO JAPAN CO., LTD. as Corporate Parent. (Rovner, Philip) (Entered: 07/19/2007)
07/19/2007	99	ANSWERING BRIEF in Opposition re 89 MOTION to Dismiss for Lack of Jurisdiction Over the Person MOTION to Dismiss for Insufficiency of Service of Process filed by LG.Philips LCD America, LG.Philips LCD Co. Ltd..Reply Brief due date per Local Rules is 7/30/2007. (Attachments: # 1 Certificate of Service)(Stitzer, Ashley) (Entered: 07/19/2007)
07/19/2007	100	ORDER GRANTING D.I. 90 Motion to Consolidate Cases. This case is consolidated into Civil Action No. 06-726-GMS. All future filings shall be captioned and filed only in the consolidated lead case. Signed by Judge Joseph J. Farnan, Jr. on 07/19/2007. (dlk) (Entered: 07/23/2007)
07/19/2007	--	Case associated with lead case: Create association to 1:06-cv-00726-GMS. (dlk) (Entered: 07/23/2007)
07/23/2007	--	Case reassigned to Judge Gregory M. Sleet. Please include the initials of the Judge (GMS) after the case number on all documents filed. (Please note all future filings shall still be captioned and filed only in the consolidated lead case 1:06-cv-00726) (rjb) (Entered: 07/23/2007)
07/23/2007	101	ANSWER to Counterclaim of defendant Chi Mei Optoelectronics USA, Inc. by LG.Philips LCD America. (Attachments: # 1 certificate of service)(Kirk, Richard) (Entered: 07/23/2007)
07/24/2007	102	ANSWER to Counterclaim OF AU OPTRONICS CORPORATION AMERICA , COUNTERCLAIM against AU Optronics Corporation America by LG.Philips LCD Co. Ltd.. (Attachments: # 1 Exhibit A)(Kirk, Richard) (Entered: 07/24/2007)
07/24/2007	103	ANSWER to Counterclaim OF AU OPTRONICS CORPORATION , COUNTERCLAIM against AU Optronics Corporation by LG.Philips LCD Co. Ltd.. (Attachments: # 1 Exhibit A)(Kirk, Richard) (Entered: 07/24/2007)
09/28/2007	104	NOTICE of AU Optronics Corporation's Reply to LG.Philips LCD Co., Ltd's Additional Counterclaims by AU Optronics Corporation re 138 Answer to Counterclaim (Pascale, Karen) (Entered: 09/28/2007)
12/14/2007	--	Case reassigned to Judge Joseph J. Farnan, Jr. Please include the initials of the Judge (JJF) after the case number on all documents filed. (rjb) (Entered: 12/14/2007)
03/13/2008	--	CORRECTING ENTRY: Amended the party name for plaintiff and counterclaim plaintiff LG. Philips LCD Co., LTD to LG Display Co., Ltd., per DI # 161 ;and amended defendant and counterclaim plaintiff LG. Philips LCD America, Inc. to LG Display America, Inc., per DI # 161 . Also confirmed with counsel as to how the amended caption to read. (nms) (Entered: 03/13/2008)
03/28/2008	105	NOTICE of Service of AU Optronics Corporation's First Set of Requests for Production of Documents and Things to LG Display Co., Ltd., Nos. 1-110; AU Optronics Corporation's Second Set of Requests for Production of

		Documents to LG Display Co., Ltd. (Nos. 111-208); AU Optronics Corporation's First Set of Interrogatories to LG Display Co., Ltd. (Nos. 1-13), AU Optronics Corporation's Second Set of Interrogatories to LG Display Co., Ltd. (Nos. 14-23), and AU Optronics Corporation's Notice of Rule 30(b)(6) Deposition of Plaintiff LG Display Co. Ltd. by Au Optronics Corporation, AU Optronics Corporation America, AU Optronics Corporation re (1 in 1:06-cv-00726-JJF) Complaint, (Keller, Karen) (Entered: 03/28/2008)
04/16/2008	--	TRANSCRIPT of Status Telephone Conference held on 2/14/2008 before Judge Farnan. Court Reporter: Dale C. Hawkins (Hawkins Reporting). (Transcript on file in Clerk's Office) (nms) (Entered: 04/16/2008)
04/25/2008	107	NOTICE OF SERVICE of Defendant AU Optronics Corporation's Objections and Responses to Plaintiff LG Display Co., Ltd.'s First Set of Interrogatories (Nos. 1-19); and Defendant AU Optronics Corporation's Objections and Responses to Plaintiff LG Display Co., Ltd.'s First Set of Requests for the Production of Documents and Things (Nos. 1-83) by AU Optronics Corporation.(Pascale, Karen) (Entered: 04/25/2008)
05/01/2008	108	Letter to The Honorable Mary Pat Thynge from Karen L. Pascale regarding production of license agreements - re (191 in 1:06-cv-00726-JJF) Letter. (Pascale, Karen) (Entered: 05/01/2008)
06/23/2008	109	NOTICE OF SERVICE of LG Display Co., Ltd.'s Objections and Responses to Attachment A to AU Optronics Corporation's Notice of Rule 30(b)(6) Deposition by LG Display Co., Ltd.. (Attachments: # 1 Certificate of Service)(Kirk, Richard) (Entered: 06/23/2008)
07/17/2008	110	NOTICE OF SERVICE of AU Optronics Corporations Responses and Objections to Plaintiff LG Display Co., Ltd.s Second Set of Interrogatories (Nos. 20-29); and AU Optronics Corporations Supplemental Objections and Responses to Plaintiff LG Display Co., Ltd.s First Set of Interrogatories (Nos. 1-19) by AU Optronics Corporation.(Pascale, Karen) (Entered: 07/17/2008)
07/30/2008	--	ORAL ORDER: LG Display Co., Ltd. shall file a response to the July 30, 2008 letter (D.I. 364 in 06-726) by Chi Mei Optoelectronics Corp. no later than 9:00 a.m. on July 31, 2008. Ordered by Judge Joseph J. Farnan, Jr. on 7/30/2008. (dlk) (Entered: 07/30/2008)
09/08/2008	--	ORAL ORDER: The September 12, 2008 Motion Day Hearing is CANCELLED regarding MOTION to Consolidate Cases filed by LG Display Co., Ltd., MOTION for Leave to File Second Amended Answer to AU Optronics Corporation's Amended Counterclaims and Additional Counterclaims filed by LG Display Co., Ltd., and the MOTION to Consolidate Cases DEFENDANT CHI MEI OPTOELECTRONICS CORPORATION'S M OTION TO CONSOLIDATE AND TO EXTEND DISCOVERY LIMITS filed by Chi Mei Optoelectronics Corporation. The motions will be decided on the papers submitted. Ordered by Judge Joseph J. Farnan, Jr. on 09/08/2008. (dlk) (Entered: 09/08/2008)
09/08/2008	--	ORAL ORDER: The September 12, 2008 Motion Day Hearing is CANCELLED regarding the CHI MEI OPTOELECTRONICS CORPORATION'S MOTION TO LIMIT THE NUMBER OF PATENTS-IN-SUIT AND STAY THE REMAINDER filed by Chi Mei Optoelectronics Corporation. A decision is deferred pending possible oral argument. Ordered by Judge Joseph J. Farnan, Jr. on 9/8/08. (dlk) (Entered: 09/08/2008)
09/08/2008	--	ORAL ORDER: The September 12, 2008 Motion Day Hearing is CANCELLED regarding Motion to Compel Chi Mei Optoelectronics Corporation to Provide Discovery filed by LG Display Co., Ltd., PLAINTIFFS CHI MEI OPTOELECTRONICS' MOTION TO COMPEL DEFENDANTS LG DISPLAY TO RESPOND TO INTERROGATORIES filed by Chi Mei Optoelectronics USA Inc.(D.I. 98 in 08-cv-00355-JJF), Chi Mei Optoelectronics Corporation, and DEFENDANTS CHI MEI OPTOELECTRONICS' MOTION TO COMPEL PLAINTIFFS LG DISPLAY TO PRODUCE DOCUMENTS RESPONSIVE TO DOCUMENT REQUEST NO. 98 filed by Chi Mei Optoelectronics Corporation. The Court will decide these motions on the papers submitted. Ordered by Judge Joseph J. Farnan, Jr. on 9/8/08. (dlk) (Entered: 09/08/2008)
11/20/2008	111	MOTION for Leave to File A First Amended Answer and Joinder In CMO's Motion For Leave To File A First Amended Answer - filed by AU Optronics Corporation America, AU Optronics Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Local Rule 7.1.1 Statement)(Lundgren, Andrew) (Entered: 11/20/2008)
11/20/2008	112	NOTICE OF MOTION by AU Optronics Corporation America, AU Optronics Corporation re 111 MOTION for Leave to File ; Requesting the following Motion Day: December 19, 2008 (Lundgren, Andrew) Modified on 11/25/2008 (nms). (Entered: 11/20/2008)
12/04/2008	113	Amended NOTICE of [AUO's Amended Notice of Subpoena And Deposition to Centric Technical Sales on December 17, 2008] by AU Optronics Corporation America, AU Optronics Corporation re (234 in 1:06-cv-00726-JJF) Notice of Service (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	114	Amended NOTICE of Subpoena And Deposition to Bell Microproducts, Inc. on December 16, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (230 in 1:06-cv-00726-JJF) Notice of Service (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	115	Amended NOTICE of Subpoena And Deposition to Axis Group, Inc. on December 17, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (229 in 1:06-cv-00726-JJF) Notice of Service (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	116	Amended NOTICE of Subpoena And Deposition to Avnet, Inc on December 16, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (228 in 1:06-cv-00726-JJF) Notice of Service (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	117	Amended NOTICE of Subpoena And Deposition to Philips Electronics N.A., Inc. on December 17, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (344 in 1:06-cv-00726-JJF) Notice (Other) (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	118	Amended NOTICE of Subpoena And Deposition to LG Electronics Alabama, Inc. on December 15, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (341 in 1:06-cv-00726-JJF) Notice (Other)

		(Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	119	Amended NOTICE of Subpoena And Deposition to LG Electronics USA, Inc. on December 15, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (342 in 1:06-cv-00726-JJF) Notice (Other) (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	120	Amended NOTICE of Subpoena And Deposition to LG Infocomm, Inc. on December 15, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (340 in 1:06-cv-00726-JJF) Notice (Other) (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	121	Amended NOTICE of Subpoena And Deposition to LG International (America), Inc. on December 15, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (357 in 1:06-cv-00726-JJF) Notice (Other) (Pascale, Karen) (Entered: 12/04/2008)
12/04/2008	122	Amended NOTICE of Subpoena And Deposition to Catalyst Sales, Inc. on December 16, 2008 by Au Optronics Corporation, AU Optronics Corporation America re (233 in 1:06-cv-00726-JJF) Notice of Service (Pascale, Karen) (Entered: 12/04/2008)
12/08/2008	--	ORAL ORDER: The Court has reviewed the parties numerous email submissions regarding discovery disputes; therefore, Counsel shall appear for the December 19, 2008 Motion Day Hearing at 10:00 AM in Courtroom 4B before Judge Joseph J. Farnan, Jr. regarding these disputes. The non-prevailing party will be assessed all fees and costs associated with these disputes. Ordered by Judge Joseph J. Farnan, Jr. on 12/8/2008. (dlk) (Entered: 12/08/2008)
12/08/2008	--	CORRECTING ENTRY: The 12/8/2008 Oral Order has been corrected to note that the non-prevailing party will be assessed fees and costs associated with email discovery dispute. Associated Cases: 1:07-cv-00357-JJF, 1:06-cv-00726-JJF(dlk) (Entered: 12/08/2008)
12/12/2008	123	NOTICE of [AUO's Notice of Withdrawal of Amended Notice of Subpoena and Deposition of Philips Electronics N.A., Inc.] by AU Optronics Corporation America, AU Optronics Corporation re (117 in 1:07-cv-00357-JJF, 731 in 1:06-cv-00726-JJF) Notice (Other) (Lundgren, Andrew) (Entered: 12/12/2008)
12/22/2008	--	ORAL ORDER: The Court GRANTS parties Motions To Consolidate (D.I. 298 in 1:06-cv-00726-JJF, D.I. 89 in 1:08-cv-00355-JJF) and (D.I. 295 in 1:06-cv-00726-JJF). Accordingly, all future filings shall be made and captioned under C.A. No. 06-726 only.. Ordered by Judge Joseph J. Farnan, Jr. on 12/19/2008. Associated Cases: 1:06-cv-00726-JJF, 1:07-cv-00357-JJF, 1:08-cv-00355-JJF(dlk) (Entered: 12/22/2008)
12/22/2008	--	Case associated with lead case: Create association to 1:06-cv-00726-JJF. Associated Cases: 1:07-cv-00357-JJF, 1:08-cv-00355-JJF(dlk) (Entered: 12/22/2008)
01/23/2009	--	ORAL ORDER: LG's "motion" regarding 30(b)(6) depos per Mr. Kirk's January 16, 2009 e-mail request is DENIED. CMO's e-mail request for 30(b)(6) deposition, per Mr. Rovner's January 21, 2009 e-mail is GRANTED.. Signed by Judge Joseph J. Farnan, Jr. on 1/22/2009. Associated Cases: 1:06-cv-00726-JJF, 1:07-cv-00357-JJF, 1:08-cv-00355-JJF(dlk) (Entered: 01/23/2009)
02/27/2009	124	Joint Stipulation of Authenticity As To Certain Documents by CHI MEI OPTOELECTRONICS USA, INC., Chi Mei Optoelectronics Corporation, Au Optronics Corporation, AU Optronics Corporation America, LG Display Co. Ltd., LG Display America Inc.. (Pascale, Karen) Modified on 3/3/2009 (nms). (Entered: 02/27/2009)
03/03/2009	--	SO ORDERED, re (124 in 1:07-cv-00357-JJF, 1019 in 1:06-cv-00726-JJF, 106 in 1:08-cv-00355-JJF) Joint Stipulation of Authenticity as to Certain Documents, filed by LG Display America Inc., LG Display Co. Ltd., CHI MEI OPTOELECTRONICS USA, INC., AU Optronics Corporation America, Au Optronics Corporation, Chi Mei Optoelectronics Corporation. Signed by Judge Joseph J. Farnan, Jr. on 3/3/2009. Associated Cases: 1:06-cv-00726-JJF, 1:07-cv-00357-JJF, 1:08-cv-00355-JJF(nms) (Entered: 03/03/2009)
03/09/2009	125	NOTICE OF SERVICE of Expert Report of Jonathan D. Putnam by Au Optronics Corporation, AU Optronics Corporation America.(Pascale, Karen) (Entered: 03/09/2009)
03/09/2009	126	NOTICE OF SERVICE of Expert Report of Dr. Aris K. Silzars on Infringement of AUO's Asserted '781, '160, '157, '506 and '069 Patents by LGD's Accused Products by Au Optronics Corporation, AU Optronics Corporation America, AU Optronics Corporation.(Pascale, Karen) (Entered: 03/09/2009)
03/09/2009	127	NOTICE OF SERVICE of Report of Expert Abbie Gregg Regarding Invalidity of United States Patent Number 6,803,984; Report of Expert Webster Howard, Ph.D. Regarding Invalidity of United States Patent Number 4,624,737; Report of Expert Lawrence Tannas, Jr. Regarding Invalidity of United States Patent Number 7,218,374; Report of Expert Webster Howard, Ph.D. Regarding Invalidity of United States Patent Numbers 5,905,274, 6,815,321, and 7,176,489; Report of Expert Tsu-Jae King Liu, Ph.D. Regarding Invalidity of United States Patent Number 5,019,002; Report of Expert Tsu-Jae King Liu, Ph.D. Regarding Invalidity of United States Patent Number 6,664,569; and Report of Expert Tsu-Jae King Liu, Ph.D. Regarding Invalidity of United States Patent Number 5,825,449 by Au Optronics Corporation, AU Optronics Corporation America, AU Optronics Corporation.(Pascale, Karen) (Entered: 03/09/2009)
05/10/2009	128	Official Transcript of Pretrial Conference held on 05-07-09 before Judge Joseph J. Farnan, Jr. Court Reporter/Transcriber Leonard A. Dibbs. Transcript may be viewed at the court public terminal or purchased through the Court Reporter/Transcriber before the deadline for Release of Transcript Restriction. After that date it may be obtained through PACER (Redaction Request due 6/1/2009., Redacted Transcript Deadline set for 6/10/2009., Release of Transcript Restriction set for 8/10/2009.). (lad) (Entered: 05/10/2009)
05/12/2009	129	MEMORANDUM ORDER Setting Bench Trial between LG and AUO for 6/2/2009 09:30 AM in Courtroom 4B before Judge Joseph J. Farnan, Jr. A second Pretrial Conference is set for 5/20/2009 01:30 PM in Courtroom 4B before Judge Joseph J. Farnan, Jr. (See Order for details). Signed by Judge Joseph J. Farnan, Jr. on 5/12/2009. Associated Cases: 1:06-cv-00726-JJF, 1:07-cv-00357-JJF(dlk) (Entered: 05/12/2009)

05/21/2009	130	Official Transcript of Final Pretrial Conference held on 05-20-09 before Judge Joseph J. Farnan, Jr. Court Reporter/Transcriber Leonard A. Dibbs. Transcript may be viewed at the court public terminal or purchased through the Court Reporter/Transcriber before the deadline for Release of Transcript Restriction. After that date it may be obtained through PACER (Redaction Request due 6/11/2009., Redacted Transcript Deadline set for 6/22/2009., Release of Transcript Restriction set for 8/19/2009.). (lad) (Entered: 05/21/2009)
05/22/2009	131	REDACTED VERSION of (1266 in 1:06-cv-00726-JJF) SEALED MOTION in Limine No. 7 To Preclude LGD's Reliance On Certain Prior Art Products And Foreign Language References by AU Optronics Corporation. (Attachments: # 1 Text of Proposed Order)(Pascale, Karen) (Entered: 05/22/2009)
07/20/2009	--	CORRECTING ENTRY: Official Transcripts of 10 day Bench Trial held in June 2009 (DI 132 thru 141) removed from member case CA 07-357 JJF. For information regarding these transcripts, SEE LEAD CASE CA 06-726 JJF, DI 1366 thru 1375. (rbe) (Entered: 07/20/2009)

US District Court Civil Docket

U.S. District - Wisconsin Western
(Madison)

1:07cv137

Au Optronics Corporation v. Lg.Philips Lcd Co, Ltd

This case was retrieved from the court on Thursday, November 05, 2009

Date Filed:	**03/08/2007**	**Class Code:**	**TERM 05/30/2007**
Assigned To:	**Judge John C Shabaz**	**Closed:**	**Yes**
Referred To:	**Magistrate Judge Crocker**	**Statute:**	
Nature of suit:	**Patent (830)**	**Jury Demand:**	**Yes**
Cause:	**PROPERTY RIGHTS; Patent**	**Demand Amount:**	**$0**
Lead Docket:	**none**	**NOS Description:**	**Patent**
Other Docket:	**None**		
Jurisdiction:	**Federal Question**		

Litigants	Attorneys
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Defendant

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Washington , DC 20006-1108
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(202) 496-7500

Date	#	Proceeding Text
03/08/2007	--	NORTC - FEE PAID.
03/08/2007	1	JS-44
03/08/2007	2	COMPLAINT - SUMMONS ISSUED.
03/08/2007	3	DISCLOSURE OF CORP. AFFIL. & FINAN. INT. BY PLTF.
03/15/2007	4	SUMMONS
03/29/2007	5	NOTICE OF APPEARANCE BY JAMES PETERSON, BRADY WILLIAMSON, GASPARE BONO AND TYLER GOODWYN FOR DEFTS.
03/29/2007	6	MOTION TO DISMISS BY DEFTS.
03/29/2007	7	BRIEF IN SUPPORT OF DEFTS. MOTION TO DISMISS.
03/29/2007	8	AFFIDAVIT OF DONG HOON HAN.
03/29/2007	9	MOTION TO ADMIT GASPARE J. BONO PRO HAC VICE.
03/29/2007	10	MOTION TO ADMIT TYLER GOODWYN PRO HAC VICE.
03/29/2007	11	AFFIDAVIT OF JAMES D. PETERSON IN SUPPORT OF MOTION TO ADMIT GASPARE J. BONO PRO HAC VICE.
03/29/2007	12	AFFIDAVIT OF JAMES D. PETERSON IN SUPPORT OF MOTION TO ADMIT TYLER GOODWYN PRO HAC VICE.
04/02/2007	13	ORDER ADMITTING GASPARE BONO PRO HAC VICE.
04/02/2007	14	ORDER ADMITTING R. TYLER GOODWYN PRO HAC VICE.
04/03/2007	15	MOTION TO ADMIT ATTYS. M.TYLER, B.RANGE, B.DIETZEL, J.CHEN, R.SHULMAN AND S.BAIK PRO HAC VICE.
04/03/2007	16	AFFIDAVIT OF JAMES R. TROUPIS.
04/03/2007	17	DISCLOSURE OF CORP. AFFIL. & FINAN. INT. BY DEFT. LG.PHILIPS LTD.
04/03/2007	18	DISCLOSURE OF CORP. AFFIL. & FINAN. INT. BY DEFT. LG.PHILIPS AMERICA.
04/04/2007	19	ORDER ADMITTING M.TYLER, B.RANGE, B.DIETZEL, J.CHEN, R.SHULMAN AND S.BAIK PRO HAC VICE.
04/16/2007	20	PPTC REPORT BY PLTF.
04/16/2007	21	PPTC REPORT BY DEFTS.
04/16/2007	22	MOTION BY DEFTS. TO TRANSFER TO DISTRICT OF DELAWARE.
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04/17/2007	26	WAIVER OF SERVICE OF SUMMONS BY DEFT. LG.PHILIPS LTD.
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04/18/2007	29	AFFIDAVIT OF MICHAEL LESTINA.
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04/30/2007	31	BRIEF IN REPLY IN SUPPORT OF DEFTS. MOTION TO DISMISS.
04/30/2007	32	AFFIDAVIT OF DONG HOON HAN (SUPPLEMENTAL).
05/02/2007	33	MOTION BY PLTF. TO ADMIT JAMES C. YOON AND JULIE HOLLOWAY PRO HAC VICE.
05/02/2007	34	AFFIDAVIT OF JAMES R. TROUPIS.
05/03/2007	35	ORDER ADMITTING JAMES YOON AND JULIE HOLLOWAY PRO HAC VICE.
05/03/2007	36	BRIEF IN REPLY (CORRECTED) IN SUPPORT OF DEFT. LG PHILIPS LCD AMERICA MOTION TO DISMISS.
05/07/2007	37	BRIEF IN OPPOSITION BY PLTF. TO DEFTS. MOTION TO TRANSFER TO DISTRICT OF DELAWARE.
05/07/2007	38	AFFIDAVIT OF PAUL BARBATO.

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05/17/2007	40	BRIEF IN REPLY IN SUPPORT OF DEFTS. MOTION TO TRANSFER TO DISTRICT OF DELAWARE.
05/18/2007	41	MOTION BY PLTF. TO COMPEL DEFT. LG PHILIPS LCD AMERICA TO RESPOND TO REQ. FOR PROD. OF INTERROGS.
05/18/2007	42	BRIEF IN SUPPORT OF PLTF. MOTION TO COMPEL.
05/18/2007	43	AFFIDAVIT OF JAMES R. TROUPIS.
05/18/2007	44	AFFIDAVIT (2ND) OF DAVID W. PANNECK.
05/22/2007	45	BRIEF IN OPPOSITION BY DEFTS. TO PLTF. MOTION TO COMPEL.
05/22/2007	46	AFFIDAVIT OF NICOLE TALBOTT SETTLE.
05/23/2007	--	TELE. MOTION HEARING SET ON #41 FOR 5/30/07, 8:30 AM.
05/24/2007	--	RECD. PROPOSED PROTECTIVE ORDER; FORWARDED TO CHAMBERS.
05/29/2007	47	JOINT RULE 26 REPORT.
05/30/2007	48	PROTECTIVE ORDER
05/30/2007	49	ORDER TRANSFERRING CASE TO DISTRICT OF DELAWARE.
06/01/2007	--	RECORD SENT TO DISTRICT OF DELAWARE.
07/21/2008	--	Further docketing is in CM/ECF at pacer.wiwd.uscourts.gov

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068500 (10) 6689629 February 10, 2004

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

6689629

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February 10, 2004

Array , , substrate for , , display, method of , , manufacturing , , array , , substrate for , , display and , , display device using the , , array , , substrate

INVENTOR: Tsujimura, Takatoshi - Fujisawa, Japan (JP)Makita, Atsuya - Sagamihara, Japan (JP); Arai, Toshiaki - Yokohama, Japan (JP)

APPL-NO: 068500 (10)

FILED-DATE: February 5, 2002

GRANTED-DATE: February 10, 2004

CORE TERMS: conductive, display, substrate, wiring, array, dummy, etching, electrode, film, aluminum, density, pad, insulating, molybdenum, pixel, thin film, transistor, tapered, manufacturing, undercut, etchant, scan, alloy, acid, photoresist, preferable, wet, thickness, region, gate

ENGLISH-ABST:

Disclosed is to provide an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display. The present invention is an array substrate for display, which includes: a thin film transistor array formed on an insulating substrate 1; a plurality of wirings 23 and 24 arranged on the insulating substrate 1; connection pads 25 and 27 arranged on unilateral ends of the wirings 23 and 24 and respectively connected therewith; and pixel electrodes 22, wherein dummy conductive patterns 29 are arranged between the ends of the connection pads 25 and 27 and ends of the pixel electrodes 22.

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1. LG Display Co., Ltd. v. Au Optronics Corp., Civil Action No. 06-726-JJF,Civil Action No. 07-357-JJF, UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE, 2010 U.S. Dist. LEXIS 12903, February 16, 2010, Decided, Findings of fact/conclusions of law at LG Display Co. v. AU Optronics Corp., 2010 U.S. Dist. LEXIS 12969 (D. Del., Feb. 16, 2010)

   CORE TERMS: expert reports, prior art, chain, license, on-sale, personal knowledge, reduction, overrule, patent, admissibility ...

2. LG Display Co., Ltd. v. AU Optronics Corp., Civil Action No. 06-726-JJF,Civil Action No. 07-357-JJF, UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE, 2010 U.S. Dist. LEXIS 12969, February 16, 2010, Decided, Objection sustained by, Objection overruled by Lg Display Co. v. AU Optronics Corp., 2010 U.S. Dist. LEXIS 19074 (D. Del., Mar. 2, 2010)

   CORE TERMS: brightness, wiring, patent, display, substrate, film, signal, layer, array, frame ...

3. AU Optronics Corp. v. LG.Philips LCD Co., 07-C-137-S , UNITED STATES DISTRICT COURT FOR THE WESTERN DISTRICT OF WISCONSIN, 2007 U.S. Dist. LEXIS 39340, May 30, 2007, Decided , Related proceeding at Chi Mei Optoelectronics Corp. v. LG Philips LCD Co., 2008 U.S. Dist. LEXIS 25977 (E.D. Tex., Mar. 31, 2008)

   CORE TERMS: personal jurisdiction, interest of justice, venue, transferred, stream of commerce, consolidation, filed suit, manufacturer, convenience, patent infringement ...

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,697	03/16/2010	6689629	7773.0084	5947

24504 7590 04/22/2010

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ATLANTA, GA 30339-5994

EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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CENTRAL REEXAMINATION UNIT

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REEXAMINATION CONTROL NO. *90/009,697*.

PATENT NO. *6689629*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Order Granting / Denying Request For Ex Parte Reexamination	Control No.	Patent Under Reexamination	
	90/009,697	6689629	
	Examiner	Art Unit	
	TUAN H. NGUYEN	3992	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed *16 March 2010* has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a)☐ PTO-892, b)☐ PTO/SB/08, c)☐ Other: _____

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

2. ☐ The request for *ex parte* reexamination is DENIED.

This decision is not appealable (35 U.S.C. 303(c)). Requester may seek review by petition to the Commissioner under 37 CFR 1.181 within ONE MONTH from the mailing date of this communication (37 CFR 1.515(c)). **EXTENSION OF TIME TO FILE SUCH A PETITION UNDER 37 CFR 1.181 ARE AVAILABLE ONLY BY PETITION TO SUSPEND OR WAIVE THE REGULATIONS UNDER 37 CFR 1.183.**

In due course, a refund under 37 CFR 1.26 (c) will be made to requester:

a) ☐ by Treasury check or,

b) ☐ by credit to Deposit Account No. _____, or

c) ☐ by credit to a credit card account, unless otherwise notified (35 U.S.C. 303(c)).

cc:Requester (if third party requester)

DECISION ON REQUEST FOR REEXAMINATION

Reexamination has been requested for claims 1-16 of United States Patent number 6,689,629 to Tsujimura et al., entitled: "ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE" (hereinafter "the '629 patent").

A substantial new question of patentability affecting claims 1-16 of the '629 patent is raised by the request for ex parte reexamination.

Substantial New Question of Patentability

In the request for reexamination, the third party requester alleges that the following prior art references raise a substantial new question of patentability of the issued claims 1-16 of the '629 patent.

1. U.S. Patent No. 6,163,356 to Song et al. (hereinafter "Song").
2. U.S. Patent No. 5,850,275 to Watanabe et al. (hereinafter "Watanabe '275").
3. U.S. Patent No. 6,862,069 to Kwak et al. (hereinafter "Kwak").
4. U.S. Patent No. 5,995,189 to Zhang (hereinafter "Zhang").
5. U.S. Patent No. 6,157,430 to Kubota et al. (hereinafter Kubota).
5. EP 0 887 695 A2 to Hirabayashi (hereinafter "Hirabayashi").
6. JP 10-333151 to Yamamoto et al. (hereinafter "Yamamoto").
7. JP 10-82909 to Harada et al. (hereinafter "Harada").

8. JP 6-82811 to Watanabe et al. (hereinafter "Watanabe").

9. JP 9-197415 to Miyashita et al. (hereinafter "Miyashita").

10. JP Pub. No. 2000-098909 to Tomoyuki (hereinafter Tomoyuki).

Prosecution History for US Patent 6,689,629

The application was filed on 02/05/2002, now Pat. No. 6,689,629.

The prosecution history of the '629 patent shows that in the first Office Action dated 05/29/2003, claims 1 and 10 was rejected under 35 U.S.C. 102(b) as being anticipated by Shirahashi et al. (US 5,285,301), and claims 3-9, 12-18 were rejected under 35 U.S.C 103(a) as being obvious over Shirahashi in view of Song et al. (US 6,163,356). Claims 2 and 11 were objected for the reason as "The prior art of record does not teach or suggest the area protected by the dummy metallization recited in claims 2 and 11".

The Patent Owner response on 08/29/2003 in which claims 1 and 10 were amended to incorporate the subject matter of claims 2 and 11 respectively. A Notice of Allowance for the claims 1, 3-10, 12-18 (renumbered as 1-16) was issued by the Examiner on 10/01/2003.

In view of the prosecution history, it is considered that the evaluation of a prior art reference that teaches or suggests a method for forming an array substrate for display or an array thereof that includes dummy conductive patterns comprising at least about

30% of the are of the insulating substrate would have been considered important in determining the patentability of the claims.

Issues Raised by the Request

The request indicates that requester considers that a substantial new question of patentability is raised as to claims 1-16 of the '629 patent based on:

Issue 1: The request indicates that requester considers that a substantial new question of patentability is raised as to claims 1-16 of the '629 patent based on Hirabayashi either alone or in view of others.

Issue 2: The request further indicates that requester considers that a substantial new question of patentability is raised as to claims 1-16 of the '629 patent based on Watanabe '275 either alone or in view of others.

Issue 3: The request further indicates that requester considers that a substantial new question of patentability is raised as to claims 1-16 of the '629 patent based on Kwak either alone or in view of others.

Issue 4: The request further indicates that requester considers that a substantial new question of patentability is raised as to claims 1-16 of the '629 patent based on Yoshinori either alone or in view of others.

Issue 5: The request further indicates that requester considers that a substantial new question of patentability is raised as to claims 1-16 of the '629 patent based on Tomoyuki either alone or in view of others.

Issue 6: The request further indicates that requester considers that a substantial new question of patentability is raised as to claims 1-16 of the '629 patent based on Zhang either alone or in view of others.

Issue 7: The request further indicates that requester considers that a substantial new question of patentability is raised as to claims 1-16 of the '629 patent based on Watanabe '811 either alone or in view of others.

Issue 8: The request further indicates that requester considers that a substantial new question of patentability is raised as to claims 1-16 of the '629 patent based on Miyashita either alone or in view of others.

Analysis of the Prior Art provided in the Request

1/. It is agreed that the consideration of Hirabayashi raises a substantial new question of patentability to at least independent claims 1, and 9 of the '629 patent.

As pointed out in Appendix CC1 of the request, Hirabayashi, fig. 1 and text on col. 1, lines 1-7 appears to disclose an array substrate for a liquid crystal display and method for forming an array substrate including a thin film transistor formed on an insulating substrate (col. 31, lines 16-35); a plurality of wiring arranged on the insulating substrate in communication with at least one of the transistor in the thin film array (fig. 2, item 7); connection pads 26 connecting to the opposite end of the plurality of wirings; pixel electrode 20 (fig. 1); and dummy conductive pattern (figs. 1, 4-7) comprising at least about 30% of the area of the insulating substrate and situated between the connection pads 26 and the pixel electrode 20 such that the dummy patterns are not in contact with any of the wiring.

There is a substantial likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the claims are patentable. However, the prosecution history of the base application, US serial No. 10/068,500, does not indicate that Hirabayashi was included for consideration by the examiner in charge of the base application. Accordingly, Hirabayashi raises a substantial new question of patentability as to at least independent claims 1, and 9 of the '629 patent which question has not been decided in the previous examination of the '629 patent.

Because independent claims 1, and 9 carry all of the limitations of the dependent claims 2-8, and 10-16 from which it stems, by raising a substantial new question of patentability with regard to independent claims 1, 9, the reference implicitly raises a substantial new question of patentability for claims 2-8, and 10-16 respectively.

2/. It is not agreed that the consideration of Watanabe '275 either alone or in view of others raises a substantial new question of patentability to at least independent claims 1, and 9 of the '629 patent.

Watanabe '275 discloses a liquid crystal display with light shield 20 formed between terminal groups 15 in a side near outgoing line groups in a display portion 14 of a liquid display panel (abstract and related fig. 1). The light shield 20 is formed to prevent any light leakage from areas between the terminal groups 15 so as to reduce the unevenness of brightness on the display portion 14 and obtain a favorable display condition (col. 4, lines 17-21).

The light shield 20 is an essential part of the liquid crystal display in order to obtain a favorable display condition as disclosed by Watanabe '275; therefore it can not be considered as a dummy, and would be removed or left as they are without being eliminated as disclosed in the patent (col. 6, lines 52-55).

Since none of the reference to Watanabe '275, Song, the '629 APA or Kubota direct to a process of etching with the use of dummy to prevent undercut of the lower conductive material; therefore, the combination of Watanabe '275 together with Song or

the '629 APA or Kubota does not result in wirings having good tapered shape as disclosed by the '629 patent.

3/. It is agreed that the consideration of Kwak raises a substantial new question of patentability to at least independent claims 1, and 9 of the '629 patent.

As pointed out in Appendix CC9 of the request, Kwak, fig. 1 and text on col. 1, lines 32-36 appears to disclose an array substrate for a liquid crystal display and method for forming an array substrate including a thin film transistor formed on an insulating substrate (col. 31, lines 43-45); a plurality of wiring arranged on the insulating substrate in communication with at least one of the transistor in the thin film array (figs. 7-10, gate links 15 and data links 33 are formed on transparent substrate 20 that connect to TFTs); connection pads (figs. 7-10, gate pads 14 and data pads 32 that contact the gate links 15 and data links 32) connecting to the opposite end of the plurality of wirings; pixel electrode 20 (col. 1, lines 45-46); and dummy conductive pattern 36, 38 (figs. 7-9) comprising at least about 30% of the area of the insulating substrate and situated between the connection pads 14, 32 and the pixel electrode 10 such that the dummy patterns are not in contact with any of the wiring (figs. 7-12, col. 4, lines 28-41).

There is a substantial likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the claims are patentable. However, the prosecution history of the base application, US serial No. 10/068,500, does not indicate that Kwak was included for consideration by the examiner in charge of

the base application. Accordingly, Kwak raises a substantial new question of patentability as to at least independent claims 1, and 9 of the '629 patent which question has not been decided in the previous examination of the '629 patent.

Because independent claims 1, and 9 carry all of the limitations of the dependent claims 2-8, and 10-16 from which it stems, by raising a substantial new question of patentability with regard to independent claims 1, 9, the reference implicitly raises a substantial new question of patentability for claims 2-8, and 10-16 respectively.

4/. It is agreed that the consideration of Yoshinori raises a substantial new question of patentability to at least independent claims 1, and 9 of the '629 patent.

As pointed out in Appendix CC13 of the request, Yoshinori, figs. 1-3 and abstract appears to disclose an array substrate for a liquid crystal display and method for forming an array substrate including a thin film transistor formed on an insulating substrate; a plurality of wiring arranged on the insulating substrate in communication with at least one of the transistor in the thin film array (scan and signal wiring that connect to the scan and signal electrodes 6 and 9); connection pads 3, 4 that connect to the scan and signal wiring; pixel electrode 10; and dummy conductive pattern 5 comprising at least about 30% of the area of the insulating substrate and situated between the connection pads 3, 4 and the pixel electrode 10 such that the dummy patterns are not in contact with any of the wiring (figs. 1-3, para. [0020]).

There is a substantial likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the claims are patentable.

However, the prosecution history of the base application, US serial No. 10/068,500, does not indicate that Yoshinori was included for consideration by the examiner in charge of the base application. Accordingly, Yoshinori raises a substantial new question of patentability as to at least independent claims 1, and 9 of the '629 patent which question has not been decided in the previous examination of the '629 patent.

Because independent claims 1, and 9 carry all of the limitations of the dependent claims 2-8, and 10-16 from which it stems, by raising a substantial new question of patentability with regard to independent claims 1, 9, the reference implicitly raises a substantial new question of patentability for claims 2-8, and 10-16 respectively.

5/. The rejection of claims 1-16 over Tomoyuki either alone or in combination with others is proposed in claim chart in appendix CC17, CC18, CC19, CC20; however, Tomoyuki reference with English translation is not submitted nor listed in the IDS dated 2/26/10. The Requester is requested to submit the Tomoyuki with English translation in the next communication for consideration.

6/. It is agreed that the consideration of Zhang raises a substantial new question of patentability to at least independent claims 1, and 9 of the '629 patent.

As pointed out in Appendix CC21 of the request, Zhang, figs. 1, 16-17 and text on col. 6, lines 25-44 appears to disclose an array substrate for a liquid crystal display and method for forming an array substrate including a thin film transistor formed on an insulating substrate; a plurality of wiring (scan lines 2 and signal lines 3) arranged on

the insulating substrate in communication with at least one of the transistor in the thin film array (col. 3, lines 32-40); connection pads 6 that connect to the scan and signal lines 2, 3; pixel electrode 12; and dummy conductive pattern 304 comprising at least about 30% of the area of the insulating substrate and situated between the connection pads 6 and the pixel electrode 12 such that the dummy patterns are not in contact with any of the wiring (figs. 4, 8, 16 and col. 10, lines 7-17).

There is a substantial likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the claims are patentable. However, the prosecution history of the base application, US serial No. 10/068,500, does not indicate that Zhang was included for consideration by the examiner in charge of the base application. Accordingly, Zhang raises a substantial new question of patentability as to at least independent claims 1, and 9 of the '629 patent which question has not been decided in the previous examination of the '629 patent.

Because independent claims 1, and 9 carry all of the limitations of the dependent claims 2-8, and 10-16 from which it stems, by raising a substantial new question of patentability with regard to independent claims 1, 9, the reference implicitly raises a substantial new question of patentability for claims 2-8, and 10-16 respectively.

7/. It is agreed that the consideration of Watanabe '811 raises a substantial new question of patentability to at least independent claims 1, and 9 of the '629 patent.

As pointed out in Appendix CC25 of the request, Watanabe '811, fig. 5 and para. [0034]-[0038] appears to disclose an array substrate for a liquid crystal display and

method for forming an array substrate including a thin film transistor formed on an insulating substrate; a plurality of wiring (signal and scanning lines 5, 9) arranged on the insulating substrate in communication with at least one of the transistor in the thin film array (para. [0035]); connection pads (inherently present) that connect to the signal and scanning lines; pixel electrode 7 (fig. 4); and dummy conductive pattern 25, 27 comprising at least about 30% of the area of the insulating substrate and situated between the connection pads and the pixel electrode 7 such that the dummy patterns are not in contact with any of the wiring (fig. 5, para. [0071]).

There is a substantial likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the claims are patentable. However, the prosecution history of the base application, US serial No. 10/068,500, does not indicate that Watanabe '811 was included for consideration by the examiner in charge of the base application. Accordingly, Watanabe '811 raises a substantial new question of patentability as to at least independent claims 1, and 9 of the '629 patent which question has not been decided in the previous examination of the '629 patent.

Because independent claims 1, and 9 carry all of the limitations of the dependent claims 2-8, and 10-16 from which it stems, by raising a substantial new question of patentability with regard to independent claims 1, 9, the reference implicitly raises a substantial new question of patentability for claims 2-8, and 10-16 respectively.

8/. It is agreed that the consideration of Miyashita raises a substantial new question of patentability to at least independent claims 1, and 9 of the '629 patent.

As pointed out in Appendix CC29 of the request, Miyashita, fig. 3 and paragraphs [0018]-[0019] appears to disclose an array substrate for a liquid crystal display and method for forming an array substrate including a thin film transistor formed on an insulating substrate; a plurality of wiring (gate and data lines 5, 6) arranged on the insulating substrate in communication with at least one of the transistor in the thin film array (fig. 2, [0019]); connection pads 5b, 6b that connect to the gate and data lines; pixel electrode 3 (fig. 3); and dummy conductive pattern 8 formed in region D comprising at least about 30% of the area of the insulating substrate and situated between the connection pads 5b and the pixel electrode 3 such that the dummy patterns are not in contact with any of the wiring (fig. 3, para. [0023]).

There is a substantial likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the claims are patentable. However, the prosecution history of the base application, US serial No. 10/068,500, does not indicate that Miyashita was included for consideration by the examiner in charge of the base application. Accordingly, Miyashita raises a substantial new question of patentability as to at least independent claims 1, and 9 of the '629 patent which question has not been decided in the previous examination of the '629 patent.

Because independent claims 1, and 9 carry all of the limitations of the dependent claims 2-8, and 10-16 from which it stems, by raising a substantial new question of patentability with regard to independent claims 1, 9, the reference implicitly raises a substantial new question of patentability for claims 2-8, and 10-16 respectively.

Summary

The use of references Hirabayashi, Kwak, Yoshinori, Watanabe '811, Zhang, and Miyashita which appear to discuss many of the key elements or limitations of claims 1-16; make it likely that a reasonable examiner would consider these teachings important in deciding whether or not the claims are patentable.

The prosecution history of the base application does not indicate that the Hirabayashi, Kwak, Yoshinori, Watanabe '811, Zhang, and Miyashita references were included for consideration by the examiner in charge of the base application.

Accordingly, such teachings are not cumulative to any written discussion on the record of the teachings of the prior art, were not previously considered not addressed during a prior examination and the same question of patentability was not the subject of a final holding of invalidity by the Federal Courts.

Accordingly, the request for reexamination is GRANTED. Claims 1-16 will be reexamined.

Conclusion

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that ex parte reexamination proceedings "will be conducted with special dispatch" (37

CFR 1.550(a)). Extensions of time in ex parte reexamination proceedings are provided for in 37 CFR 1.550(c).

The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity or other prior or concurrent proceeding, involving the 6,689,629 patent throughout the course of this reexamination proceeding. The requester is also reminded of the ability to similarly appraise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

Telephone numbers for reexamination inquiries:

Reexamination and Amendment practice

(571) 272-7703

Central Reexam Unit (CRU)

(571) 272-7705

Reexamination Facsimile Transmission No.

(571) 272-9900

All correspondence relating to this *ex parte* reexamination proceeding should be directed:

By Mail to: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450

Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

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Any inquiry concerning this communication should be directed to Tuan Nguyen at telephone number 571-272-1694

Signed:

Tuan H. Nguyen
Primary Examiner
Central Reexamination Unit
Art Unit 3992

Conferees:

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90009697	6689629
	Examiner	Art Unit
	TUAN H NGUYEN	3992

SEARCHED

Class	Subclass	Date	Examiner
None			

SEARCH NOTES

Search Notes	Date	Examiner
Reviewed of patented file's prosecution history	4/16/10	TN

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

Reexamination	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90009697	6689629
	Certificate Date	Certificate Number

Requester Correspondence Address:	☐ Patent Owner	☒ Third Party

SONG K. JUNG
MCKENNA LONG AND ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

LITIGATION REVIEW ☒	TN (examiner initials)	04/20/2010 (date)
Case Name		Director Initials
Open 1:07cv357 Au Optronics Corp. v. Lg. Philips Lcd Co Ltd et al		MK for 6CM
Closed 1:07cv137 Au Optronics Corp. v. Lg. Philips Lcd Co. Ltd et al		↓

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	NUMBER
1. None	

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	90009697
Filing Date	2010-03-16
First Named Inventor	Tsujimura
Art Unit	3992
Examiner Name	
Attorney Docket Number	250129-1080

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	1	2000098909	JP	A	2000-04-07	Sanyo Electric Co. Ltd.		☐
	2	02-189922	JP	A	1990-07-25	NEC Corp.		☐
	3	05-061072	JP	A	1993-03-12	Hitachi Ltd.		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	90009697
	Filing Date	2010-03-16
	First Named Inventor	Tsujimura
	Art Unit	3992
	Examiner Name	
	Attorney Docket Number	250129-1080

	4	10-090706	JP	A	1998-04-10	Toshiba Corp.		☐
	5	10-240150	JP	A	1998-09-11	Samsung Electron Co. Ltd.		☐
	6	10-282528	JP	A	1998-10-23	LG Electron Inc.		☐
	7	11-242211	JP	A	1999-09-07	Sharp Corp, Sony Corp.		☐
	8	11-153816	JP	A	1999-06-08	Citizen Watch Co. Ltd.		☐
	9	09-146097	JP	A	1997-06-06	Sharp Corp., UK Government		☐

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Japanese Language Office Action dated December 26, 2008 and English translation of Office Action.	☐
	2	Japanese Language Office Action dated May 12, 2009 and English translation of Office Action.	☐
	3	Japanese Language Appeal Decision dated January19, 2006 and English translation of Appeal Decision.	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	90009697
	Filing Date	2010-03-16
	First Named Inventor	Tsujimura
	Art Unit	3992
	Examiner Name	
	Attorney Docket Number	250129-1080

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	90009697
	Filing Date	2010-03-16
	First Named Inventor	Tsujimura
	Art Unit	3992
	Examiner Name	
	Attorney Docket Number	250129-1080

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Daniel R. McClure/	Date (YYYY-MM-DD)	2010-07-12
Name/Print	Daniel R. McClure	Registration Number	38962

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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	1/1339	５００		1/1339	５００
Ｇ０９Ｆ	9/35	３０５	Ｇ０９Ｆ	9/35	３０５

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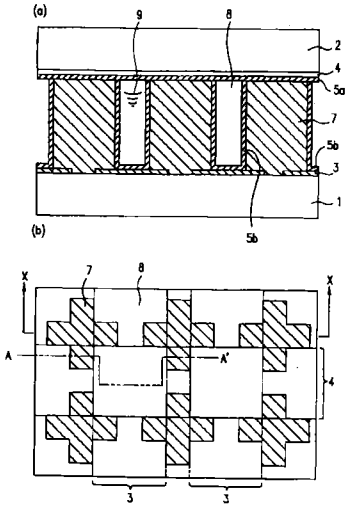
最終頁に続く

(54)【発明の名称】　液晶表示装置

(57)【要約】

【課題】　「クロマト現象」を生じ難くして表示品位の向上を図れ、しかも、広視野角特性に優れると共にセル厚を一定に維持することができるようにする。

【解決手段】　液晶層９を挟んでガラス基板１と２とが対向配設され、両基板１、２間の液晶層９中の所定箇所には柱状スペーサ７が両基板１、２に達するように設けられる。ガラス基板２の液晶層９側の内表面には、ストライプ状の信号電極４と垂直配向層５ａが形成されている。ガラス基板１の液晶層９側の内表面には、信号電極４と交差する状態で信号電極３がストライプ状に形成されており、信号電極３と信号電極４との交差部分で絵素が構成される。この絵素の四隅に相当する角に前記柱状スペーサ７が配置される。柱状スペーサ７の側面やガラス基板１上に垂直配向層５ｂが形成される。



【特許請求の範囲】

【請求項1】　各々電極を有する一対の基板と、該一対の基板に挟持された液晶層とを有している液晶表示装置において、

該液晶層は負の誘電異方性を有する液晶分子からなり、両基板に達するように柱状スペーサが設けられており、該一対の基板の液晶層に接する表面および該柱状スペーサの表面に垂直配向層が形成され、該液晶層は絵素毎に少なくとも一つの該柱状スペーサにて規定される絵素領域を有するとともに、該液晶層への電圧無印加時には該液晶分子が該一対の基板の表面に対し略垂直に配向し、該液晶層への電圧印加時には該液晶分子が該絵素領域毎に軸対称状に配向していることを特徴とする液晶表示装置。

【請求項2】　前記一対の基板の少なくともどちらか一方の基板の前記液晶層に接する表面に、高分子材料からなる軸対称配向固定層が形成されている請求項1に記載の液晶表示装置。

【請求項3】　対向配設された基板および誘電体シートと、これらの間に形成された隔壁とで囲まれたライン状空間が放電チャンネルとなっているプラズマ発生基板と、

該プラズマ発生基板の該誘電体シートに対して一定の間隙を保持して対向配設され、かつ、該ライン状の放電チャンネルと交差するようライン状の信号電極が形成された第2の基板と、

該誘電体シートと該第2の基板との間に液晶層とを有している、プラズマアドレス型液晶表示装置において、

該液晶層は負の誘電異方性を有する液晶分子からなり、該誘電体シートと該第2の基板とに達するように柱状スペーサが設けられており、該誘電体シートおよび該第2の基板の液晶層に接する表面および該柱状スペーサの表面に垂直配向層が形成され、該液晶層は絵素毎に少なくとも一つの該柱状スペーサにて規定される絵素領域を有するとともに、該液晶層への電圧無印加時には該液晶分子が該誘電体シートと該第2の基板の表面に対し略垂直に配向し、該液晶層への電圧印加時には該液晶分子が該絵素領域毎に軸対称状に配向していることを特徴とするプラズマアドレス型の液晶表示装置。

【請求項4】　前記第2の基板および前記誘電体シートの少なくともどちらか一方の前記液晶層に接する表面に、高分子材料からなる軸対称配向固定層が形成されている請求項3に記載の液晶表示装置。

【請求項5】　前記柱状スペーサが、前記絵素領域の周囲の少なくとも4箇所に配設されていることを特徴とする請求項1ないし4のいずれかに記載の液晶表示装置。

【請求項6】　前記柱状スペーサが、前記絵素領域の各々に対応するものを点対称または線対称の位置に配して形成されていることを特徴とする請求項5に記載の液晶表示装置。

【請求項7】　前記柱状スペーサが、前記絵素領域の角部もしくは四辺に接するように、または角部および四辺の両方のうちの任意の箇所に接するように形成されていることを特徴とする請求項5または6に記載の液晶表示装置。

【請求項8】　前記柱状スペーサの該一対の基板と水平な方向での断面形状が、四角形、四角形の角を丸めた形、十字形、T字形、くの字形、円形、および楕円形のいずれかである請求項1ないし7のいずれかに記載の液晶表示装置。

【請求項9】　前記柱状スペーサが、前記絵素領域の角部と、四辺に接しながら四辺のそれぞれを2等分もしくは3等分する箇所に配設されていることを特徴とする請求項1に記載の液晶表示装置。

【請求項10】　前記柱状スペーサの前記一対の基板と水平な方向での断面形状は、四角形、四角形の角を丸めた形、円形、および半円形のいずれかであり、該柱状スペーサに外接する四角形が互いに隣接する絵素の間に収まる大きさであり、かつ、該柱状スペーサの短い方の一辺が5μmよりも長いことを特徴とする請求項9に記載の液晶表示装置。

【請求項11】　前記柱状スペーサを複数有し、互いに隣接する該柱状スペーサの間隔をD、該柱状スペーサの断面形状が四角形の場合、該四角形の一辺の長さをｄｓとし、該柱状スペーサの断面形状が円形の場合、該円形の直径をｄｓとしたとき、長さの比ｙ（＝Ｄ／ｄｓ）が、

$0.1 \leqq y \leqq 4.49e^{-0.0607ds} + 1.5$

の関係にあることを特徴とする請求項9または10に記載の液晶表示装置。

【請求項12】　前記柱状スペーサが、前記絵素領域の角部を除いた四辺に接するように配設されていることを特徴とする請求項1から7のいずれかに記載の液晶表示装置。

【請求項13】　前記柱状スペーサの前記一対の基板と水平な方向での断面形状は、長方形または長方形の角を丸めた形であり、絵素に対して垂直な辺は5μmよりも長く、隣接する絵素間の長さよりも短く、絵素に対して平行な辺の長さが、絵素の各辺の長さの20％よりも長く99％よりも短いことを特徴とする請求項12に記載の液晶表示装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、例えばパーソナルコンピュータ、ワードプロセッサ、アミューズメント機器、テレビジョン装置などの平面ディスプレイ等に好適に用いられる広視野角特性を有する液晶表示装置に関する。

【0002】

【従来の技術】上述した平面ディスプレーに利用される

液晶表示装置（ＬＣＤ）としては、現在、ＴＮモードを主に使用したものが知られている。かかるＴＮモードの液晶表示装置は、視野角が狭いため、それを改善すべく広視野角化を図ることが行われている。

【０００３】広視野角化を図る技術として、液晶分子を各絵素ごとに軸対称状に配向させ、広視野角化を図る表示モード（Axially Symmetric Aligned Microcell Mode:ＡＳＭモード）が提案されている（特開平６－３０１０１５号公報および特開平７－１２０７２８号公報）。この技術は、一対の基板間に、高分子壁およびこれにより囲まれた液晶領域からなる表示媒体を挟持させ、かつ、液晶領域毎に液晶分子を軸対称状に配向させる技術であり、この技術による場合には視角特性を著しく改善させることが可能となる。

【０００４】また、他の技術として、絵素領域ごとに液晶分子が軸対称配向した、広視野角化を図り得る液晶層を有し、全方位視角特性の優れた高コントラストの液晶表示装置を比較的簡単に得ることができる技術が提案されている（特願平８－３４１５９０号）。この技術を、図２２に基づいて説明する。図２２は、この技術を適用した液晶表示装置の具体的構成を示す模式図であり、図２２（ｂ）はその平面図、図２２（ａ）は図２２（ｂ）のＸ－Ｘ線による断面図である。この液晶表示装置は、所定の間隙をもって対向配設されたガラス基板１０１とガラス基板１０２とを有し、両基板１０１、１０２間には負の誘電率異方性を有する液晶材料からなる液晶層１０９が挟持されている。図上側のガラス基板１０２の内表面には、信号電極１０４がストライプ状に形成されており、この上を覆ってポリイミド等の垂直配向層１０５がほぼ全面に形成されている。また、図下側のガラス基板１０１の内表面には、信号電極１０３が前記信号電極１０４と交差する状態でストライプ状に形成されており、さらにその上に格子状の区画壁１０６が設けられ、この区画壁１０６の上に選択的に柱状突起１０７が図上側のガラス基板１０２に達するように設けられている。前記区画壁１０６は、例えば感光性樹脂を、マスクを介して露光現像することによりパターニング形成されており、柱状突起１０７も区画壁１０６と同様に、例えば感光性樹脂を、マスクを介して露光現像することによりパターニング形成されている。これら信号電極１０３、区画壁１０６及び柱状突起１０７の上は、ポリイミド等からなる垂直配向層１０５が被覆されている。

【０００５】この技術においては、区画壁１０６によって絵素領域１０８の位置および大きさを規定している。区画壁１０６によって囲まれた部分が絵素領域１０８となり、両信号電極１０３、１０４の間の電圧無印加時には、絵素領域１０８内の液晶分子が一対の基板１０１、１０２に対して略垂直に配向し、電圧印加時には液晶分子が各絵素領域１０８毎に軸対称状に配向する。また、区画壁１０６と基板１０２との間に存在する柱状突起１０７は、基板１０２に接する故に、セル厚を一定に維持する機能を有する。

【０００６】更には、前記特願平８－３４１５９０号においては、電圧印加時において各絵素領域毎の液晶分子を安定に軸対称状配向させるべく、一対の基板の少なくとも一方の絵素領域に対応する領域上の凹凸表面に、高分子材料からなる軸対称配向固定層を設ける技術も開示している。この軸対称配向固定層の形成は、例えば、負の誘電率異方性を有する液晶材料と光硬化性材料とを含んでなる前駆体混合物を、一対の基板間に配し、この混合物を光照射することにより前駆体混合物を硬化させることにより実現できる。

【０００７】ところで、上述したＴＮモードのＬＣＤや、各絵素のオンオフ制御を行うスイッチング素子として薄膜トランジスタ（ＴＦＴ）を用いたＴＦＴ－ＬＣＤに代わる、２０インチ型を越える大型ディスプレイとして開発が進められている技術の一つに、プラズマアドレス型の液晶表示装置（ＰＡＬＣＤ）が知られている（例えば特開平１－２１７３９６号公報や特開平４－２８５９３１号公報）。

【０００８】このプラズマアドレス型の液晶表示装置は、図２３に示すように、液晶層２０２を挟んで一方側（図の上側）に透明な基板２０１を有し、他方側（図の下側）に薄板ガラス２１６と基板２１１とが対向配設されたプラズマ発生基板２１０を有する。プラズマ基板２１０の基板２１１と薄板ガラス２１６との間には、ライン状に隔壁２１２が形成され、この隔壁２１２と、基板２１１と、薄板ガラス２１６とで囲まれた空間は、電離用ガスが封入されたライン状のチャンネル２１３を構成する。各チャンネル２１３内には、電離用ガスをイオン化するためのアノード電極２１４およびカソード電極２１５が設けられている。一方、基板２０１の液晶層２０２側には、データ線としての透明電極２０５が、ストライプ状に、かつ、ライン状のチャンネル２１３に対して垂直方向に配線されている。前記液晶層２０２は、基板２０１と薄板ガラス２１６とに挟持されており、基板２０１と薄板ガラス２１６との間のセル厚は、例えばプラスチックビーズ等のセル厚制御材２０６にて一定に維持されている。なお、基板２０１および薄板ガラス２１６の液晶層２０２側の表面には、図示しない配向膜が形成されている。

【０００９】上述したプラズマアドレス型の液晶表示装置を対象として広視野角化を実現する技術として、図２４に示すように、液晶セルの表示媒体が、高分子壁とこれにて囲まれた液晶領域とからなり、高分子壁が液晶セルのセル厚制御材としての機能を果たす技術が提案されている（特開平９－１９７３８４号公報）。

【００１０】図２４（ａ）は、この技術を適用したプラズマアドレス型の液晶表示装置を示す断面図であり、図２４（ｂ）はその絵素配列を示す平面図である。なお、

図２３と同一部分には同一番号を付している。

【００１１】このプラズマアドレス型の液晶表示装置は、図２３に示す液晶層２０２の部分が異なり、その液晶層２０２に代わる表示媒体２２０が液晶領域２２０ａとこれを囲む高分子壁２２０ｂとからなっており、液晶領域２２０ａ内の液晶分子は軸対称状に配向している。また、この液晶領域２２０ａは、図２４（ｂ）に示すようにマトリクス状に配置されている。なお、図２４（ａ）中の２２１および２２２は、それぞれ偏光板を示す。

【００１２】さらに、前記特開平９－１９７３８４号公報には、他の技術として、図２５に示すように、表示媒体中に隔壁の少なくとも１つと交差して壁状スペーサが設けられているプラズマアドレス型の液晶表示装置が開示されている。

【００１３】図２５（ａ）はそのプラズマアドレス型の液晶表示装置を示す断面図であり、図２５（ｂ）はその平面図である。なお、図２３と同一部分には同一番号を付している。このプラズマアドレス型の液晶表示装置は、図２５（ｂ）に示すように、表示媒体２２０を挟む基板２０１とプラズマ発生基板２１０との間に、プラズマ発生基板２１０の内部に設けられたチャンネル２１３を隔てる隔壁２１２の少なくとも１つと交差して壁状スペーサ２２３が設けられている。この壁状スペーサ２２３は、プラズマ発生基板２１０の隔壁２１２と同様の基板間隙保持手段としての機能を有する。

【００１４】

【発明が解決しようとする課題】しかしながら、上述した広視野角化ＬＣＤやプラズマアドレス型の液晶表示装置においては、以下のような問題点があった。

【００１５】特開平６－３０１０１５号公報および特開平７－１２０７２８号公報で提案されている広視野角化ＬＣＤ（ＡＳＭモード）は、正の誘電異方性を有する液晶材料と光硬化樹脂との混合物から、相分離を利用して高分子壁と液晶領域とを形成するものであり、複雑な温度制御を必要とする相分離工程を使用するので、製造が難しい。また、形成された軸対称配向状態が不安定であり、特に高温において信頼性に欠けるという問題があった。

【００１６】特願平８－３４１５９０号で提案している広視野角化ＬＣＤにおいては、表示媒体中に、区画壁と、その上には選択的に形成される柱状突起との２層構造を設けている。上記構造を形成するには、２回のパターニング工程を必要とするため、製造コストが高くなり、また製造タクト時間が長くなるという問題点があった。また、精密なアライメントが要求されるため、アライメントマージンが必要となったり、歩留りが低下するという問題点があった。

【００１７】特開平１－２１７３９６号や特開平４－２８５９３１号に開示されているプラズマアドレス型の液晶表示装置においては、セル厚を一定に維持するためにビーズを使用した場合、ビーズの基板などに対する接触面積が小さいため、セル作製時および真空注入による表示媒体の注入時に、ビーズとの接触部分に応力が集中し、チャンネルと表示媒体とを隔てる薄板ガラスが破壊する可能性があった。

【００１８】特開平９－１９７３８４号に開示されているプラズマアドレス型の液晶表示装置においては、液晶材料と光硬化樹脂との混合物から、相分離を利用して高分子壁と液晶領域とを形成するものであり、複雑な温度制御を必要とする相分離工程を使用するので、製造が難しい。また、形成された軸対称配向状態が不安定であり、特に高温において信頼性に欠けるという問題があった。

【００１９】特願平８－３４１５９０号で提案している広視野角化ＬＣＤにおいては、区画壁が絵素領域を実質的に包囲するように格子状に形成されている。また、特開平９－１９７３８４号に開示されているプラズマアドレス型の液晶表示装置においては、壁状スペーサが隔壁と交差するように形成されている。また、前者の特願平８－３４１５９０号では区画壁が形成されてから液晶セルに液晶材料を注入し、後者の特開平９－１９７３８４号では壁状スペーサ形成されてから液晶セルに液晶材料を注入する。このため、区画壁または壁状スペーサが液晶材料を注入する際の障害となり、液晶材料の注入速度を低下させる原因となっていた。そのため、注入時間が増大して製造コストが高くなるという問題点があった。

【００２０】一般に、液晶表示装置に用いられている液晶材料は数種の液晶材料からなる混合物であり、このような液晶材料の混合物を液晶セルに注入する際には、混合物の各成分の移動速度や分配係数に差があることにより、混合物の混合比に基づき、液晶セルの液晶材料の注入口からの距離に応じた面内分布が生じる、いわゆる「クロマト現象」が起きる。それにより、混合物の混合比に基づく液晶セルの面内分布に起因する表示むらが起こる。前述の「クロマト現象」は、液晶材料の注入速度が減少するとより顕著になり、表示むらが増大し、液晶表示装置の表示品位が低下するという問題点があった。

【００２１】特に、特願平８－３４１５９０号で提案されている、高分子材料からなる軸対称配向固定層を設ける方法においては、液晶材料に加えて、光硬化性材料も含ませているため、「クロマト現象」が生じ易くなり、表示むらがより増大し、液晶表示装置の表示品位がより低下するという問題点があった。

【００２２】本発明は、このような従来技術の課題を解決すべくなされたものであり、「クロマト現象」を生じ難くして表示品位の向上を図れ、しかも、広視野角特性に優れると共にセル厚を一定に維持することができる液晶表示装置を提供することを目的とする。

【0023】
【課題を解決するための手段】本発明の液晶表示装置は、各々電極を有する一対の基板と、該一対の基板に挟持された液晶層とを有している液晶表示装置において、該液晶層は負の誘電異方性を有する液晶分子からなり、両基板に達するように柱状スペーサが設けられており、該一対の基板の液晶層に接する表面および該柱状スペーサの表面に垂直配向層が形成され、該液晶層は絵素毎に少なくとも一つの該柱状スペーサにて規定される絵素領域を有するとともに、該液晶層への電圧無印加時には該液晶分子が該一対の基板の表面に対し略垂直に配向し、該液晶層への電圧印加時には該液晶分子が該絵素領域毎に軸対称状に配向し、そのことにより上記目的が達成される。
【0024】本発明の液晶表示装置において、前記一対の基板の少なくともどちらか一方の基板の前記液晶層に接する表面に、高分子材料からなる軸対称配向固定層が形成されている構成とすることができる。
【0025】本発明の液晶表示装置において、対向配設された基板および誘電体シートと、これらの間に形成された隔壁とで囲まれたライン状空間が放電チャンネルとなっているプラズマ発生基板と、該プラズマ発生基板の該誘電体シートに対して一定の間隙を保持して対向配設され、かつ、該ライン状の放電チャンネルと交差するようライン状の信号電極が形成された第２の基板と、該誘電体シートと該第２の基板との間に液晶層とを有している、プラズマアドレス型液晶表示装置において、該液晶層は負の誘電異方性を有する液晶分子からなり、該誘電体シートと該第２の基板とに達するように柱状スペーサが設けられており、該誘電体シートおよび該第２の基板の液晶層に接する表面および該柱状スペーサの表面に垂直配向層が形成され、該液晶層は絵素毎に少なくとも一つの該柱状スペーサにて規定される絵素領域を有するとともに、該液晶層への電圧無印加時には該液晶分子が該誘電体シートと該第２の基板の表面に対し略垂直に配向し、該液晶層への電圧印加時には該液晶分子が該絵素領域毎に軸対称状に配向し、そのことにより上記目的が達成される。
【0026】本発明の液晶表示装置において、前記第２の基板および前記誘電体シートの少なくともどちらか一方の前記液晶層に接する表面に、高分子材料からなる軸対称配向固定層が形成されている構成とすることができる。
【0027】本発明の液晶表示装置において、前記柱状スペーサが、前記絵素領域の周囲の少なくとも４箇所に配設されている構成とすることができる。
【0028】本発明の液晶表示装置において、前記柱状スペーサが、前記絵素領域の各々に対応するものを点対称または線対称の位置に配して形成されている構成とすることができる。
【0029】本発明の液晶表示装置において、前記柱状スペーサが、前記絵素領域の角部もしくは四辺に接するように、または角部および四辺の両方のうちの任意の箇所に接するように形成されている構成とすることができる。
【0030】本発明の液晶表示装置において、前記柱状スペーサの該一対の基板と水平な方向での断面形状が、四角形、四角形の角を丸めた形、十字形、Ｔ字形、くの字形、円形および楕円形のいずれかである構成とすることができる。
【0031】前記柱状スペーサが、前記絵素領域の角部と、四辺に接しながら四辺のそれぞれを２等分もしくは３等分する箇所に配設されていることが好ましい。
【0032】前記柱状スペーサの前記一対の基板と水平な方向での断面形状は、四角形、四角形の角を丸めた形、円形、および半円形のいずれかであり、該柱状スペーサに外接する四角形が互いに隣接する絵素の間に収まる大きさであり、かつ、該柱状スペーサの短い方の一辺が５μｍよりも長いことが好ましい。
【0033】前記柱状スペーサを複数有し、互いに隣接する該柱状スペーサの間隔をＤ、該柱状スペーサの断面形状が四角形の場合、該四角形の一辺の長さをｄｓとし、該柱状スペーサの断面形状が円形の場合、該円形の直径をｄｓとしたとき、長さの比ｙ（＝Ｄ／ｄｓ）が、
$0.1 \leq y \leq 4.49e^{-0.0607ds} + 1.5$
の関係にあることが好ましい。
【0034】前記柱状スペーサが、前記絵素領域の角部を除いた四辺に接するように配設されてもよい。
【0035】前記柱状スペーサの前記一対の基板と水平な方向での断面形状は、長方形または長方形の角を丸めた形であり、絵素に対して垂直な辺は５μｍよりも長く、隣接する絵素間の長さよりも短く、絵素に対して平行な辺の長さが、絵素の各辺の長さの２０％よりも長く９９％よりも短い構成することが好ましい。
【0036】以下、本発明の作用について説明する。
【0037】本発明にあっては、垂直配向膜の存在により、その垂直配向膜と接する液晶分子が垂直配向膜に垂直に配向する。このとき、絵素領域の周囲の少なくとも４箇所に、柱状スペーサが配置されていることが好ましい。さらに、前記４箇所が一絵素領域から見て、点対称または線対称の位置に配置されているのが好ましい。例えば、絵素領域の四隅に配置することができる。このような配置の柱状スペーサによって軸対称配向する絵素領域を規定することができると共に、柱状スペーサによって液晶セルのセル厚を一定に保持させることができる。また、柱状スペーサが各絵素毎における絵素領域の一部に配されているので、柱状スペーサが液晶材料を注入する際の障害物とならないため、液晶材料の注入速度を低下させることがない。そのため、「クロマト現象」が生じ難くなり、「クロマト現象」に起因する表示むらを減

少でき、液晶表示装置の表示品位を向上させることができる。

【００３８】また、軸対称配向固定層を少なくともどちらか一方の基板に形成した場合には、その軸対称配向固定層にて軸対称配向となっている絵素領域の軸位置を所定の位置に一致させることが可能となり、安定した軸対称配向が得られる。本発明で言う軸対称配向固定層は、例えば柱構造を有するセル内に、液晶材料と光硬化性モノマーとの混合物を注入し、該セルに軸対称配向を電圧印加により発生させ、その後に光照射して配向固定することにより形成される。

【００３９】また、本発明のアラズマアドレス型の液晶表示装置にあっては、第２の基板や誘電体シートに対する柱状スペーサの接触面積が大きいため、貼り合わせ工程等のセル作製時及び液晶材料の注入時に、誘電体シートとしての薄板ガラスと柱状スペーサとの接触部分に応力が集中することを抑制できるため、誘電体シートである薄板ガラスが破壊することを防止することができる。また、液晶層の各絵素毎における絵素領域の周囲の少なくとも４箇所に柱状スペーサが配置されているので、柱状スペーサによって軸対称配向する絵素領域を規定することができると共に、柱状スペーサによって液晶セルのセル厚を一定に保持させることができる。また、柱状スペーサが各絵素毎における絵素領域の一部に配されているので、柱状スペーサが液晶材料を注入する際の障害物とならないため、液晶材料の注入速度を低下させることがない。そのため、「クロマト現象」が生じ難くなり、「クロマト現象」に起因する表示むらを減少でき、液晶表示装置の表示品位を向上させることができる。

【００４０】また、第２の基板および誘電体シートの少なくともどちらか一方に、軸対称配向固定層を形成した場合には、その軸対称配向固定層にて軸対称配向となっている絵素領域の軸位置を所定の位置に一致させることが可能となり、安定した軸対称配向が得られる。

【００４１】また、本発明のプラズマアドレス型の液晶表示装置にあっては、液晶層が負の誘電異方性を有する液晶分子からなり、かつ、プラズマ発生基板および第２の基板の各々の液晶層に接する表面に垂直配向層が形成されており、電圧無印加時には液晶分子が該一対の基板に対して略垂直に配向し、電圧印加時には液晶分子が各絵素領域毎に軸対称状に配向する構成としているので、絵素領域毎に液晶分子が軸対称配向した視角特性の優れた高コントラストの表示が得られる。

【００４２】また、本発明の液晶表示装置における柱状スペーサの断面形状としてはどのような形状であってもよいが、その一例として、例えば図２１（ａ）～（ｄ）に示すように断面形状が十字形、四角形、Ｔ字形、くの字形、円形または楕円形のものなどを使用することができる。このような、柱状スペーサは、後述する実施形態で述べるように、１回のパターニング工程で形成することができるので、複数のパターニング工程で必要となる精密なアライメントが不要となり、歩留まりが向上するとともに、製造工程を簡略化し、製造タクト時間を短縮することができるため、製造コストを低く抑えることが可能となる。

【００４３】

【発明の実施の形態】以下に、本発明の実施形態につき図面に基づいて具体的に説明する。

【００４４】なお、本発明でいう「軸対称配向」とは、渦巻き状配向、同心円状配向及び放射状配向も含む。軸対称状配向とは、その一つの形態としては、たとえば、一方の基板上で渦巻き状に、他方の基板上で逆方向の渦巻き状に液晶分子が配向している状態がある。他の形態としては、同心円状や放射状などの液晶分子方向のものを同種または異種のものを組み合わせ、上下の基板上で互いに直交した配向方向を有する状態のものがある。更に、他の形態として、微小領域内で、例えば、４方向に配向しているが巨視的には全方位的に配向している形態を含む。

【００４５】また、「絵素」は、一般に、表示を行う最小単位として定義される。本願明細書において用いられる「絵素領域」という用語は、「絵素」に対応する表示素子の一部の領域をさす。ただし、縦横比が大きい絵素（長絵素）の場合、一つの長絵素に対して、複数の絵素領域を形成してもよい。絵素に対応して形成される絵素領域の数は、軸対称配向が安定に形成され得る限り、可及的に少ない方が好ましい。

【００４６】（実施形態１）図１は、本実施形態に係る液晶表示装置の具体的構成を模式的に示す図である。図１（ａ）は、その液晶表示装置を示す断面図（図１（ｂ）のＸ－Ｘ線による断面図）であり、図１（ｂ）はその要部を示す平面図である。

【００４７】この液晶表示装置は、液晶層９を挟んで一対の基板、例えばガラス基板１とガラス基板２とが所定の間隙を持って対向配設されており、両基板１、２間の周囲には液晶層９を封止するシール材（図示せず）が設けられ、また、液晶層９中の所定箇所には柱状スペーサ７が両基板１、２に達するように設けられている。

【００４８】前記ガラス基板２の液晶層９側の内表面には、例えばＩＴＯのような透明な導電膜からなる信号電極４がストライプ状に形成されており、更に、その上を覆って基板２のほぼ全面にポリイミド等の垂直配向層５ａが形成されている。

【００４９】また、前記ガラス基板１の液晶層９側の内表面には、カラーフィルタ（図示せず）及びブラックマトリックス（図示せず）が形成され、その上に例えばＩＴＯのような透明な導電膜からなる信号電極３がストライプ状に形成されており、この信号電極３は、前記信号電極４とは交差する状態で設けられ、信号電極３と信号電極４との交差部分で絵素が構成される。前記絵素６に

対応して、絵素領域８が形成される。前記カラーフィルタ（図示せず）は、各絵素毎に異なるＲ、Ｇ、Ｂ用の着色層を有するものであり、また、ブラックマトリックス（図示せず）はカラーフィルタ（図示せず）の各着色層の間に配して形成されている。このガラス基板１の上には、前記絵素領域８の四隅に相当する角に前記柱状スペーサ７が配置されている。この状態のガラス基板１の内表面に、具体的には柱状スペーサ７の側面および柱状スペーサ７の非形成部分のガラス基板１上に、ポリイミド等の垂直配向層５ｂが形成されている。なお、垂直配向層５ｂは、柱状スペーサ７の上表面（前記垂直配向膜５ａと接する表面）にも形成してもよい。

【００５０】（基本動作）図２を参照しながら、本発明の液晶表示装置の動作原理を説明する。図２の（ａ）及び（ｂ）は電圧無印加時の状態を示し、（ｃ）及び（ｄ）は電圧印加時の状態を示し、（ａ）及び（ｃ）は一絵素領域の断面図（図１（ｂ）のＡ－Ａ´線による断面図）、（ｂ）及び（ｄ）は上面をクロスニコル状態の偏光顕微鏡で観察した結果を示す。ただし、図１と同一部分には同一符号を付している。

【００５１】電圧無印加時には、図２（ａ）に示すように液晶分子９ａは、垂直配向層５ａ、５ｂの配向規制力によって、基板１、２に垂直な方向に配向している。電圧無印加状態の絵素領域８をクロスニコル状態の偏光顕微鏡で観察すると、図２（ｂ）に示したように、暗視野を呈する（ノーマリーブラックモード）。電圧を印加すると、負の誘電異方性を有する液晶分子９ａに、液晶分子の長軸を電界の方向に対して垂直に配向させる力が働くので、図２（ｃ）に示すように基板１、２に垂直な方向から傾く（中間調表示状態）。この状態の絵素領域８をクロスニコル状態の偏光顕微鏡で観察すると図２（ｄ）に示すように、偏光軸から４５°方向に消光パターンが観察される。

【００５２】電圧印加直後には、絵素領域８内の大多数の液晶分子９ａの倒れていく方向は一義的に決まらないため、一絵素領域８内に、複数の液晶ドメイン（連続的に配向した領域：ディスクリネーションラインの発生が無い領域）が発生し、各々の液晶ドメイン内では液晶分子９ａが軸対称配向中心軸を中心に軸対称配向している過渡的な状態となる。さらに電圧を印加し続けると、複数の液晶ドメインが一つに融合し、絵素領域８内の液晶分子９ａが、一つの軸対称状配向中心軸を中心として軸対称配向状態を示す安定した状態になる。図２（ｄ）は中間調表示状態の電圧を印加した場合に、軸対称状配向中心軸１１を中心として液晶分子９ａが軸対称配向している様子を示している。

【００５３】（絵素領域を規定する柱状スペーサ）本発明の液晶表示装置は絵素領域８の周囲に柱状スペーサ７が配置されている。この柱状スペーサ７がなく、電圧印加時の液晶分子９ａの配向を規制する因子が液晶層に存在しない場合、電圧が印加されても、個々の液晶分子９ａの倒れていく方向は一義的に決まらないため、液晶ドメイン（連続的に配向した領域：ディスクリネーションラインの発生が無い領域）が形成される位置または、大きさを規定されないので、ランダム配向状態になってしまい、中間調表示においてざらついた表示となる。

【００５４】柱状スペーサ７を形成することにより、軸対称配向を呈する絵素領域８の位置および大きさが規定される。柱状スペーサ７は電圧印加時の液晶分子９ａの配向を規制するために形成されている。電圧が印加されると、柱状スペーサ７側面に垂直配向層５ｂが形成されているため、柱状スペーサ７近傍の液晶分子９ａは、基板１、２の表面に平行な平面内において、柱状スペーサ７の表面に対して垂直方向に倒れていく。続いて、前記柱状スペーサ７近傍の液晶分子９ａに隣接する液晶分子９ａが、前記柱状スペーサ７近傍の液晶分子９ａの倒れた方向とほぼ同じ方向に倒れていく。言い換えると、隣接する液晶分子９ａ同士は、できるだけ液晶分子９ａのダイレクター（分子長軸の方向）が連続するような配向状態をとろうとする。配向規制因子である柱状スペーサ７から遠ければ遠いほど液晶分子９ａは柱状スペーサ７の配向規制力の影響を受け難い。従って、柱状スペーサ７から遠い位置にある液晶分子９ａは、電圧印加直後には、倒れていく方向は一義的に決まらないため、一絵素領域８内に、液晶分子９ａのダイレクターが不連続になる点、即ち、ディスクリネーションラインが発生し、複数の液晶ドメインが存在する過渡的な状態となる。さらに電圧を印加し続けると、液晶ドメインと液晶ドメインの境界であるディスクリネーションライン、即ち、液晶分子９ａのダイレクターが不連続になる点において、外場（例えば電界）の力により、隣接する液晶分子９ａ同士のダイレクターが連続になるように、配向状態を変え、より安定な状態へ移行しようとする。ある程度電圧を印加し続けてやると、複数の液晶ドメインが一つに融合し、最終的には、絵素領域８内の液晶分子９ａは、一つの軸対称状配向中心軸１１を中心として軸対称配向状態を示すようになる。

【００５５】柱状スペーサ７の断面形状は、電圧印加時の液晶分子９ａの配向状態に影響を及ぼす。柱状スペーサ７の断面の辺の向きは、電圧印加時に液晶分子９ａが基板１、２に垂直な方向から傾いていく方向に影響を及ぼす。これは、電圧が印加されると、柱状スペーサ７側面に垂直配向層５ｂが形成されているため、柱状スペーサ７近傍の液晶分子９ａは、基板１、２の表面に平行な平面内において、柱状スペーサ７の表面に対して垂直方向に倒れて行く。直線形状の辺を有している方が好ましい。さらには、柱状スペーサ７の断面形状としては、例えば十字形、四角形、Ｔ字形、くの字形が挙げられる。必ずしも辺の形状が直線状でなくてもよく、例えば円形や楕円形であってもよい。

【００５６】柱状スペーサ７の配置・配列は、絵素領域８の位置や大きさを規定するとともに、絵素領域８内の液晶分子９ａが電圧印加時に軸対称配向状態を示すようになるかどうかに影響を及ぼす。絵素領域８の位置や大きさを規定するには、絵素領域８の周囲の少なくとも４箇所に、柱状スペーサ７が配置されていることが好ましい。さらに、前記４箇所が一絵素領域８から見て、点対称または線対称の位置に配置されているのが好ましい。例えば、絵素領域８の四隅に配置することができる。柱状スペーサ７の断面の一辺が絵素領域８の四辺のどれかの一辺に接するように配置することができる。柱状スペーサ７の断面の一辺が曲線状の場合、曲線の外接線が絵素領域８の四辺のどれかの一辺にほぼ一致するように配置すればよい。また、例えば、断面形状が長方形の柱状スペーサ７を絵素領域８の四辺のどれかの一辺に接するように配置する場合には、長辺側を絵素領域８の四辺に平行になるように配置するのがより好ましい。

【００５７】

【実施例】以下、本発明の実施例を示すが、本発明はこれに限定されるものではない。

【００５８】（実施例１）図３を参照しながら、実施形態１の液晶表示装置の製造方法を説明する。

【００５９】図３は、この液晶表示装置の製造方法を示す工程図である。

【００６０】まず、工程（ａ）で、一方のガラス基板１の片面に、各絵素毎に異なるＲ、Ｇ、Ｂ用の着色層を有するカラーフィルタ（図示せず）及び各着色層の間に配するようにブラックマトリックス（図示せず）を形成する。更に、その上に信号電極３を形成する。

【００６１】次に、工程（ｂ）で、ガラス基板１の前記ブラックマトリックス（図示せず）上に柱状スペーサ７を形成する。柱状スペーサ７は、例えば、レジスト等の感光性樹脂を基板上に塗布し、フォトマスクを介してパターニングして形成する。したがって、この柱状スペーサ７は、１回のパターニング工程で形成することができる。よって、複数のパターニング工程で必要となる精密なアライメントが不要となり、歩留まりが向上するとともに、製造工程を簡略化し、製造タクト時間を短縮することができるため、製造コストを低く抑えることが可能となる。

【００６２】次に、工程（ｃ）で、柱状スペーサ７を形成したガラス基板１上に、垂直配向層５ｂを形成する。

【００６３】次に、工程（ｄ）で、もう一方のガラス基板２の片面に、信号電極４を形成する。

【００６４】次に、工程（ｅ）で、信号電極４を形成したガラス基板２上に、垂直配向層５ａを形成する。

【００６５】次に、工程（ｆ）で、ガラス基板１とガラス基板２とを貼り合わせる。

【００６６】次に、工程（ｇ）で、ガラス基板１とガラス基板２間に、液晶を真空注入方式等で注入して液晶層８を設ける。

【００６７】したがって、このようにして作製された液晶表示装置においては、垂直配向膜５ａ、５ｂの存在により、その垂直配向膜５ａ、５ｂと接する液晶分子９が垂直配向膜５ａ、５ｂに垂直に配向する。このとき、液晶層８の各絵素毎における絵素領域の角に柱状スペーサ７が配置されているので、柱状スペーサ７によって軸対称配向する絵素領域を規定することができると共に、柱状スペーサ７によって液晶セルのセル厚を一定に保持させることができる。また、柱状スペーサ７が各絵素毎における絵素領域の角に配されているので、柱状スペーサが液晶材料を注入する際の障害物とならないため、液晶材料の注入速度を低下させることがない。そのため、「クロマト現象」が生じ難くなり、「クロマト現象」に起因する表示むらの発生を減少でき、液晶表示装置の表示品位を向上させることができる。

【００６８】（実施例２）図４は、本実施形態１の変形例である。図４（ａ）はその液晶表示装置を示す断面図｛図４（ｂ）のＹ－Ｙ線による断面図｝であり、図４（ｂ）はその要部を示す平面図である。

【００６９】この図４の液晶表示装置においては、各絵素毎、つまり各絵素領域８毎に、一方の基板１に軸対称配向固定層１０が設けられ、その上に垂直配向膜５ｂが形成されている。

【００７０】前記軸対称配向固定層１０は、柱状スペーサ７の上から基板１側に向いて徐々に厚みを増大し、柱状スペーサ７の基板１側の端部近傍で厚みを最大とした後、その端部から遠ざかるに伴って基板１上で厚みを徐々に減少するように形成されている。したがって、この軸対称配向固定層１０の最底部が各絵素の中心に位置する状態となり、これに伴って、軸対称配向となっている各絵素領域８の軸位置が、軸対称配向固定層１０の最底部に応じた位置になる。

【００７１】したがって、この図４に示す液晶表示装置においては、軸対称配向の軸位置を軸対称配向固定層１０により所定の位置に制御することが可能となる。

【００７２】なお、上述した図１や図４に示した液晶表示装置は、ストライプ状の両信号電極が対向する部分で絵素が構成される単純マトリクス型の液晶表示装置を例に挙げているが、本発明はこれに限らず、アクティブマトリクス型の液晶表示装置にも適用できる。そのアクティブマトリクス型の液晶表示装置は、例えば、一方の基板上に、薄膜トランジスタ（ＴＦＴ）などのスイッチング素子と、そのスイッチング素子にゲート信号やソース信号を送る２種類の信号電極と、前記スイッチング素子を介して送られてきた信号にて駆動されるマトリクス状の絵素電極とを有し、他方の基板上にその基板のほぼ全面に対向電極が形成された構成のものである。

【００７３】以下の実施例３から実施例１０では、実施形態１で用いられる柱状スペーサの断面形状や配置の更

なる例を説明する。

【0074】（実施例3）図3に示したように、コーニング社製7059ガラス基板1，2の上に、100nmの厚みの透明電極3，4を形成し、さらにITO3の上にJCR BLACK535（JSR社製）をスピンコート法で4．5μmの膜厚になるように塗布し、ホットプレート上で80℃／5分間加熱した。図5に示すような100μm角の絵素領域を囲むように絵素領域の四隅と四辺の中央に、25μm角の断面形状の柱状スペーサ7が形成できるようなマスクを用い、マスク越しにコンタクト露光を40秒行った。露光時の照度は365nmで10mW／cm²であった。これを専用現像液CD－200CR（50倍希釈、25℃）で60秒現像し、純水シャワーで60秒間リンスを行った後、220℃の循環オーブンで30分間ポストベークを行い柱状スペーサ7を形成した。

【0075】両ガラス基板のITOが形成された側に垂直配向膜JALS－204（JSR社製）を80nmの膜厚で塗布し、180℃で1時間ポストベークを行い配向膜層5a，5bを作製して、両ガラス基板1、2をシール剤を介して貼り合わせた。

【0076】誘電異方性が負の液晶（△ε：－4．0、△n＝0．08、セルギャップ4．5μmで90度ツイストとなるようにカイラル剤を添加）を先のセルに注入してクロスニコル下で偏光顕微鏡観察を行った。電圧を基板間に印加すると、図6に示すように絵素領域の中央から四辺に向かって消光模様が観察され、軸対称状に液晶分子が配向していた。

【0077】（実施例4）実施例3と同様にガラス基板にJCR BLACK535（JSR社製）を6μmの膜厚になるようにスピンコートし、ホットプレート上で80℃／5分間加熱した。図7および図8に示すような100μm角の絵素領域を囲むように絵素領域の四隅と辺の中央（辺を2等分する点）および／または辺を3等分する点上に柱状スペーサが来るように設計したマスクを用いて、実施例3と同様に露光、現像、焼成を行い柱状スペーサ7を形成し、実施例3と同様に配向膜形成、液晶材料注入を行った。クロスニコル下で電圧を印加しながら偏光顕微鏡観察を行ったところ、図9および図10に示すように絵素領域の中央から四辺に向かって消光模様が観察され、液晶分子は軸対称状に配向していた。

【0078】（実施例5）実施例3と同様にガラス基板にJCR BLACK535（JSR社製）を6μmの膜厚になるようにスピンコートし、ホットプレート上で80℃／5分間加熱した。図11に示すように、100μm角の絵素領域を囲むように絵素領域の四辺の四隅を除く辺に柱状スペーサが来るように設計したマスクを用いて、実施例3と同様な露光、現像、焼成を行い柱状スペーサ7を形成し、実施例3と同様な配向膜形成、液晶材料注入を行った。クロスニコル下で電圧を印加しながら偏光顕微鏡観察を行ったところ、図12に示すように絵素子領域の中央から四辺に向かって消光模様が観察され、液晶分子は軸対称状に配向していた。

【0079】（実施例6）コーニング社製7059ガラス基板1の上にITOからなる厚み100nmの透明電極3を形成し、さらにこの上にに膜厚が5μmになるようにV259－PA（新日鐵化学社製）をスピンコート法で塗布した。ホットプレート上で100℃／3分間加熱した後に循環オーブンで80℃／10分間さらに加熱した。図13のように100μm×100μm角の絵素領域40を有してその周囲に配設される四角形の柱状スペーサ7の隣接する絵素の辺に垂直な方向の長さがaとなるようなマスクを用い、コンタクト露光を120秒行った。露光時の照度は365nmで10mW／cm²であった。これを0．4％－K_2CO_3．aqで150秒現像し、純水シャワーで120秒間リンスを行った後、240℃の循環オーブンで1時間ポストベークを行い柱状スペーサ7を形成した。垂直配向膜JALS－204（JSR社製）を80nmの膜厚で塗布し、180℃で1時間ポストスペークを行い配向膜層5aを作製した。

【0080】一方、100nm厚のITOからなる透明電極4の付いたガラス基板2の上にも同じ垂直配向膜JALS－204を80nmの膜厚になるように塗布して配向膜層5bを作製して両ガラス基板1，2をシール剤を介して貼り合わせた。

【0081】誘電異方性が負の液晶（△ε＝－4．0、△n＝0．08、セルギャップ5μmで90度ツイストとなるようにカイラル剤を添加）を先のセルに注入してクロスニコル下で偏光顕微鏡観察を行った。

【0082】絵素に垂直な方向の長さaがブラックマトリクスの線幅bよりも大きいと、ブラックマトリクスから柱状スペーサがはみ出してしまい、絵素領域内にスペーサが侵入し、開口率を低下させてしまう。絵素に垂直な方向の長さaが大きい場合には電圧を基板間に印加すると絵素毎に液晶分子は軸対称状に配向するが、aの値が5μmを下回ると軸対称状の配向が得られなかった。

【0083】なお、本実施例における柱状スペーサの断面形状は、実質的に四角形であれば良く、四角形の角を丸めた形でもよい。このことは、実施例において例示するすべての断面形状についていえる。特に、フォトリソグラフィ工程等の加工精度で、形状が多少変化しても本発明の効果は得られる。

【0084】（実施例7）コーニング社製7059ガラス基板1の上にITOからなる厚み100nmの透明電極3を形成し、さらにこの上にに膜厚が5μmになるようにV259－PA（新日鐵化学社製）をスピンコート法で塗布した。ホットプレート上で100℃／3分間加熱した後に循環オーブンで80℃／10分間さらに加熱した。図14のように100μm×100μm角の絵素領域40を有してその周囲に配設される円形の柱状スペ

ーサ7の直径がcとなるようなマスクを用い、実施例6と同条件で露光、現像、焼成を行い柱状スペーサ7を形成した。さらに実施例6と同条件で配向膜層を形成し両基板を貼り合わせてセルを作製した。

【0085】誘電異方性が負の液晶（△ε＝－4．0、△n＝0．08、セルギャップ5μmで90度ツイストとなるようにカイラル剤を添加）を先のセルに注入してクロスニコル下で偏光顕微鏡観察を行った。

【0086】ブラックマトリクスの線幅bに対して円形の柱状スペーサ7の直径cがc＞bとなると、ブラックマトリクスから柱状スペーサがはみ出してしまい、開口率を低下させてしまう。cが大きい場合には電圧を基板間に印加すると絵素毎に液晶分子は軸対称状に配向するが、cの値が5μmを下回ると軸対称状の配向が得られなかった。

【0087】（実施例8）コーニング社製7059ガラス基板1の上にITOからなる厚み1,00nmの透明電極3を形成し、さらにこの上にに膜厚が5μmになるようにV259－PA（新日鐵化学社製）をスピンコート法で塗布した。ホットプレート上で100℃／3分間加熱した後に循環オーブンで80℃／10分間さらに加熱した。図15のように100μm×100μm角の絵素領域40を有してその周囲に配設される半円形の柱状スペーサ7の半径がeとなるようなマスクを用い、実施例6と同条件で露光、現像、焼成を行い柱状スペーサ7を形成した。さらに実施例6と同条件で配向膜層を形成し両基板を貼り合わせてセルを作製した。

【0088】誘電異方性が負の液晶（△ε＝－4．0、△n＝0．08、セルギャップ5μmで90度ツイストとなるようにカイラル剤を添加）を先のセルに注入してクロスニコル下で偏光顕微鏡観察を行った。

【0089】ブラックマトリクスの線幅bに対して円形の柱状スペーサ7の半径eがe＞bとなると、ブラックマトリクスから柱状スペーサがはみ出してしまい、開口率を低下させてしまう。eが大きい場合には電圧を基板間に印加すると絵素毎に液晶分子は軸対称状に配向するが、eの値が5μmを下回ると軸対称状の配向が得られなかった。

【0090】（実施例9）コーニング社製7059ガラス基板1の上にITOからなる厚み100nmの透明電極3を形成し、この上に膜厚が5μmになるようにJNPC－43（JSR社製）をスピンコート法で塗布した。ホットプレート上で80℃／3分間加熱した後、図16（a）および（b）に示すように柱状スペーサ7の長さの一辺がdsであり、隣の柱状スペーサとの間隔Dが表1のように異なるマスクパターンを用いて、マスク越しにコンタクト露光を60秒行った。露光時の照度は365nmで10mW／cm²であった。これを現像液CD（15%希釈、25℃）で150秒現像し、純水シャワーで120秒間リンスを行った後、200℃の循環オーブンで1時間ポストベークを行い柱状スペーサ7を形成した。

【0091】垂直配向膜JALS－204（JSR社製）を80nmの膜厚で塗布し、180℃で1時間ポストベークを行い配向膜層5aを作製した。一方、100nm厚のITOからなる透明電極4の付いたガラス基板2の上にも同じ垂直配向膜JALS－204を80nmの膜厚になるように塗布して配向膜層5bを作製して両ガラス基板1，2をシール剤を介して貼り合わせた。

【0092】誘電異方性が負の液晶（△ε＝－4．0、△n＝0．08、セルギャップ5μmで90度ツイストとなるようにカイラル剤を添加）を先のセルに注入してクロスニコル下で偏光顕微鏡観察を行った。

【0093】

【表1】

【0094】液晶層に電圧を印加しながら偏光顕微鏡下で観察すると、ほぼ完全に軸対称状に液晶分子が配向するセルからあまり軸対称状に液晶分子が配向しないセルまであった。

【0095】絵素300個あたりで液晶分子が軸対称状に配向している絵素の割合が90%以上のセルは中間調でもほとんどざらつきが見られないので良品（○）、70%以上のセルは中間調でややざらつきが感じられるが用途により使用できるグレーゾーン（△）、軸対称状配向が得られる絵素の割合が70%未満で使用に適さないセル（□）と評価した。その結果を図17に示す。図17から明きからな様に、互いに隣接する柱状スペーサの間隔をD、柱状スペーサの断面形状が四角形の場合（図16（a））、該四角形の一辺の長さをdsとし、柱状

スペーサの断面形状が円形の場合（図１６（ｂ））、円形の直径をｄｓとし、ｄｓを横軸に長さの比ｙ（＝Ｄ／ｄｓ）を縦軸にとると、軸対称配向が得られる絵素の割合に応じて、この座標系のある範囲に集まっている。この実験結果から、液晶表示装置として使用できる範囲は、

$0.1 \leqq y \leqq 4.49e^{-0.0607ds}+1.5$

であり、より好ましくは

$0.5 \leqq y \leqq 4.49e^{-0.0607ds}+1.1$

であることが分かる。

【００９６】（実施例１０）コーニング社製７０５９ガラス基板１の上にＩＴＯからなる厚み１００ｎｍの透明電極３を形成し、この上に膜厚が５μｍになるようにＪＮＰＣ－４３（ＪＳＲ社製）をスピンコート法で塗布した。ホットプレート上で８０℃／３分間加熱した。図１８のように絵素に垂直方向の長さがａであり水平方向の長さがｂである柱状スペーサ７を作製できるように設計したマスクパターンを用いて、マスク越しにコンククト露光を４０秒行った。ここでは、絵素の一辺の長さが１００μｍであり、図のように隣接する絵素間の長さｃ（ブラックマトリクスの幅に相当）は２０μｍであった。露光時の照度は３６５ｎｍで１０ｍＷ／ｃｍ^{2}であった。これを現像液ＣＤ（１５％希釈、２５℃）で１５０秒現像し、純水シャワーで１２０秒間リンスを行った後、２００℃の循環オーブンで１時間ポストベークを行い柱状スペーサ７を形成した。ａの値がｃより大きいと柱状スペーサが絵素領域内に侵入するので、開口率の低下を引き起こしてしまう。

【００９７】垂直配向膜ＪＡＬＳ－２０４（ＪＳＲ社製）を８０ｎｍの膜厚で塗布し、１８０℃で１時間ポストスベークを行い配向膜層５ａを作製した。一方、１００ｎｍ厚のＩＴＯからなる透明電極４の付いたガラス基板２の上にも同じ垂直配向膜ＪＡＬＳ－２０４を８０ｎｍの膜厚になるように塗布して配向膜層５ｂを作製して両ガラス基板１、２をシール剤を介して貼り合わせた。誘電異方性が負の液晶材料（$\Delta\varepsilon=-4.0$、Δn：０．０８、セルギャップ５μｍで９０度ツイストとなるようにカイラル剤を添加）を先のセルに注入してクロスニコル下で偏光顕微鏡観察を行い、絵素３００個あたりで軸対称状に液晶分子が配向している絵素の割合（軸対称率）を算出した。結果を表２に示す。

【００９８】

【表２】

【００９９】上記表２中の×は液晶材料が注入できなかったこと又は液晶材料が注入されなかったために軸対称状の配向を形成することができなかったことを示している。上記の表２から、ｂ（柱状スペーサのその柱状スペーサが隣接する絵素の辺に平行な方向の長さ）が長いほど軸対称率は高く均一な液晶表示装置が作製できることがわかる。しかしながら、絵素の辺に平行な方向の長さｂが絵素の辺の長さｄと等しくなってしまうと液晶材料が注入できなくなってしまい、表示装置を形成できなくなるので、ｂ／ｄの値が９９％を越えないことが好ましい。

【０１００】一方絵素の辺に平行な方向の長さｂの値が小さくなっていき、一定の値を下回ると軸対称率が低下していく。液晶分子がすべての絵素で軸対称状に配向していれば問題はないが、この割合が減ってくると中間調でざらつきが見られるようになってしまう。軸対称率が７０％を下回ると使用に適さなくなってしまうのでｂ／ｄの値が２０％より大きいことが好ましい。軸対称率が９０％を越えると中間調でもほとんどざらつきは見られなく、注入に時間がかかりすぎるとタクトの問題も発生するので、これらを考慮すると、ｂ／ｄの値が４０％～９０％であることが更に好ましい。

【０１０１】（実施形態２）実施形態２は、プラズマアドレス型の液晶表示装置に適用した場合である。

【０１０２】図１９は、本実施形態に係るプラズマアドレス型の液晶表示装置の具体的構成を示す模式断面図である。

【０１０３】この液晶表示装置は、液晶層２９を挟んで一方側（図の上側）に透明なガラス等からなる基板２８を有し、他方側（図の下側）に誘電対シートとしての薄板ガラス２３と基板２４とが対向配設されたプラズマ発生基板２２を有する。プラズマ基板２２の基板２４と薄板ガラス２３との間には、ライン状に隔壁２７が形成され、この隔壁２７と、基板２４と、薄板ガラス２３とで囲まれた空間は、電離用ガスが封入されたライン状のチャンネル２５を構成する。各チャンネル２５内には、電離用ガスをイオン化するためのアノード電極Ａおよびカソード電極Ｋが設けられている。

【０１０４】一方、基板２８の液晶層２９側には、カラーフィルタ３３が実施形態１と同様の構成を設けられており、その上に、データ線としての透明電極３０が、ストライプ状に、かつ、ライン状のチャンネル２５に対して交差して、例えば垂直方向に配線されている。前記液晶層２９は、基板２８と薄板ガラス２３とに挟持されて

おり、基板２８と薄板ガラス２３との間のセル厚は、柱状スペーサ３７にて一定に維持されている。液晶層２９は、柱状スペーサ３７によって規定される複数の絵素領域２６が形成されている。なお、基板２８および薄板ガラス２３の液晶層２９側の表面には、図示しない配向膜が形成されている。また、基板２８、カラーフィルタ３３、透明電極３０および液晶層２９からなる部分は表示セル２１を構成する。

【０１０５】このように構成された液晶表示装置の一方側（図上側）に偏光板（不図示）が設けられ、他方側（図下側）に偏光板とバックライト（共に不図示）とが設けられている。

【０１０６】この液晶表示装置の製造方法は、図１に示す実施形態１の製造工程とほぼ同一であるが、本実施形態２においては、図３のガラス基板２の代わりに、図１９で示すプラズマ発生基板２２を用いる。このプラズマ発生基板２２の作製は、公知の方法により作製される。

【０１０７】このようにして作製された液晶表示装置においては、液晶層２９の各絵素毎における絵素領域２６の角に柱状スペーサ３７が配置されているので、柱状スペーサ３７によって軸対称配向する絵素領域２６を規定することができると共に、柱状スペーサ３７によって液晶セルのセル厚を一定に保持させることができる。また、柱状スペーサ３７が各絵素毎における絵素領域２６の角に配されているので、柱状スペーサ３７が液晶材料を注入する際の障害物とならないため、液晶材料の注入速度を低下させることがない。そのため、「クロマト現象」が生じ難くなり、「クロマト現象」に起因する表示むらを減少でき、液晶表示装置の表示品位を向上させることができる。

【０１０８】また、基板２８および誘電体シートとしての薄板ガラス２３の少なくともどちらか一方に、実施形態１と同様の軸対称配向固定層を形成した場合には、その軸対称配向固定層にて軸対称配向となっている絵素領域の軸位置を所定の位置に一致させることが可能となり、安定した軸対称配向が得られる。

【０１０９】なお、柱状スペーサ３７の配置については、図２０（ａ）～（ｃ）に示すように可及的にカラーフィルタ３３のブラックマトリックスの上であるようするのが好ましい。その理由は、柱状スペーサ３７とブラックマトリックスとの位置を揃えるのが光透過性の点で好ましく、表示面積の向上を図れるからである。

【０１１０】また、本実施形態２においては薄板ガラス２３および基板２８の各々の液晶層に接する表面に垂直配向層が形成されているので、液晶層２９の材料に負の誘電異方性を有する液晶を用いる場合には、電圧無印加時には液晶分子を基板に対して略垂直に配向させ、また、電圧印加時には液晶分子を各絵素領域毎に軸対称状に配向させることが可能となる。よって、絵素領域毎に液晶分子が軸対称配向した視角特性の優れた高コントラストの表示が得られる。

【０１１１】また、上下の偏光板の偏光軸を直交になるように配置されており、電圧ＯＦＦ状態では、液晶分子は基板に垂直に配向しているため、偏光板を通して液晶パネルに入射した光は液晶パネルを透過せず、完全な黒表示ができるため、高コントラストが得られるという特徴がある。

【０１１２】なお、上述した実施形態１、２においては、柱状スペーサの断面形状としては図２１（ａ）に示す十字形のものを使用しているが、本発明において用いる柱状スペーサの断面形状はどのような形状であってもよく、その一例として、例えば図２１（ｂ）～（ｆ）に示すように断面形状が四角形、Ｔ字形、くの字形、円形または楕円形のものなどを使用することができる。また、実施形態１の実施例３から１０において例示した柱状スペーサの断面形状や配置を実施形態２に適用できることは言うまでもない。

【０１１３】

【発明の効果】以上詳述したように本発明による場合には、柱状スペーサが各絵素毎における絵素領域の周囲の一部に配されているので、柱状スペーサが液晶材料を注入する際の障害物とならないため、液晶材料の注入速度を低下させることがなく、そのため、「クロマト現象」が生じ難くなり、「クロマト現象」に起因する表示むらを減少でき、液晶表示装置の表示品位を向上させることができる。また、垂直配向膜の存在により、その垂直配向膜と接する液晶分子を垂直配向膜に垂直に配向させることができ、このとき、絵素領域の周囲の少なくとも４箇所に柱状スペーサが配置されているので、柱状スペーサによって軸対称配向する絵素領域を規定することができると共に、柱状スペーサによって液晶セルのセル厚を一定に保持させることができる。

【０１１４】したがって、本発明によると、絵素領域毎に液晶分子が軸対称配向した視角特性の優れた高コントラストの液晶表示装置を提供することが可能となる。このため、本発明の液晶表示装置は、パーソナルコンピューター、ワードプロセッサ、アミューズメント機器、テレビジョン装置などの平面ディスプレイや、シャッター効果を利用した表示板、窓、扉、壁などに好適に用い得ることはもちろん、更には、例えばＨＤＴＶなどの高品位テレビ、ＣＡＤ用平面ディスプレーなどに利用できる大型平面表示装置にも適用できる。

【図面の簡単な説明】

【図１】（ａ）は本発明の実施形態１に係る液晶表示装置の具体的構成を模式的に示す断面図｛（ｂ）のＸ－Ｘ線による断面図｝であり、（ｂ）はその要部を示す平面図である。

【図２】（ａ）及び（ｂ）は電圧無印加時の状態を示し、（ｃ）及び（ｄ）は電圧印加時の状態を示し、（ａ）及び（ｃ）は一絵素領域の断面図（図１（ｂ）の

Ａ－Ａ´線による断面図）、（ｂ）及び（ｄ）は上面をクロスニコル状態の偏光顕微鏡で観察した結果を示す。

【図３】図１の液晶表示装置の製造方法を示す工程図（断面図）である。

【図４】（ａ）は本発明の実施形態１に係る他の液晶表示装置の具体的構成を模式的に示す断面図｛（ｂ）のＹ－Ｙ線による断面図｝であり、（ｂ）はその要部を示す平面図である。

【図５】実施例３で作製する液晶セルの柱状スペーサの配置を示す模式図である。

【図６】実施例３で作製した液晶セルの観察結果の模式図である。

【図７】実施例４で作製する液晶セルの柱状スペーサの配置を示す模式図である。

【図８】実施例４で作製する液晶セルの柱状スペーサの配置を示す模式図である。

【図９】実施例４で作製した液晶セルの観察結果の模式図である。

【図１０】実施例４で作製した液晶セルの観察結果の模式図である。

【図１１】実施例５で作製する液晶セルの柱状スペーサの配置を示す模式図である。

【図１２】実施例５で作製した液晶セルの観察結果の模式図である。

【図１３】実施例６で作製する液晶セルの柱状スペーサの配置を示す模式図である。

【図１４】実施例７で作製する液晶セルの柱状スペーサの配置を示す模式図である。

【図１５】実施例８で作製する液晶セルの柱状スペーサの配置を示す模式図である。

【図１６】実施例９で作製する液晶セルの柱状スペーサの配置を示す模式図である。

【図１７】軸対称状配向が得られる絵素の割合を、隣接する柱状スペーサの間隔をＤ、柱状スペーサの断面形状が四角形の場合の一辺の長さまたは柱状スペーサの断面形状が円形の場合の直径をｄｓとし、ｄｓを横軸に、長さの比ｙ（＝Ｄ／ｄｓ）を縦軸とする座標系で示したグラフである。

【図１８】実施例１０で作製する液晶セルの柱状スペーサの配置を示す模式図である。

【図１９】本発明の実施形態２に係るプラズマアドレス型の液晶表示装置を示す模式図（断面図）である。

【図２０】本発明の実施形態２に係るプラズマアドレス型の液晶表示装置における柱状スペーサと隔壁との位置関係を模式的に示す平面図である。

【図２１】本発明に好適に用いられる柱状スペーサの断面形状の一例を示す図である。

【図２２】従来の液晶表示装置を示す模式図であり、（ａ）は断面図であり、（ｂ）は平面図である。

【図２３】従来のプラズマアドレス型の液晶表示装置を示す模式図（断面図）である。

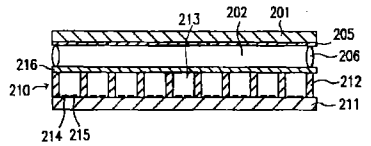
【図２４】従来の他のプラズマアドレス型液晶表示装置を示す模式図であり、（ａ）はその断面図であり、（ｂ）はその平面図である。

【図２５】従来の他のプラズマアドレス型液晶表示装置を示す模式図であり、（ａ）はその断面図であり、（ｂ）はその平面図である。

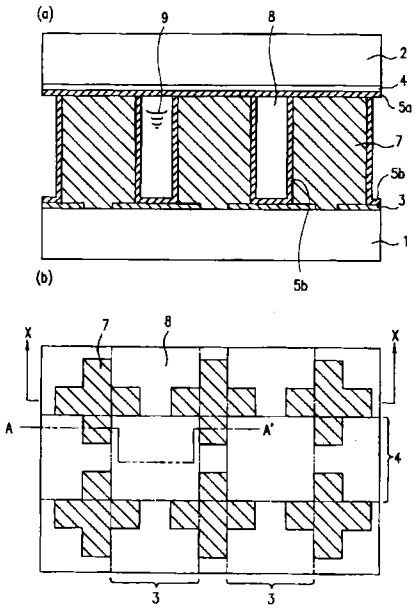
【符号の説明】

１、２　ガラス基板
３、４　信号電極
５ａ、５ｂ　垂直配向層
７　柱状スペーサ
８　液晶領域
９　液晶層
１０　軸対称配向固定層
２１　表示セル
２２　プラズマ発生基板
２３　薄板ガラス
２４、２８　基板
２５　チャンネル
Ａ　アノード
Ｋ　カソード
２７　隔壁
２９　液晶層
３０　透明電極
３３　カラーフィルタ
３７　柱状スペーサ
４０　絵素領域
４１　ブラックマトリクス

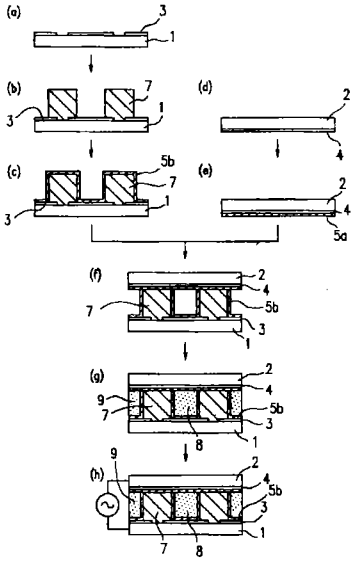
【図２３】



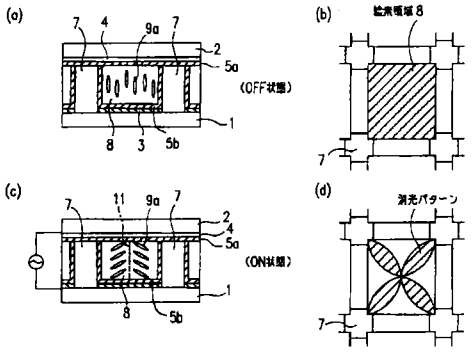
【図1】


(a)
9
8
2
4
5a
7
5b
3
1
5b
(b)
X
7
8
X
A
A'
4
3
3

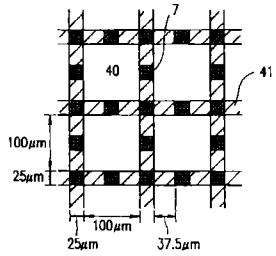
【図3】


(a)
3
1
(b)
7
3
1
(c)
5b
7
3
1
(d)
2
4
(e)
2
4
5a
(f)
2
4
7
5b
3
1
(g)
2
4
9
7
5b
3
8
1
(h)
9
2
4
5b
3
7
8
1

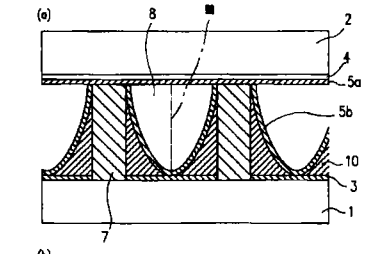
【図2】


(a)
7
4
9a
7
2
5a
(OFF状態)
1
8
3
5b
(b)
検索領域8
7
(c)
7
11
9a
7
2
4
5a
(ON状態)
1
8
5b
(d)
消光パターン
7

【図5】


7
40
41
100μm
25μm
100μm
25μm
37.5μm

【図4】



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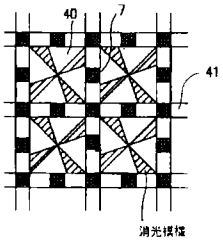

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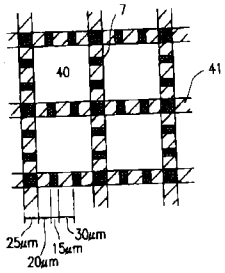

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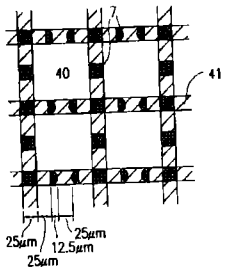
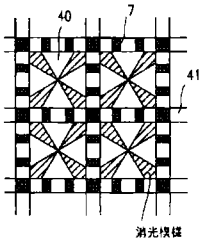


【図9】



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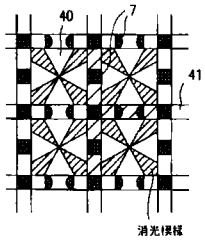

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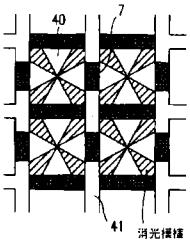
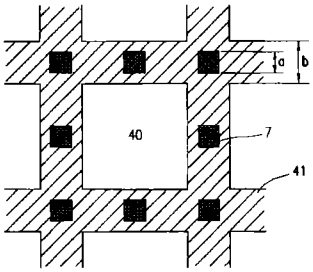
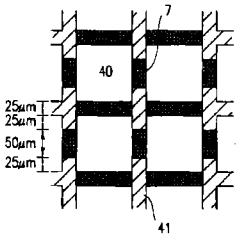


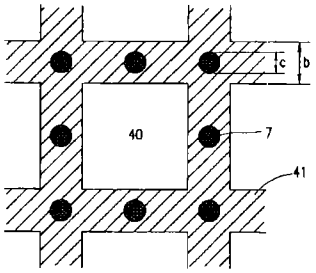
【図13】



【図11】



【図14】



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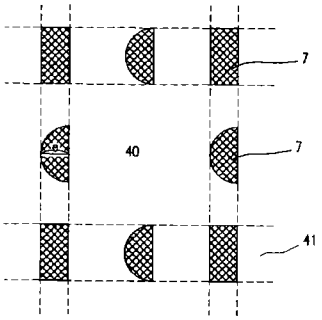

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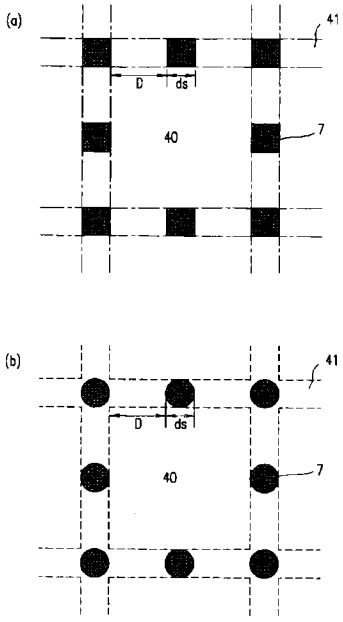

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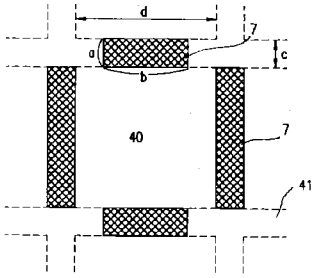

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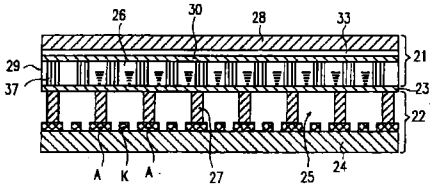

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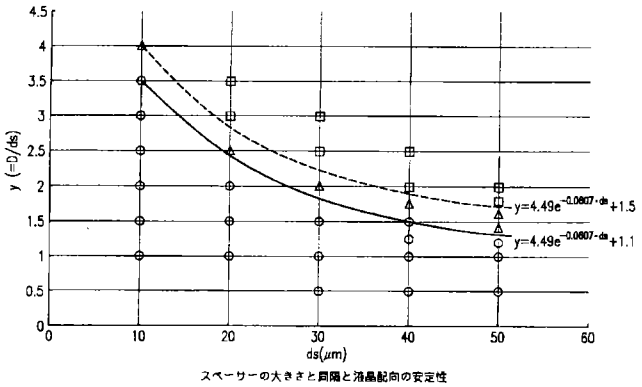
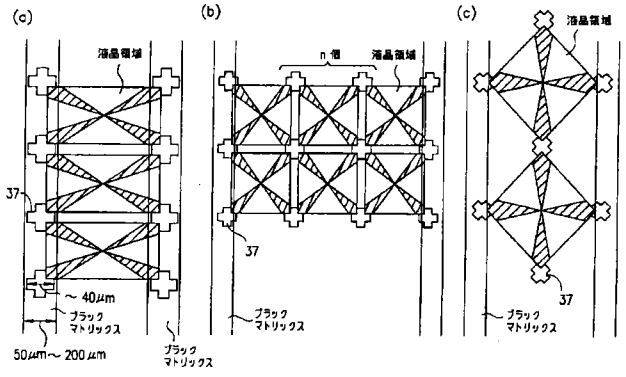


スペーサーの大きさと間隔と液晶配向の安定性

【図20】



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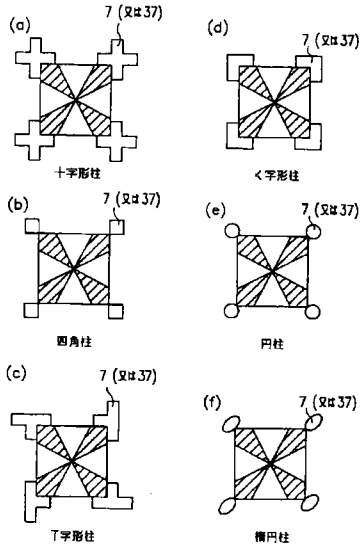
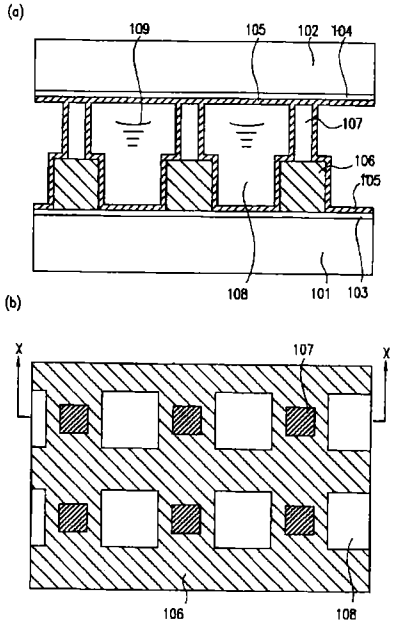
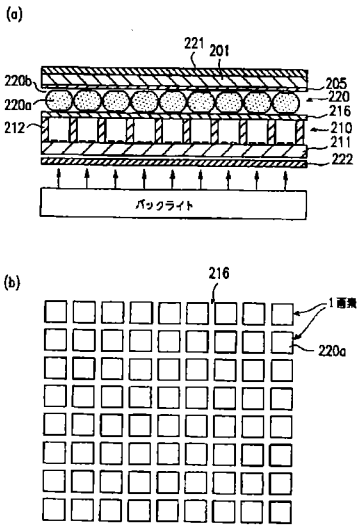

(a)
7（又は37）
十字形柱
(d)
7（又は37）
く字形柱
(b)
7（又は37）
四角柱
(e)
7（又は37）
円柱
(c)
7（又は37）
T字形柱
(f)
7（又は37）
楕円柱

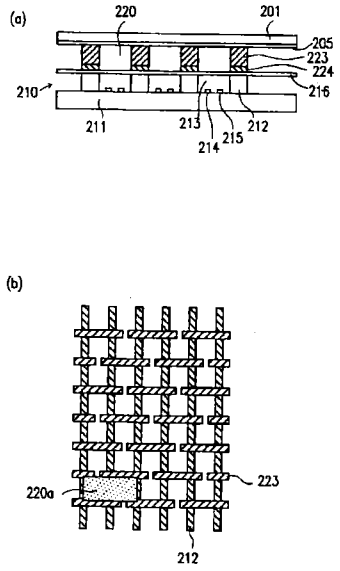
【図22】


(a)
109
105
102
104
107
106
105
108
101
103
(b)
X
107
X
106
108

【図24】


(a)
221
201
220b
205
220a
220
216
212
210
211
222
バックライト
(b)
216
1画素
220a

【図25】



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	1/1337	５１０		1/1337	５１０
	1/1339	５００		1/1339	５００

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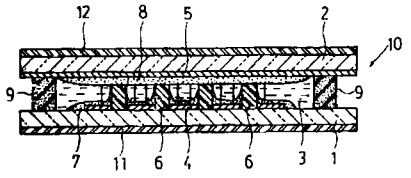
(54)【発明の名称】　反強誘電性液晶パネル

(57)【要約】

【課題】　反強誘電性液晶パネルを用いた液晶表示装置の表示品質および信頼性を高める。

【解決手段】　一対の基板１，２にそれぞれ短冊状の複数の透明電極４，５を形成し、その透明電極４，５が互いに直交するように基板１，２を対向させて、シール材９によって接着し、その間隙に反強誘電性液晶３を封入する。そして、少なくとも隣接する透明電極４の隙間と隣接する透明電極５の隙間の交差部に対応する位置に、感光樹脂によるギャップ材６を第１の基板１に固定して設ける。そして、基板１上に少なくとも透明電極４を被覆するように、基板２上に透明電極５を被覆するように、それぞれ配向膜７，８を形成する。



【特許請求の範囲】
【請求項１】　第１の透明電極を短冊状に複数形成した第１の基板と、第２の透明電極を短冊状に複数形成した第２の基板とを、その第１の透明電極と第２の透明電極とが互いに略直交して対向するように僅かな間隙を設けて対向配置しその間隙に反強誘電性液晶を封入してなる反強誘電性液晶パネルであって、
少なくとも前記複数の第１の透明電極相互の隙間と前記複数の第２の透明電極相互の隙間との交差部に対応する位置に、前記第１の基板に固定して設けられた絶縁材からなるギャップ材と、
前記第１の基板上に少なくとも前記第１の透明電極を被覆するように形成した第１の配向膜と、
前記第２の基板上に前記記第２の透明電極を被覆するように形成した第２の配向膜とを有することを特徴とする反強誘電性液晶パネル。
【請求項２】　前記第１の配向膜が、前記ギャップ材の表面にも形成されている請求項１記載の反強誘電性液晶パネル。
【請求項３】　前記ギャップ材が感光樹脂によって形成された請求項１又は２記載の反強誘電性液晶パネル。
【請求項４】　請求項１乃至３のいずれか一項に記載の反強誘電性液晶パネルにおいて、
前記ギャップ材に接着材付きシリカビーズが被着され、その接着材によって該ギャップ材と前記第２の基板とが接着固定されている反強誘電性液晶パネル。
【請求項５】　前記ギャップ材が、前記第１の透明電極の間隙と前記第２の透明電極の隙間の交差部に対応する位置で、長手辺部と短手辺部とが直交する平面形状が十字状のギャップ材である請求項１乃至４のいずれか一項に記載の反強誘電性液晶パネル。
【請求項６】　前記第１の配向膜と前記第２の配向膜が、それぞれ前記十字状のギャップ材の長手辺部または短手辺部のいずれかに略平行な方向に配向処理されている請求項５記載の反強誘電性液晶パネル。
【請求項７】　前記ギャップ材が、少なくとも前記第１の透明電極の間隙と前記第２の透明電極の隙間の交差部を含む前記各隙間に対応する位置に点在して形成されている請求項１乃至４のいずれか一項に記載の反強誘電性液晶パネル。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】この発明は、表示装置や光シャッタなどに用いられる液晶パネルの一種である反強誘電性液晶パネルに関する。
【０００２】
【従来の技術】反強誘電性液晶パネルを用いた液晶表示装置は、従来のネマティック液晶パネルを用いたものと比べて、応答速度が速く視野角が広いという特徴をもつため、今後の発展が期待されている。反強誘電性液晶は、強誘電性液晶と同様にスメクティック層構造を持つ。この反強誘電性液晶を封入する基板間のセルギャップを１～３μｍ程度とし、液晶分子がその基板面と平行に並ぶように配向処理した液晶セル内では、電界誘起によるスイッチング現象が生じる。
【０００３】すなわち、電圧無印加時には、液晶分子の長軸が層の法線に対して交互に反対方向に所定角度傾斜し、分子長軸と直交する方向に発生する自発分極の方向が、層ごとに上向きと下向きの交互配向構造をとり、セル全体としては、自発分極が０の反強誘電層となる。一方、電圧が印加されると、その電圧による電界方向に一致する方向に液晶分子の自発分極が配向するように各液晶分子が回動して、スメクティック層の法線に対して全て同じ方向へ傾いた強誘電層を示す。この時の液晶分子の傾く方向は印加される電圧の極性に依存する。
【０００４】このような反強誘電性液晶の電界誘起による層状態のスイッチング現象を利用して、透過する光の偏光状態を変化させ、偏光板との組み合わせによって透過光量を制御するようにして、液晶表示パネルや液晶シャッタを構成することができる。
【０００５】ここで、従来の反強誘電性液晶パネルの構造について、図１３の断面図を用いて説明する。この反強誘電性液晶パネル１００は、いずれもガラス板からなる第１の基板１０１と第２の基板１０２とを対向配置し、その間隙に反強誘電性液晶１０３を封入している。
【０００６】その第１の基板１０１と第２の基板１０２の互いに対向する面には、それぞれ短冊状の透明電極１０５，１０６が互いに略直交する方向に多数並べて形成されている。そして、その各透明電極１０５，１０６をそれぞれ被覆するように、ポリイミドやポリアミック酸の樹脂膜を塗布した配向膜１０７，１０８が形成されて、その各表面にラビング法による配向処理が施されている。
【０００７】また、第１の基板１０１と第２の基板１０２との間隙を一定に保つために、両基板間に球径が１．５μｍ～１．７μｍ程度のシリカビーズ１０９がギャップ材として散布されている。このシリカビーズ１０９は、セルギャップを均一にするため５００個／mm^2 ～１０００個／mm^2 の密度で散布される。
【０００８】１１０は、第２の基板１０２に熱硬化型接着剤を用いて形成されたシール材であり、第１の基板１０１と第２の基板１０２が位置合わせして重ね合わせられ、このシール材１１０によって接着されることにより、反強誘電性液晶１０３が注入される間隙が密閉（シール）される。
【０００９】このシール材１１０は、第２の基板１０２の周辺部に沿ってパターン形成されれた熱硬化型接着剤であり、第１の基板１０１を重ねて接着した後、１．０～２．０ｋｇ・cm^{-2} の圧力を加えながら１２０℃～１６０℃の温度で１時間～２時間、炉の中で焼成処理が施さ

れることにより硬化する。このように構成された反強誘電性液晶パネル１００の第１の基板１０１と第２の基板１０２の外側に、それぞれ互いに偏光軸が直交するようにして偏光板１１１，１１２を配置し、液晶表示パネルを構成する。

【００１０】このような反強誘電性液晶パネル１００では、第１の透明電極１０５と第２の透明電極１０６との各交差部ごとに、反強誘電性液晶に対する電圧の無印加と印加を制御することができ、それによって反強誘電性液晶の反強誘電状態と強誘電状態とを選択的に生起させ、この反強誘電性液晶パネル１００を透過する光の偏光状態を部分的に変えることができる。

【００１１】そこで、この反強誘電性液晶パネル１００の両側に、偏光軸が互いに直交する一対の偏光板１１１，１１２を配置することによって、光の透過光量を第１の透明電極１０５と第２の透明電極１０６との交差部である表示画素ごとに制御して各種の表示を行なうことができる。

【００１２】

【発明が解決しようとする課題】このような反強誘電性液晶パネルは、従来のツイストネマチック液晶を用いた液晶表示パネルに比べて、第１の基板１０１と第２の基板１０２との間隙（ギャップ）が小さく、好ましくは２μｍ以下であるため、そのギャップを一定に保つために、前述のように球径が１．５μｍ～１．７μｍ程度のシリカビーズ１０９をギャップ材として用いているが、それによって次のような問題があった。

【００１３】すなわち、図１３に示した反強誘電性液晶パネル１００の第１，第２の基板１０１，１０２の外面に、偏光板１１１，１１２を貼り合わせた液晶表示パネルでは、表示画素部（第１の透明電極１０５と第２の透明電極１０６との交差部）にもシリカビーズ１０９が散布されているため、そのシリカビーズ１０９によって液晶分子の動きが規制されて白抜けが生じたり、シリカビーズ１０９周辺の回折光の影響で微妙な光抜けが生じたりするという問題があった。

【００１４】また、第１，第２の基板１０１と１０２を重ね合わせて反強誘電性液晶パネル１００を作成する際、位置合わせ工程で若干のズレ応力が働くために、シリカビーズ１０９が微妙にズレて配向膜１０７，１０８に配向欠陥が生じ、電圧の無印加時における黒レベルが低下するという問題もあった。これらのことは、結果的に反強誘電性液晶パネルを用いた液晶表示パネルのコントラストを低下させるばかりでなく、配向膜を傷つけたりするとこにより配向不良を生じ、品質面での信頼性が低下するという問題を生じていた。

【００１５】また、反強誘電性液晶パネルの場合、前述のように基板間のギャップが２μｍ以下という狭ギャップであるため、反強誘電性液晶に電圧を印加するための駆動周波数に共振して両基板がわずかに振動する。この振動によりシリカビーズが移動して配向膜を傷つけてしまうため、次第に配向力の低下を招くという問題もある。

【００１６】さらに、反強誘電性液晶パネルは、図１３に示した第１の基板１０１と第２の基板１０２の両側に偏光板１１１，１１２を貼り付けて液晶表示パネルを構成する際に、５～３０ｇ／ｃｍ² 以上の圧力を加えるため、反強誘電性液晶分子特有の規則正しく並んだ層構造が上下からの圧力で破壊される恐れがあった。それによって配向欠陥が生じ、表示品質が悪くなるという問題もあった。

【００１７】そのため、従来の反強誘電性液晶パネルは、層構造を破壊することのないように偏光板を貼り付けるのに特別な装置を必要とするばかりでなく、パネル上面からのペン入力が可能なタッチパネルなどには使用することができないという欠点があった。

【００１８】この発明は、このような従来の反強誘電性液晶パネルにおける種々の問題を解決するためになされたものである。すなわち、反強誘電性液晶を挟持する一対の基板間の狭いギャップを一定に保持でき、且つ配向膜を傷つけて配向欠陥を生じる恐れをなくし、液晶表示パネルとして使用したときに高品質な表示と高い信頼性が得られるようにするとともに、パネル面に多少の圧力が加わっても、反強誘電性液晶の層構造が破壊されることなく、正常に使用できるようにすることを目的とする。

【００１９】

【課題を解決するための手段】上記の目的を達成するため、この発明の反強誘電性液晶パネルは、第１の透明電極を短冊状に複数形成した第１の基板と、第２の透明電極を短冊状に複数形成した第２の基板とを、その第１の透明電極と第２の透明電極とが互いに略直交して対向するように僅かな間隙を設けて対向配置し、その間隙に反強誘電性液晶を封入してなる反強誘電性液晶パネルにおいて、次のようなギャップ材と配向膜を設けたものである。

【００２０】すなわち、絶縁材からなるギャップ材を、少なくとも上記複数の第１の透明電極相互の隙間と上記複数の第２の透明電極相互の隙間との交差部に対応する位置に、前記第１の基板に固定して設ける。また、上記第１の基板上に少なくとも前記第１の透明電極を被覆するように第１の配向膜を形成し、上記第２の基板上に上記第２の透明電極を被覆するように第２の配向膜を形成している。

【００２１】上記第１の配向膜は、上記ギャップ材の表面にも形成してもよい。また、上記ギャップ材は感光樹脂によって容易に形成される。そのギャップ材に接着材付きシリカビーズが被着し、その接着材によって、ギャップ材と第２の基板とが接着固定されるようにするとよい。上記ギャップ材を、第１の透明電極の間隙と第２の

透明電極の隙間の交差部に対応する位置で、長手辺部と短手辺部とが直交する平面形状が十字状のギャップ材にするとよい。

【００２２】その場合、上記第１の配向膜と第２の配向膜が、それぞれ十字状のギャップ材の長手辺部または短手辺部のいずれかに略平行な方向に配向処理されるようにするのが望ましい。上記ギャップ材を、少なくとも第１の透明電極の間隙と第２の透明電極の隙間の交差部を含む各隙間に対応する位置に点在するように形成してもよい。

【００２３】

【発明の実施の形態】以下、この発明の反強誘電性液晶パネルについて、その最適な実施形態を図面を参照して詳細に説明する。

【００２４】（第１の実施形態：図１，図５～８）図１は、この発明による反強誘電性液晶パネルの第１の実施形態を示す断面図である。なお、この図１および他の実施形態の説明に使用する図２乃至図４も、図示の都合上パネルの厚さ方向の寸法比率を大幅に拡大して示している　この反強誘電性液晶パネル１０は、いずれもガラス板からなる第１の基板１と第２の基板２とを対向配置し、その間隙に反強誘電性液晶３を封入している。

【００２５】その第１の基板１と第２の基板２の互いに対向する面には、それぞれ膜圧０．２５μｍ程度の酸化インジウム錫（ＩＴＯ）膜により、短冊状の第１の透明電極４と第２の透明電極５が互いに略直交する方向に多数並べて形成されている。図１においては、第１の基板１上の複数の第１の透明電極４は、紙面平行な方向に所定の間隔を置いて並び、紙面に直交する方向に細長く形成されている。また、第２の基板２上の複数の第２の透明電極５は、紙面直交する方向に所定の間隔を置いて並び、紙面に平行な方向に細長く形成されている。

【００２６】そして、複数の第１の透明電極４相互の隙間と複数の第２の透明電極５相互の隙間との交差部に対応する位置に、感光樹脂からなる平面形状が十字状のギャップ材６を、図５に示すように第１の基板１の内面に固定して設けている。このギャップ材６については、後で詳述する。

【００２７】さらに、第１の基板１の内面に、第１の透明電極４及びギャップ材６を被覆するように第１の配向膜７を形成し、第２の基板２の内面にも、第２の透明電極５を被覆するように第２の配向膜８が形成されている。この配向膜７，８についても、後で詳述する。

【００２８】さらに、第２基板２の内面にシール材９がパターン形成されており、第１の基板１と第２の基板２が位置合わせして重ね合わせられ、このシール材９によって接着されることにより、反強誘電性液晶３が注入される間隙が密閉（シール）される。

【００２９】このシール材９は、第２の基板２の周辺部に沿ってパターン形成された熱硬化型接着剤あるいは紫外線硬化型接着材である。熱硬化型接着剤を用いる場合には第１の基板１を重ねて接着した後、１．０～２．０ｋｇ／ｃｍ² の圧力を加えながら１３０℃～１６０℃の温度で３０分～２時間、炉の中で焼成処理が施されることにより硬化する。

【００３０】その後、反強誘電性液晶３が第１の基板１と第２の基板２の間隙に充填され、その反強誘電性液晶３の注入に要した孔が封止されて、反強誘電性液晶パネル１０が構成される。この反強誘電性液晶パネル１０の第１の基板１と第２の基板２の外側に、それぞれ互いに偏光軸が直交するようにした、偏光板１１，１２を配置して液晶表示パネルを構成する。

【００３１】この反強誘電性液晶パネル１０、およびそれに偏光板１１，１２を組み合わせて構成した液晶表示パネルの動作原理は、前述した従来例の場合と同じであるので、説明を省略する。なお、この実施形態においては、複数の第１の透明電極４と複数の第２の透明電極５の各交差部が各表示画素となる。

【００３２】ここで、図５及び図６も参照して、十字状のギャップ材６の詳細について説明する。十字ギャップ材６は、図５及び図６に示すように、厚さ約１．７μｍ、幅が約１０μｍ程度の長手辺部６ａと短手辺部６ｂとが直交して、十字を構成するように形成されている。なお、図５においては図示の都合上、ギャップ材６の厚さを大幅に拡大して示している。

【００３３】そして、各ギャップ材６の長手辺部６ａは隣接する第１の透明電極４，４の隙間Ｓ１に位置し、短手辺部６ｂは隣接する第２の透明電極５，５の間隙Ｓ２に対応する位置にあり、長手辺部６ａと短手辺部６ｂの交差部６ｃが、隙間Ｓ１と隙間Ｓ２との交差部に対応する位置となるように形成されている。

【００３４】したがって、第１の透明電極４と第２の透明電極５との各交差部である表示画素部１７の４つの角部から、その表示画素部１７の周囲を囲むように、ギャップ材６の長手辺部６ａと短手辺部６ｂとが形成されている。この十字状のギャップ材６は微細な構成であるが、感光樹脂を用いて、フォトリソグラフィ法によって容易に形成することができる。

【００３５】そこで、そのギャップ材６の形成方法の一例を説明する。まず、第１の基板１の電極形成面に、各第１の透明電極４を被覆するように、アクリル系のネガ型感光樹脂（例えばＪＮＰＣ－４３：日本合成ゴム社製）をスピンナ法を用いて５５０～６５０ｒｐｍの回転数で塗布し、８０℃の温度で約１分間炉内でプリベークする。それによって、厚さが約１．７μｍの感光樹脂膜を形成する。

【００３６】その後、多数の十字状のギャップ材６の配置に対応するパターンを形成したフォトマスクを位置合わせして、第１の基板１上の感光樹脂膜に重ね合わせ、露光機で波長が３６０ｎｍの光によって露光する。

【００３７】その後、この第１の基板１を現像液（例えば、ＭＦ－３１２：シプレイマイクロジャパン(株)製）の中に入れ、感光樹脂膜の光に照射されなかった部分を落とす。さらに、この第１の基板１を１９０℃～２００℃の窒素雰囲気中の炉内に１時間投入し、ポストベイクを施す。このようにして、図５に示すような多数の十字状のギャップ材６を、第１の基板１上に固定して容易に形成することができる。

【００３８】次に、図１に示した第１，第２の配向膜７，８の形成方法について説明する。第１の基板上には、ギャップ材６と各透明電極４とを被覆するように、第１の配向膜７を形成し、第２の基板２上にも、各透明電極５を被覆するように第２の配向膜８を形成する。

【００３９】この配向膜７，８は、いずれもポリイミド（溶媒揮発型）やポリアミック酸（反応型）の樹脂膜を、基板１，２上に印刷機を用いて塗布するとともに、それを２００℃～２５０℃の温度で１時間加熱処理して硬化させて形成した後、ラビング法により配向処理を施す。このとき、配向膜としてポリイミド膜を形成する場合には、例えば、ＲＮ－１０２４（日産化学社製の商品名）やＪＩＦ（日本合成ゴム社製の商品名）を使用し、ポリアミック酸の膜を形成する場合には、例えば、ＲＮ－１１０２（日産化学社製の商品名）を使用する。

【００４０】また、この配向膜７，８に対しては、それぞれブラシローラによってラビングして配向処理を施す。その配向処理の方向は、図７に矢印付きの破線で第１の配向膜７の配向方向を、矢印付き実線で第２の配向膜８の配向方向を示すように、種々の方向にすることができるが、十字状のギャップ材６との関係で、その長手辺部６ａと平行な方向ａか、短手辺部６ｂと平行な方向ｂのいずれかの方向とするのが好ましい。

【００４１】図７に示す方向ａあるいは方向ｂ以外の方向でも配向処理は可能であるが、例えば方向ｃのように、長手辺部６ａに対して約４５度傾斜した方向に配向処理を施すと、ギャップ材６の交差部６ｃの周囲のブラシローラによって配向処理を施せない部分が大きくなり、配向欠陥が生じやすく、それが画素内に形成されてしまうため好ましくない。これに対し、図７の方向ａまたは方向ｂに配向処理する場合は、配向欠陥はギャップ材６の長手辺部６ａまたは短手辺部６ｂに沿って形成されるため、画素内に形成されることが少なくなるので、表示に与える影響が少ない。

【００４２】なお、配向膜７，８には図７に破線と実線で示すように互いに平行な方向に配向処理を施す必要があるが、図８の（Ａ）に示すようにその向き（ブラシローラを前向き回転で移動させる方向）も同じ場合はパラレルラビングといい、液晶分子に対するプレチルトの方向も同じになる。これに対して、図８の（Ｂ）に示すようにその向きが互いに反対である場合はアンチパラレルラビングといい、液晶分子に対するプレチルトの方向も逆になる。そして、反強誘電性液晶は、図８の（Ａ）に示すようにパラレルラビングを施した配向膜７、８によってアンチパラレル配向となり、これとは逆に同図（Ｂ）のアンチパラレルラビングによってパラレル配向となる。

【００４３】この反強誘電性液晶パネル１０は、以上のような構成であるから、隣接する第１の透明電極４，４の隙間と隣接する第２の透明電極５，５の隙間との交差部に対応する位置、すなわち、図５に示す第１の透明電極４と第２の透明電極５との交差部である表示画素部１７の４角からその周囲を囲むように、平面形状が十字状のギャップ材６が、第１の基板１に固定して設けられている。

【００４４】したがって、第１の基板１と第２の基板２との間のギャップが、このギャップ材６の高さ（約１．７μｍ）によって規制され、一定に保持される。そして、このギャップ６材は、隣接する表示画素部１７の隙間に設けられているので、ギャップ材６自体によって表示画素部１７に白抜けが生じるようなことはない。また、このギャップ材６は第１の基板１に固定されているため、振動等によって移動する恐れがないので、従来のシリカビーズのように配向膜７，８を傷つけて配向不良を引き起こす恐れもない。

【００４５】また、十字状のギャップ材６が第１の基板１に固定された構造になっているから、対向する第１，第２の基板１，２がパネルの外側にも内側にも変形しない構造となっている。そのため、第１，第２の基板１，２が反強誘電性液晶の駆動周波数に共振して振動することも抑制されるとともに、パネルの外側からの圧力により、反強誘電性液晶３の層構造が破壊されて配向の乱れを生じるようなことも防止される。

【００４６】このように、この反強誘電性液晶パネル１０は、反強誘電性液晶に特有の層構造が破壊されたり、配向膜が傷付けられたりすることなく、常に液晶分子の配向を正常に制御することができるので、液晶表示パネルとして使用したときに、表示品質が高くかつ信頼性の高いパネルとなる。なお、パネルの外側からの圧力により、反強誘電性液晶３の層構造を破壊する恐れがなくなるので、タッチパネルとして使用することも可能になる。

【００４７】（第２の実施形態：図２）次に、この発明による反強誘電性液晶パネルの第２の実施形態について、図２を参照して説明する。図２において、図１と対応する部分には同一の符号を付してあり、第１の実施形態との相違点を中心に説明し、共通点については詳しい説明を省略する。

【００４８】この反強誘電性液晶パネル１０は、第１の基板１上と第２の基板２上に、それぞれ短冊状の複数の第１透明電極４と第２の透明電極５をそれぞれ所定間隔で平行に形成するとともに、第１の透明電極４と第２の

透明電極５とを互いに直交するように対向配置し、シール材９によって第１の基板１と第２の基板２とを張り合わせて、その間隙に反強誘電性液晶３を封入している点、および第２の基板上に第２の透明電極５を覆うように配向膜８を形成している点は、第１の実施形態と共通である。

【００４９】第１の実施形態と相違するのは、第１の基板１上に第１の透明電極４を覆うように第１の配向膜７を形成して、その表面に配向処理を施した後、十字状のギャップ材６を、第１の実施形態の場合と同様な位置に形成した点である。

【００５０】そのため、第１の配向膜７はギャップ材６を被覆せずに、透明電極４だけを被覆するように形成される。したがって、第１の基板１上に透明電極４を被覆するように、第１の実施形態の場合と同様な樹脂を塗布した後、焼成して硬化させて第１の配向膜７を形成する。その後、この配向膜７の全面をブラシローラでラビングすることによって配向処理を施す。

【００５１】そして、十字状のギャップ材６は、第１の配向膜７を形成して配向処理を施した第１の基板１の全面に、その配向膜７を被覆するようにネガ型感光性樹脂を塗布してプリベークした後、ギャップ材６の平面パターンを形成したフォトマスクを重ね合わせて露光及び現像し、その感光性樹脂の未照射部分を落として形成する。こうして、形状および大きさと配置状態は第１の実施形態と同様なギャップ材６を、第１の基板１上に固定して形成することができる。

【００５２】この実施形態の反強誘電性液晶パネルの場合は、第１の配向膜７に配向処理を施す際に、十字状のギャップ材６がない略平坦な配向膜７の全面にラビング処理を施すことができるので、第１の実施形態のものと比較して配向欠陥を生じることが少ない利点がある。しかし、ギャップ材６をパターン形成する際の現像処理によって、配向膜７に施された配向性能が若干低下する可能性もある。その他の点は、第１の実施形態と同様であるから、説明を省略する。

【００５３】（第３の実施形態：図３，図９，図１０）次に、この発明による反強誘電性液晶パネルの第３の実施形態について、図３図９，および図１０を参照して説明する。図３において、図１と対応する部分には同一の符号を付してあり、第１の実施形態との相違点を中心に説明し、共通点については説明を省略する。

【００５４】この第３の実施形態の反強誘電性液晶パネル１０において、図１に示した第１の実施形態の反強誘電性液晶表示パネルと相違する点は、十字状のギャップ材６のに接着剤付きシリカビーズ１５を被着および埋設することにより、この接着剤付きシリカビーズ１５の接着剤によって、ギャップ材６の上部を第１の基板２側の配向膜８に接着している点である。

【００５５】図３においては、ギャップ材６の高さ方向の寸法を大幅に拡大して示しているため、接着剤付きシリカビーズ１５の径がギャップ材６の高さに比べて極めて小さく示されている。しかし、実際には、図９に接着剤付きシリカビーズ１５を被着したギャップ６の一部を拡大して示すように、幅１０μｍで高さ１．７μｍのギャップ材６に対して、直径約１．７μｍ（ギャップ材６の高さと略等しい）の接着剤付きシリカビーズ１５が多数被着されている。

【００５６】その接着剤付きシリカビーズ１５は、図１０にその断面を示すように、比重の大きな球形（直径１．５μｍ）のシリカビーズ１５ａの表面に、エポキシ接着剤１５ｂを厚さ約０．１μｍ程度の膜厚で塗布して、直径を約１．７μｍの球体に形成したものである。

【００５７】この接着剤付きシリカビーズ１５を被着した十字状のギャップ材６は、次のようにして形成される。先ず、第１の実施形態の場合と同様に、第１の基板１上にネガ型感光樹脂を塗布してからプリベークを施す。

【００５８】次いで、乾式スペーサ散布機を用いて、その感光樹脂膜の表面に３００個　㎜²～１２００個／㎜²の密度で接着剤付きシリカビーズ１５を散布する。すると多数の接着剤付きシリカビーズ１５を一様に被着した感光樹脂膜が得られる。その後、接着剤付きシリカビーズ１５が感光樹脂上に馴染むために、１０分程度水平状態で待ち、温度８０℃で１分間、炉内でプレスキュアする。

【００５９】そして、第１の実施形態の場合と同様に、多数の十字状のギャップ材の平面的配置パターンを形成したフォトマスクを重ね合わせて、露光および現像処理を施した後、未照射部分の感光樹脂をそこに被着している接着剤付きシリカビーズ１５とともに落とす。

【００６０】さらに、この第１の基板１をポストベイクのために、１２０℃の窒素雰囲気中の炉内に１時間入れる。このとき、温度が１５０℃以上になると、接着剤付きシリカビーズ１５の図１０に示したエポキシ接着剤１５ｂが溶融してしまうため、十分注意する必要がある。

【００６１】このようにして形成した十字状のギャップ材６の接着剤付きシリカビーズ１５は、その直径がギャップ材６の厚さと略同等であるから、ギャップ材６の中に埋もれてしまうことは少なく、図９に示したようにギャップ材６の上面から一部が突出する。したがって、この第１の基板１に第２の基板２を重ね合わせてシール材９によって接着すると、接着剤付きシリカビーズ１５の表面に塗布されたエポキシ接着剤１５ｂが、第２の基板２上の第２の配向膜８に当接する。

【００６２】そこで、第１の基板１と第２の基板２の上下関係を図３と反対にして、第１の基板１を上側にし、シール材９を硬化するために、１３０℃から１６０℃の炉内に約３０分から２時間投入する。こうすると、各接着剤付きシリカビーズ１５の表面に塗布されたエポキシ

接着剤15bが溶融して重力で流れ落ち、第2の基板2上の配向膜8との接触部に集まる。そのため、その接着材によってギャップ材6の先端部と第2の基板2とを強固に接着することができる

【0063】この実施形態によれば、接着剤付きシリカビーズ15によって、十字状のギャップ材6を第2の基板2にも固定することができるため、第1，第2の基板1，2の剛性を高め、前述の各実施形態のものよりも反強誘電性液晶3の層構造を破壊しないように保護する機能を高めることができる。その他の点は、第1の実施形態と同様であるから説明を省略する。

【0064】（第4の実施形態：図4）次に、この発明による反強誘電性液晶パネルの第4の実施形態について、図4を参照して説明する。図4において、図1乃至第3と対応する部分には同一の符号を付してあり、第3の実施形態との相違点のみを説明し、共通点については説明を省略する。

【0065】この第4の実施形態の反強誘電性液晶パネル10において、図3に示した上述の第3の実施形態と相違する点は、第1の基板1側の第1の配向膜7を、図2に示した第2の実施形態と同様に、ギャップ材6を形成する前に形成し、その全面に配向処理を施した後、接着剤付きシリカビーズ15を被着したギャップ材6を形成している点だけである。そのため、ギャップ材6の表面には第1の配向膜7が形成されていない。

【0066】第1の基板1上に、接着剤付きシリカビーズ15を被着したギャップ材6を形成する方法は、第1の基板1上に第1の配向膜7を形成して配向処理を施した後に、その配向膜7上にネガ型感光性樹脂を塗布し、接着剤付きシリカビーズ15を散布する点以外は、第3の実施形態の場合と同様である。この接着剤付きシリカビーズ15の表面のエポキシ接着材15b（図10）によって、ギャップ材6を第2の基板2にも固着する点も、それによる効果も第3の実施形態と同じである。

【0067】（その他の実施形態）なお、以上の各実施形態の説明においては、ギャップ材として、平面形状が十字状のギャップ材6を形成したが、図11に示すように小型円柱状のギャップ材16を、十字状に並べて集合体ギャップを形成してもよい。あるいは、図12に示すように、少なくとも隣接する第1の透明電極4，4の隙間S1と、隣接する第2の透明電極5，5の隙間S2との交差部に対応する位置に、小型円柱状のギャップ材16を点在させてもよい。勿論、この隙間S1，S2の交差部以外の部分に対応する位置にも、ギャップ材16を設けてもよい。

【0068】例えば、透明電極同士の間隔が10μmでそれを覆い隠すためにクロム（Cr）等で形成されるブラックマトリクスの幅が12μmの場合、円柱状のギャップ材16の直径は10μm程度とする。このギャップ材の平面形状は、十字状や円形に限らず、多角形や長方形、あるいはT字状やL字状のものなどを含んでもよい。

【0069】このようなギャップ材として、アクリル性のネガ型感光樹脂を用いた例について説明したが、ポジ型感光性樹脂を用いることもできる。ただし、ポジ型感光性樹脂を用いる場合は、現像液が配向を傷める恐れがあるため、この点でネガ型感光樹脂を用いる方が好ましい。第1及び第3の実施形態のようにギャップ材を形成した後に配向膜を形成する場合には、現像液によって配向面を傷める恐れがないから、ポジ型感光性樹脂を用いてもよい。

【0070】なお、感光樹脂を使用することにより、第1の基板の全面に塗布した感光樹脂膜を、露光および現像処理することによって、多数の微細なギャップ材を簡単にパターニングして形成することができるが。エッチング等の方法用いる場合には感光樹脂以外の絶縁材を使用することもできる。

【0071】

【発明の効果】以上説明してきたように、この発明による反強誘電性液晶パネルは、少なくとも隣接する第1の透明電極相互の隙間と隣接する第2の透明電極相互の隙間との交差部に対応する位置に、絶縁材からなるギャップ材が第1の基板1に固定して設けられている。そのため、第1の基板1と第2の基板2との間のギャップが、このギャップ材の高さによって規制され、一定に保持される。

【0072】そして、この反強誘電性液晶パネルを液晶表示パネルに使用する場合、ギャップ材は、隣接する表示画素部の隙間に設けられることになるので、ブラックマトリクスによって隠され、ギャップ材自体によって表示画素部に白抜けが生じるようなことはない。また、このギャップ材は第1の基板に固定されているため、振動等によって移動する恐れがないので、従来のシリカビーズのように配向膜を傷つけて配向不良を引き起こす恐れもない。

【0073】また、ギャップ材が少なくとも第1の基板に固定されて設けられているから、対向する第1，第2の基板がパネルの外側にも内側にも変形しにくい構造となっており、第1，第2の基板が反強誘電性液晶の駆動周波数に共振して振動することが抑制されるとともに、パネルの外側からの圧力により、反強誘電性液晶の層構造が破壊されて配向の乱れを生じるようなことも防止される。

【0074】また、外部からの圧力によって、反強誘電性液晶に特有の層構造が破壊されたり、配向膜が傷付けられたりすることがなく、常に液晶分子の配向を正常に制御することができるので、液晶表示パネルとして使用したときに、表示品質が高くかつ信頼性の高いパネルとなる。

【0075】なお、パネルの外側からの圧力により、反

強誘電性液晶の層構造を破壊する恐れもなくなるので、タッチパネルとして使用することも可能になる。このような効果は、ギャップ材を十字状に形成したり、ギャップ材に接着剤付きシリカビーズを被着し、その接着剤によってギャップ材を第２の基板にも固着するようにすることによって、一層高めることができる。

【図面の簡単な説明】

【図１】この発明による反強誘電性液晶パネルの第１の実施形態の構造を模式的に示す断面図である。

【図２】この発明による反強誘電性液晶パネルの第２の実施形態の構造を模式的に示す断面図である。

【図３】この発明による反強誘電性液晶パネルの第３の実施形態の構造を模式的に示す断面図である。

【図４】この発明による反強誘電性液晶パネルの第４の実施形態の構造を模式的に示す断面図である。

【図５】図１における第１，第２の透明電極４，５および十字状のギャップ材６の配置形状を部分的に拡大して示す斜視図である。

【図６】図１における十字状のギャップ材６の平面図である。

【図７】図１における第１，第２の配向膜７，８に対する配向処理方向の説明に供する図である。

【図８】同じく配向処理方向の異なる例を示す図である。

【図９】図３および図４における接着剤付きシリカビーズ１５のギャップ材６への被着状態を拡大して示す斜視図である。

【図１０】図９に示す接着剤付きシリカビーズ１５の断面図である。

【図１１】この発明による反強誘電性液晶パネルに設けるギャップ材の他の形状および配置例を示す平面図である。

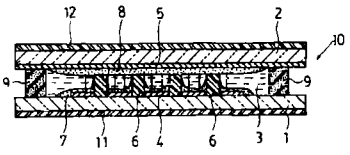
【図１２】この発明による反強誘電性液晶パネルに設けるギャップ材のさらに他の配置例を，第１，第２の透明電極とともに示す平面図である。

【図１３】従来の反強誘電性液晶パネルの構造を模式的に示す断面図である。

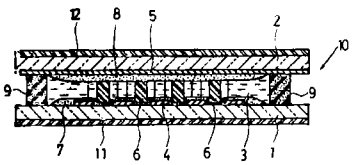
【符号の説明】

１：第１の基板　　２：第２の基板
３：反強誘電性液晶　　４：第１の透明電極
５：第２の透明電極　　６：十字状のギャップ材
７：第１の配向膜　　８：第２の配向膜
９：シール材　　１０：反強誘電性液晶パネル
１１，１２：偏光板
１５：接着剤付きシリカビーズ
１６：小型円柱状のギャップ材
１７：表示画素部

【図１】



【図２】



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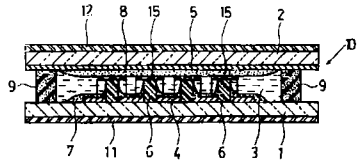

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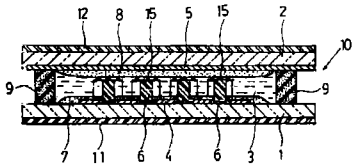

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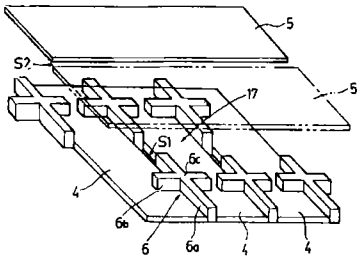

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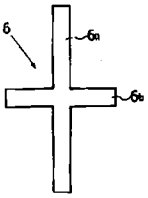

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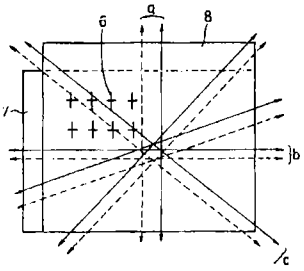

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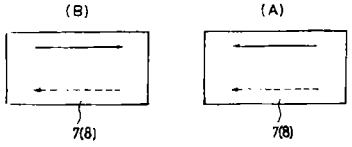

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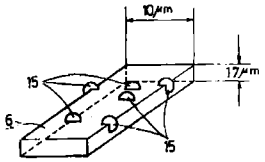

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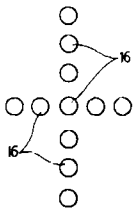
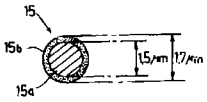
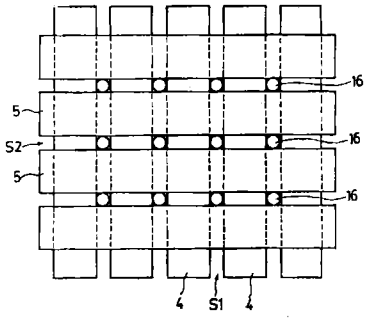


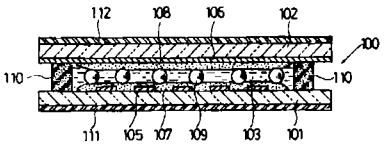
【図10】



【図12】



【図13】



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(51)Int.Cl.[6]		識別記号	庁内整理番号	ＦＩ			技術表示箇所
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		５１０				５１０	
		５２０				５２０	
	1/1343				1/1343		
	1/141				1/137	５１０	

審査請求　未請求　請求項の数９　ＯＬ　（全 22 頁）

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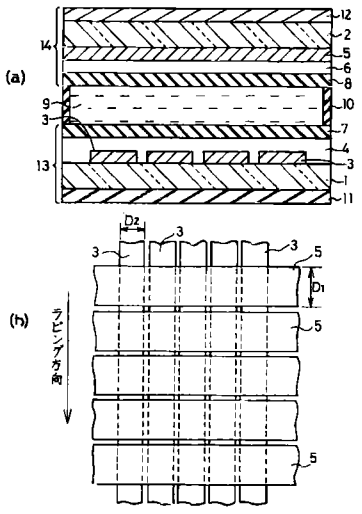
最終頁に続く

(54)【発明の名称】　液晶表示装置

(57)【要約】
【課題】　欠陥のない均一な配向状態を実現し、均一かつ高コントラストの表示特性で表示を行うことができる液晶表示装置を提供する。
【解決手段】　所定範囲における数が走査電極５…より多い信号電極３…を有する電極基板１３の配向膜７に、信号電極３…の長手方向と平行またはほぼ平行に一軸配向処理を施す。一方、走査電極５…を有する電極基板１４の配向膜８に、走査電極５…の長手方向と垂直またはほぼ垂直に一軸配向処理を施す。また、配向膜７・８の配向の方向を平行にする。これにより、電極による段差でＣ２配向の成長が妨げられる回数が少なくなるので、均一なＣ２Ｕ配向を容易に得ることができる。



【特許請求の範囲】
【請求項１】絶縁性かつ透光性の基板、この基板上にストライプ状に配列される複数の電極およびこれらの電極を覆う配向膜を有し、それぞれの電極が交差するように対向して配される透光性の一対の電極基板と、
上記電極基板間に封入される強誘電性液晶とを備え、
上記両電極基板のうち所定範囲における電極数が多い方の電極基板が電極の長手方向と平行またはほぼ平行に一軸配向処理が施される一方、他方の電極基板が電極の長手方向と垂直またはほぼ垂直に一軸配向処理が施され、
上記両電極基板に施される一軸配向処理が平行またはほぼ平行となることを特徴とする液晶表示装置。
【請求項２】上記両電極基板間の間隔を保持するとともに上記両電極基板を接合する間隔保持体が、所定範囲における電極数が多い方の電極基板の隣り合う電極間に、電極の長手方向と平行にかつストライプ状に配列されていることを特徴とする請求項１に記載の液晶表示装置。
【請求項３】絶縁性かつ透光性の基板、この基板上にストライプ状に配列される複数の電極およびこれらの電極を覆う配向膜を有し、それぞれの電極が交差するように対向して配される透光性の一対の電極基板と、
上記電極基板間に封入される強誘電性液晶とを備え、
上記両電極基板のうち最も幅の狭い電極を有する方の電極基板が電極の長手方向と平行またはほぼ平行に一軸配向処理が施される一方、他方の電極基板が電極の長手方向と垂直またはほぼ垂直に一軸配向処理が施され、
上記両電極基板に施される一軸配向処理が平行またはほぼ平行となることを特徴とする液晶表示装置。
【請求項４】上記両電極基板間の間隔を保持するとともに上記両電極基板を接合する間隔保持体が、最も幅の狭い電極を有する方の電極基板の隣り合う電極間に、電極の長手方向と平行にかつストライプ状に配列されていることを特徴とする請求項３に記載の液晶表示装置。
【請求項５】絶縁性かつ透光性の基板、この基板上にマトリクス状に配列される複数の画素電極およびこれらの画素電極を覆う配向膜を有する画素電極基板と、
絶縁性かつ透光性の基板、この基板上に設けられる対向電極およびこの対向基板を覆う配向膜を有し、対向電極と上記画素電極とが対向するように上記画素電極基板と対向して配される対向電極基板と、
上記画素電極基板と上記対向電極基板との間に封入される強誘電性液晶とを備え、
上記画素電極基板が上記画素電極の長辺方向と平行またはほぼ平行に一軸配向処理が施される一方、上記対向電極基板が上記画素電極基板に施される一軸配向処理と平行またはほぼ平行となるように一軸配向処理が施されていることを特徴とする液晶表示装置。
【請求項６】上記画素電極基板と上記対向電極基板との間の間隔を保持するとともにその両電極基板を接合する間隔保持体が、隣り合う上記画素電極間に、上記画素電極の長辺方向と平行にかつストライプ状に配列されていることを特徴とする請求項５に記載の液晶表示装置。
【請求項７】１画素分の表示領域に複数の上記電極または上記画素電極が設けられ、上記間隔保持体が１画素分の表示領域を最小単位として上記電極または上記画素電極を区切ることを特徴とする請求項１、３または５に記載の液晶表示装置。
【請求項８】１画素分の表示領域当たりに複数設けられるカラーフィルタを備え、
１画素分の表示領域内の上記電極または上記画素電極が、同じ表示領域に設けられる複数のカラーフィルタの個々に対応するように設けられていることを特徴とする請求項７に記載の液晶表示装置。
【請求項９】１画素分の表示領域内の上記電極または上記画素電極が、空間分割階調表示のための分割数に応じて設けられていることを特徴とする請求項７に記載の液晶表示装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、強誘電性液晶を用いた液晶表示装置に係り、詳しくは、配向欠陥をなくすようにした液晶表示装置に関するものである。
【０００２】
【従来の技術】従来、液晶表示装置は、ネマチック液晶を用いたものが主流となっている。このような液晶表示装置としては、ＴＮ(Twisted Nematic) 型の液晶表示装置およびＴＮ型を改良したＳＴＮ(Super-Twisted Nematic) 型の液晶表示装置が挙げられる。
【０００３】ＴＮ型液晶表示装置では、光透過率の電圧に依存するしきい特性が十分に急峻でないため、駆動方式のマルチプレックス化が進むにつれて駆動マージンが狭くなり、十分なコントラストが得られなくなるという欠点がある。また、ＳＴＮ型液晶表示装置では、液晶分子が大きなツイスト角で配向されることにより、上記のような欠点を改善することができるものの、大容量表示に用いると、コントラストや応答速度が低下するという欠点がある。
【０００４】そこで、このような欠点を改良するために、キラルスメクチックＣ液晶、すなわち強誘電性液晶を用いた液晶表示装置が、"Applied Physics Letters" 36, (1980) p.899において、N.A.Clark とS.T.Lagerwall とによって提案されている。この液晶表示装置では、液晶分子の誘電異方性を利用したネマチック液晶を駆動する液晶表示装置と異なり、強誘電性液晶の自発分極の極性と電界の極性とを整合させる回転力を用いている。
【０００５】強誘電性液晶は、図２０（ａ）（ｂ）に示すように、バルク状態では、液晶分子１０１の長軸がスメクチック層を区切る層面１０２の法線ｚに対し一定の角度θ傾斜し、かつその傾斜方位が層間で法線ｚに沿って一定の角度Φずつ回転するような分子配列がヘリカル

ピッチにわたって形成されている。また、各液晶分子１０１…は、長軸と法線ｚとのいずれにも直交する方向に自発分極１０３を有している。

【０００６】このような強誘電性液晶は、図２１（ａ）に示すように、偏光板が貼り合わされた２枚の電極基板がヘリカルピッチより薄いギャップで対向して配されてなるセル１０４に注入されると、上記の螺旋構造がほどける。これにより、液晶分子１０１が法線ｚに対してチルト角＋θ傾いて安定する領域と、液晶分子１０１が逆方向にチルト角－θ傾いて安定する領域とが混在して２つの安定した状態が形成される。

【０００７】このような強誘電性液晶に液晶分子１０１の長軸と一方の偏光板の偏光軸１０５とを一致させた状態で電界を印加することにより、図２１（ｂ）に示すように、液晶分子１０１の長軸と自発分極１０３の向きとが一様に揃えられる。このとき、負の電界を印加すると複屈折効果が生じないので、入射光は複屈折しない。この状態から、図２１（ｃ）に示すように、印加する電界の極性を切り替えることにより、液晶分子１０１の配向が一定の状態から別の状態へと切り替えられるスイッチング動作が行われる。

【０００８】これにより、セル１０４内の強誘電性液晶では入射光が複屈折する。したがって、２つの偏光子でセル１０４を挟持することにより光の透過を制御して、暗状態（図２１（ｂ））と明状態（図２１（ｃ））とを得ることができる。

【０００９】また、電界の印加を停止しても、液晶分子１０１の配向が界面の配向規制力によって電界印加時の状態に維持される。これが、強誘電性液晶のメモリ性としての特徴となっている。さらに、スイッチングは、電界が自発分極１０３に直接作用するため、ネマチック液晶表示装置の１／１０００以下で高速応答することができ、それにより高速表示が可能になる。

【００１０】強誘電性液晶は、上記のような双安定性、メモリ性および高速応答性だけでなく、広視野角等の有用な特長を備えている。そこで、近年では、高精細かつ大容量の液晶表示装置への強誘電性液晶の応用が盛んに進められている。

【００１１】

【発明が解決しようとする課題】しかしながら、上記のような強誘電性液晶にも多くの問題がある。まず、強誘電性を示すキラルスメクチックＣ相の液晶は、通常のネマチック液晶に比較して分子環境の対称性が低くかつ結晶性が高いため、一様に配向させることが困難であり、これにより均一な表示を得ることが困難である。

【００１２】強誘電性液晶の研究の初期においては、スメクチックＣ相が基板に垂直に並ぶブックシェルフ型と呼ばれる層構造をなすと考えられていた。しかし、従来のラビング等による一軸配向法を用いて作製されたセルにおいては、スイッチング現象や光学特性が予想されていたものと大きく異なり、提案されていた分子配向モデルとは全く異なるスイッチング動作を行っていたことが判ってきた。

【００１３】その大きな要因として、図２２に示すように、基板１０６・１０６間に形成される各スメクチック層１０７…がシェブロンと呼ばれる中間部で屈曲した構造をなすことが、Ｘ線を用いた小角散乱法によりすでに解析されている。この構造は、液晶と基板１０６との界面でのプレチルト角とスメクチック層１０７の屈曲方向との関係から、図２３（ｂ）（ｃ）に示すように、Ｃ１状態とＣ２状態とに分類される。また、上記の構造は、対向する基板１０６・１０６間で液晶分子が一様に配向しているユニフォーム配向と液晶分子が捩れて配向しているツイスト配向にも分類される。

【００１４】ユニフォーム配向は、分子がほぼ一軸配向しているので、偏光軸が互いに直交する２枚の偏光板により消光位が現れるが、ツイスト配向では、捩れた分子により旋光が生じるため消光位が現れない。したがって、強誘電性液晶の配向状態としては、Ｃ１Ｕ（C1-Uniform），Ｃ２Ｕ（C2-Uniform），Ｃ１Ｔ（C1-Twisted），Ｃ２Ｔ（C2-Twisted）の４種類が存在する（"LIQUID CRYSTALS" 1993, Vol.15,No.5,p.669-p.687参照）。

【００１５】これらの配向のうち、Ｃ２Ｕ配向は、高コントラストが得られるなどの理由から、表示装置に適している（"Ferroelectrics" 1993,Vol.149,pp.183-192および"JAPANESE JOURNAL OF APPLIED PHYSICS" VOL.33,pp.1972-1976,No.10A,APRIL,1994 参照）。

【００１６】上記のようなシェブロン構造では、図２３（ａ）に示すように、スメクチック層１０７…の傾く方向が異なる箇所にいわゆるジグザク欠陥が現れる。このジグザグ欠陥は、ラビング方向に向かって発生する曲線状のヘアピン欠陥と、ラビング方向と逆の方向に向かって発生する鋭角状のライトニング欠陥とに分けられる。

【００１７】均一な表示特性を得るためには、このような欠陥の存在が問題となるのは勿論、欠陥を挟んだ両側の配向状態で光学特性が大きく異なる。それゆえ、ジグザグ欠陥が発生しないように、スメクチック層の屈曲方向を一様に制御することが重要である（前出の"LIQUID CRYSTALS" 参照）。

【００１８】ユニフォーム配向とツイスト配向とが混在する状態は、コントラストの低下や表示のチラツキが生じるため、表示装置においては好ましくない。ユニフォーム配向およびツイスト配向は、液晶の自発的な捩れ力、液晶と配向膜との分子間相互作用、極性エネルギーなどに支配されると考えられている。このため、両配向が混在することの影響は、液晶材料と配向膜材料との組み合わせを調整することにより制御される。

【００１９】一方、Ｃ１状態およびＣ２状態の安定性は、液晶の層傾斜角およびチルト角と配向膜のプレチルト角θ_p（図２３（ｂ））との関係などの幾何学的な効

果により支配されると考えられている。このため、従来では、上記の角度の関係を制御することが提案されているが（"Ferroelectrics" 1991,Vol.114,pp.3-26 参照）、その制御が不完全なため、実際には有効な解決策とはなっていない。

【００２０】その原因としては、スメクチック層１０７の傾く方向が、液晶のチルト角および層傾斜角とプレチルト角との関係だけではなく、特開平１－１７９９１５号公報に開示されているように、基板間に設けられるスペーサのような異物が原因で突発的に反転することが挙げられる。この場合には、スペーサが核となってジグザグ欠陥が発生すると考えられる。

【００２１】また、キラルスメクチックＣ液晶は、結晶性が高く流動しにくい性質を有しているため、機械的な衝撃を受けるとスメクチック層構造が崩れてしまい、一旦、ネマティック相以上の温度に加熱しないと元の配向状態に戻らないという問題を有している。この問題を解決するためには、衝撃を緩和する手法を採り入れる必要がある。

【００２２】例えば、特公平２－１７００７号公報には、感光性ポリイミドなどを用いて柱状や帯状の突起体をセル内に設けることが提案されている。また、特開昭６３－１１６１２６号公報には、接着性を有するスペーサにより対向する基板を強固に接着することが提案されている。これらによれば、衝撃を受けても突起体やスペーサにより基板が撓まないため、衝撃が液晶に伝わらない。しかしながら、これらの構造は、スペーサ同士の間隔が狭いと、液晶の注入性が損なわれ、一部の画素に液晶が注入されなくなるおそれがある。

【００２３】本発明は、上記の事情に鑑みてなされたものであって、欠陥のない均一な配向状態を実現し、均一かつ高コントラストの特性で表示を行うことができる液晶表示装置を提供することを目的としている。さらに、本発明は、液晶の注入性を良好に保つ一方で、機械的衝撃に対しても分子配向の乱れることのない液晶表示装置を提供することを目的としている。

【００２４】

【課題を解決するための手段】本発明の第１の液晶表示装置は、上記の課題を解決するために、絶縁性かつ透光性の基板、この基板上にストライプ状に配列される複数の電極およびこれらの電極を覆う配向膜を有し、それぞれの電極が交差するように対向して配される透光性の一対の電極基板と、これらの電極基板間に封入される強誘電性液晶とを備え、上記両電極基板のうち所定範囲における電極数が多い方の電極基板が電極の長手方向と平行またはほぼ平行に一軸配向処理が施される一方、他方の電極基板が電極の長手方向と垂直またはほぼ垂直に一軸配向処理が施され、上記両電極基板に施される一軸配向処理が平行またはほぼ平行となることを特徴としている。

【００２５】上記の構成において、両電極基板上には、電極部分と隣り合う電極同士の間に現れる基板部分とが存在する。電極部分と基板部分とでは、導電体と絶縁体というように帯電の状態が異なり、さらに表面エネルギーの極性成分および非極性成分も異なる。このため、それぞれの部分が配向膜を介して強誘電性液晶に与える影響も異なる。このような配向膜の下地の変化は、スメクチック層の成長を妨げる要因となる。

【００２６】これに対し、上記の構成では、配向方向が所定範囲における数が多い電極の長手方向と平行またはほぼ平行に統一されている。これにより、強誘電性液晶において、配向膜の下地の状態の変化が少ない方向に沿ってスメクチック層が成長する。それゆえ、スメクチック層の成長が妨げられにくくなり、ジグザグ欠陥の発生のない均一な配向状態を得ることができる。

【００２７】上記第１の液晶表示装置において、好ましくは、上記両電極基板間の間隔を保持するとともに上記両電極基板を接合する間隔保持体が、所定範囲における電極数が多い方の電極基板の隣り合う電極間に、電極の長手方向と平行にかつストライプ状に配列されている。

【００２８】このように、間隔保持体が配向方向に沿ってストライプ状に配列されているので、スメクチック層の成長が間隔保持体によって妨げられることはない。それゆえ、ジグザグ欠陥の発生のない均一な配向状態を得ることができる。しかも、間隔保持体が両電極基板を接合するので、機械的衝撃により配向が乱れることはない。

【００２９】本発明の第２の液晶表示装置は、上記の課題を解決するために、絶縁性かつ透光性の基板、この基板上にストライプ状に配列される複数の電極およびこれらの電極を覆う配向膜を有し、それぞれの電極が交差するように対向して配される透光性の一対の電極基板と、これらの電極基板間に封入される強誘電性液晶とを備え、上記両電極基板のうち最も幅の狭い電極を有する方の電極基板が電極の長手方向と平行またはほぼ平行に一軸配向処理が施される一方、他方の電極基板が電極の長手方向と垂直またはほぼ垂直に一軸配向処理が施され、上記両電極基板に施される一軸配向処理が平行またはほぼ平行となることを特徴としている。

【００３０】上記の構成では、配向方向が最も幅の狭い電極の長手方向と平行またはほぼ平行な方向に統一されている。これにより、強誘電性液晶において、配向膜の下地の状態の変化が少ない方向に沿ってスメクチック層が成長する。それゆえ、スメクチック層の成長が妨げられにくくなり、ジグザグ欠陥の発生のない均一な配向状態を得ることができる。

【００３１】上記第２の液晶表示装置において、好ましくは、上記両電極基板間の間隔を保持するとともに上記両電極基板を接合する間隔保持体が、最も幅の狭い電極を有する方の電極基板の隣り合う電極間に、電極の長手

方向と平行にかつストライプ状に配列されている。

【００３２】このように、間隔保持体が配向方向に沿ってストライプ状に配列されているので、スメクチック層の成長が間隔保持体によって妨げられることはない。それゆえ、ジグザグ欠陥の発生のない均一な配向状態を得ることができる。しかも、間隔保持体が両電極基板を接合するので、機械的衝撃により配向が乱れることはない。

【００３３】本発明の第３の液晶表示装置は、上記の課題を解決するために、絶縁性かつ透光性の基板、この基板上にマトリクス状に配列される複数の画素電極およびこれらの画素電極を覆う配向膜を有する画素電極基板と、絶縁性かつ透光性の基板、この基板上に設けられる対向電極およびこの対向基板を覆う配向膜を有し、対向電極と上記画素電極とが対向するように上記画素電極基板と対向して配される対向電極基板と、上記画素電極基板と上記対向電極基板との間に封入される強誘電性液晶とを備え、上記画素電極基板が上記画素電極の長辺方向と平行またはほぼ平行に一軸配向処理が施される一方、上記対向電極基板が上記画素電極基板に施される一軸配向処理と平行またはほぼ平行となるように一軸配向処理が施されていることを特徴としている。

【００３４】上記の構成では、両電極基板の配向方向が、画素電極の長辺方向と平行またはほぼ平行な方向に統一されている。これにより、強誘電性液晶において、配向膜の下地の状態の変化が少ない方向に沿ってスメクチック層が成長する。それゆえ、スメクチック層の成長が妨げられにくくなり、ジグザグ欠陥の発生のない均一な配向状態を得ることができる。

【００３５】上記第３の液晶表示装置において、好ましくは、上記画素電極基板と上記対向電極基板との間の間隔を保持するとともにその両電極基板を接合する間隔保持体が、隣り合う上記画素電極間に、上記画素電極の長辺方向と平行にかつストライプ状に配列されている。

【００３６】このように、間隔保持体が配向方向に沿ってストライプ状に配列されているので、スメクチック層の成長が間隔保持体によって妨げられることはない。それゆえ、ジグザグ欠陥の発生のない均一な配向状態を得ることができる。しかも、間隔保持体が両電極基板を接合するので、機械的衝撃により配向が乱れることはない。

【００３７】また、上記第１ないし第３のいずれかの液晶表示装置において、好ましくは、１画素分の表示領域に複数の上記電極または上記画素電極が設けられ、上記間隔保持体が１画素分の表示領域を最小単位として上記電極または上記画素電極を区切るようになされている。この構成では、１画素分の表示領域に複数の上記電極または上記画素電極が、次のように、カラー表示または空間分割階調表示に用いられる。すなわち、１画素分の表示領域当たりに複数設けられるカラーフィルタを備え、１画素分の表示領域内の上記電極または上記画素電極が、同じ表示領域に設けられる複数のカラーフィルタの個々に対応するように設けられている。または、１画素分の表示領域内の上記電極または上記画素電極が、空間分割階調表示のための分割数に応じて設けられている。

【００３８】上記の構成では、間隔保持体が１画素分の表示領域を最小単位とする間隔をおいて配置されることにより、間隔保持体同士の間隔がある程度広く確保される。それゆえ、強誘電性液晶の注入が容易になり、各画素に短時間で十分強誘電性液晶が注入される。また、１画素分の表示領域が間隔保持体により区切られないので、画素内での表示特性が間隔保持体の影響を受けることはない。

【００３９】

【発明の実施の形態】

〔実施の形態１〕本発明の第１の実施の形態について図１ないし図９に基づいて説明すれば、以下の通りである。

【００４０】本実施の形態に係る液晶表示装置は、図１（ａ）に示すような液晶パネルを備えている。この液晶パネルは、互いに対向する２枚のガラス基板１・２を有している。なお、透光性かつ絶縁性を有しておれば、ガラス基板１・２の代わりにポリメチルメタクリレート等の樹脂からなる基板を用いてもよい。

【００４１】ガラス基板１の表面には、例えばインジウム錫酸化物（ＩＴＯ）からなる複数の透明な信号電極３…が互いに平行に形成されている。その上には、例えばSiO_2からなる透明な絶縁膜４が積層される。一方、ガラス基板２上には、信号電極３…と同様な材料からなる複数の透明な走査電極５…が信号電極３…と直交するように互いに平行に配置されている。その上には、絶縁膜４と同様の材料からなる透明な絶縁膜６で被覆されている。

【００４２】絶縁膜４・６上には、ラビング処理などの一軸配向処理が施された配向膜７・８がそれぞれ形成されている。配向膜７・８は、ポリイミド膜、ナイロン膜、ポリビニルアルコール膜などの有機高分子膜やSiO_2傾方蒸着膜が用いられる。

【００４３】ガラス基板１は、信号電極３…が形成される側と反対側の面に偏光板１１が設けられている。一方、ガラス基板２は、走査電極５…が形成される側と反対側の面に偏光板１２が設けられている。これらの偏光板１１・１２は、偏光軸が互いに直交するように配置されている。

【００４４】上記のように、ガラス基板１、信号電極３…、絶縁膜４、配向膜７および偏光板１１により、電極基板１３が形成される。一方、ガラス基板２、走査電極５…、絶縁膜６、配向膜８および偏光板１２により、電極基板１４が形成される。

【００４５】液晶（強誘電性液晶）９は、封止剤１０に

より貼り合わされた電極基板１３・１４の間に形成される空間内に充填されている。

【００４６】図１（ｂ）に示すように、信号電極３…および走査電極５…が交差して形成される方形の領域が、本液晶表示装置における画素となっている。また、ストライプ状の走査電極５…および信号電極３…は、それぞれ均一な幅D_1・D_2に形成されており、走査電極５…が信号電極３…より広い幅（$D_1 > D_2$）となっている。加えて、信号電極３…および走査電極５…は、ともに同じ厚さに形成されている。

【００４７】隣接する走査電極５・５の間隔および隣接する信号電極３・３の間隔は、全て等しく設定されている。通常、隣接する電極間の間隔（以降、電極スペースと称する）は、表示装置の開口率（表示に寄与する電極部分の割合）が最大になるように設定される。実質的には、電極スペースは、露光、現像、エッチングといった電極パターニング工程の限界によって決定される。このため、表示装置内では、電極スペースが一定に設定されることが一般的である。

【００４８】信号電極３…および走査電極５…は、本液晶表示装置において１本の走査電極５上の画素数と１本の信号電極３上の画素数とが等しくなるように、数が設定されている。したがって、１本の信号電極３と１本の走査電極５とが交差する領域が１つの画素を形成する構成では、信号電極３…および走査電極５…の数は等しくなる。また、後述する変形例の液晶表示装置のように、１つの画素を構成する信号電極３が複数に分割される構成では、信号電極３…が走査電極５…より多くなる。

【００４９】電極基板１３においては、配向膜７に対し、信号電極３…の長手方向と平行またはほぼ平行な方向にラビング処理が施される。一方、電極基板１４においては、配向膜８に対し、走査電極５…の長手方向と垂直またはほぼ垂直な方向にラビング処理が施される。また、配向膜７・８に対するラビング処理は、平行となるように行われる。

【００５０】本液晶表示装置においては、所定範囲における電極数が少ない電極基板について、その電極の長手方向と平行（ほぼ平行）にラビング処理が施される。したがって、走査電極５の幅D_1が走査電極の幅D_2より狭ければ（$D_1 < D_2$）、配向膜７・８に対するラビング処理の方向が上記の場合と逆になる。

【００５１】上記のように構成される本液晶表示装置では、信号電極３…に沿ってラビング処理が施されることにより、電極による基板上の段差の数が少ない方向にスメクチック層が成長する。これにより、欠陥の発生しやすい段差の影響を少なくすることができ、電極基板１３・１４の全面にわたってＣ２Ｕ配向を得ることができる。

【００５２】これに対し、図２に示す液晶表示装置では、電極基板１３において、配向膜７に対し、信号電極３…の長手方向と垂直またはほぼ垂直な方向にラビング処理を施し、電極基板１４において、配向膜８に対し、走査電極５…の長手方向と平行またはほぼ平行な方向にラビング処理を施している。このような場合、すなわち、ラビング方向を走査電極５…の長手方向と平行とした場合、Ｃ２Ｕ配向やＣ１Ｔ配向が混在することにより、ジグザグ欠陥が隣接する信号電極３・３の間からラビング方向に沿って延びるように発生する。

【００５３】一般に、強誘電性液晶は、高温側から等方相、ネマチック相、スメクチックＡ相を経て強誘電相であるスメクチックＣ相へと相転移する。スメクチックＡ相からスメクチックＣ相への転移では、先にＣ１配向が現れ、続いて僅かに低温になるとＣ２配向が現れる（"JAPANESE JOURNAL OF APPLIED PHYSICS" VOL.30,No.10B, OCTOBER,1991,pp.L1823-L1825 参照）。

【００５４】Ｃ２配向は、Ｃ１配向から変化しながら液晶パネル内を成長する。このとき、室温までの相転移において液晶パネルの全面でＣ１配向からの成長が完了すれば、ジグザグ欠陥のない均一な配向が得られる。しかしながら、Ｃ２配向が成長を完了しないうちにＣ１配向が残ると、得られる配向にはジグザグ欠陥が生じてしまう。

【００５５】このように、結晶性の高いスメクチックＣ相でのＣ２配向の成長は一種の結晶成長と考えることができる。成長の方向は、一軸配向方向であるラビング方向と一致している。従来、問題となっていたスペーサ等の異物によるジグザグ欠陥は、異物によってＣ２配向の成長が妨げられることが原因になって突発的に発生すると考えられる。

【００５６】ストライプ状の電極では、電極部分と電極スペースの部分とで電極の厚さの段差があり、構造的な異物と考えることができる。一方、電極部分と電極スペースの部分とでは、配向膜７・８および絶縁膜４・６の下地の状態がそれぞれＩＴＯ（電極）とガラス（ガラス基板）とで異なるという差異がある。ＩＴＯとガラスとでは、表面エネルギーの極性成分および非極性成分が異なる。さらに、顕著には、ＩＴＯが導電性材料である一方、ガラスが絶縁性材料であることから、表面における帯電の状態が大きく異なる。それゆえ、上記のような下地の状態が、数百Åという薄さの配向膜７・８を介して、液晶９との分子間力に影響すると考えられる。

【００５７】本願出願人は、特願平７－９６８１９号において、１画素内でセルギャップを変化させて階調表示を行う構成を創案している。この構成では、１画素内において一方の基板上の電極の厚さを電極の長手方向と垂直な方向に沿って異ならせることにより、階調表示を行うようになっている。また、この構成において、ラビング処理は、電極の厚さが異なる方向と垂直な方向、すなわち電極の長手方向と平行な方向に施される。

【００５８】上記の構成では、厚さが変化する電極と対

向する電極は、均一な厚さに形成されており、両電極は直交するように配されている。したがって、ラビング処理は、単に構造的に大きな異物である厚い電極の影響を軽減する方向になされているだけであり、前述の分子間の相互作用による影響に関与するように施されてはいない。

【００５９】これに対し、本液晶表示装置では、両電極３・５の厚さが同じであり、かつガラス基板１・２上での両電極３・５の厚さも同じであることから、ラビング処理が、上記の分子間の相互作用による影響を軽減する方向になされていることは明らかである。

【００６０】ここで、図２の構成では、図１（ｂ）の構成に比べ、より多くの電極スペースを横切る方向にラビングが施されるので、Ｃ２配向の成長が妨げられやすい。したがって、同様な構造をなす液晶表示装置においては、ラビング方向が段差の数の少ない方の電極を横切る方向であることにより、均一なＣ２Ｕ配向を容易に得ることができる。

【００６１】以上述べたように、本実施の形態に係る液晶表示装置では、所定範囲内での数が多い方の電極（信号電極３）側の配向膜７に、その電極の長手方向と平行な方向にラビング処理を施すことにより、配向欠陥のない均一なＣ２Ｕ配向を得ることができる。それゆえ、本液晶表示装置は、均一かつ高コントラストで表示を行うことができる。

【００６２】〔変形例１〕次に、本実施の形態の第１の変形例について説明する。

【００６３】本変形例に係る液晶表示装置では、図３に示すように、信号電極３が２つの分割電極（以降、電極と称する）３ａ・３ｂにより構成されており、電極３ａが電極３ｂより広い幅に形成されている。また、各１本の電極３ａ・３ｂと１本の走査電極５とが交差する領域により、１つの画素が形成される。このような構成では、１画素への電圧の印加が４種類の組み合わせで行われるので、階調表示が可能となる。

【００６４】上記のように構成される液晶表示装置を、走査電極５および電極３ａ・３ｂの幅、配向膜７・８および液晶９の材料を種々変更して実際に作製した。

【００６５】この液晶表示装置の作製に際しては、走査電極５の幅を２００～５００μｍの範囲に設定し、電極３ａの幅を１００～３００μｍの範囲に設定し、電極３ｂの幅を５０～１５０μｍの範囲に設定し、いずれの組み合わせにおいても走査電極５の幅が最も広くなるようにした。

【００６６】また、SiO_2 を用いて絶縁膜４・６を形成し、特開平７－１７５０６８号公報に開示されている材料を用いて配向膜７・８を形成した。この配向膜７・８は、具体的には、アミン成分としての２，２－ビス［４－（４－アミノフェノキシ）フェニル］プロパンと、カルボン酸成分としての１，２，４，５－ベンゼンテトラカルボン酸二無水物とをそれぞれ主原料として縮合形成されたポリイミド膜からなっている。このポリイミド膜は、次のようにして得られる。

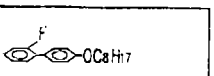
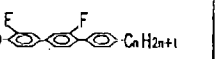
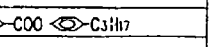
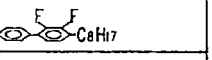
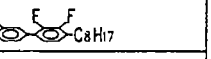
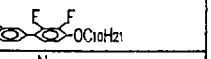
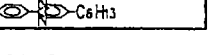
【００６７】まず、上記のアミン成分と、上記のカルボン成分と、１－アミノ－４－トリメトキシシリルベンゼンとを８：７：１．８のモル比でＮＭＰに混合し、１５℃で５時間重合することによりポリアミド酸１０％のＮＭＰ溶液を得る。このＮＭＰ溶液をスピンコート法により絶縁膜４・６上に塗布し、１００℃で５分間仮焼成し、さらに、２００℃で１時間焼成することにより、５００オングストローム程度にポリイミド膜を形成する。ポリイミド膜の作製工程においては、上記の焼成温度を３００℃としてもよいし、上記のモル比を、５：４：１．８、４：３：０．９、６０：５９：１．８または１：１：０としてもよい。

【００６８】配向膜７・８に対するラビング処理は、信号電極３の長手方向に平行な方向に行った。また、液晶９の材料として、メルク社製の強誘電性液晶ＳＣＥ－８および本願出願人の出願に係る特願平６－２３７８５１号に記載された強誘電性液晶組成物を用いた。この強誘電性液晶組成物は、上記特願平６－２３７８５１号の実施例に記載された組成物であり、例えば、表１に示す１７種類の化合物および２種類の光学活性化合物のうちのいくつかが表３および表４の組成比で組み合わされて得られた組成物である。

【００６９】

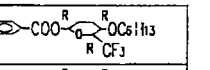
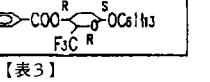
【表１】

化合物の構造

化合物1	m=8	
化合物2	m=9	
化合物3	m=10	
化合物4	m=5 n=8	
化合物5	m=8 n=5	
化合物6	m=8 n=8	
化合物7	m=7 n=7	
化合物8	m=7 n=8	
化合物9	m=7 n=9	
化合物10	m=8 n=8	
化合物11	m=8 n=10	
化合物12	m=9 n=6	
化合物13		
化合物14		
化合物15		
化合物16		
化合物17		

【0070】　　【表2】

光学活性化合物の構造

化合物18	
化合物19	

【0071】　　【表3】

組成物1～10の組成（重量%）

		化合物												
		1	2	3	4	5	6	12	13	14	15	16	17	18	19
組成物	1	16.5	16.5	16.5	16.5	16.5	16.5							0.7	0.3
	2	14.8	14.8	14.8	14.8	14.8	14.8	10.0						0.7	0.3
	3	13.2	13.2	13.2	13.2	13.2	13.2	20.0						0.7	0.3
	4	14.8	14.8	14.8	14.8	14.8	14.8		10.0					0.7	0.3
	5	13.2	13.2	13.2	13.2	13.2	13.2		20.0					0.7	0.3
	6	14.8	14.8	14.8	14.8	14.8	14.8			10.0				0.7	0.3
	7	13.2	13.2	13.2	13.2	13.2	13.2			20.0				0.7	0.3
	8	13.2	13.2	13.2	13.2	13.2	13.2				20.0			0.7	0.3
	9	14.8	14.8	14.8	14.8	14.8	14.8					10.0		0.7	0.3
	10	14.8	14.8	14.8	14.8	14.8	14.8						10.0	0.7	0.3

【0072】　　【表4】

組成物１１～２０の組成（重量%）

		化合物													
		4	7	8	9	10	11	12	13	14	15	16	17	18	19
組成物	11		5.0	9.9	14.9	19.8	29.7	19.8						0.7	0.3
	12	10.0	4.6	8.9	13.4	17.8	26.7	17.8						0.7	0.3
	13	20.0	4.0	7.9	11.9	15.8	23.7	15.8						0.7	0.3
	14		4.6	8.9	13.4	17.8	26.7	17.8	10.0					0.7	0.3
	15		4.5	8.9	13.4	17.8	26.7	17.8		10.0				0.7	0.3
	16		4.0	7.9	11.9	15.8	23.7	15.8		20.0				0.7	0.3
	17		4.0	7.9	11.9	15.8	23.7	15.8			20.0			0.7	0.3
	18		4.5	8.9	13.4	17.8	26.7	17.8				10.0		0.7	0.3
	19		4.6	8.9	13.4	17.8	26.7	17.8					10.0	0.7	0.3
	20		4.0	7.9	11.9	15.8	23.7	15.8					20.0	0.7	0.3

【００７３】このようにして作製した全ての液晶表示装置について、ラビングローラの回転数、ステージの移動速度、ラビングの押し込み量、ラビング回数等のラビング条件を調整することにより、表示領域の全体で均一なＣ２Ｕ配向を容易に得ることができた。

【００７４】なお、ここでのラビング条件は、以下に示す通りである。括弧内には、より好ましい範囲を記す。

ローラ回転数：５０～１００００ｒｐｍ（２００～２０００ｒｐｍ）

ステージ移動速度：５～１００ｍｍ／ｓｅｃ（１０～５０ｍｍ／ｓｅｃ）

押し込み量：０．１～３．０ｍｍ（１．０～２．０ｍｍ）

ラビング回数：１～３０回（３～７回）

この変形例の比較例として、同様な構成でラビング方向を走査電極５の長手方向と平行にした液晶表示装置を作製した。この液晶表示装置においては、上記のようにラビング条件を調整したにも関わらず、ほとんどの場合、ジグザグ欠陥が多く発生し、均一なＣ２Ｕ配向を得ることができなかった。

【００７５】〔変形例２〕続いて、本実施の形態の他の変形例について説明する。

【００７６】本変形例に係る液晶表示装置は、図４（ａ）（ｂ）に示すように、図１（ｂ）の電極構造と同様な電極構造を含んでおり、さらにスペーサ１５…を備えている。このスペーサ１５…は、感光性ポリイミドからなり、信号電極３…の各電極スペースに、信号電極３…と平行、すなわちストライプ状に配されている。また、スペーサ１５…は、ガラス基板１・２および走査電極５…に接着されており、間隔保持体として機能している。

【００７７】上記のように構成される本変形例では、スペーサ１５…と平行な方向にラビング処理が行われる。このような変形例において、上記のラビング条件を調整することにより、均一なＣ２Ｕ配向を得ることが概ね容易であった。

【００７８】この変形例に対し、図５（ａ）（ｂ）に示すように、スペーサ１５…と同様な材料からなるスペーサ１６…が走査電極５…の各電極スペースに設けられ、かつラビング方向がスペーサ１６…と平行な方向である液晶表示装置を比較例として作製した。この液晶表示装置では、ラビング条件を調整したにも関わらず、ほとんどの場合、ジグザグ欠陥が多く発生し、均一なＣ２Ｕ配向を得ることができなかった。

【００７９】なお、図４（ｂ）および図５（ｂ）においては、前記の絶縁膜４・６、配向膜７・８等を省略しており、後述の図６（ｂ）ないし図８（ｂ）においても同様に省略している。

【００８０】また、本変形例では、スペーサ１５…により、機械的衝撃による配向状態の乱れがなく、配向状態が保持される。

【００８１】特公平２－１７００７号公報には、ストライプ状の電極間に平行に帯状突起体が設けられ、それと平行な方向にラビング処理を行う構成が開示されている。ところが、この構成では、本実施例のように幅が設定された対向する２種類の電極との配置関係が特定されていない。

【００８２】ここで、変形例１の液晶表示装置と同様な構成で、スペーサ１５…を有する液晶表示装置を実際に作製した。この液晶表示装置の作製においては、次の手順で厚さ１．５μｍのスペーサ１５…を形成した。まず、感光性アクリル樹脂（日本合成ゴム社製－品番ＪＮＰＣ）をスピンコート法で１．５μｍの厚さに形成し、８０℃で３分間焼成する。続いて、フォトマスクを用いて露光および現像し、さらに２００℃で６０分間本焼成を行う。

【００８３】このように作製した全ての液晶表示装置について、ラビング条件を調整することにより、表示領域の全体で均一なＣ２Ｕ配向を容易に得ることができた。また、各液晶表示装置に落下、指による押圧などによる衝撃を加えても、配向が乱れることはなかった。

【００８４】この変形例の比較例として、同様な構成でスペーサ１５…の形成方向およびラビング方向を走査電極５の長手方向と平行にした液晶表示装置を作製した。この液晶表示装置においては、耐衝撃性については、上記の構成とほぼ同等の性能を得ることができたが、ジグ

ザグ欠陥が多く発生し、均一なC2U配向を得ることができなかった。

【0085】〔変形例3〕引き続いて、本実施の形態のさらに他の変形例について説明する。

【0086】本変形例に係る液晶表示装置は、図6（a）（b）に示すように、ガラス基板2上に1画素単位で3原色のR，G，Bに対応するマイクロカラーフィルタ17…が形成されている。隣接するマイクロカラーフィルタ17・17の間には、遮光層（ブラックマトリクス）18…が形成されている。上記のマイクロカラーフィルタ17…は、オーバーコート層19で覆われており、オーバーコート層19上に走査電極5…が形成されている。

【0087】ガラス基板1上に形成される信号電極3は、1画素分においてR，G，Bの各マイクロカラーフィルタ17…に対応するように3つの分割電極（以降、電極と称する）3c・3d・3eにより構成されている。スペーサ15…は、1画素毎の電極スペースに設けられている。また、電極スペーサ15…は複数画素毎に設けられていてもよい。

【0088】単純マトリクス方式のカラー液晶表示装置では、通常、オーバーコート層が通常アクリル、ポリイミド等の有機材料からなるため、その上に精細なITO透明電極をエッチング等の手法により形成することが困難である。これは、ITOの有機材料への密着性がITOのガラス基板への密着性より劣るからである。したがって、上記の構成では、幅の広い走査電極5…がオーバーコート層19上に形成されることにより、その影響を軽減することができる。

【0089】さらに、上記の構成では、図7（a）（b）に示すように、空間分割階調表示のために、信号電極3が、それぞれ2分割された電極3c・3cと、電極3d・3dと、電極3e・3eとからなっていてもよい。この構成において、スペーサ15…は、R，G，B毎に信号電極3を区切る各電極スペースに形成されている。また、スペーサ15…は、図8（a）（b）に示すように、1画素毎に設けられていてもよい。

【0090】図7（a）（b）に示す構成のように、スペーサ15…の数を多くすれば、耐衝撃性を高めるには好適である。しかしながら、隣接するスペーサ15・15同士の間隔が狭くなるほど液晶の注入時間が長くなるため、場合によっては液晶が注入されない画素が残るおそれがある。このような問題に対しては、図8（a）（b）に示す構成のように、スペーサ15・15同士の間隔をある程度広く確保すればよい。注入を良好に行うためのスペーサ15・15同士の間隔は、10μm以上必要であり、好ましくは100μm以上あればよい。

【0091】スペーサ15・15同士の間隔は、上記のように耐衝撃性と液晶の注入工程とを考慮して決定されるが、カラーフィルタまたは画素のいずれを分割することに関わらず、本変形例に係る液晶表示装置においては、1画素として機能する電極を最小単位として、1画素毎または複数画素毎にスペーサ15…を設けることが望ましい。

【0092】1画素を最小単位としてスペーサ15…で1画素または複数画素が区切られる構造では、画素内の部分は、スペーサ15…によるスイッチングしきい値等の影響を同一とすることができる。これに対し、1画素がスペーサ15で区切られる構成では、画素内で特性が微妙に異なるおそれがあり、これによりカラー表示や階調表示に悪影響が及ぶ。

【0093】ここで、図8（a）（b）に示す構成の液晶表示装置を実際に作製した。作製においては、変形例1での手順と同様にしてスペーサ15…を形成した。また、液晶材料等は、変形例1と同様のものを使用した。

【0094】このように作製した全ての液晶表示装置について、表示領域の全体で均一なC2U配向を得ることができた。また、各液晶表示装置に衝撃を加えても、配向が乱れることはなかった。さらに、液晶材料を注入する際には、全ての画素に十分に液晶を注入することができた。

【0095】上記の液晶表示装置に対し、図9に示すように、信号電極3…についての全ての電極スペースにスペーサ15…を有する以外は図8（a）（b）に示す液晶表示装置と同様の構成の液晶表示装置を作製した。この液晶表示装置では、液晶材料を注入する際に、液晶が注入されない画素が残った。

【0096】なお、後述する第2の実施の形態についても、分割された信号電極5…を有し、かつスペーサ15…が設けられる液晶表示装置を作製したが、本変形例の液晶表示装置とほぼ同様な結果が得られた。

【0097】〔実施の形態2〕本発明の第2の実施の形態について図10ないし図14に基づいて説明すれば、以下の通りである。なお、前記第1の実施の形態における構成要素と同等の機能を有する本実施の形態における構成要素については、同様の符号を付記してその説明を省略する。

【0098】本実施の形態に係る液晶表示装置は、図10（a）に示すように、電極構造を除いて、前記の実施の形態1と同等に構成されている。本液晶表示装置では、ガラス基板1上に信号電極21…がストライプ状に設けられる一方、ガラス基板2上に走査電極22…がストライプ状に設けられている。信号電極21…および走査電極22…は互いに交差するように配されている。

【0099】図10（b）に示すように、信号電極21…および走査電極22…が交差して形成される方形の領域が、本液晶表示装置における画素となっている。また、走査電極22…は、均一な幅D_3に形成され、信号電極21…は、図中左側から右側にかけて順次幅が狭くなるように形成されている。信号電極21の最も広い幅

と最も狭い幅はそれぞれD_4・D_5であり、D_5＜D_3＜D_4となるように電極幅が設定されている。

【0100】信号電極21…および走査電極22…は、ともに同じ厚さに形成されている。また、隣接する信号電極21・21の間隔および隣接する走査電極22・22の間隔は、全て等しく設定されている。

【0101】信号電極21…および走査電極22…は、本液晶表示装置において1本の信号電極21上の画素数と1本の走査電極22上の画素数とが等しくなるように、数が設定されている。したがって、1本の信号電極21と1本の走査電極22とが交差する領域が1つの画素を形成する構成では、信号電極21…および走査電極22…の数は等しくなる。したがって、後述する変形例の液晶表示装置のように、1つの画素を構成する信号電極21および走査電極22が同数に分割される構成でも、信号電極21と走査電極22…とは同数になる。

【0102】電極基板13'においては、配向膜7に対し、信号電極21…の長手方向と平行またはほぼ平行な方向にラビング処理が施される。一方、電極基板14'においては、配向膜8に対し、走査電極22…の長手方向と垂直またはほぼ垂直な方向にラビング処理が施される。また、配向膜7・8に対するラビング処理は、平行となるように行われる。

【0103】本液晶表示装置においては、最も幅の狭い電極を有する電極基板について、その電極の長手方向と平行（ほぼ平行）にラビング処理が施される。したがって、走査電極22…が最も幅の狭い電極を含んでおれば、配向膜7・8に対するラビング処理の方向が上記の場合と逆になる。

【0104】上記のように構成される本液晶表示装置では、信号電極21に沿ってラビング処理が施されることにより、電極による基板上の段差の数が少ない方向にスメクチック層が成長する。これにより、欠陥の発生しやすい段差の影響を少なくすることができ、電極基板13'・14'の全面にわたってC2U配向を得ることができる。

【0105】これに対し、図11に示すように、ラビング方向を走査電極22…の長手方向と平行にした場合、C2U配向やC1T配向が混在することにより、ジグザグ欠陥が隣接する信号電極21・21の間からラビング方向に沿って延びるように発生する。このジグザグ欠陥は、特に電極の幅が狭い領域で集中して発生している。

【0106】このようなラビング方向による配向状態の差異は、顕微鏡による観察から、次のように説明することができる。

【0107】C2配向の成長過程で段差または電極スペースによりC2配向の成長が妨げられても、それに続く電極部分では新たにC2配向が成長する。このため、成長方向に対する電極幅が広ければ、発生したジグザグ欠陥が電極部分から成長したC2配向に取り込まれて消失する。しかし、成長方向に対する電極幅が狭ければ、発生したジグザグ欠陥が電極部分から成長したC2配向に取り込まれるより先に、次の段差または電極スペースによりC2の成長が妨げられる。

【0108】したがって、液晶表示装置においては、幅の狭い電極に対してC2配向が妨げられないようにラビング方向を定めることが望ましい。

【0109】〔変形例1〕続いて、本実施の形態の変形例について説明する。

【0110】本変形例に係る液晶表示装置では、図12に示すように、信号電極21が2つの電極21a・21bに分割されており、走査電極22が2つの電極22a・22bに分割されている。電極21aは電極21bより広い幅に形成され、電極22aは電極22bより広い幅に形成されている。しかも、電極21aは全電極中最も広く、電極21bは全電極中最も狭くなっている。また、各1本の電極21a・21bと各1本の電極22a・22bとが交差する領域により、1つの画素が形成される。このような構成では、1画素への電圧の印加が16種類の組み合わせで行われるので、階調表示が可能となる。

【0111】上記のように構成される液晶表示装置を、電極21a・21bおよび電極22a・22bの幅、配向膜7・8および液晶9の材料を種々変更して実際に作製した。

【0112】この液晶表示装置の作製に際しては、電極21a・21bの幅をそれぞれ200～400μm、100～200μmの範囲に設定し、電極22a・22bの幅をそれぞれ300～500μm、50～100μmの範囲に設定し、いずれの組み合せにおいても、前述の電極幅の順になるようにした。

【0113】また、SiO_2を用いて絶縁膜4・6を形成し、特開平7－175068号公報に開示されている材料を用いて配向膜7・8を形成した。配向膜7・8に対するラビング処理は、信号電極21の長手方向に平行な方向に行った。また、液晶9の材料として、メルク社製の強誘電性液晶SCE－8および本願出願人の出願に係る特願平6－237851号に記載された強誘電性液晶組成物を用いた。

【0114】このようにして作製した全ての液晶表示装置について、ラビングローラの回転数、ステージの移動速度、ラビングの押し込み量、ラビング回数等のラビング条件を調整することにより、均一なC2U配向を容易に得ることができた。

【0115】上記の液晶表示装置の比較例として、同様な構成でラビング方向を走査電極22の長手方向と平行にした液晶表示装置を作製した。この液晶表示装置においては、上記のようにラビング条件を調整したにも関わらず、ほとんどの場合、ジグザグ欠陥が多く発生し、均一なC2U配向を得ることができなかった。

【0116】以上述べたように、本実施の形態に係る液晶表示装置では、最も幅の狭い電極（信号電極21）側の配向膜7に、その電極の長手方向と平行な方向にラビング処理を施すことにより、配向欠陥のない均一なC2U配向を得ることができる。それゆえ、本液晶表示装置は、均一かつ高コントラストで表示を行うことができる。

【0117】〔変形例2〕続いて、本実施の形態の他の変形例について説明する。

【0118】本変形例に係る液晶表示装置は、図13（a）（b）に示すように、図10（b）の電極構造と同様な電極構造を含んでおり、さらにスペーサ15…を備えている。このスペーサ15…は、第1の実施の形態における変形例2の構成と同様に、信号電極21…の電極スペースに、信号電極21…と平行、すなわちストライプ状に配されている。

【0119】上記のように構成される本変形例では、スペーサ15…と平行な方向にラビング処理が行われる。このような変形例において、上記のラビング条件を調整することにより、均一なC2U配向を得ることが概ね容易であった。

【0120】この変形例に対し、図14（a）（b）に示すように、スペーサ16…が走査電極22…の電極スペースに設けられ、かつラビング方向がスペーサ16…と平行な方向である比較例の液晶表示装置を作製した。この液晶表示装置では、ラビング条件を調整したにも関わらず、ほとんどの場合、ジグザグ欠陥が多く発生し、均一なC2U配向を得ることができなかった。

【0121】なお、図13（b）および図14（b）においては、前記の絶縁膜4・6、配向膜7・8等を省略している。

【0122】また、本変形例では、スペーサ15…により、機械的衝撃による配向状態の乱れがない。

【0123】ここで、変形例1の液晶表示装置と同様な構成で、スペーサ15…を有する液晶表示装置を実際に作製した。この液晶表示装置の作製においては、第1の実施の形態における変形例2での手順と同様にして厚さ1．5μmのスペーサ15…を形成した。そして、その液晶表示装置に対し、同様に耐衝撃試験を行った。

【0124】このように作製した全ての液晶表示装置について、ラビング条件を調整することにより、表示領域の全体で均一なC2U配向を容易に得ることができた。また、各液晶表示装置に衝撃を加えても、配向が乱れることはなかった。

【0125】この変形例の比較例として、同様な構成でスペーサ16…の形成方向およびラビング方向を走査電極22の長手方向と平行にした液晶表示装置を作製した。この液晶表示装置においては、耐衝撃性については、上記の構成とほぼ同等の性能を得ることができたが、ジグザグ欠陥が多く発生し、均一なC2U配向を得ることができなかった。

【0126】〔実施の形態3〕本発明の第3の実施の形態について図15ないし図19に基づいて説明すれば、以下の通りである。なお、前記第1の実施の形態における構成要素と同等の機能を有する本実施の形態における構成要素については、同様の符号を付記してその説明を省略する。

【0127】本実施の形態に係る液晶表示装置は、図15（a）に示すように、互いに対向する2枚のガラス基板1・2を備えている。

【0128】ガラス基板1の表面には、例えばAlからなるゲート線31…が互いに平行に形成され、そのゲート線31…上に図示しない絶縁膜を介して例えばAlからなるソース線32…が互いに形成されている。ゲート線31…およびソース線32…は、互いに交差するように配されている。また、隣接するゲート線31・31と隣接するソース線32・32とで囲まれる領域には、画素電極33が配されている。画素電極33…は、ガラス基板1における全体にわたってマトリクス状に配されている。

【0129】画素電極33…は、隣接する3個で1画素の表示を行うように構成されており、それぞれがR・G・Bの色の表示を担うようになっている。図15（b）に示すように、1画素がほぼ正方形をなすため、画素電極33…の個々はソース線32…に沿って長くなる長方形をなしている。また、画素電極33…の短辺と長辺とは、それぞれゲート線31とソース線32とに平行となるように形成されている。

【0130】ゲート線31…とソース線32…との各交差部の近傍には、TFT（薄膜トランジスタ）34…が形成されている。薄膜トランジスタ34は、ゲートがゲート線31に接続され、ソースがソース線32に接続され、ドレインが画素電極33に接続されている。

【0131】上記のゲート線31…、ソース線32…、画素電極33…およびTFT34…は、図示しない透明の絶縁膜および配向膜7により覆われている。また、ガラス基板1のゲート線31…等が形成された面と反対側の面には、偏光板11が形成されている。

【0132】一方、ガラス基板2の表面には、共通電極35が形成されており、この共通電極35は配向膜8により覆われている。また、ガラス基板2の共通電極35…等が形成された面と反対側の面には、偏光板12が形成されている。

【0133】上記のように、ガラス基板1、ゲート線31…等により、電極基板36が形成される。一方、ガラス基板2、共通電極35等により、電極基板37が形成される。また、液晶（強誘電性液晶）9は、図示しない封止剤により貼り合わされた電極基板36・37の間に形成される空間内に充填されている。

【0134】電極基板36においては、配向膜7に対

し、図15（b）に示すように、画素電極33…の長辺方向と平行またはほぼ平行な方向にラビング処理が施される。一方、電極基板37においては、配向膜8に対し、一方向にラビング処理が施される。また、配向膜7・8に対するラビング処理は、平行となるように行われる。

【0135】上記のように構成される本液晶表示装置では、画素電極33…の長辺方向に沿ってラビング処理が施されることにより、電極による基板上の段差の数が少ない方向にスメクチック層が成長する。これにより、欠陥の発生しやすい段差の影響を少なくすることができ、全面にわたってC2U配向を得ることができる。

【0136】これに対し、図16に示すように、ラビング方向を画素電極33…の短辺方向と平行にした場合、C2U配向やC1T配向が混在することにより、ジグザグ欠陥がゲート線31…と画素電極33…との間からラビング方向に沿って延びるように発生する。

【0137】本実施例に係る液晶表示装置を、画素電極33の長辺および短辺、配向膜7・8ならびに液晶9の材料を種々変更して実際に作製した。

【0138】この液晶表示装置の作製に際しては、画素電極33の長辺と短辺とをそれぞれ200～500μm、50～300μmの範囲に設定した。また、絶縁膜、配向膜7・8および液晶9については、第1の実施の形態における変形例1で述べた液晶表示装置と同じ材料を用いた。

【0139】このようにして作製した全ての液晶表示装置について、ラビング条件を調整することにより、表示領域の全体で均一なC2U配向を容易に得ることができた。

【0140】上記の液晶表示装置に対し、同様な構成でラビング方向を画素電極33の短辺方向と平行にした液晶表示装置を作製した。この液晶表示装置においては、ラビング条件の調整にも関わらず、ほとんどの場合でジグザグ欠陥が多く発生し、均一なC2U配向を得ることができなかった。

【0141】以上述べたように、本実施の形態に係る液晶表示装置では、配向膜7・8に、画素電極33の長辺方向と平行な方向にラビング処理を施すことにより、配向欠陥のない均一なC2U配向を得ることができる。それゆえ、本液晶表示装置は、均一かつ高コントラストで表示を行うことができる。

【0142】〔変形例1〕ここで、本実施の形態の変形例について説明する。

【0143】本変形例に係る液晶表示装置は、図17（a）（b）に示すように、図15（b）の電極構造と同様な電極構造を含んでおり、さらにスペーサ15…を備えている。このスペーサ15…は、ソース線32…上の各電極スペースに、画素電極33…の長辺と平行、すなわちストライプ状に配されている。

【0144】上記のように構成される液晶表示装置を実際に作製した。この液晶表示装置の作製においては、前記のように、画素電極33の長辺と短辺とをそれぞれ200～500μm、50～300μmの範囲に設定し、さらに第1の実施の形態における変形例2での手順と同様にして厚さ1．5μmのスペーサ15…を形成した。そして、その液晶表示装置に対し、同様に耐衝撃試験を行った。

【0145】このように作製した全ての液晶表示装置について、ラビング条件を調整することにより、表示領域の全体で均一なC2U配向を容易に得ることができた。また、各液晶表示装置に衝撃を加えても、配向が乱れることはなかった。

【0146】上記の液晶表示装置に対し、図18（a）（b）に示すように、スペーサ15…と同様な材料からなるスペーサ16…が、ゲート線31…上の各電極スペースに、画素電極33…の短辺と平行に配され、かつラビング方向がその短辺と平行な方向である液晶表示装置を比較例として作製した。この液晶表示装置においては、十分な耐衝撃性を得ることができたが、ラビング条件を調整したにも関わらず、ジグザグ欠陥が多く発生し、均一なC2U配向を得ることができなかった。

【0147】なお、図17（a）（b）および図18（a）（b）においては、画素電極33とスペーサ15・16との配置関係を示す便宜上、配向膜7・8等を省略しており、後述の図19（a）（b）についても同様に省略している。

【0148】〔変形例2〕続いて、本実施の形態の他の変形例について説明する。

【0149】本変形例に係る液晶表示装置は、図19（a）（b）に示すように、ガラス基板2上に遮光層18…が交互に組み込まれたマイクロカラーフィルタ17…が形成されている。上記のマイクロカラーフィルタ17…は、オーバーコート層19で覆われており、オーバーコート層19上に共通電極35が形成されている。

【0150】ガラス基板1上に形成される画素電極33…は、1画素分においてR，G，Bの各マイクロカラーフィルタ17…に対応するように配されている。スペーサ15…は、画素電極33の長辺に沿った1画素毎の電極スペースに設けられている。また、電極スペーサ15…は複数画素毎に設けられていてもよい。さらに、ラビング処理は、前記の変形例1と同様の方向に行われる。

【0151】このように構成される液晶表示装置を実際に作製したが、表示領域の全体で均一なC2U配向を得ることができた。また、各液晶表示装置に衝撃を加えても、配向が乱れることはなかった。さらに、スペーサ15…の間隔が1画素単位に設定されているので、液晶材料を注入する際に、全ての画素に十分液晶材料が注入された。

【0152】なお、図示はしないが、空間分割階調を行

う場合、第1の実施の形態の変形例3のように、R，G，Bに対応する画素電極がそれぞれ分割される。

【0153】また、本実施の形態では、スイッチング素子としてTFT34を用いた液晶表示装置について説明したが、これに限らず、画素電極とこれに対向する電極を有する構造であれば、例えばM1M素子を用いた液晶表示装置であってもよい。

【0154】さらに、本実施の形態では、画素電極33…が平行かつ並列に配される構成について述べたが、画素電極33…の配列はこれに限定されない。例えば、R，G，Bに対応する画素電極33が三角形状に配される、いわゆるデルタ配列の構成であってもよい。

【0155】

【発明の効果】以上のように、本発明の請求項1に記載の液晶表示装置は、絶縁性かつ透光性の基板、この基板上にストライプ状に配列される複数の電極およびこれらの電極を覆う配向膜を有し、それぞれの電極が交差するように対向して配される透光性の一対の電極基板と、これらの電極基板間に封入される強誘電性液晶とを備え、上記両電極基板のうち所定範囲における電極数が多い方の電極基板が電極の長手方向と平行またはほぼ平行に一軸配向処理が施される一方、他方の電極基板が電極の長手方向と垂直またはほぼ垂直に一軸配向処理が施され、上記両電極基板に施される一軸配向処理が平行またはほぼ平行となる構成である。

【0156】これにより、所定範囲で数が少ない電極群を横切る方向すなわち配向膜の下地の状態の変化が少ない方向に沿ってスメクチック層が成長する。それゆえ、スメクチック層の成長が妨げられにくくなり、ジグザグ欠陥の発生のない均一な配向状態を得ることができる。したがって、本液晶表示装置を採用すれば、均一かつ高コントラストの表示特性を得ることができるという効果を奏する。

【0157】本発明の請求項2に記載の液晶表示装置は、上記の請求項1に記載の液晶表示装置において、上記両電極基板間の間隔を保持するとともに上記両電極基板を接合する間隔保持体が、所定範囲における電極数が多い方の電極基板の隣り合う電極間に、電極の長手方向と平行にかつストライプ状に配列されている構成である。

【0158】これにより、スメクチック層の成長が間隔保持体によって妨げられることがなく、ジグザグ欠陥の発生のない均一な配向状態を得ることができる。しかも、間隔保持体が両電極基板を接合するので、機械的衝撃により配向が乱れることはない。したがって、本液晶表示装置を採用すれば、耐衝撃性を高めて安定した表示特性を得ることができるという効果を奏する。

【0159】本発明の請求項3に記載の液晶表示装置は、絶縁性かつ透光性の基板、この基板上にストライプ状に配列される複数の電極およびこれらの電極を覆う配向膜を有し、それぞれの電極が交差するように対向して配される透光性の一対の電極基板と、上記電極基板間に封入される強誘電性液晶とを備え、上記両電極基板のうち最も幅の狭い電極を有する方の電極基板が電極の長手方向と平行またはほぼ平行に一軸配向処理が施される一方、他方の電極基板が電極の長手方向と垂直またはほぼ垂直に一軸配向処理が施され、上記両電極基板に施される一軸配向処理が平行またはほぼ平行となる構成である。

【0160】これにより、配向方向が最も幅の狭い電極を含まない電極群を横切る方向すなわち配向膜の下地の状態の変化が少ない方向に沿ってスメクチック層が成長する。それゆえ、スメクチック層の成長が妨げられにくくなり、ジグザグ欠陥の発生のない均一な配向状態を得ることができる。したがって、本液晶表示装置を採用すれば、均一かつ高コントラストの表示特性を得ることができるという効果を奏する。

【0161】本発明の請求項4に記載の液晶表示装置は、上記の請求項3に記載の液晶表示装置において、上記両電極基板間の間隔を保持するとともに上記両電極基板を接合する間隔保持体が、最も幅の狭い電極を有する方の電極基板の隣り合う電極間に、電極の長手方向と平行にかつストライプ状に配列されている構成である。

【0162】これにより、スメクチック層の成長が間隔保持体によって妨げられることがなく、ジグザグ欠陥の発生のない均一な配向状態を得ることができる。しかも、間隔保持体が両電極基板を接合するので、機械的衝撃により配向が乱れることはない。したがって、本液晶表示装置を採用すれば、耐衝撃性を高めて安定した表示特性を得ることができるという効果を奏する。

【0163】本発明の請求項5に記載の液晶表示装置は、絶縁性かつ透光性の基板、この基板上にマトリクス状に配列される複数の画素電極およびこれらの画素電極を覆う配向膜を有する画素電極基板と、絶縁性かつ透光性の基板、この基板上に設けられる対向電極およびこの対向基板を覆う配向膜を有し、対向電極と上記画素電極とが対向するように上記画素電極基板と対向して配される対向電極基板と、上記画素電極基板と上記対向電極基板との間に封入される強誘電性液晶とを備え、上記画素電極基板が上記画素電極の長辺方向と平行またはほぼ平行に一軸配向処理が施される一方、上記対向電極基板が上記画素電極基板に施される一軸配向処理と平行またはほぼ平行となるように一軸配向処理が施されている構成である。

【0164】これにより、配向方向が所定範囲で画素電極同士のスペースの数がより少なくなるように画素電極群を横切る方向すなわち配向膜の下地の状態の変化が少ない方向に沿ってスメクチック層が成長する。それゆえ、スメクチック層の成長が妨げられにくくなり、ジグザグ欠陥の発生のない均一な配向状態を得ることができ

る。したがって、本液晶表示装置を採用すれば、均一かつ高コントラストの表示特性を得ることができるという効果を奏する。

【０１６５】本発明の請求項６に記載の液晶表示装置は、上記の請求項５に記載の液晶表示装置において、上記画素電極基板と上記対向電極基板との間の間隔を保持するとともにその両電極基板を接合する間隔保持体が、隣り合う上記画素電極間に、上記画素電極の長辺方向と平行にかつストライプ状に配列されている構成である。

【０１６６】これにより、スメクチック層の成長が間隔保持体によって妨げられることがなく、ジグザグ欠陥の発生のない均一な配向状態を得ることができる。しかも、間隔保持体が両電極基板を接合するので、機械的衝撃により配向が乱れることはない。したがって、本液晶表示装置を採用すれば、耐衝撃性を高めて安定した表示特性を得ることができるという効果を奏する。

【０１６７】本発明の請求項７に記載の液晶表示装置は、上記の請求項１、３または５に記載の液晶表示装置において、１画素分の表示領域に複数の上記電極または上記画素電極が設けられ、上記間隔保持体が１画素分の表示領域を最小単位として上記電極または上記画素電極を区切る構成である。

【０１６８】これにより、間隔保持体同士の間隔がある程度広く確保される。それゆえ、強誘電性液晶の注入が容易になり、各画素に短時間で十分強誘電性液晶が注入される。また、１画素分の表示領域が間隔保持体により区切られないので、画素内での表示特性が不均一になることはない。したがって、本液晶表示装置を採用すれば、液晶の注入不均一を防止し、良好な表示特性を得ることができるという効果を奏する。

【０１６９】本発明の請求項８に記載の液晶表示装置は、上記の請求項７に記載の液晶表示装置において、１画素分の表示領域当たりに複数設けられるカラーフィルタを備え、１画素分の表示領域内の上記電極または上記画素電極が、同じ表示領域に設けられる複数のカラーフィルタの個々に対応するように設けられている構成であるので、カラー表示の可能な液晶表示装置においても、良好な表示特性を得ることができるという効果を奏する。

【０１７０】本発明の請求項９に記載の液晶表示装置は、上記の請求項７に記載の液晶表示装置において、１画素分の表示領域内の上記電極または上記画素電極が、空間分割階調表示のための分割数に応じて設けられている構成であるので、空間分割階調表示の可能な液晶表示装置においても、良好な表示特性を得ることができる。

【図面の簡単な説明】

【図１】本発明の第１の実施の形態に係る液晶表示装置の要部の構造を示す断面図および電極構造を示す平面図である。

【図２】図１の液晶表示装置とラビング方向を異ならせた液晶表示装置における電極構造とジグザグ欠陥との関係を示す平面図である。

【図３】本発明の第１の実施の形態の変形例１に係る液晶表示装置の電極構造を示す平面図である。

【図４】本発明の第１の実施の形態の変形例２に係る液晶表示装置の電極構造を示す平面図およびこの平面図のＡ－Ａ’線矢視断面図である。

【図５】図４の液晶表示装置とラビング方向を異ならせた液晶表示装置の電極構造を示す平面図およびこの平面図のＢ－Ｂ’線矢視断面図である。

【図６】本発明の第１の実施の形態の変形例３に係る液晶表示装置の電極構造を示す平面図およびこの平面図のＣ－Ｃ’線矢視断面図である。

【図７】本発明の第１の実施の形態の変形例３に係る他の液晶表示装置の電極構造を示す平面図およびこの平面図のＤ－Ｄ’線矢視断面図である。

【図８】本発明の第１の実施の形態の変形例３に係るさらに他の液晶表示装置の電極構造を示す平面図およびこの平面図のＥ－Ｅ’線矢視断面図である。

【図９】図８の液晶表示装置よりさらにスペーサが多く設けられた液晶表示装置の電極構造を示す平面図である。

【図１０】本発明の第２の実施の形態に係る液晶表示装置の要部の構造を示す断面図および電極構造を示す平面図である。

【図１１】図１０の液晶表示装置とラビング方向を異ならせた液晶表示装置における電極構造とジグザグ欠陥との関係を示す平面図である。

【図１２】本発明の第２の実施の形態の変形例１に係る液晶表示装置の電極構造を示す平面図である。

【図１３】本発明の第２の実施の形態の変形例２に係る液晶表示装置の電極構造を示す平面図およびこの平面図のＦ－Ｆ’線矢視断面図である。

【図１４】図１３の液晶表示装置とラビング方向を異ならせた液晶表示装置の電極構造を示す平面図およびこの平面図のＧ－Ｇ’線矢視断面図である。

【図１５】本発明の第３の実施の形態に係る液晶表示装置の要部の構造を示す斜視図および電極構造を示す平面図である。

【図１６】図１５の液晶表示装置とラビング方向を異ならせた液晶表示装置における電極構造とジグザグ欠陥との関係を示す平面図である。

【図１７】本発明の第３の実施の形態の変形例１に係る液晶表示装置の電極構造を示す平面図およびこの平面図のＨ－Ｈ’線矢視断面図である。

【図１８】図１７の液晶表示装置とラビング方向を異ならせた液晶表示装置の電極構造を示す平面図およびこの平面図のＩ－Ｉ’線矢視断面図である。

【図１９】本発明の第３の実施の形態の変形例２に係る液晶表示装置の電極構造を示す平面図およびこの平面図

のＪ－Ｊ’線矢視断面図である。

【図２０】スメクチックＣ相の液晶分子の配列を模式的に示した斜視図および層面の法線の方向から見た正面図である。

【図２１】強誘電性液晶のヘリカルピッチより薄いギャップで対向するセルにおいて、分子の螺旋構造がほどけた状態、液晶分子の長軸と自発分極の向きとが一様に揃えられた状態、およびこの状態から液晶分子の配向が別の状態へと切り替えられた状態を示す斜視図である。

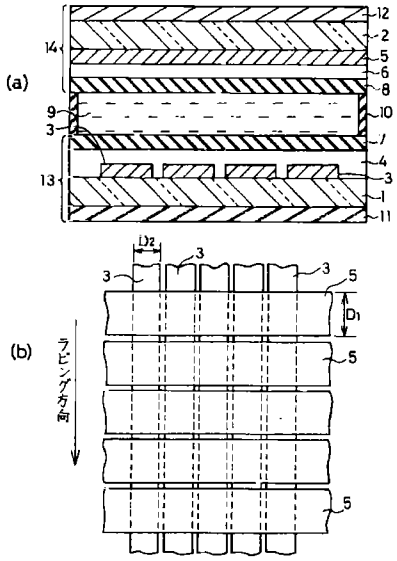
【図２２】各スメクチック層のシェブロン構造を示す正面図である。

【図２３】表示面上に現れたジグザグ欠陥を示す説明図、ジグザグ欠陥を生じさせるシェブロン構造を示す正面図およびジグザグ欠陥の発生部付近の液晶分子の配向状態を模式的に示した斜視図である。

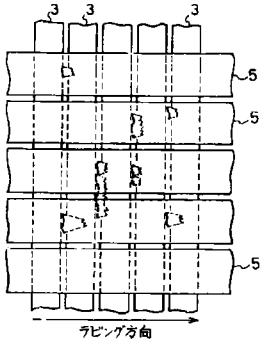
【符号の説明】

３・２１	信号電極（電極）
３ａ～３ｅ	分割電極
５・２２	走査電極（電極）
７・８	配向膜
１３・１４	電極基板
１３’・１４’	電極基板
１５	スペーサ（間隔保持体）
１７	マイクロカラーフィルタ（カラーフィルタ）
３３	画素電極
３５	共通電極（対向電極）
３６	電極基板（対向電極基板）

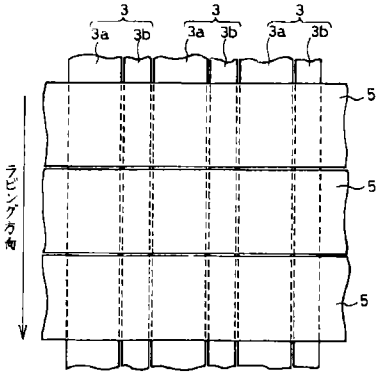
【図１】



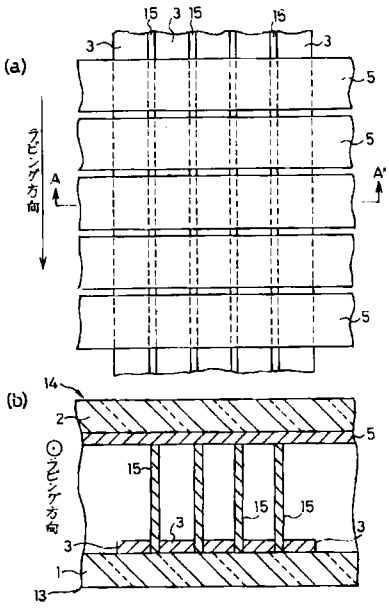
【図２】



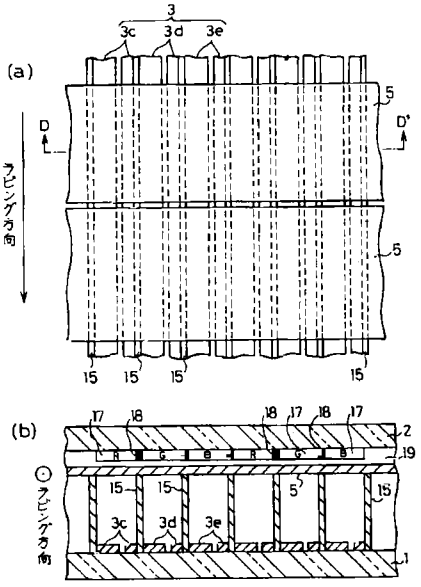
【図３】



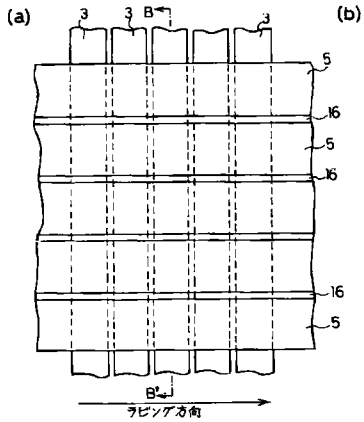
【図4】


(a)
(b)
ラビング方向
A
A'
15
3
5
14
2
1
13
16

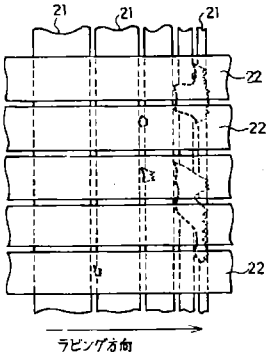
【図7】


(a)
(b)
ラビング方向
D
D'
3
3c
3d
3e
5
15
17
18
19
2
1
R
G
B

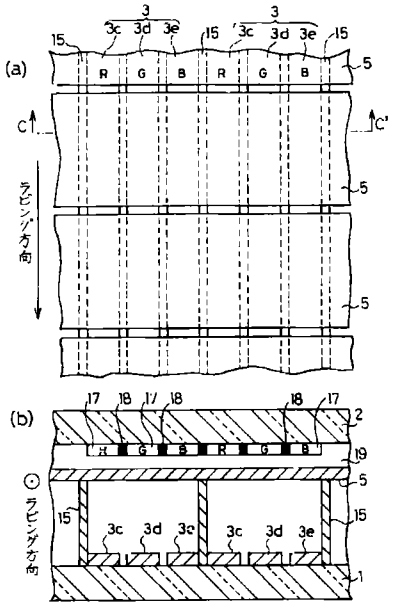
【図5】


(a)
(b)
B
B'
3
5
16
2
1
ラビング方向

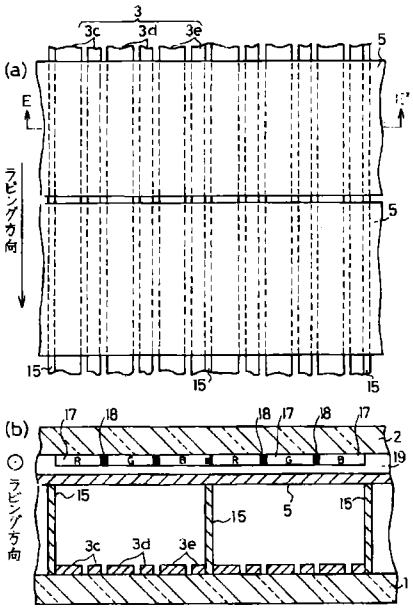
【図11】


21
22
ラビング方向

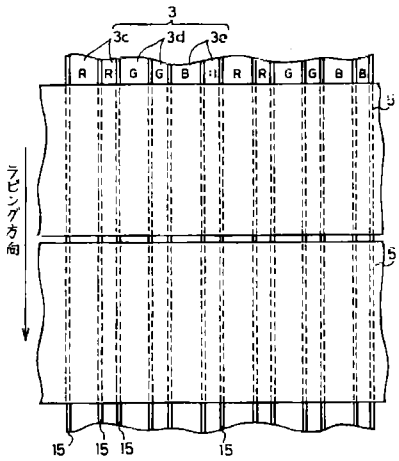
【図6】



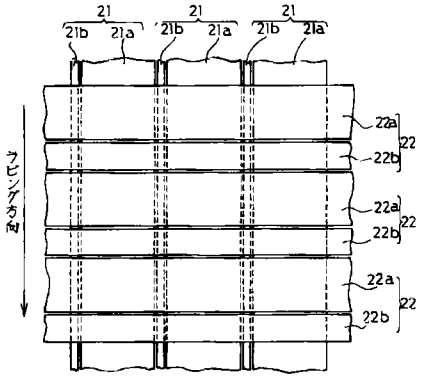
【図8】



【図9】



【図12】



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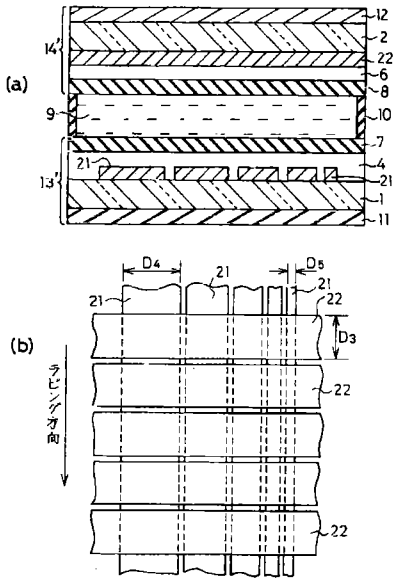
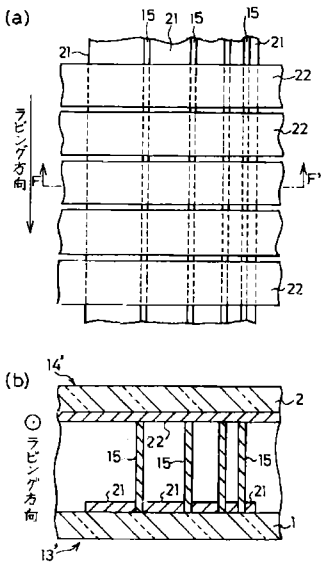
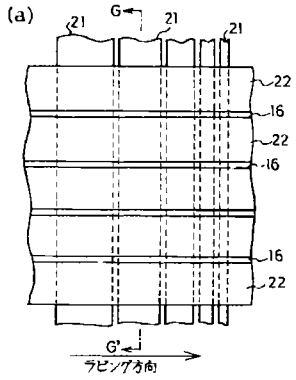


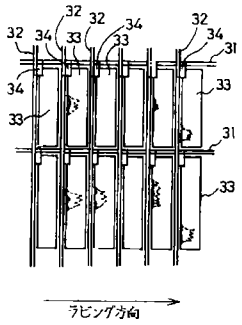
【図13】



【図14】



【図16】



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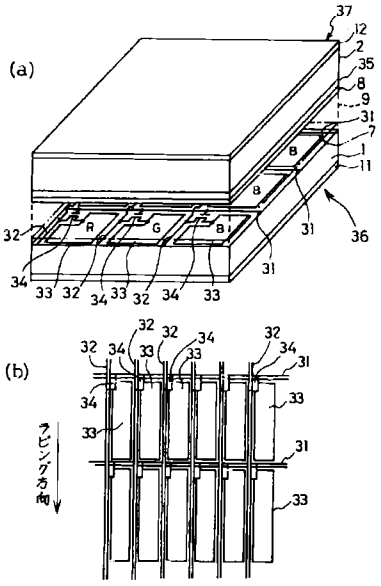
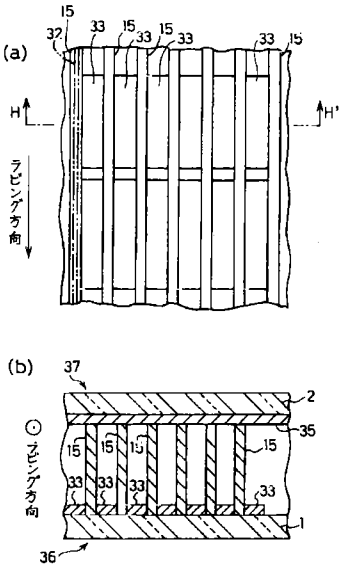
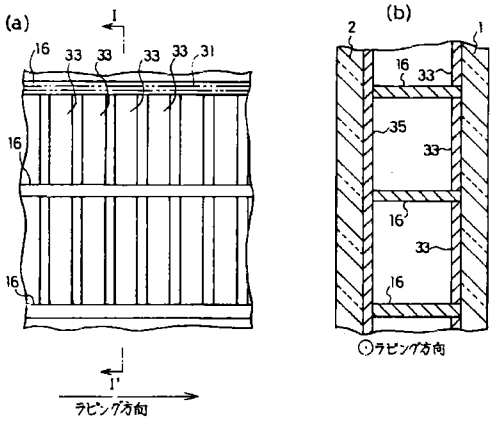


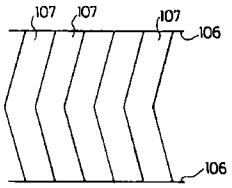
【図17】



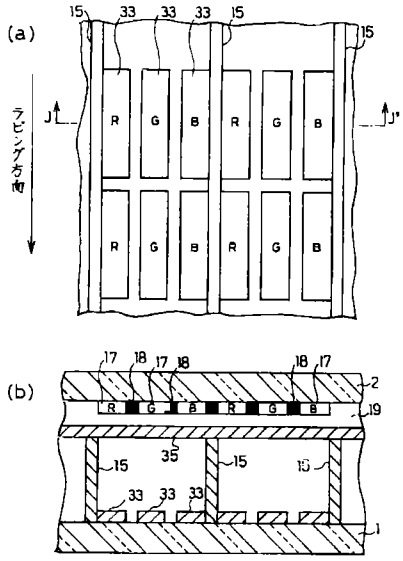
【図18】



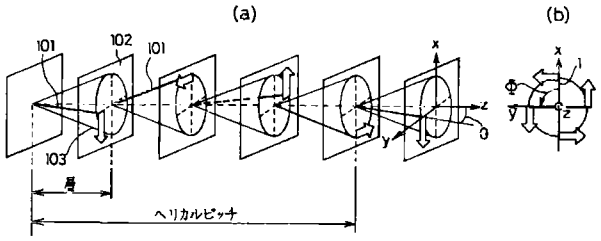
【図22】



【図19】



【図20】



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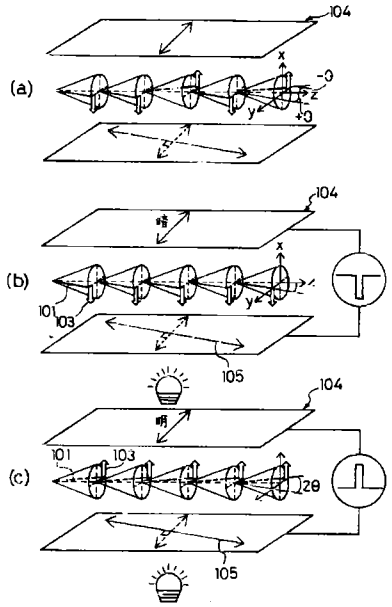
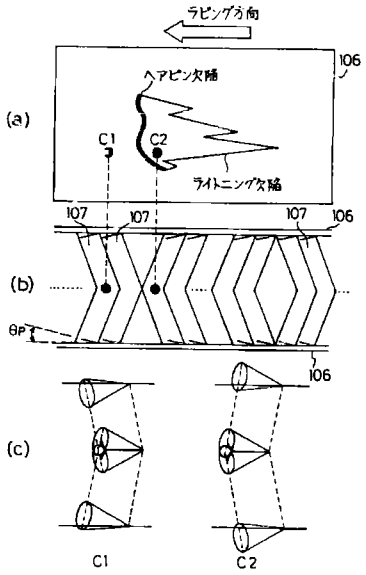


【図23】



フロントページの続き

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THE SECRETARY OF STATE FOR DEFENCE IN HER BRITANNIC MAJESTY'S GOVERNMENT OF THE UNETED KINGDOM OF GREAT BRITAIN AND NORTHERN IRELAND
イギリス国、ジー・ユー・14・6・テイー・デイー、ハンツ、フアーンボロー（番地なし）

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Office Action

Application No.	Application No. 2001-029587
Date of Draft	December 26, 2008
Examiner	Hazime KITAGAWA 9804 2100
Agent	Shinya MAYAMA et al.
Applied Section	Section 29(1), 29(2), 36

This application should be rejected on the grounds described hereunder. When there is any response to the grounds, the applicant can submit an argument within three(3)months from the date of dispatch.

GROUNDS

(Ground 1)
The invention relating to the following claims described hereunder should not be granted in accordance with the provision of Section 29(1)(iii) of Japanese Patent Law because the present invention was described in a following distributed publication, or made publicly available through an electric telecommunication line in Japan or foreign country, prior to the filing of the present patent application.

(Ground 2)
The invention relating to the following claims of the present application should not be granted in accordance with the provision of Section 29(2) of Japanese Patent Law because the present invention could be made easily by a person having an ordinary skilled in the art of the invention based on an invention described in a following distributed publication, or made publicly available through an electric telecommunication line in Japan or foreign country, prior to the filing of the present patent application.

NOTE: (Refer to the list of the references cited with regard to the reference cited)

Claims 1, 3, 7, 9, 12 to 14
Ground 1 and/or 2
Either cited Refs. 1 and/or 2

Remarks:
(Regarding to claim 1 - 1)
In the cited reference, there is the description of an array substrate for display device, comprising:

a thin film transistor array formed on a dielectric substrate (transparent glass substrate, SUB),

multiple wirings formed on the dielectric substrate (scanning signal line GL, video signal line DL),

a connecting pad each disposed on one end of the wirings and each

being connected to said wirings (gate terminal GTM, drain terminal DTM), and

pixel electrodes (transparent pixel electrodes, ITO), wherein dummy conductor patterns (dummy lines DGL, DDL) are disposed between the end of said connecting pad and the terminal of pixel electrode.

(Regarding to claim 1 -2)
In the invention described in the cited reference 2, it is recognized that the connecting pads are provided on one end of the drain wiring DL being connected with drain driver and one end of the gate wiring GL being connected with a gate driver respectively; if the above recognition is not applied, such configuration should be an well-known and commonly used technique so that a person with ordinary skill in the art could be easily reached.
Therefore, in Fig. 5 and Fig. 6 of the cited reference 2, it is deemed that there is the description of the array substrate for display device comprising;

a thin film transistor array formed on the dielectric substrate (transparent dielectric substrate 11a, 21a),

multiple wirings(drain wiring DL, gate wiring GL) formed on the dielectric substrate,

a connecting pad each disposed on one end of the wirings and each being connected to said wirings, and

connecting pad provided on the one end of the wire to be connected to said wires respectively, and

pixel electrodes (pixel electrodes 12, 22), wherein
the dummy conductor patterns (dummy film 5a, dummy electrodes 22a, 22b) are disposed between the ends of said connecting pad and the end of the pixel electrodes; or it is almost deemed that the array substrate for the display device as such could be readily reached by a person with ordinary skill in the art.

(Regarding claim 14)
In the paragraph [0048] of cited reference 2, there is the following description:
"and for the above each embodiment, it was described as one embodiment in which the solid state device to which the film material of the present invention is patterned is applied to the active matrix liquid crystal display device of a poly-silicon type TFT, however the present invention is not limited thereto. For other examples, the solid-state device could be applicable for an amorphous-silicon type TFT active-matrix liquid crystal display device as well as a passive-matrix liquid crystal display device. In addition, the application is not limited for a liquid crystal display device, for example, the present invention could be applicable for devices with which thin film electrodes are patterned on the substrate such as a solar cell."

Therefore, the use of the invention described in cited reference 2 for an electro-luminescence display device could be easily made by a person with ordinary skill in the art.

Claims 2, 8
Ground 2
Any one of Refs. 1 or 2, and Ref. 3

Remarks:
The lines 16-18 of the left-upper column on page 2 in Ref. 3, there is the following description:
"the pattern density which tends to cause side-etching or under-cuts is about less than 25% though it is different depending on the etching condition".
And, in the lines 7-14 of the right-upper column on page 2, there is the following description:
"Provision of this dummy pattern 4b, the density of the entire pattern could be increased to 60% even though the pattern density of the original pattern 4a is 10%.".
Based on the above descriptions of Ref. 3, it could be easily reached by a person with ordinary skill in the art to set the densities of the dummy film 5a and the dummy electrodes 22a, 22b in the invention of Ref. 1 or to set the densities of the dummy lines DGL, DDL in Ref. 2 to be equal to or more than 30 area percents.

Claims 4 to 6, 10, 11
Ground 2
Any one of Refs. 1 or 2 and Ref. 4

Remarks:
In the column [0041] of Ref. 4, there is the following description:
"a gate pattern including a gate line 200, a gate electrode 210 and a gate pad 220 with double layers was formed on the transparent dielectric substrate 100 by layering sequentially an aluminum film or an aluminum alloy film and a molybdenum-tungsten film in the thicknesses of 0.1-0.5 micro-meters and 0.02-0.15 micro-meters, respectively, and then subjected to photo-etching using a first mask.".
In the invention described in either cited Refs. 1 or 2, to form the similar wirings could be easily reached by a person with ordinary skill in the art.

(Ground 3)
This application of which description in claims does not satisfy the requirements prescribed in Article 36 (6)(ii) of Japanese Patent Law with respect to following points.

NOTE
With respect to the description in claim 2, there is the description of "said dummy conductor pattern has more than 30 area %",however it is unclear which part is to be compared with 30 area % of the dummy pattern (with whole substrate, or with the area between the end of connecting pad and terminal of pixel electrode, or other part).
Claim 8 should be argued same as above comments.

Accordingly, the invention relate to the claims 2, 8 and claims 10 to 14 which cites these claims 2 and 8 become unclear.

List of the References Cited

1. Japanese Patent (Laid-Open) Heisei No. 05-061072
2. Japanese Patent (Laid-Open) No. 2000-098909
3. Japanese Patent (Laid-Open) Heisei No. 02-189922
4. Japanese Patent (Laid-Open) Heisei No. 10-240150

Record of the results after search of prior art documents;

Field of search: IPC
G09F 9/00 - 9/30
G02F 1/1345
H01L 21/3205
H05B 33/14 -33/26

Prior Art Reference:
Japanese Patent (Laid-Open) Heisei No. 10-090706
Japanese Patent (Laid-Open) Heisei No. 10-282528

This record of the search of the prior art documents does not compose the Office Action.

When the applicant has any inquiry relating to the contents of this office action, or if you would like an interview, please call to: Tel 03-3581-1101 extension (3274)
Hajime KITAGAWA, Patent Examination First Division.

拒絶理由通知書

特許出願の番号	特願２００１－０２９５８７
起案日	平成２０年１２月２６日
特許庁審査官	北川　創　９８０４　２Ｉ００
特許出願人代理人	間山　進也（外　５名）　様
適用条文	第２９条第１項、第２９条第２項、第３６条

この出願は、次の理由によって拒絶をすべきものです。これについて意見がありましたら、この通知書の発送の日から３か月以内に意見書を提出してください。

理　由

（理由１）

この出願の下記の請求項に係る発明は、その出願前に日本国内又は外国において、頒布された下記の刊行物に記載された発明又は電気通信回線を通じて公衆に利用可能となった発明であるから、特許法第２９条第１項第３号に該当し、特許を受けることができない。

（理由２）

この出願の下記の請求項に係る発明は、その出願前に日本国内又は外国において頒布された下記の刊行物に記載された発明又は電気通信回線を通じて公衆に利用可能となった発明に基いて、その出願前にその発明の属する技術の分野における通常の知識を有する者が容易に発明をすることができたものであるから、特許法第２９条第２項の規定により特許を受けることができない。

記　　（引用文献等については引用文献等一覧参照）

請求項１、３、７、９、１２－１４
理由１または理由２
引用文献１、２のいずれか
備考：
（請求項１について－１）
引用文献１には、
絶縁性基板（透明ガラス基板ＳＵＢ）上に形成された薄膜トランジスタアレイと、該絶縁性基板上に配置された複数の配線（走査信号線ＧＬ、映像信号線ＤＬ

）と、該配線の一端に配置され前記配線にそれぞれ接続される接続パッド（ゲート端子ＧＴＭ、ドレイン端子ＤＴＭ）と、画素電極（透明画素電極ＩＴＯ）とを含む表示用アレイ基板であって、前記接続パッドの端部と画素電極端部との間にダミー導体パターン（ダミー線ＤＧＬ、ＤＤＬ）が配置された表示用アレイ基板が記載されている。

（請求項１について－２）

引用文献２に記載の発明において、ドレインドライバに接続されるドレイン線ＤＬの一端及びゲートドライバに接続されるゲート線ＧＬの一端には、接続パッドを設けられていると認められ、仮にそうでないとしても、そのように構成することは、周知慣用であり、当業者が容易に想到することができたことである。

したがって、引用文献２の図５、図６には、

絶縁性基板（透明絶縁基板１１ａ、２１ａ）上に形成された薄膜トランジスタアレイと、該絶縁性基板上に配置された複数の配線（ドレイン線ＤＬ、ゲート線ＧＬ）と、該配線の一端に配置され前記配線にそれぞれ接続される接続パッドと、画素電極（画素電極１２、２２）とを含む表示用アレイ基板（ＴＦＴアレイ基板１１、２１）であって、前記接続パッドの端部と画素電極端部との間にダミー導体パターン（ダミー膜５ａ、ダミー電極２２ａ、２２ｂ）が配置された表示用アレイ基板

が記載されているか、少なくともそのように構成することは、当業者が容易に想到することができたことである。

（請求項１４について）

引用文献２の【００４８】には、

「また、上記各実施の形態においては、本発明にかかる膜材がパターン形成された固体装置をポリシリコン形ＴＦＴ方式アクティブマトリックス液晶表示装置に適用した例を示したが、これに限定されない。他に例えば、同固体装置をアモルファスシリコン形ＴＦＴアクティブマトリクス液晶表示装置に適用してもよいし、パッシブマトリクス液晶表示装置に適用してもよい。さらに液晶表示装置に限定されず、例えば太陽電池セル等、薄膜電極が基板上にパターン形成されるものであれば同様にこの発明を適用することができる。」

と記載されており、引用文献２に記載の発明を、エレクトロ・ルミネッセンス・ディスプレイ・デバイスとして使用することは、当業者が容易に想到することができたことである。

請求項２、８

理由２

引用文献１、２のいずれかと引用文献３

引用文献３の第２頁左上欄第１６－１８行には、
「サイドエツチングやアンダーカットが生じ易いパターン密度はエツチング条件により異なるが、はぼ２５％以下の場合である。」
と記載され、第２頁右下欄第７－１４行には、
「このダミーパターン４ｂを設けることにより、本来のパターン４ａのパターン密度が１０％の場合にも、パターン全体の密度を６０％に増大することが可能となる。」
と記載されている。

引用文献３の上記記載に基づいて、引用文献１に記載の発明において、ダミー膜５ａ、ダミー電極２２ａ、２２ｂの密度を、または引用文献２に記載の発明において、ダミー線ＤＧＬ、ＤＤＬの密度を、３０面積%以上にすることは、当業者が容易に想到することができたことである。

請求項４－６、１０、１１
理由２
引用文献１、２のいずれかと引用文献４
備考：

引用文献４の【００４１】には、
「透明な絶縁基板１００上にアルミニウム膜またはアルミニウム合金膜とモリブデンータングステン合金膜０．１～０．５μｍ、０．０２～０．１５μｍの厚さで順に積層し第１マスクを用いてホトエッチングしてゲート線２００、ゲート電極２１０およびゲートパッド２２０を含み二重膜からなるゲートパターンを形成する。」
と記載されている。

引用文献１、２のいずれかに記載の発明においても、配線を同様に形成することは、当業者が容易に想到することができたことである。

（理由３）

この出願は、特許請求の範囲の記載が下記の点で、特許法第３６条第６項第２号に規定する要件を満たしていない。

記

請求項２に、「前記ダミー導体パターンは、３０面積%以上である」と記載されているが、ダミー導体パターンが、何に対して（基板全体に対してか、接続パッドの端部と画素電極端部との間の面積に対してか、或いは他のものに対してか）、３０面積%以上であるのか明確でない。

請求項８についても同様。

よって、請求項２、８及びこれらの請求項を引用する請求項１０－１４に係る発明は明確でない。

引　用　文　献　等　一　覧

１．特開平０５－０６１０７２号公報
２．特開２０００－０９８９０９号公報
３．特開平０２－１８９９２２号公報
４．特開平１０－２４０１５０号公報

先行技術文献調査結果の記録

・調査した分野　ＩＰＣ

Ｇ０９Ｆ　９／００　－　９／３０
Ｇ０２Ｆ　１／１３４５
Ｈ０１Ｌ　２１／３２０５
Ｈ０５Ｂ　３３／１４　－　３３／２６

・先行技術文献

特開平１０－０９０７０６号公報
特開平１０－２８２５２８号公報

この先行技術文献調査結果の記録は拒絶理由を構成するものではありません。

この拒絶理由通知書について不明な点があるとき、または、この出願について面接を希望されるときは、下記にご連絡下さい。

特許審査第一部 ナノ物理（エネルギー線応用）　北川　創
ＴＥＬ　０３－３５８１－１１０１　（内線３２７４）

Decision of Final Rejection

Application No.	Application No. 2001-029587
Date of Draft	May 12, 2009
Examiner	Hazime KITAGAWA 9804 2I00
Name of the invention	Array substrate for display, method of manufacturing array substrate for display and display device using the array substrate
Agent	Shinya MAYAMA et al.

This application should be rejected on the grounds 1 and 2 described in Office Action dated December 26, 2008.
Subject matters in arguments and amendments have been examined, however no basis to reverse the previously given reasons for refusal has been found.

Remarks:
The applicant claims the followings in the arguments.

(1) "This application adopts the configuration of describing an array substrate for display, comprising:
(c) a plurality of wiring arranged on the insulating substrate, each wiring having a first end, the wiring in communication with at least one of the transistors in the thin film array,
(d) connection pads, each connection pad contacting the first end of at most one of the plurality of wirings,
(e) pixel electrodes,
(f) a plurality of dummy conductive patterns, each being disposed between any two adjacent connection pads and corresponding pixel electrode surrounds, and
(g) pixel electrodes wherein said dummy conductive patterns are not in contact with any of the wiring in the area."

"However the cited reference 1 only discloses the configuration of disposing dummy conductive patterns in outside of each signal conductor, and above adoption of configuration (d) and (e) in this application is not disclosed nor indicated."

(2) "In addition to the above differences, referring the cited reference 2, even though it is disclosed that the dummy films are formed in surrounding area of film materials to protect the film materials from damages when they are brush-washed, but the dummy films are formed on multiple wirings to cover the pixel electrode in accordance with specification (0026) and fig.1, and does not adopt the configuration described as (c),(d),and(f), in this application. Furthermore, the dummy film in cited reference 2 is formed in completely different level from the level of forming the wiring, and therefore it is clear that the dummy film has no function at the time of forming the wiring and

has completely different function."

(3)" In the cited reference 1, the dummy conductive patterns are disposed in outside of signal wirings placed in outermost edge, to prevent the cleavage of wires of the signal conductor placed in the outermost edge. And for the cause of the cleavage of wires, there are limited descriptions as the difference in etching conditions and/or the adhesion of some strains in specification (0005) and (0006), and therefore the dummy conductive patterns do not have such function described in this application as to prevent the undercut of wirings."

(4)" In addition to the above, even referring to the specification 0025 of cited reference 2, there is only the description that TFT source electrodes are connected with the pixel electrodes 12 formed on the insulating substrate 11, and the dummy film of the cited reference 2 is not formed in the forming step of wirings as described in the application and therefore the function of the dummy film is completely different respectively, with the consideration of the relation among gate line GLs, pixel electrodes 13, and contact hall shown in fig 1."

Consideration of the above (1) claimed by applicant.

As described in Office Action, the invention described in the cited reference 1 comprising;
(d) connection pads(gate terminal GTM, drain terminal DTM) to connect with one wiring out of multiple wirings at the first terminal end of wirings(scanning signal line GL, image signal line DL),
(e)pixel electrodes (transparent pixel electrode ITO1),

Therefore, no rational is found in the argument by the applicant that the invention described in cited reference 1 does not disclose and indicate the configuration of the invention (d) and (e) relating claim 1 of present application.

Consideration of the above (2) claimed by applicant.

As described in Office Action, it is recognized that the connecting pads are disposed on one end of drain line DL for connecting drain driver and one end of gate line GL for connecting with gate driver in the invention described in cited reference 2, and even if it is not the case, it is well-known and commonly used art and could be reached by a person skilled in the art.

Consequently in the invention described in the cited reference 2, at least the following configurations could be easily reached by a person skilled in the art.
(c) a plurality of wiring (drain line DL, gate line GL)arranged on the insulating substrate (transparent insulating substrate 11a, 21a), each wiring having a first end, the wiring in communication with at least one

of the transistors in the thin film array,
(d) connection pads, each connection pad contacting the first end of at most one of the plurality of wirings,
(f) a plurality of dummy conductive patterns(dummy film 5a, dummy electrode 22a, 22b), each being disposed between any two adjacent connection pads and corresponding pixel electrode surrounds,

And ,with regard to the applicant's assertion in argument (2) as "level of forming the dummy film is formed to be in completely different level from the level of forming the wirings, it is obvious that the dummy film has no function at the time of forming wirings, and each function is completely different respectively", there are no restricted descriptions of the level of forming dummy conductive patterns and wirings, and the function of the dummy conductive pattern in the claim of the present application. And the invention relating to Claim 1 includes the invention to have different forming level for dummy conductive film from the level for forming wiring and different function.

Consideration of the above (3) claimed by applicant.

In Claim 1 of this application, there are no restricted descriptions of the function of dummy conductive patterns, and the invention relating to Claim 1 of this application includes the invention described in the cited reference 1.

Consideration of the above (4) claimed by applicant.

In Claim 1 of this application, there are no restriction for forming dummy conductive patterns in the step of forming wirings, and hence the invention relating to Claim 1 of this application includes the invention described in the cited reference 2.

Consequently any of the above argued points by applicant could not be accepted.
And it is recognized that the similar configuration is described in cited reference 1 and 2, with regard to the description of (g) "said dummy conductive patterns are not in contact with any of the wirings in said area." , of which descriptions are added to the claim 1 of this application by amendment.

With the all above considerations, the invention relating to the amended claims 1-14 of this application should not be granted in accordance with the provision of Section 29(1)(iii) and Section 29(2) of Japanese Patent Law because the present invention was described in the cited reference 1 and 2, and/or could be made easily by a person having an ordinary skill in the art of the invention based on the cited reference 1-4 described in said Office Action.

When there is a complaint against this decision, the applicant can request

the trial to the commissioner of Japan Patent Office within three(3) months (four(4) months for the absentee) from the date of dispatch. (Section 121(1) of Japanese Patent Law)

(Instructions under Section 46(2) of Administrative Procedure Law) Only the trial for cancellation against the decision for the Request of Trial can be requested in this decision of final rejection. (Section 178(6) of Japanese Patent Law)

I certify that matters described above are identical with those recorded on the file.
Date of certification May 13, 2009
Makoto YOSHIKOSHI
Administrative Officer, Ministry of Economy and Industry

拒絶査定

特許出願の番号	特願２００１－０２９５８７
起案日	平成２１年　５月１２日
特許庁審査官	北川　創　９８０４　２Ｉ００
発明の名称	表示装置用アレイ基板、アレイ基板の製造方法、および該アレイ基板を用いた表示デバイス
特許出願人	エーユー　オプトロニクス　コーポレイション
代理人	間山　進也（外　５名）

この出願については、平成２０年１２月２６日付け拒絶理由通知書に記載した理由１及び理由２によって、拒絶をすべきものです。

なお、意見書及び手続補正書の内容を検討しましたが、拒絶理由を覆すに足りる根拠が見いだせません。

備考：

出願人は、意見書において以下の旨主張している。

（１）「本願は、

（ｃ）該絶縁性基板の上に配置され、それぞれが第１の端部を有し、前記薄膜トランジスタアレイの少なくとも１つに接続され、複数の材料が積層されてなる複数の配線と、

（ｄ）該配線の前記第１の端部において前記複数の配線のうちの１の配線に接続する接続パッドと、

（ｅ）画素電極と、

（ｆ）隣接する２つの前記接続パッドおよび対応する画素電極の端部の間の領域に配置された複数のダミー導体パターンと、

（ｇ）前記ダミー導体パターンは、前記領域内の前記配線に非接続とされる、表示用アレイ基板

の構成を採用する点で、引例１では、ダミー導体パターンが各信号導体よりも外側に配置される構成を開示するのみであり、本願の上記構成（ｄ）および（ｅ）を採用する点については何ら開示および示唆するものではありません。」

（２）「さらに上記相違点について、引例２を参照しても、引例２では、ブラシ洗浄を行う際に膜材の損傷を防止するために、膜材の周囲にダミー膜を形成する点を開示するものではありますが、当該ダミー膜は、明細書（００２６）および図１などを参照すれば、画素電極を包囲するように複数の配線にまたがって形成されており、本願の（ｃ）、（ｄ）、（ｆ）の構成を採用するものではありませんし、さらに、引例２のダミー膜は、配線の形成されるレベルとはまったく異な

るレベルに形成されるのであって、配線形成時には何らの機能を果たすものではないことは明らかであり、その機能はまったく相違するものであります。」
（３）「引例１では、最外縁の信号導体の割線を防止するために、当該最外縁の信号線の外部にダミー導体パターンを配置するものであり、その割線の原因についても、明細書（０００５）段落および（０００６）段落を参照すれば、割線の理由として単にエッチング条件の相違や汚れの付着を記載するのみであり、本願のように、配線のアンダーカットを防止する機能を有するものではありません。」
（４）「さらに引例２を参照しても、引例２では、明細書（００２５）段落を参照すれば絶縁性基板１１上に形成された画素電極１２に対し、ＴＦＴのソース電極が接続されていることが記載されており、また、図１を参照すればゲートラインＧＬｓと、画素電極１３と、コンタクトホールとの関係からしても、引例２のダミー膜は、本願のように、配線の形成工程において形成されるものではなく、その機能はまったく相違するものであります。」

上記出願人の主張（１）について検討する。拒絶理由通知書にも記載のように、引用文献１に記載の発明は、
（ｄ）配線（走査信号線ＧＬ、映像信号線ＤＬ）の第１の端部において複数の配線のうちの１の配線に接続する接続パッド（ゲート端子ＧＴＭ、ドレイン端子ＤＴＭ）と、
（ｅ）画素電極（透明画素電極ＩＴＯ１）と
を有している。引用文献１に記載の発明は、本願請求項１に係る発明の構成（ｄ）および（ｅ）を開示および示唆しないとの出願人の主張は根拠がない。

上記出願人の主張（２）について検討する。拒絶理由通知書にも記載のように、引用文献２に記載の発明において、ドレインドライバに接続されるドレイン線ＤＬの一端及びゲートドライバに接続されるゲート線ＧＬの一端には、接続パッドを設けられていると認められ、仮にそうでないとしても、そのように構成することは、周知慣用であり、当業者が容易に想到することができたことである。
したがって、引用文献２に記載の発明において、
（ｃ）該絶縁性基板（透明絶縁基板１１ａ、２１ａ）の上に配置され、それぞれが第１の端部を有し、薄膜トランジスタアレイの少なくとも１つに接続され、複数の材料が積層されてなる複数の配線（ドレイン線ＤＬ、ゲート線ＧＬ）と、
（ｄ）該配線の前記第１の端部において前記複数の配線のうちの１の配線に接続する接続パッドと、
（ｆ）隣接する２つの前記接続パッドおよび対応する画素電極（画素電極１２、２２）の端部の間の領域に配置された複数のダミー導体パターン（ダミー膜５ａ、ダミー電極２２ａ、２２ｂ）と
を有するよう構成することは、少なくとも当業者が容易に想到することができた

ことである。

また、上記出願人の主張（２）における「引例２のダミー膜は、配線の形成されるレベルとはまったく異なるレベルに形成されるのであって、配線形成時には何らの機能を果たすものではないことは明らかであり、その機能はまったく相違するものであります。」との主張については、本願請求項１において、ダミー導体パターンと配線の形成されるレベルやダミー導体パターンの機能について限定されておらず、本願請求項１に係る発明は、引用文献２に記載のような、ダミー膜が配線の形成されるレベルとは異なるレベルに形成され、機能も相違する発明を含んでいる。

上記出願人の主張（３）について検討する。本願請求項１において、ダミー導体パターンの機能について限定されておらず、本願請求項１に係る発明は、引用文献１に記載の発明を含んでいる。

上記出願人の主張（４）について検討する。本願請求項１において、ダミー導体パターンが配線の形成工程において形成されることは限定されておらず、本願請求項１に係る発明は、引用文献２に記載の発明を含んでいる。

したがって、上記出願人の主張はいずれも採用することができない。

また、補正により、本願請求項１に追加された（ｇ）「前記ダミー導体パターンは、前記領域内の前記配線に非接続とされる」との事項についても、引用文献１、２は、いずれも同様の構成を有していると認められる。

以上から、補正後の本願請求項１－１４に係る発明は、上記拒絶理由通知書に引用した引用文献１、２に記載された発明であるか、引用文献１－４から当業者が容易に発明をすることができたものであるから、特許法第２９条第１項第３号及び第２項から、特許を受けることができない。

この査定に不服があるときは、この査定の謄本の送達があった日から３月以内（在外者にあっては、４月以内）に、特許庁長官に対して、審判を請求することができます（特許法第１２１条第１項）。

（行政事件訴訟法第４６条第２項に基づく教示）

この査定に対しては、この査定についての審判請求に対する審決に対してのみ取消訴訟を提起することができます（特許法第１７８条第６項）。

上記はファイルに記録されている事項と相違ないことを認証する。

認証日　平成21年 5月13日　経済産業事務官　吉越　誠

Appeal Decision

Appeal No.2003-13340

Appellant: International Business Machines Corporation
New Orchard Road, Armonk, New York 10504, U.S.A.

Representative Patent Attorney: Hiroshi Sakaguchi
IBM Japan, Ltd., Yamato complex, 1623-14 Shimotsuruma, Yamato-shi, Kanagawa

Representative Patent Attorney: Yoshihiro Ichii
IBM Japan, Ltd., Yamato complex, 1623-14 Shimotsuruma, Yamato-shi, Kanagawa

Sub Representative Patent Attorney: Mitsuo Matsui
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Sub Representative Patent Attorney: Yuko Igarashi
Nishishinbashi YS Bldg., 3F, 19-2, Nishishinbashi 2-chome, Minato-ku, Tokyo

The appeal case against examiner's decision of rejection of the Japanese Patent Application No.H-122923, laid open on November 24, 2000, with Laid-Open No.2000-321580, is concluded as follows.

Conclusion

Appeal is not approved.

Reasons

1. Prosecution History

The present application is filed on April 28, 1999. The decision of the rejection was made on April 7, 2003, against which an appeal was filed on July 11, 2003 with an amendment according to the Japanese Patent Low Art. $17^{bis}(1)$, item 3.

2. Decision to Decline Amendment Submitted on July 11, 2003

[Conclusion]

The amendment Submitted on July 11, 2003 is declined.

[Reasons]

(1) Amendment

The amendment includes the following amendment to Claim 1:

"1. A liquid crystal display comprising:

first and second substrates facing each other,

columnar spacers for regulating a cell gap between the both substrates, said spacers being made from a photosensitive resin and disposed solely in a non-display region of either or both of the first and the second substrates and having a hardness (DH) of from 26 to 30, and

liquid crystal sandwiched between the first and the second substrates."

The above amendment is intended to narrow the scope of the invention by limiting shape and location of the spacers. Then, it is examined whether or not the amended claim 1 is independently patentable at the time of filing of the present patent application.

(2) Inventions described in the cited references

The cited reference 1, Japanese Patent Application Laid-Open No.6-273774, describes the followings.

"[0004] [Problems to be solved by the invention]

The present invention was made to solve the aforesaid problems. An object of the present invention is to provide a spacer for a liquid crystal display and a liquid crystal display comprising the same, which spacer is plastic, and has high hardness and modulus of elasticity and thereby enables one to regulate a gap easily, reduce the number of the spacers per area, and improve display quality.

...

[0019] Firstly, K value that defines a hardness of the spacer is explained.

...

[0024] This K value universally and quantitatively represents a hardness of a spherical body. By using the K value, a hardness of the spacer can be represented quantitatively and unambiguously.

...

[0026] A spacer having a K value higher than 1500 kgf/mm^2 is so hard that it may damage a surface of a film used for aligning liquid crystal during a manufacturing process of a liquid crystal display. Further, it may cause bubbles to form in the liquid crystal display when a temperature lowers, because it does not compressively deform according to shrinkage of a liquid crystal.
[0027] A spacer having a K value smaller than 500 kgf/mm^2 is too soft to control a gap between substrates. The number of distributed spacer per area should be larger, which may decrease display contrast."

A document showing state of art technology, Japanese Patent Application Laid-Open No.8-286194, hereinafter referred to as well-known document 1, describes the followings.
"[0045] (Preparation of a spacer) Using the photosensitive resin composition prepared in Synthesis Example 2, ... a film of the photosensitive resin composition having a uniform thickness of 5.5 m was obtained. Then, through a photomask which has a pattern for exposing only a part of the light shielding parts to a light having a diameter of 12 m, UV light of 365 nm wavelength was irradiated to the photosensitive composition film with an exposure does of 150 mJ/cm^2. The pattern was developed with a 2.4 wt% aqueous solution of tetramethylammonium hydroxide solution and thereby spacers made from the photosensitive composition were formed only in the part of the light shielding parts. After washing with pure water the color filter substrate with the spacers patterned thereon, the spacers made from the photosensitive composition were heat-cured at 180 °C for 2 hours. As a result, 5- m high resin spacers having a high compression strength and elasticity were obtained.
[0046] (Assembling of a liquid crystal display) By using the color filter substrate having the resin spacers and the electrode substrate with a transparent electro-conductive layer formed thereon, and then filling a gap between the two substrates with a liquid crystal composition for a TFT, LIXON 5005, ex Chisso Corp., a TFT liquid crystal display was assembled. The display had little variation in its cell gap, no display heterogeneity, no color heterogeneity, and no fringe pattern. Because there is no spacer in the effective display

area, an image with high quality was obtained without dark dots, and low contrast and quality due to misalignment of liquid crystal caused by a spacer. Figure 1 is an enlarged longitudinal sectional view of the liquid crystal display thus obtained. The liquid crystal display 11 comprises the color filter substrate 5a having the spacers shown in Figure 5, the electrode substrate 12 having no color filter, and liquid crystal 13 sandwiched between the both substrates arranged in parallel with a gap therebetween maintained constant with the spacers 10. "

In Fig.5 which is a enlarged sectional view of the color filter provided with the spacer, a columnar spacer 10 is described on the light shielding 8.

The well-known document 1 thus describes a liquid crystal display which has no spacer in its effective display area and comprises the color filter substrate 5a having the columnar spacers which are made from a photosensitive resin and have high compression strength and elasticity, the electrode substrate 12 having no color filter, and liquid crystal 13 sandwiched between the both substrates arranged in parallel with a gap therebetween maintained constant with the spacers.

Another document showing state of art technology, Japanese Patent Application Laid-Open No.1-134336, hereinafter referred to as well-known document 2, describes the followings.

"Claim 1. A liquid crystal display comprising a pair of substrates having electrodes, alignment layers formed on the substrates, and spacers, said spacers being fixed on at least one of said alignment layers formed on the substrates and arranged in dots.";

"The number of the spacer 11 may be determined at will and enough number of spacers can be formed to resist a pressure applied to the spacers. ... The spacers can be formed outside the pixel array on the alignment layer ... and thereby image quality is improved."

Figs. 1 (a) to (d) and related description in the specification

show that a photosensitive polyimide 3 is applied on the alignment layer of the substrate 2 with electrodes; a predetermined area of the applied polyimide is exposed to a light; and spacers are formed after removing unexposed polyimide. Figs. 1 and 3 show columnar spacers and Fig.5 shows a cross sectional view of a liquid crystal display having a liquid crystal sandwiched between a pair of substrates with electrodes.

The well-known document 2 thus describes a liquid crystal display comprising a pair of substrates having electrodes, columnar spacers made from a photosensitive polyimide, and a liquid crystal sandwiched between said pair of substrates, said spacers formed outside the pixel area of at least one of said substrates having electrodes.

Still another document showing state of art technology, Japanese Patent Application Laid-Open No.9-127513, hereinafter referred to as well-known document 3, describes the followings.

"Claim 1. A liquid crystal display comprising

a first electrode substrate having a first electrode and a first light shielding means,

a second electrode substrate having a second electrode and a second light shielding means, said second electrode substrate facing the first electrode substrate with a gap between the second electrode substrate and the first electrode substrate,

a means to maintain said gap, said mans being made from a photosensitive resin and provided at an intersection of the first light shielding means and the second light shielding means, and

a liquid crystal composition held in the gap.";

"[0072]

[Effects of the invention] As explained above, by subjecting a photosensitive resin applied on the electrode substrate to exposure and development processes, columnar spacers can be formed easily only in non-display area with low cost in a short period of time. The gap between the both electrode substrates can be uniformly maintained, so that there is no decreased contrast or image heterogeneity caused by conventional spacers. Further, image quality can be improved and