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(54) **ARRAY SUBSTRATE FOR DISPLAY, METHOD OF MANUFACTURING ARRAY SUBSTRATE FOR DISPLAY AND DISPLAY DEVICE USING THE ARRAY SUBSTRATE**

(75) Inventors: **Takatoshi Tsujimura**, Fujisawa (JP); **Atsuya Makita**, Sagamihara (JP); **Toshiaki Arai**, Yokohama (JP)

(73) Assignee: **AU Optronics Corporation**

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USPC **438/25**; 438/149; 438/73; 257/72; 257/748

(58) **Field of Classification Search**
None
See application file for complete search history.

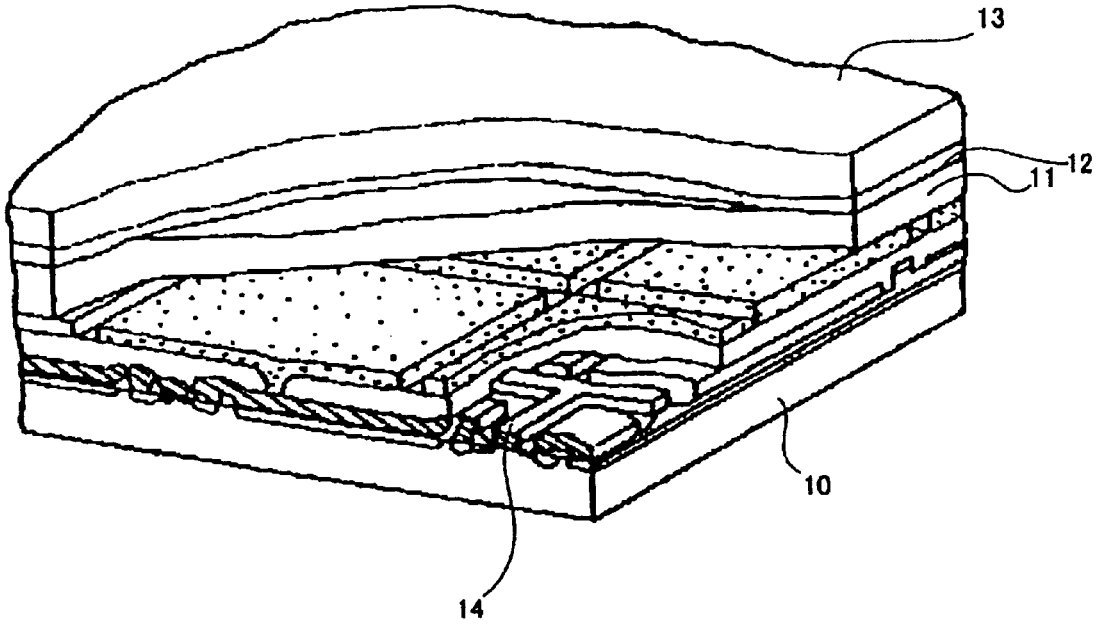
(56) **References Cited**

To view the complete listing of prior art documents cited during the proceeding for Reexamination Control Number 90/009,697, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

Primary Examiner — Tuan H Nguyen

(57) **ABSTRACT**

Disclosed is to provide an array substrate for display, a method of manufacturing the array substrate for display and a display device using the array substrate for display.
The present invention is an array substrate for display, which includes: a thin film transistor array formed on an insulating substrate **1**; a plurality of wirings **23** and **24** arranged on the insulating substrate **1**; connection pads **25** and **27** arranged on unilateral ends of the wirings **23** and **24** and respectively connected therewith; and pixel electrodes **22**, wherein dummy conductive patterns **29** are arranged between the ends of the connection pads **25** and **27** and ends of the pixel electrodes **22**.



EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **2**, **4**, **10**, **12** and **13** are cancelled.

Claims **1**, **3**, **7**, **9**, **11** and **14-16** are determined to be patentable as amended.

Claims **5**, **6** and **8**, dependent on an amended claim, are determined to be patentable.

New claim **17** is added and determined to be patentable.

1. An array substrate for display, comprising:

[a layer of**]** an insulating substrate**[**, having an area**]**;

a thin film transistor array **[**formed**]** on the insulating substrate;

a plurality of **[**wiring arranged**]** *wirings* on the insulating substrate, each wiring having a first end, **[**the**]** *each* wiring in communication with at least one **[**of the transistors**]** *transistor* in the thin film *transistor* array, *and at least one of the wirings comprising at least an upper layer and a lower layer of conductive materials, wherein the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof*;

a plurality of connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

a plurality of pixel electrodes**[**,**]**; and

a plurality of dummy conductive patterns *on the insulating substrate, wherein* the *plurality of* dummy *conductive* patterns **[**comprising**]** *comprises* at least about 30% of **[**the**]** *an* area of the insulating substrate**[**, the dummy conductive patterns situated**]** between the connection pads and the pixel electrodes **[**such that**]**, *and* the dummy **[**patters**]** *conductive patterns* are not in contact with any of the **[**wiring**]** *wirings*.

3. The array substrate for display according to claim **[2]** *1* wherein the lower layer wiring material is selected from the group consisting of aluminum and aluminum alloys.

7. The array substrate for display according to claim **[4]** *1* wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

9. A **[**meted**]** *method* for forming an array substrate for display, comprising:

forming a layer of an insulating substrate**[**, having an area**]**;

forming a thin film transistor array **[**formed**]** *on the insulating substrate;*

forming a plurality of wirings on the insulating substrate, each wiring having a first end, **[**the**]** *each* wiring in communication with at least **[**on of the transistors**]** *one transistor* in the thin film *transistor* array*, wherein at least one of the wirings comprises at least an upper layer and a lower layer of conductive materials, and the upper layer wiring material is selected from the group consisting of molybdenum, chromium, tantalum, titanium and alloys thereof*;

forming *a plurality of* connections pads, each connection pad contacting the first end of at most one of the plurality of wirings;

forming *a plurality of* pixel electrodes**[**,**]**; and

forming *a plurality of* dummy conductive patterns *on the insulating substrate, wherein* the *plurality of* dummy conductive patterns **[**comprising**]** *comprises* at least about 30% of **[**the**]** *an* area of the insulating substrate**[**, the dummy patterns situated**]** between the connection pads and the pixel electrodes **[**such that**]**, *and* the dummy **[**patters**]** *conductive patterns* are not in contact with any of the **[**wiring**]** *wirings*.

11. The method for forming an array substrate for display according to claim **[10]** *9* wherein the lower layer wiring materials is selected from the group consisting of aluminum and aluminum alloys.

14. The method for forming an array substrate for display according to claim **[13]** *9* wherein the upper wiring material is selected from the group consisting of molybdenum and alloys thereof.

15. The method for forming an array substrate for display according to claim **[12]** *9* wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

16. The method for forming an array substrate for display according to claim **[13]** *9* wherein the upper layer wiring material is selected such that the upper layer wiring material does not become insoluble in an acid or alkaline etchant.

17. An array substrate for display, comprising:

an insulating substrate;

an array of thin film transistors on the insulating substrate;

a plurality of wirings on the insulating substrate, each wiring having a first end, and each wiring directly connecting with at least one thin film transistor in the array;

a plurality of connections pads, each connection pad contacting the first end of at most one of the plurality of wiring

a plurality of pixel electrodes; and

a plurality of dummy conductive patterns on the insulating substrate, wherein the plurality of dummy conductive patterns comprises at least about 30% of an area of the insulating substrate between the connection pads and the pixel electrodes.

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