

*Elements  
of Chemical  
Reaction  
Engineering*  
*Second Edition*

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TABLE 11-1

Type of Limitation	Variation of Reaction Rate with:		
	Velocity	Particle Size	Temperature
External diffusion	$U^{1/2}$	$(d_p)^{-3/2}$	$\approx$ Linear
Internal diffusion	Independent	$(d_p)^{-1}$	Exponential
Surface reaction	Independent	Independent	Exponential

If an industrial reaction is not mass transfer-limited, it is probably run incorrectly.

L. D. Schmidt, U. of Minn.

through the bed, particle diameter, and temperature for the three types of limitations we have been discussing.

The exponential temperature dependence for internal diffusion limitations is usually not as strong a function of temperature as is the dependence for surface reaction limitations. If we would calculate an activation energy between 8 and 24 kJ/mol, chances are that the reaction is strongly diffusion-limited. An activation energy of 200 kJ/mol, however, indicates that the reaction is reaction rate-limited.

## 11.8 Chemical Vapor Deposition (CVD) Reactors

As discussed in Section 6.6, CVD is a very important process in the microelectronics industry. The fabrication of microelectronic devices may include as few as 30 or as many as 200 individual steps to produce chips with up to  $10^6$  transducers per chip. An abbreviated schematic of the steps involved in producing a typical computer chip is shown in Figure 11-11.

Starting from the upper left we see that single crystal silicon ingots are grown in a Czochralski crystalizer, then sliced into wafers, and chemically and physically polished. These polished wafers serve as a starting material for a variety of microelectronic devices. A typical fabrication sequence is shown for processing the wafer beginning with the formation of an  $\text{SiO}_2$  layer on top of the silicon. The  $\text{SiO}_2$  layer may be formed either by oxidizing a silicon layer or by laying down a  $\text{SiO}_2$  layer by Chemical Vapor Deposition (CVD). Next the wafer is masked with a polymer photoresist (PR), a template with the pattern to be etched onto the  $\text{SiO}_2$  layer is placed over the PR and the wafer is exposed to ultraviolet irradiation. If the mask is a positive PR, the light will cause scission in the polymer so that the exposed areas will dissolve when the wafer is placed in the developer. On the other hand, when a negative PR mask is exposed to ultraviolet irradiation, crosslinking of the polymer chains occurs and the *unexposed* areas dissolve in the developer. The undeveloped portion of the PR (in either case) will protect the covered areas from etching.

After the exposed areas of  $\text{SiO}_2$  are etched to form trenches (either by wet etching (see P5-11) or plasma etching), the remaining PR is removed. Next the wafer is placed in a furnace containing gas molecules of the desired

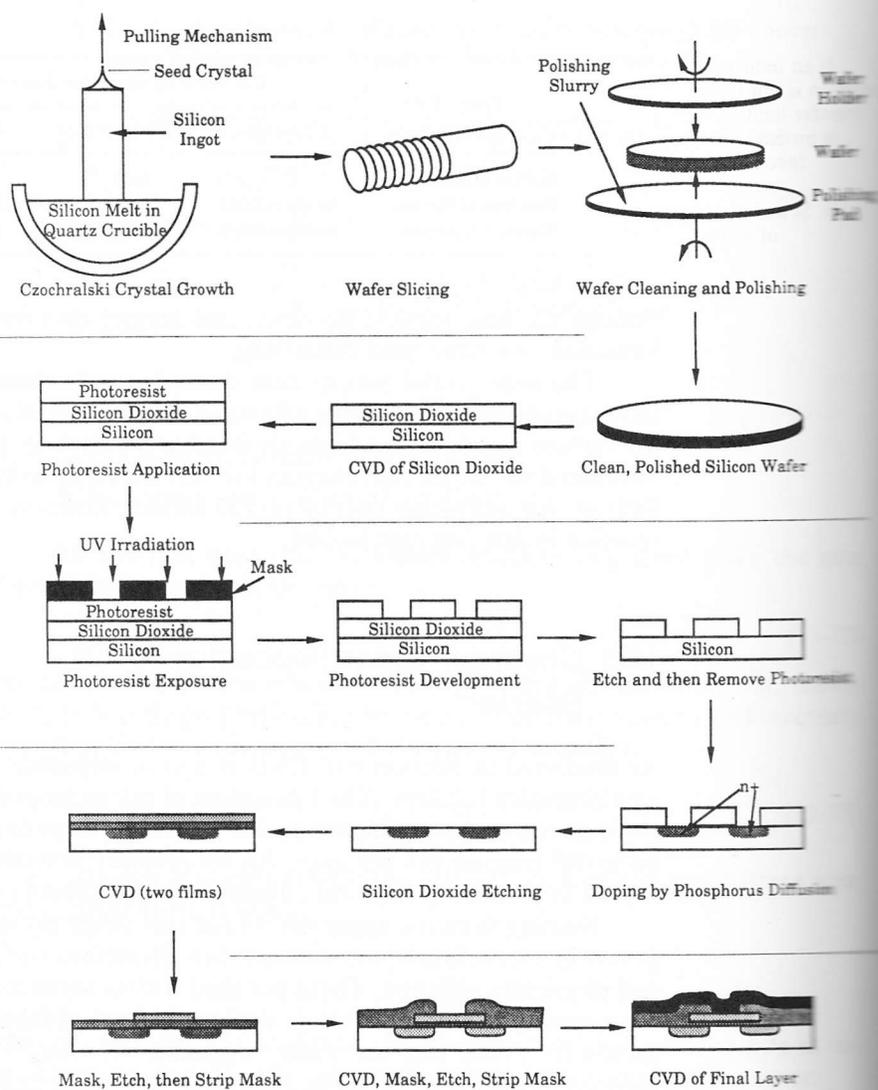


Figure 11-11 Microelectronic fabrication steps.

dopant, which then diffuse into the exposed silicon. After diffusion of dopant to the desired depth in the wafer it is removed and then covered with  $\text{SiO}_2$  by CVD. The sequence of masking, etching, CVD, and metallization continues until the desired device is formed. A schematic of a final chip is shown in the lower right-hand corner of Figure 11-11.

One of the key steps in the chip making process is the deposition of different semiconductors and metals on the surface of the chip. This step can be achieved by CVD. CVD mechanisms were discussed in Chapter 6; consequently this section will focus on CVD reactors. A number of CVD reactor types have been used, such as barrel reactors, boat reactors, and

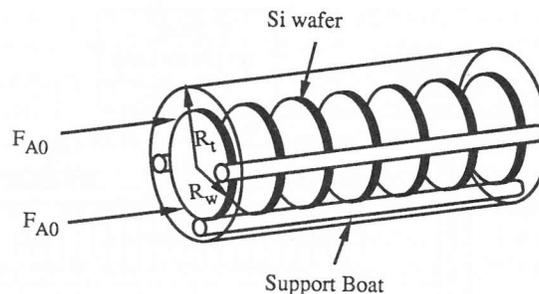
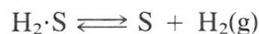
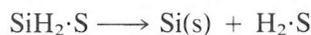


Figure 11-12 LPCVD boat reactor.

horizontal and vertical reactors. A description of these reactors and modeling equations are given by Jensen.<sup>6</sup>

One of the more common CVD reactors is the Horizontal Low Pressure CVD (LPCVD) reactor. This reactor operates at pressures of approximately 100 Pa. The main advantage of the LPCVD is its capability of processing a large number of wafers without detrimental effects to film uniformity. Owing to the large increases in the diffusion coefficient at low pressures (recall Table 10-2) surface reactions are more likely to be controlling than mass transfer. A schematic of a LPCVD reactor is shown in Figure 11-12.

To illustrate LPCVD modeling we shall use a specific but simplified example, the deposition of silicon from a gas stream of  $\text{SiH}_2$ . The reaction mechanism is



Here we have assumed that the equilibrium for the dissociation of  $\text{SiH}_4$  discussed in Problem 6-3 lies far to the right.

The corresponding rate law is

$$r''_{\text{Si}} = \frac{k_1 P_{\text{SiH}_2}}{1 + K_1 P_{\text{H}_2} + K_2 P_{\text{SiH}_2}} \quad (11-75)$$

Recalling that the adsorption constants  $K_1$  and  $K_2$  decrease with increasing temperatures, an excellent approximation at high temperature is

$$1 \gg (K_1 P_{\text{H}_2} + K_2 P_{\text{SiH}_2})$$

consequently, the deposition rate can be modeled as first-order in  $\text{SiH}_2$ , i.e.,

$$r''_{\text{Si}} \cong k_1 P_{\text{SiH}_2} \cong k C_{\text{SiH}_2} \cong k C_A \quad (11-76)$$

where  $A \equiv \text{SiH}_2$

<sup>6</sup> K. F. Jensen, *Chemical Engineering Science*, 42, 923 (1987).

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