Interconnect Capacitances, Crosstalk, and Signal Delay in Vertically Integrated Circuits

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Abstract

The impact of the three-dimensional circuit structure in Vertically Integrated Circuits (VICs) on interconnect capacitances, crosstalk and signal delay is investigated based on measurements and simulations. In comparison with planar IC technologies, increased substrate coupling and reduced coupling capacitances between adjacent interconnection lines considerably improve the noise immunity for VICs with chiplayers fabricated in silicon-bulk technology. For thin-film silicon-on-insulator chiplayers, noise immunity can be assured through the integration of conductive layers between active chips. The reduced interconnection lengths at system level lead to decreased interconnect delays despite higher total interconnect capacitances.

Introduction

Vertically Integrated Circuits (VIC) consist of independently processed chiplayers, which are stacked on top of each other with polyimide (ε_r=3.5) as interlayer-dielectric. The individual chips are thinned down to a few microns of remaining substrate thickness prior to assembly. Extremely high integration densities in the three-dimensional circuit structure allow the realization of complete multifunctional systems on a single stack of chips [1,2]. The possibility of fabricating a huge number of direct interconnects [3,4] between adjacent chiplayers provides an adequate vertical interconnection bandwidth. Fig. 1 shows a schematic cross-sectional view of a two-layer VIC which forms the basis of the study. Chiplayers fabricated in silicon-bulk and thin-film silicon-on-insulator (SOI)-technology are investigated.

Interconnect capacitances in VICs

The densely packed circuit structure in VICs has considerable impact on the characteristics of interconnection lines. Especially interconnect capacitances in the upper metallization layers of the bottom chiplayer are strongly affected by additional coupling to the upper chiplayer. Fig. 2 shows the increase in capacitance per unit length due to the additional coupling to the substrate of the upper chiplayer fabricated in silicon bulk technology. The impact of the thickness *h* of the interlayer dielectric on the capacitances of

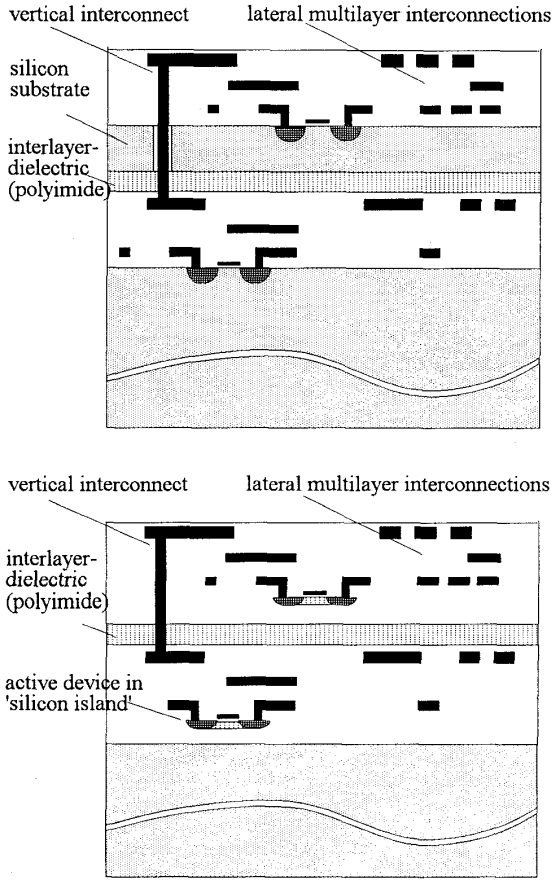

Fig. 1: Schematic cross-sectional view of two-layer Vertically Integrated Circuits (VICs) with chiplayers fabricated in silicon-bulk technology (top) and thin-film SOI-technology (bottom).

interconnection lines with different width is depicted. Measured data show good agreement with simulation results. While the substrate capacitance is considerably increased, coupling between interconnection lines in the same

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metallization layer decreases substantially. Fig. 3 shows the total and intralayer coupling capacitances per unit length as a function of line spacing in 3D-structures (VIC- bottom layer) compared to planar technology. Deviations of measured values from simulated results are mainly due to inhomogeneities in the interlayer dielectric.

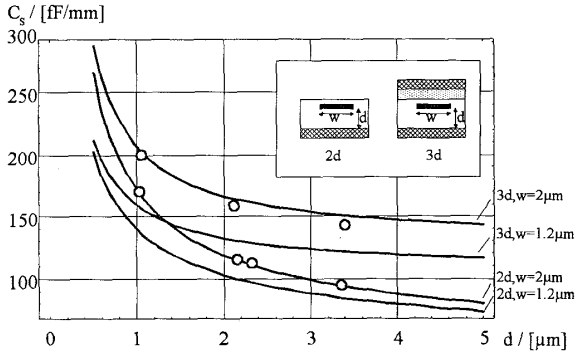

Fig. 2: Substrate capacitance C_s of interconnection lines in the bottom layer of a VIC (3d, with 1 µm polyimide, $\varepsilon_r = 3.5$ and 0.8 µm of passivation between the chiplayers) and in planar ICs (2d) as a function of the thickness d of the underlying dielectric (SiO_2). (o) indicates measured capacitance values for linewidth $w = 2$ µm and line thickness $t = 0.8$ µm.

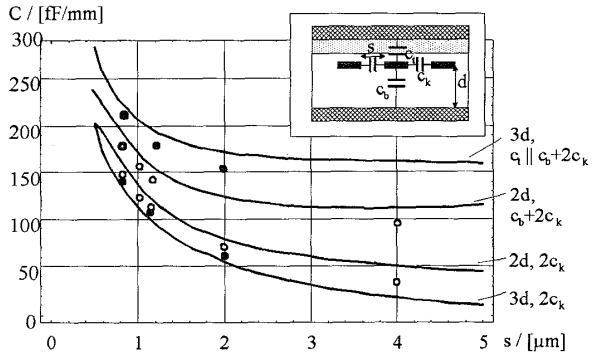

Fig. 3: Coupling capacitance and total capacitance per unit length as a function of the line spacing s. linewidth $w = 2$ µm, line thickness $t = 0.8$ µm, thickness d of underlying dielectric = 3 µm, 0.8 µm passivation and 1 µm of polyimide between the chiplayers. (•) indicate measured capacitances for the VIC-bottom layer, (o) indicate measured values for planar technology, respectively.

Signal crosstalk in 3D circuit structures

The worst case peak crosstalk amplitude V_{pct} at a quiescent signal line between two neighboring lines simultaneously switching at an amplitude of V_{in} can be expressed with the following equation:

$$V_{pct} = V_{in} \cdot \frac{2c_k \cdot l}{(c_t + c_b + 2c_k) \cdot l + C_L + C_{dr}} \qquad (1)$$

c_t, c_b and c_k are capacitances per unit length to top substrate, bottom substrate and neighboring line, respectively. l is the coupled line length, C_L the load capacitance of the line, and C_{dr} the driver output capacitance. Additional coupling to interconnects not directly adjacent is neglected for simplicity. Fig. 4 shows the ratio of the worst case peak crosstalk amplitude at an unloaded signal line (C_L , C_{dr}=0) to the input voltage of the two neighboring lines simultaneously switching as a function of the line spacing s. Compared to the planar case, in the 3D-IC the line spacing s can be chosen much smaller without reaching the logic threshold voltage of CMOS gates. Even with reduced absolute values of V_{pct} due to finite C_L and C_{dr}, noise immunity on VICs is considerably improved.

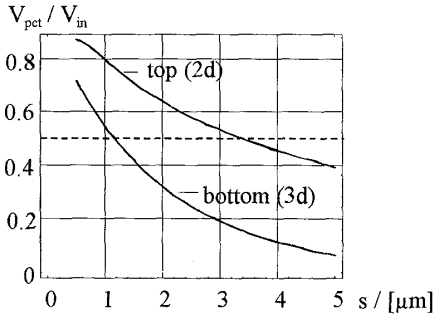

Fig. 4: Ratio of peak crosstalk amplitude to input voltage at a minimum sized unloaded line between two simultaneously switching interconnection lines as a function of the line spacing s (linewidth $w = 1.2$ µm, line thickness $t = 0.8$ µm, dielectric thickness $d = 3.0$ µm, polyimide thickness $h_{pi} = 1.0$ µm, $\varepsilon_r = 3.5$).

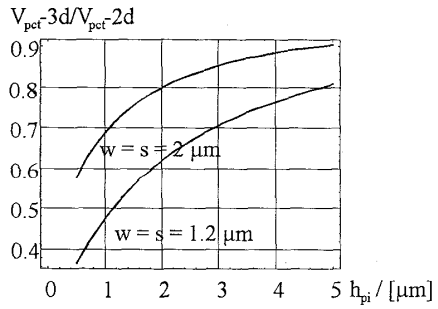

Fig.5: Ratio of peak crosstalk voltage of bottom layer line to top layer line or interconnect on planar IC as function of the thickness h_{pi} of the interlayer dielectric (polyimide, ε_r=3.5).

Fig. 5 shows the worst case crosstalk amplitude ratio on a signal line on the bottom chiplayer to the respective value for a line on the top layer or on a planar IC. The amplitude ratio is independent of line loading and is depicted as a function of the polyimide thickness between the chiplayers. The combination of additional substrate coupling and decreased coupling between adjacent lines (c. f. Figs. 2 and 3) considerably increases noise immunity in VICs and allows smaller spacings between adjacent signal lines. Fig. 6 shows measured crosstalk amplitudes on a 1 cm long interconnection line between two parallel lines simultaneously switching (w = s = 1.2 µm, Vin = 3.3 V) in the upper (top) and lower (bottom) VIC chiplayer. The reduced absolute values are due to impedance mismatch and load capacitances of the measurement setup, but the experiment reproduces the correct amplitude ratio.

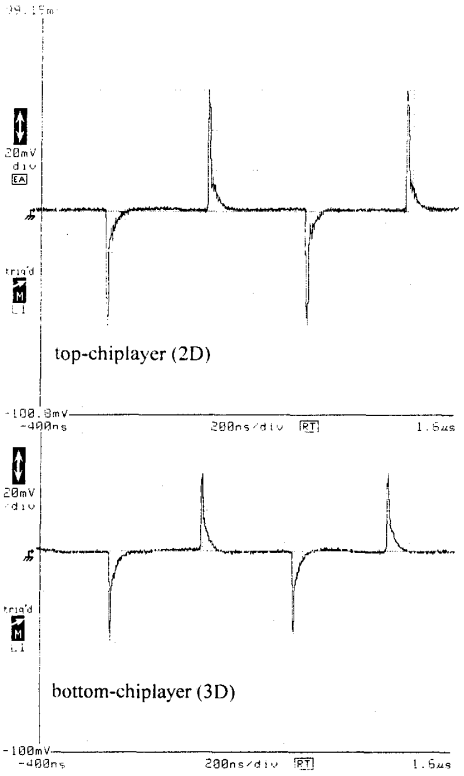

Fig. 6: Measured crosstalk on a 1 cm long interconnection line between two minimum spaced simultaneously switching lines on upper chiplayer (top) and lower chiplayer (bottom) ($w = s$ =1.2 µm, t = 0.8 µm, d = 3 µm, h_{pi} = 1 µm).

For silicon bulk technology, the substrate of the upper layer is capacitively decoupled from the underlying circuitry. Fig. 7 shows an SEM photomicrograph of a two layer VIC with 8.5 µm of substrate in the upper chiplayer and 1 µm of polyimide between the layers.

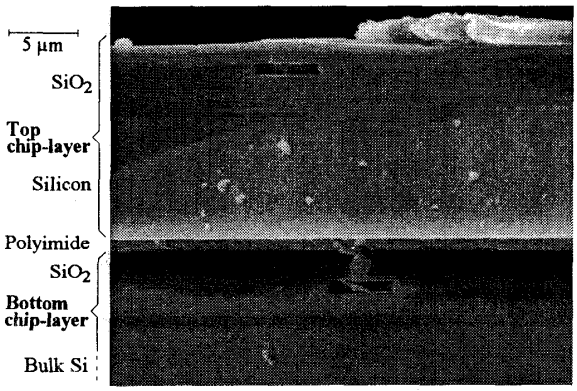

Fig. 7: SEM photomicrograph of a VIC with two chiplayers in silicon-bulk technology and 1 µm of polyimide between the layers.

With chiplayers fabricated in thin-film SOI-technology, capacitive shielding between the chiplayers is not assured by a silicon layer. Fig. 8 shows the coupling capacitance c_i between a signal line in the lowest metallization layer of the upper chip and a conductive plane in the topmost metallization layer of the bottom chip, and the intralayer coupling capacitance c_k as a function of the thickness of the interlayer dielectric h_{pi}. Measured data in Fig. 8 are obtained from a specimen simulating the dimensional properties of a stacked structure of thin-film SOI-chiplayers. For noise sensitive applications, interlayer coupling in thin-film SOI-structures can be prevented by the integration of conductive layers between the active chiplayers.

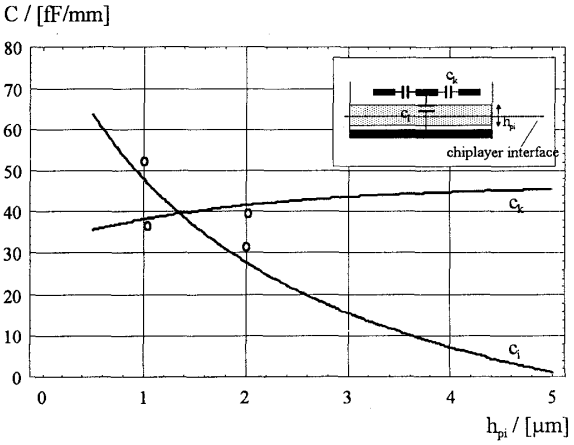

Fig. 8: Intra- and Interlayer coupling capacitances for a VIC with thin-film SOI-chiplayers, w = 2 µm, s = 2 µm, t = 0.8 µm, d = 0.9 µm (oxide under top-metallization).

Interconnect delay in VICs

The increased total capacitances of interconnects in the bottom layer (c. f. Fig. 2) affect the signal transmission considerably. For equal line lengths the additional coupling to the upper chiplayer leads to increased signal delays. Fig. 9 shows measured signal traces for a falling transition at the end of a 1 cm long interconnection line on bottom- and top chiplayer of a VIC.

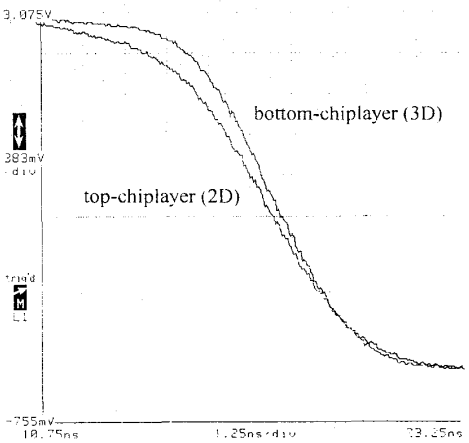

Fig. 9: Signal transition at the end of a 1 cm long interconnection line on bottom- and top-chiplayer, $w = 1.2$ µm, $t = 0.8$ µm, $d = 0.3$ µm, $h_{pi} = 1$ µm.

Based on the measured capacitance values, delay calculations for interconnection lines of different lengths were performed. The lines are loaded with a minimum size inverter and driven by a buffer of cascaded inverters optimized for minimum power-delay product [5]. The signal delay τ_d on an interconnection line of length l is given by the following equation:

$$\tau_d = \ln 2 \cdot (R_{dr} c_w l + R_{dr} C_L + 0.5 r_w c_w l^2 + r_w C_L l) + \tau_{dr} \qquad (2)$$

τ_{dr} and R_{dr} are intrinsic driver delay and output resistance, C_L is the load capacitance and r_w the line resistance per unit length. The wiring capacitance per unit length is given by:

$$c_w = c_t + c_b + 2c_k \quad \text{for 3D-IC (bottom layer), and}$$
$$c_w = c_b + 2c_k \quad \text{for planar IC.} \qquad (3)$$

c_t and c_b are the capacitances to top- and bottom-substrate. A single contribution of the coupling capacitances c_k to the interconnect delay corresponding to quiescent neighboring lines is assumed. Indicated in Fig. 10 is the signal delay on the top metallization layers of a planar IC or on the top chiplayer in a VIC (A) as a function of the interconnection length. A line of equal length in the bottom chiplayer (B) shows increased signal delay due to the higher capacitance per unit length. The integration of systems on VIC leads to shorter interconnection lengths. Traces (C) and (D) show reduced interconnect delays compared to (A) for two layer and four layer VICs with the same chip area as the planar system. The edge length of the chiplayers is taken as measure of the interconnection length.

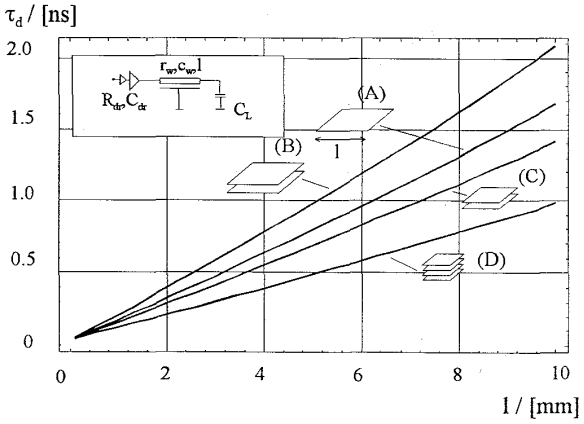

Fig. 10: Signal delay for global interconnection lines as a function of line length l in planar system (A), VIC-realization (bottom layer) using the same length (B), two-layer (C) and four layer structure (D) with equal area and reduced interconnection lengths.

Conclusion

With increasing system size, signal delays on interconnection lines and crosstalk requirements can influence the system performance considerably. Compared to planar realizations, VICs allow major reductions in both signal delay and crosstalk due to the reduced coupling capacitances, increased substrate coupling and reduced wire lengths. In conclusion, major constraints on interconnect system design can be alleviated using vertical integration technology.

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