3-D MULTICHIP PACKAGING FOR MEMORY MODULES

by

Robert T. Crowley and E. Jan Vardaman
TechSearch International, Inc.
9430 Research Blvd., Bldg. 4, Suite 400
Austin, Texas 78759 USA
Tel: (512) 343-4508 Fax: (512) 343-4509

Abstract

High density memory packaging is important for high performance computing systems and for small size memory systems. Smaller single chip packages as well as multichip packages have been developed for these applications. Three-dimensional (3-D) packaging is another technique that provides size and performance benefits. Memory chips are well suited to 3-D stacking techniques due to the relatively low number of I/O terminals, the ability to share many common signal lines, and low power dissipation. This paper presents an analysis of recent worldwide developments in 3-D multichip packaging for memory modules, including analyses of assembly processes and vertical interconnection.

Key Words: 3-D, Stacked, Memory, Vertical, Interconnection

Introduction

Performance and size are the driving factors for memory subsystems in many applications. Smaller single chip packages, such as the thin small outline package (TSOP) and the ball grid array (BGA) package, help to shrink the amount of board space required for memory chips. As these chips are mounted closer to the processor in computer applications, the signal propagation time decreases. Planar multichip module assembly has been used to further decrease the amount of area and the chip-to-chip spacing. Three-dimensional (3-D) packaging techniques have been developed to provide even greater packaging efficiencies for applications in space, defense, and computing. Our research has identified more than 30 companies that have developed 3-D packaging solutions, most aimed at memory packaging. These techniques include stacked packaged chips, laminated bare chips, stacked 2-D MCMs, stacked wafers, and folded flex circuits. In some cases, these 3-D modules incorporate multiple conventional 2-D modules. In other cases, multiple chips are assembled into a stack that can be mounted on a conventional MCM. In either case, memory stacking will be important to MCM assembly either as an end application for MCMs or as components for MCM assembly. This paper describes the key applications for memory stacking; compares the assembly processes, volumetric efficiency, and vertical interconnection techniques for 3-D multichip memory modules; and reviews the current status of the industry infrastructure.

Applications

Three-dimensional packaging techniques have been developed for many non-memory applications including focal plane array detectors that contain as many as 64 signal processor chips in one stack, and parallel processor computer architectures based on stacked MCM technology. Space and military applications have been instrumental to the development of 3-D technology, often under ARPA funding. However, computer applications

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will drive the technology into commercial production. The major applications for 3-D memory are all related to memory stacking: secondary cache memory, SIMM replacements for DRAM storage, solid state disk drives, and high density PCMCIA memory cards.

Solid State Data Recorders

Observation satellites generate a large amount of data that must be stored and then transmitted back to earth. Electromechanical recorders are being replaced by solid state data recorders for several reasons including: less vibration, smaller size, less mass, and greater data storage and retrieval flexibility. To image a 60 km x 60 km area with 1.8 meter resolution, 10 Gbits of data storage are required with a 100 Mbit/sec data rate. Matra Marconi Space France plans to assemble 10 Gbit recorders in 1994 and 1Tbit recorders by 2002 for this application [1]. Several other companies have developed solid state data recorder technology based on 3-D memory stacking technology including Texas Instruments, General Electric, and Harris. Each of these companies has chosen a unique stacking approach including stacked bare die, stacked MCMs, and stacked packages. Today's technology requires more than one thousand 1Mbit chips to make a 1Gbit recorder, while future systems may use sixteen thousand 64Mbit chips for a 1Tbit recorder. Hermetic enclosures are required for space operation. This can be implemented at the single chip level, complete recorder level, or an intermediate level.

Processor Memory Stacks

Computer processor chips and digital signal processing (DSP) chips require high-speed memory located near the processor. High performance workstation applications can benefit from the reduced cache memory access times made possible by memory stacking. Sun Microsystems recently incorporated cache memory stacks on a server's processor board. Smart weapons benefit from memory chip stacking size reductions in addition to performance improvements. Texas Instruments uses memory stacks on Aladdin processor MCMs and dual C30 DSP modules [2]. Irvine Sensors, in cooperation with nCUBE and NASA's Jet Propulsion Lab, developed a memory stack that is integrated into a compact node for a massively parallel processor computer [3].

Most applications use stacks with four to nine memory chips. Both bare chip stacks (e.g. Irvine Sensors, Texas Instruments, and Thomson-CSF) or packaged chip stacks (e.g. Dense-Pac Microsystems, Fujitsu, Mitsubishi, RTB Technology, and Staktek) can be used. However, the major barrier is cost. If 3-D technology does not become cost competitive with single chip packages and SIMMs, it will not be adopted.

Memory Cards

PCMCIA cards have tight restrictions on thickness and size. Bare die stacking can quadruple the memory storage density. Matsushita has developed a process using stacked TAB technology to build memory cards [4]. IBM has licensed Irvine Sensors technology and could incorporate this into future memory cards.

Solid State Disk Drives

Memory stacking can be used for solid state disk drives that offer higher speed than rotating storage devices. At least three companies are investigating stacked wafer technologies in an effort to make this product a reality.

3-D Techniques

Three fundamental packaging techniques have been developed for 3-D assemblies: packaged chips, bare chips, and multichip modules. Other techniques that have not been commercialized yet include stacked wafers and folded flex circuitry. TechSearch International

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has identified 27 companies that have investigated 3-D packaging techniques with eleven companies in production; most are still in the R&D phase [5].

Stacked Packages

Packaged chip assembly techniques include standard packages and custom packages. Thomson-CSF and Mitsubishi have developed stacking techniques using standard TSOPs to provide low cost memory stacks. Thomson-CSF mounts TSOPs to copper lead frames, stacks the packages, and then molds the stack in plastic [6]. The stack is sawed into a cube, and the edges of the stack are interconnected by laser patterning a metal layer deposited on the surface of the cube. Mitsubishi stacks TSOP packages and solders the leads to a pair of printed circuit boards on each side of the stack [7]. For hermetic applications, ceramic leadless chip carrier (LCC) packages can be stacked as done by Dense-Pac Microsystems. Harris has developed a low temperature cofired ceramic (LTCC) tub that can hold two memory chips. The tubs are stacked in such a way as to hermetically seal each layer [8].

To increase density even further, several custom packages have been developed for stacking memory chips. Dense-Pac Microsystems has developed a non-hermetic stackable package that uses a 2-layer LTCC substrate. The IC is glued to the ceramic and interconnected with wire bonding [9]. This process is limited to low I/O ICs such as memory chips. RTB Technology and Staktek Corporation have developed similar plastic packages for stacking memory chips. Hitachi has developed a unique stackable chip carrier for high density memory stacking. Individual TCPs are bonded to printed circuit board (PCB) frames [10]. Each frame is slightly larger than the chip and has a window punched out of the middle such that the top surface of the chip is flush with the top of the PCB. This minimizes the stack height.

Stacked Bare Die

Even greater density can be obtained by stacking bare die. Several techniques have been developed by Irvine Sensors, Texas Instruments, Thomson-CSF, Matsushita Electric Industrial, and Fujitsu. Irvine Sensors laminates several thin chips into a cube and then uses a thin film deposition and patterning process to interconnect the chips along one or more faces of the cube [11]. The key to this technology is Irvine's "T-connect" between the thin film metal on the surface of the chip and the thin film metal on the face of the cube. Texas Instruments also routes the signals to one edge of the IC, but uses TAB leads to create metal studs that extend beyond the edge of the chip. These studs are soldered to a silicon substrate for interconnection. Thomson-CSF uses a sacrificial TAB tape frame as a lead frame. The IC is wire bonded to the tape, and then processed similar to the stacked TSOP discussed above. Matsushita and Fujitsu have developed stacked TCP techniques. Matsushita bonds the TCP stack to a PCB while Fujitsu bonds the TCPs to a copper lead frame.

Stacked MCMs

Bare die can be mounted on multichip modules which are then stacked vertically to create high density general purpose electronics systems and mass memory systems. AT&T, E-Systems, General Electric, Hughes, Matra Marconi Space France, Matsushita Electronic Components, and Motorola have all developed stacking technologies for multichip modules.

GE extended its chips-first HDI process into the third dimension by stacking MCMs and applying thin film interconnection layers along one or more edges of the stack [12]. GE built a 40 Mbyte memory stack prototype containing twenty 16Mbit DRAMs using three 2-D HDI substrates.

Matra Marconi Space France developed a hybrid bare die/MCM approach for solid state

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recorders. Two chips are wire bonded to an MCM substrate, and then two more chips are laid on top but rotated 90 degrees.

Matsushita has developed a stacked MCM technology suitable for memory systems [13]. A 16Mbyte DRAM module was constructed using 32 4Mbit DRAMs. Eight glass substrate MCM layers were stacked to create a module measuring 26mm x 26mm x 19mm. Each layer contains 4 DRAMs and 4 chip capacitors. The MCMs are vertically interconnected by soldering the C-shaped QFP lead frames to each other.

Stacked Wafers

Wafer stacking is being investigated by at least three U.S. companies. Undiced wafers can be stacked without dicing the wafers into chips. Several technical issues need to be addressed with this technology including electrical wafer feedthroughs, reliable wafer-to-wafer interconnection, and fault tolerancy for defective ICs.

Flex Circuit Structures

Another novel technique involves flex circuitry. Multiple ICs can be bonded to one piece of flex circuit and then folded or stacked to create a compact 3-D memory structure. At least three companies are investigating this today, including Harris, MCC, and MMS. Harris has developed a folded flex circuit technique suitable for memory stacking. Memory chips are bonded to the flex circuit which is then folded to create a compact structure. The flex circuit provides the first-level connection to the chip, the chip-to-chip vertical interconnection, and the flex connector for the entire stack.

Volumetric Efficiency

All of the bare chip and packaged chip stacking technologies have been used for memory chip stacking, while only three of the MCM stacking techniques have been used for memories.

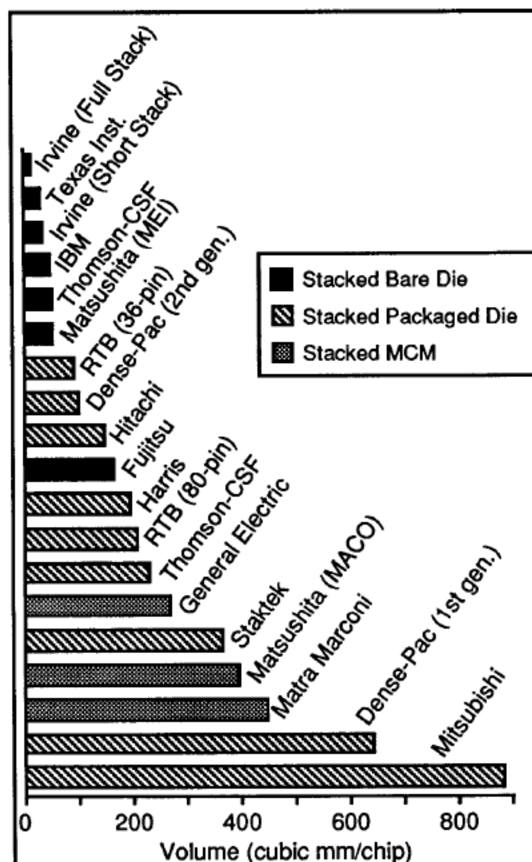

Figure 1. Bare chip stacks are most dense, followed by custom packages, multichip modules, and standard chip packages.

Volumetric efficiency is easier to compare for memory circuits than for image processor or microprocessor circuitry. The relative volume of memory stacks are compared in figure 1. This chart was generated by dividing the volume of a stack by the number of chips in the stack. Most modules used 1Mbit SRAMs or 4Mbit DRAMs,

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although there are a few exceptions. The minimum volume of a technology depends on the size and thickness of the chip, and each company used different chips. Therefore, it is difficult to make direct comparisons between two companies. However, the figure does highlight the relative density of the different 3-D techniques. Stacked bare die is most dense, but requires the most complicated manufacturing process. Custom packages, designed for stacking, simplify the manufacturing process (test, burn-in, and handling) and can provide comparable density to bare chip stacks. Stacked MCMs require more volume per chip than custom packages. Standard packages (LCCs and TSOPs) produce the largest modules.

Vertical Interconnection

Vertical interconnection is a critical design issue for 3-D packaging. Various techniques have been developed including thin film metal deposition and patterning, solder dipped connections, laser-machined conductors, Z-axis conductive polymers, printed circuit boards, metal pins, solder balls, TAB tape, and fuzz buttons.

Vertical interconnection techniques can be classified as peripheral connections or array connections. Peripheral connections require that all signals be routed to the edge of the stack and then routed from layer to layer. Many peripheral techniques are limited even further because each vertical path must be shared between all the layers. This is acceptable for stacked memory applications but not mixed circuitry applications. Array connection techniques allow for more vertical channels than peripheral connections. Furthermore, many array techniques allow custom placement of the vertical connections for each layer for maximum flexibility.

Soldered Connections

Soldered connections are the most common approach for stack interconnection. However, many different techniques have been developed. Dense-Pac Microsystems uses a solder dipping process to interconnect the castellated edges of the stack. Matsushita and Fujitsu use a hot bar soldering process to interconnect two to four layers of TAB-mounted memory chips. Hitachi joins PWB frames together with solder-filled through-holes. Matsushita solders the formed lead frames for stacked MCMs. Motorola has developed a process for stacking BGA modules using solder balls on both sides of the substrate. Staktek and RTB Technology use pins inserted and soldered through the leads on each package in the stack. Texas Instruments and Mitsubishi use 2-D interconnecting substrates (silicon MCM and PWB respectively) that are soldered to the leads from each chip or package.

Thin Film Connections

Thin film metallization on one or more faces of the memory stack provides greater wiring density and wiring flexibility than most soldered connections. Irvine Sensors, General Electric, and Thomson-CSF all use forms of thin film interconnection.

Infrastructure

The 3-D memory module industry is still in the infancy stage. Many companies have developed technologies and are building patent portfolios for future protection. A few companies offer commercial memory modules or assembly services, but only in limited volume today. Many companies are offering their technology for license to other companies. While it is possible to buy memory modules, obtain contract assembly, and license technology, no applications are using memory stacks in high volume.

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