November 14-15, 1990 Makuhari, Chiba, Japan pp. 267-272

EVALUATION OF CUBIC (CUMULATIVELY BONDED IC) DEVICES

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ABSTRACT

Thin film device layer bonding technology, referred as to Cumulatively bonded IC (CUBIC) technology, has been developed for 3D-IC fabrication. Advantages of the CUBIC technology are its ability to make device layers independently on the Si-substrates using a conventional IC fabrication process, the lack of heat damage during the device bonding process, and its short process turn around time. In this paper, concept of CUBIC technology and key process technologies involved are described in detail, and its application to future electron device fabrications will be discussed.

1. INTRODUCTION

In the field of system which consists of a large amount of electronic functional blocks, the packaging density has been the major impetus to the system performance improvement. A lot of technical approaches to attaining high packaging density have been proposed[1-2]. Among them is three dimensional IC fabrication, where several device layers are stacked in the vertical direction.

Three dimensional ICs are made by repeated SOI (Silicon-On-Insulator) formation and device fabrication on the SOI film. To obtain the SOI film, a polysilicon film on silicon dioxide is melted and recrystallized by scanned laser beam or electron beam. However, serious problems in the 3D-IC fabrication process, hereafter called as "beam recrystallization method", are pointed out[3,4]. First, with increasing the number of stacking layers, quality control of the SOI film becomes difficult. Second, underlying device layers suffer from heat-damage during upper layer device fabrication. Furthermore, a long process turn around time (TAT) and low productivity also restrict mass production of 3D-ICs since the number of process steps extremely increases with the device layer.

In this paper, a new 3D-IC fabrication technology, referred to as CUBIC (CUmulatively Bonded IC) technology is proposed, and its future applications are described.

2. Concept of CUBIC technology

Figure 1 illustrates the concept of CUBIC technology[5]. The CUBIC technology involves the device thinning process and the device bonding process. First, the 1st, 2nd and 3rd device layers are made independently on bulk Si substrates using a conventional IC fabrication process. Next, the silicon crystals underlying the 2nd and 3rd device layers are eliminated to obtain thin film devices. Then, vertical wirings are made for signal and power transmission from the front surface to the back surface of the thin film devices. Finally, the thin film devices are bonded mechanically and electrically.

The CUBIC technology has a lot of advantages superior to the ordinary 3D-IC fabrication technology using a beam recrystallization method. One of the most attractive advantages of the CUBIC technology is its ability to make the device layers independently on bulk Si-substrates, thus shortening the process TAT of 3D-IC fabrication. The other advantage of the CUBIC technology is the lack of heat damage because of a low device bonding temperature. Thus, the CUBIC technology is expected to be applicable to the 3D-IC fabrication having a large number of stacking device layers.

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3. Key technologies

In order to realize the CUBIC technology, the key issues are how to obtain thin film devices, make electrical path from the front surface to the back surface of the thin film devices, and make device-to-device electrical interconnections in the bonded structure. In this section, the technologies which were developed to solve these issues are described.

3-1. Device thinning

Thin film devices were obtained using preferential polishing technique[6,7] as shown in Figure 2. First, a backing substrate is adhered to the device surface of the silicon wafer. Then, most of silicon underlying the device layer is eliminated by grinding, and the residual part (50-100um) is removed by preferential polishing. The preferential polishing proceeds with the following two steps: (1) silicon reacts with the polishing liquid such as organic amine solution, producing silicon hydrate, and (2) the silicon hydrate is removed mechanically by a polishing pad. Since no reaction occurs between SiO_2 and the polishing liquid, the polishing stops automatically at the LOCOS back surface(SiO_2) to give a thin film device. Figure 3 shows photographs of a NMOSFET formed on silicon substrate and the back-surface view of the thin film NMOSFET obtained. The thin film device layer, with the thickness of 2um, was mechanically stable because of the backing substrate support.

3-2. Back surface wiring

The electrical paths from the front surface to the back surface of the thin film device were made using the back surface wiring technology. After the preferential polishing (see Figure 3), the poly-Si and $MoSi_2$/Al patterns on the LOCOS front surface become visible from the LOCOS back surface, thus enabling us to make the back surface patterns which are aligned with the front surface patterns. Namely, through-hole patterns and back surface W/Al wiring patterns are made on the LOCOS back surface.

Figure 4 shows the patterns used for confirmation of electrical interconnection between the poly-Si wirings and the back surface W/Al wirings. The through-hole size was 2umx2um. The contact array obtained revealed an ohmic-contact property, and the contact resistance between the poly-Si and the W/Al wirings was $3x10^{-8}$[$ohm \cdot cm^2$].

3-3. Bump/pool Contact

Device-to-device electrical interconnections were made using the "bump/pool contact" technology[8] as shown in Figure 5. The bonding mechanism is as the follows. At first, tungsten bumps, which are a high melting point conductive material, are formed on the polyimide-coated device layer. Au/In pools, where the alloy with low melting point is partially plugged in the polyimide film, are formed on the other device layer. These two layers are aligned by infrared microscopy with the W bumps just over the Au/In pools, then heated above melting temperature of the Au/In alloy and put together. The device layers bond to each other due to the solid phase fixing force between the bumps and the pools, giving the device-to-device electrical interconnections. In addition, the polyimide to polyimide adhesion force helps the mechanical bonding between the device layers.

The bump/pool contact is advantageous for making fine-pitch interconnection because the molten Au/In alloy doesn't overflow during the bonding. The low bonding temperature below 400°C prevents the device layers from heat-damage. The third advantage is that the bump/pool contact has a stable bonding structure with not only horizontal but also vertical bonding tolerances. The horizontal and vertical tolerances are determined essentially by the resolving power of infrared microscopy and by the bump height. At the present time, the horizontal and vertical tolerances are of ±3um and ±1.5um, respectively.

Figure 6 shows the patterns used for confirming electrical interconnection between the $MoSi_2$/Al wiring and the W/Al wiring by the

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bump/pool contact technology. Here, the $MoSi_2$/Al patterns on the one Si-substrate (Fig. 6(a)) were aligned with the W/Al patterns on the other Si-substrate (Fig. 6(b)). As shown in Figure 6(c), 1,600 links were electrically connected in the contact array with the bumps and the pools. The bump/pool contact revealed an ohmic contact property, and the contact resistance between the bump and the pool was 5×10^{-6} [$ohm \cdot cm^2$].

4. Evaluation and application

In order to evaluate the CUBIC technology, a dual active layered device was fabricated. Figure 7 shows the steps for a dual active layered device fabrication using CUBIC technology, which consists of the preferential polishing, the back surface wiring, and the bump/pool contact technologies. First, NMOSFETs for the 1st (lower) and the 2nd (upper) layers are fabricated independently on silicon substrates, and then W bumps, the size of 2umx2um and the height of 2.0um, are fabricated on the $MoSi_2$/Al wirings. After the backing substrate adhesion on the 2nd device layer (Fig. 7(a)), the silicon underlying the 2nd device layer is removed by grinding and preferential polishing (Fig. 7(b)). Then, through-holes, the size of 3umx3um, back surface W/Al wirings and Au/In pools, the size of 8umx8um and the depth of 2.5um , are formed on the back surface (Fig. 7(c)). The thin film device obtained is used as a building block. Note that the pools on the back surface are electrically connected to the bumps. Next, the thin film NMOSFET for the 2nd layer is aligned over the bulk NMOSFET for the 1st layer using infrared microscopy, and then pressed together (Fig. 7(d)). The thin film NMOSFET is electrically interconnected to the bulk NMOSFET by the bump/pool contacts. Finally, the backing substrate and the adhesive on the 2nd NMOSFET are removed by etching (Fig. 7(e)).

Figure 8 shows photograph and schematic view of the dual active layered device obtained. The source and gate of the thin film NMOSFET (the 2nd layer) were electrically interconnected to those of the bulk NMOSFET (the 1st layer) through the bump/pool contacts. The drains, on the other hand, were not connected each other. The drain currents of the thin film NMOSFET were lower than those of the bulk NMOSFET[9] as shown in Figure 9. Optimization of the preferential polishing will improve the thin film NMOSFET performance by reducing stress and/or crystal defects in the active silicon device area. Consequently, it is proved that the CUBIC technology is really applicable for making 3D-IC fabrication even though minor process refining is still needed.

Figure 10 illustrates application examples of the CUBIC technology to future electron device fabrications. Multi-functional 3D-IC such as vertical stacking of memory and processor blocks will be realized with high production yield by using CUBIC technology (Fig. 10(a)). High performance multi layered IC will be fabricated by stacking thin film inter-CMOS devices as building blocks (Figure 10(b)), since the inter-CMOS devices, in which PMOSFET is located above NMOSFET, have many advantages of latch-up-free structure and less photomasks required for ion implantation process steps[10].

5. Summary

CUBIC technology, which is a thin film device bonding technology, has been developed. The thin film devices are made using preferential polishing technology, the vertical interconnections from the front surface of the thin film device to the back surface are made using back surface wiring technology, and the device-to-device interconnections in the bonding structure are made by bump/pool contacts.

The advantages of CUBIC technology are its ability to make device layers independently on bulk Si substrates using a conventional IC fabrication process, the lack of heat damage, and its short process TAT. Thus, CUBIC technology will be applicable to mass production of many kinds of 3D-IC possible.

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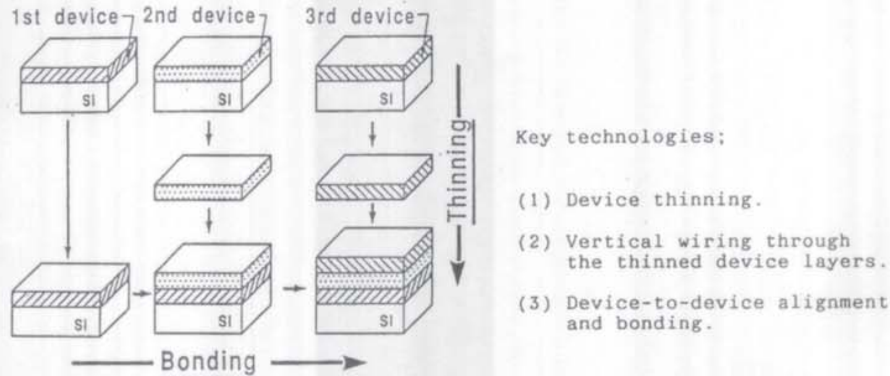

Figure 1 Concept of the CUBIC technology and the key technologies involved.

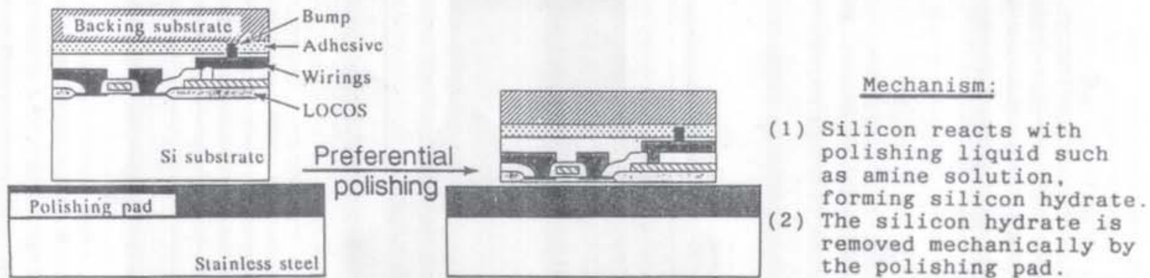

Figure 2 Device thinning process using "preferential polishing".

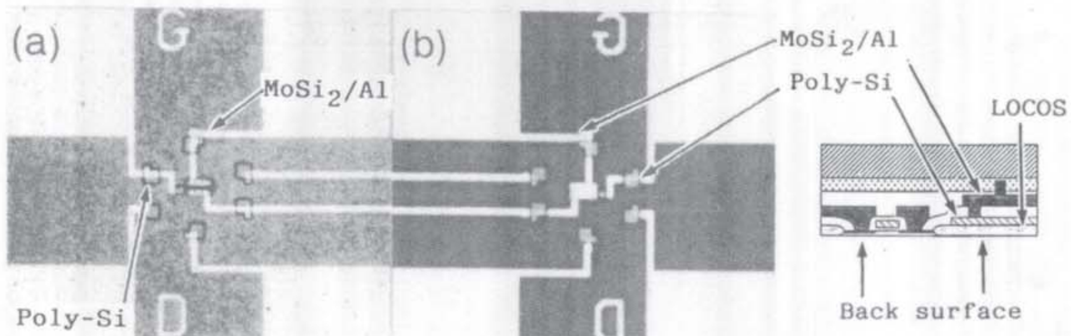

Figure 3 Photographs of (a) NMOSFET formed on a bulk Si-substrate and (b) the back surface view of the thin film NMOSFET obtained by "preferential polishing".

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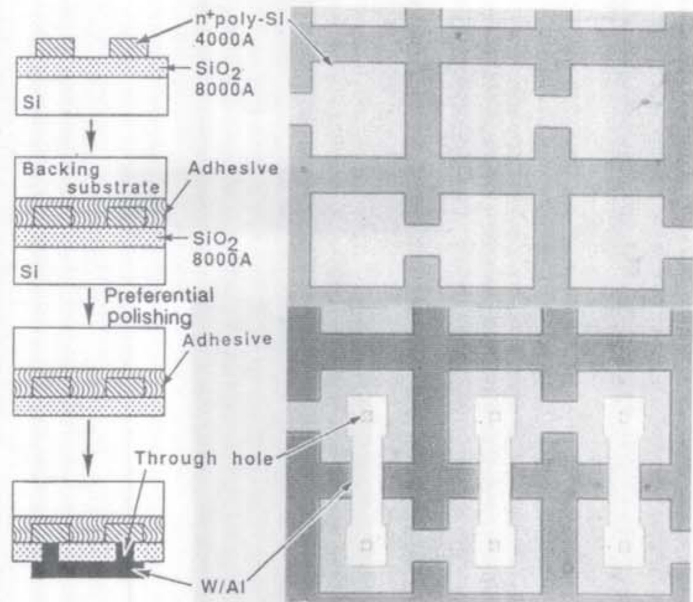

Figure 4 Sequence of back-surface wiring process steps.

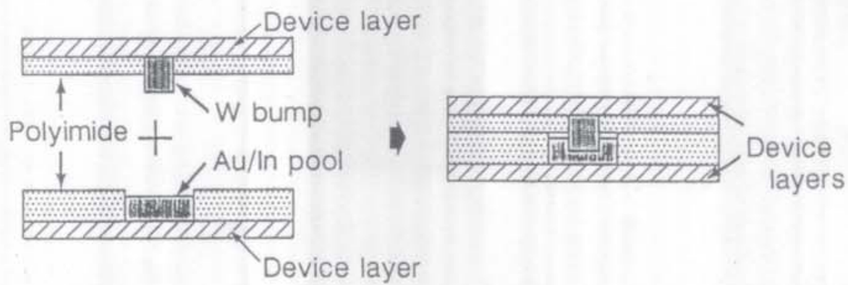

Figure 5 Schematic cross sectional views of device-to-device interconnection using a bump/pool contact.

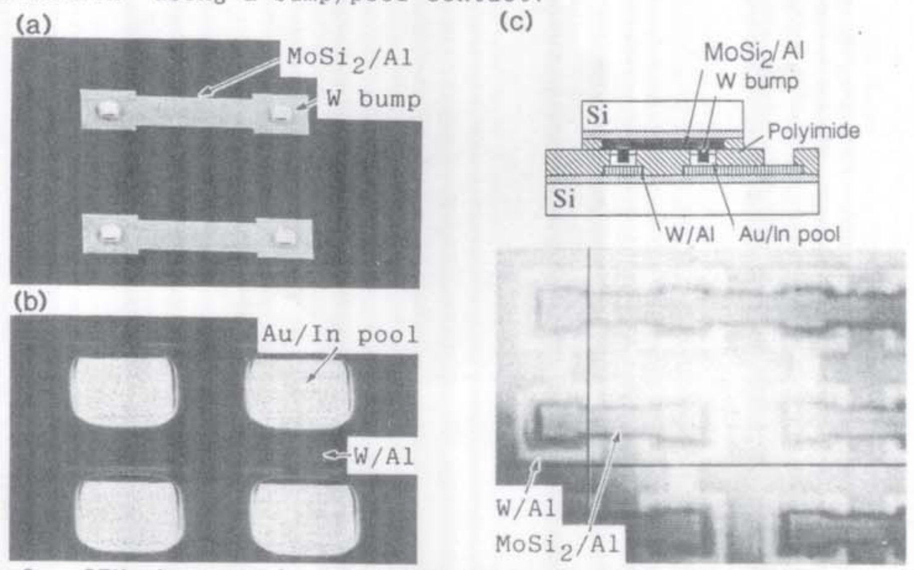

Figure 6 SEM photographs of (a) W bumps on $MoSi_2/Al$ wirings, (b) Au/In pools on W/Al wirings, and (c) schematic cross sectional view and infrared-photograph of the device-to-device interconnections using bump/pool contacts.

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