Three-Dimensional IC Trends

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Invited Paper

VLSI will be reaching to the limit of minimization in the 1990s, and after that, further increase of packing density or functions might depend on the vertical integration technology.

Three-dimensional (3-D) integration is expected to provide several advantages, such as 1) parallel processing, 2) high-speed operation, 3) high packing density, and 4) multifunctional operation.

Basic technologies of 3-D IC are to fabricate SOI layers and to stack them monolithically. Crystallinity of the recrystallized layer in SOI has increasingly become better, and very recently crystal-axis controlled, defect-free single-crystal area has been obtained in chip size level by laser recystallization technology.

Some basic functional medels showing the concept or image of a future 3-D IC were fabricated in two or three stacked active layers.

Some other proposals of subsystems in the application of 3-D structure, and the technical issues for realizing practical 3-D IC, i.e., the technology for fabricating high-quality SOI crystal on complicated surface topology, crosstalk of the signals between the stacked layers, total power consumption and cooling of the chip, will also be discussed in this paper.

Introduction

The ultimate IC structure of the future is thought to consist of stacked active IC layers sandwiched by insulating materials.

Various devices or circuit functions, such as photosensors, logic circuits, memories, and CPUs, will be arranged in each active layer and, as a result, a remarkable improvement in packing density and functional performance will be realized.

In 1979, it was reported that polysilicon deposited on insulator can be melted and recrystallized by laser irradiation [1] and that the crystal perfection of the layer can be adequate to allow the fabrication of devices.

The quality of the recrystallized layer can be characterized by carrier mobility. As shown in Fig. 1, the electron mobility reported so far has increased year by year and has attained a value comparable to bulk crystals. This improvement was a trigger for starting research and development of 3-D ICs.

A partial 3-D structure has already been tried for a dynamic memory (DRAM) cell [2], [3]. For high-density RAMs, such as the 4-Mbit DRAM, the area of the memory cell capacitor is limited, so in order to increase the cell capacitance, a 3-D structure, i.e., a trench cell or a stacked capacitor cell, has been tried. This partial 3-D structure will be used in 2-D VLSIs within a few years.

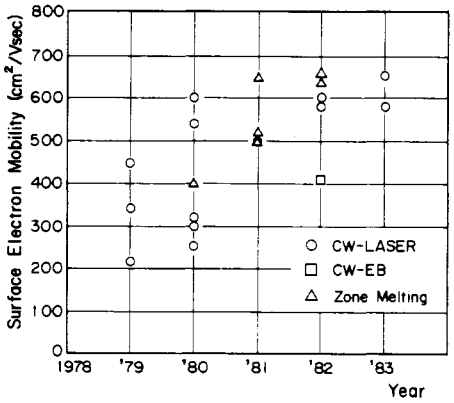

Fig. 1. Progress of surface carrier mobility of MOSFET fabricated on SOI layer. ○—CW laser; □—electron beam; △—carbon strip heater.

To achieve a breakthrough in the packing density of advanced VLSIs, it is reasonable to consider a 3-D structure, containing either partially or completely stacked active layers. Fig. 2 shows a forecast of the development of 3-D ICs schematically, as 3-D technology progresses. This figure was obtained from the 3-D IC Research Committee of the 3-D

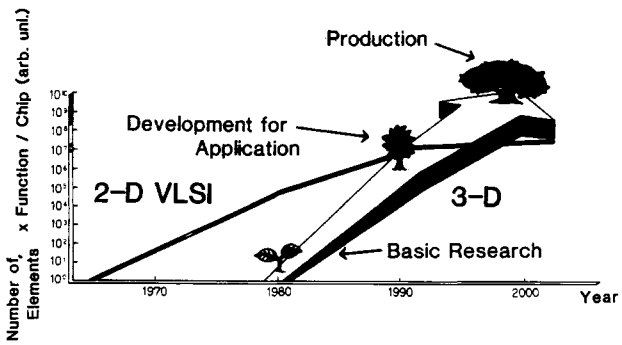

Fig. 2. Forecast of progress of 3-D technology.

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project directed by the MITI of Japan. According to discussion in the Committee, the basic technology for stacking active layers will be developed before 1990. With this technology, various kinds of circuits, such as high-packing-density memory, high-speed logic or image processors are expected to be designed and realized in a single chip between 1990 and 2000.

A 3-D IC for practical use is not available now, but functional models have been fabricated in stacked double or triple active layers demonstrating the concept of a future 3-D IC.

This paper describes SOI process technology, which is the basic technology for fabricating 3-D structures, and the 3-D devices which have already been fabricated in the laboratory. Features, problems, and trends in fabrication technology as well as the design and architecture of 3-D devices will be discussed.

3-D IC Structure

Fig. 3 shows a typical basic structure of 3-D devices proposed by several researchers. Fig. 3(a) is a flip-chip, which is an attempt to realize the stacked 3-D form by chip assembly technology. This technology has already been used in computers as a connection between a group of single chips and a printed circuit board. In this technology, the number of connections are restricted by reliability and bump size constraints. Fig. 3(b) shows a new approach based on wafer process technology. The chips are attached face-to-face by pressure [4]. The minimum connection area is 10 μm^2, which is large compared with the device feature size (1–2 μm), but the number of connections will be greatly increased by this technology. Fig. 3(c) and (d) shows a monolithic 3-D structure. At first, the passive elements, such as the DRAM-cell capacitor or the load resistor of a SRAM, will be stacked three-dimensionally similarly to the multilevel interconnections of today's LSIs. Fig. 3(c) shows 3-D integration performed at the transistor level [5]. Load transistors of a CMOS inverter of a CMOS static RAM cell are fabricated in the upper layer to form a partial 3-D structure. The first 3-D IC which has active elements or uses single-crystal material in the stacked layer may have the configuration shown in Fig. 3(c). Fig. 3(d) shows the stacked form of LSI layers in a complete 3-D structure, which is the final goal of the 3-D Project in Japan. In this structure, the degree of freedom in circuit or system design circuit layout, and the reliability of the interconnections are expected to be very high. This structure is one of the promising VLSI candidates of the future, and may represent a final configuration of VLSI.

This paper will discuss mainly the trends in the kind of 3-D structure shown in Fig. 3(d).

Features of 3-D IC

Although it is not well known what kinds of systems can best be realized in 3-D ICs as opposed to 2-D ICs, the advantages expected for 3-D ICs are as follows:

1) high packing density, or super large integration
2) high speed
3) parallel signal processing
4) integration of many functions on a single chip.

High-Packing Density

The fundamental advantage of 3-D integration, compared to 2-D integration, is in packing density. As the number of integrated active layers increases, larger integration

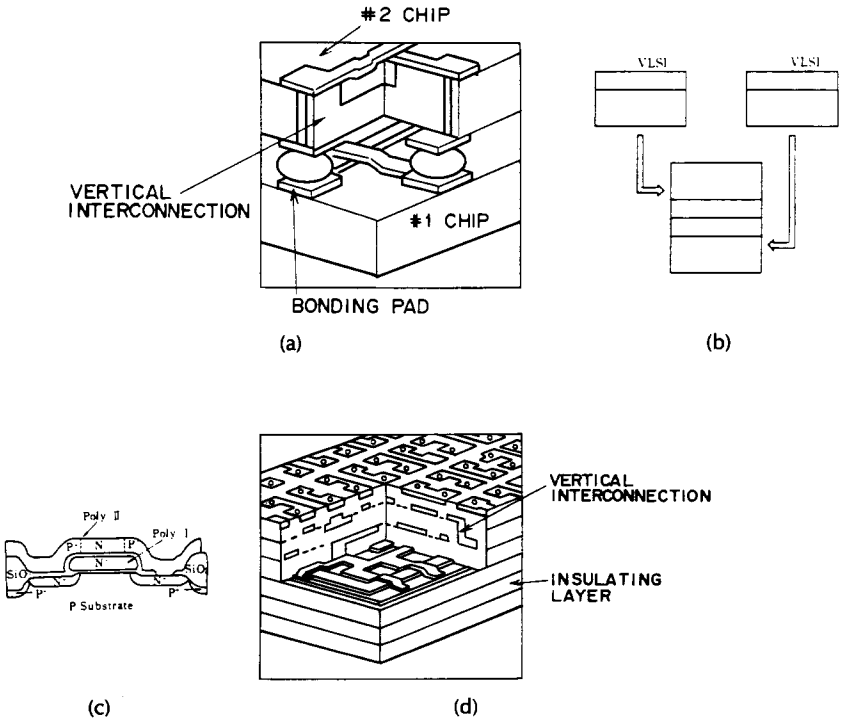


Fig. 3. Basic concepts of 3-D device structure. (a) Two 2-D LSI connected by flip-chip bonding. (b) Chip attachment by press. (c) Partially stacked structure in transistor level

becomes possible. Input and output circuits which consume high electrical power are not required for every active layer. For instance, a 10-layer 3-D IC needs only one set of I/O circuits. Accordingly, power dissipation per circuit function is extremely small in 3-D ICs compared to 2-D ICs. The original advantages of integrated circuits, such as small size, light weight, and high reliability, are preserved even in 3-D IC structures.

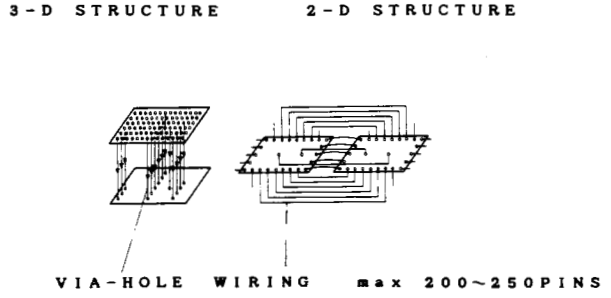
High-Speed Performance

High-speed performance is associated with shorter interconnection delay time and parallel processing. The increase of propagation delay due to a long interconnection line (higher resistivity, larger capacitance) is especially serious in the latest 2-D VLSI circuits. It is possible to exchange signals between upper and lower active circuit layers through via holes in 3-D ICs. In 2-D ICs, the longest signal interconnection length becomes several to ten millimeters, but in 3-D ICs the length between upper and lower layers is on the order of 1–2 μm. In addition, parasitic capacitance is considerably smaller in 3-D ICs, since the active elements are fabricated on the insulator. The transistor itself consequently exhibits excellent high-speed performance. For these reasons, twice the operating speed is possible in the best case of 3-D ICs. High-speed operation of SOI devices has been already verified by several pioneering researchers [6].

Shortening of interconnections and signal transfer through vertical via holes in the 3-D configuration provides advantages for the design of large-scale systems. One of the restrictions on system design, that subsystems must be connected with the minimum number of connections possible, may be mitigated. High-impedance drive will become possible, and the number of I/O buffers will be considerably decreased in a total system. The advantages will cause a major change in chip design and layout design.

Parallel Processing

Parallel processing is expected to be realized more easily in 3-D structures. Several thousands or several tens of thousands of via holes are present in these devices, and many information signals can be transferred from higher to lower layers (or *vice versa*) through them. The size of a via hole is 1–2 μm with present process technology. In 2-D LSIs, the number of bonding pads which can be prepared on a chip limits the number of signals to be taken out. The maximum number of pads is now 200–250 (Fig. 4). As a result of parallel processing, the signal processing speed of the system will be greatly improved.



Integration of Functions

Integration of many functions is one of the special features of 3-D ICs. Each layer or set of several active layers can have its own function. At the device level, different types of devices, such as MOS and bipolar, and different characteristics provided by different process technologies, can be assigned to each active layer. It is possible to make use of these advantages for system design. Circuit selection (analog and digital) and the use of photosensors, light-emitting elements, and SAW devices can be implemented in a 3-D chip. For example, it is possible to prepare a video sensor on the top layer, then an A/D converter, ALU, memory, and CPU in the lower layers to realize an intelligent image processor in a multilayered 3-D structure.

Optimization of system design becomes easy by the proper choice of the most suitable process and circuits for the corresponding active layer.

SOI Technology (Recrystallization of Si)

There are three primary methods for fabricating SOI structures: 1) solid-state epitaxial growth, 2) recrystallization of poly-Si by an energetic beam, such as a laser beam, an electron beam, or infrared light, and 3) buried SiO_2 formation in a Si crystal by oxygen implantation or anodic oxidation.

To fabricate 3-D ICs successfully, the wafer temperature during the crystallization should be kept low enough not to destroy or seriously change the performance of devices already fabricated in the lower layers. For this reason, laser or electron-beam recrystallization is thought to be suitable for 3-D IC fabrication. A laser or an electron beam with a diameter of around 100 μm is scanned across the wafer and selectively melts the poly-Si. The time that the poly-Si is molten is on the order of several milliseconds, and the temperature of the substrate remains low.

It is thought to be easier and more practical to recrystallize each small active area than to recrystallize a whole

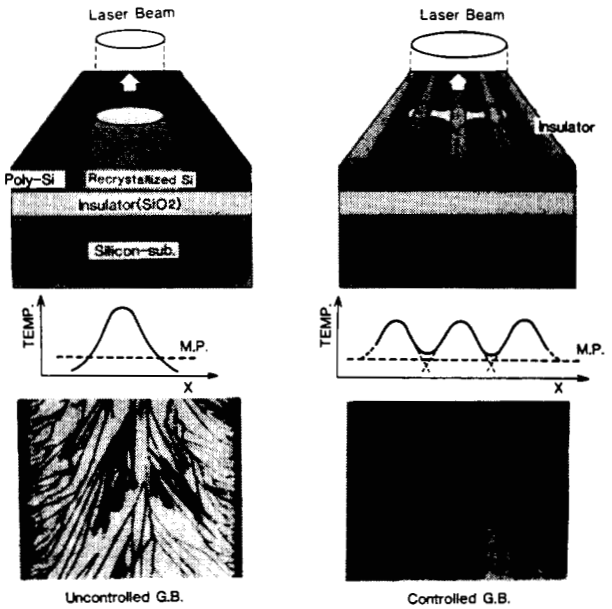


Fig. 5. Thermal profile in poly-Si under laser irradiation and the generation of grain boundaries in the recrystallized layer.

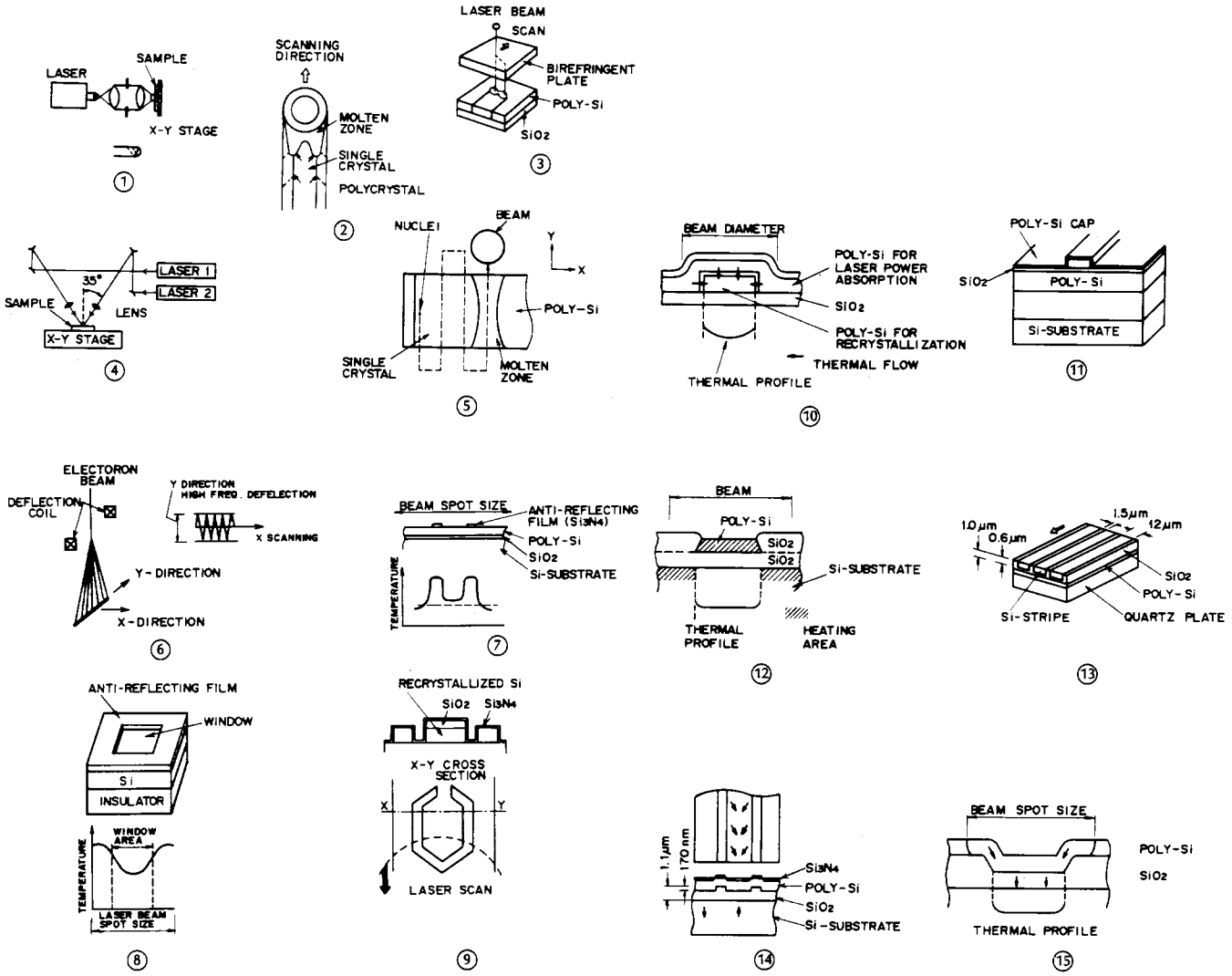


Fig. 6. Various kinds of recrystallization methods to make a preferable thermal profile in the molten zone of the polysilicon. a) By the intensity profile of laser or electron-beam spot ① Beam profile change by using mask [8] (Stanford University, single crystal of 45 μm × 50 μm). ② Donut-type beam by oscillation mode modification [9] (Fujitsu, crystal of 600-nm length). ③ Beam-splitting type [10] (NEC, crystallized area of 20 μm × 1 mm). ④ Double laser beams [11] (Fujitsu, 20 μm; Matsushita, 1.8 mm). ⑤ Electron-beam oscillation—oscillatory growth method [12] (AT&T Bell Labs., 50 μm × 50 μm). ⑥ Quasi-linear electron beam (Toshiba, Tokyo Institute of Technology, 300 μm). b) By patterning the antireflection thin film or absorption layer on the top of the polysilicon (selective recrystallization). ⑦ Stripe-patterned antireflecting thin film [13] (CNET, Mitsubishi, 20 μm × 400 μm). ⑧ Patterned antireflecting thin film [14] (Fujitsu). ⑨ Changing the reflectivity (moated island) [15] (General Electric, 18 μm × 50 μm). ⑩ Indirect heating [16] (Fujitsu, 20 μm × 60 μm). ⑪ Double poly-Si layer recrystallization (Sharp). c) By modifying the heat transfer from molten zone of poly-Si. ⑫ Locos island (edge heating [17] (TI, HP, Mitsubishi, Matsushita, Sharp, 10 μm × 50 μm). ⑬ Buried-stripe structure [18] (NEC, 12 μm × 500 μm). ⑭ Relief structure of SiO_2 (control of thermal flow to a substrate) (Mitsubishi, 8 μm × 200 μm). ⑮ Heat sink structure (Fujitsu).

wafer. The basic concept of recrystallization of restricted active areas is to form two adjacent thermal peaks or a periodic temperature profile, as shown in Fig. 5. Crystallization from one nuclei or polysilicon is possible by this method, and the crystal growth proceeds along the desired direction from one seed, realizing single-crystal growth of the desired area.

Fig. 6 summarizes specific methods of realizing the preferable thermal profile in the molten zone of the polysilicon:

b) obtaining a thermal profile by changing the energy absorption characteristics by patterning the antireflecting thin film or absorption layer on the top of the polysilicon;
c) changing the heat transfer selectively by the material design of the sample structure.

Crystal quality is evaluated by a variety of methods, such as TEM, laser-Raman spectroscopy, and the etch-pit grid method (observation of the pit figure which appears de-

current of MOS transistors fabricated in the recrystallized area.

The characteristics of a "good" transistor are quite comparable with those of a bulk device. The problem is the variation of the characteristics across a wafer, which is one order of magnitude larger than that of the bulk. This variation is primarily caused by two effects: crystal defects, such as small-angle grain boundaries; and poor or no control of the crystal axis. In order to eliminate the crystal defects or to lower their density, experimental techniques are being refined by stabilizing the intensity of the energetic beam, scan speed, and position accuracy. To gain more control of the crystal axis, the so-called lateral-seeding method [7] must be improved.

Other Process Technology Required for Fabricating 3-D ICs

Planarization of the Stacked Surface

3-D stacked structures present problems for recrystallization technology that are not encountered in the fabrication of simple SOI structures [19].

1) The insulator surface and the poly-Si surface, where crystal growth takes place, are not flat.

2) Several kinds of materials with different thermal conductivities are stacked in a complicated manner in the lower layers.

These characteristics perturb the ideal thermal profile and hence disturb smooth crystal growth. To resolve problem 1), surface planarization technology more accurate than that required for conventional 2-D LSIs is required. Planarization by reflow of silicate glass (PSG or BPSG), sputter etching [20], spin-on-glass coating, and etch-back technology with an organic resist material [21] are used to planarize the surface within ± 0.1 μm. Fig. 7 shows the surface planarization obtained by etch-back technology [21].

The technology needed to overcome problem 2) is not established. The methods mainly used are to overcome the fast heat transfer to the bulk by putting an antireflecting material selectively above the area of high thermal conductivity, or to have a thicker inter-insulating layer to reduce the variations in heat transfer across the wafer [19].

Interconnection Material

The interconnection material must not be degraded by the heat treatment employed in subsequent fabrication process steps including the effects of thermal heat shock by energetic beam irradiation of the upper layers. We must use refractive metal or its silicide for interconnections of 3-D ICs [20]. Doped polysilicon can also be used when the circuit design allows for the consequent low propagation speed.

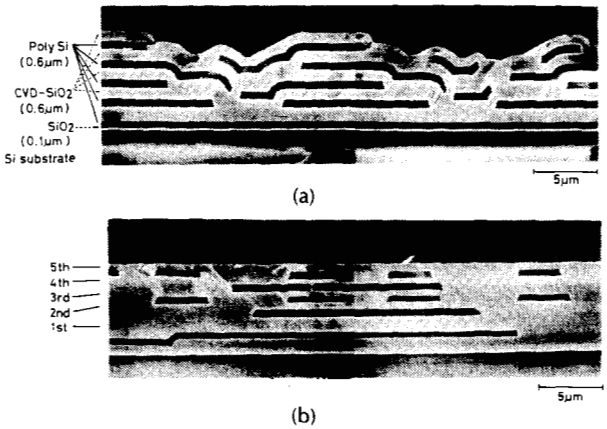


Fig. 7. SEM photographs of cross section of five-level poly-

Via Holes

Fine patterning and etching of via holes to connect the upper and lower active layers are more difficult compared with multilevel metallization in 2-D LSIs because the aspect ratio of the via hole increases to 2 or 3 (i.e., 1-μm square hole with a height of 2–3 μm). Selective growth or deposition of conductive materials and an accurate etching technology are required for the fabrication of via holes in highly packed 3-D LSIs.

Low-Temperature Processing

Process temperatures should be lowered enough not to redistribute the impurities in the lower active layers already fabricated.

Fig. 8 shows an SEM cross-sectional photograph and a schematic drawing of a 3-level, 3-D IC fabricated by using some of the technologies mentioned above [22].

The first layer is fabricated by 3-μm NMOS technology in the bulk; the second layer by 3-μm CMOS technology in the SOI; and the third (SOI) layer by 3-μm NMOS technology. Each layer has its own interconnection and can be operated independently. Each active layer is connected electrically through via holes, and signals can be transferred between the layers.

Fig. 9 shows the TEG (Test Element Group) and the fabrication masks used for testing the 3-D structural device.

Fig. 10 summarizes the *V–I* characteristics and the carrier mobility for MOS transistors fabricated in three stacked layers. The mobilities obtained in the second and third layers are slightly smaller than that of the bulk, but the difference of the mean value is rather small [22]. The mobility of the transistors which show good *I–V* characteristics is almost the same as that of the bulk. The problem is the large variation of the mobility caused by the generation of grain boundaries in the active layer and by differences in the recyrstallized crystal axis, which is not closely controlled in this work.

In future circuits, which may be operated with a power supply voltage of around 3 V, more accurate control of the threshold voltage will be required; hence, a method for crystal axis control, such as lateral seeding, must be developed.

Fabricated Functional Model of the 3-D IC

Several small-scale test devices have been fabricated in the laboratory. Fig. 11 shows an image processor, one of the model systems that might be realized with a 3-D IC. Because this kind of system is conventionally very heavy and massive, its use has been limited. If the image processor with a proper level of intelligence could be realized in a single chip, the range of applications would be considerably widened.

We divided a model system tentatively into two parts and converted each to simplified functional models: a 10-bit lin-

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